

High Efficiency Thyristor

$$V_{RRM} = 1200 \text{ V}$$

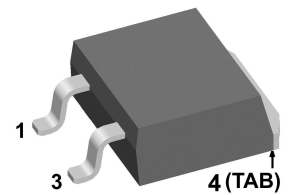
$$I_{TAV} = 15 \text{ A}$$

$$V_T = 1.35 \text{ V}$$

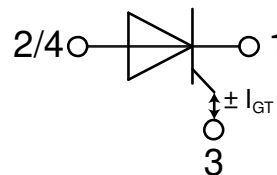
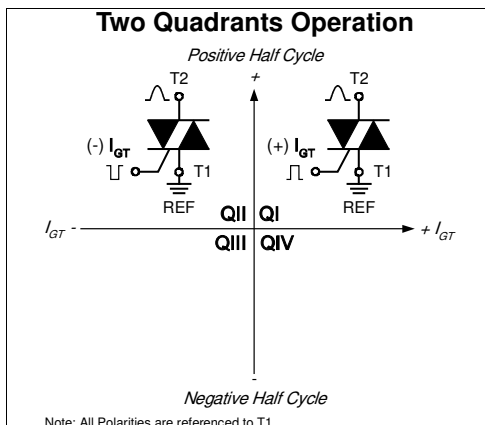
Two Quadrants Operation QI & QII
 Single Thyristor with two gate polarities

Part number

CLA15E1200NPZ



Backside: anode



Features / Advantages:

- Thyristor for line frequency
- Planar passivated chip
- Long-term stability
- Two gate current polarities usable
 - positive -> quadrant I
 - negative -> quadrant II

Applications:

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

Package: TO-263 (D2Pak-HV)

- Industry standard outline
- RoHS compliant
- Epoxy meets UL 94V-0

Disclaimer Notice

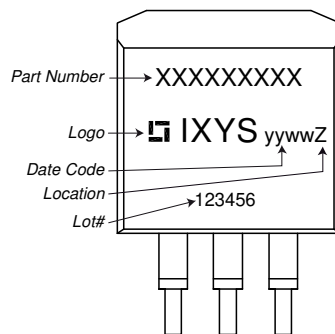
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Thyristor			Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}\text{C}$			1300	V
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}\text{C}$			1200	V
I_{RD}	reverse current, drain current	$V_{R/D} = 1200\text{ V}$	$T_{VJ} = 25^{\circ}\text{C}$		10	μA
		$V_{R/D} = 1200\text{ V}$	$T_{VJ} = 125^{\circ}\text{C}$		1.5	mA
V_T	forward voltage drop	$I_T = 15\text{ A}$	$T_{VJ} = 25^{\circ}\text{C}$		1.35	V
		$I_T = 30\text{ A}$			1.68	V
		$I_T = 15\text{ A}$	$T_{VJ} = 125^{\circ}\text{C}$		1.35	V
		$I_T = 30\text{ A}$			1.79	V
I_{TAV}	average forward current	$T_C = 120^{\circ}\text{C}$	$T_{VJ} = 150^{\circ}\text{C}$		15	A
$I_{T(RMS)}$	RMS forward current	180° sine			23	A
V_{T0}	threshold voltage	} for power loss calculation only	$T_{VJ} = 150^{\circ}\text{C}$		0.89	V
r_T	slope resistance				30	m Ω
R_{thJC}	thermal resistance junction to case				0.95	K/W
R_{thCH}	thermal resistance case to heatsink			0.3		K/W
P_{tot}	total power dissipation		$T_C = 25^{\circ}\text{C}$		130	W
I_{TSM}	max. forward surge current	$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}\text{C}$		170	A
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$		185	A
		$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 150^{\circ}\text{C}$		145	A
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$		155	A
I^2t	value for fusing	$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}\text{C}$		145	A ² s
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$		140	A ² s
		$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 150^{\circ}\text{C}$		105	A ² s
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$		100	A ² s
C_J	junction capacitance	$V_R = 400\text{ V}$ $f = 1\text{ MHz}$	$T_{VJ} = 25^{\circ}\text{C}$		4	pF
P_{GM}	max. gate power dissipation	$t_p = 30\text{ }\mu\text{s}$	$T_C = 150^{\circ}\text{C}$		5	W
		$t_p = 300\text{ }\mu\text{s}$			1	W
P_{GAV}	average gate power dissipation				0.2	W
$(di/dt)_{cr}$	critical rate of rise of current	$T_{VJ} = 150^{\circ}\text{C}; f = 50\text{ Hz}$ repetitive, $I_T = 45\text{ A}$			150	A/ μs
		$t_p = 200\text{ }\mu\text{s}; di_G/dt = 0.3\text{ A}/\mu\text{s};$ $I_G = 0.3\text{ A}; V = \frac{2}{3} V_{DRM}$ non-repet., $I_T = 15\text{ A}$			500	A/ μs
$(dv/dt)_{cr}$	critical rate of rise of voltage	$V = \frac{2}{3} V_{DRM}$	$T_{VJ} = 150^{\circ}\text{C}$		500	V/ μs
		$R_{GK} = \infty$; method 1 (linear voltage rise)				
V_{GT}	gate trigger voltage	$V_D = 6\text{ V}$	$T_{VJ} = 25^{\circ}\text{C}$		1.3	V
			$T_{VJ} = -40^{\circ}\text{C}$		1.6	V
I_{GT}	gate trigger current	$V_D = 6\text{ V}$	$T_{VJ} = 25^{\circ}\text{C}$		± 20	mA
			$T_{VJ} = -40^{\circ}\text{C}$		± 40	mA
V_{GD}	gate non-trigger voltage	$V_D = \frac{2}{3} V_{DRM}$	$T_{VJ} = 150^{\circ}\text{C}$		0.2	V
I_{GD}	gate non-trigger current				± 1	mA
I_L	latching current	$t_p = 10\text{ }\mu\text{s}$	$T_{VJ} = 25^{\circ}\text{C}$		70	mA
		$I_G = 0.3\text{ A}; di_G/dt = 0.3\text{ A}/\mu\text{s}$				
I_H	holding current	$V_D = 6\text{ V}$ $R_{GK} = \infty$	$T_{VJ} = 25^{\circ}\text{C}$		70	mA
t_{gd}	gate controlled delay time	$V_D = \frac{1}{2} V_{DRM}$	$T_{VJ} = 25^{\circ}\text{C}$		2	μs
		$I_G = 0.3\text{ A}; di_G/dt = 0.3\text{ A}/\mu\text{s}$				
t_q	turn-off time	$V_R = 100\text{ V}; I_T = 15\text{ A}; V = \frac{2}{3} V_{DRM}$ $T_{VJ} = 125^{\circ}\text{C}$ $di/dt = 10\text{ A}/\mu\text{s}$ $dv/dt = 20\text{ V}/\mu\text{s}$ $t_p = 200\text{ }\mu\text{s}$		150		μs

Package TO-263 (D2Pak-HV)		Ratings				
Symbol	Definition	Conditions	min.	typ.	max.	Unit
I_{RMS}	RMS current	per terminal			35	A
T_{VJ}	virtual junction temperature		-40		150	°C
T_{op}	operation temperature		-40		125	°C
T_{stg}	storage temperature		-40		150	°C
Weight				1.5		g
F_C	mounting force with clip		20		60	N
$d_{Spp/App}$	creepage distance on surface / striking distance through air	terminal to terminal	4.2			mm
$d_{Spb/Apb}$		terminal to backside	4.7			mm

Product Marking



Part description

- C = Thyristor (SCR)
- L = High Efficiency Thyristor
- A = (up to 1200V)
- 15 = Current Rating [A]
- E = Single Thyristor with two gate polarities
- 1200 = Reverse Voltage [V]
- N = Three Quadrants operation: QI - QIII
- PZ = TO-263AB (D2Pak) (2HV)

Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	CLA15E1200NPZ-TRL	CLA15E1200NPZ-TRL	Tape & Reel	800	517595
Alternative	CLA15E1200NPZ-TUB	CLA15E1200NPZ	Tube	50	523755

Similar Part	Package	Voltage class
CLA15E1200NPB	TO-220AB (3)	1200

Equivalent Circuits for Simulation

* on die level

$T_{VJ} = 150^{\circ}\text{C}$



Thyristor

$V_{0\ max}$	threshold voltage	0.89	V
$R_{0\ max}$	slope resistance *	27	mΩ



Outlines TO-263 (D2Pak-HV)



Dim.	Millimeter		Inches	
	min	max	min	max
A	4.06	4.83	0.160	0.190
A1	typ. 0.10		typ. 0.004	
A2	2.41		0.095	
b	0.51	0.99	0.020	0.039
b2	1.14	1.40	0.045	0.055
c	0.40	0.74	0.016	0.029
c2	1.14	1.40	0.045	0.055
D	8.38	9.40	0.330	0.370
D1	8.00	8.89	0.315	0.350
D2	2.3		0.091	
E	9.65	10.41	0.380	0.410
E1	6.22	8.50	0.245	0.335
e	2,54 BSC		0,100 BSC	
e1	4.28		0.169	
H	14.61	15.88	0.575	0.625
L	1.78	2.79	0.070	0.110
L1	1.02	1.68	0.040	0.066
W	typ. 0.02	0.040	typ. 0.0008	0.002

All dimensions conform with and/or within JEDEC standard.

