DATA SHEET

CLA Series: Silicon Limiter Diodes and Ceramic Hermetic Packaged Devices

Applications

- LNA receiver protection
- Commercial and defense radar

Features

- Established limiter diode process
- High power, mid-range, and cleanup designs
- Low insertion loss: 0.1 dB @ 10 GHz
- Peak power handling to +74 dBm
- Ultra low spike leakage power
- Tight control of I layer base width

Description

The Isolink CLA series of silicon limiter diodes provides passive receiver protection over a wide range of frequencies from 100 MHz to over 20 GHz. These devices use a well-established silicon technology resulting in high resistivity and tightly controlled base width PIN limiter diodes. Limiter circuits using these devices perform with strong limiting action and low loss.

The CLA series consists of ten individual chip designs of different intrinsic region base widths and capacitances designed to accommodate multi-stage limiter applications. The mesa-constructed, thin base width, low capacitance CLA4601 series, CLA4602 series, CLA4604 series, and CLA4605 series are designed for low-level and cleanup applications. The CLA4603 series, CLA4606 series, CLA4607 series, CLA4608 series and CLA4610 series are planar designs designated for high-power and mid-range applications.

The CLA4609 series thick base width mesa diode is designed for coarse limiter-stage applications.

The absolute maximum ratings of the CLA diode series are provided in Table 1. Electrical specifications are specified in Table 2. Typical performance characteristics are provided in Table 3 and Figures 1 through 4.

Table 1. CLA Series Absolute Maximum Ratings[1]

Parameter	Symbol	Minimum	Typical	Maximum	Units
Power dissipation	P_{DIS}			$\frac{Maximum\ T_J\ -\ Case\ Temp}{Thermal\ Resistance_{junction-to-case}}$	W
Reverse voltage	V_R			Minimum rated breakdown voltage	V
Forward current	I_F			200	mA
Junction temperature	T_J	–65		+175	°C
Storage temperature	T_{STG}	–65		+200	°C
Electrostatic discharge:					
Charged Device Model (CDM), Class 4				1000	V
Human Body Model (HBM), Class 1C				1000	V
Machine Model (MM), Class A				150	V

1 Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

***ESD HANDLING**: Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD when handling or transporting. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD handling precautions should be used at all times.*

Table 2. CLA Series Electrical Specifications[1,2] (1 of 2)

Part Number	Breakdown Voltage (V) Min to Max	I Region (µm) Nominal	Total Capacitance (C_T) @ 0 V (pF) Typical	Total Capacitance (C_T) @ 6 V (pF) Maximum	Series Resistance (RS) @ 10 mA (Ω) Typical	Minority Carrier Lifetime (TL) @ 10 mA (ns) Typical	Thermal Resistance (θ) [3] Average (°C/W) Maximum
CLA4601-203	15 to 30	1.0	0.37	0.35	2.0	5	150
CLA4601-210	15 to 30	1.0	0.37	0.35	2.0	5	140
CLA4601-219	15 to 30	1.0	0.37	0.35	2.0	5	200
CLA4601-240	15 to 30	1.0	0.37	0.35	2.0	5	200
CLA4602-203	15 to 30	1.0	0.45	0.40	1.5	5	110
CLA4602-210	15 to 30	1.0	0.45	0.40	1.5	5	100
CLA4602-219	15 to 30	1.0	0.45	0.35	1.5	5	160
CLA4602-240	15 to 30	1.0	0.45	0.40	1.5	5	160
CLA4603-203	20 to 45	1.5	0.45	0.35	1.5	5	130
CLA4603-210	20 to 45	1.5	0.45	0.40	1.5	5	120
CLA4603-219	20 to 45	1.5	0.45	0.40	1.5	5	180
CLA4603-240	20 to 45	1.5	0.45	0.35	1.5	5	180
CLA4604-203	30 to 60	2.0	0.37	0.30	2.0	7	130
CLA4604-210	30 to 60	2.0	0.37	0.35	2.0	7	120
CLA4604-219	30 to 60	2.0	0.37	0.30	2.0	7	160
CLA4604-240	30 to 60	2.0	0.37	0.30	2.0	7	180

Table 2. CLA Series Electrical Specifications[1,2] (2 of 2)

Part Number	Breakdown Voltage (V) Min to Max	I Region (µm) Nominal	Total Capacitance (C_T) @ 0 V (pF) Typical	Total Capacitance (C_T) @ 6 V (pF) Maximum	Series Resistance (RS) @ 10 mA (Ω) Typical	Minority Carrier Lifetime (TL) @ 10 mA (ns) Typical	Thermal Resistance (θ)[3] Average (°C/W) Maximum
CLA4605-203	30 to 60	2.0	0.45	0.30	1.5	7	100
CLA4605-210	30 to 60	2.0	0.45	0.40	1.5	7	90
CLA4605-219	30 to 60	2.0	0.45	0.40	1.5	7	150
CLA4605-240	30 to 60	2.0	0.45	0.35	1.5	7	150
CLA4606-203	45 to 75	2.5	0.45	0.35	1.5	10	110
CLA4606-210	45 to 75	2.5	0.45	0.40	1.5	10	100
CLA4606-219	45 to 75	2.5	0.45	0.40	1.5	10	160
CLA4606-240	45 to 75	2.5	0.45	0.35	1.5	10	106
CLA4607-203	120 to 180	7.0	0.45	0.35 @ 38 V	1.5	50	70
CLA4607-210	120 to 180	7.0	0.45	0.40 @ 38 V	1.5	50	60
CLA4607-219	120 to 180	7.0	0.45	0.40 @ 38 V	1.5	50	120
CLA4607-240	120 to 180	7.0	0.45	0.35 @ 38 V	1.5	50	120
CLA4608-203	120 to 180	7.0	0.85	0.75 @ 38 V	0.5	100	45
CLA4608-210	120 to 180	7.0	0.85	0.75 @ 38 V	0.5	100	35
CLA4608-219	120 to 180	7.0	0.85	0.70 @ 38 V	0.5	100	100
CLA4608-240	120 to 180	7.0	0.85	0.70 @ 38 V	0.5	100	100
CLA4609-203	250 (Min)	20.0	0.51	0.40	1.0	1175	45
CLA4609-210	250 (Min)	20.0	0.51	0.45	1.0	1175	35
CLA4609-219	250 (Min)	20.0	0.51	0.40	1.0	1175	100
CLA4609-240	250 (Min)	20.0	0.51	0.40	1.0	1175	100
CLA4610-203	80 to 120	4.5	0.38	0.40	1.7	20	182
CLA4610-210	80 to 120	4.5	0.38	0.45	1.7	20	81
CLA4610-219	80 to 120	4.5	0.38	0.40	1.7	20	152
CLA4610-240	80 to 120	4.5	0.38	0.40	1.7	20	163

1 Performance is guaranteed only under the conditions listed in this table and is not guaranteed over the full operating or storage temperature ranges. Operation at elevated temperatures may reduce reliability of the device.

2 T_{OP} = +25 °C, CJ measured at 1 MHz, RS measured at 500 MHz, CW thermal resistance for infinite heat sink, unless otherwise noted.

3 Thermal resistance is calculated from the measured power dissipation @ f = 2.6 GHz, T_J max = 175 °C and T_{CASE} = 85 °C

Table 3. Typical Performance @ 25 °C @ 2.6 GHz, Z_0 = 50 Ω[1]

Part Number	Insertion Loss @ –10 dBm (dB)	CW Input Power for 1 dB Insertion Loss (dBm)	Maximum CW Input Power (dBm)	Maximum Pulsed Input Power (dBm) [2]	Output @ Maximum Pulsed Input (dBm) [2]	Recovery Time (ns) [3]	Spike Leakage (ergs) [4]
CLA4601	0.1	12	36	65	21	5	Note 5
CLA4602	0.1	12	36	65	24	5	Note 5
CLA4603	0.1	10	38	67	22	5	Note 5
CLA4604	0.1	11	40	70	24	5	Note 5
CLA4605	0.1	12	40	70	27	5	0.08
CLA4606	0.1	14	41	71	27	5	0.03
CLA4607	0.1	26	43	73	39	5	0.21
CLA4608	0.2	26	43	73	44	5	0.15
CLA4609	0.3	37	44	74	50	5	25.77
CLA4610	0.1	24	40	57	32	5	Note 5

1 Diode chip is mounted on a 0.5 oz Cu PC board using 1 to 2 mils of conductive epoxy. Bond wire connections are made with 0.8 mil Au wire. Limiter configured with shunt connected diode and 22 nH ground return and 100 pF DC blocking capacitors.

2 Pulsed power measurements taken at 1 µs pulse width, @ f = 10 KHz, and 0.1% duty cycle.

3 Recovery time represents the transition time from the high-loss state to the low-loss state following the removal of a high-power input. It is defined as the time from the end of the high-power pulse to the time when insertion loss has returned to within 3 dB of the quiescent (low-power) state.

4 Spike Leakage (ergs) = $t_s \times P_s \times 10^7$ where t_s is the spike width at the half-power point (in seconds) and P_S is the maximum spike amplitude in watts.

5 Not detectable under current test conditions described in Note 2.

Typical Performance Characteristics
(Tested at 25 °C, Board and Connector Loss Are Not De-Embedded)

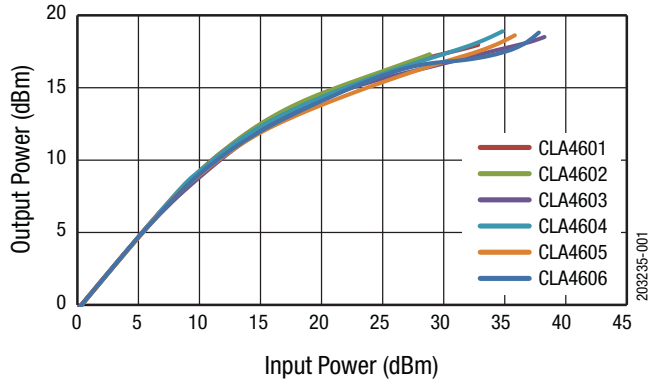


Figure 1. CLA4601 to CLA4606 CW Output vs Input Power

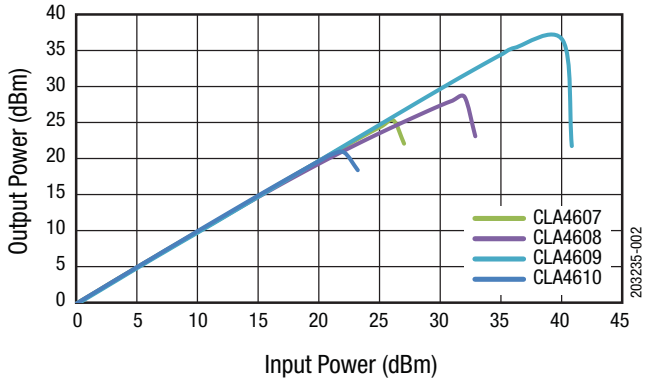


Figure 2. CLA4607 to CLA4610 CW Output vs Input Power

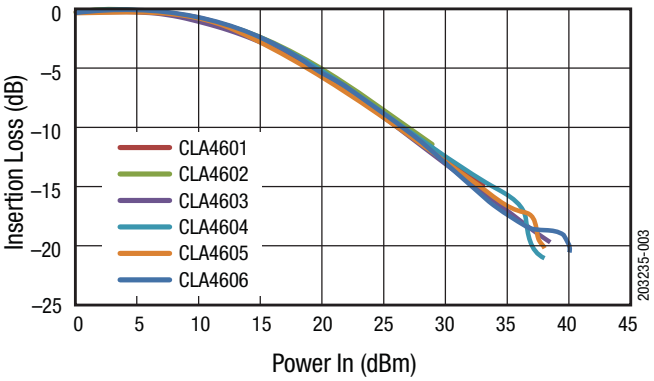


Figure 3. LCA4601 to CLA4606 Insertion Loss vs CW Input Power

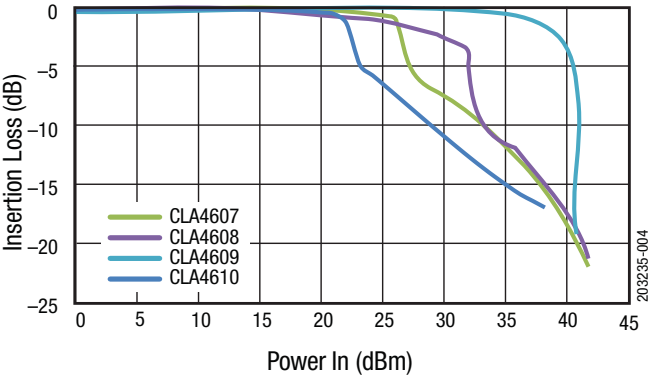


Figure 4. CLA4607 to CLA4610 Insertion Loss vs CW Input Power

Technical Description

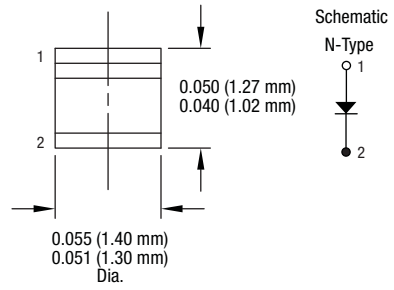
The limiter can be used in various configurations to meet different application requirements. For example, in low-to-medium power applications, a single-stage limiter can be used. In this case, an inductor must be used in parallel with the limiter to create a DC return choke.

A dual-stage limiter design can handle much higher power. The first stage works as the coarse stage (CLA4607 through CLA4610), and the second stage works as the cleanup stage (CLA4601 through CLA4606).

Package dimension drawings are provided in Figures 5 through 8.

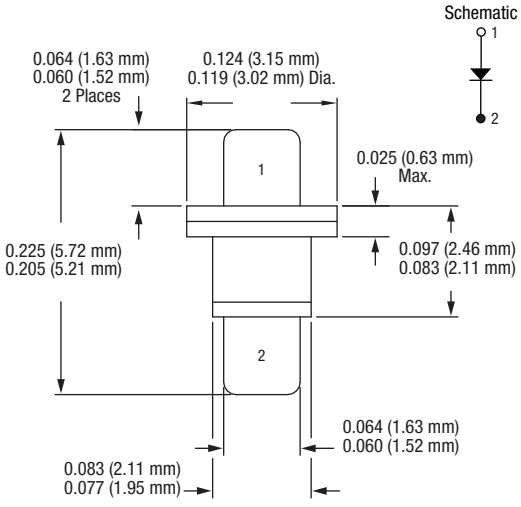
For detailed application information, refer to the Skyworks Application Note: *PIN Limiter Diodes in Receiver Protectors* at www.skyworksinc.com.

Package Outline Drawings



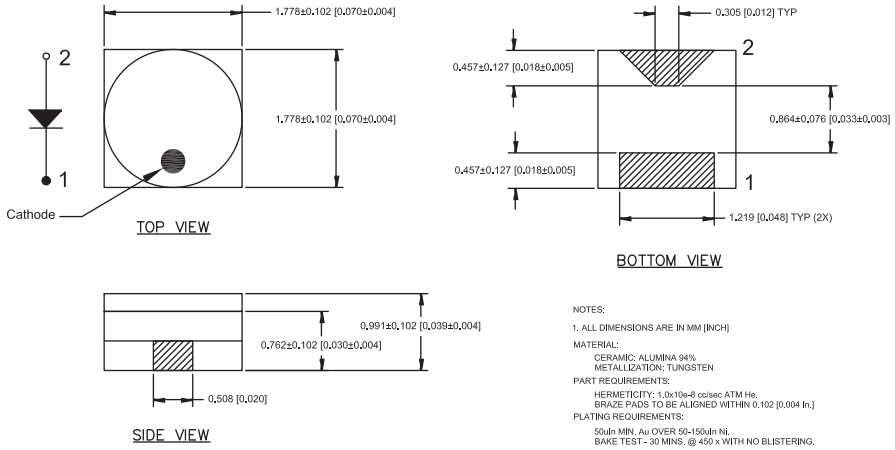
Dimensions are in inches (millimeters shown in parentheses) 203235-005

Figure 5. -203 Package

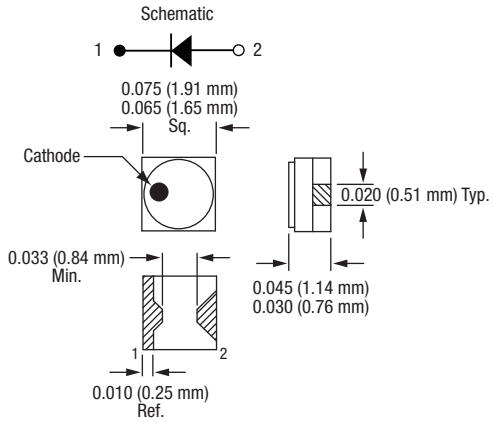


Dimensions are in inches (millimeters shown in parentheses) 203235-006

Figure 6. -210 Package



Version A

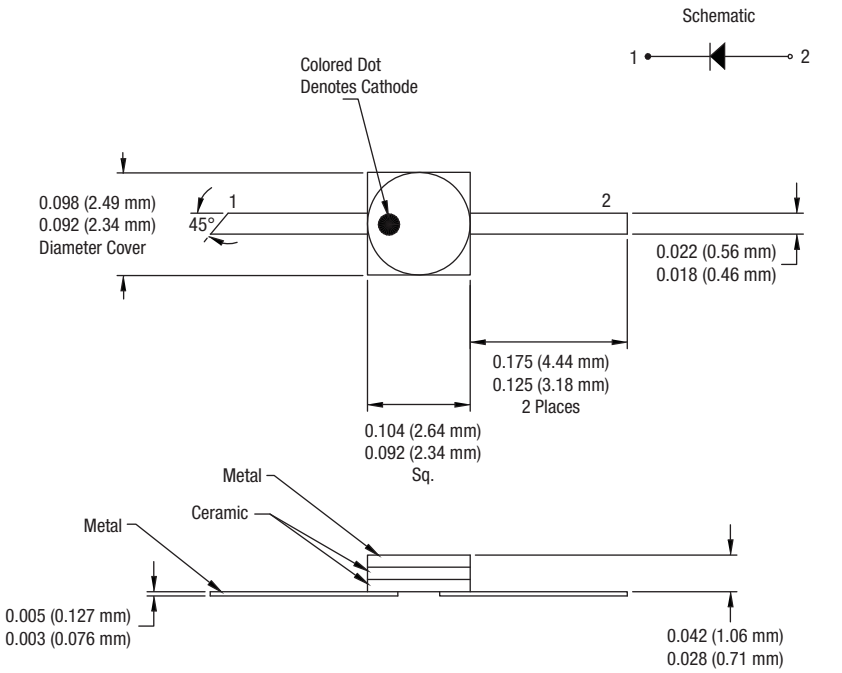


Dimensions are in inches (millimeters shown in parentheses)

Version B

203235-007

Figure 7. -219 Package



Dimensions are in inches (millimeters shown in parentheses)

203235-008

Figure 8. -240 Package