DATA SHEET

CLA4611-085LF: Surface-Mount Limiter Diode

Applications

- Low-loss, high-power limiters
- Receiver protectors

Features

- Low small signal insertion loss: 0.3 dB
- Typical threshold level: +25 dBm
- Low capacitance: 0.25 pF
- Low-profile, ultra-miniature QFN (3-pin, 2 x 2 mm) package (MSL1, 260 °C per JEDEC J-STD-020)

Skyworks Green™ products are compliant with all applicable legislation and are halogen-free. For additional information, refer to *Skyworks Definition of Green™*, document number SQ04–0074.

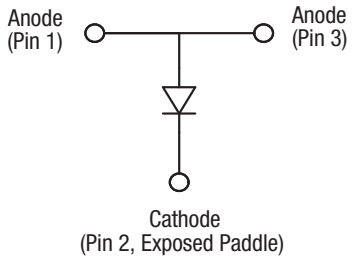


Figure 1. CLA4611-085LF Block Diagram

Description

The CLA4611-085LF is a surface-mountable, low-capacitance silicon PIN limiter diode designed as a shunt connected PIN diode for high power limiter applications from 10 MHz to over 6 GHz.

Maximum resistance at 10 mA is 1.2 Ω and maximum capacitance at 38 V is 0.25 pF (typical). The combination of low junction capacitance, low parasitic inductance, low thermal resistance, and nominal 12 µm I-region width, makes the CLA4611-085LF useful in large signal limiter applications. The threshold level is +25 dBm, nominal.

A block diagram of the CLA4611-085LF is shown in Figure 1. The absolute maximum ratings of the CLA4611-085LF are provided in Table 1. Electrical specifications are provided in Table 2.

Typical performance characteristics of the CLA4611-085LF are provided in Table 3 and illustrated in Figure 4.

Table 1. CLA4611-085LF Absolute Maximum Ratings[1]

Parameter	Symbol	Minimum	Maximum	Units
Reverse voltage	V_R		180	V
Forward current @ 25 °C	I_F		200	mA
CW power dissipation @ 85 °C	P_D		0.7	W
Peak pulse power dissipation @ 85 °C (10% duty cycle)			7	W
Storage temperature	T_{STG}	-65	+200	°C
Junction temperature	T_J		175	°C
Operating temperature	T_A	-55	+150	°C
Electrostatic discharge:	ESD			
Charged Device Model (CDM), Class 4			1000	V
Human Body Model (HBM), Class 1B			500	V
Machine Model (MM), Class A			100	V

1 Exposure to maximum rating conditions for extended periods may reduce device reliability. There is no damage to device with only one parameter set at the limit and all other parameters set at or below their nominal value. Exceeding any of the limits listed here may result in permanent damage to the device.

ESD HANDLING: *Although this device is designed to be as robust as possible, electrostatic discharge (ESD) can damage this device. This device must be protected at all times from ESD when handling or transporting. Static charges may easily produce potentials of several kilovolts on the human body or equipment, which can discharge without detection. Industry-standard ESD handling precautions should be used at all times.*

Table 2. CLA4611-085LF Electrical Specifications[1] (T_A = +25 °C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
Reverse current	I_R	V_R = 120 V			10	µA
Capacitance	C_T	f = 1 MHz, V_R = 38 V		0.25	0.35	pF
Series resistance	R_S	f = 500 MHz, I_F = 10 mA		0.75	1.2	Ω
Carrier lifetime	T_L	I_F = 10 mA		300		ns
I region width	W			12		µm
CW thermal resistance	θ_{JC}	Junction-to-case		132		°C/W
Peak thermal resistance	θ_P	Single 1 µs pulse width, junction-to-case (0.01% duty cycle)		0.15		°C/W

1 Performance is guaranteed only under the conditions listed in this table.

Table 3. Typical Performance @ 25 °C

Part Number	Insertion Loss @ -10 dBm (dB)	Input Power for 1 dB Loss (dBm)	Maximum Pulsed Input Power (dBm)	Output @ Maximum Pulsed Input (dBm)	Maximum CW Input power (W)	Recovery Time (ns)
CLA4611-085LF	0.3	25	66	42	10	300

Notes:
Limiter power results @ 1 GHz for shunt connected, single limiter diode and DC return in 50 Ω line.
Maximum pulsed power for 1 µs pulse and 0.01% duty factor with chip @ 25 °C heat sink. Derate linearly to 0 W @ 175 °C.
Maximum CW input power @ 25 °C heat sink. Derate linearly to 0 W @ 175 °C.
Recovery time to insertion loss from limiting state.

Functional Description

The PIN limiter diode can be described as an incident power controlled, RF variable resistor. When there is no large input signal present, the impedance of the limiter diode is at its maximum, which produces minimum insertion loss, typically less than 0.2 dB. The presence of a large input signal temporarily forces the impedance of the diode to a much lower value, which produces an impedance mismatch that reflects the majority of the input signal power back towards its source.

During the limiting process, a DC current is generated by the PIN limiter diode. The current is not the result of rectification, but is the result of charge carriers being forced into the I layer by the forward alternations of the large input signal. A complete path must be provided for this current or the diode is not capable of limiting. Therefore, an RF choke or similar structure must be provided to complete the path for DC current flow.

The DC block capacitors shown in Figure 2 are optional; they protect the limiter diode from external DC voltage that may be present in the source or load circuits.

A cross section of the suggested printed circuit board design is shown in Figure 3. The via shown in this view is critical, both for electrical performance and for thermal performance. It is recommended that several vias should be placed under the entire footprint of the exposed paddle (pin 2) to minimize both electrical inductance to the system ground and thermal resistance to the system heat sink.

For more information about the operation of limiter diodes, refer to the Skyworks Application Note, *PIN Limiter Diodes in Receiver Protectors*, document number 200480.

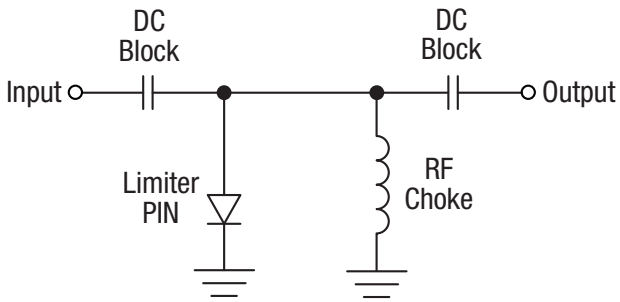


Figure 2. Single Stage Limiter Circuit

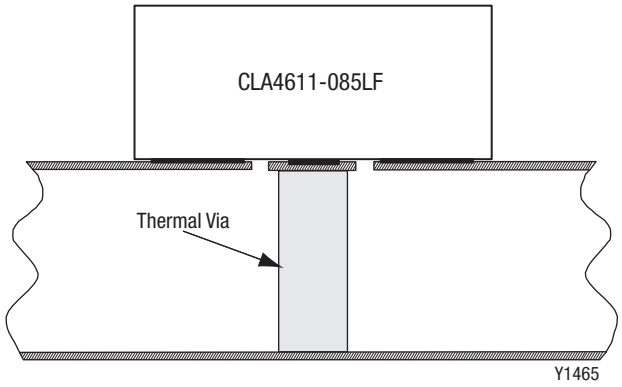


Figure 3. Cross-Sectional View of Suggested Printed Circuit Board

Typical Performance Characteristics

(T_A = 25 °C, Unless Otherwise Noted)

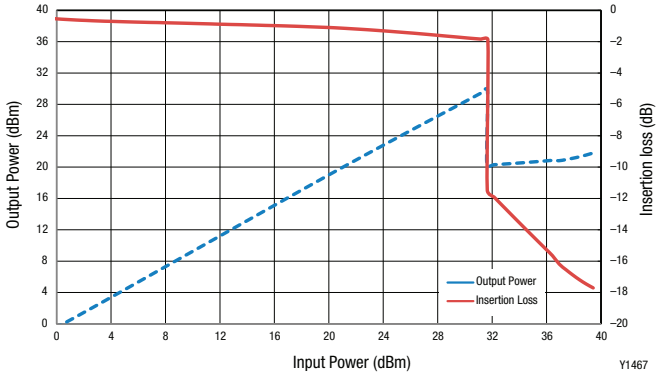


Figure 4. Insertion Loss and Output Power vs Input Power (f = 1.0 GHz, Board Loss Included)

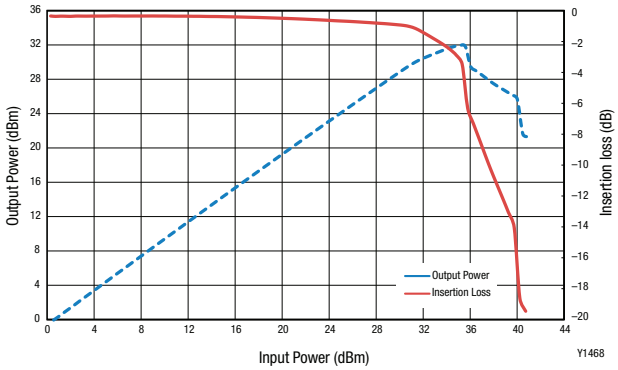


Figure 5. Insertion Loss and Output Power vs Input Power (f = 2.6 GHz, Board Loss Included)

High-Power Limiter Design Application

The CLA4611-085LF PIN limiter diode is designed for shunt applications in receiver protection power limiter circuits. Compared to other surface mount packages, the design of the QFN package produces lower thermal resistance and also reduces the effects of the parasitic inductance of the anode bond wires.

A cross-sectional view of the CLA4611-085LF PIN limiter diode is shown in Figure 5. The cathode of the die is soldered directly to the top of the exposed paddle. This paddle is composed of copper, so its thermal resistance is very low.

The copper ground paddle minimizes the total thermal resistance between the I layer, which is the location where most heat is generated under normal operation, and the surface to which the package is mounted. Minimal thermal resistance between the I layer and the external environment minimizes junction temperature.

The electrically equivalent circuit of the CLA4611-085LF PIN limiter diode is shown in Figure 6. The inductances of pins 1 and 2, as well as the inductances of the bond wires are in series with the input and output transmission lines of the external circuit rather than the portion of the circuit that contains the shunt PIN limiter diode.

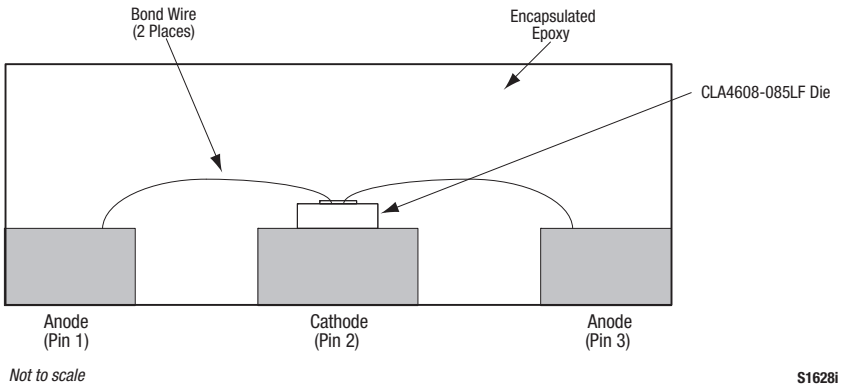


Figure 5. Cross-Sectional View of the CLA4611-085LF

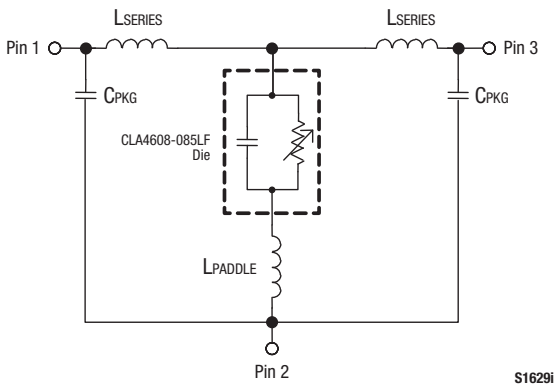


Figure 6. CLA4611-085LF Electrically Equivalent Circuit

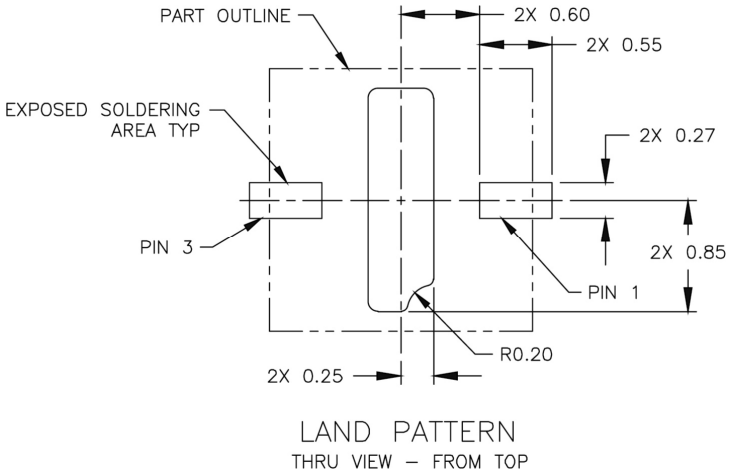


Figure 7. CLA4611-085LF PCB Layout Footprint

Package Dimensions

The PCB layout footprint for the CLA4611-085LF is shown in Figure 7. Typical part markings are shown in Figure 8. Package dimensions are provided in Figure 9, and Figure 10 provides the tape and reel dimensions.

Package and Handling Information

Instructions on the shipping container label regarding exposure to moisture after the container seal is broken must be followed. Otherwise, problems related to moisture absorption may occur when the part is subjected to high temperature during solder assembly.

The CLA4611-085LF is rated to Moisture Sensitivity Level 1 (MSL1) at 260 °C. It can be used for lead or lead-free soldering. For additional information, refer to the Skyworks Application Note, *Solder Reflow Information*, document number 200164.

Care must be taken when attaching this product, whether it is done manually or in a production solder reflow environment. Production quantities of this product are shipped in a standard tape and reel format.

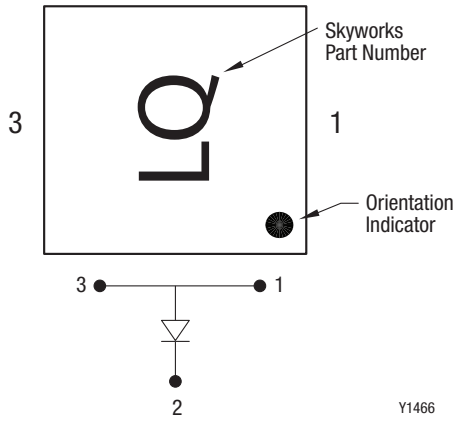
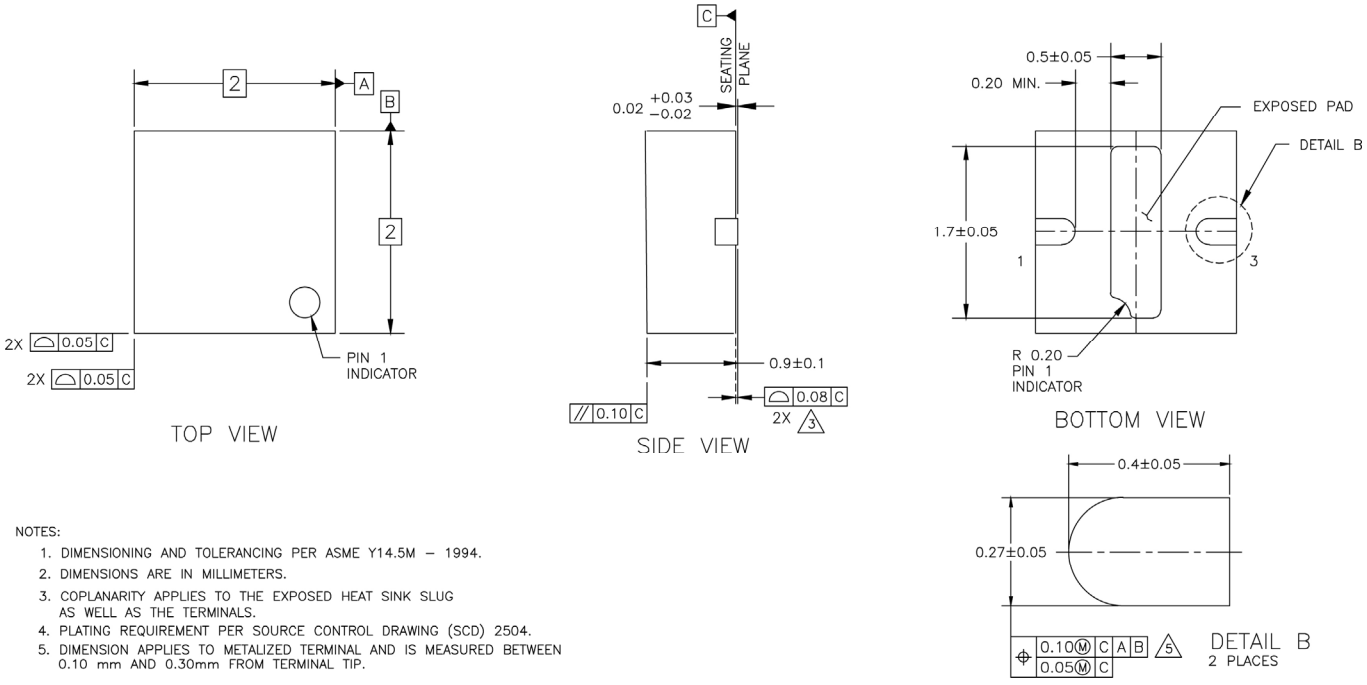


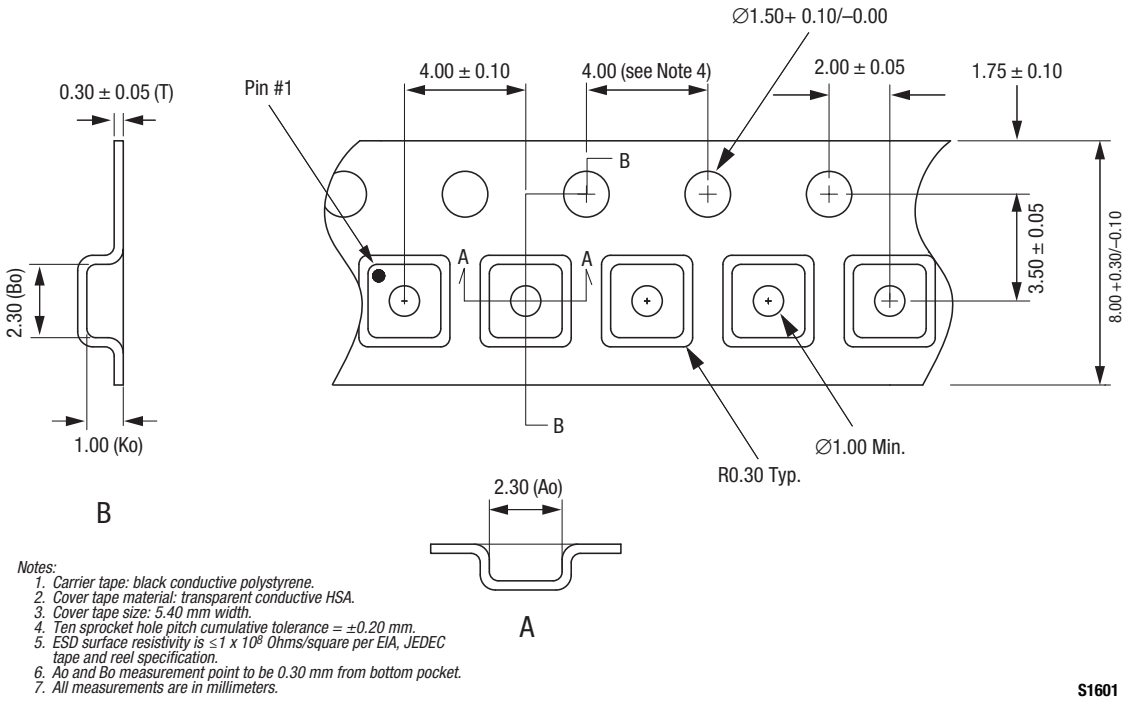
Figure 8. Typical Part Markings (Top View)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M – 1994.
2. DIMENSIONS ARE IN MILLIMETERS.
3. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
4. PLATING REQUIREMENT PER SOURCE CONTROL DRAWING (SCD) 2504.
5. DIMENSION APPLIES TO METALIZED TERMINAL AND IS MEASURED BETWEEN 0.10 mm AND 0.30mm FROM TERMINAL TIP.

Figure 9. CLA4611-085LF Package Dimension Drawing



Notes:
1. *Carrier tape: black conductive polystyrene.*
2. *Cover tape material: transparent conductive HSA.*
3. *Cover tape size: 5.40 mm width.*
4. *Ten sprocket hole pitch cumulative tolerance = ±0.20 mm.*
5. *ESD surface resistivity is ≤1 x 10^8 Ohms/square per EIA, JEDEC tape and reel specification.*
6. *Ao and Bo measurement point to be 0.30 mm from bottom pocket.*
7. *All measurements are in millimeters.*

Figure 10. CLA4611-085LF Tape and Reel Dimensions