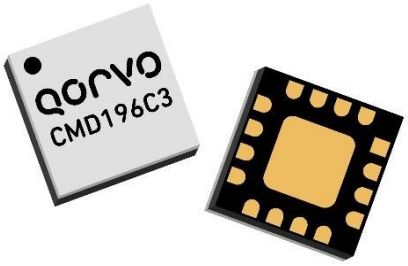
CMD196C3

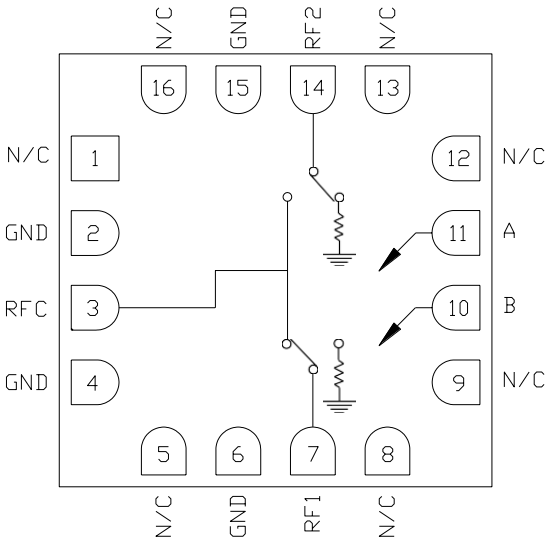
DC-18 GHz SPDT Non-reflective Switch

Product Overview

The CMD196C3 is a general purpose broadband high isolation non-reflective MMIC SPDT switch housed in a leadless 3x3 mm surface mount package. Covering DC to 18 GHz, the CMD196C3 features a low insertion loss of 1.5 dB and high isolation of 46 dB at 8 GHz. The CMD196C3 operates using complementary control voltage logic lines of 0/-5 V and requires no bias supply.



Functional Block Diagram



Key Features

- Low Loss Broadband Performance
- High Isolation
- Fast Switching Speed
- Non-Reflective Design
- Pb-Free RoHs Compliant 3x3 SMT Package

Ordering Information

Part No.	Description
CMD196C3	Tape and Reel, Qty=100

Electrical Performance (V_{ctl} = 0/-5 V, T_A = 25° C, F = 8 GHz)

Parameter	Min	Typ	Max	Units
Frequency Range		DC - 18		GHz
Insertion Loss		1.5		dB
Isolation		46		dB
Return Loss - On State		17		dB
Return Loss RF1, RF2 - Off State		17		dB
Input P1dB		23		dBm
Switching Characteristics tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)		 1.8 11/4		 ns ns

Absolute Maximum Ratings

Parameter	Rating
RF Input Power	+27 dBm
Control Voltage Range (A, B)	+0.5V to -7.5V
Channel Temperature, Tch	150° C
Operating Temperature	-40 to 85° C
Storage Temperature	-55 to 150° C
Thermal Resistance, Q_{JC} (insertion loss path)	103° C/W
Thermal Resistance, Q_{JC} (terminated path)	258° C/W
Terminated Power Level (V_{ctl} = -5 V, CW)	+24 dBm

Exceeding any one or combination of the maximum ratings may cause permanent damage to the device.

Control Voltages

State	Bias Condition
Low	0 to -0.5V @ 1 uA Typ
High	-3V @ 1 uA Typ to -7V @ 6 uA Typ

Truth Table

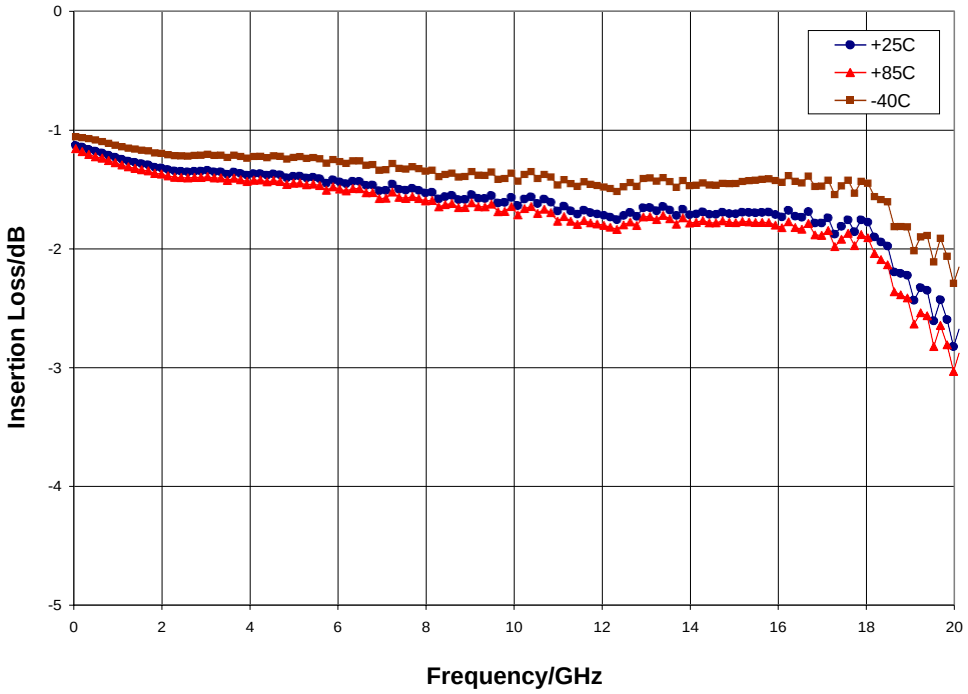
Control Input		Signal Path State	
A	B	RFC to RF1	RFC to RF2
High	Low	On	Off
Low	High	Off	On

Electrical Specifications (V_{ctl} = 0/-5 V, T_A = 25° C)

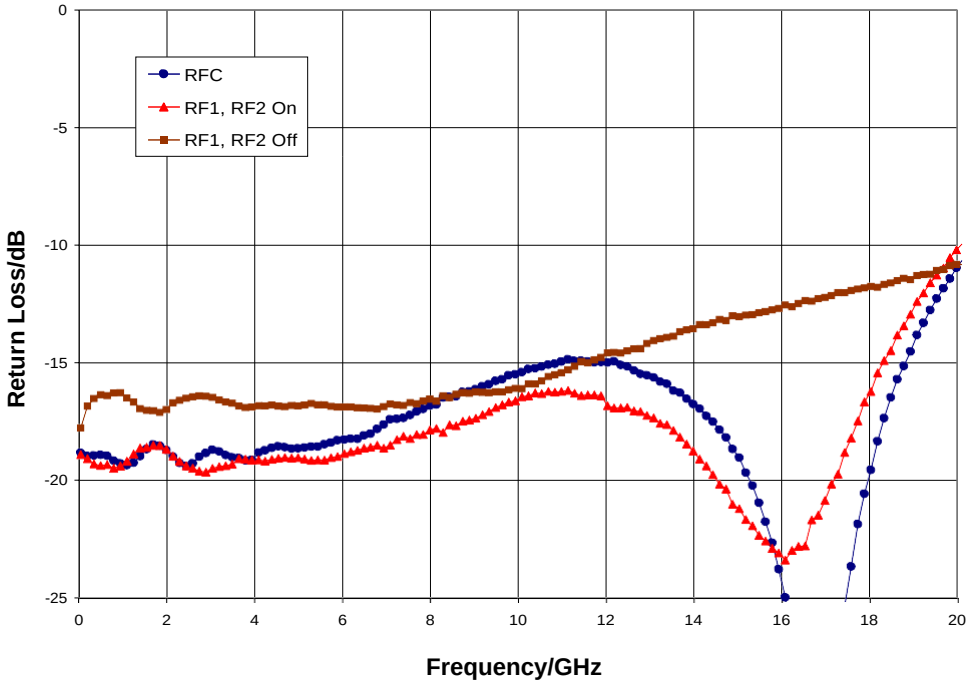
Parameter	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Units
Frequency Range		DC - 8			DC - 14			DC - 18		GHz
Insertion Loss		1.5	1.9		1.7	2.1		1.8	2.2	dB
Isolation	41	46		40	45		32	37		dB
Return Loss - On State		18			15			17		dB
Return Loss - RF1, 2 - Off State		17			15			12		dB
Input P1dB		23			23			23		dBm
Input IP3		37			38			38		dBm
Switching Characteristics tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF		 1.8 11/4			 1.8 11/4			 1.8 11/4		 ns ns

Typical Performance

Insertion Loss vs. Temperature

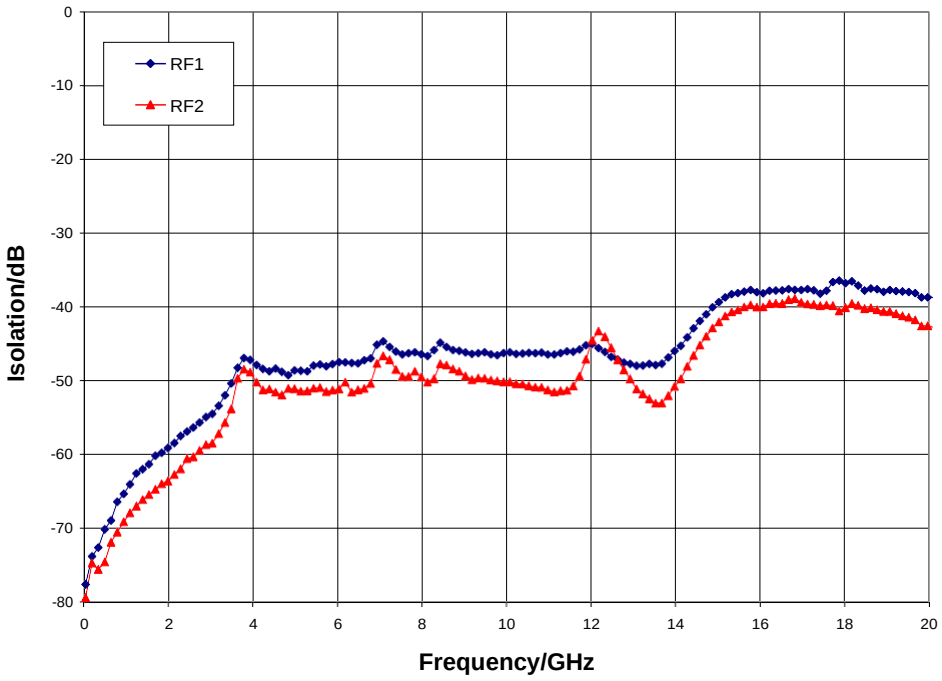


Return Loss

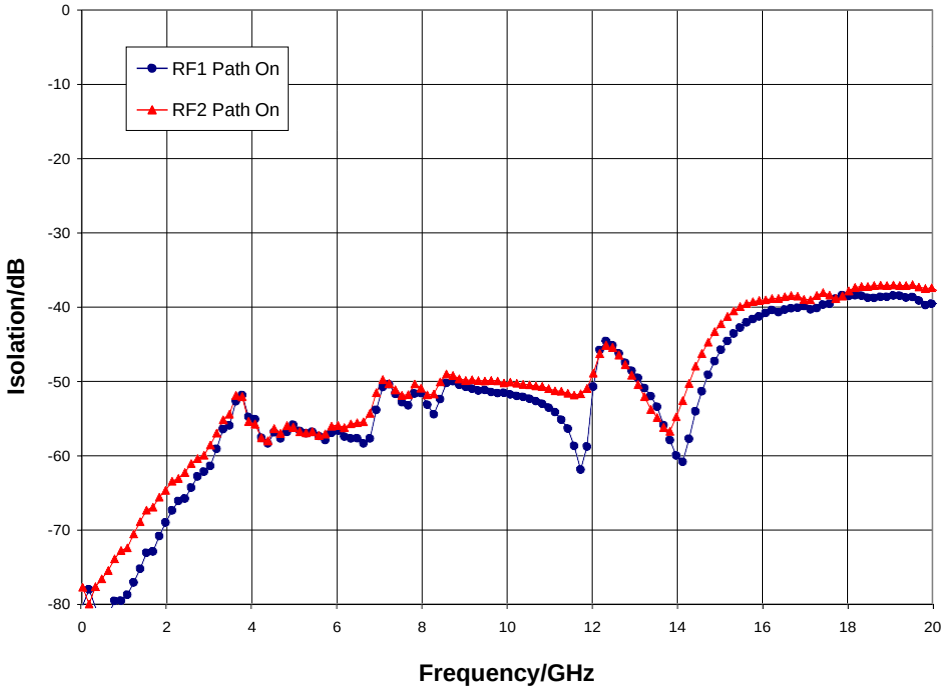


Typical Performance

Isolation Between Ports RFC and RF1/RF2

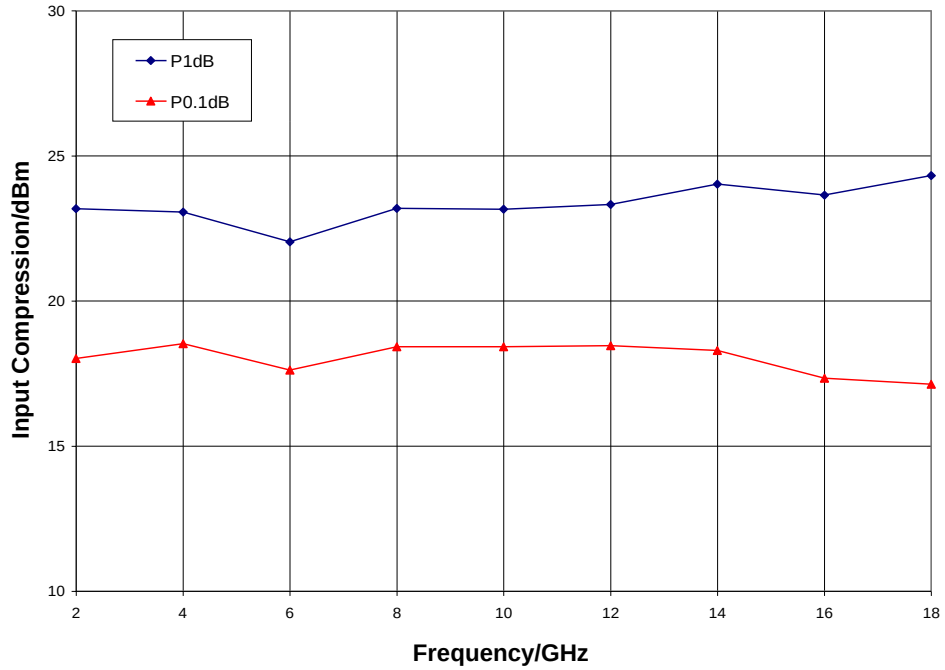


Isolation Between Ports RF1 and RF2

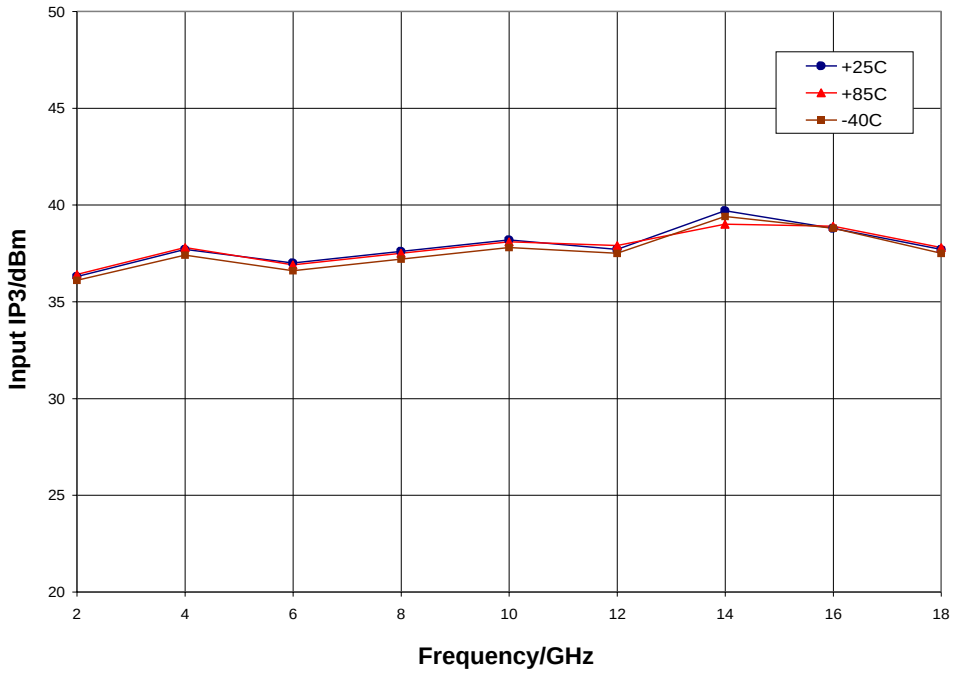


Typical Performance

Input P1dB and P0.1dB Compression Point

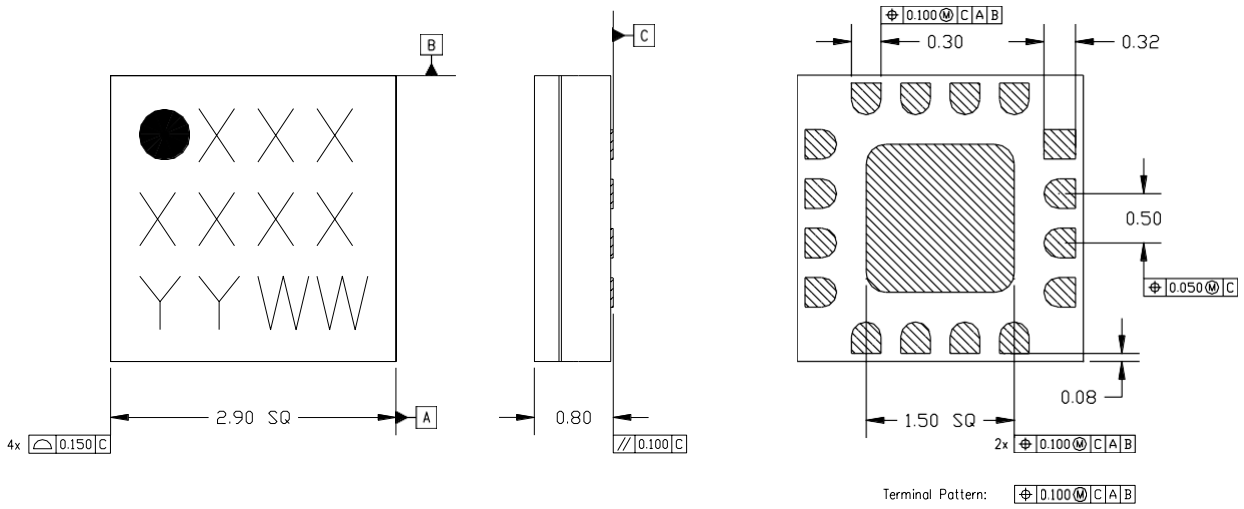


Input Third Order Intercept Point



Mechanical Information

Package Information and Dimensions



Notes:

1. All dimensions shown in mm.
2. Material: Black alumina
3. Lead finish:
   - 3.1. Ni: 8.89um max, 1.27um min
   - 3.2. Pd: 0.17um max, 0.07um min
   - 3.3. Au: 0.254um max, 0.03um min
4. Marking
   - 4.1. Line 1: Part number
     - 4.1.1. Example: CMD196C3 shall be marked as 196
   - 4.2. Line 2: Lot number
   - 4.3. Line 3: Date code - Last 2 digits of the year of manufacture followed by a 2 digit week code
5. Alternate pin #1 identifier is a single square pad
6. Alternate die paddle may have chamfered corners

Recommended PCB Land Pattern

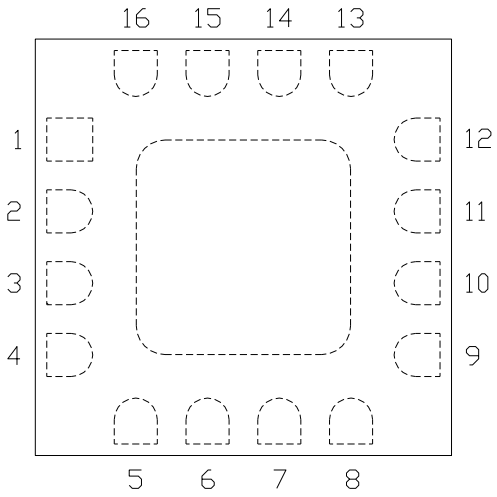
Qorvo recommends that the user develop the land pattern that will provide the best design for proper solder reflow and device attach for their specific application. Please review Qorvo Application Note AN 105 for a recommended land pattern approach.

Recommended Solder Reflow Profile

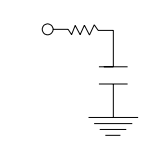
Qorvo recommends screen printing with belt furnace reflow to ensure proper solder reflow and device attach. Please review Qorvo Application Note AN 102 for a recommended solder reflow profile.

Pin Description

Pin Diagram

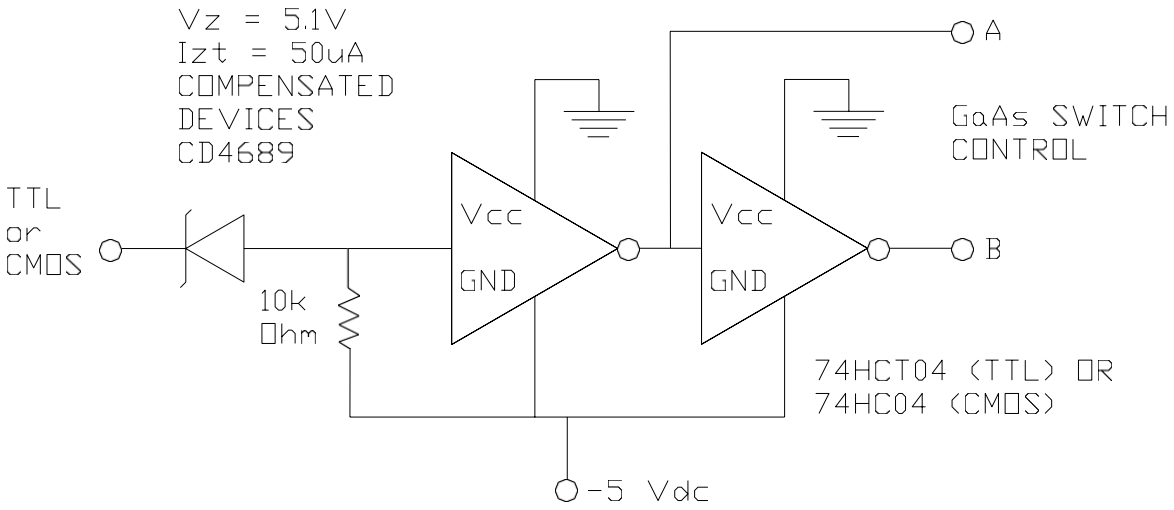


Functional Description

Pin	Function	Description	Schematic
1, 5, 8, 9, 12, 13, 16	N/C	No connection required These pins may be connected to RF / DC ground	
2, 4, 6, 15 and die paddle	Ground	Connect to RF / DC ground	
3, 7, 14	RFC, RF1, RF2	These pins are DC coupled and matched to 50 ohm Blocking capacitors are required if RF line potential is not equal to 0 V	
10	CTLB	See truth table and control voltage table	
11	CTLA	See truth table and control voltage table	

Applications Information

Suggested Driver Circuit

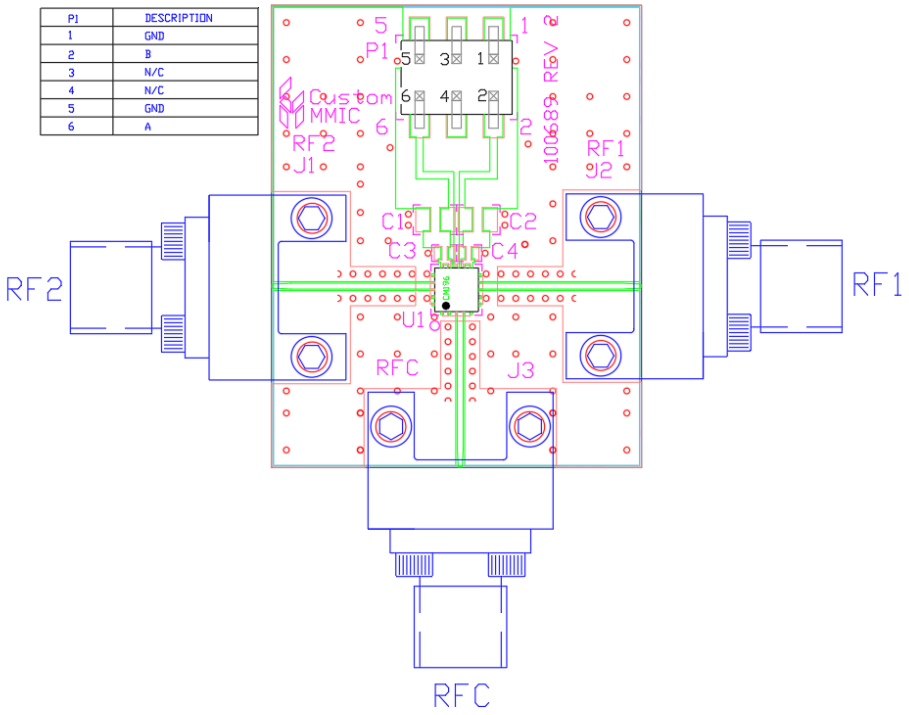


GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Applications Information

Evaluation Board

The circuit board shown has been developed for optimized assembly at Qorvo. A sufficient number of via holes should be used to connect the top and bottom ground planes. As surface mount processes vary, careful process development is recommended.



Bill of Material

Designator	Value	Description
J1, J2, J3		SMA End Launch Connector
P1		6 Pin Header
U1		CMD196C3 SPDT Switch
PCB		100628 Evaluation PCB