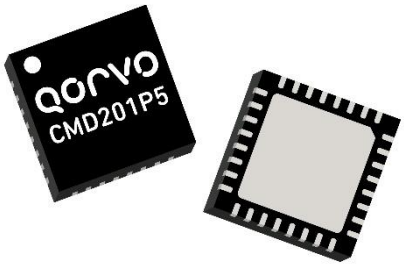
CMD201P5

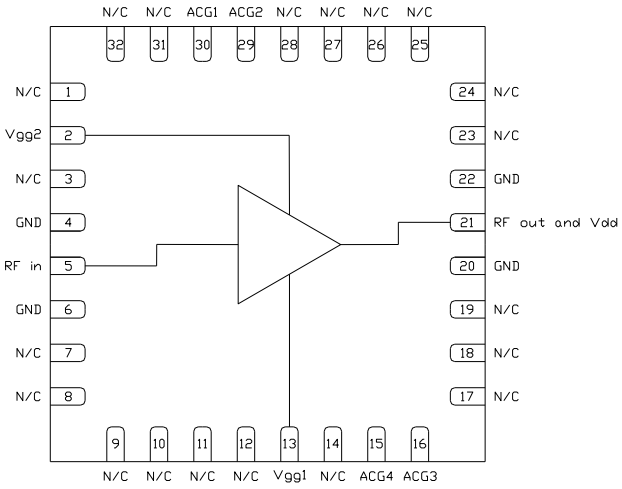
DC-20 GHz Distributed Power Amplifier

Product Overview

The CMD201P5 is wideband GaAs MMIC distributed power amplifier which operates from DC to 20 GHz. The amplifier delivers 11 dB of gain with a corresponding output 1 dB compression point of +27 dBm and output IP3 of 37 dBm at 10 GHz. The CMD201P5 is a 50 ohm matched design which eliminates the need for RF port matching.



Functional Block Diagram



Key Features

- Ultra Wideband Performance
- High Linearity
- High Output Power
- Excellent Return Losses
- Pb-Free RoHs Compliant 5x5 QFN Package

Ordering Information

Part No.	Description
CMD201P5	50 pcs on 7" reel
CMD201P5-EVB	Evaluation Board

Electrical Performance (V_{dd} = 10.0 V, V_{gg1} = -0.55 V, V_{gg2} = 5.0 V, T_A = 25° C, F = 10 GHz)

Parameter	Min	Typ	Max	Units
Frequency Range		DC - 20		GHz
Gain		11		dB
Noise Figure		3.4		dB
Input Return Loss		16		dB
Output Return Loss		17		dB
Output P1dB		27		dBm
Output IP3		38		dBm
Output IP2		38		dBm
Supply Current		400		mA

Absolute Maximum Ratings

Parameter	Rating
Drain Voltage, V_{dd}	12.0 V
Gate1 Voltage, V_{gg1}	-2.0 to 0 V
Gate2 Voltage, V_{gg2}	6.0 V
RF Input Power	+30 dBm
Channel Temperature, Tch	150° C
Power Dissipation, Pdiss	5.43 W
Thermal Resistance, Q_{JC}	11.9° C/W
Operating Temperature	-40 to 85° C
Storage Temperature	-55 to 150° C

Exceeding any one or combination of the maximum ratings may cause permanent damage to the device.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{dd}	8.0	10.0	12.0	V
I_{dd}		400		mA
V_{gg1}		-0.55		V
V_{gg2}		5.0		V

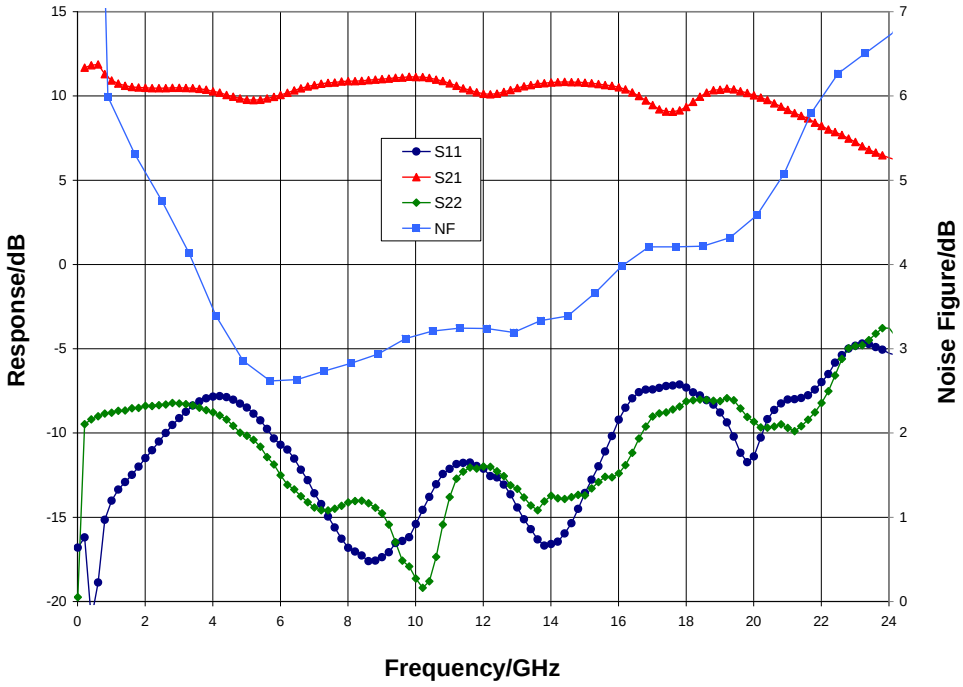
Electrical performance is measured at specific test conditions. Electrical specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications (V_{dd} = 10.0 V, V_{gg1} = -0.55 V, V_{gg2} = 5.0 V, T_A = 25° C)

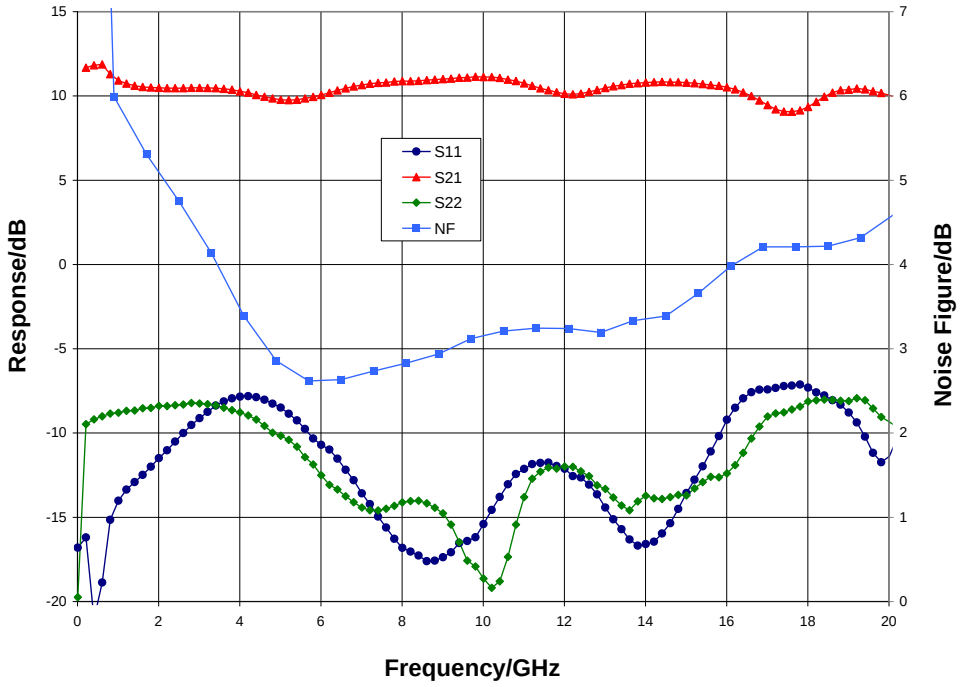
Parameter	Min	Typ	Max	Min	Typ	Max	Units
Frequency Range		DC - 6			6 - 20		GHz
Gain	8	10		7	10		dB
Noise Figure		5			4		dB
Input Return Loss		8			10		dB
Output Return Loss		8			10		dB
Output P1dB	25	28		24	27		dBm
Output IP3		37			36		dBm
Output IP2		41			40		dBm
Supply Current	300	400	500	300	400	500	mA
Gain Temperature Coefficient		0.009			0.014		dB/°C
Noise Figure Temperature Coefficient		0.01			0.014		dB/°C

Typical Performance

Broadband Performance, V_{dd} = 10 V, V_{gg1} = -0.55 V, V_{gg2} = 5 V, I_{dd} = 400 mA, T_A = 25° C

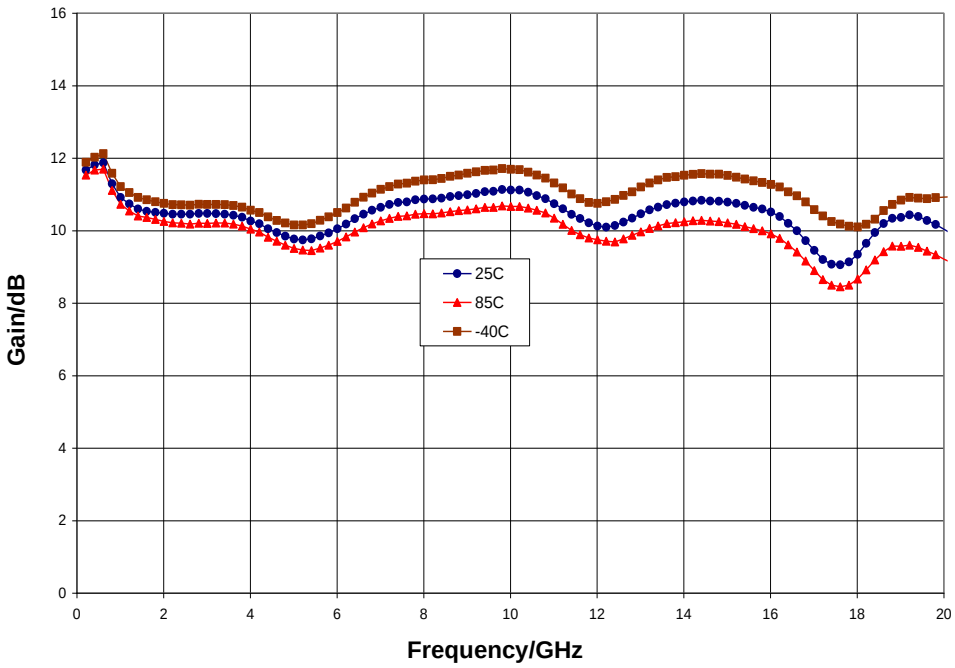


Narrow-band

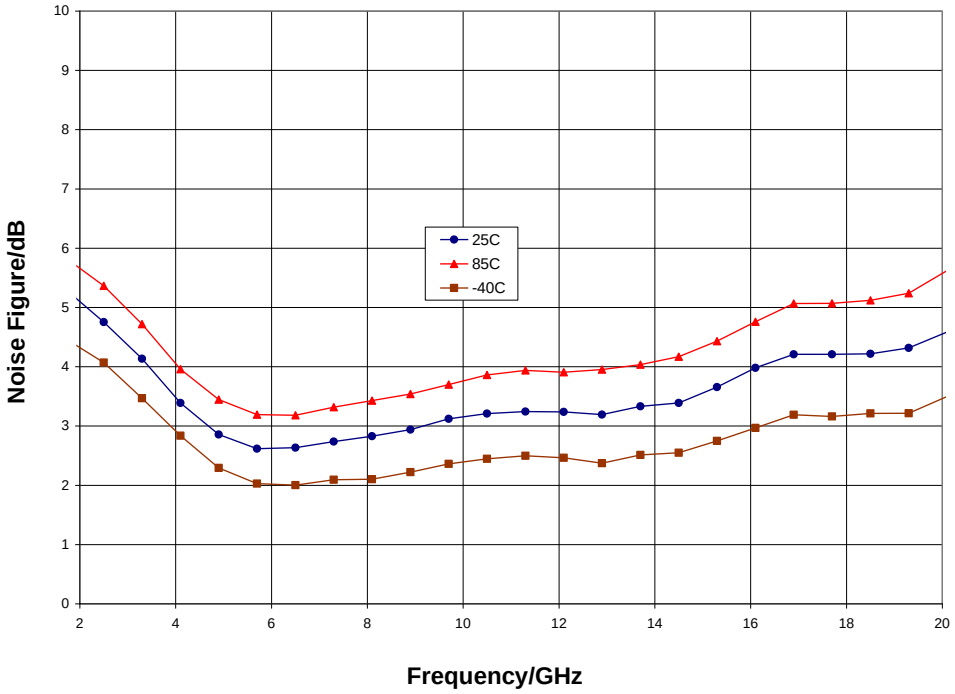


Typical Performance

Gain vs. Temperature, V_{dd} = 10 V, V_{gg1} = -0.55 V, V_{gg2} = 5 V

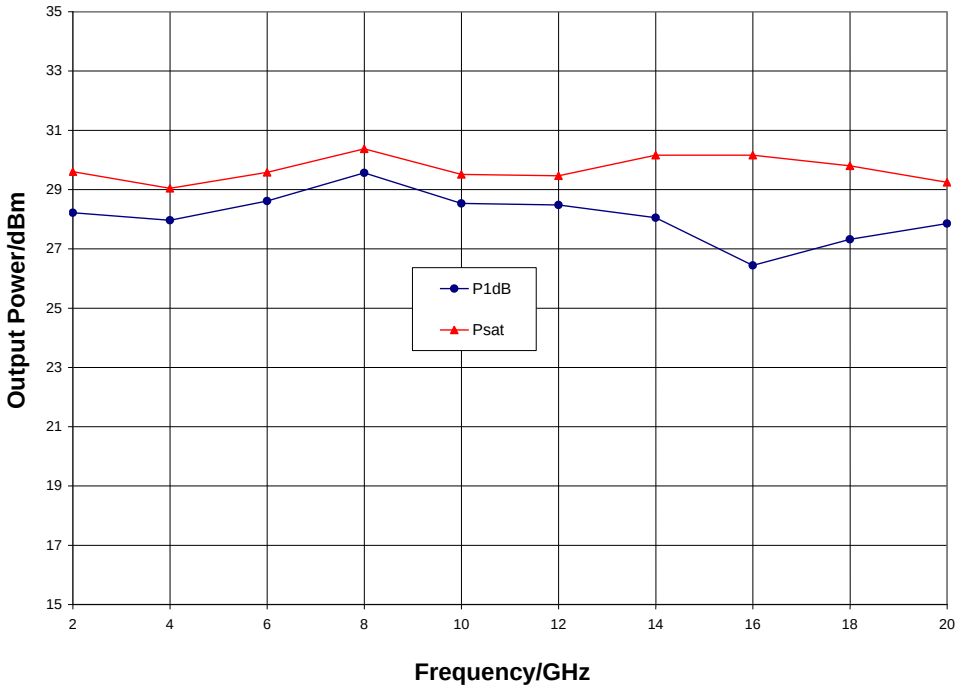


Noise Figure vs. Temperature, V_{dd} = 10 V, V_{gg1} = -0.55 V, V_{gg2} = 5 V

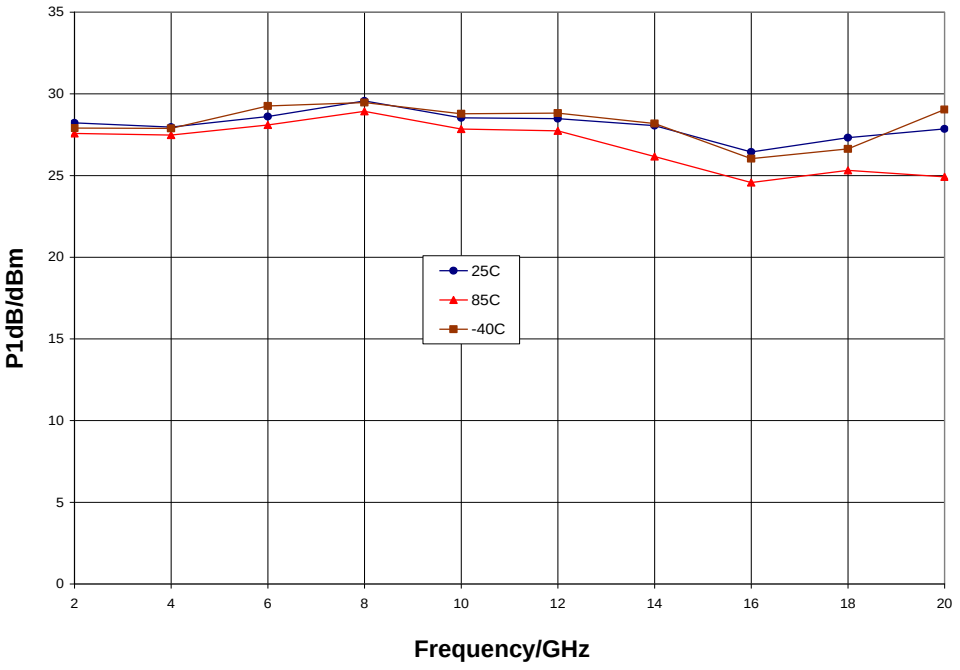


Typical Performance

Output Power, V_{dd} = 10 V, V_{gg1} = -0.55 V, V_{gg2} = 5 V, T_A = 25° C

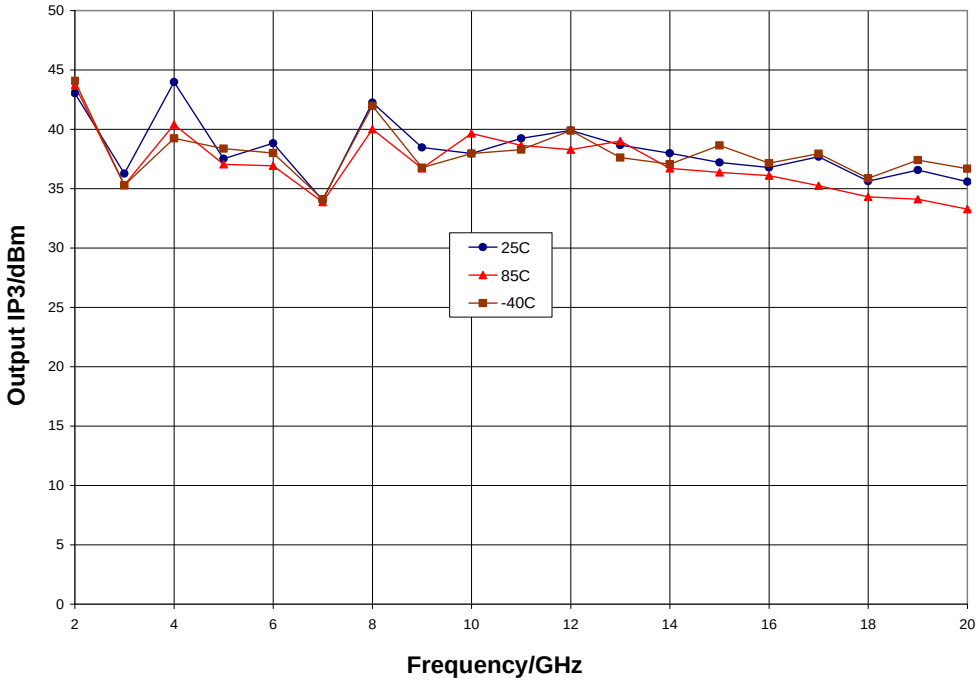


Output P1dB vs. Temperature, V_{dd} = 10 V, V_{gg1} = -0.55 V, V_{gg2} = 5 V

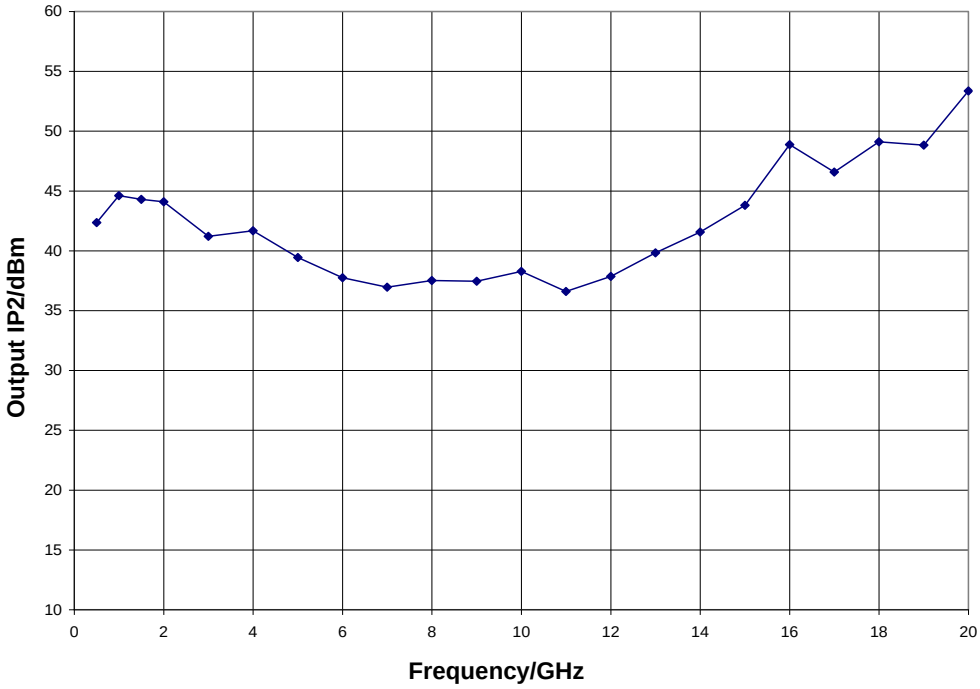


Typical Performance

Output IP3 vs. Temperature, V_{dd} = 10 V, V_{gg1} = -0.55 V, V_{gg2} = 5 V

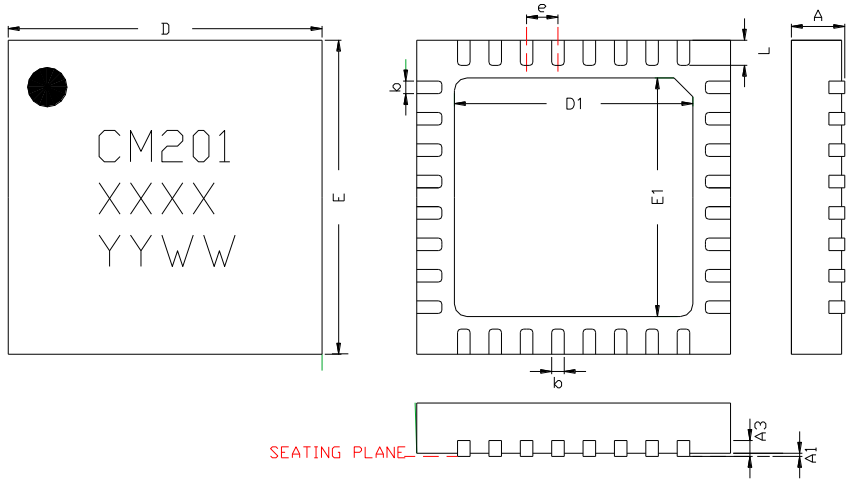


Output IP2, V_{dd} = 10 V, V_{gg1} = -0.55 V, V_{gg2} = 5 V



Mechanical Information

Package Information and Dimensions



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3	---	0.25REF.	---
b	0.18	0.23	0.30
D	4.85	5.00	5.15
D1	---	3.8BSC	---
E	4.85	5.00	5.15
E1	---	3.8BSC	---
e	---	0.50BSC	---
L	0.30	0.40	0.50

Notes:

1. Dimensions are in millimeters
2. RoHs compliant mold compound
3. Lead frame material: Copper alloy
4. Lead finish: 100% matte Sn
5. Indicated dimension/tolerance applies to leads and exposed pads

Recommended PCB Land Pattern

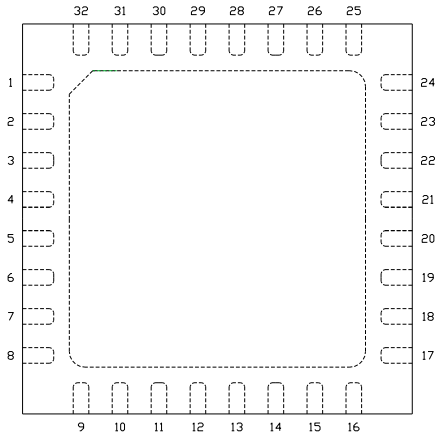
Qorvo recommends that the user develop the land pattern that will provide the best design for proper solder reflow and device attach for their specific application. Please review Qorvo Application Note AN 105 for a recommended land pattern approach.

Recommended Solder Reflow Profile

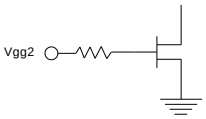
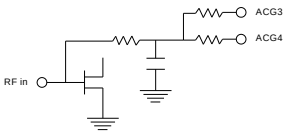
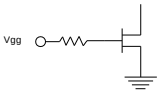
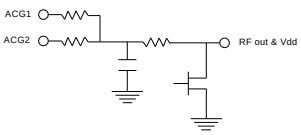
Qorvo recommends screen printing with belt furnace reflow to ensure proper solder reflow and device attach. Please review Qorvo Application Note AN 102 for a recommended solder reflow profile

Pin Description

Pin Diagram



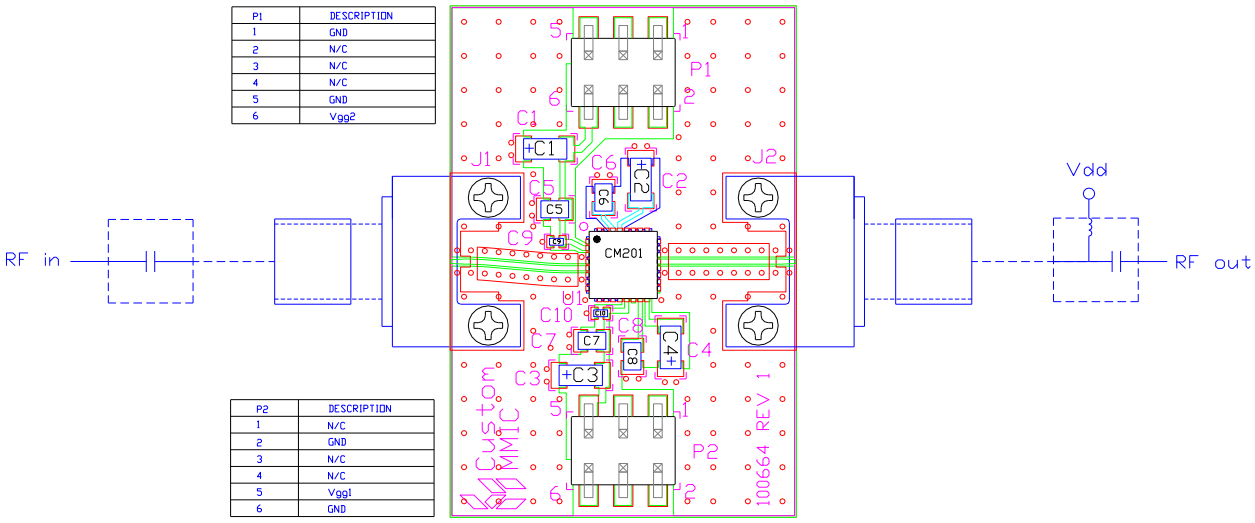
Functional Description

Pin	Function	Description	Schematic
1, 3, 7 - 12, 14, 17 - 19, 23 - 28, 31, 32	N/C	No connection required These pins may be connected to RF / DC ground	
4, 6, 20, 22 and die paddle	Ground	Connect to RF / DC ground	
2	V_{gg2}	Power supply voltage Decoupling and bypass caps required	
5	RF in	50 ohm matched input	
15, 16	ACG4, 3	Low frequency termination Attach bypass capacitor per application circuit	
13	V_{gg1}	Power supply voltage Decoupling and bypass caps required	
21	RF out & V_{dd}	Power supply voltage and 50 ohm matched output	
29, 30	ACG2, 1	Low frequency termination Attach bypass capacitor per application circuit	

Applications Information

Evaluation Board

The circuit board shown has been developed for optimized assembly at Qorvo. A sufficient number of via holes should be used to connect the top and bottom ground planes. As surface mount processes vary, careful process development is recommended.



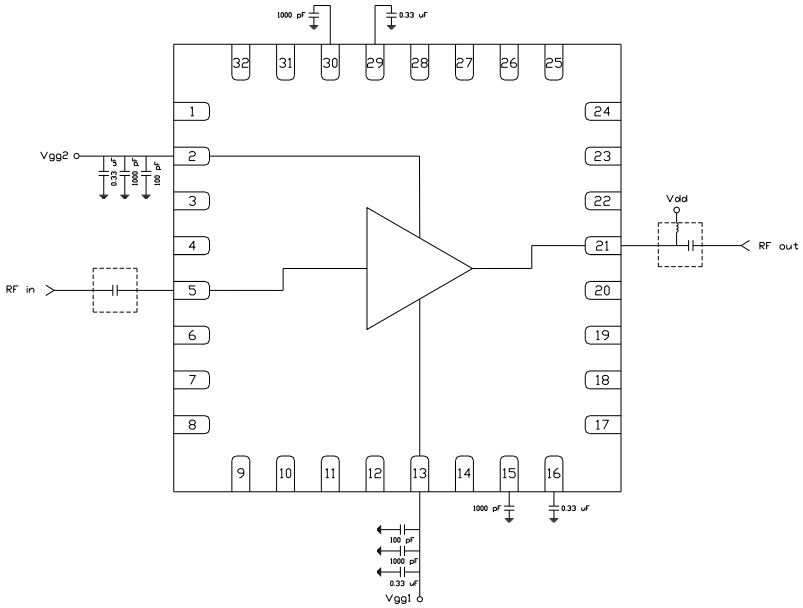
Bill of Material

Designator	Value	Description
J1, J2		SMA End Launch Connector
P1, P2		6 Pin DC Header
C1 - C4	0.33 µF	Capacitor, Tantalum
C5 - C8	1000 pF	Capacitor, 0603
C9, C10	100 pF	Capacitor, 0402
U1		CMD201P5 Driver Amplifier
PCB		100664 Evaluation PCB

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Applications Information

Application Circuit



Note: Drain voltage (V_{dd}) must be applied through a broadband bias tee or external bias network.
External DC block is required on RF input.

Biasing and Operation

The CMD201P5 is biased with a positive drain supply, a negative gate1 supply and a positive gate2 supply. Performance is optimized when the drain voltage is set to +10 V. The recommended gate1 and gate2 voltages are -0.55 V and +5 V respectively.

Turn ON procedure:

1. Apply gate voltage V_{gg1} and set to -2 V
2. Apply drain voltage V_{dd} and set to +10 V
3. Apply gate voltage V_{gg2} and set to +5 V
4. Increase V_{gg1} (less negative) to achieve a drain current of 400 mA

Turn OFF procedure:

1. Turn off gate voltage V_{gg2}
2. Turn off drain voltage V_{dd}
3. Turn off gate voltage V_{gg1}

RF power can be applied at any time.