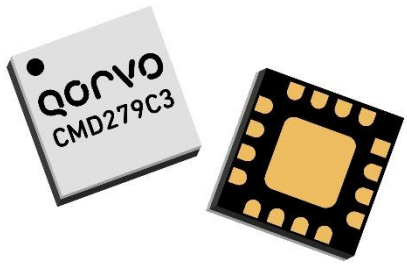
CMD279C3

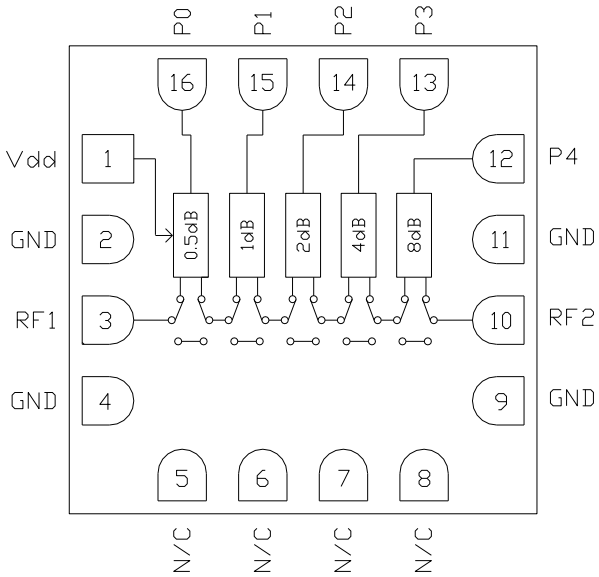
2-18 GHz 5-bit Digital Attenuator

Product Overview

The CMD279C3 is a positive controlled, wideband GaAs MMIC 5-bit digital attenuator housed in a leadless 3x3 mm surface mount package. Each bit of the attenuator is controlled by a single voltage of either 0 V or +5 V. The attenuator bit values are 0.5 (LSB), 1, 2, 4, and 8 dB, for a total attenuation of 15.5 dB. The CMD279C3 has a low insertion loss of 3.5 at 9 GHz and the attenuation accuracy is typically 0.2 dB step error. The CMD279C3 is a 50 ohm matched design which eliminates the need for RF port matching



Functional Block Diagram



Key Features

- Wideband Performance
- Low Insertion Loss
- Wide Attenuation Range
- Pb-Free RoHs Compliant 3x3 QFN Package

Ordering Information

Part No.	Description
CMD279C3	100pcs on 7'' reel
CMD279C3-EVB	Evaluation Board

Electrical Performance (V_{dd} = 5 V, Vctl = 0 / +5 V, T_A = 25° C, F = 9 GHz)

Parameter	Min	Typ	Max	Units
Frequency Range		2 - 18		GHz
Insertion Loss		3.5		dB
Attenuation Range		15.5		dB
Input Return Loss		13		dB
Output Return Loss		13		dB
Input P0.1dB		27		dBm
Input IP3		42		dBm
Switching Speed		25		ns

Absolute Maximum Ratings

Parameter	Rating
Bias Voltage, V_{dd}	8 V
Control Voltage, V_{ctl}	8 V
RF Input Power	+27 dBm
Thermal Resistance, Q_{JC}	115.28° C/W
Operating Temperature	-40 to 85° C
Storage Temperature	-55 to 150° C

Exceeding any one or combination of the maximum ratings may cause permanent damage to the device.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{dd}	2.5	5	5.5	V

Electrical performance is measured at specific test conditions. Electrical specifications are not guaranteed over all recommended operating conditions.

Truth Table

Control Voltage Input					Attenuation State RF1 - RF2 (dB)
P0 0.5 dB	P1 1 dB	P2 2 dB	P3 4 dB	P4 8 dB	
High	High	High	High	High	Reference (insertion loss)
Low	High	High	High	High	0.5
High	Low	High	High	High	1.0
High	High	Low	High	High	2.0
High	High	High	Low	High	4.0
High	High	High	High	Low	8.0
Low	Low	Low	Low	Low	15.5

Any combination of the above states will result in an attenuation approximately equal to the sum of the bits selected.

Control Voltage

State	Bias Condition
High	V_{dd} ± 0.3 V
Low	0 ± 0.3 V

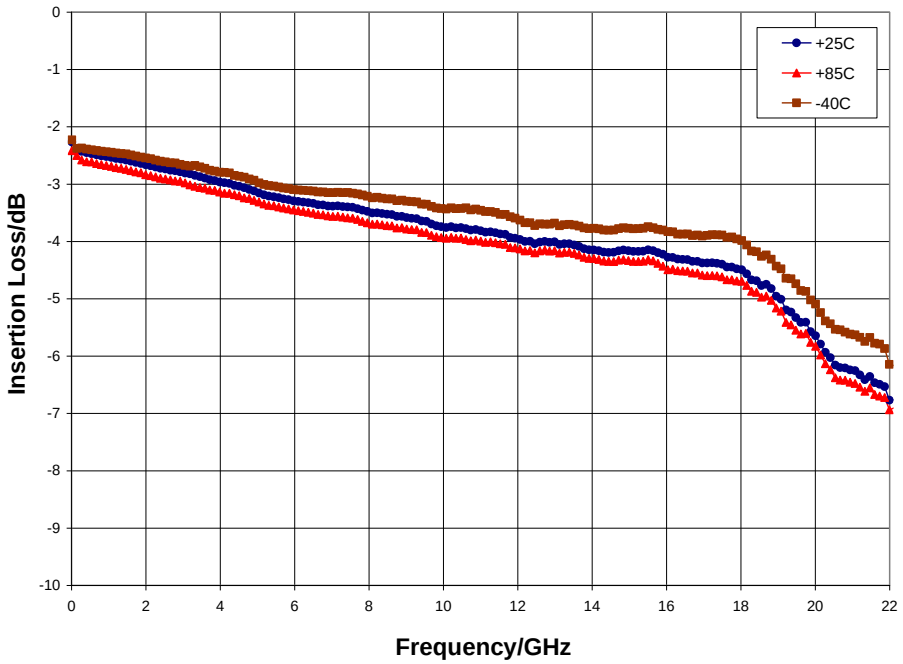
Electrical Specifications (V_{dd} = +5 V, V_{ctl} = 0/+5 V, T_A = 25° C)

Parameter	Min	Typ	Max	Min	Typ	Max	Units
Frequency Range		2 - 10			10 - 18		GHz
Insertion Loss		3.2	4.3		4.2	5	dB
Attenuation Range		15.5			15.5		dB
Attenuation Accuracy 0.5 - 7.5 dB States 8 - 15.5 dB States		± 0.4 Max ± 0.6 + 10% of Atten. Setting Max			± 0.4 Max ± 0.6 + 10% of Atten. Setting Max		 dB dB
Input Return Loss		13			13		dB
Output Return Loss		13			13		dB
Input P0.1 dB		26.5			26.5		dBm
Input IP3		42			42		dBm

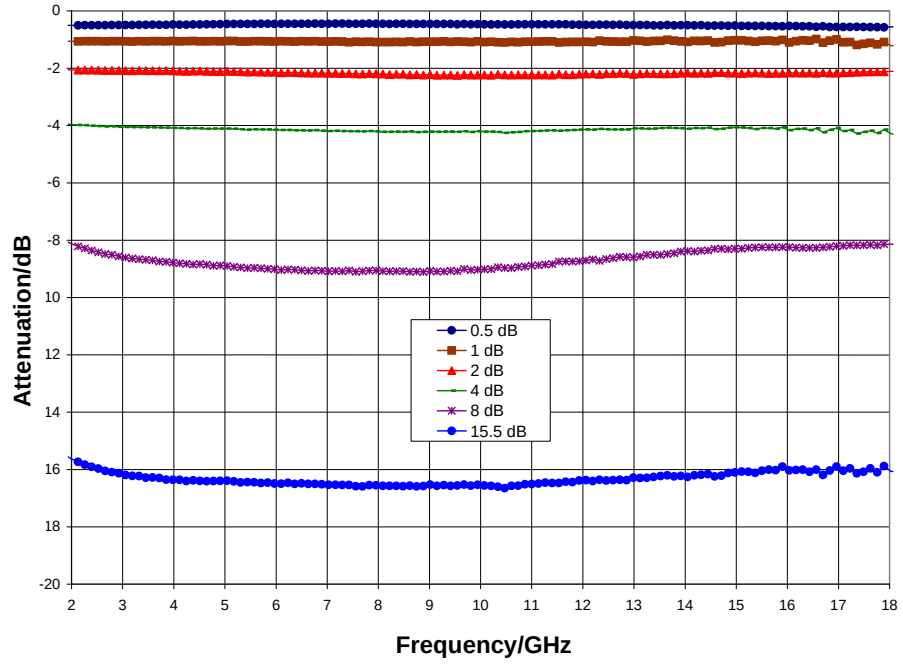
Note: Specification applies to major states

Typical Performance

Insertion Loss versus Temperature

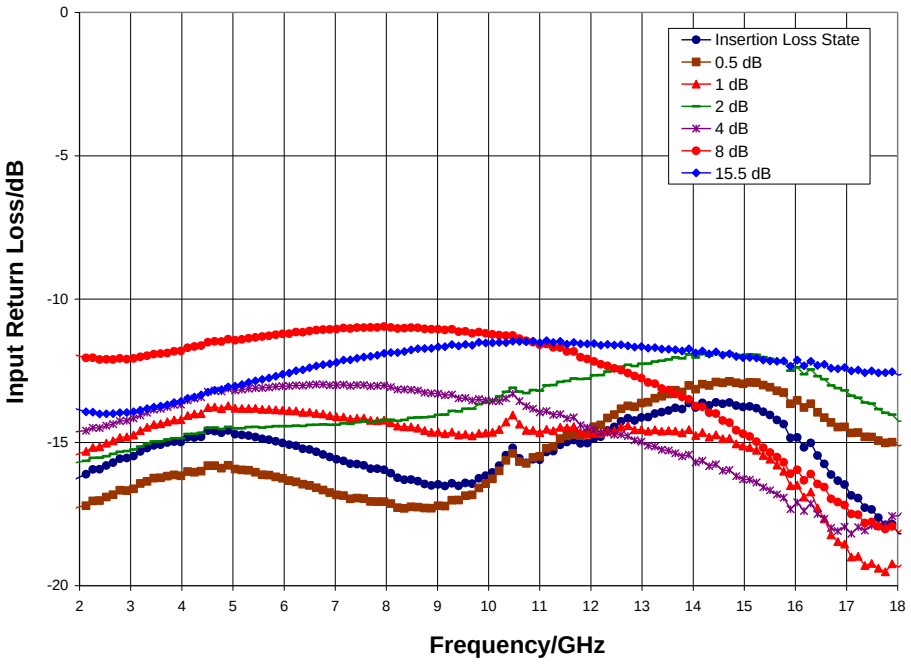


Normalized Attenuation (major states only), T_A = 25° C

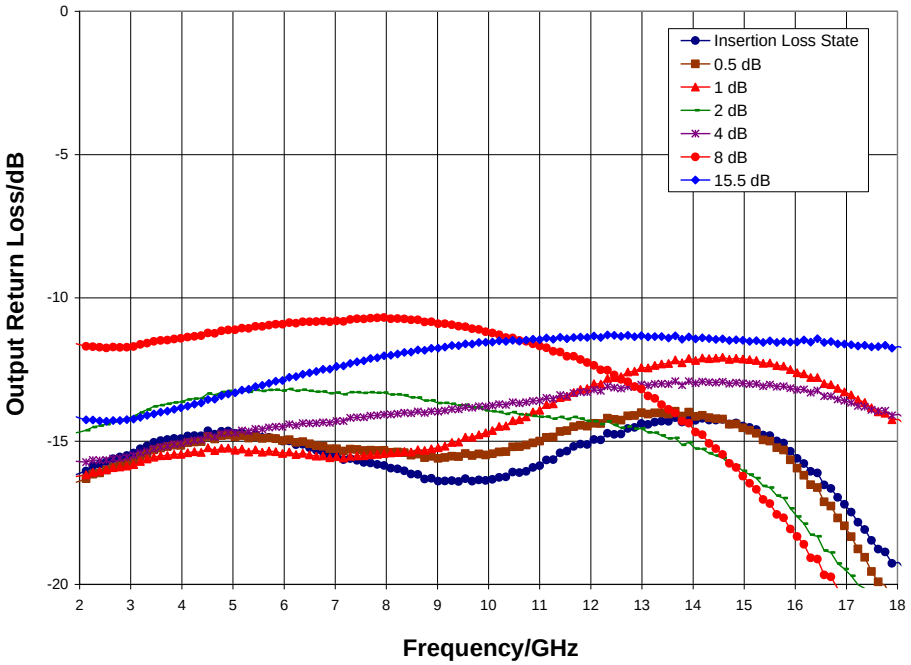


Typical Performance

Input Return Loss (major states only), T_A = 25° C

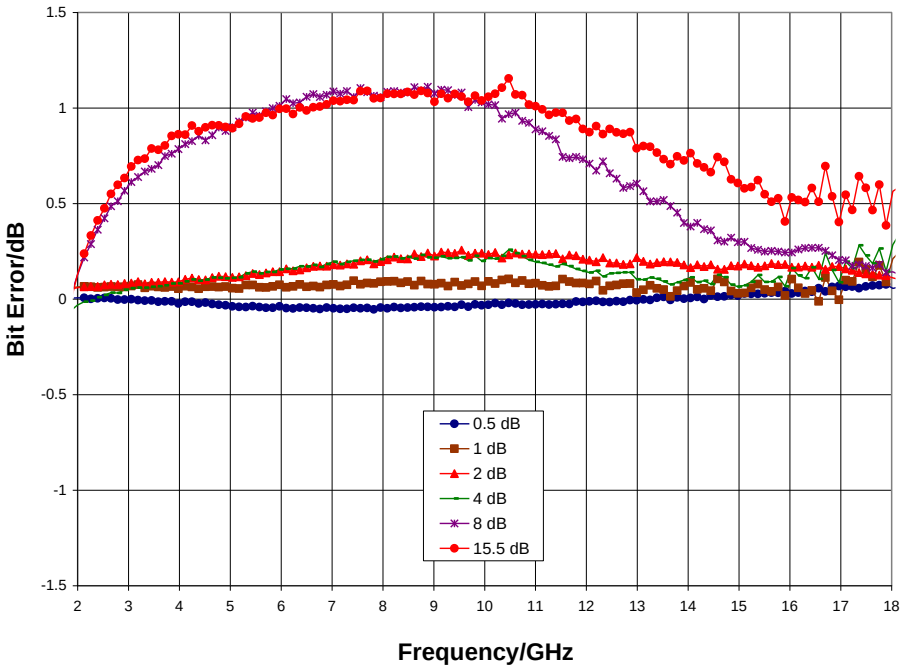


Output Return Loss (major states only), T_A = 25° C

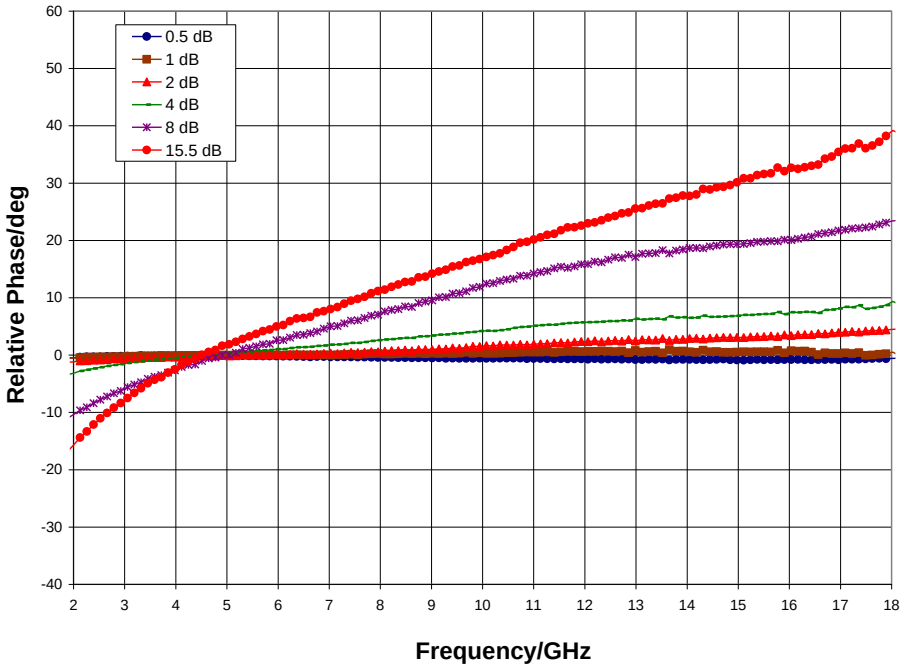


Typical Performance

Bit Error versus Frequency, T_A = 25° C

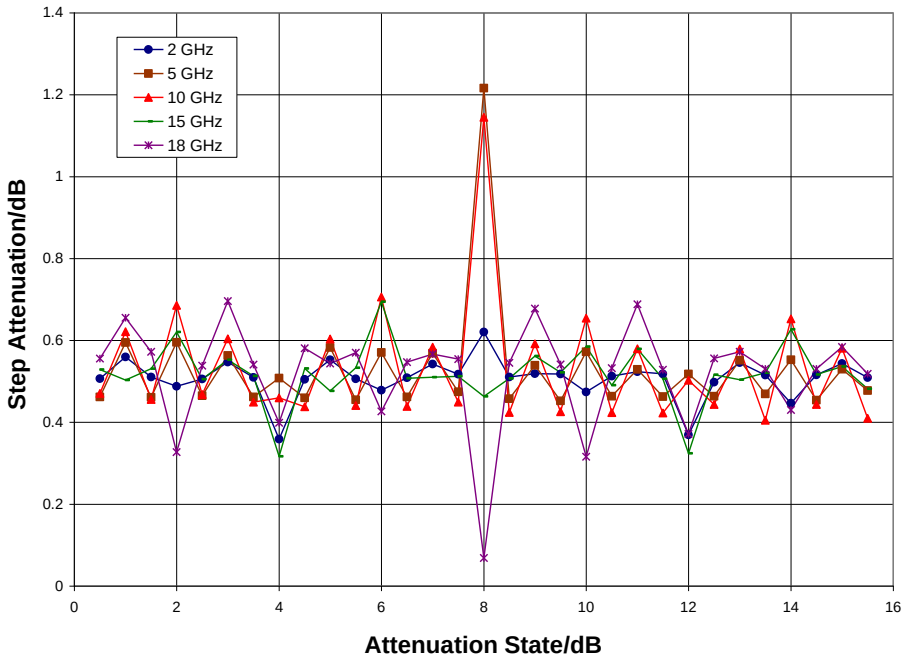


Relative Phase versus Frequency, T_A = 25° C

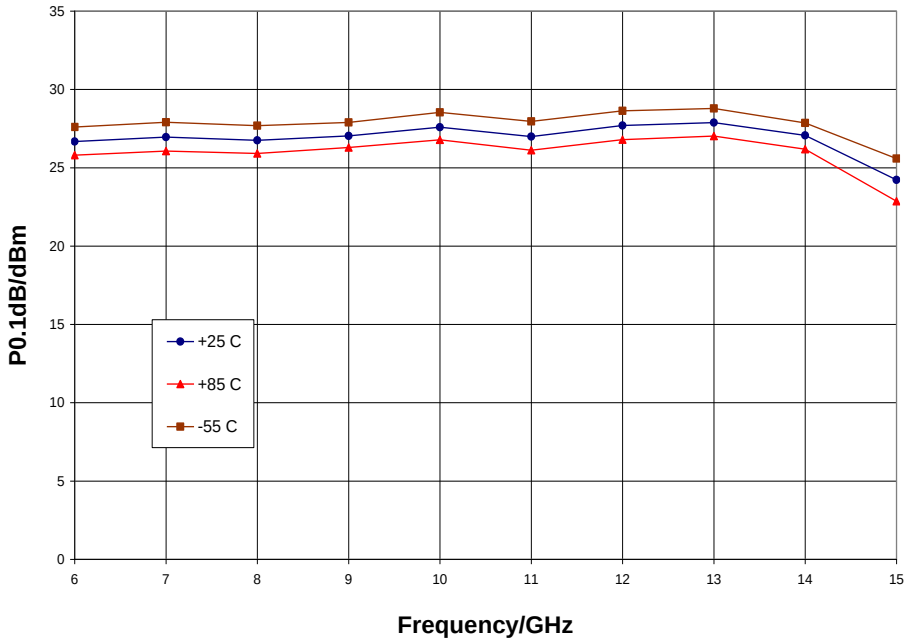


Typical Performance

Step Attenuation versus Attenuation State, T_A = 25° C

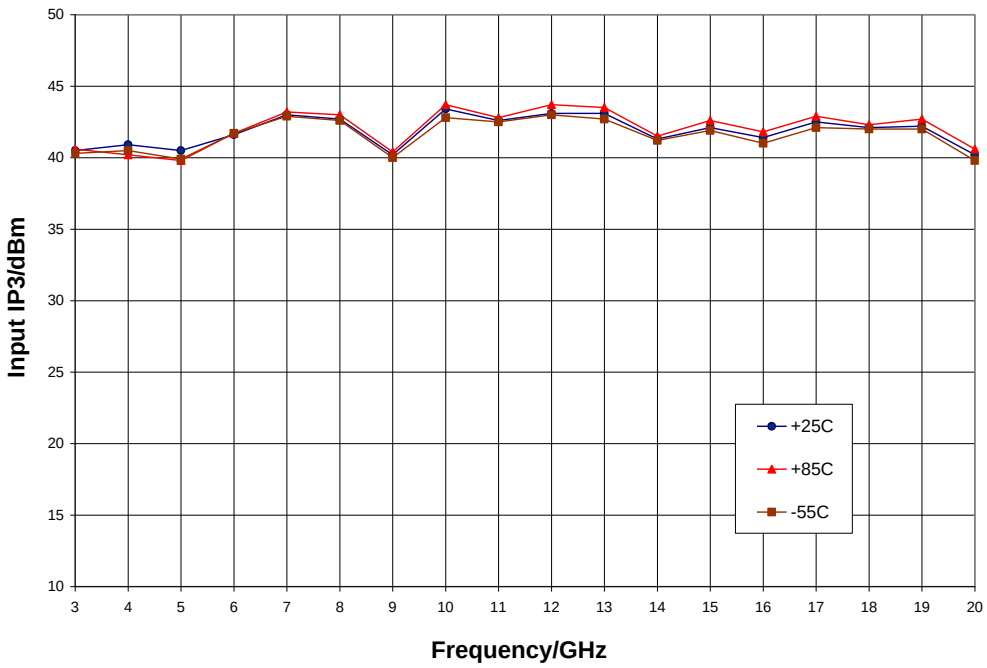


Input Power for 0.1 dB Compression (insertion loss state)



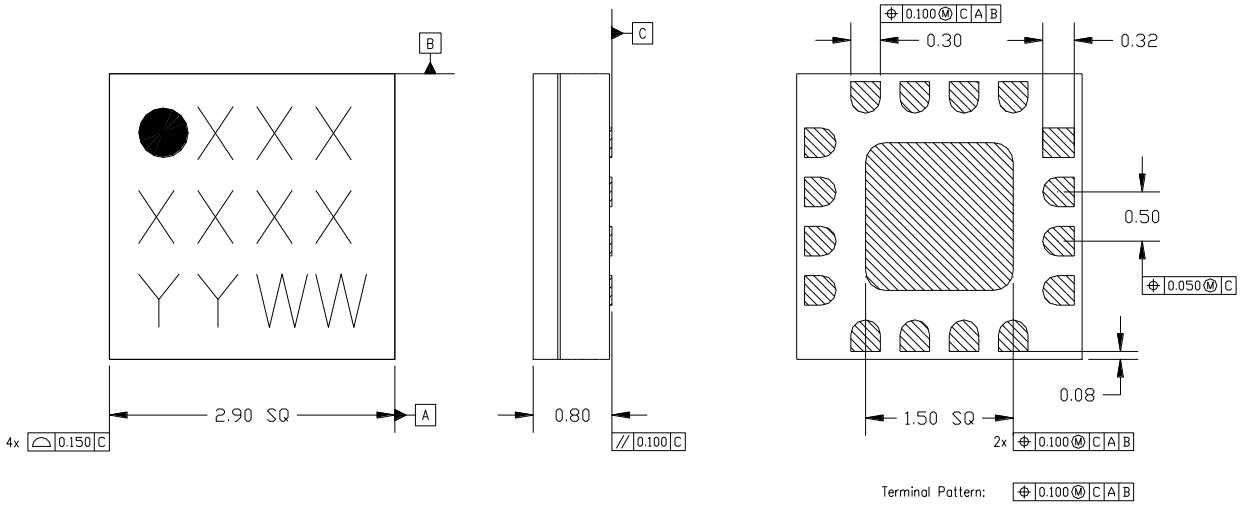
Typical Performance

Input IP3 versus Temperature (insertion loss state)



Mechanical Information

Package Information and Dimensions



Notes:

1. All dimensions shown in mm.
2. Material: Black alumina
3. Lead finish:
   - 3.1. Ni: 8.89um max 1.27um min
   - 3.2. Pd: 0.17um max, 0.07um min
   - 3.3. Au: 0.254um max, 0.03um min
4. Marking
   - 4.1. Line 1: Part number
     - 4.1.1. Example: CMD196C3 shall be marked as 196
   - 4.2. Line 2: Lot number
   - 4.3. Line 3: Date code - Last 2 digits of the year of manufacture followed by a 2 digit week code
5. Alternate pin #1 identifier is a single square pad
6. Alternate die paddle may have chamfered corners

Recommended PCB Land Pattern

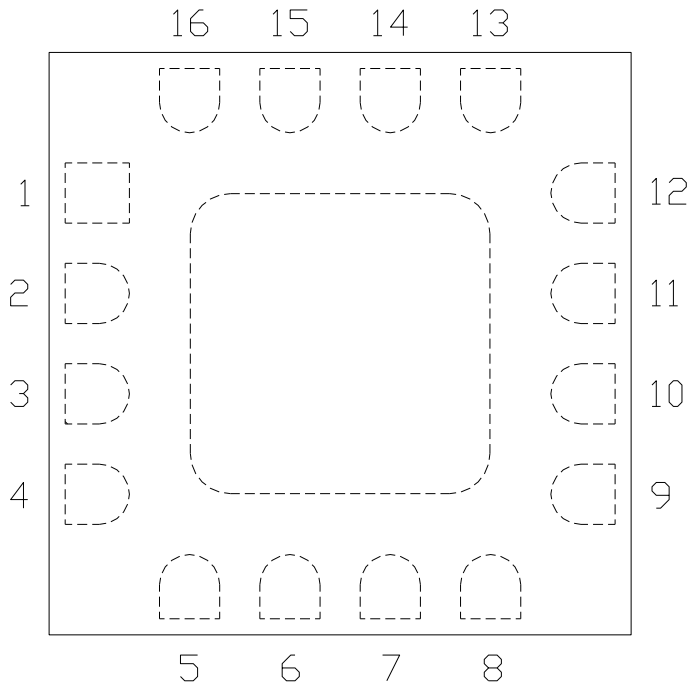
Qorvo recommends that the user develop the land pattern that will provide the best design for proper solder reflow and device attach for their specific application. Please review Qorvo Application Note AN 105 for a recommended land pattern approach.

Recommended Solder Reflow Profile

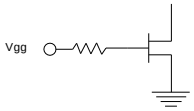
Qorvo recommends screen printing with belt furnace reflow to ensure proper solder reflow and device attach. Please review Qorvo Application Note AN 102 for a recommended solder reflow profile.

Pin Description

Pin Diagram



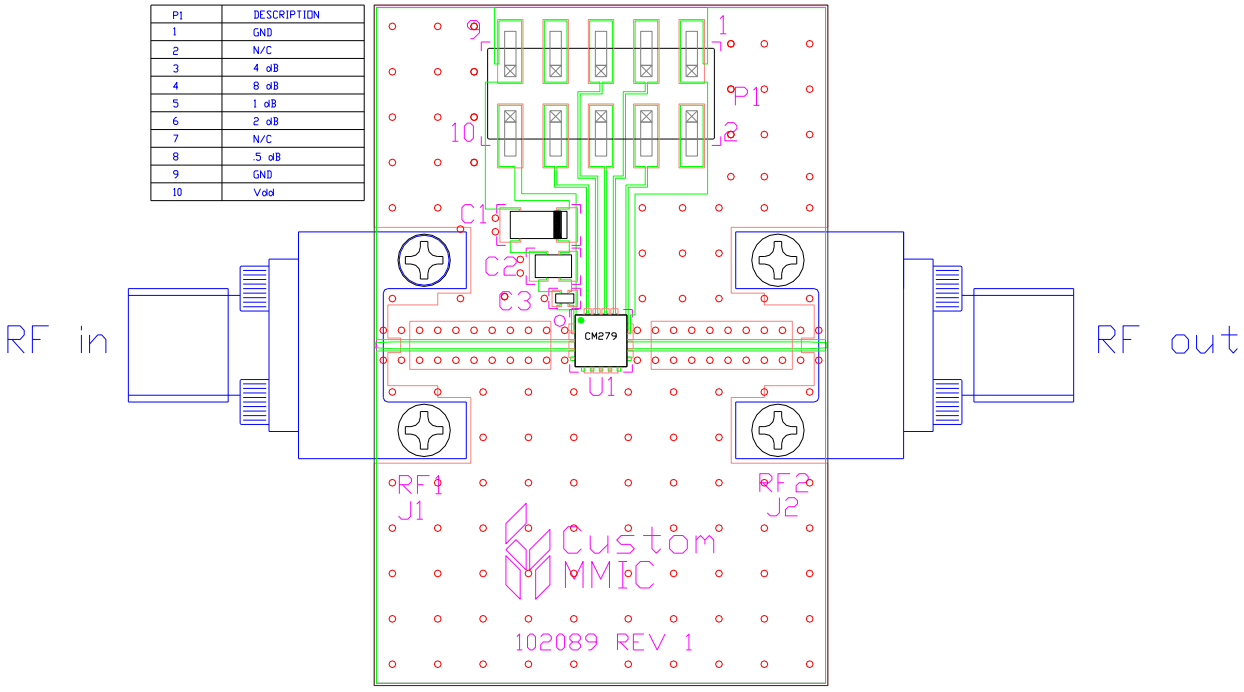
Functional Description

Pin	Function	Description	Schematic
1	V_{dd}	Positive bias +5 V	
2, 4, 9, 11 and die paddle	Ground	Connect to RF / DC ground	
3, 10	RF1, RF2	DC coupled, 50 ohm matched External blocking capacitors are required	
5 - 8	N/C	No connection required These pins may be connected to RF / DC ground	
12 - 16	P4 - P0	Bit control voltages, see truth table for values	

Applications Information

Evaluation Board

The circuit board shown has been developed for optimized assembly at Qorvo. A sufficient number of via holes should be used to connect the top and bottom ground planes. As surface mount processes vary, careful process development is recommended.



Designator	Value	Description
J1, J2		SMA End Launch Connector
P1		10 Pin Header
C1	0.33 µF	Capacitor, Tantalum
C2	1000 pF	Capacitor, 0603
C3	100 pF	Capacitor, 0402
U1		CMD279C3 DATT
PCB		102089 Evaluation PCB

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.