CMD279
2-30 GHz 5-bit Digital Attenuator

Product Overview

The CMD279 is positive controlled, wideband GaAs MMIC 5-bit digital attenuator die which operates from 2 to 30 GHz. Each bit of the attenuator is controlled by a single voltage of either 0 V or +5 V. The attenuator bit values are 0.5 (LSB), 1, 2, 4, and 8 dB, for a total attenuation of 15.5 dB. The CMD279 has a low insertion loss of 3.5 at 10 GHz and the attenuation accuracy is typically 0.2 dB step error. The CMD279 is a 50 ohm matched design which eliminates the need for RF port matching. The CMD279 offers full passivation for increased reliability and moisture protection.

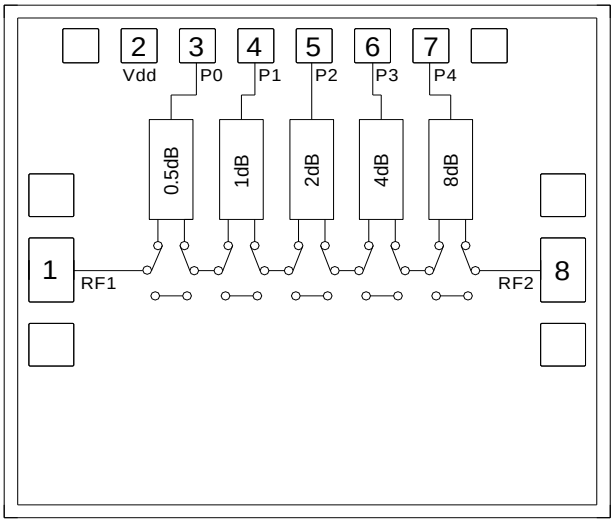
Key Features

- Ultra Wideband Performance
- Low Insertion Loss
- Wide Attenuation Range
- Small Die Size

Ordering Information

Part No.	Description
CMD279	100pcs in gel pack

Functional Block Diagram



Electrical Performance (V_{dd} = 5 V, V_{ctl} = 0 / +5 V, T_A = 25° C, F = 10 GHz)

Parameter	Min	Typ	Max	Units
Frequency Range		2 - 30		GHz
Insertion Loss		3.5		dB
Attenuation Range		15.5		dB
Input Return Loss		15		dB
Output Return Loss		15		dB
Input P0.1dB		27		dBm
Input IP3		42		dBm
Switching Speed		25		ns

Absolute Maximum Ratings

Parameter	Rating
Bias Voltage, V_{dd}	8 V
Control Voltage, V_{ctl}	8 V
RF Input Power	+27 dBm
Thermal Resistance, Q_{JC}	115.28° C/W
Operating Temperature	-55 to 85° C
Storage Temperature	-55 to 150° C

Exceeding any one or combination of the maximum ratings may cause permanent damage to the device.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{dd}	2.5	5	5.5	V

Electrical performance is measured at specific test conditions. Electrical specifications are not guaranteed over all recommended operating conditions.

Truth Table

Control Voltage Input					Attenuation State RF1 - RF2 (dB)
P0 0.5 dB	P1 1 dB	P2 2 dB	P3 4 dB	P4 8 dB	
High	High	High	High	High	Reference (insertion loss)
Low	High	High	High	High	0.5
High	Low	High	High	High	1.0
High	High	Low	High	High	2.0
High	High	High	Low	High	4.0
High	High	High	High	Low	8.0
Low	Low	Low	Low	Low	15.5

Any combination of the above states will result in an attenuation approximately equal to the sum of the bits selected.

Control Voltage

State	Bias Condition
High	V_{dd} ± 0.3 V
Low	0 ± 0.3 V

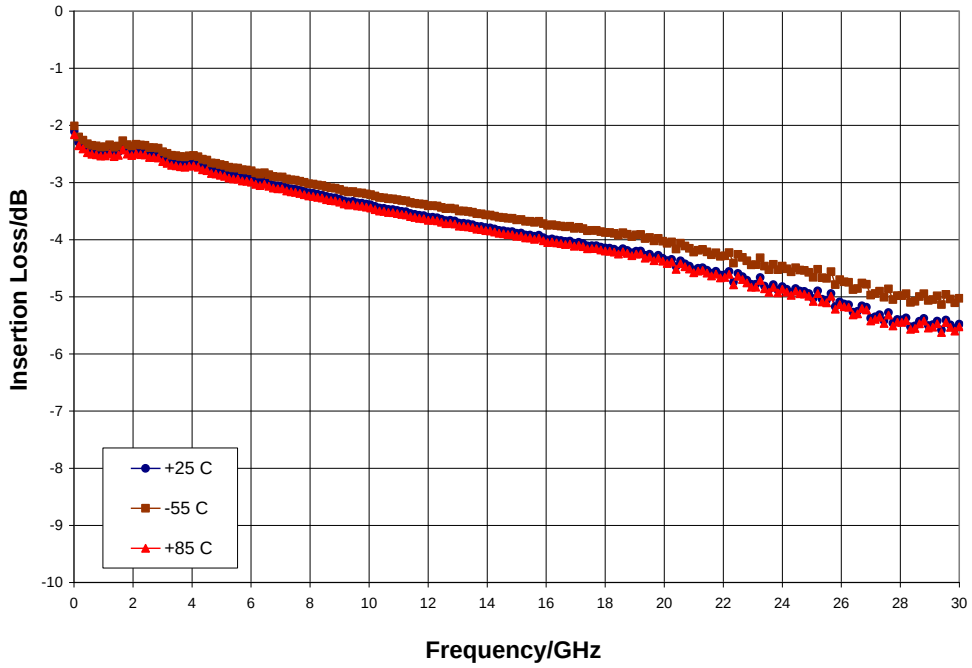
Electrical Specifications (V_{dd} = +5 V, V_{ctl} = 0/+5 V, T_A = 25° C)

Parameter	Min	Typ	Max	Min	Typ	Max	Units
Frequency Range		2 - 18			18 - 30		GHz
Insertion Loss		3	4.7		5	6	dB
Attenuation Range		15.5			15.5		dB
Attenuation Accuracy 0.5 - 7.5 dB States 8 - 15.5 dB States		± 0.3 Max ± 0.3 + 8% of Atten. Setting Max			± 0.4 Max ± 0.6 + 11% of Atten. Setting Max		 dB dB
Input Return Loss		15			15		dB
Output Return Loss		15			15		dB
Input P0.1 dB		26.5			26.5		dBm
Input IP3		42			42		dBm

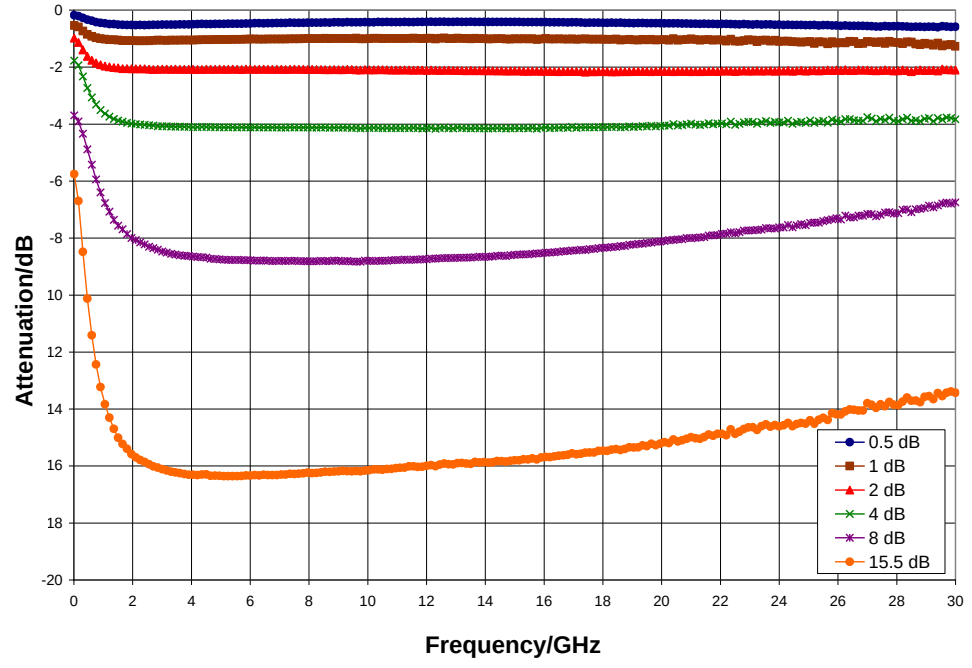
Note: Specification applies to major states

Typical Performance

Insertion Loss versus Temperature

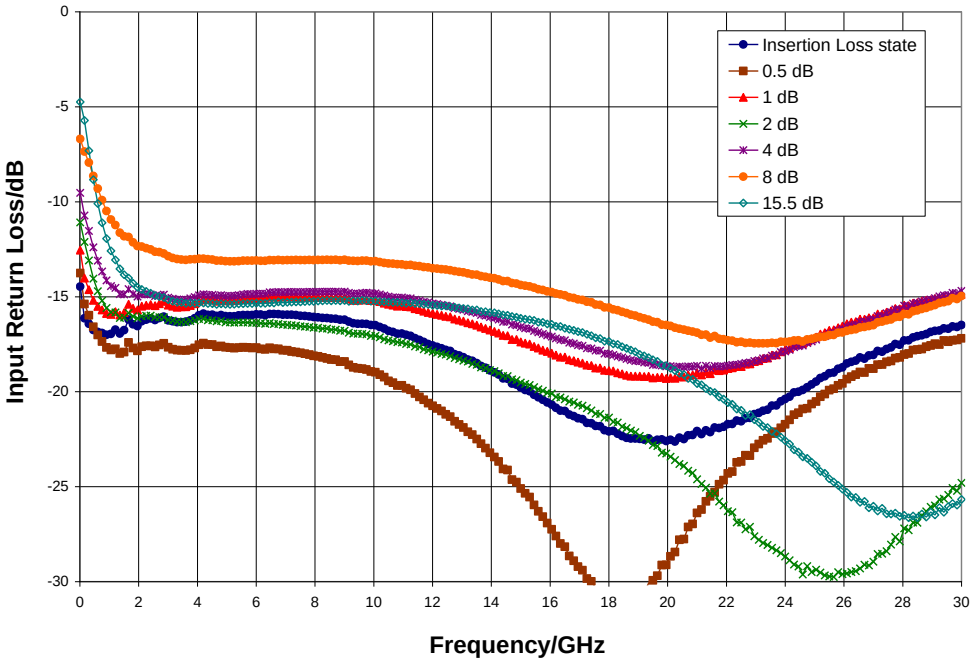


Normalized Attenuation (major states only), T_A = 25° C

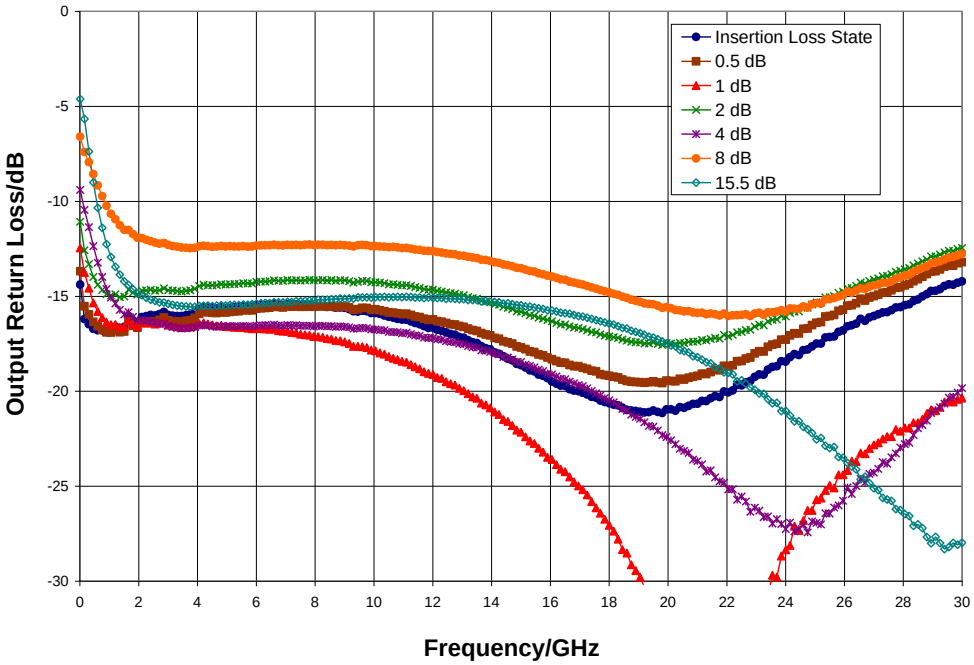


Typical Performance

Input Return Loss (major states only), T_A = 25° C

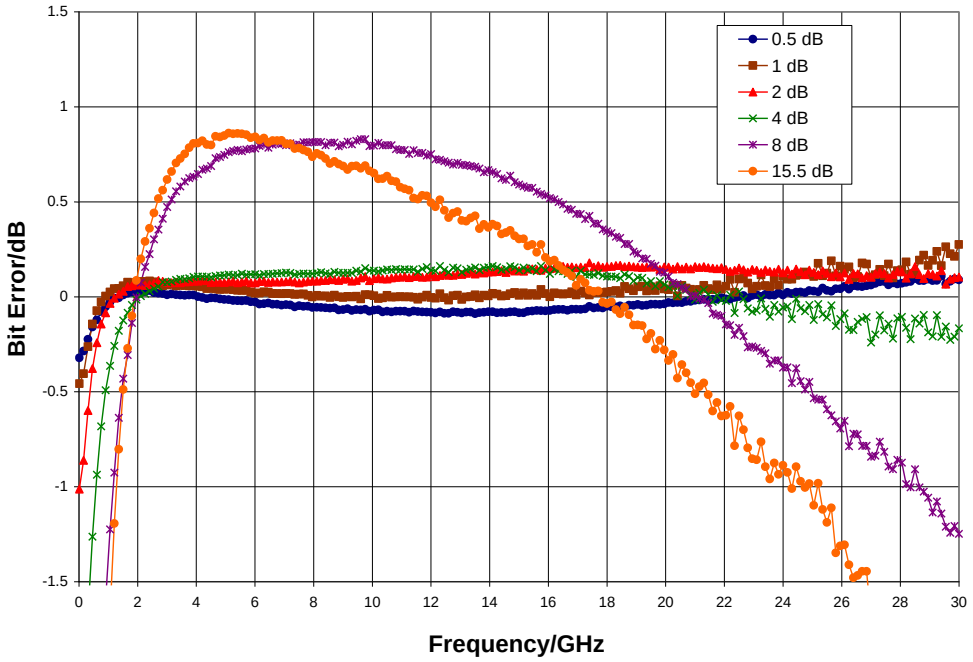


Output Return Loss (major states only), T_A = 25° C

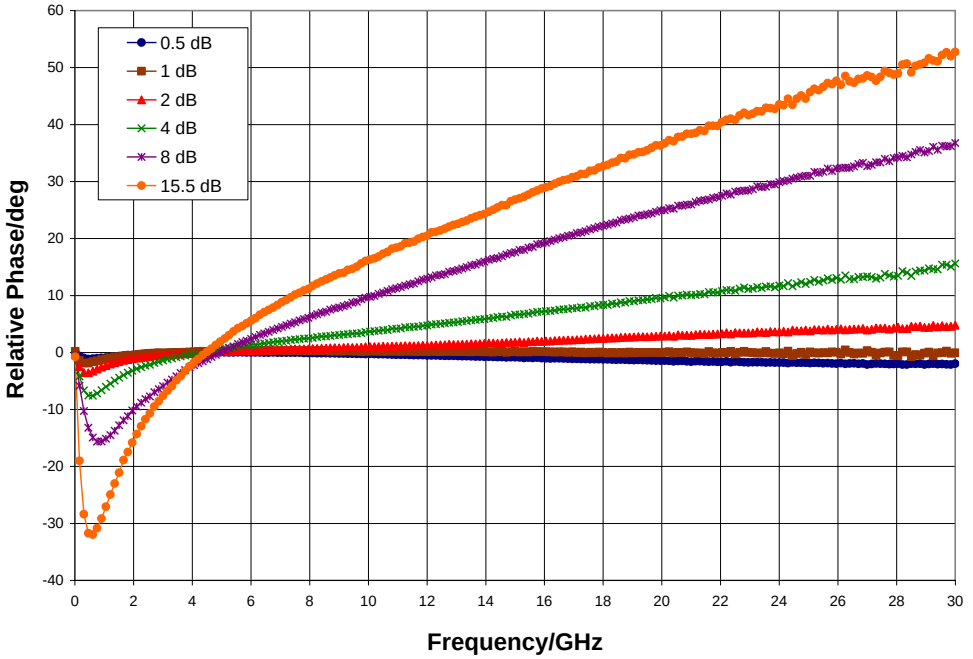


Typical Performance

Bit Error versus Frequency, T_A = 25° C

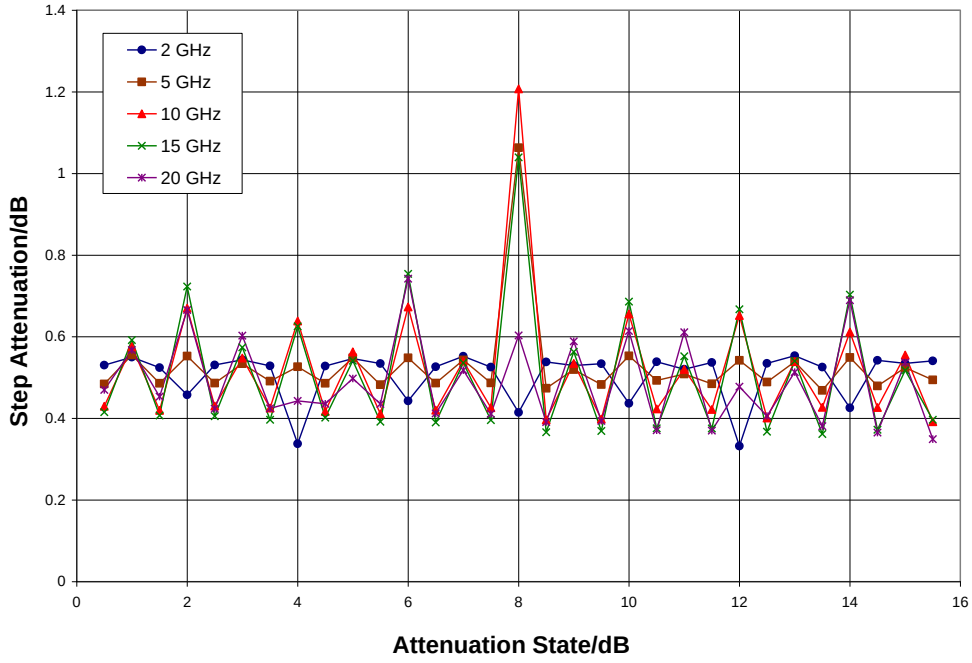


Relative Phase versus Frequency, T_A = 25° C

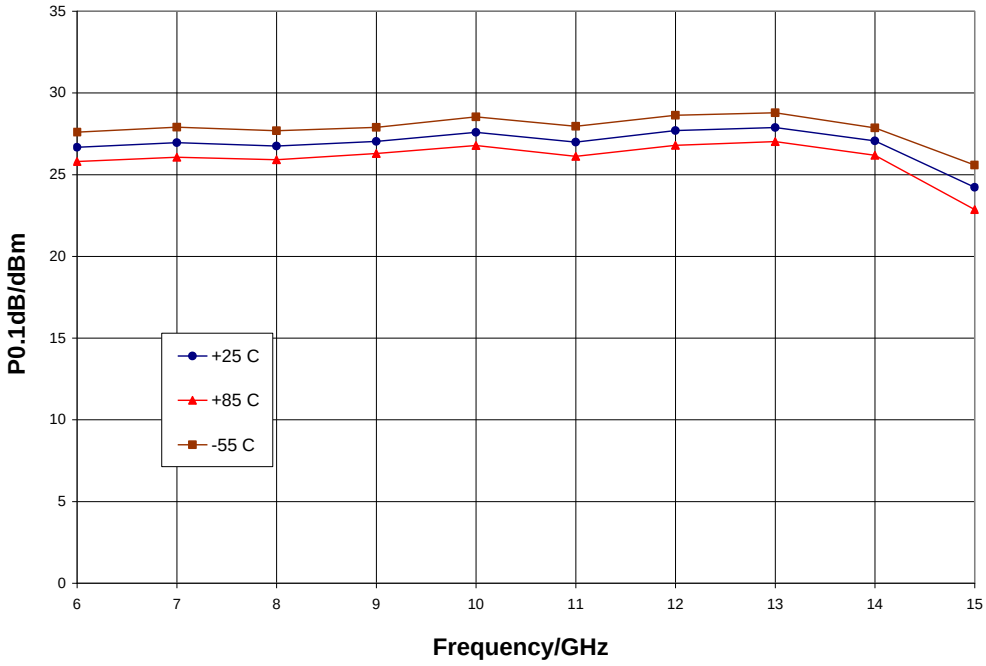


Typical Performance

Step Attenuation versus Attenuation State, T_A = 25° C

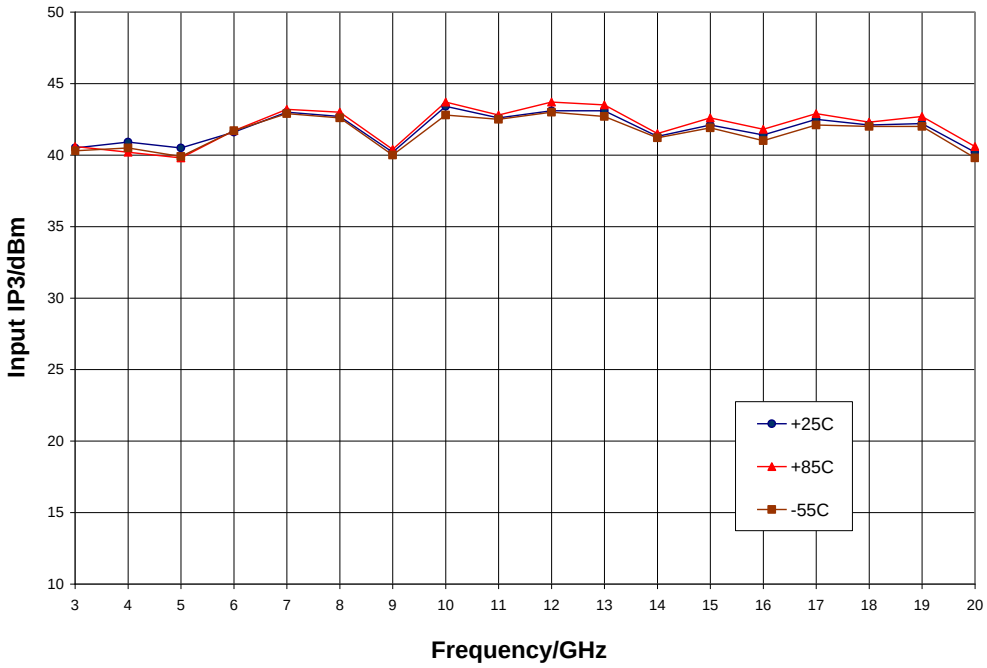


Input Power for 0.1 dB Compression (insertion loss state)



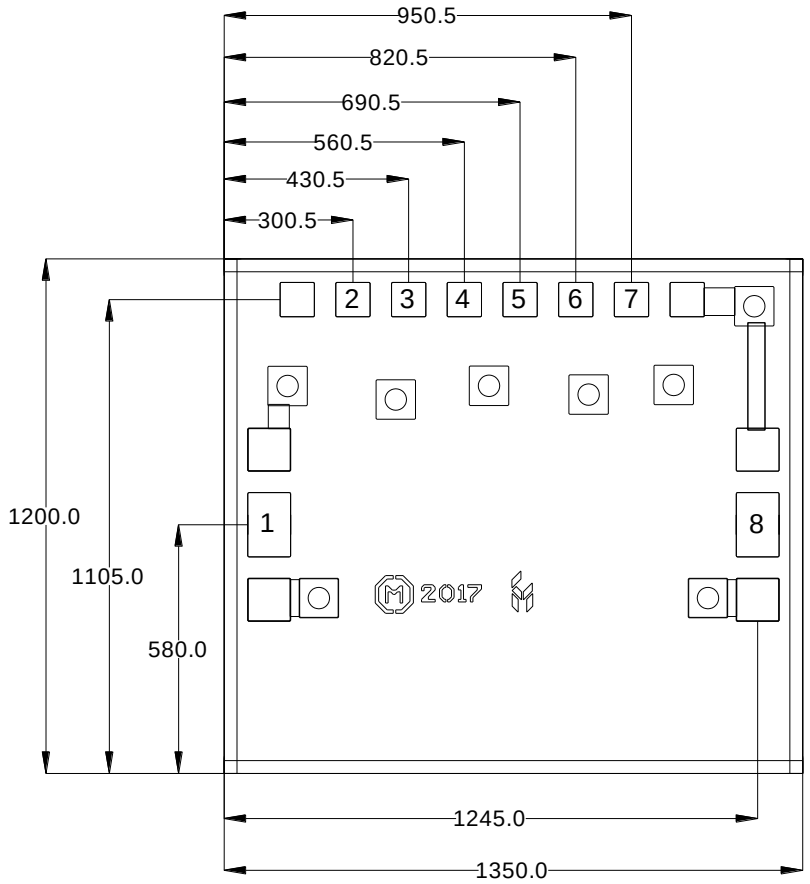
Typical Performance

Input IP3 versus Temperature (insertion loss state)



Mechanical Information

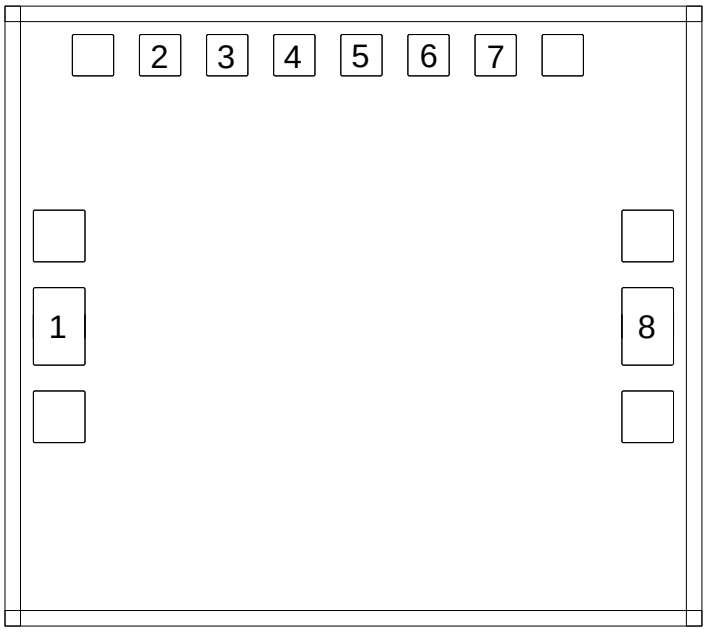
Die Outline (all dimensions in microns)



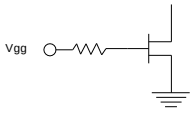
Notes:
1. No connection required for unlabeled pads
2. Backside is RF and DC ground
3. Backside and bond pad metal: Gold
4. Die is 100 microns thick
5. DC bond pads (2, 3, 4, 5, 6, 7) are 80 x 80 microns square
6. RF bond pads (1, 8) are 100 x 150 microns

Pad Description

Pad Diagram



Functional Description

Pad	Function	Description	Schematic
1, 8	RF1, RF2	DC coupled, 50 ohm matched. External blocking capacitors are required	
2	V_{dd}	Positive bias +5 V	
3, 4, 5, 6, 7	P0 - P4	Bit control voltages, see truth table for values	
Backside	Ground	Connect to RF / DC ground	

Applications Information

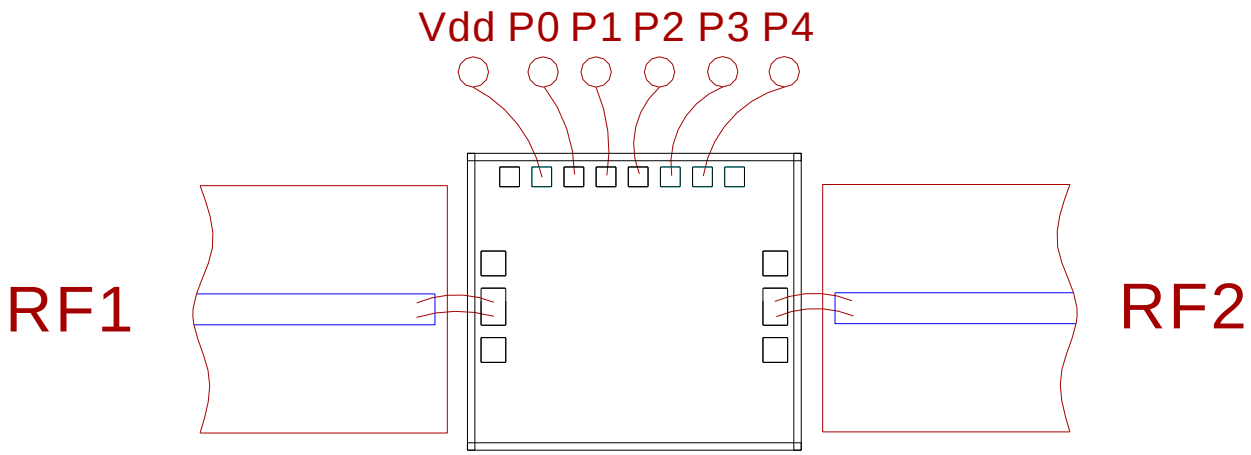
Assembly Guidelines

The backside of the CMD279 is RF ground. Die attach should be accomplished with electrically and thermally conductive epoxy only. Eutectic attach is not recommended. Standard assembly procedures should be followed for high frequency devices. The top surface of the semiconductor should be made planar to the adjacent RF transmission lines, and the RF decoupling capacitors placed in close proximity to the DC connections on chip.

RF connections should be made as short as possible to reduce the inductive effect of the bond wire. Use of a 0.8 mil thermosonic wedge bonding is highly recommended as the loop height will be minimized. The RF input and output require a single bond wire as shown.

The semiconductor is 100 um thick and should be handled by the sides of the die or with a custom collet. Do not make contact directly with the die surface as this will damage the monolithic circuitry. Handle with care.

Assembly Diagram



Biasing and Operation

The CMD279 has five control lines and a V_{dd} bias port. The CMD279 will not operate unless V_{dd} is applied to the MMIC.

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test