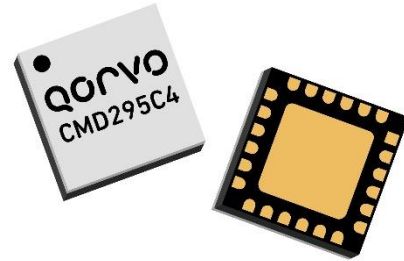
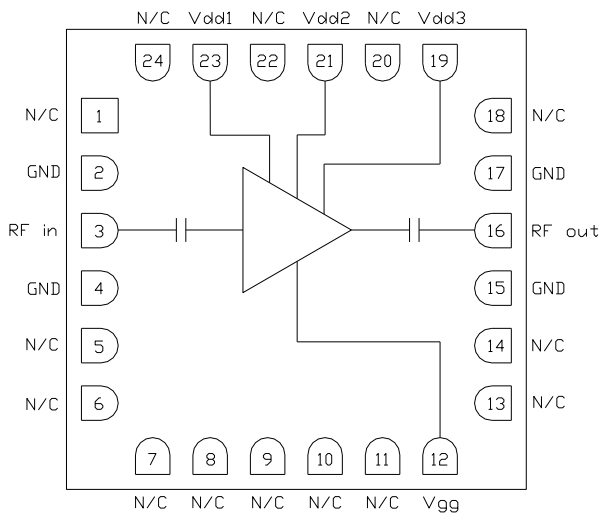


Product Overview

The CMD295C4 is a wideband driver amplifier housed in a leadless surface mount package ideally suited for military, space and communications systems where small size and high linearity are needed. At 10 GHz the device delivers greater than 27 dB of gain with a corresponding output 1 dB compression point of +16 dBm and an output IP3 of 29 dBm. The CMD295C4 is a 50 ohm matched design which eliminates the need for external DC blocks and RF port matching.



Functional Block Diagram



Key Features

- Wide Bandwidth
- High Linearity
- Low Current Consumption
- Pb-Free RoHs Compliant 4x4 mm SMT Package

Ordering Information

Part No.	Description
CMD295C4	100 pcs on 7" reel
CMD295C4-EVB	Evaluation Board

Electrical Performance ($V_{dd} = 3.0\text{ V}$, $V_{gg} = 2.0\text{V}$, $T_A = 25^\circ\text{C}$, $F = 10\text{ GHz}$)

Parameter	Min	Typ	Max	Units
Frequency Range		2 - 20		GHz
Gain		27		dB
Noise Figure		3		dB
Input Return Loss		12		dB
Output Return Loss		18		dB
Output P1dB		16		dBm
Output IP3		29		dBm
Output IP2 (sum term, $f_1 + f_2$)		37		dBm
Supply Current		145		mA

Absolute Maximum Ratings

Parameter	Rating
Drain Voltage, V_{dd}	4.25 V
Gate Voltage, V_{gg}	3 V
RF Input Power	+20 dBm
Channel Temperature, T_{ch}	150° C
Power Dissipation, P_{diss}	681 mW
Thermal Resistance, Q_{jC}	95° C/W
Operating Temperature	-40 to 85° C
Storage Temperature	-55 to 150° C

Exceeding any one or combination of the maximum ratings may cause permanent damage to the device.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{dd}	2.0	3.0	4.0	V
I_{dd}		145		mA
V_{gg}		2.0		V
I_{gg}		1		mA

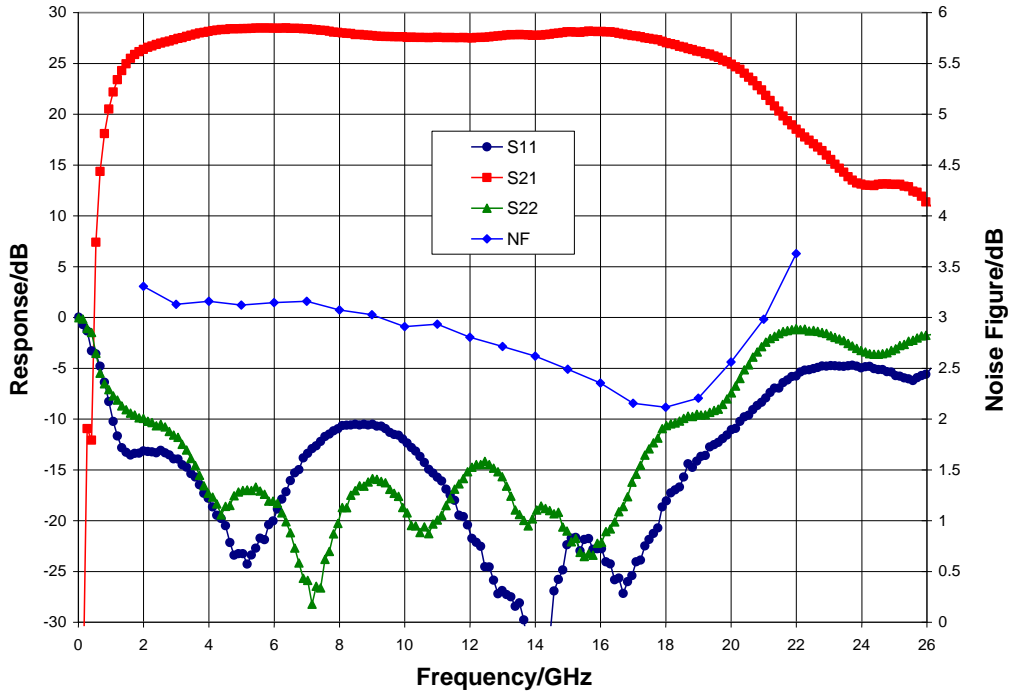
Electrical performance is measured at specific test conditions. Electrical specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications ($V_{dd} = 3.0$ V, $V_{gg} = 2.0$ V, $T_A = 25$ °C)

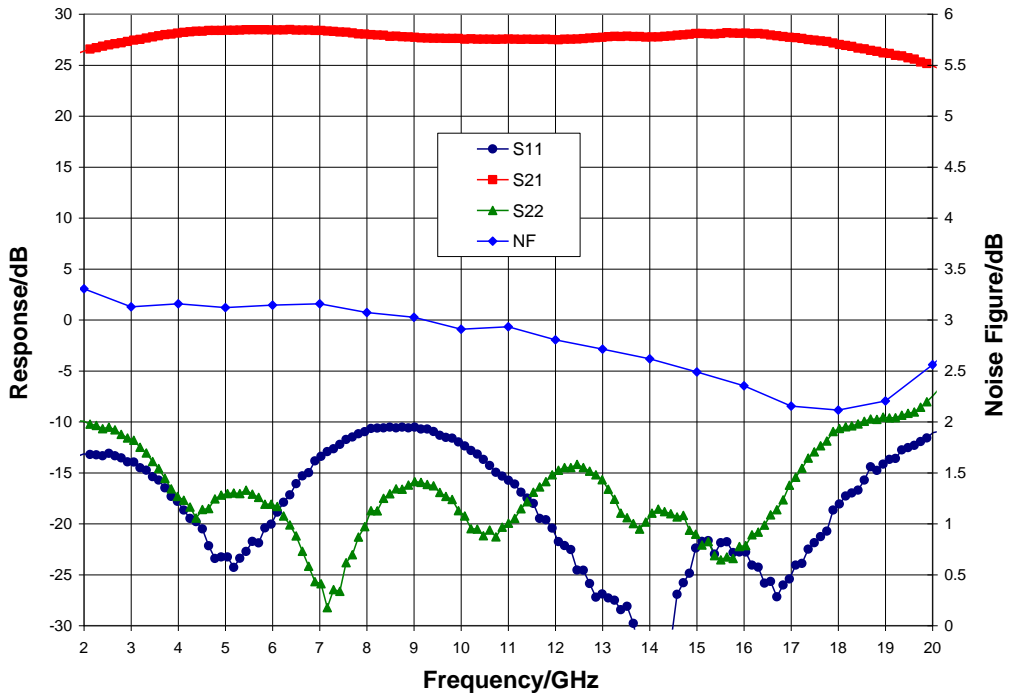
Parameter	Min	Typ	Max	Min	Typ	Max	Units
Frequency Range		2 - 18			18 - 20		GHz
Gain	23.5	27.5		22	26		dB
Noise Figure		3			2.5		dB
Input Return Loss		13			13		dB
Output Return Loss		15			10		dB
Output P1dB	13	16		13	16		dBm
Output IP3		29			26.5		dBm
Output IP2 (sum term, $f_1 + f_2$)		35			33		dBm
Supply Current	95	145	190	95	145	190	mA
Gain Temperature Coefficient		0.018			0.018		dB/°C
Noise Figure Temperature Coefficient		0.01			0.01		dB/°C

Typical Performance

Broadband Performance, $V_{dd} = 3.0\text{ V}$, $V_{gg} = 2.0\text{ V}$, $I_{dd} = 135\text{ mA}$, $T_A = 25^\circ\text{ C}$

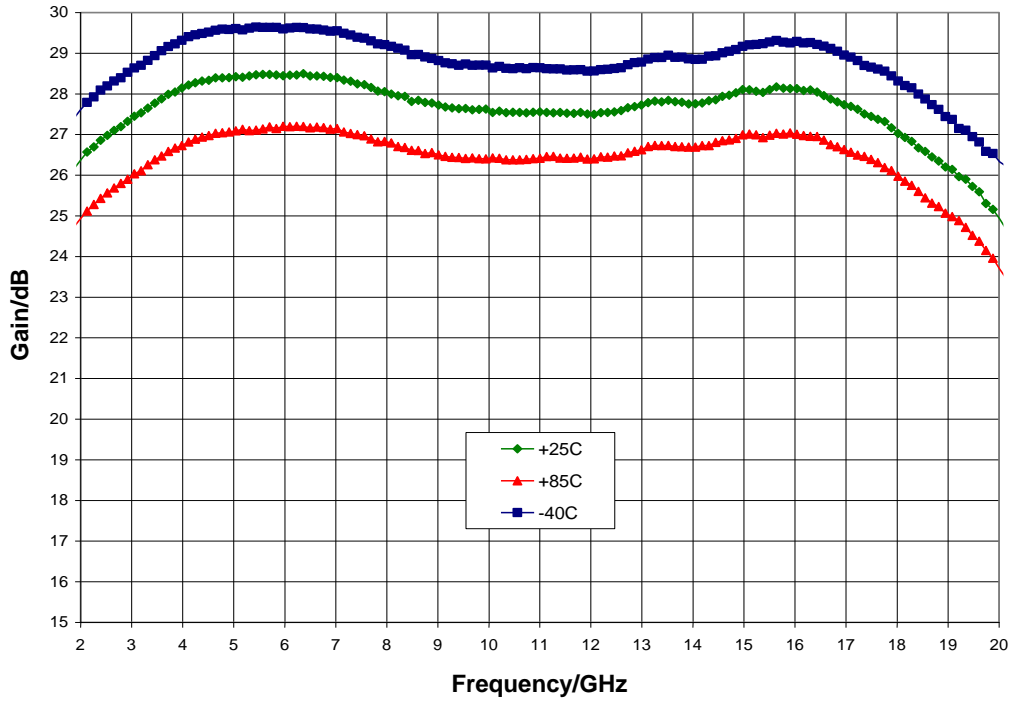


Narrow-band Performance, $V_{dd} = 3.0\text{ V}$, $V_{gg} = 2.0\text{ V}$, $I_{dd} = 135\text{ mA}$, $T_A = 25^\circ\text{ C}$

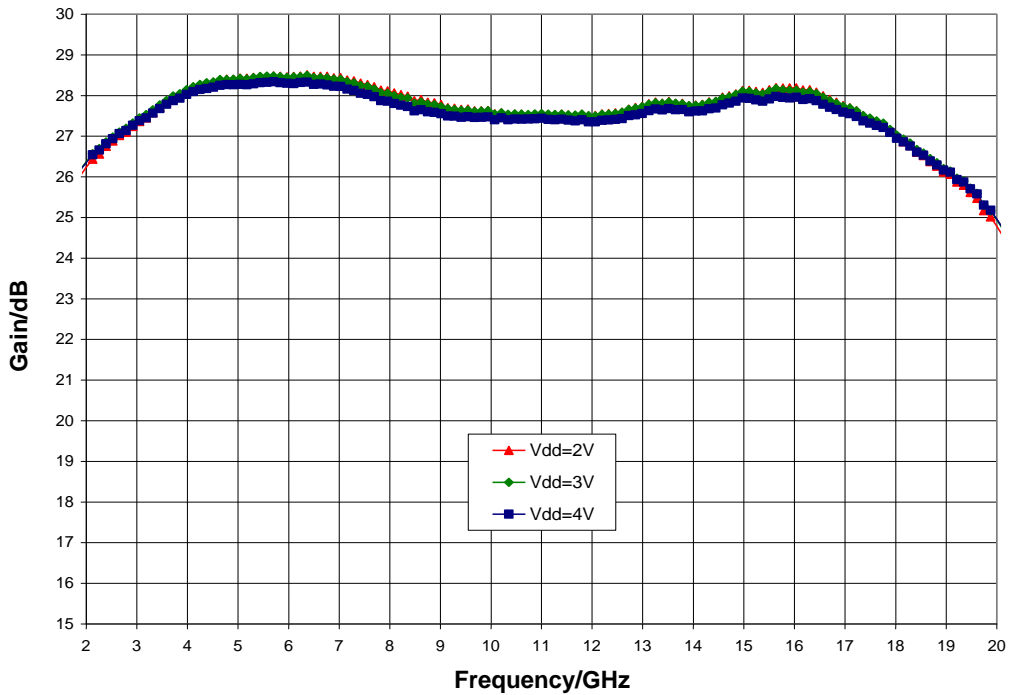


Typical Performance

Gain vs. Temperature, $V_{dd} = 3.0\text{ V}$, $V_{gg} = 2.0\text{ V}$

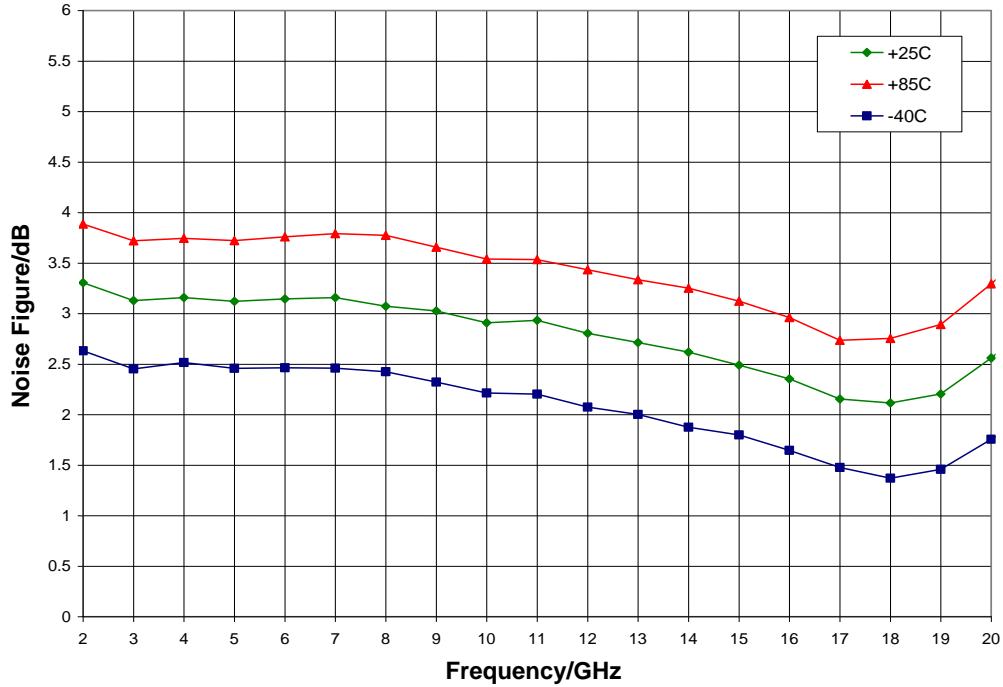


Gain vs. V_{dd} , $V_{gg} = 2.0\text{ V}$, $T_A = 25^\circ\text{ C}$

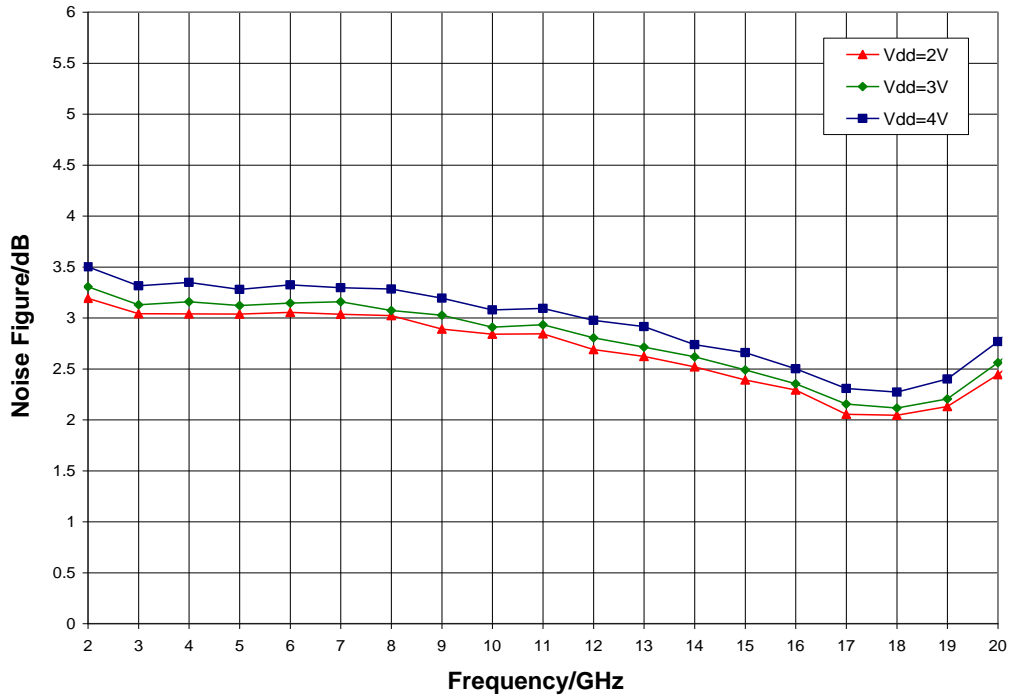


Typical Performance

Noise Figure vs. Temperature, $V_{dd} = 3.0\text{ V}$, $V_{gg} = 2.0\text{ V}$

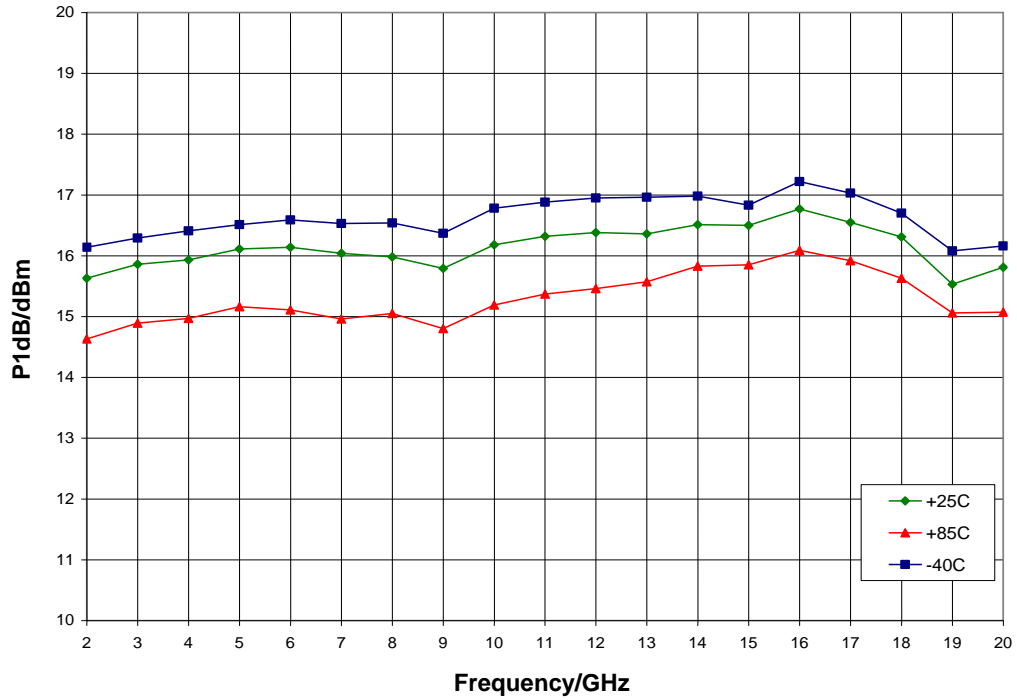


Noise Figure vs. V_{dd} , $V_{gg} = 2.0\text{ V}$, $T_A = 25^\circ\text{ C}$

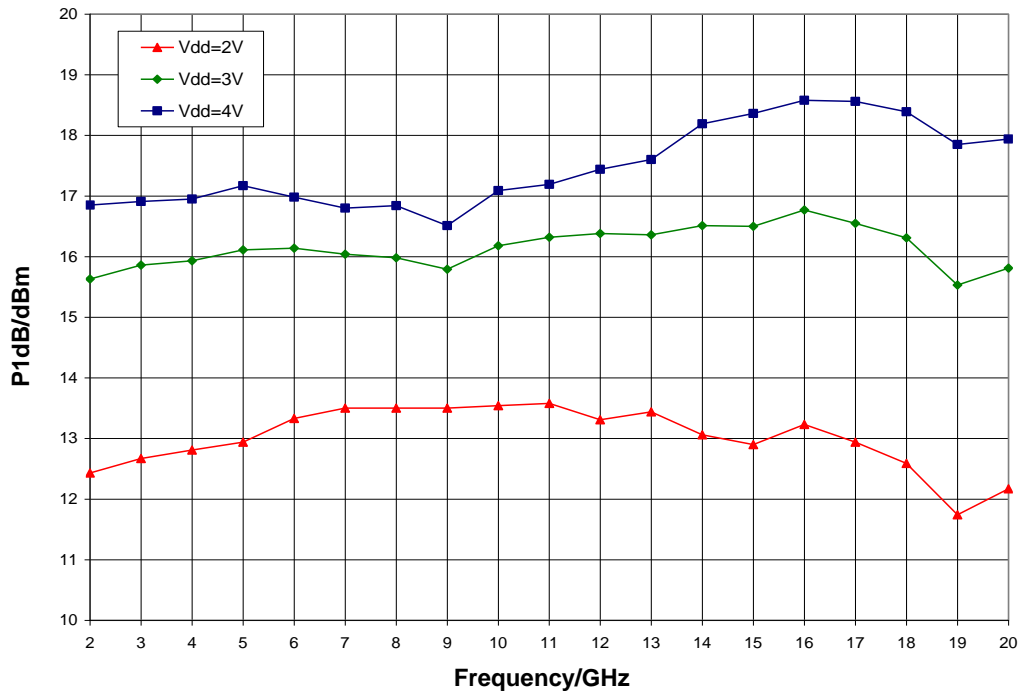


Typical Performance

P1dB vs. Temperature, $V_{dd} = 3.0\text{ V}$, $V_{gg} = 2.0\text{ V}$

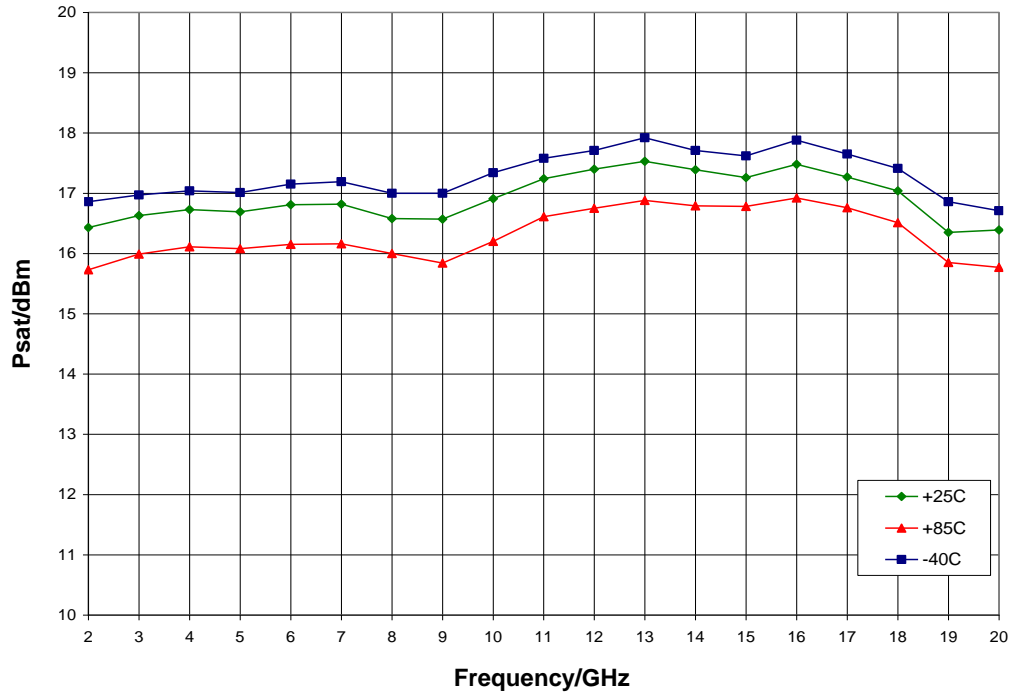


P1dB vs. V_{dd} , $V_{gg} = 2.0\text{ V}$, $T_A = 25^\circ\text{ C}$

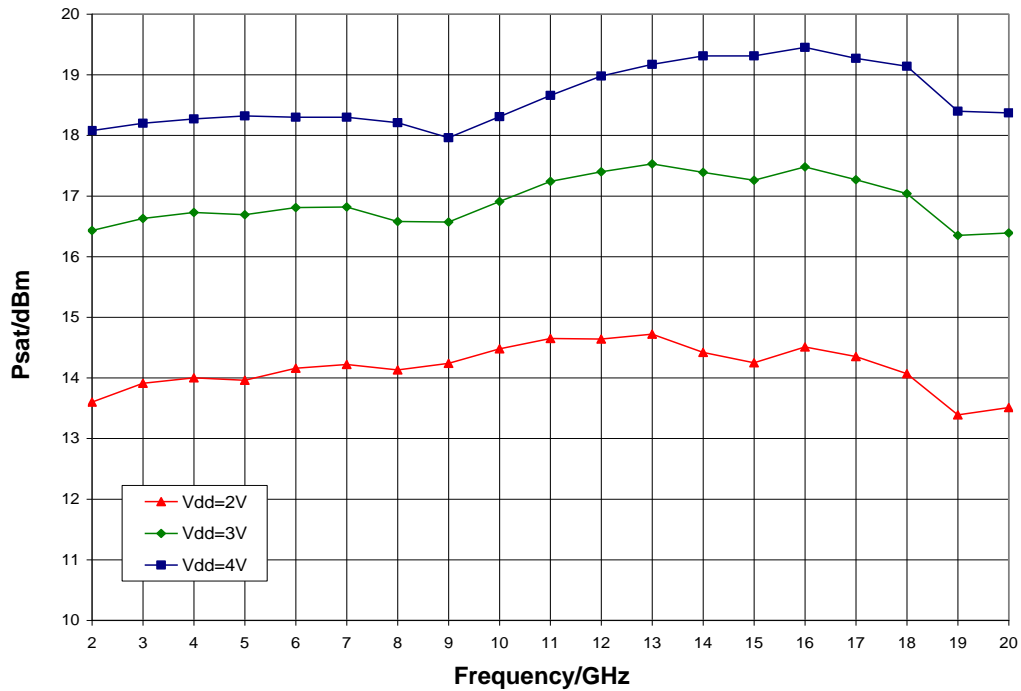


Typical Performance

Psat vs. Temperature, $V_{dd} = 3.0\text{ V}$, $V_{gg} = 2.0\text{ V}$

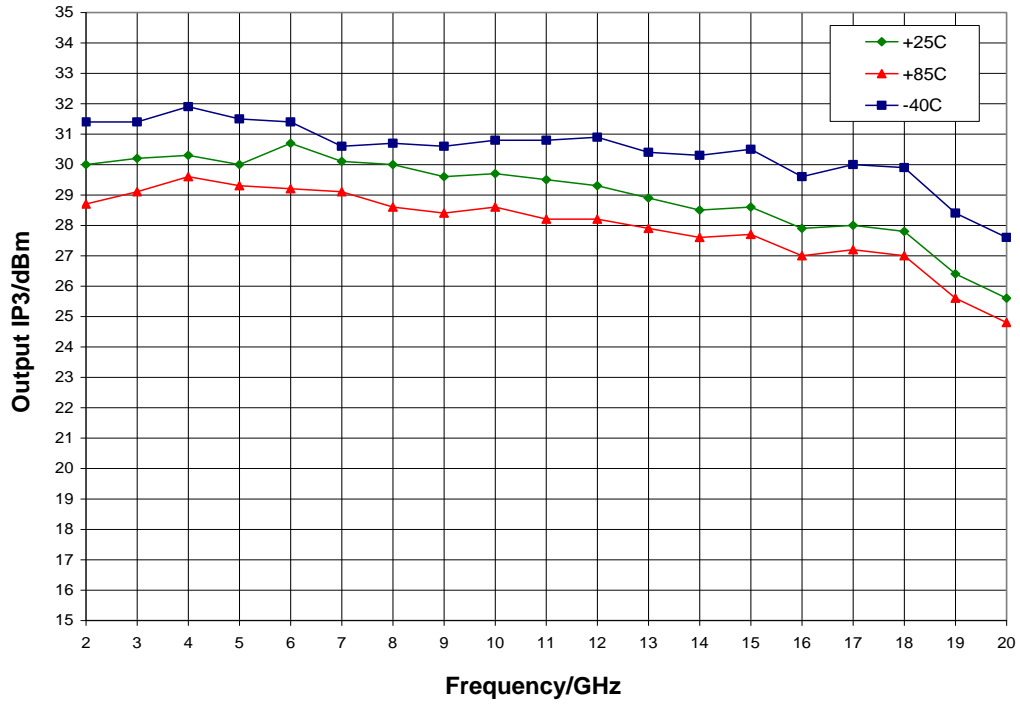


Psat vs. V_{dd} , $V_{gg} = 2.0\text{ V}$, $T_A = 25^\circ\text{ C}$

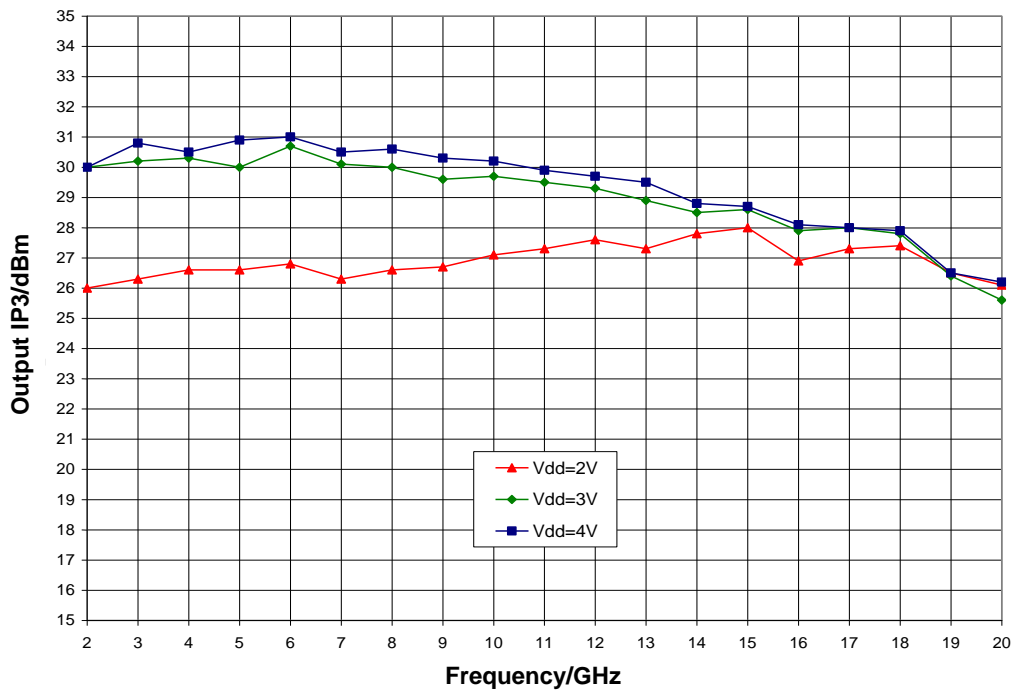


Typical Performance

Output IP3 vs. Temperature, $V_{dd} = 3.0\text{ V}$, $V_{gg} = 2.0\text{ V}$

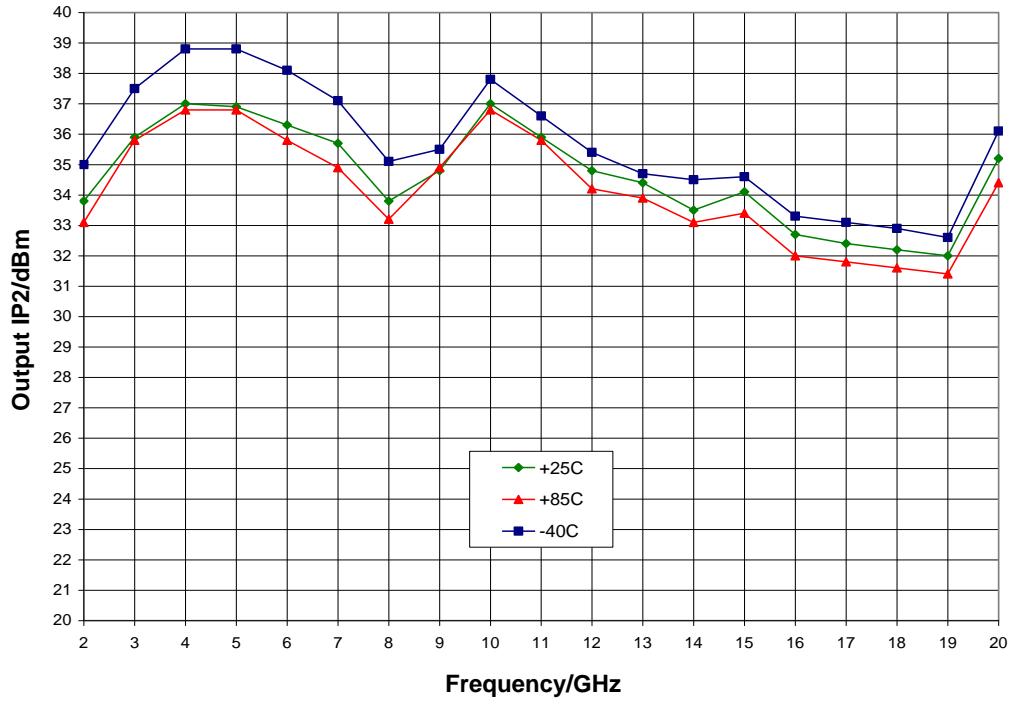


Output IP3 vs. V_{dd} , $V_{gg} = 2.0\text{ V}$, $T_A = 25^\circ\text{ C}$

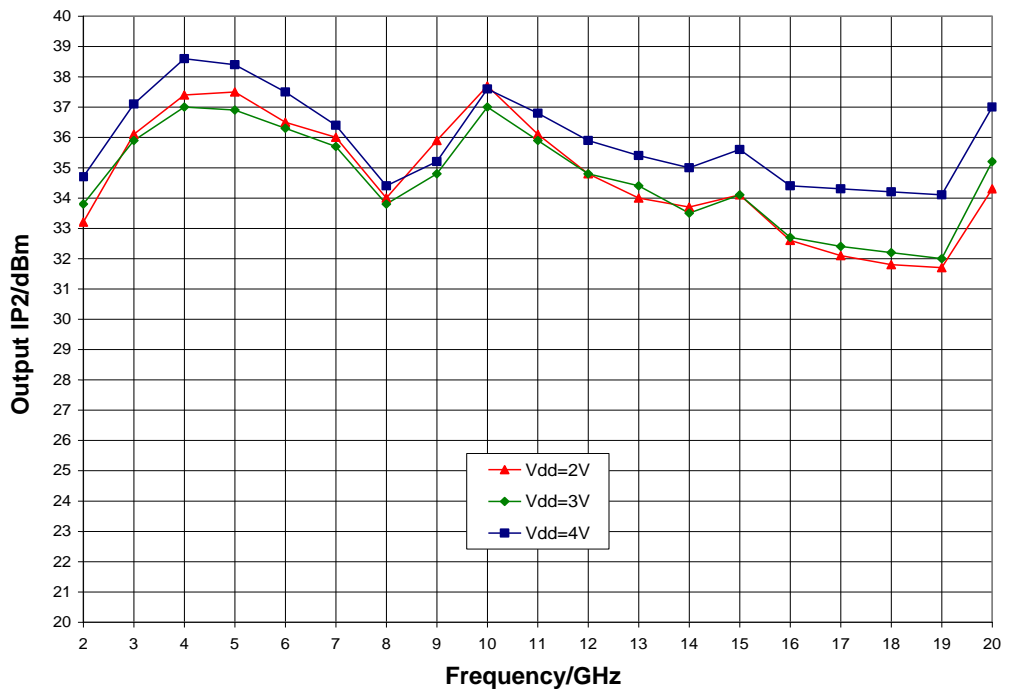


Typical Performance

Output IP2 vs. Temperature, $V_{dd} = 3.0\text{ V}$, $V_{gg} = 2.0\text{ V}$

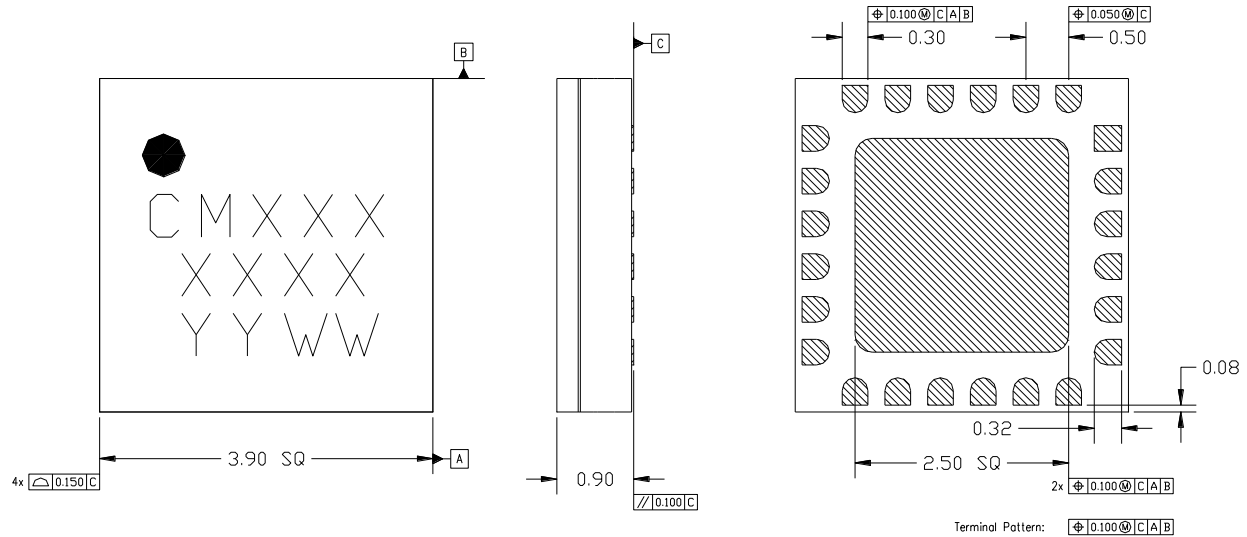


Output IP2 vs. V_{dd} , $V_{gg} = 2.0\text{ V}$, $T_A = 25^\circ\text{ C}$



Mechanical Information

Package Information and Dimensions



Notes:

- All dimensions shown in mm.
- Material: Black alumina
- Lead finish
 - Ni: 8.89 μ m max, 1.27 μ m min
 - Pd: 0.17 μ m max, 0.07 μ m min
 - Au: 0.254 μ m max, 0.03 μ m min
- Marking
 - Line 1: Part number
 - Example: CMD191C4 shall be marked as CM191
 - Line 2: Lot number
 - Line 3: Date code - Last 2 digits of the year of manufacture followed by a 2 digit week code
- Alternate pin #1 identifier is a single square pad
- Alternate die paddle may have chamfered corners

Recommended PCB Land Pattern

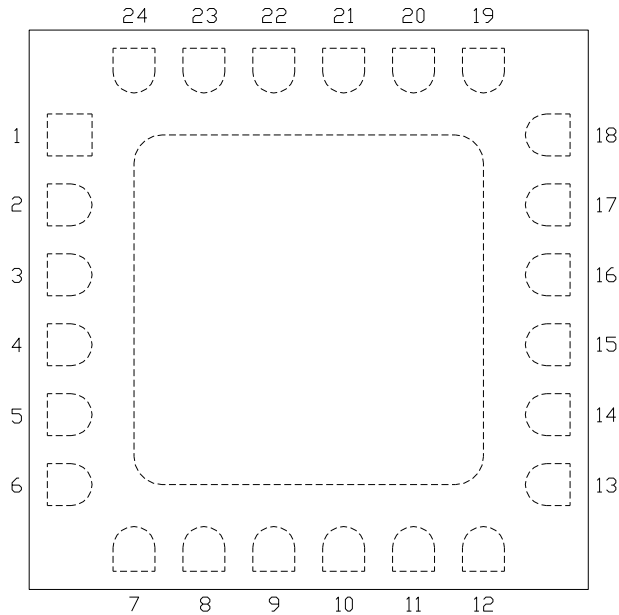
Qorvo recommends that the user develop the land pattern that will provide the best design for proper solder reflow and device attach for their specific application. Please review Qorvo Application Note AN 105 for a recommended land pattern approach.

Recommended Solder Reflow Profile

Qorvo recommends screen printing with belt furnace reflow to ensure proper solder reflow and device attach. Please review Qorvo Application Note AN 102 for a recommended solder reflow profile.

Pin Description

Pin Diagram

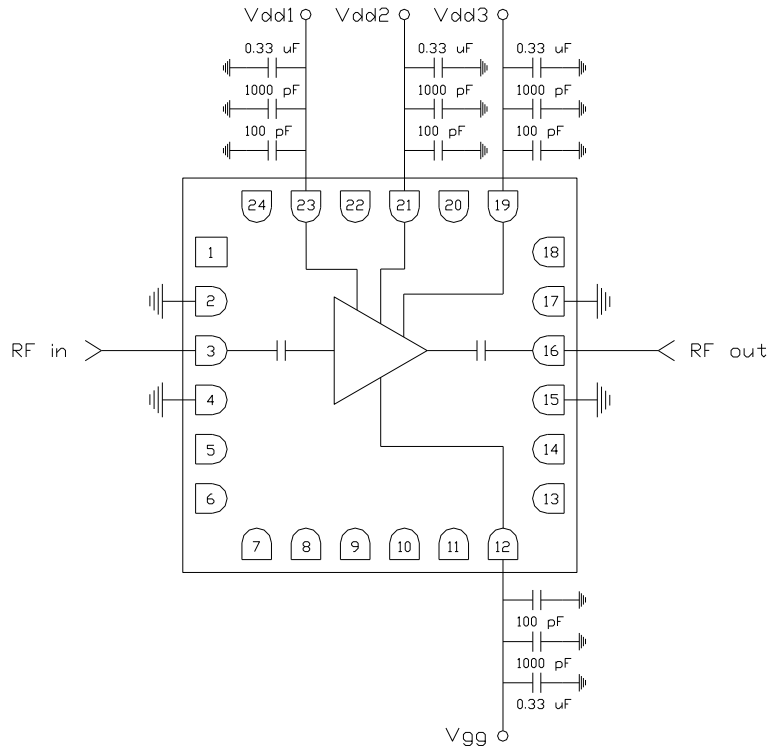


Functional Description

Pad	Function	Description	Schematic
1, 5 - 11, 13, 14, 18, 20, 22, 24	N/C	No connection required These pins may be connected to RF / DC ground	
2, 4, 15, 17 and die paddle	Ground	Connect to RF / DC ground	
3	RF in	DC blocked and 50 ohm matched	
12	V_{gg}	Power supply voltage Decoupling and bypass caps required	
16	RF out	DC blocked and 50 ohm matched	
23, 21, 19	$V_{dd1, 2, 3}$	Power supply voltage Decoupling and bypass caps required	

Applications Information

Application Circuit



Biasing and Operation

The CMD295C4 is biased with a positive drain supply and positive gate supply. Sequencing of the drain and gate supply is not required. Performance is optimized when the drain voltage is set to +3.0 V. The recommended gate voltage is +2.0 V.

Recommended turn on procedure:

1. Apply drain voltages $V_{dd1,2,3}$ and set to +3 V
2. Apply gate voltage V_{gg} and set to +2 V

Recommended turn off procedure:

1. Turn off gate voltage V_{gg}
2. Turn off drain voltages $V_{dd1,2,3}$

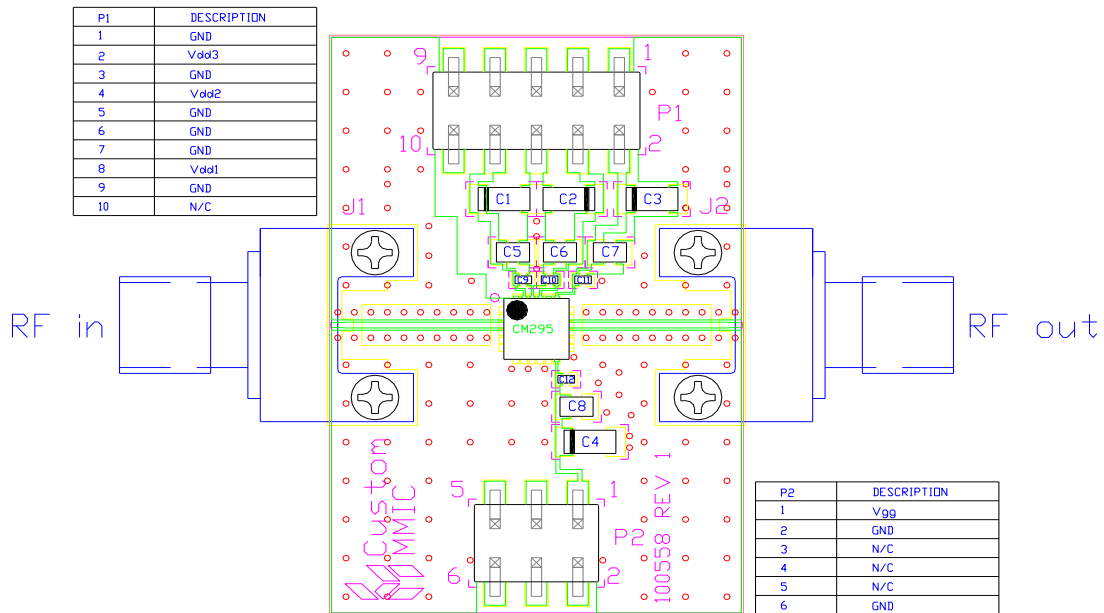
Refer to Application Note 103: Amplifier Biasing Techniques for instructions on how to implement a single supply biasing scheme.

RF power can be applied at any time.

Applications Information

Evaluation Board

The circuit board shown has been developed for optimized assembly at Qorvo. A sufficient number of via holes should be used to connect the top and bottom ground planes. As surface mount processes vary, careful process development is recommended.



Bill of Material

Designator	Value	Description
J1, J2		SMA End Launch Connector
P1		10 Pin Header
P2		6 Pin Header
C1 - C4	0.33 μ F	Capacitor, Tantalum
C5 - C8	1000 pF	Capacitor, 0603
C9 - C12	100 pF	Capacitor, 0402
U1		CMD295C4 Driver Amplifier
PCB		100558 Evaluation PCB

GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.