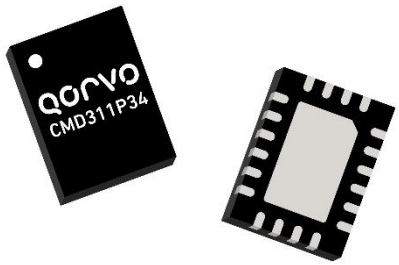
CMD311P34

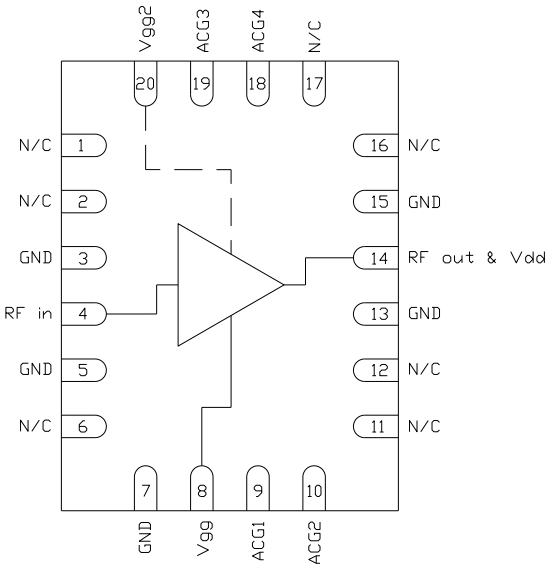
DC-20 GHz Distributed Driver Amplifier

Product Overview

The CMD311P34 is wideband GaAs MMIC distributed amplifier housed in a leadless 3x4 mm plastic surface mount package. The amplifier operates from DC to 20 GHz and delivers greater than 12 dB of gain with a corresponding output 1 dB compression point of +11 dBm and noise figure of 2.5 dB at 10 GHz. The CMD311P34 is a 50 ohm matched design which eliminates the need for RF port matching.



Functional Block Diagram



Note: V_{gg2} is optional for gain control

Key Features

- Wideband Performance
- Low Noise Figure
- High Linearity
- Low Current Consumption
- Pb-Free RoHs Compliant 3x4 QFN Package

Ordering Information

Part No.	Description
CMD311P34	100 pcs on 7” reel
CMD311P34-EVB	Evaluation Board

Electrical Performance (V_{dd} = 5.0 V, V_{gg} = 5.0 V, T_A = 25° C, F = 10 GHz)

Parameter	Min	Typ	Max	Units
Frequency Range		DC - 20		GHz
Gain		12		dB
Noise Figure		2.5		dB
Input Return Loss		20		dB
Output Return Loss		20		dB
Output P1dB		11		dBm
Output IP3		22		dBm
Supply Current		40		mA

Absolute Maximum Ratings

Parameter	Rating
Drain Voltage, V_{dd}	9.0
Gate Voltage, V_{gg}	6.0
RF Input Power	+20 dBm
Channel Temperature, Tch	150° C
Power Dissipation, Pdiss	789 mW
Thermal Resistance, Q_{JC}	82.4° C/W
Operating Temperature	-40 to 85° C
Storage Temperature	-55 to 150° C

Exceeding any one or combination of the maximum ratings may cause permanent damage to the device.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{dd}	3.0	5.0	8.0	V
I_{dd}		40		mA
V_{gg}		5.0		V
I_{gg}		1.5		mA

Electrical performance is measured at specific test conditions. Electrical specifications are not guaranteed over all recommended operating conditions.

Drain Current vs. Drain Voltage

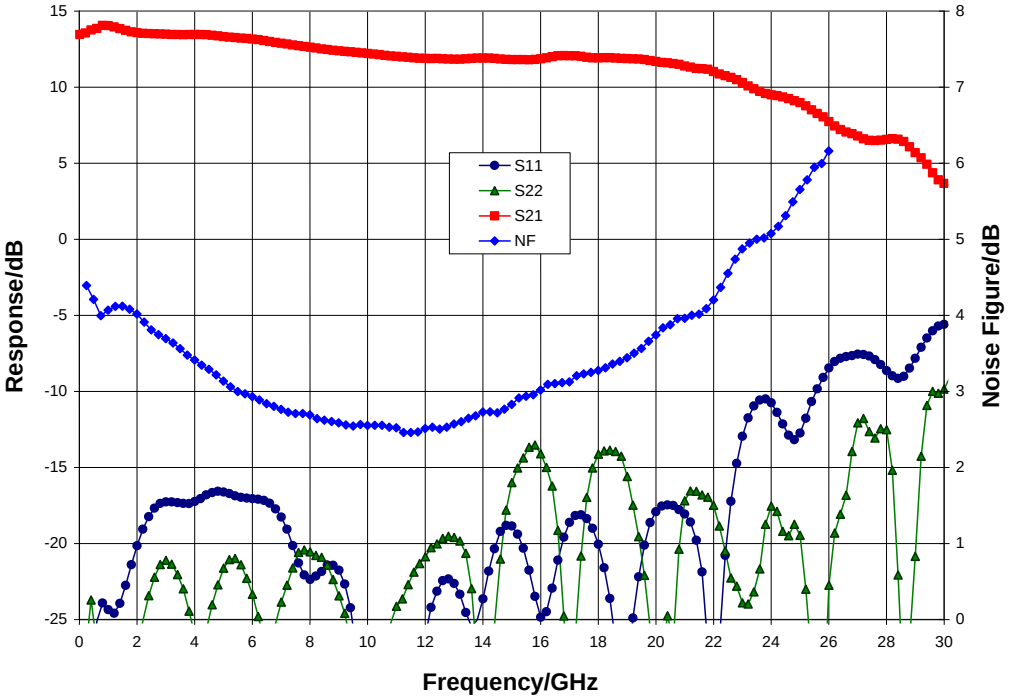
V_{dd} (V)	I_{dd} (mA)
3.0	19
4.0	29
5.0	40

Electrical Specifications (V_{dd} = 5.0 V, V_{gg} = 5.0 V, T_A = 25° C)

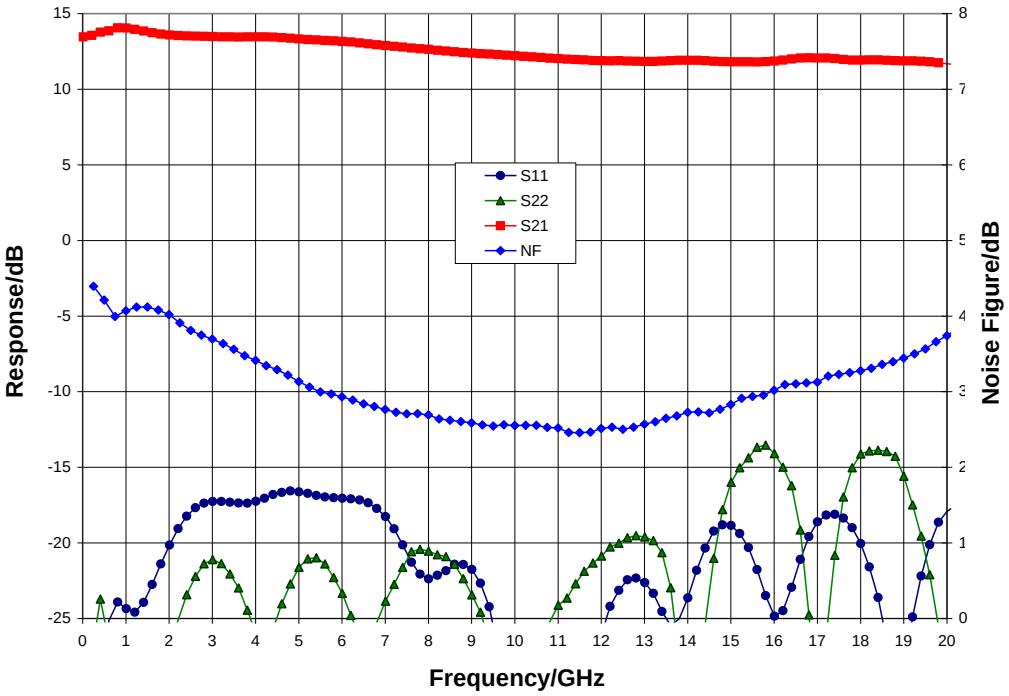
Parameter	Min	Typ	Max	Min	Typ	Max	Units
Frequency Range		DC - 10			10 - 20		GHz
Gain	9.5	13		9	12		dB
Noise Figure		3			3		dB
Input Return Loss		17			18		dB
Output Return Loss		22			15		dB
Output P1dB	8	11		7	10		dBm
Output IP3		22			20		dBm
Supply Current	28	40	52	28	40	52	mA
Gain Temperature Coefficient		0.013			0.02		dB/°C
Noise Figure Temperature Coefficient		0.01			0.015		dB/°C

Typical Performance

Broadband Performance, V_{dd} = 5.0 V, V_{gg} = 5.0 V, T_A = 25° C

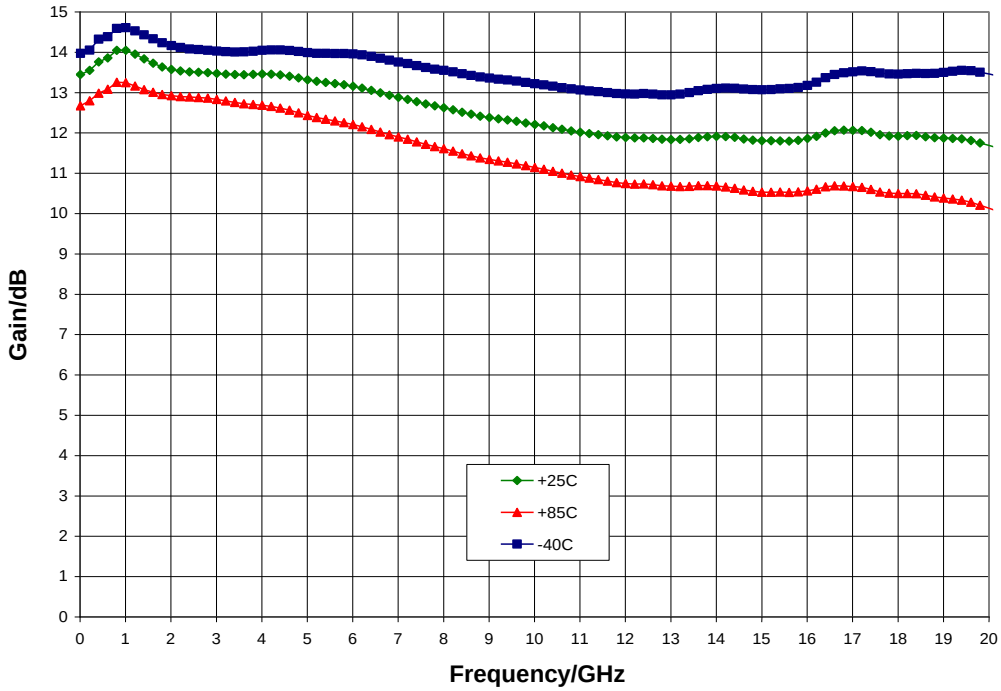


Narrow-band Performance, V_{dd} = 5.0 V, V_{gg} = 5.0 V, T_A = 25° C

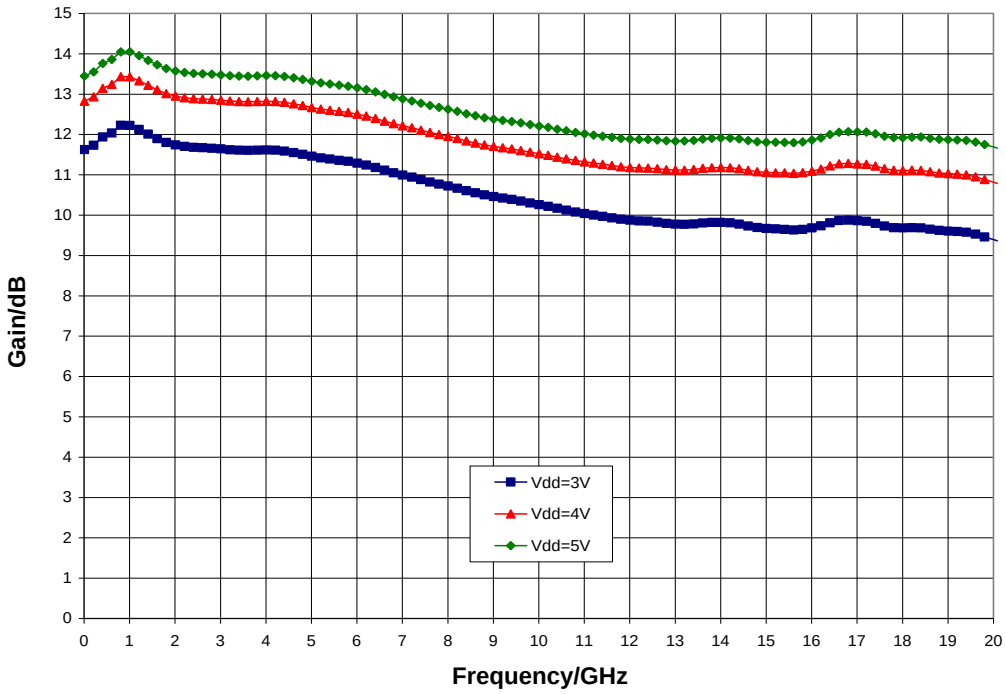


Typical Performance

Gain vs. Temperature, V_{dd} = 5.0 V, V_{gg} = 5.0 V

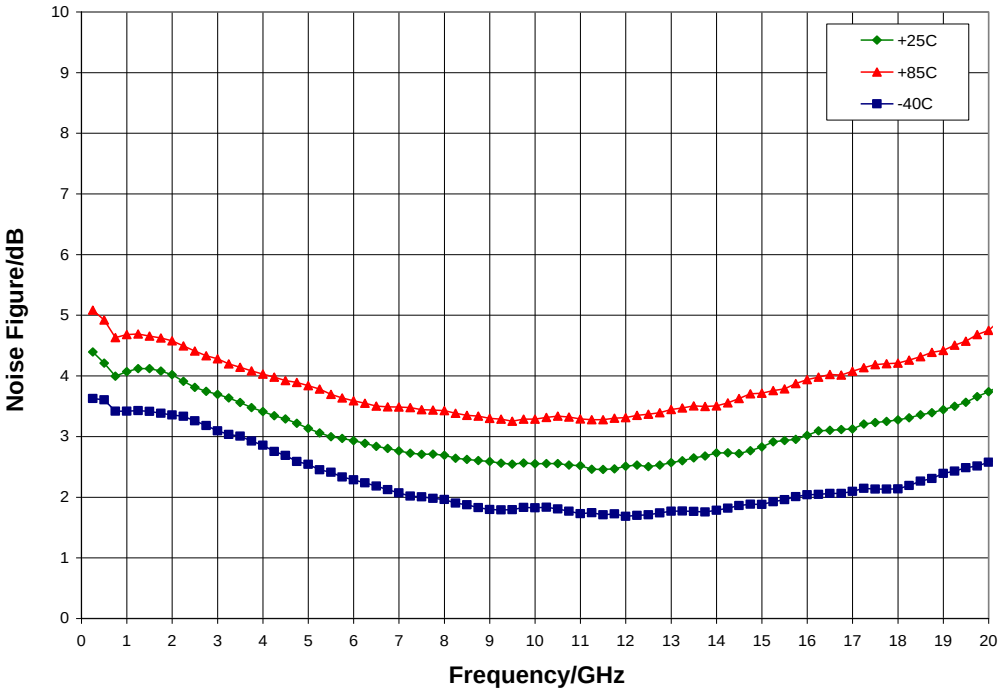


Gain vs. V_{dd}, V_{gg} = V_{dd}, T_A = 25° C

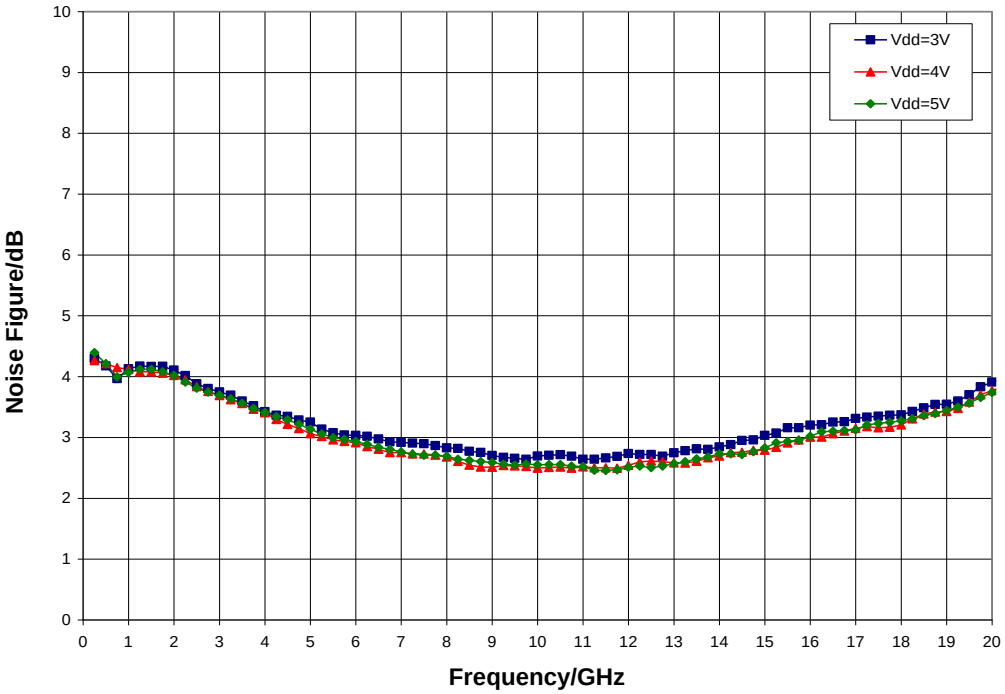


Typical Performance

Noise Figure vs. Temperature, V_{dd} = 5.0 V, V_{gg} = 5.0 V

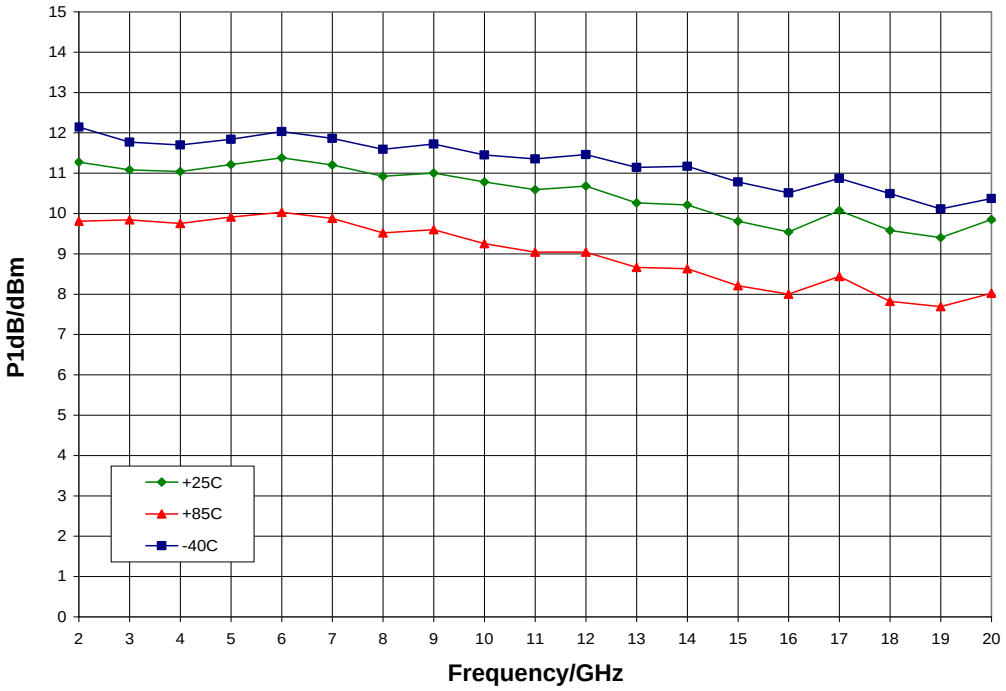


Noise Figure vs. V_{dd}, V_{gg} = V_{dd}, T_A = 25° C

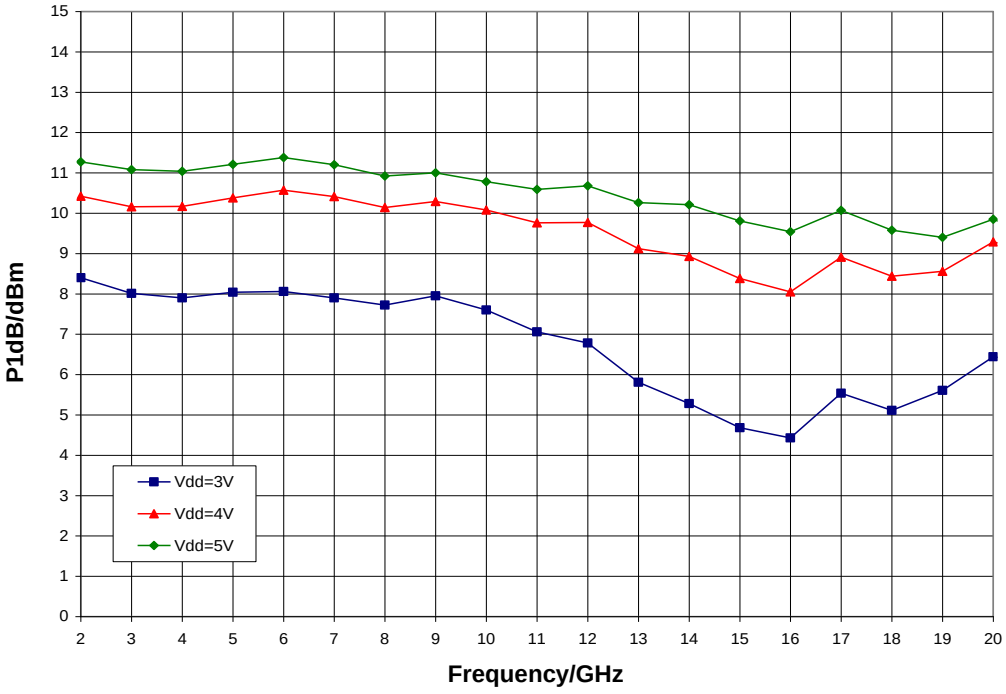


Typical Performance

P1dB vs. Temperature, V_{dd} = 5.0 V, V_{gg} = 5.0 V

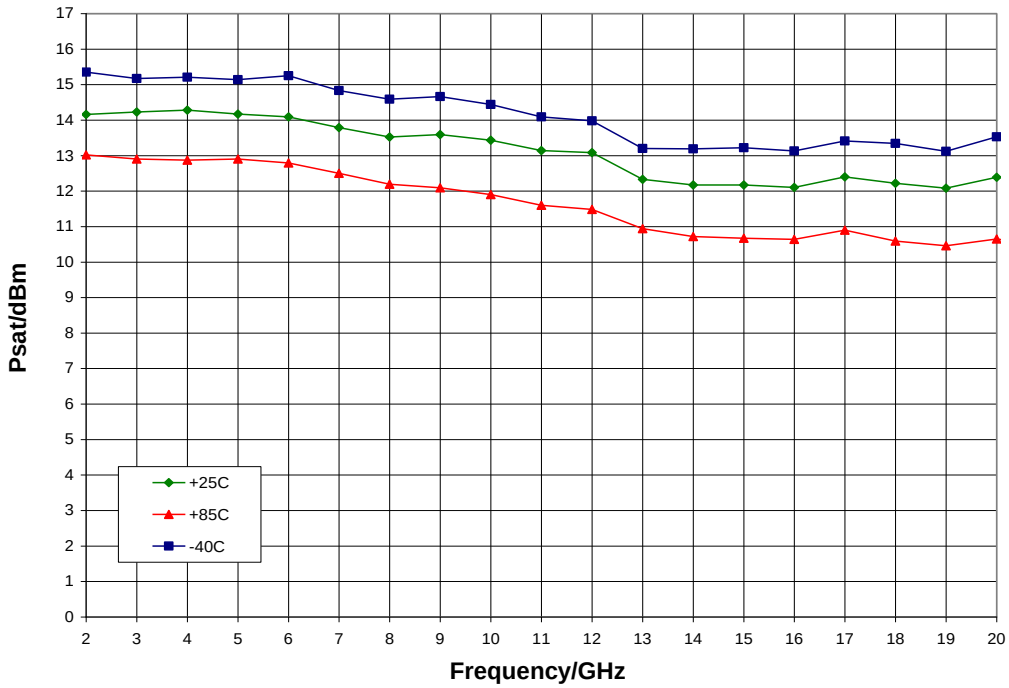


P1dB vs. V_{dd}, V_{gg} = V_{dd}, T_A = 25° C

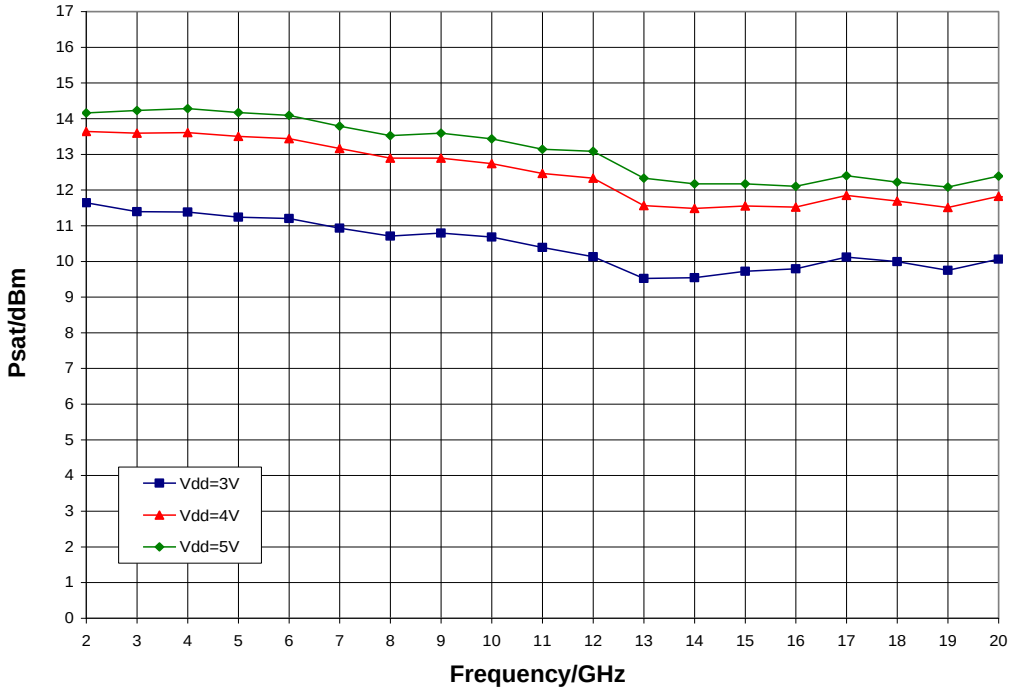


Typical Performance

Psat vs. Temperature, V_{dd} = 5.0 V, V_{gg} = 5.0 V

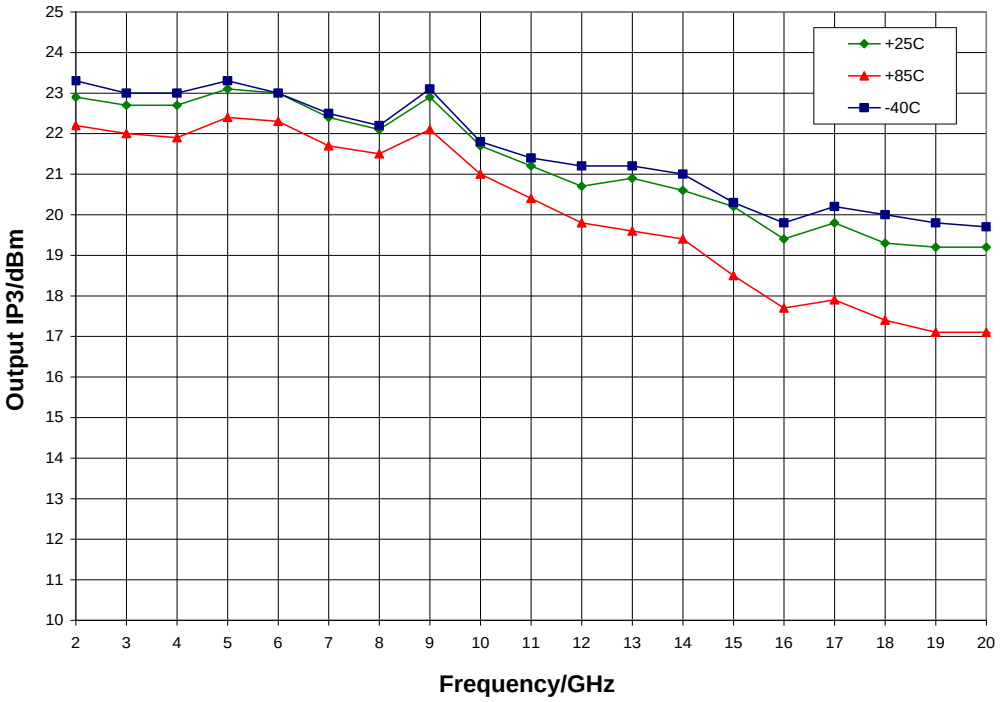


Psat vs. V_{dd}, V_{gg} = V_{dd}, T_A = 25° C

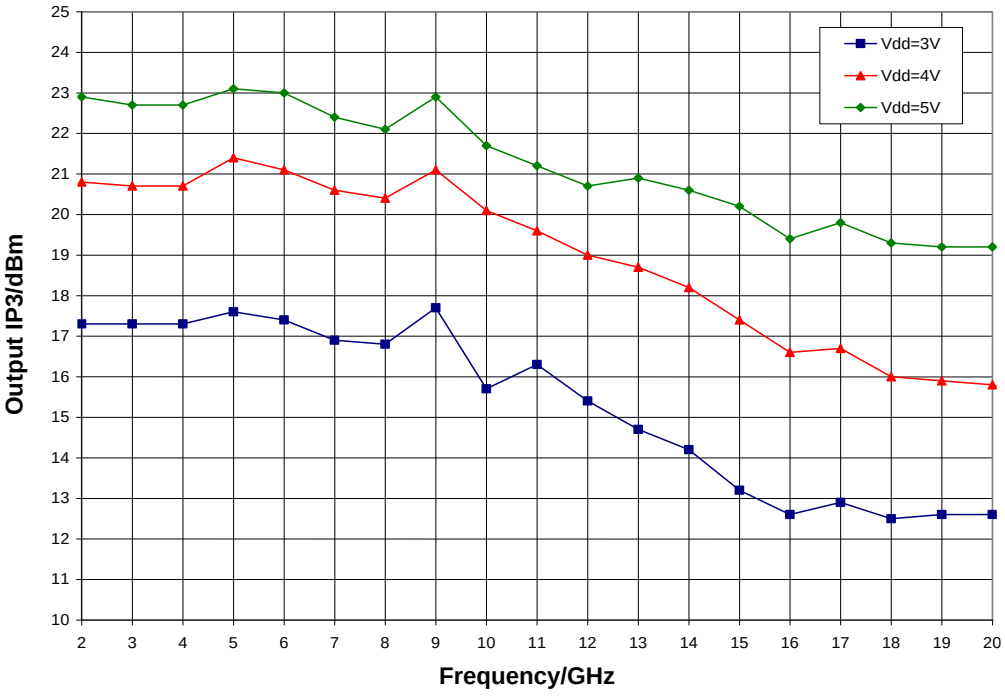


Typical Performance

Output IP3 vs. Temperature, V_{dd} = 5.0 V, V_{gg} = 5.0 V

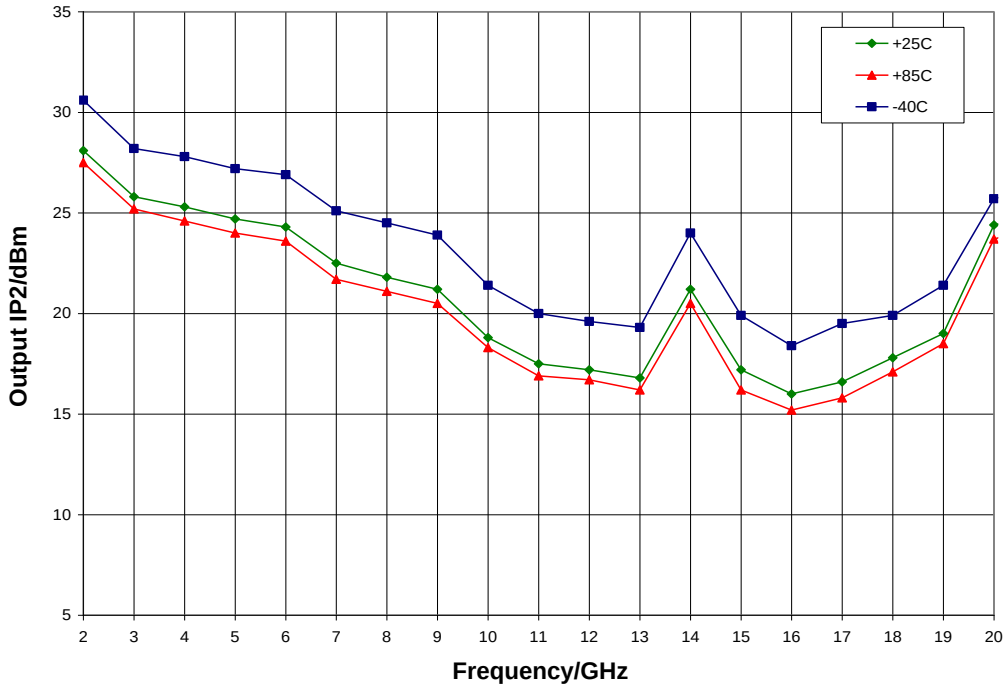


Output IP3 vs. V_{dd}, V_{gg} = V_{dd}, T_A = 25° C

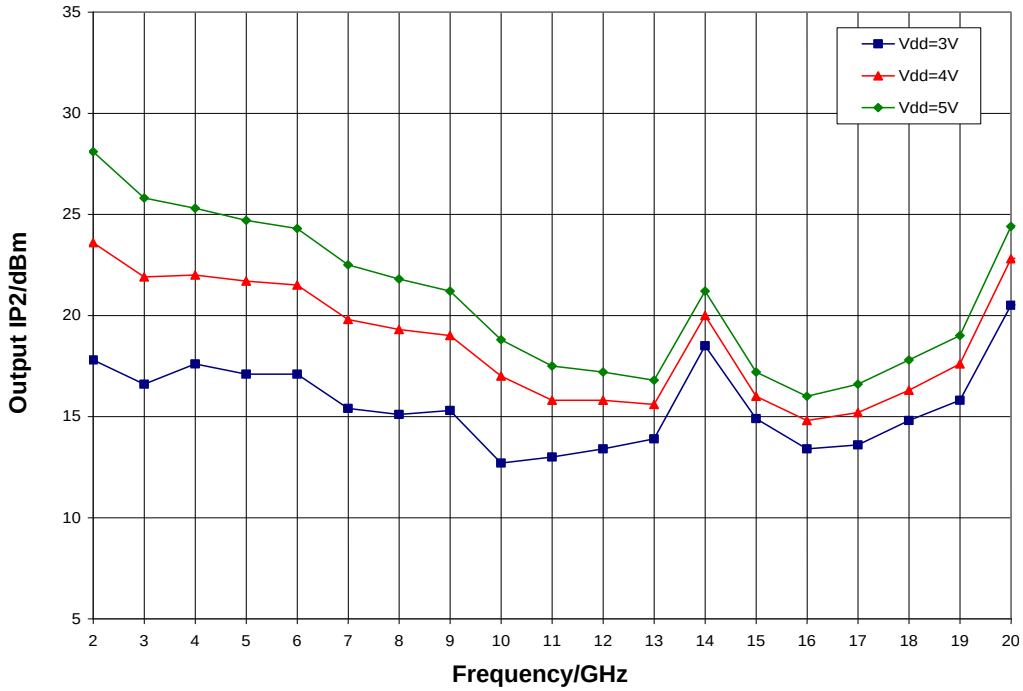


Typical Performance

Output IP2 vs. Temperature, V_{dd} = 5.0 V, V_{gg} = 5.0 V

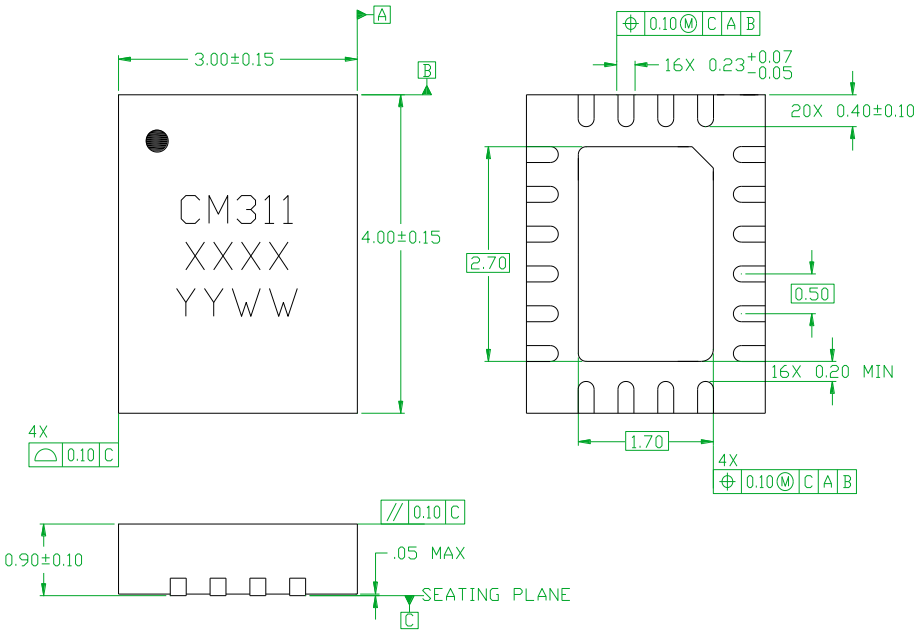


Output IP2 vs. V_{dd}, V_{gg} = V_{dd}, T_A = 25° C



Mechanical Information

Package Information and Dimensions



Notes:

1. Dimensions are in millimeters
2. RoHS compliant mold compound
3. Lead frame material: Copper alloy
4. Lead finish: 100% matte Sn
5. Indicated dimension/tolerance applies to leads and exposed pad

Recommended PCB Land Pattern

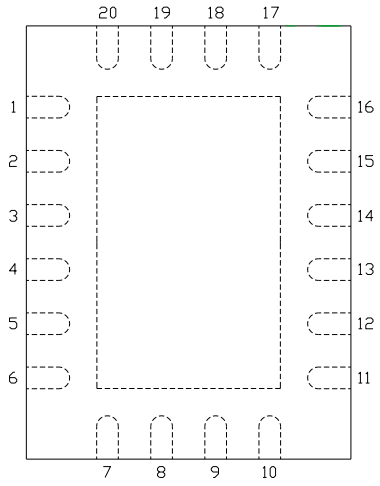
Qorvo recommends that the user develop the land pattern that will provide the best design for proper solder reflow and device attach for their specific application. Please review Qorvo Application Note AN 105 for a recommended land pattern approach.

Recommended Solder Reflow Profile

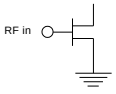
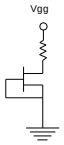
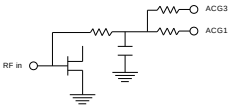
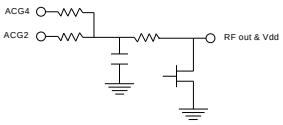
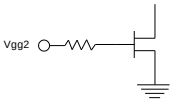
Qorvo recommends screen printing with belt furnace reflow to ensure proper solder reflow and device attach. Please review Qorvo Application Note AN 102 for a recommended solder reflow profile.

Pin Description

Pin Diagram

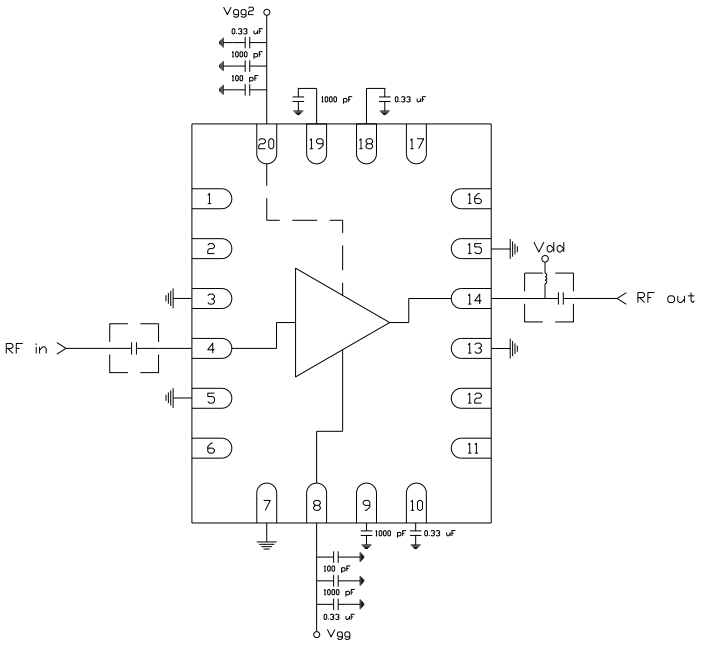


Functional Description

Pad	Function	Description	Schematic
1, 2, 6, 11, 12, 16, 17	N/C	No connection required These pins may be connected to RF / DC ground	
4	RF in	50 ohm matched input	
7	Ground	This pin must be connected to RF / DC ground for nominal operation	
8	V_{gg}	Power supply voltage Decoupling and bypass caps required	
9, 19	ACG1, 3	Low frequency termination Attach bypass capacitor per application circuit	
10, 18	ACG2, 4	Low frequency termination Attach bypass capacitor per application circuit	
14	RF out & V_{dd}	Supply voltage and 50 ohm matched output	
20	V_{gg2}	Optional supply voltage for gain control Decoupling and bypass caps required Pin must be left open if unused	
3, 5, 13, 15 and die paddle	Ground	Connect to RF / DC ground	

Applications Information

Application Circuit



Note: Drain voltage (V_{dd}) must be applied through a broadband bias tee or external bias network.
External DC block is required on RF input.

Biasing and Operation

The CMD311P34 is biased with a positive drain supply and positive gate supply. Performance is optimized when the drain voltage is set to +5.0 V. The recommended gate voltage is +5.0 V.

Turn ON procedure:

1. Apply drain voltage V_{dd} and set to +5 V
2. Apply gate voltage V_{gg} and set to +5 V

Turn OFF procedure:

1. Turn off gate voltage V_{gg}
2. Turn off drain voltage V_{dd}

RF power can be applied at any time.

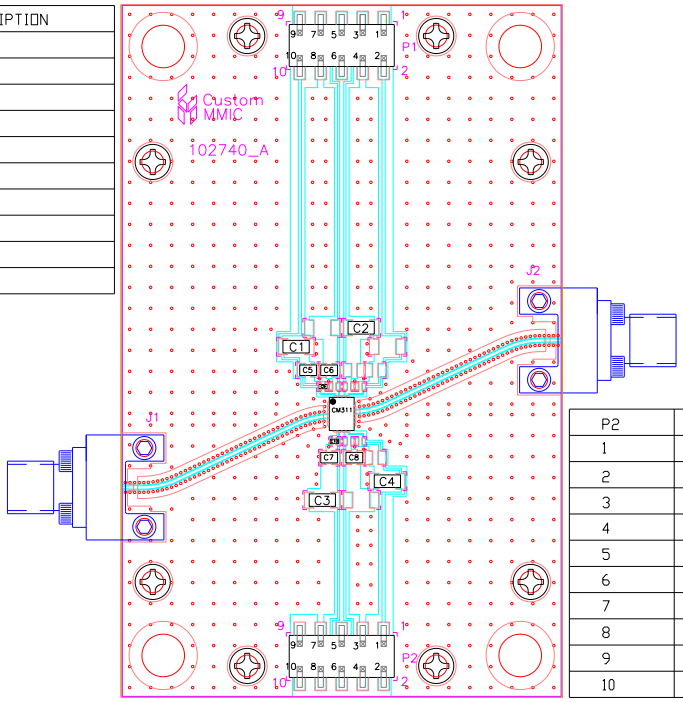
GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.

Applications Information

Evaluation Board

The circuit board shown has been developed for optimized assembly at Qorvo. A sufficient number of via holes should be used to connect the top and bottom ground planes. As surface mount processes vary, careful process development is recommended.

P1	DESCRIPTION
1	GND
2	N/C
3	ACG4
4	GND
5	N/C
6	N/C
7	ACG3
8	GND
9	GND
10	Vgg2



P2	DESCRIPTION
1	ACG2
2	GND
3	GND
4	ACG1
5	N/C
6	N/C
7	GND
8	Vgg
9	N/C
10	GND

Bill of Material

Designator	Value	Description
J1, J2		SMA End Launch Connector
P1, P2		10 Pin DC Header
C1 - C4	0.33 µF	Capacitor, Tantalum
C5 - C8	1000 pF	Capacitor, 0603
C9, C10	100 pF	Capacitor, 0402
U1		CMD311P34 Driver Amplifier
PCB		102740 Evaluation PCB