CMPA801B030D1

8 – 11 GHz, 40 W GaN HPA

Description

Wolfspeed's CMPA801B030D1 is a 40W MMIC HPA utilizing Wolfspeed's high performance, 0.15um GaN on SiC production process. The CMPA801B030D1 operates from 8-11 GHz and supports both defense and commercial-related radar applications. The CMPA801B030D1 achieves 40 W of saturated output power with 20 dB of large signal gain and typically 40% power-added efficiency under pulsed operation. CW operation is also an option.

The CMPA801B030D1 provides improved RF performance over previous generations allowing customers to improve SWaP-C benchmarks in their next-generation systems.

Figure 1. CMPA801B030D1

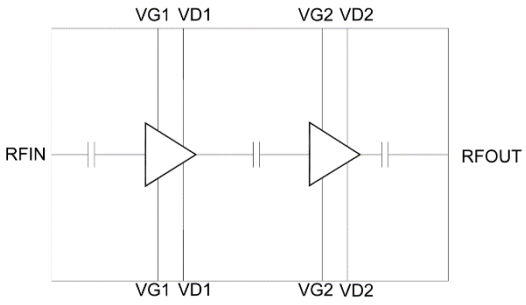


Figure 2. Functional Block Diagram

Features

- Psat: 40 W
- PAE: 40 %
- LSG: 20 dB
- S21: 27 dB
- S11: -10 dB
- S22: -6 dB
- Pulsed / CW operation

Note: Features are typical performance across frequency under 25C operation. Please reference performance charts for additional information.

Applications

- Military and Commercial Radar

RoHS COMPLIANT

4600 Silicon Drive | Durham, NC 27703 | Wolfspeed.com

Absolute Maximum Ratings

Parameter	Symbol	Units	Value	Conditions
Drain Voltage	V_d	V	28	
Gate Voltage	V_g	V	-10, +2	
Drain Current	I_d	A	4	
Gate Current	I_g	mA	12.9	
Input Power	P_{in}	dBm	29	
Dissipated Power	P_{diss}	W	98	85 °C
Storage Temperature	T_{stg}	°C	-55, +150	
Mounting Temperature	T_J	°C	260	30 seconds
Junction Temperature	T_J	°C	225	MTTF > 1E6
Output Mismatch Stress	VSWR	Ψ	5:1	

Recommended Operating Conditions

Parameter	Symbol	Units	Typical Value	Conditions
Drain Voltage	Vd	V	28	
Gate Voltage	Vg	V	-1.8	
Drain Current	Idq	mA	800	
Input Power	Pin	dBm	26	
Case Temperature	Tcase	°C	-40 to 85	

RF Specifications

Test conditions unless otherwise noted: Vd=28V, Idq= 800mA, PW=100uS, DC=10%, T_{base}=25 °C

Parameter	Units	Frequency	Min	Typical	Max	Conditions
Frequency	GHz		8		11	
Output Power	dBm	8		45.5		Pin = 26 dBm
		10		46.5		
		11		46.5		
Power-added Efficiency	%	8		40		Pin = 26 dBm
		10		39		
		11		36		
LSG	dB	8		19.5		Pin = 26 dBm
		10		20.5		
		11		20.5		
Small-Signal Gain (S21)	dB	8		28.5		
		10		26		
		11		25		
Input Return Loss	dB			-10		
Output Return Loss	dB			-6		

Test conditions unless otherwise noted: Vd=28V, Idq= 800mA, PW=100uS, DC=10%, Pin = 26dBm, T_{base}=25 °C, Frequency =9.5 GHz

Figure 3: Pout v. Frequency v. Temperature

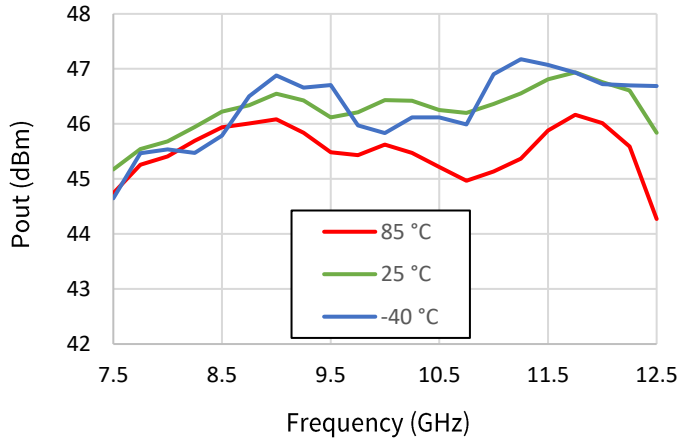


Figure 4: PAE v. Frequency v. Temperature

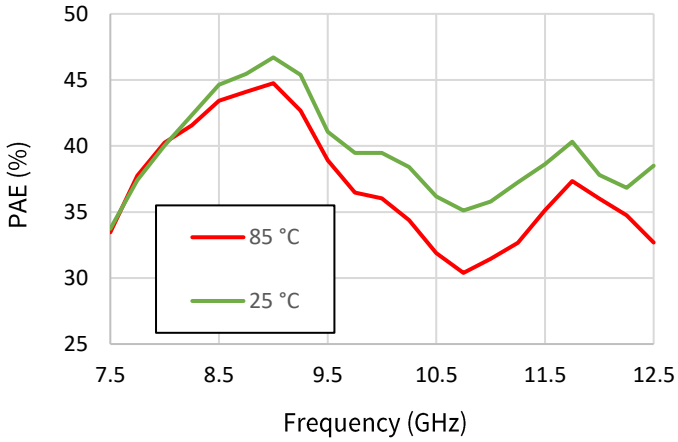


Figure 5: Id v. Frequency v. Temperature

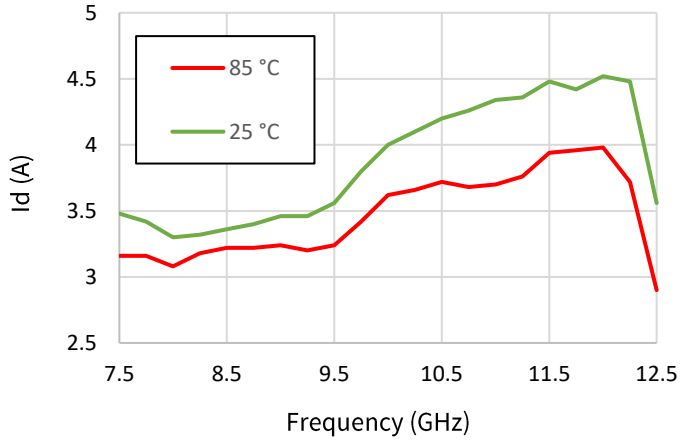


Figure 6: Ig v. Frequency v. Temperature

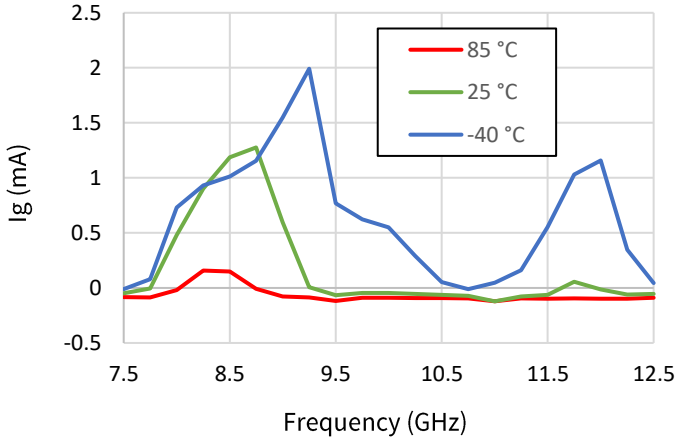
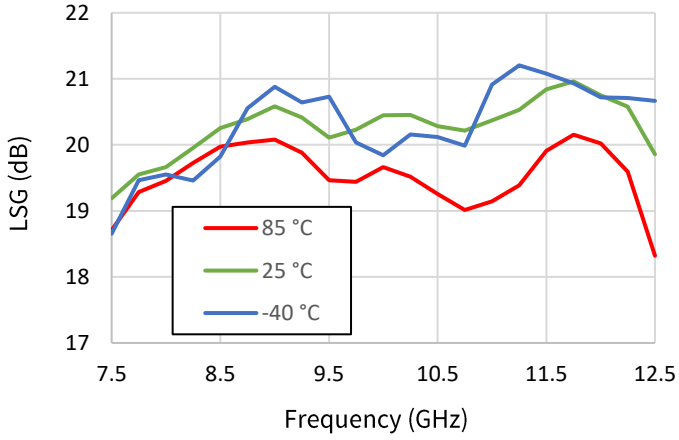


Figure 7: LSG v. Frequency v. Temperature



Test conditions unless otherwise noted: Vd=28V, Idq= 800mA, PW=100uS, DC=10%, Pin = 26dBm, T_{base}=25 °C, Frequency =9.5 GHz

Figure 8: Pout v. Frequency v. Vd

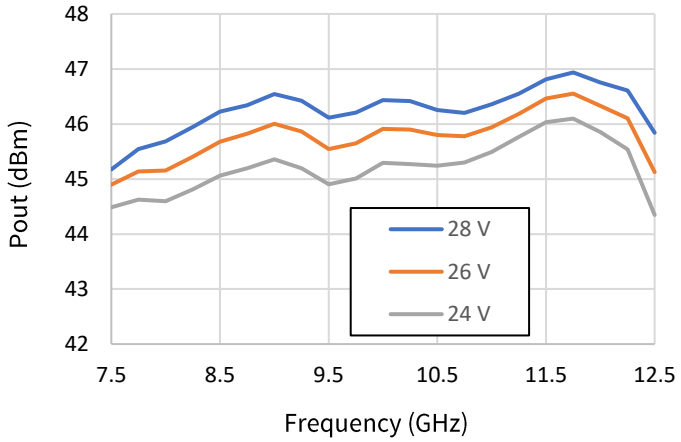


Figure 9: PAE v. Frequency v. Vd

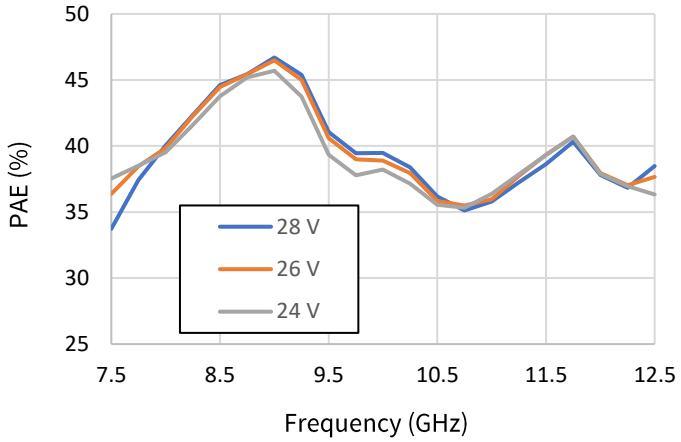


Figure 10: Id v. Frequency v. Vd

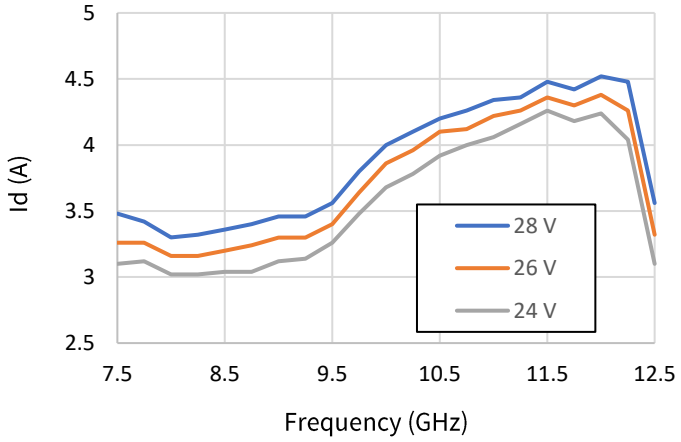


Figure 11: Ig v. Frequency v. Vd

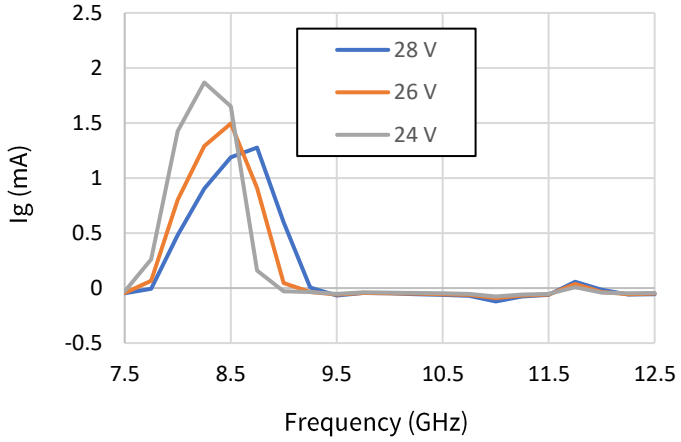
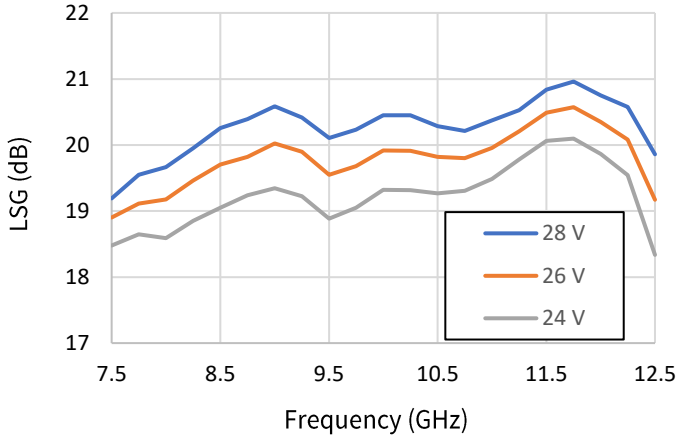


Figure 12: LSG v. Frequency v. Vd



Test conditions unless otherwise noted: Vd=28V, Idq= 800mA, PW=100uS, DC=10%, Pin = 26dBm, T_{base}=25 °C, Frequency =9.5 GHz

Figure 13: Pout v. Frequency v. Idq

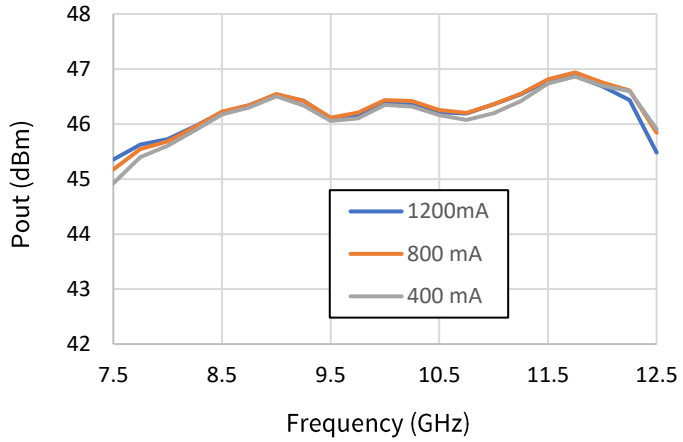


Figure 14: PAE v. Frequency v. Idq

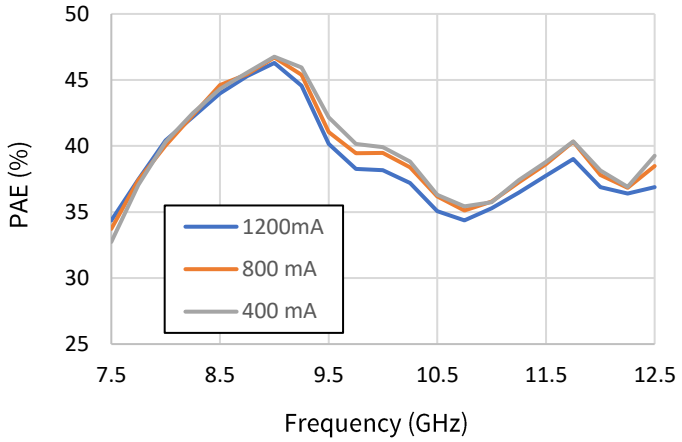


Figure 15: Id v. Frequency v. Idq

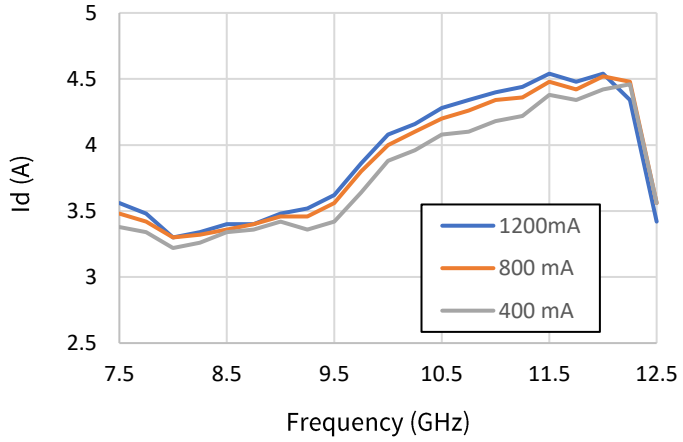


Figure 16: Ig v. Frequency v. Idq

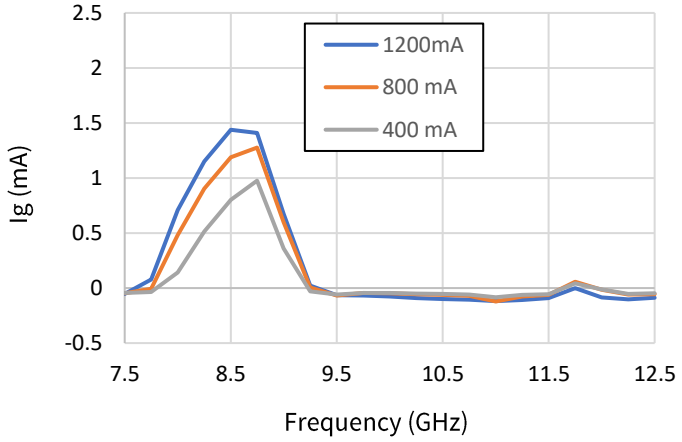
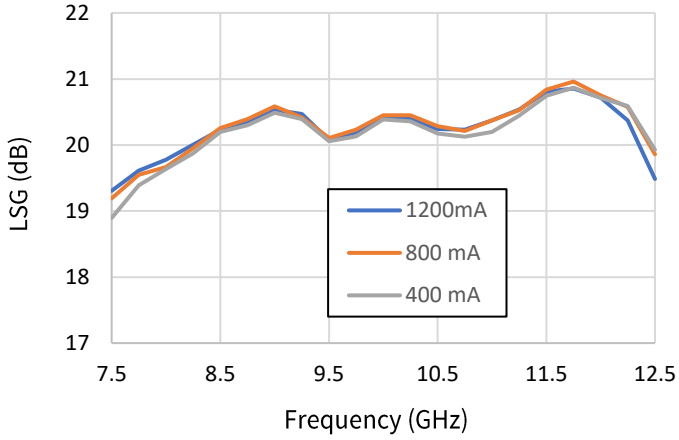


Figure 17: LSG v. Frequency v. Idq



Test conditions unless otherwise noted: Vd=28V, Idq= 800mA, PW=100uS, DC=10%, Pin = 26dBm, T_{base}=25 °C, Frequency =9.5 GHz

Figure 18: Pout v. Pin v. Frequency

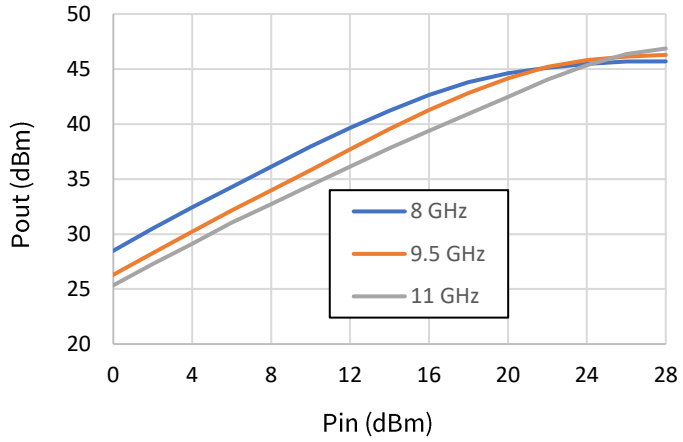


Figure 19: PAE v. Pin v. Frequency

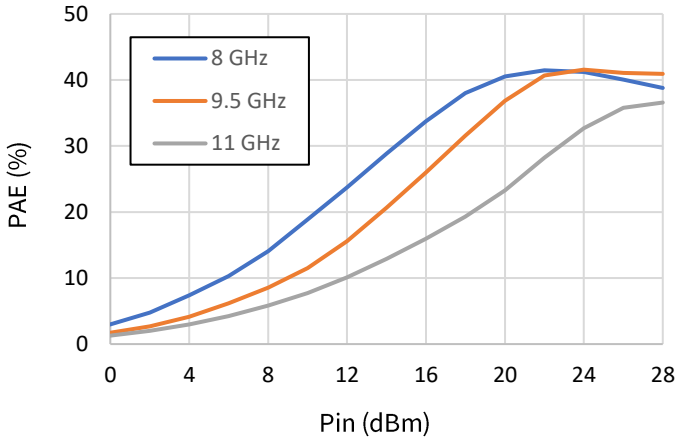


Figure 20: Id v. Pin v. Frequency

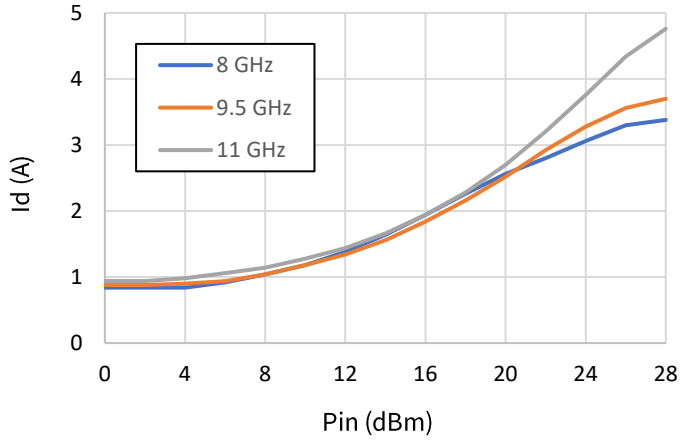


Figure 21: Ig v. Pin v. Frequency

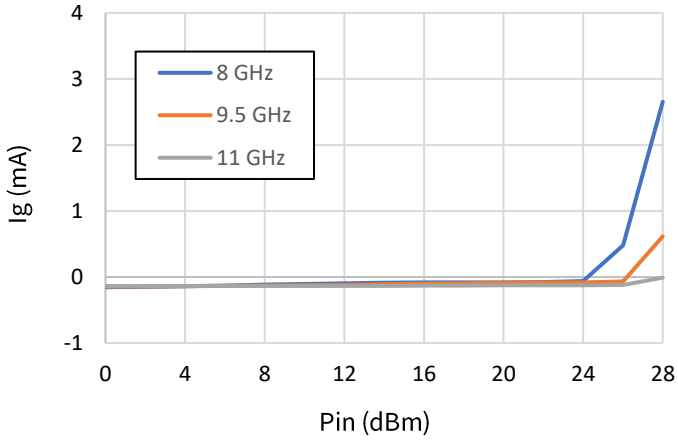
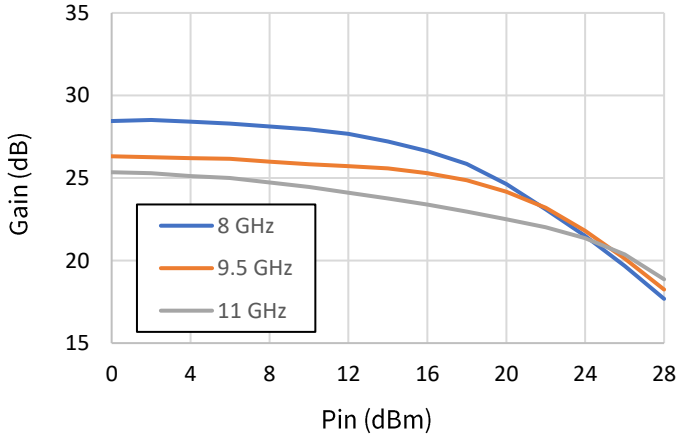


Figure 22: Gain v. Pin v. Frequency



Test conditions unless otherwise noted: Vd=28V, Idq= 800mA, PW=100uS, DC=10%, Pin = 26dBm, T_{base}=25 °C, Frequency =9.5 GHz

Figure 23: Pout v. Pin v. Temperature

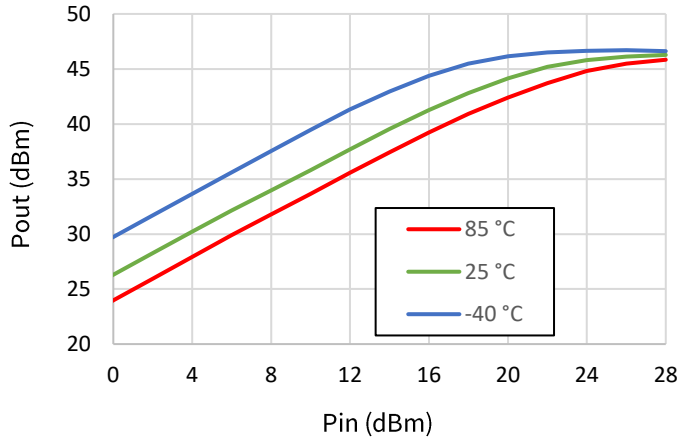


Figure 24: PAE v. Pin v. Temperature

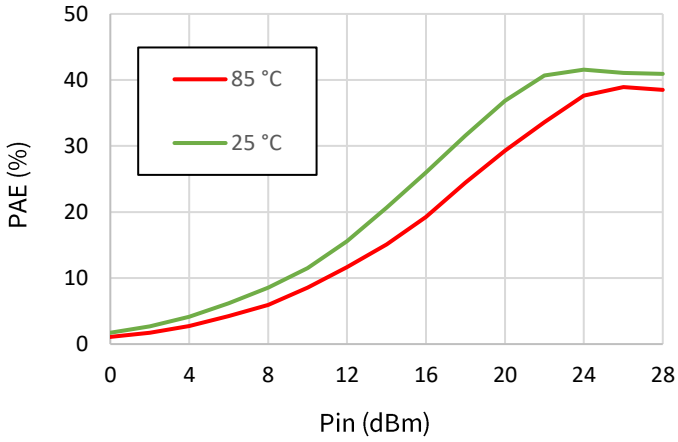


Figure 25: Id v. Pin v. Temperature

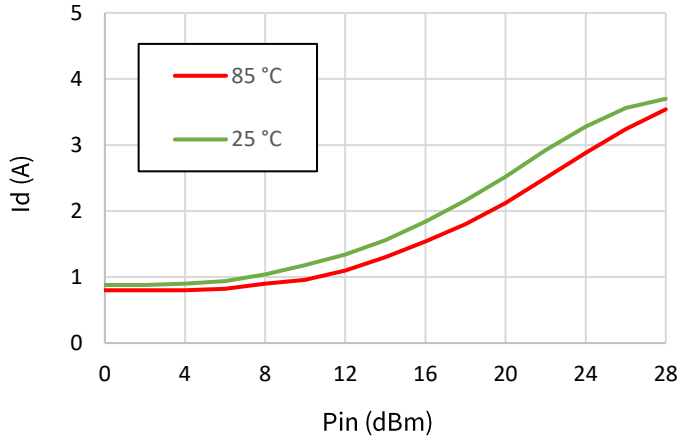


Figure 26: Ig v. Pin v. Temperature

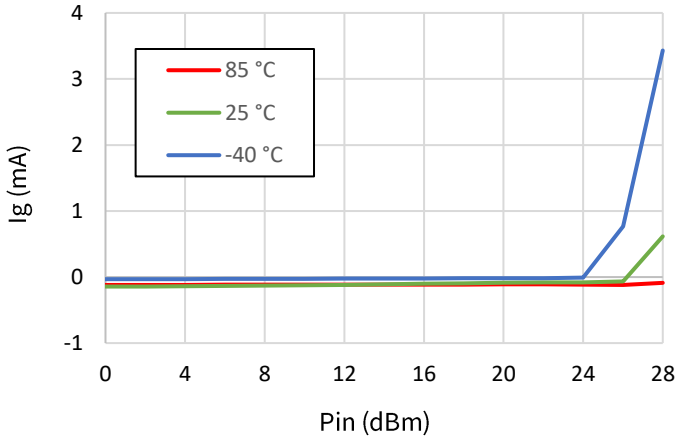
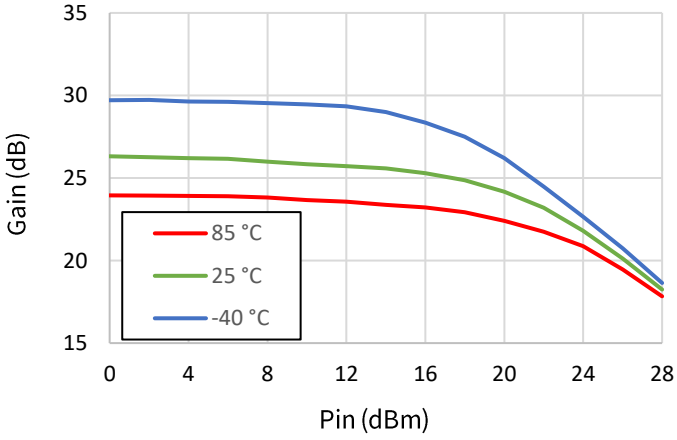


Figure 27: Gain v. Pin v. Temperature



Test conditions unless otherwise noted: Vd=28V, Idq= 800mA, PW=100uS, DC=10%, Pin = 26dBm, T_{base}=25 °C, Frequency =9.5 GHz

Figure 28: Pout v. Pin v. Vd

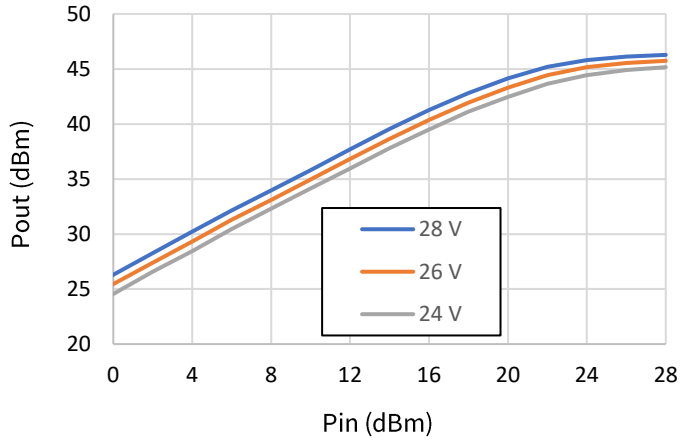


Figure 29: PAE v. Pin v. Vd

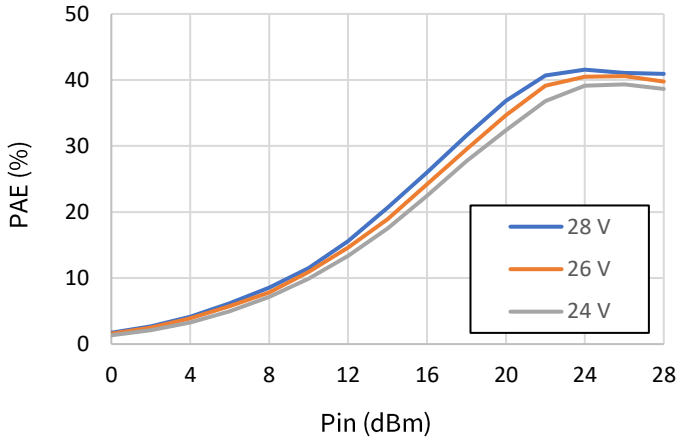


Figure 30: Id v. Pin v. Vd

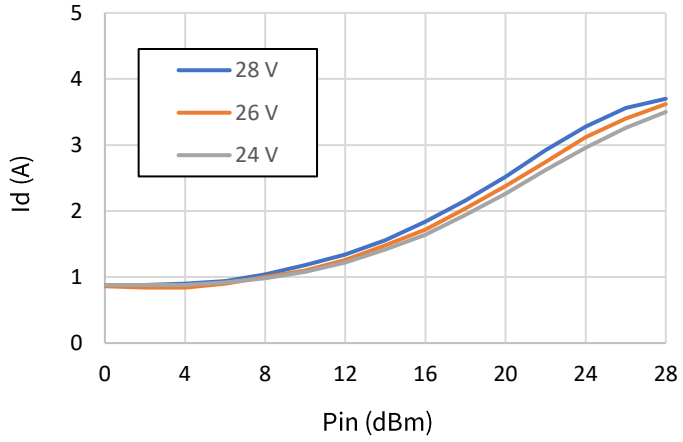


Figure 31: Ig v. Pin v. Vd

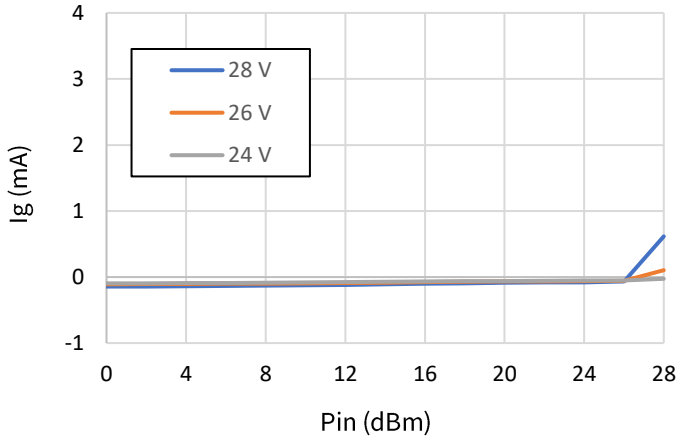
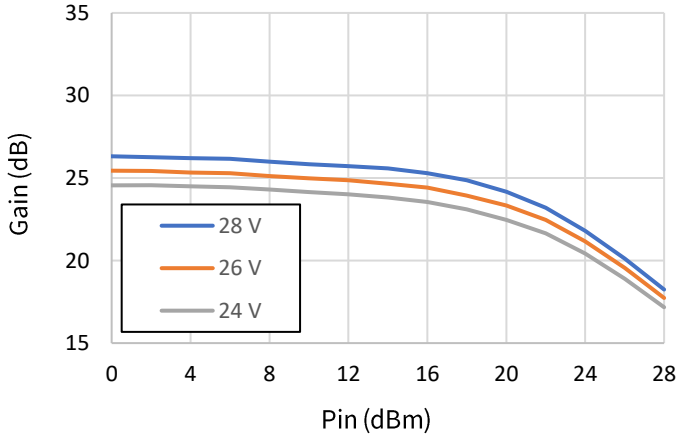


Figure 32: Gain v. Pin v. Vd



Test conditions unless otherwise noted: Vd=28V, Idq= 800mA, PW=100uS, DC=10%, Pin = 26dBm, T_{base}=25 °C, Frequency =9.5 GHz

Figure 33: Pout v. Pin v. Idq

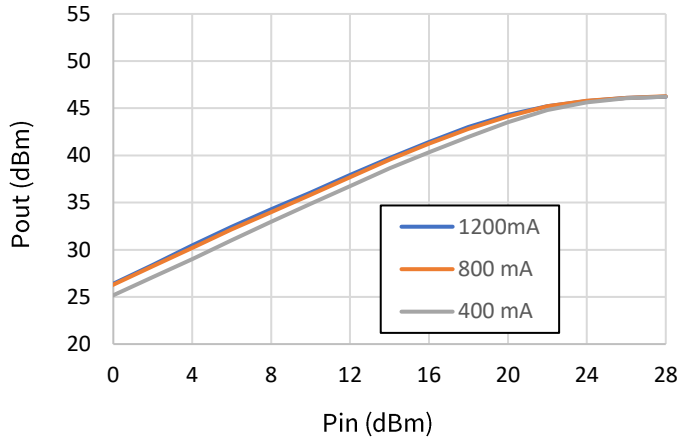


Figure 34: PAE v. Pin v. Idq

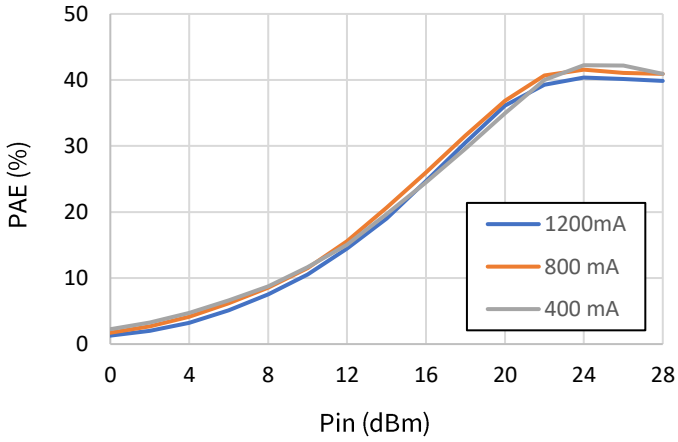


Figure 35: Id v. Pin v. Idq

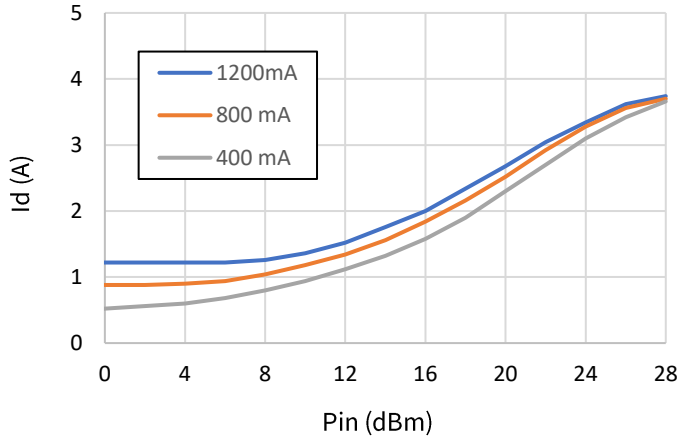


Figure 36: Ig v. Pin v. Idq

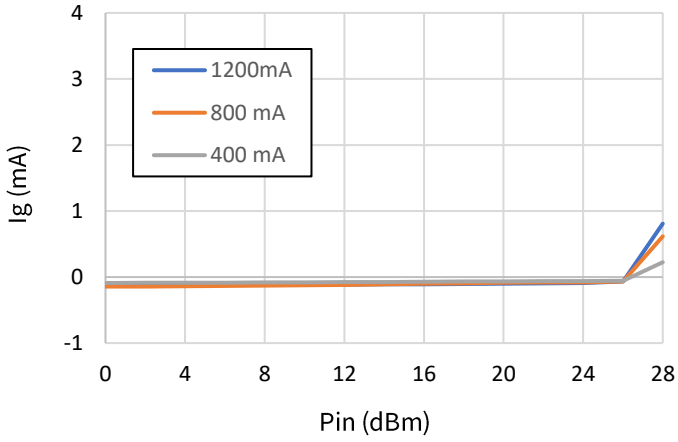
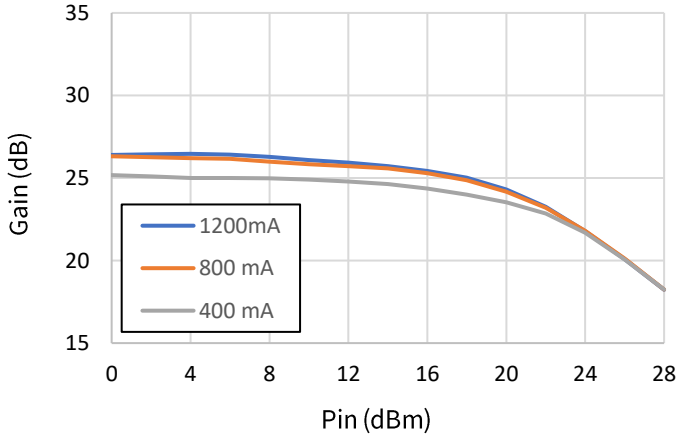


Figure 37: Gain v. Pin v. Idq



Test conditions unless otherwise noted: Vd=28V, Idq= 800mA, Pin = -20Bm, T_{base}=25°C

Figure 38: S21 v. Frequency v. Temperature

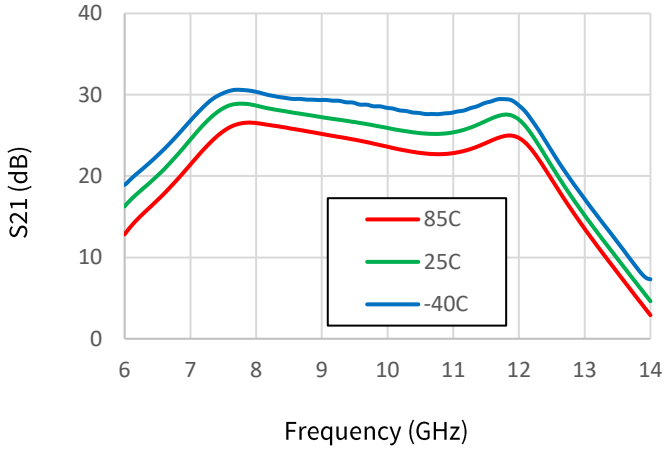


Figure 39: S21 v. Frequency v. Vd

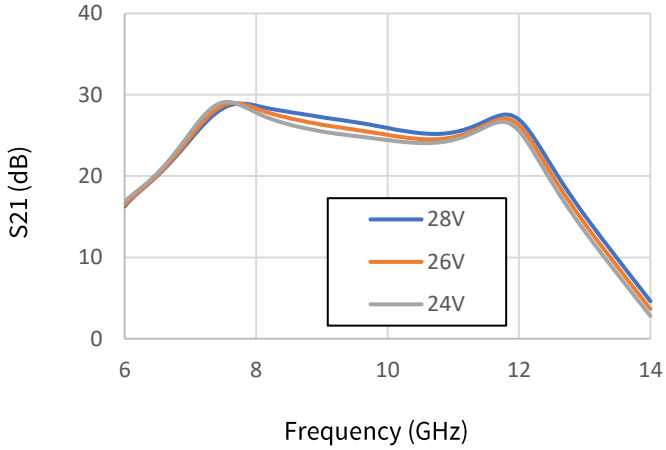


Figure 40: S11 v. Frequency v. Temperature

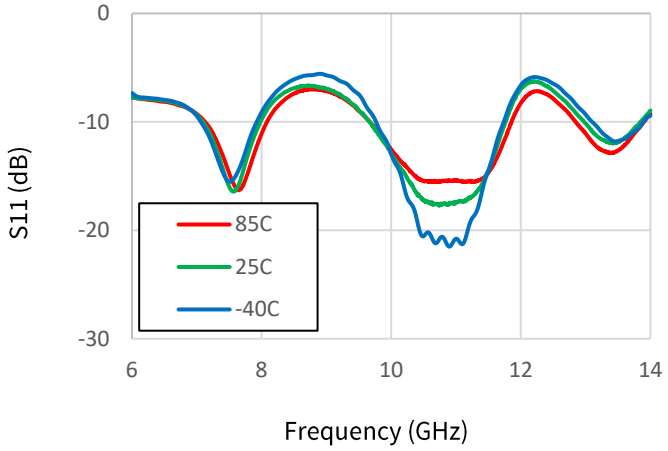


Figure 41: S11 v. Frequency v. Vd

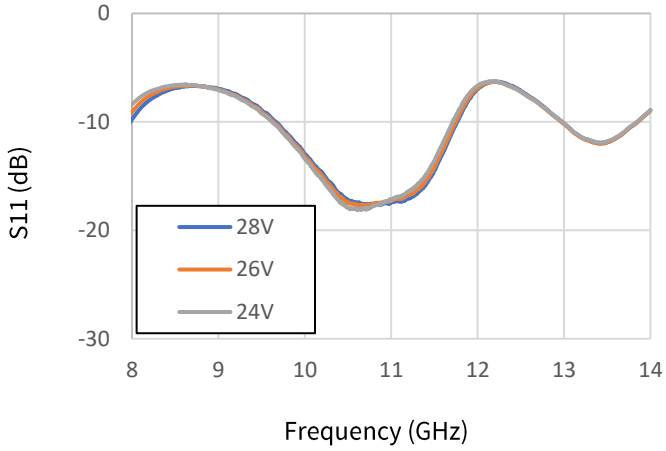


Figure 42: S22 v. Frequency v. Temperature

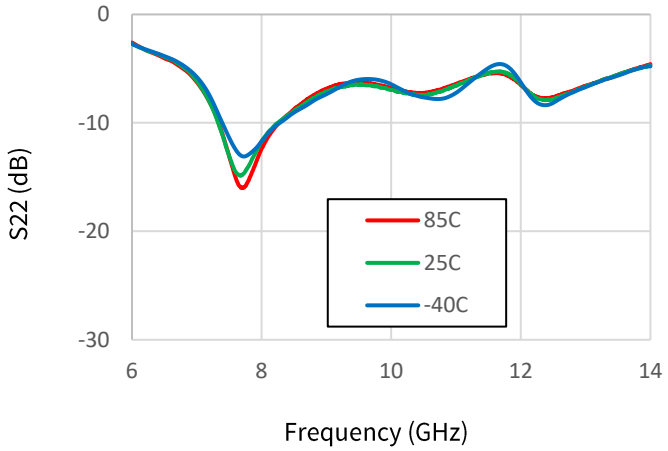
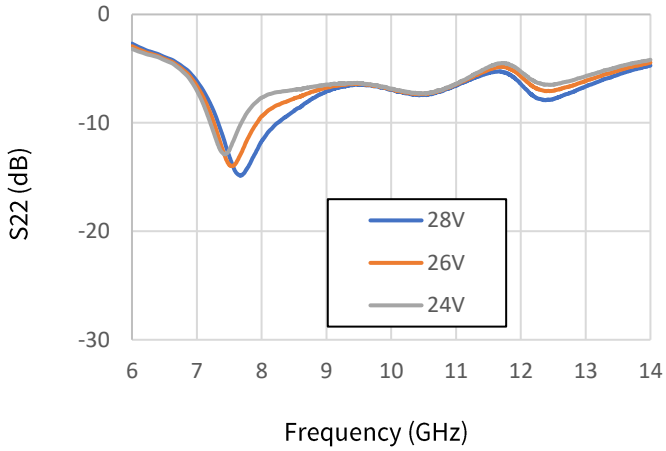


Figure 43: S22 v. Frequency v. Vd



Test conditions unless otherwise noted: Vd=28V, Idq= 800mA, Pin = -20Bm, T_{base}=25°C

Figure 44: S21 v. Frequency v. Idq

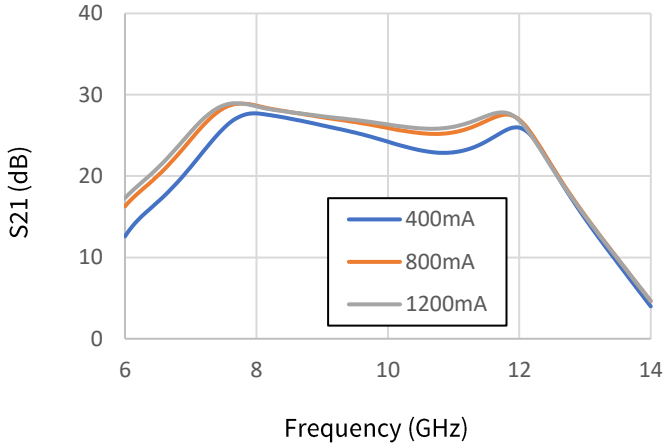


Figure 45: S11 v. Frequency v. Idq

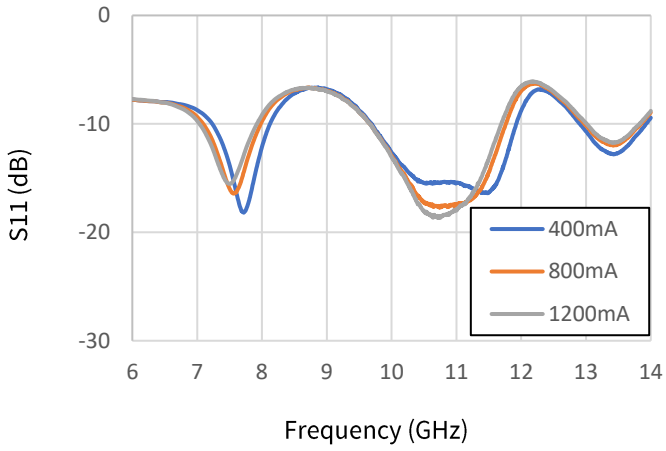
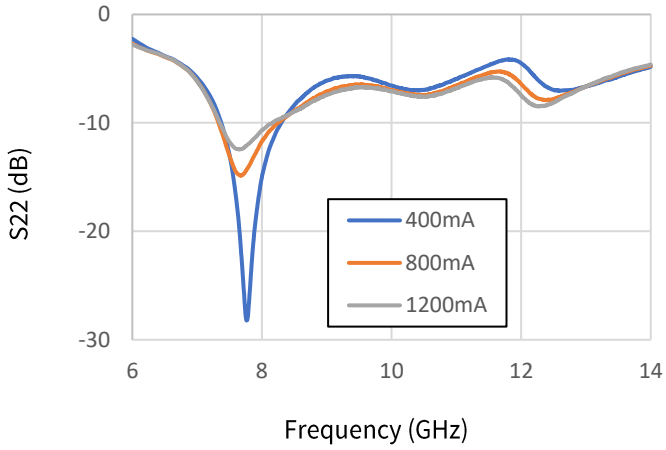


Figure 46: S22 v. Frequency v. Idq



Test conditions unless otherwise noted: Vd=28V, Idq= 800mA, PW= 100uS, DC=10%, Pin = 26dBm, T_{base}=25°C

Figure 53: 2f v. Pout v. Temperature, 8 GHz

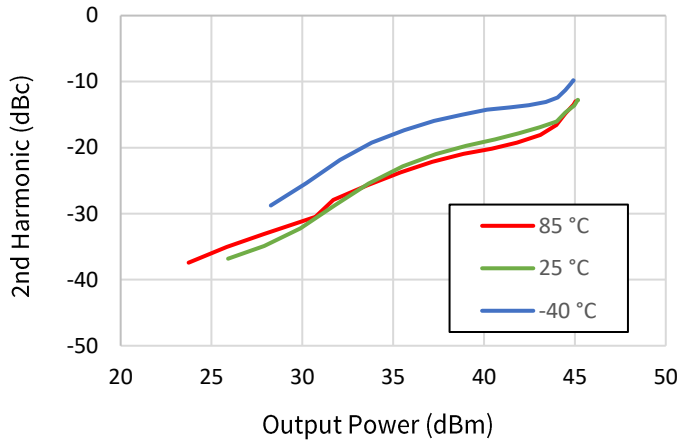


Figure 54: 2f v. Pout v. Vd, 8 GHz

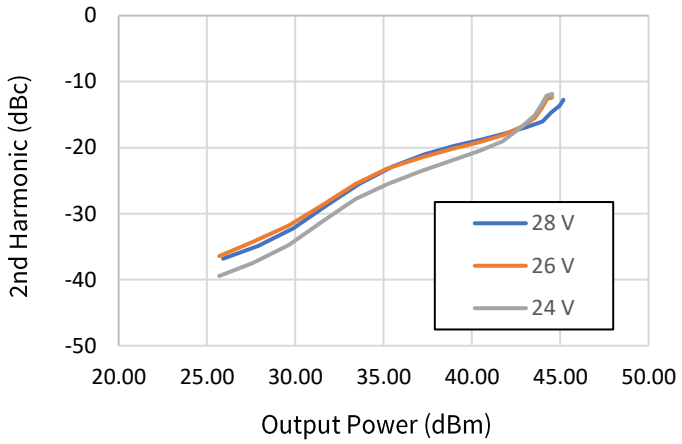


Figure 55: 2f v. Pout v. Temperature, 9.5 GHz

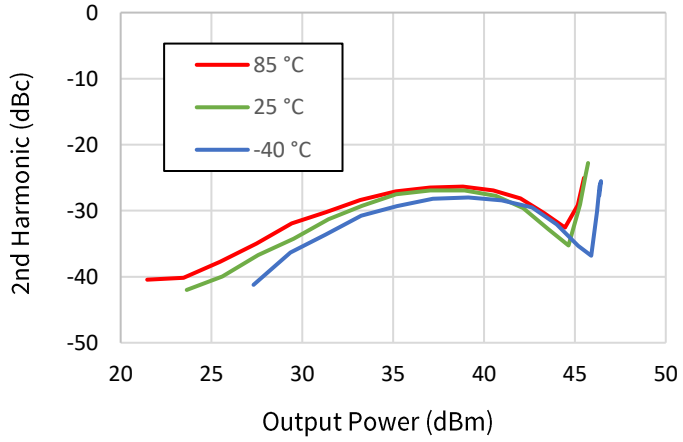


Figure 56: 2f v. Pout v. Vd, 9.5 GHz

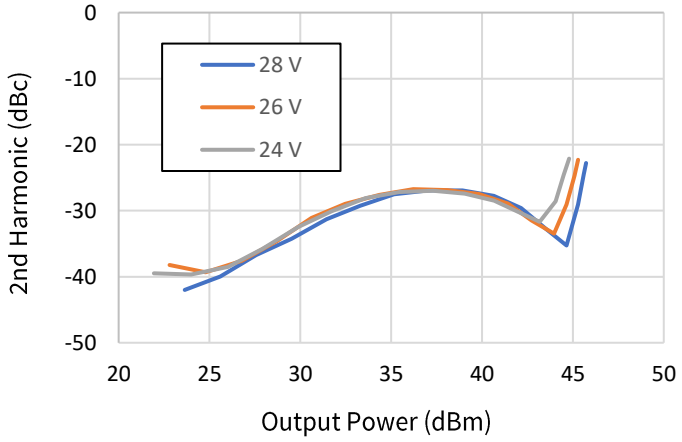


Figure 57: 2f v. Pout v. Temperature, 11 GHz

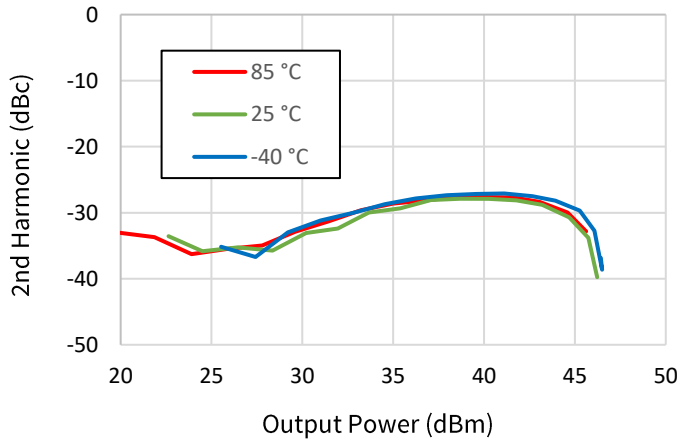
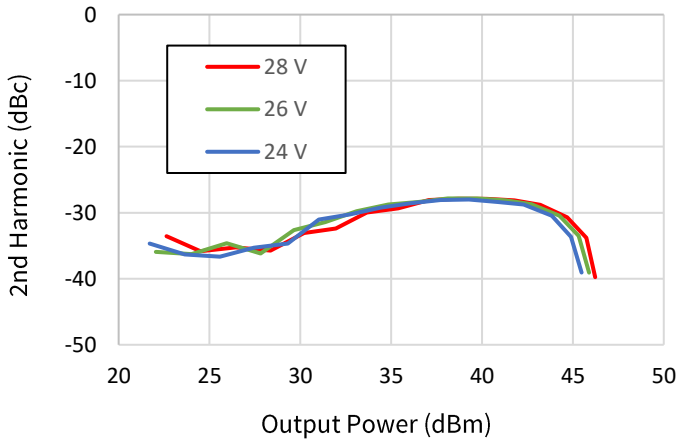


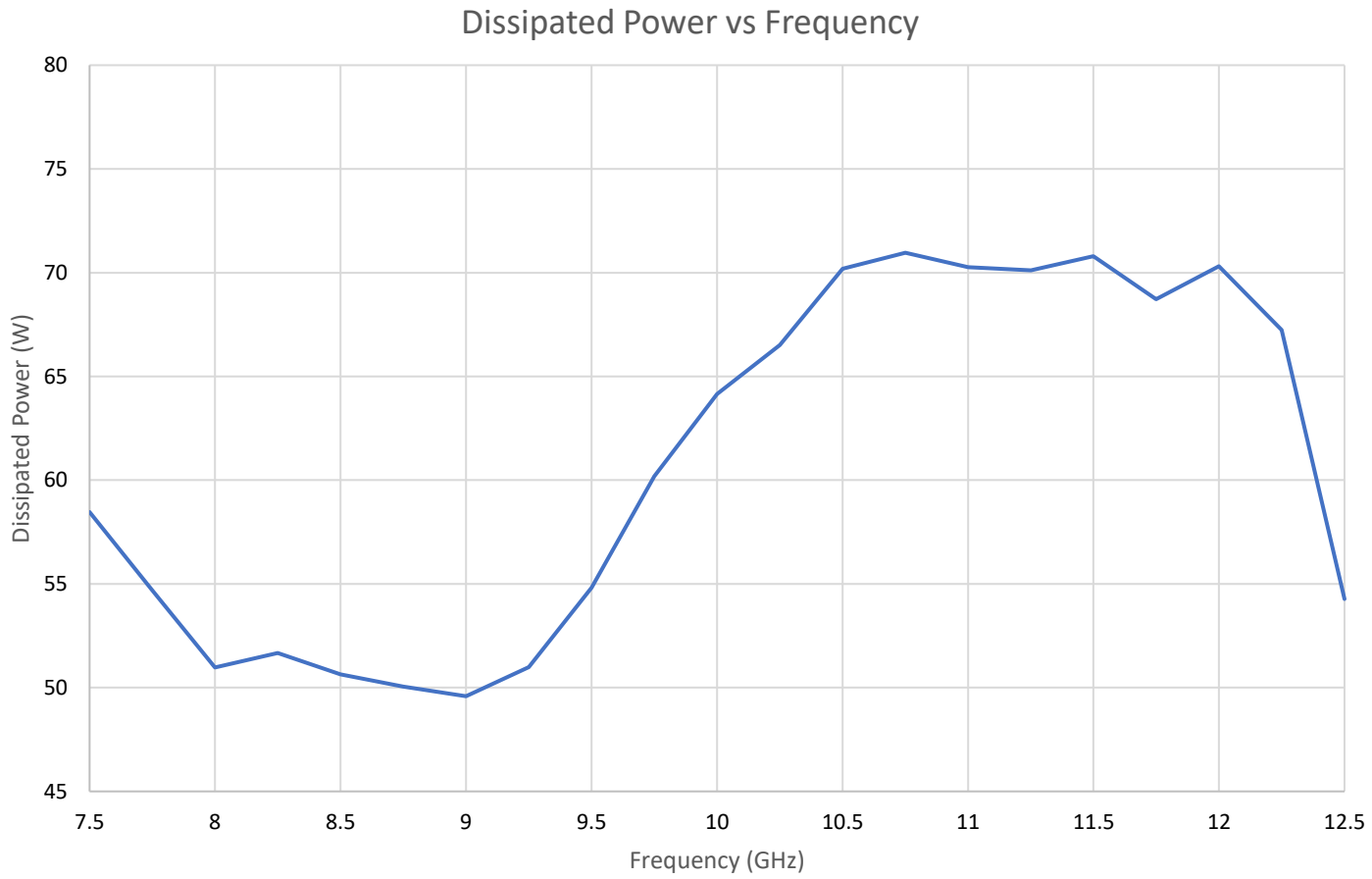
Figure 58: 2f v. Pout v. Vd, 11 GHz



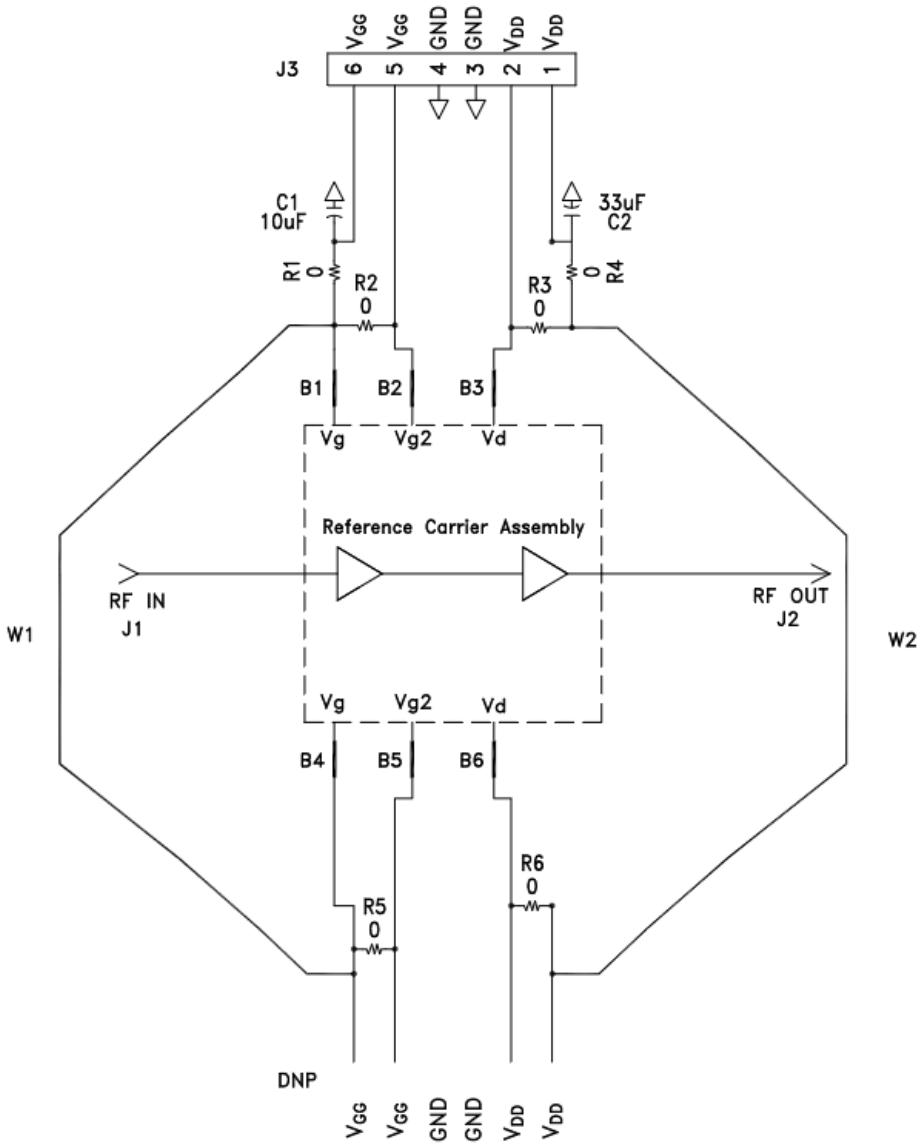
Thermal Characteristics

Parameter	Symbol	Value	Operating Conditions
Operating Junction Temperature	T_J	186 °C	Pulse Width = 100uS, Duty Cycle = 10%, P_{Diss} = 71W, T_{base}=85 °C
Thermal Resistance, Junction to Back of Die	$R_{\theta JC}$	1.42 °C/W	

Power Dissipation v. Frequency (Tcase = 85C)



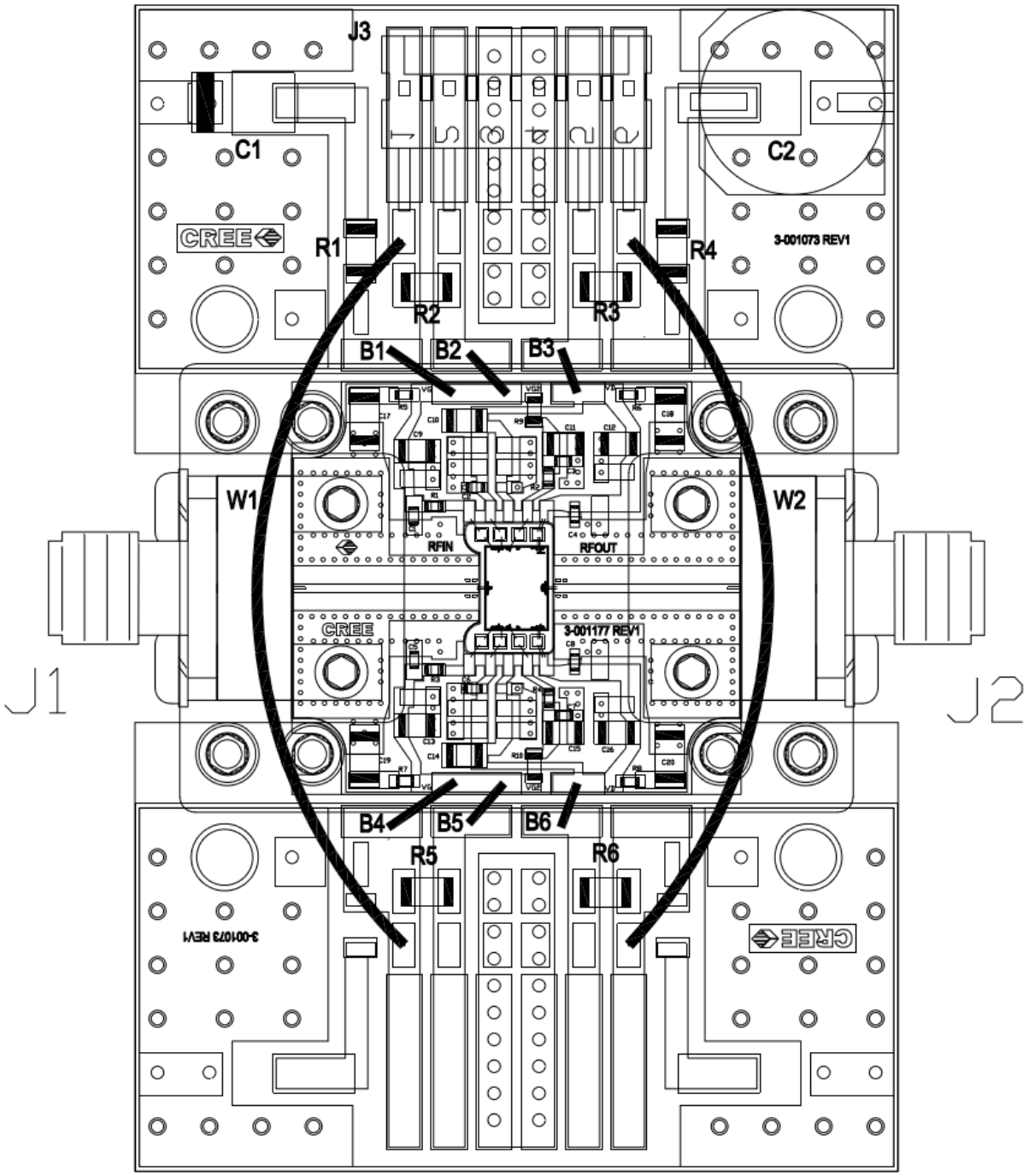
CMPA801B030D1-AMP Evaluation Board Schematic Drawing



CMPA801B030D1-AMP Evaluation Board Bill of Materials

Reference Designator	Description	Qty
J1, J2	CONNECTOR SMA JACK (FEMALE) END LAUNCH	2
J3	6-PIN DC HEADER, RIGHT ANGLE	1
R1-R6	RESISTOR, 0 OHMS, 1206	6
C1	CAPACITOR, 10UF, TANTALUM	1
C2	CAPACITOR, 33UF, ELECTROLYTIC	1
B1-B6	JUMPER WIRE	6
W1-W2	WIRE, BLACK, 22AWG (~2”)	2

CMPA801B030D1-AMP Evaluation Board Assembly Drawing



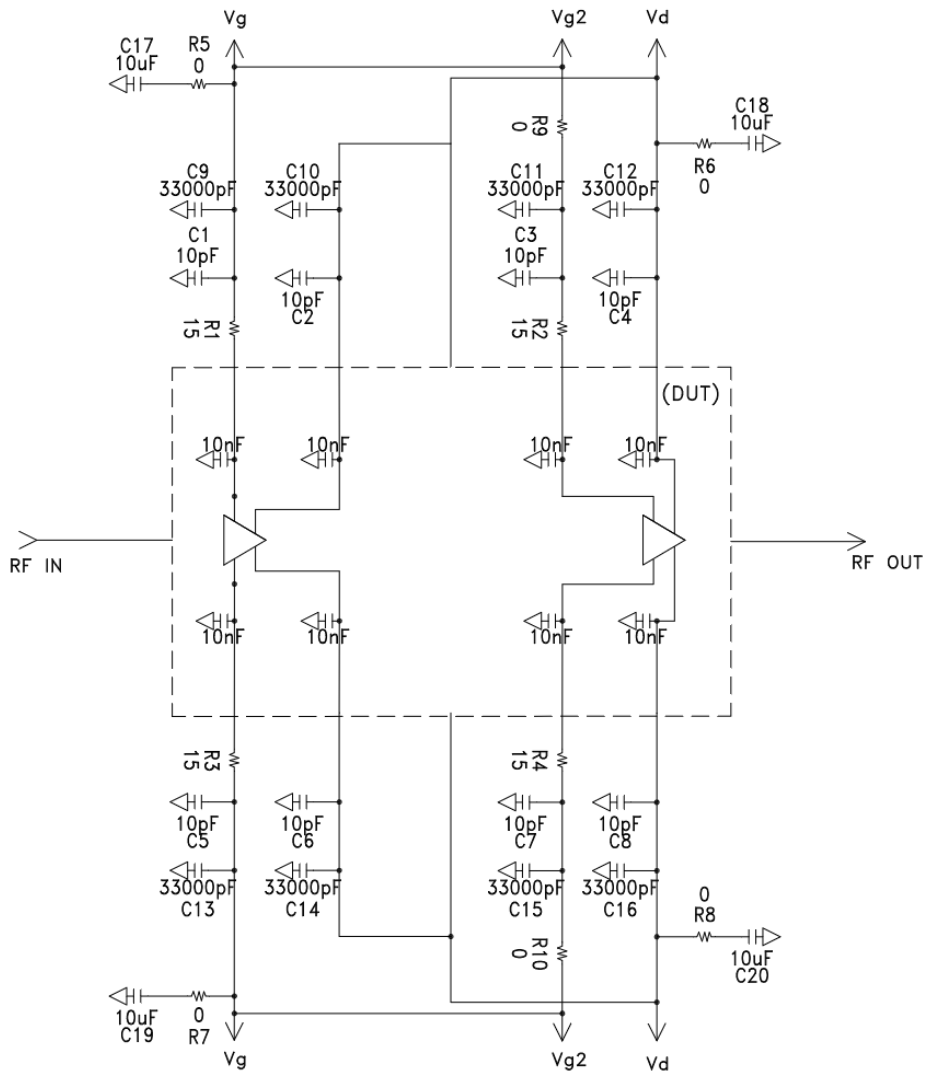
Bias On Sequence

1. Ensure RF is turned-off
2. Apply pinch-off voltage of -5 V to the gate (Vg)
3. Apply nominal drain voltage (Vd)
4. Adjust Vg to obtain desired quiescent drain current (Idq)
5. Apply RF

Bias Off Sequence

1. Turn RF off
2. Apply pinch-off to the gate (Vg=-5V)
3. Turn off drain voltage (Vd)
4. Turn off gate voltage (Vg)

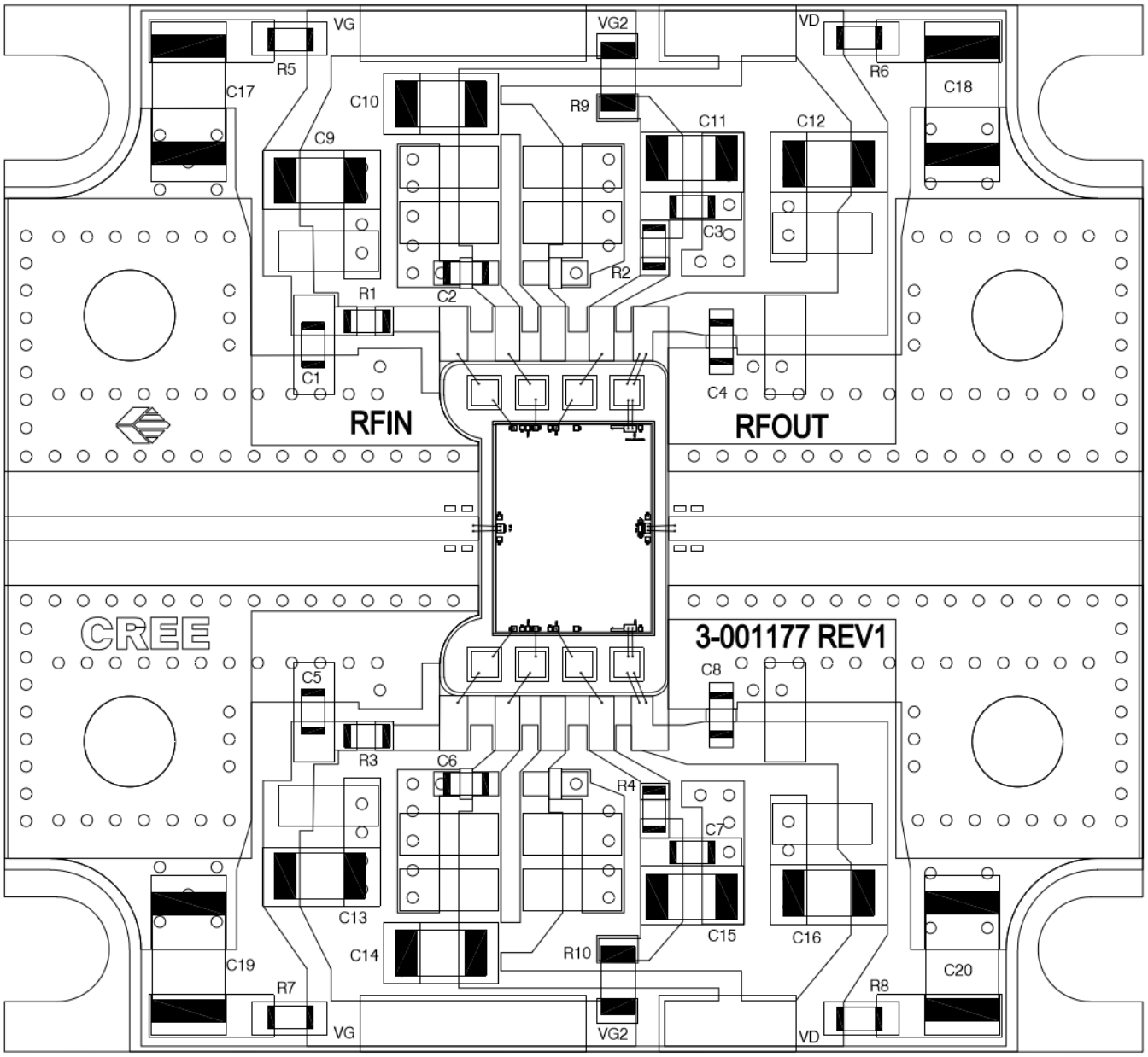
CMPA801B030D1-AMP Carrier Schematic Drawing



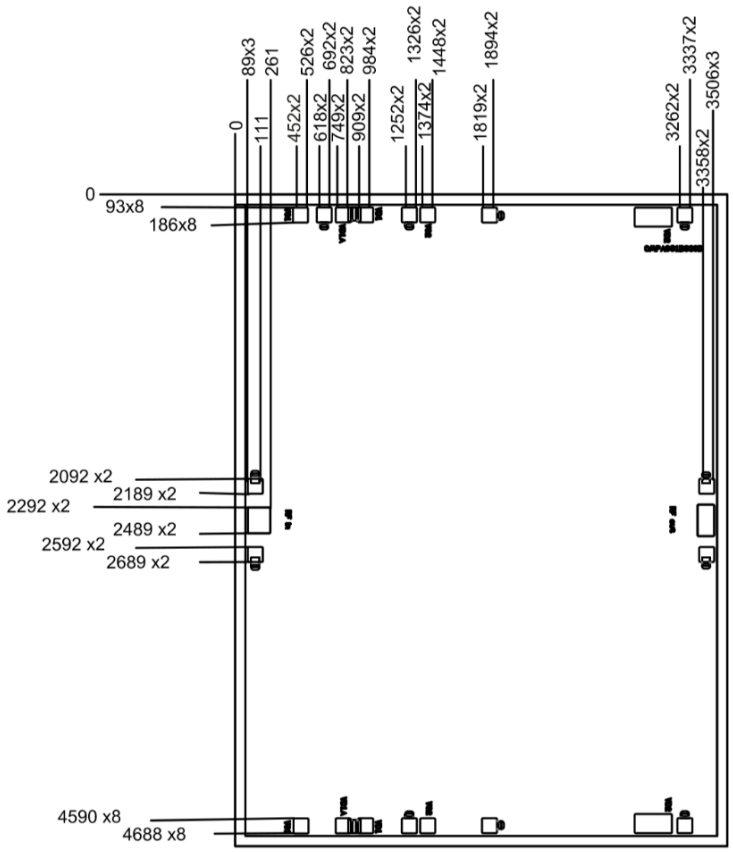
CMPA801B030D1-AMP Carrier Bill of Materials

Reference Designator	Description	Qty
R1 – R4	RESISTOR, 0402, 15 Ohms	4
R5 – R8	RESISTOR, 0402, 0 Ohms	4
R9, R10	RESISTOR, 0603, 0 Ohms	2
C1 – C8	CAPACITOR, 10 pF, 5%, 0402, ATC	8
C9 – C16	CAPACITOR, 33000 pF, 0805, X7R	8
C17 – C20	CAPACITOR, 10 uF, 1206	4

CMPA801B030D1-AMP Carrier Assembly Drawing



Product Dimensions



Overall die size 4780 x 3610 (+0/-50) microns, die thickness 100 (+/-10) micron.
All Gate and Drain pads must be wire bonded for electrical connection.

Pad	Function	Description	Pad Size (microns)	Note
1	RF-IN	RF-Input pad. Matched to 50 ohm.	190 x 165	4
2	VG1_A	Gate control for stage 1. V_G ~ 2.0 - 3.5 V.	110 x 110	1,2
3	VG1_B	Gate control for stage 1. V_G ~ 2.0 - 3.5 V.	110 x 110	1,2
4	VD1_A	Drain supply for stage 1. V_D = 28 V.	110 x 110	1
5	VD1_B	Drain supply for stage 1. V_D = 28 V.	110 x 110	1
6	VG2_A	Gate control for stage 2A. V_G ~ 2.0 - 3.5 V.	110 x 110	1,3
7	VG2_B	Gate control for stage 2A. V_G ~ 2.0 - 3.5 V.	110 x 110	1,3
8	VD2_A	Drain supply for stage 2A. V_D = 28 V.	274 x 140	1
9	VD2_B	Drain supply for stage 2B. V_D = 28 V.	274 x 140	1
10	RF-Out	RF-Output pad. Matched to 50 ohm.	150 x 150	4

Note 1: Attach bypass capacitor to pads 2-9 per application circuit
Note 2: VG1_A and VG1_B are connected internally so it would be enough to connect either one for proper operation
Note 3: VG2_A and VG2_B are connected internally so it would be enough to connect either one for proper operation
Note 4: The RF Input and Output pad have a ground-signal-ground with a nominal pitch of 1 mil (25 um). The RF ground pads are 110 x 110 microns

Electrostatic Discharge (ESD) Classification

Parameter	Symbol	Class	Test Methodology
Human body Model	HBM	TBD	JEDEC JESD22 A114-D
Charge Device Model	CDM	TBD	JEDEC JESD22 C101-C