| 64-pin Q1/L9 | Pin | | Description |
|---|---|---|---|
| Pin No. | Name | Type | |
| 52 | SYSCLK2 | OP | Synthesised digital clock output 2 |
| 53 | SCLK | IP | C-BUS serial clock input from the µC |
| 54 | RDATA | TS OP | 3-state C-BUS serial data output to the µC. This output is high impedance when not sending data to the µC. |
| 55 | CDATA | IP | C-BUS serial data input from the µC |
| 56 | CSN | IP | C-BUS chip select input from the µC |
| 57 | IRQN | OP | ówire-Orableôoutput for connection to the Interrupt Request input of the µC. This output is pulled down to $DV_{SS}$ when active and is high impedance when inactive. An external pull-up resistor is required. |
| 58 | DVCORE | PWR | Internally generated digital core voltage of approximately 1.8V. This pin should be decoupled to $DV_{SS}$ by capacitors mounted close to the device pins |
| 59 | MOSI | OP | SPI: Master Out Slave In |
| 60 | SSOUT1 | OP | SPI: Slave Select Out 1 |
| 61 | MISO | IP | SPI: Master In Slave Out |
| 62 | SSOUT0 | OP | SPI: Slave Select Out 0 |
| 63 | CLK | OP | SPI: Serial Clock |
| 64 | GPIOA | BI | General Purpose I/O |
| EXPOSED METAL PAD | SUBSTRATE | ~ | On this device, the central metal pad (which is exposed on the Q1 package only) may be electrically unconnected or, alternatively, may be connected to Analogue ground (AVss). **No other electrical connection is permitted.** |

**Notes:**
IP = Input (+ PU/PD = internal pull-up / pull-down resistor of approximately 75kq )
OP = Output
BI = Bidirectional
TS OP = 3-state Output
PWR = Power Connection
NC = No Connection - should NOT be connected to any signal