In each case, it will strip out the 'S' symbols or channel status bits, de-interleave and decode the remaining symbols and place the resulting 12 (RD-LAP) or 6 (MDC) bytes into the Data Block Buffer, setting the BFREE and IRQ bits of the Status Register to '1' when the task is complete.

If an 'Intermediate' block is received then the µC should read out all 12 or 6 bytes from the Data Block Buffer and ignore the CRCERR bit of the Status Register, for a 'Last' block the µC need only read the first 8 or 4 bytes from the Data Block Buffer, and the CRCERR bit in the Status Register will reflect the validity of the received checksum.

As each of the 'S' symbols or channel status bits of the block is received, the SVAL bits of the Status Register will be updated and the SRDY bit set to '1'. (If the SSIEN bit of the Mode Register is '1', then the Status Register IRQ bit will also be set to '1'.) Note that when the third 'S' symbol is received in RD-LAP mode the SRDY bit will be set to '1' coincidentally with the BFREE bit also being set to '1'.

SFS: Search for Frame Sync (RD-LAP and MDC)
This task causes the modem to search the received signal for a 24-symbol (RD-LAP) or 40-bit (MDC) sequence which matches the required Frame Synchronisation pattern(s) allowing 5 bits in error for MDC mode. In RD-LAP mode the allowable errors are approximately 3 bits when FSTOL = 0, 7 bits when FSTOL = 1.

In RD-LAP mode when a match is found the modem will read in the following 'S' symbol, then set the BFREE, IRQ and SRDY bits of the Status Register to '1' and update the SVAL bits. The µC may then write the next task to the Command Register.

In MDC mode when a match is found the modem will set the BFREE, IRQ bits of the Status Register to ‘1’ and set the FSTYPE bit according to the type of Frame Synchronisation pattern received. The µC may then write the next task to the Command Register.

R4S: Read 4 Symbols (RD-LAP only)
This task causes the modem to read the next 4 symbols and translate them directly (without de-interleaving or FEC) to an 8-bit byte which is placed into the Data Block Buffer. The BFREE and IRQ bits of the Status Register will then be set to '1' to indicate that the µC may read the data byte from the Data Block Buffer and write the next task to the Command Register.

This task is intended for special tests and channel monitoring - perhaps preceded by SFS task.

Note that although it is possible to construct message formats which do not rely on the block formatting of the THB, TIB and TLB tasks by using T4S or T24S tasks to transmit and R4S to receive the user’s data, anyone attempting this should be aware that the receive level and timing measurement circuits need to see a reasonably ‘random’ distribution of all four possible symbols in the received signal to operate correctly, and should therefore ‘scramble’ the binary data before transmission.

R8B: Read 8 Bits (MDC only)
This task reads the next 8 received bits and places the resulting 8-bit byte directly (without any attempt to de-interleave, remove channel status bits or apply FEC) into the Data Block Buffer. The BFREE and IRQ bits of the Status Register will then be set to '1' to indicate that the µC may read the data byte from the Data Block Buffer and write the next task to the Command Register.