

**4-Mbit (512K x 8/256K x 16) nvSRAM
带实时时钟**

特性

- 访问时间为 25 ns 和 45 ns
- 内部采用 512K x 8 (CY14B104K) 或 256K x 16 (CY14B104M) 的组织方式
- 只需一个小电容，即可在断电时实现自动存储
- 可通过软件、器件引脚或断电时自动存储 (AutoStore on Power Down) 触发存储至 QuantumTrap 非易失性元件
- 可通过软件或加电触发回读至 SRAM
- 可靠性高
- 无限次读、写和回读循环
- 一百万次 QuantumTrap 存储循环
- 20 年数据保留时间
- 3V +20%, -10% 单电源供电
- 能够实现数据完整性的赛普拉斯 nvSRAM，功能齐全的实时时钟 (RTC)

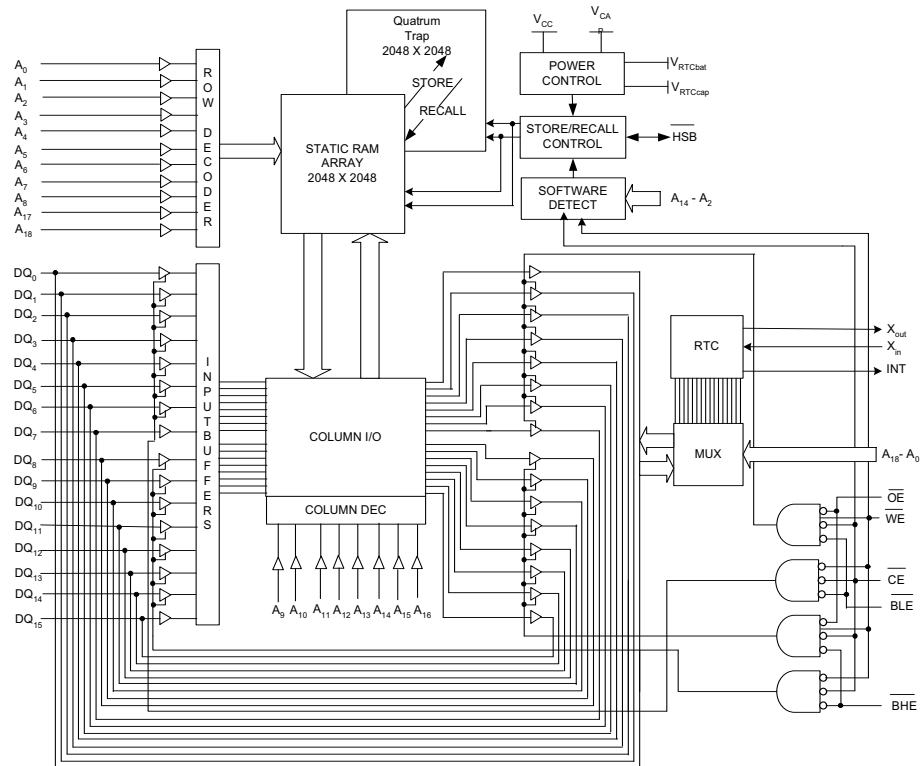
- 看门狗定时器
- 带可编程中断的时钟警报
- RTC 备用电容或电池
- 工业级温度
- 44 和 54 引脚 TSOP II 封装
- 无铅、符合 RoHS 标准

功能说明

赛普拉斯 CY14B104K 和 CY14B104M 将 4 Mbit 的非易失性静态 RAM 和功能齐全的 RTC 整合在了一个单片集成电路中。嵌入式非易失性元件通过采用 QuantumTrap 技术，打造出了世界上最可靠的非易失性存储器。SRAM 能够实现无限次读写循环，而独立的非易失性数据则存储在非易失性元件中。

RTC 功能提供了一个带闰年跟踪及可编程高精度振荡器的精确时钟。警报功能可以编程，以便设置定期的分、时、日或月警报。此外，还提供用于进程控制的可编程看门狗定时器。

逻辑框图 [1、2、3]



- 注:
1. 地址 A₀ - A₁₈ 适用于 x8 配置; 地址 A₀ - A₁₇ 适用于 x16 配置。
 2. 数据 DQ₀ - DQ₇ 适用于 x8 配置; 数据 DQ₀ - DQ₁₅ 适用于 x16 配置。
 3. BHE 和 BLE 仅适用于 x16 配置。

文档修订记录页

文档标题 : CY14B104K, CY14B104M 4-Mbit (512K x 8/256K x 16) nvSRAM 带实时时钟				
文档编号 : 001-63439				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3002218	VLX	08/06/2010	Translation of spec 001-07103 *P
*A	4400717	SCHC	06/06/2014	No technical updates.

销售、解决方案和法律信息

全球销售和设计支持

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