# CY23S09, CY23S05

# Low Cost 3.3 V Spread Aware Zero Delay Buffer

## Features

- 10 MHz to 100 MHz and 133 MHz operating range, compatible with CPU and PCI bus frequencies
- Zero input-output propagation delay
- Multiple low skew outputs
  - Output-output skew less than 250 ps
  - Device-device skew less than 700 ps
  - One input drives five outputs (CY23S05)
  - One input drives nine outputs, grouped as 4 + 4 + 1 (CY23S09)
- Less than 200 ps Cycle-to-cycle jitter
- Test mode to bypass PLL (CY23S09 only, see Select Input Decoding for CY23S09 on page 4)
- Available in space saving 16-pin, 150-mil SOIC, 4.4 mm TSSOP (CY23S09) or 8-pin, 150-mil SOIC package (CY23S05)
- 3.3 V operation, advanced 0.65µ CMOS technology
- Spread Aware

## Functional Description

The CY23S09 is a low cost 3.3 V zero delay buffer designed to distribute high speed clocks and is available in a 16-pin SOIC package. The CY23S05 is an 8-pin version of the CY23S09. It accepts one reference input, and drives out five low skew clocks. The -1H versions of each device operate at up to 100 and 133 MHz frequencies and have higher drive than the -1 devices.

All parts have on-chip PLLs that lock to an input clock on the REF pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad.

The CY23S09 has two bans of four outputs each, which can be controlled by the select inputs as shown in the Select Input Decoding table on Select Input Decoding for CY23S09 on page 4. If all output clocks are not required, Bank B can be three-stated. The select inputs also allow the input clock to be directly applied to the outputs for chip and system testing purposes.

The CY23S09 and CY23S05 PLLs enter a power down mode when there are no rising edges on the REF input. In this state, the outputs are three-stated and the PLL is turned off, resulting in less than 12.0 µA of current draw (for commercial temperature devices) and 25.0 µA (for industrial temperature devices). The CY23S09 PLL shuts down in one additional case, as shown in the Select Input Decoding for CY23S09 on page 4.

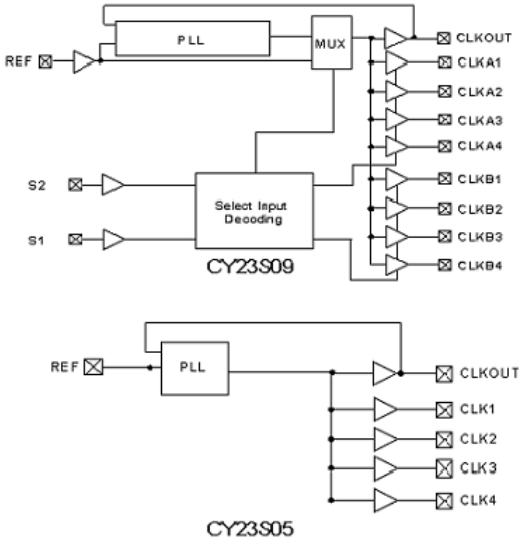
Multiple CY23S09 and CY23S05 devices can accept the same input clock and distribute it. In this case, the skew between the outputs of two devices is guaranteed to be less than 700 ps.

All outputs have less than 200 ps of cycle-to-cycle jitter. The input to output propagation delay on both devices is guaranteed to be less than 350 ps; the output to output skew is guaranteed to be less than 250 ps.

The CY23S05 and CY23S09 is available in two different configurations, as shown in the Ordering Information on page 8. The CY23S05-1 and CY23S09-1 is the base part. The CY23S05-1H and CY23S09-1H is the high drive version of the -1, and its rise and fall times are much faster than -1.

For a complete list of related resources, click here.

## Logic Block Diagram



## Contents

## Pinouts

**Figure 1. Pin Configuration – CY23S09**

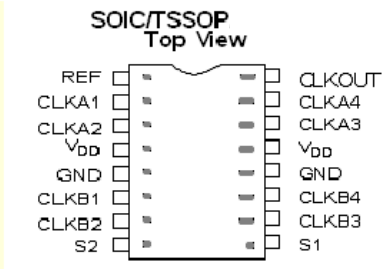



**Figure 2. Pin Configuration – CY23S05**

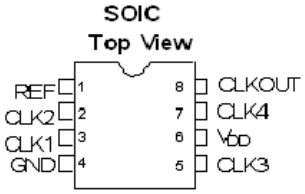



**Table 1. Pin Description for CY23S09**

| Pin | Signal | Description |
|---|---|---|
| 1 | REF[1] | Input reference frequency, 5 V tolerant input |
| 2 | CLKA1[2] | Buffered clock output, bank A |
| 3 | CLKA2[2] | Buffered clock output, bank A |
| 4 | $V_{DD}$ | 3.3 V supply |
| 5 | GND | Ground |
| 6 | CLKB1[2] | Buffered clock output, bank B |
| 7 | CLKB2[2] | Buffered clock output, bank B |
| 8 | S2[3] | Select input, bit 2 |
| 9 | S1[3] | Select input, bit 1 |
| 10 | CLKB3[2] | Buffered clock output, bank B |
| 11 | CLKB4[2] | Buffered clock output, bank B |
| 12 | GND | Ground |
| 13 | $V_{DD}$ | 3.3 V supply |
| 14 | CLKA3[2] | Buffered clock output, bank A |
| 15 | CLKA4[2] | Buffered clock output, bank A |
| 16 | CLKOUT[2] | Buffered output, internal feedback on this pin |

**Table 2. Pin Description for CY23S05**

| Pin | Signal | Description |
|---|---|---|
| 1 | REF[1] | Input reference frequency, 5 V tolerant input |
| 2 | CLK2[2] | Buffered clock output |
| 3 | CLK1[2] | Buffered clock output |
| 4 | GND | Ground |
| 5 | CLK3[2] | Buffered clock output |
| 6 | $V_{DD}$ | 3.3 V supply |
| 7 | CLK4[2] | Buffered clock output |
| 8 | CLKOUT[2] | Buffered clock output, internal feedback on this pin |

**Notes**
1. Weak pull down.
2. Weak pull down on all outputs.
3. Weak pull up on these inputs.

## Select Input Decoding for CY23S09

| S2 | S1 | CLOCK A1–A4 | CLOCK B1–B4 | CLKOUT[4] | Output Source | PLL Shutdown |
|---|---|---|---|---|---|---|
| 0 | 0 | Three-state | Three-state | Driven | PLL | N |
| 0 | 1 | Driven | Three-state | Driven | PLL | N |
| 1 | 0 | Driven | Driven | Driven | Reference | Y |
| 1 | 1 | Driven | Driven | Driven | PLL | N |

## Functional Overview

### Zero Delay and Skew Control

All outputs must be uniformly loaded to achieve Zero Delay between the input and output. Because the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input-output delay. This is shown in the above graph.

For applications requiring zero input-output delay, all outputs, including CLKOUT, must be equally loaded. Even if CLKOUT is not used, it must have a capacitive load equal to that on other outputs, to obtain zero input-output delay. If input to output delay adjustments are required, use the above graph to calculate loading differences between the CLKOUT pin and other outputs.

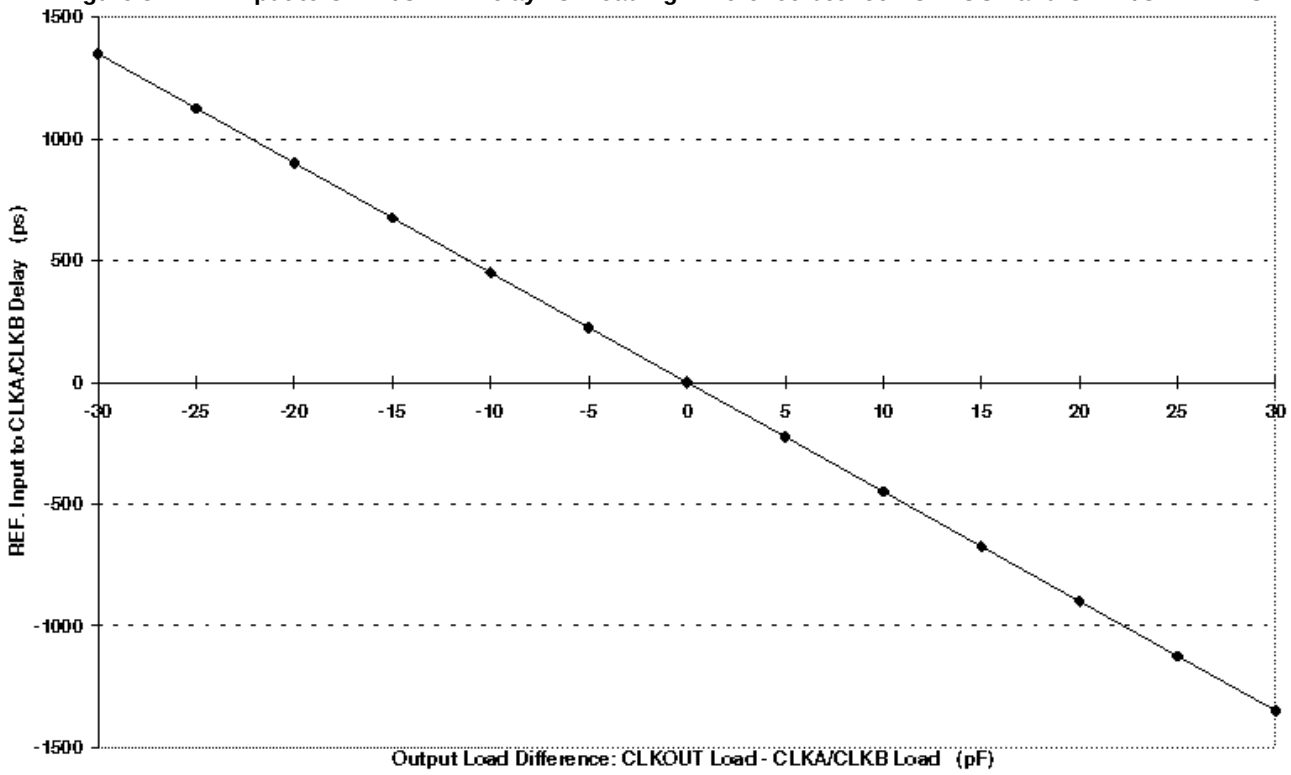
For zero output-output skew, be sure to load all outputs equally. For further information refer to the application note titled AN1234 - Understanding Cypress's Zero Delay Buffers.

### Spread Aware

Many systems being designed now use a technology called Spread Spectrum Frequency Timing Generation. Cypress is one of the pioneers of SSFTG development and designed this product so as not to filter off the Spread Spectrum feature of the Reference input, assuming it exists. When a zero delay buffer is not designed to pass the SS feature through, the result is a significant amount of tracking skew, which may cause problems in systems requiring synchronization.

For more details on Spread Spectrum timing technology, please see the Cypress Whitepaper EMI and Spread Spectrum Technology.

**Figure 3. REF. Input to CLKA/CLKB Delay vs. Loading Difference between CLKOUT and CLKA/CLKB Pins**




**Note**
4. This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and output.

## Maximum Ratings

Supply voltage to ground potential .....–0.5 V to +7.0 V
DC input voltage (Except REF) .....–0.5 V to $V_{DD}$ + 0.5 V
DC input voltage REF.....–0.5 V to 7 V
Storage temperature .....–65 °C to +150 °C
Maximum soldering temperature (10 seconds)..... 260 °C
Junction temperature..... 150 °C
Static discharge voltage
(per MIL-STD-883, Method 3015) .....> 2,000 V

## Operating Conditions for CY23S05SXX-XX and CY23S09SXX-XX (Industrial, Commercial Devices)[5]

| Parameter | Description | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply voltage | 3.0 | 3.6 | V |
| $T_A$ | Operating temperature - Ambient (Commercial) | 0 | 70 | °C |
| | Operating temperature - Ambient (Industrial) | -40 | 85 | °C |
| $C_L$ | Load capacitance, below 100 MHz | | 30 | pF |
| $C_L$ | Load capacitance, from 100 MHz to 133 MHz | | 10 | pF |
| $C_{IN}$ | Input capacitance | | 7 | pF |

## Electrical Characteristics for CY23S05SXX-XX and CY23S09SXX-XX (Industrial, Commercial Devices)

| Parameter | Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IL}$ | Input LOW voltage[6] | | | 0.8 | V |
| $V_{IH}$ | Input HIGH voltage[6] | | 2.0 | | V |
| $I_{IL}$ | Input LOW current | $V_{IN}$ = 0 V | | 50.0 | µA |
| $I_{IH}$ | Input HIGH current | $V_{IN}$ = $V_{DD}$ | | 100.0 | µA |
| $V_{OL}$ | Output LOW voltage[7] | $I_{OL}$ = 8 mA (–1)<br>$I_{OH}$ = 12 mA (–1H) | | 0.4 | V |
| $V_{OH}$ | Output HIGH voltage[7] | $I_{OH}$ = –8 mA (–1)<br>$I_{OL}$ = –12 mA (–1H) | 2.4 | | V |
| $I_{DD}$ (PD mode) | Power-down supply current | REF = 0 MHz | | 12.0 | µA |
| $I_{DD}$ | Supply current | Unloaded outputs at 66.67 MHz, SEL inputs at $V_{DD}$ | | 32.0 | mA |

## Switching Characteristics for CY23S05SXC-1 and CY23S09SXC-1 Commercial Temperature Devices [8]

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| t1 | Output frequency | 30 pF load<br>10 pF load | 10<br>10 | | 100<br>133.33 | MHz<br>MHz |
| | Duty cycle[7] = $t_2 \div t_1$ | Measured at 1.4 V, $F_{out}$ = 66.67 MHz | 40.0 | 50.0 | 60.0 | % |
| t3 | Rise time[7] | Measured between 0.8 V and 2.0 V | | | 2.50 | ns |
| $t_4$ | Fall time[7] | Measured between 0.8 V and 2.0 V | | | 2.50 | ns |
| $t_5$ | Output-to-output skew[7] | All outputs equally loaded | | | 250 | ps |
| $t_6$ | Delay, REF Rising Edge to CLKOUT Rising Edge[7] | Measured at $V_{DD}$/2 | | 0 | ±350 | ps |
| $t_7$ | Device-to-device skew[7] | Measured at $V_{DD}$/2 on the CLKOUT pins | | 0 | 700 | ps |
| $t_J$ | Cycle-to-cycle jitter[7] | Measured at 66.67 MHz, loaded outputs | | | 200 | ps |
| $t_{LOCK}$ | PLL lock time[7] | Stable power supply, valid clock presented on REF pin | | | 1.0 | ms |

**Notes**
5. Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power up. Power supply sequencing is NOT required.
6. REF input has a threshold voltage of $V_{DD}$/2.
7. Parameter is guaranteed by design and characterization. Not 100% tested in production.
8. All parameters specified with loaded outputs.

## Switching Characteristics for CY23S05SXI-1H Industrial Temperature Devices[8]

| Parameter | Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| t1 | Output frequency | 30 pF load<br>10 pF load | 10<br>10 | | 100<br>133.33 | MHz<br>MHz |
| | Duty cycle[7] = $t_2 \div t_1$ | Measured at 1.4 V, $F_{out}$ = 66.67 MHz | 40.0 | 50.0 | 60.0 | % |
| | Duty cycle[7] = $t_2 \div t_1$ | Measured at 1.4 V, $F_{out}$ <50.0 MHz | 45.0 | 50.0 | 55.0 | % |
| t3 | Rise time[7] | Measured between 0.8 V and 2.0 V | | | 1.50 | ns |
| $t_4$ | Fall time[7] | Measured between 0.8 V and 2.0 V | | | 1.50 | ns |
| $t_5$ | Output-to-output skew[7] | All outputs equally loaded | | | 250 | ps |
| $t_6$ | Delay, REF Rising Edge to CLKOUT Rising Edge[7] | Measured at $V_{DD}/2$ | | 0 | ±350 | ps |
| $t_7$ | Device-to-Device Skew[7] | Measured at $V_{DD}/2$ on the CLKOUT pins of devices | | 0 | 700 | ps |
| $t_8$ | Output slew rate[7] | Measured between 0.8 V and 2.0 V using Test Circuit #2 | 1 | | | V/ns |
| $t_J$ | Cycle-to-cycle jitter[7] | Measured at 66.67 MHz, loaded outputs | | | 200 | ps |
| $t_{LOCK}$ | PLL lock time[7] | Stable power supply, valid clock presented on REF pin | | | 1.0 | ms |

## Switching Waveforms

**Figure 4. Duty Cycle Timing**

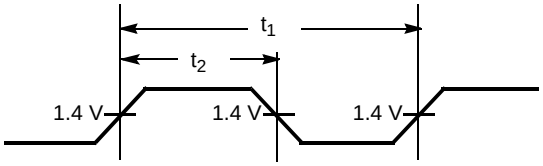



**Figure 5. All Outputs Rise/Fall Time**

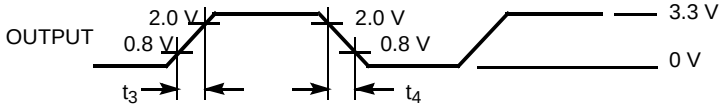



**Figure 6. Output-Output Skew**

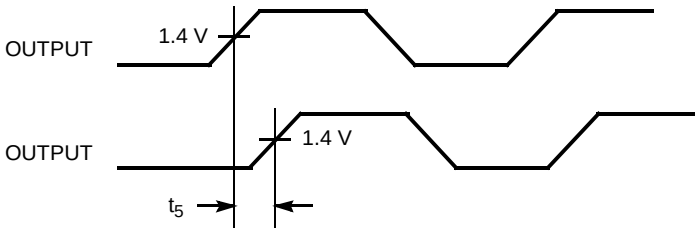
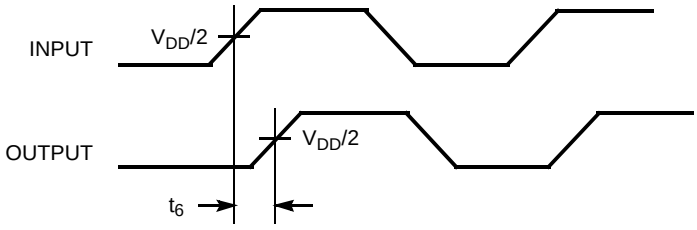
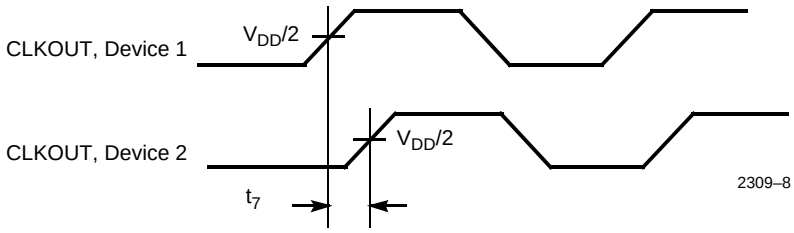



**Figure 7. Input-Output Propagation Delay**



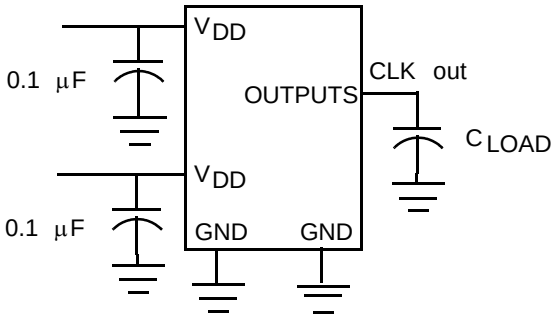
## Switching Waveforms continued

**Figure 8. Device-Device Skew**

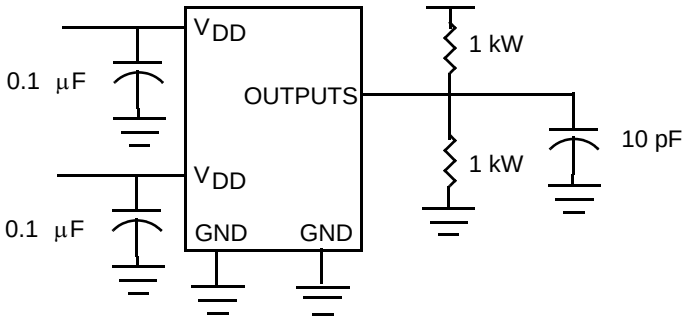



## Test Circuits

**Test Circuit # 1**




**Test Circuit # 2**




For parameter t8 (output slew rate) on –1H devices

## Thermal Resistance

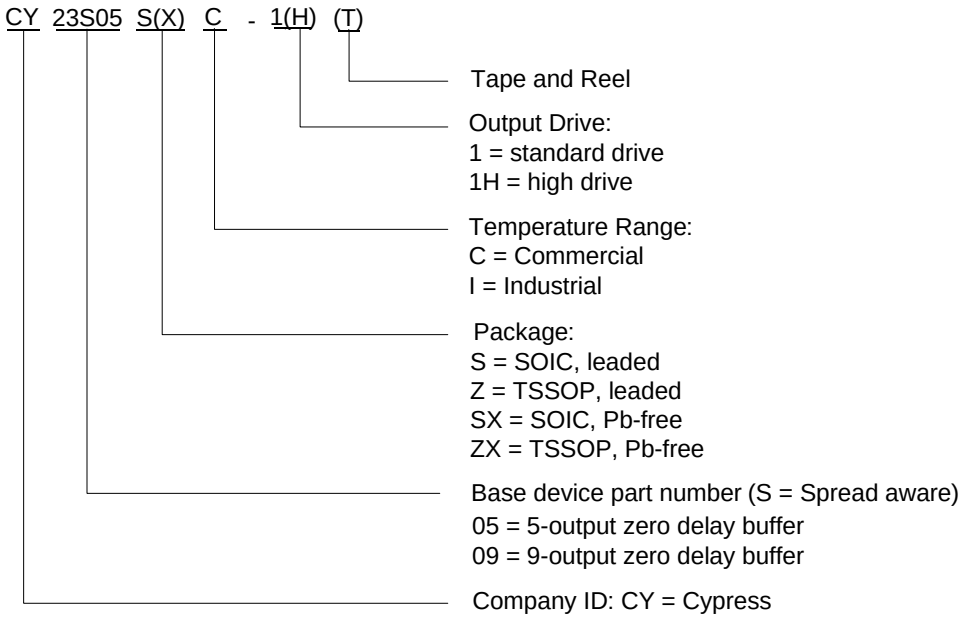
| Parameter[9] | Description | Test Conditions | 8-pin SOIC | 16-pin SOIC | 16-pin TSSOP | Unit |
|---|---|---|---|---|---|---|
| Theta $J_A$ | Thermal resistance (junction to ambient) | Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51. | 132 | 108 | 108 | °C/W |
| Theta $J_C$ | Thermal resistance (junction to case) | | 43 | 37 | 17 | °C/W |

**Note**
9. These parameters are guaranteed by design and are not tested.

## Ordering Information

| Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|
| **Pb-Free** | | | |
| CY23S05SXC-1 | SZ08 | 8-pin 150-mil SOIC | Commercial (0 ° to 70 °C) |
| CY23S05SXC-1T | SZ08 | 8-pin 150-mil SOIC – Tape and Reel | Commercial (0 ° to 70 °C) |
| CY23S05SXC-1H | SZ08 | 8-pin 150-mil SOIC | Commercial (0 ° to 70 °C) |
| CY23S05SXC-1HT | SZ08 | 8-pin 150-mil SOIC – Tape and Reel | Commercial (0 ° to 70 °C) |
| CY23S05SXI-1 | SZ08 | 8-pin 150-mil SOIC | Industrial (–40 ° to 85 °C) |
| CY23S05SXI-1T | SZ08 | 8-pin 150-mil SOIC – Tape and Reel | Industrial (–40 ° to 85 °C) |
| CY23S09SXC-1 | SZ16 | 16-pin 150-mil SOIC | Commercial (0 ° to 70 °C) |
| CY23S09SXC-1T | SZ16 | 16-pin 150-mil SOIC – Tape and Reel | Commercial (0 ° to 70 °C) |
| CY23S09SXC-1H | SZ16 | 16-pin 150-mil SOIC | Commercial (0 ° to 70 °C) |
| CY23S09SXC-HT | SZ16 | 16-pin 150-mil SOIC – Tape and Reel | Commercial (0 ° to 70 °C) |
| CY23S09ZXC-1H | ZZ16 | 16-pin 4.4 mm TSSOP | Commercial (0 ° to 70 °C) |
| CY23S09ZXC-1HT | ZZ16 | 16-pin 4.4 mm TSSOP – Tape and Reel | Commercial (0 ° to 70 °C) |

### Ordering Code Definitions

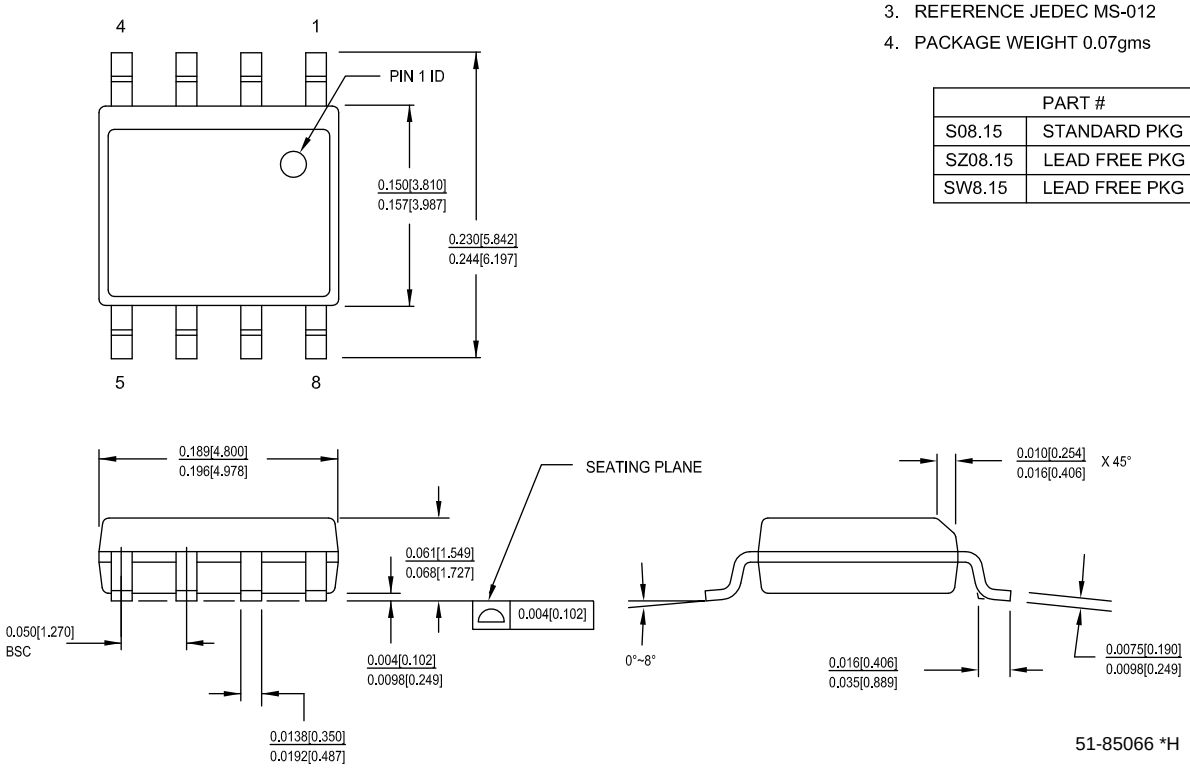


## Package Diagrams

**Figure 9. 8-Pin (150-Mil) SOIC S08 and SZ08**

1. DIMENSIONS IN INCHES[MM] MIN.
   MAX.
2. PIN 1 ID IS OPTIONAL,
   ROUND ON SINGLE LEADFRAME
   RECTANGULAR ON MATRIX LEADFRAI
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

| PART # | |
|---|---|
| S08.15 | STANDARD PKG |
| SZ08.15 | LEAD FREE PKG |
| SW8.15 | LEAD FREE PKG |



## Package Diagrams continued

**Figure 10. 16-Pin (150-Mil) SOIC S16 and SZ16**

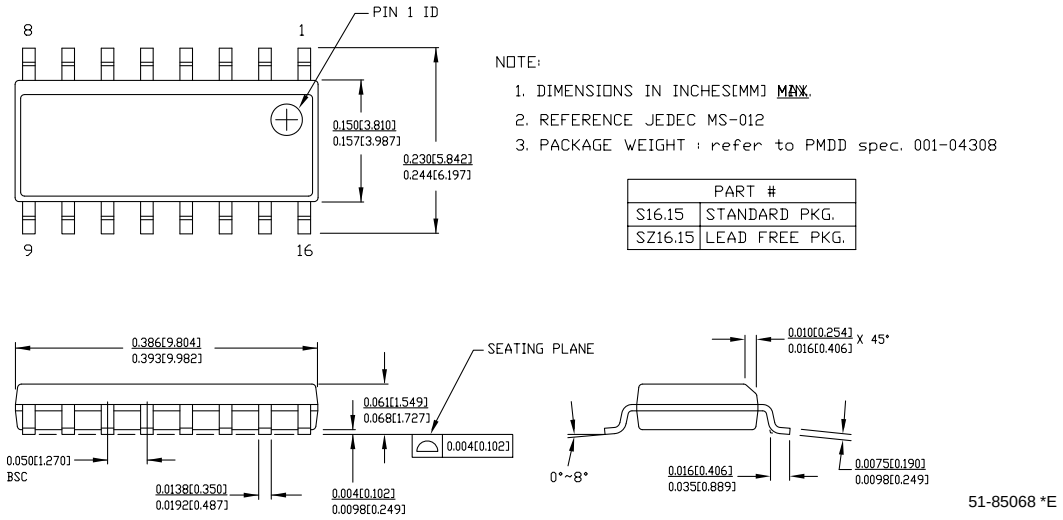
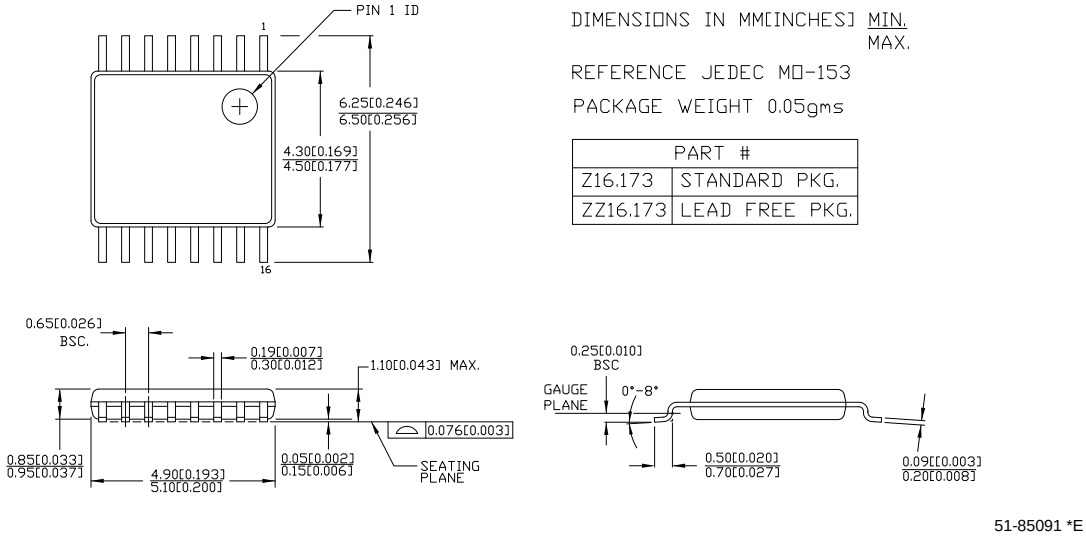



**Figure 11. 16-Pin TSSOP 4.40 mm Body Z16 and ZZ16**



## Acronym

| Acronym | Description |
|---|---|
| CMOS | complementary metal oxide semiconductor |
| EMI | electromagnetic interference |
| PLL | phase-locked loop |
| SOIC | small outline integrated circuit |
| SS | spread spectrum |
| SSFTG | spread spectrum frequency timing generator |
| SSOP | shrunk small outline package |
| TSSOP | thin shrunk small outline package |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| MHZ | megahertz |
| uA | microamperes |
| mA | milliamperes |
| ms | milliseconds |
| ns | nanoseconds |
| % | percent |
| pF | picofarads |
| ps | picoseconds |
| V | volt |

## Document History Page

| Document Title: CY23S09/CY23S05 Low Cost 3.3 V Spread Aware Zero Delay Buffer<br>Document Number: 38-07296 | | | | |
|---|---|---|---|---|
| **Rev.** | **ECN No.** | **Submission Date** | **Orig. of Change** | **Description of Change** |
| ** | 111147 | 11/14/01 | DSG | Changed from spec number 38-01094 to 38-07296 |
| *A | 111773 | 02/20/02 | CTK | Added 150-mil SSOP option |
| *B | 122885 | 12/22/02 | RBI | Added power-up requirements to Operating Conditions |
| *C | 267849 | See ECN | RGL | Added Lead-Free devices |
| *D | 2595524 | 10/23/08 | CXQ/PYRS | Added device “Status” to Ordering Information |
| *E | 2761988 | 09/10/09 | KVM | Removed obsolete parts from Ordering Information table: CY23S09ZC-1, CY23S09OC-1, CY23S09OC-1H, CY23S09ZXC-1, CY23S09OXC-1, CY23S09OXC-1H.<br>Added CY23S05SXC-1T, CY23S05SXC-1HT, CY23S09SXC-1T, CY23S09SXC-1HT, CY23S09ZXC-1HT.<br>Removed Status column from Ordering Information table; added footnote.<br>Updated package names and added numerical temperature range to Ordering Information table.<br>Removed QSOP package drawing. |
| *F | 2897373 | 03/22/10 | CXQ | Removed part numbers CY23S05SC-1, CY23S05SC-1H, CY23S09SC-1, CY23S09SC-1H, and CY23S09ZC-1H from Ordering Information table.<br>Added CY23S05SXI-1 and CY23S05SXI-1T to Ordering Information table.<br>Updated package diagrams.<br>Updated copyright section. |
| *G | 3394655 | 10/04/11 | PURU | Added Figure 3<br>Updated Hyper links<br>Updated Package Diagrams<br>Added Ordering Code Definitions, Acronym, and Units of Measure. |
| *H | 4564025 | 11/07/2014 | TAVA | Removed the SSOP package in Features.<br>Updated Figure 1 (removed SSOP).<br>Updated Figure 7.<br>Replaced all occurrences of SC and SI with SXC and SXI in the following tables:<br>Operating Conditions for CY23S05SXX-XX and CY23S09SXX-XX (Industrial, Commercial Devices)[5]<br><br>Electrical Characteristics for CY23S05SXX-XX and CY23S09SXX-XX (Industrial, Commercial Devices)<br><br>Switching Characteristics for CY23S05SXC-1 and CY23S09SXC-1 Commercial Temperature Devices [8]<br><br>Switching Characteristics for CY23S05SXI-1H Industrial Temperature Devices[8]<br><br>Updated the table, Operating Conditions for CY23S05SXX-XX and CY23S09SXX-XX (Industrial, Commercial Devices)[5].<br>Removed CY23S09SI-1H in the table title, in Switching Characteristics for CY23S05SXI-1H Industrial Temperature Devices[8].<br>Updated Figure 9, Figure 10, and Figure 11 in Package Diagrams. |
| *I | 5738816 | 05/24/2017 | PSR | Updated the link for AN1234.<br>Added Thermal Resistance.<br>Updated the Cypress logo, copyright information, Sales, Solutions, and Legal Information based on the new template. |