# CY62157G Automotive

# 8-Mbit (512K words × 16-bit) Static RAM with Error-Correcting Code (ECC)

## Features

- AEC-Q100 Qualified
- Ultra-low standby power
  - Typical standby current: 5 µA
  - Maximum standby current: 35 µA
- High speed: 45 ns/55 ns
- Embedded error-correcting code (ECC) for single-bit error correction[1, 2]
- Temperature ranges:
  - Automotive-A: –40 °C to +85 °C
- Wide operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V
- 1.5-V data retention
- Transistor-transistor logic (TTL)-compatible inputs and outputs
- Available in Pb-free 48-ball VFBGA, 48-pin TSOP II, and 44-pin TSOP I packages

## Functional Description

CY62157G is a high-performance CMOS low-power (MoBL®) SRAM device with embedded ECC. This device is offered in dual chip-enable.

Devices with dual chip-enable are accessed by asserting both chip-enable inputs – $\overline{CE_1}$ as LOW and $CE_2$ as HIGH.

Data writes are performed by asserting the Write Enable input ($\overline{WE}$) LOW, and providing the data and address on device data ($I/O_0$ through $I/O_{15}$) and address ($A_0$ through $A_{19}$) pins respectively. The Byte High/Low Enable ($\overline{BHE}$, $\overline{BLE}$) inputs control byte writes, and write data on the corresponding I/O lines to the memory location specified. $\overline{BHE}$ controls $I/O_8$ through $I/O_{15}$; $\overline{BLE}$ controls $I/O_0$ through $I/O_7$.

Data reads are performed by asserting the Output Enable ($\overline{OE}$) input and providing the required address on the address lines. Read data is accessible on I/O lines ($I/O_0$ through $I/O_{15}$). Byte accesses can be performed by asserting the required byte enable signal ($\overline{BHE}$, $\overline{BLE}$) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os ($I/O_0$ through $I/O_{15}$) are placed in a HI-Z state when the device is deselected ($\overline{CE_1}$ HIGH / $CE_2$ LOW for dual chip-enable device), or control signals are de-asserted ($\overline{OE}$, $\overline{BLE}$, and $\overline{BHE}$).

These devices also have a unique “Byte Power down” feature where if both the Byte Enables ($\overline{BHE}$ and $\overline{BLE}$) are disabled, the device seamlessly switches to standby mode irrespective of the state of the chip enable(s), thereby saving power.

The CY62157G device is available in a Pb-free 48-ball VFBGA, 48-pin TSOPI, and 44-pin TSOP II packages. Refer to the Logic Block Diagram – CY62157G on page 2,the Pin Configurations on page 4, and the associated footnotes for details.

## Product Portfolio

| Product | Range | $V_{CC}$ Range (V) | Speed (ns) | Power Dissipation | | | |
|---|---|---|---|---|---|---|---|
| | | | | Operating $I_{CC}$, (mA), $f = f_{max}$ | | Standby, $I_{SB2}$ (µA) | |
| | | | | Typ [3] | Max | Typ [3] | Max |
| CY62157G18 | Automotive-A | 1.65 V to 2.2 V | 55 | 18 | 22 | 4.5 | 8 |
| CY62157G30 | | 2.2 V to 3.6 V | 45 | 18 | 25 | 1.4 | 6.5 |

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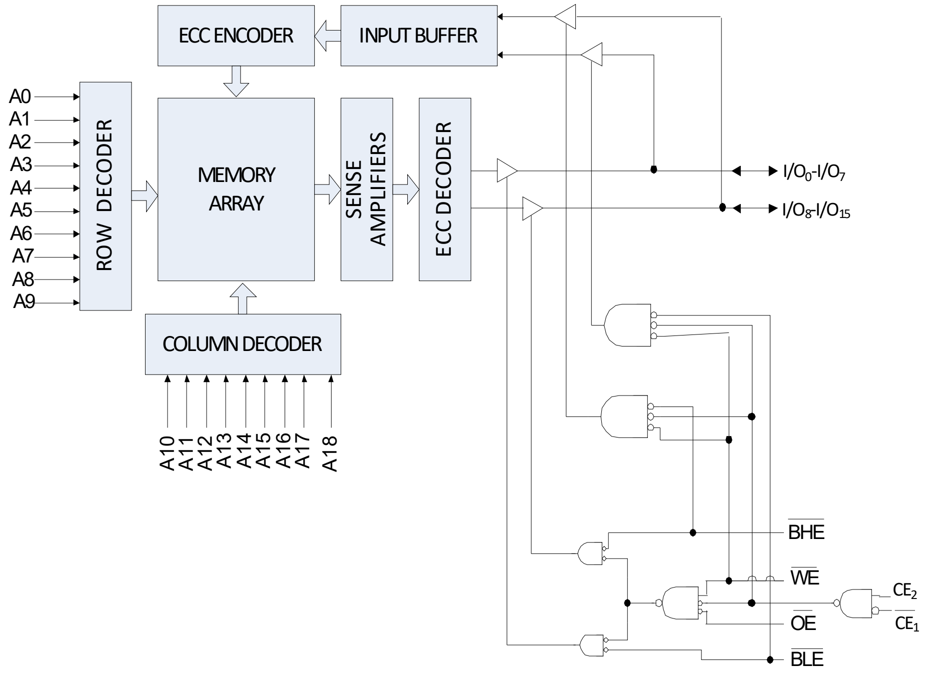
**Notes**

1. SER FIT rate <0.1 FIT/Mb. Refer to AN88889 for details.
2. This device does not support automatic write-back on error detection.
3. Indicates the value for the center of distribution at 3.0 V (or 1.8 V), 25 °C and not 100% tested.

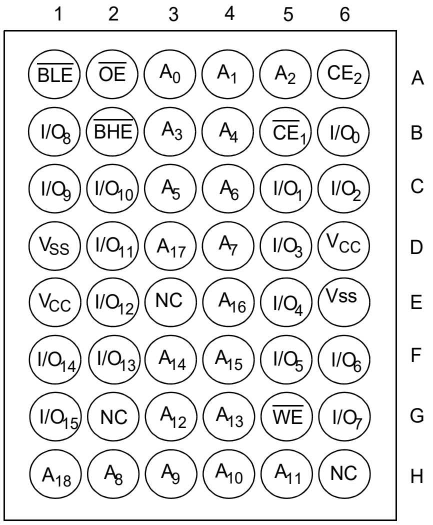
## Logic Block Diagram – CY62157G



## Contents

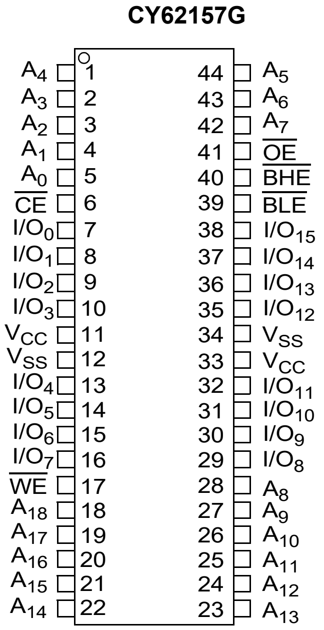
## Pin Configurations

**Figure 1. 48-ball VFBGA Pinout [4]**



| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| A | $\overline{BLE}$ | $\overline{OE}$ | $A_0$ | $A_1$ | $A_2$ | $CE_2$ |
| B | $I/O_8$ | $\overline{BHE}$ | $A_3$ | $A_4$ | $\overline{CE}_1$ | $I/O_0$ |
| C | $I/O_9$ | $I/O_{10}$ | $A_5$ | $A_6$ | $I/O_1$ | $I/O_2$ |
| D | $V_{SS}$ | $I/O_{11}$ | $A_{17}$ | $A_7$ | $I/O_3$ | $V_{CC}$ |
| E | $V_{CC}$ | $I/O_{12}$ | NC | $A_{16}$ | $I/O_4$ | $V_{SS}$ |
| F | $I/O_{14}$ | $I/O_{13}$ | $A_{14}$ | $A_{15}$ | $I/O_5$ | $I/O_6$ |
| G | $I/O_{15}$ | NC | $A_{12}$ | $A_{13}$ | $\overline{WE}$ | $I/O_7$ |
| H | $A_{18}$ | $A_8$ | $A_9$ | $A_{10}$ | $A_{11}$ | NC |

**Figure 2. 44-pin TSOP II Pinout [4]**



| Signal | Pin | Pin | Signal |
|---|---|---|---|
| $A_4$ | 1 | 44 | $A_5$ |
| $A_3$ | 2 | 43 | $A_6$ |
| $A_2$ | 3 | 42 | $A_7$ |
| $A_1$ | 4 | 41 | $\overline{OE}$ |
| $A_0$ | 5 | 40 | $\overline{BHE}$ |
| $\overline{CE}$ | 6 | 39 | $\overline{BLE}$ |
| $I/O_0$ | 7 | 38 | $I/O_{15}$ |
| $I/O_1$ | 8 | 37 | $I/O_{14}$ |
| $I/O_2$ | 9 | 36 | $I/O_{13}$ |
| $I/O_3$ | 10 | 35 | $I/O_{12}$ |
| $V_{CC}$ | 11 | 34 | $V_{SS}$ |
| $V_{SS}$ | 12 | 33 | $V_{CC}$ |
| $I/O_4$ | 13 | 32 | $I/O_{11}$ |
| $I/O_5$ | 14 | 31 | $I/O_{10}$ |
| $I/O_6$ | 15 | 30 | $I/O_9$ |
| $I/O_7$ | 16 | 29 | $I/O_8$ |
| $\overline{WE}$ | 17 | 28 | $A_8$ |
| $A_{18}$ | 18 | 27 | $A_9$ |
| $A_{17}$ | 19 | 26 | $A_{10}$ |
| $A_{16}$ | 20 | 25 | $A_{11}$ |
| $A_{15}$ | 21 | 24 | $A_{12}$ |
| $A_{14}$ | 22 | 23 | $A_{13}$ |

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**Note**

4. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.

## Pin Configurations

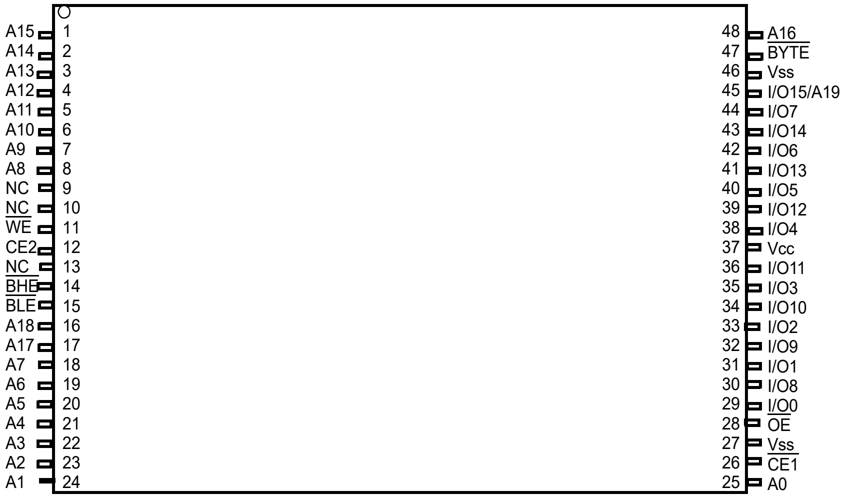

**Figure 3. 48-pin TSOP I Pinout (Top View)** [5, 6]

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**Notes**

5. NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.
6. Tie the $\overline{\text{BYTE}}$ pin in the 48-pin TSOP I package to $V_{CC}$ to use the device as a 512K × 16 SRAM. The 48-pin TSOP I package can also be used as a 1M × 8 SRAM by tying the $\overline{\text{BYTE}}$ signal to $V_{SS}$. In the 1M × 8 configuration, Pin 45 is the extra address line A19, while $\overline{\text{BHE}}$, $\overline{\text{BLE}}$, and $I/O_8$ to $I/O_{14}$ pins are not used and can be left floating.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ............................... –65 °C to + 150 °C

Ambient temperature
with power applied ................................. –55 °C to + 125 °C

Supply voltage
to ground potential [7] .......................... –0.5 V to $V_{CC}$ + 0.5 V

DC voltage applied to outputs
in HI-Z state [7] .................................... –0.5 V to $V_{CC}$ + 0.5 V

DC input voltage [7] ............................ –0.5 V to $V_{CC}$ + 0.5 V

Output current into outputs (LOW) ............................. 20 mA

Static discharge voltage
(MIL-STD-883, Method 3015) ................................ >2001 V

Latch-up current ..................................................... >140 mA

## Operating Range

| Grade | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Automotive-A | –40 °C to +85 °C | 1.65 V to 2.2 V<br>2.2 V to 3.6 V |

**Note**

7. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = $V_{CC}$ + 2 V for pulse durations of <2 ns.

## DC Electrical Characteristics

Over the Operating Range

| Parameter | Description | | Test Conditions | | 45/55 ns (Automotive-A) | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | Min | Typ [9] | Max | |
| $V_{OH}$ | Output HIGH voltage | 1.65 V to 2.2 V | $V_{CC}$ = Min, $I_{OH}$ = –0.1 mA | | 1.4 | – | – | V |
| | | 2.2 V to 2.7 V | $V_{CC}$ = Min, $I_{OH}$ = –0.1 mA | | 2.0 | – | – | |
| | | 2.7 V to 3.6 V | $V_{CC}$ = Min, $I_{OH}$ = –1.0 mA | | 2.4 | – | – | |
| $V_{OL}$ | Output LOW voltage | 1.65 V to 2.2 V | $V_{CC}$ = Min, $I_{OL}$ = 0.1 mA | | – | – | 0.2 | V |
| | | 2.2 V to 2.7 V | $V_{CC}$ = Min, $I_{OL}$ = 0.1 mA | | – | – | 0.4 | |
| | | 2.7 V to 3.6 V | $V_{CC}$ = Min, $I_{OL}$ = 2.1 mA | | – | – | 0.4 | |
| $V_{IH}$ | Input HIGH voltage[8] | 1.65 V to 2.2 V | – | | 1.4 | – | $V_{CC}$ + 0.2 | V |
| | | 2.2 V to 2.7 V | – | | 1.8 | – | $V_{CC}$ + 0.3 | |
| | | 2.7 V to 3.6 V | – | | 2.0 | – | $V_{CC}$ + 0.3 | |
| $V_{IL}$ | Input LOW voltage[8] | 1.65 V to 2.2 V | – | | –0.2 | – | 0.4 | V |
| | | 2.2 V to 2.7 V | – | | –0.3 | – | 0.6 | |
| | | 2.7 V to 3.6 V | – | | –0.3 | – | 0.8 | |
| $I_{IX}$ | Input leakage current | | GND ≤ $V_{IN}$ ≤ $V_{CC}$ | | –1.0 | – | +1.0 | µA |
| $I_{OZ}$ | Output leakage current | | GND ≤ $V_{OUT}$ ≤ $V_{CC}$, Output disabled | | –1.0 | – | +1.0 | µA |
| $I_{CC}$ | $V_{CC}$ operating supply current | 1.65 V to 2.2 V | $V_{CC}$ = Max, $I_{OUT}$ = 0 mA, CMOS levels | f = $f_{MAX}$ | – | 18 | 22 | mA |
| | | | | f = 1 MHz | – | 6 | 7 | mA |
| | | 2.2 V to 3.6 V | $V_{CC}$ = Max, $I_{OUT}$ = 0 mA, CMOS levels | f = $f_{MAX}$ | – | 18 | 25 | mA |
| | | | | f = 1 MHz | – | 6 | 7 | mA |
| $I_{SB1}$[10] | Automatic power down current – CMOS inputs; $V_{CC}$ = 2.2 to 3.6 V | | $\overline{CE}_1$ ≥ $V_{CC}$ – 0.2 V or<br>$CE_2$ ≤ 0.2 V or<br>($\overline{BHE}$ and $\overline{BLE}$) ≥ $V_{CC}$ – 0.2 V,<br>$V_{IN}$ ≥ $V_{CC}$ – 0.2 V or<br>$V_{IN}$ ≤ 0.2 V,<br>f = $f_{max}$ (address and data only),<br>f = 0 ($\overline{OE}$, and $\overline{WE}$),<br>$V_{CC}$ = $V_{CC(max)}$ | | – | 1.4 | 6.5 | µA |
| $I_{SB1}$[10] | Automatic power down current – CMOS inputs; $V_{CC}$ = 1.65 to 2.2 V | | | | – | – | 8 | µA |
| $I_{SB2}$[10] | Automatic power down current – CMOS inputs; $V_{CC}$ = 2.2 to 3.6 V | | $\overline{CE}_1$ ≥ $V_{CC}$ – 0.2 V or<br>$CE_2$ ≤ 0.2 V or<br>($\overline{BHE}$ and $\overline{BLE}$) ≥ $V_{CC}$ – 0.2 V,<br>$V_{IN}$ ≥ $V_{CC}$ – 0.2 V or<br>$V_{IN}$ ≤ 0.2 V,<br>f = 0, $V_{CC}$ = $V_{CC(max)}$ | | – | 1.4 | 6.5[11] | µA |
| $I_{SB2}$[10] | Automatic power down current – CMOS inputs; $V_{CC}$ = 1.65 to 2.2 V | | | | – | – | 8 | µA |

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**Notes**

8. $V_{IL(min)}$ = –2.0 V and $V_{IH(max)}$ = $V_{CC}$ + 2 V for pulse durations of < 2 ns.
9. Indicates the value for the center of Distribution at 3.0 V (or 1.8V), 25 °C and not 100% tested.
10. Chip enables ($\overline{CE}_1$ and $CE_2$) and $\overline{BHE}$, $\overline{BLE}$ must be tied to CMOS levels to meet the $I_{SB1}$/$I_{SB2}$/$I_{CCDR}$ spec. Other inputs can be left floating.
11. ISB2 (max.) for 44TSOP package = 8uA, only when the chip is deselected by disabling both BHE and BLE.

## Capacitance

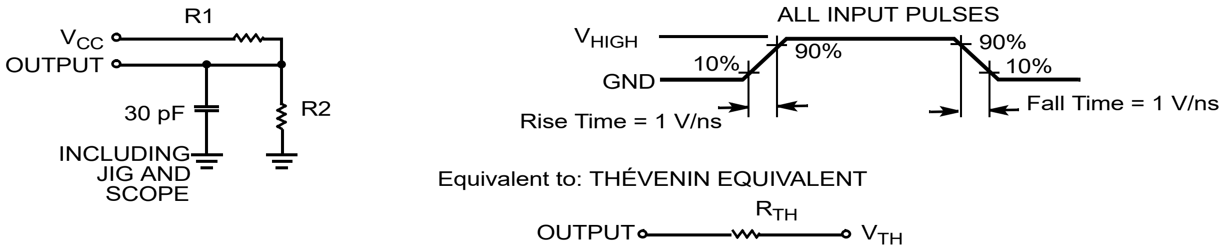
| Parameter [12] | Description | Test Conditions | Max | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $T_A$ = 25 °C, f = 1 MHz, $V_{CC} = V_{CC(typ)}$ | 10 | pF |
| $C_{OUT}$ | Output capacitance | | 10 | pF |

## Thermal Resistance

| Parameter [12] | Description | Test Conditions | 48-ball VFBGA | 44-pin TSOP II | 48-pin TSOP I | Unit |
|---|---|---|---|---|---|---|
| $\Theta_{JA}$ | Thermal resistance (junction to ambient) | Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board | 36.92 | 65.91 | 60.07 | °C/W |
| $\Theta_{JC}$ | Thermal resistance (junction to case) | | 13.55 | 13.96 | 9.73 | °C/W |

## AC Test Loads and Waveforms

**Figure 4. AC Test Loads and Waveforms**



| Parameters | 1.8 V | 2.5 V | 3.0 V | Unit |
|---|---|---|---|---|
| R1 | 13500 | 16667 | 1103 | Ω |
| R2 | 10800 | 15385 | 1554 | Ω |
| $R_{TH}$ | 6000 | 8000 | 645 | Ω |
| $V_{TH}$ | 0.80 | 1.20 | 1.75 | V |

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**Note**

12. Tested initially and after any design or process changes that may affect these parameters.

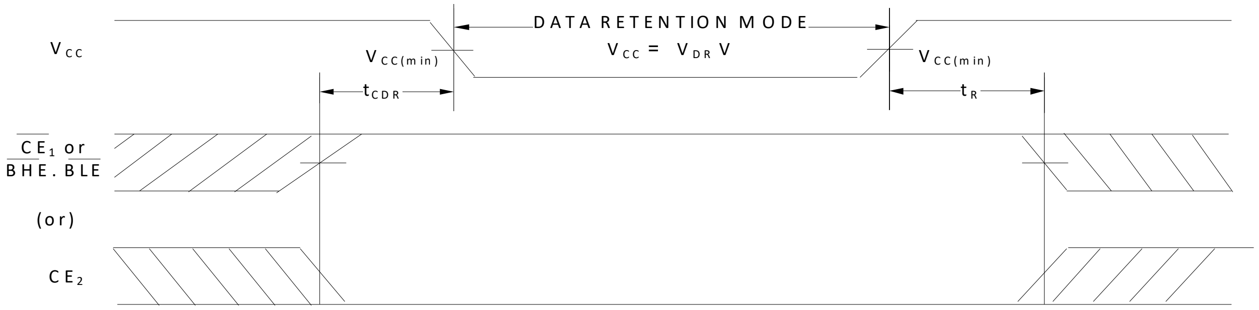
## Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | | (Automotive-A) | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min | Typ [13] | Max | |
| $V_{DR}$ | $V_{CC}$ for data retention | $2.2\text{ V} < V_{CC} \le 3.6\text{ V}$ | | 1 | – | – | V |
| | | $1.65\text{ V} < V_{CC} \le 2.2\text{ V}$ | | 1 | – | – | V |
| $I_{CCDR}$[14] | Data-retention current (For 3.3-V typical device) | $\overline{CE}_1 \ge V_{CC} - 0.2\text{ V}$ or $CE_2 \le 0.2\text{ V}$ or $(\overline{BHE}$ and $\overline{BLE}) \ge V_{CC} - 0.2\text{ V}$,<br>$V_{IN} \ge V_{CC} - 0.2\text{ V}$ or $V_{IN} \le 0.2\text{ V}$ | $2.2\text{ V} < V_{CC} \le 3.6\text{ V}$ | – | 1.4 | 6.5 | μA |
| | | $\overline{CE}_1 \ge V_{CC} - 0.2\text{ V}$ or $CE_2 \le 0.2\text{ V}$ or $(\overline{BHE}$ and $\overline{BLE}) \ge V_{CC} - 0.2\text{ V}$,<br>$V_{IN} \ge V_{CC} - 0.2\text{ V}$ or $V_{IN} \le 0.2\text{ V}$ | Vcc = 1.5 V | – | 3.2 | 8 | μA |
| | | $\overline{CE}_1 \ge V_{CC} - 0.2\text{ V}$ or $CE_2 \le 0.2\text{ V}$ or $(\overline{BHE}$ and $\overline{BLE}) \ge V_{CC} - 0.2\text{ V}$,<br>$V_{IN} \ge V_{CC} - 0.2\text{ V}$ or $V_{IN} \le 0.2\text{ V}$ | Vcc = 1.2 V | – | 4 | 9 | μA |
| | Data-retention current (For 1.8V Typical device) | $1.2\text{ V} < Vcc \le 2.2\text{ V}$<br>$\overline{CE}_1 \ge V_{CC} - 0.2\text{ V}$ or $CE_2 \le 0.2\text{ V}$ or $(\overline{BHE}$ and $\overline{BLE}) \ge V_{CC} - 0.2\text{ V}$,<br>$V_{IN} \ge V_{CC} - 0.2\text{ V}$ or $V_{IN} \le 0.2\text{ V}$ | | – | 5 | 9 | – |
| $t_{CDR}$[15] | Chip deselect to data-retention time | – | | 0 | – | – | – |
| $t_R$[16] | Operation-recovery time | – | | 45/55 | – | – | ns |

## Data Retention Waveform

Figure 5. Data-Retention Waveform [17]



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**Notes**

13. Indicates the value for the center of distribution at 3.0 V, 25°C and not 100% tested.
14. Chip enables ($\overline{CE}_1$ and $CE_2$) must be tied to CMOS levels to meet the $I_{SB1}/I_{SB2}/I_{CCDR}$ spec. Other inputs can be left floating.
15. Tested initially and after any design or process changes that may affect these parameters.
16. Full device operation requires linear $V_{CC}$ ramp from $V_{DR}$ to $V_{CC(min)} \ge 100\ \mu s$ or stable at $V_{CC(min)} \ge 100\ \mu s$.
17. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Deselect the chip by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

## Switching Characteristics

| Parameter [18] | Description | 55 ns | | 45 ns | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| **Read Cycle** | | | | | | |
| $t_{RC}$ | Read cycle time | 55 | – | 45 | – | ns |
| $t_{AA}$ | Address to data valid | – | 55 | – | 45 | ns |
| $t_{OHA}$ | Data hold from address change | 10 | – | 10 | – | ns |
| $t_{ACE}$ | $\overline{CE}_1$ LOW and $CE_2$ HIGH to data valid / $\overline{CE}$ LOW | – | 55 | – | 45 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to data valid / $\overline{OE}$ LOW | – | 25 | – | 22 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low Z [19] | 5 | – | 5 | – | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High Z [19, 20] | – | 20 | – | 18 | ns |
| $t_{LZCE}$ | $\overline{CE}_1$ LOW and $CE_2$ HIGH to Low Z [19] | 10 | – | 10 | – | ns |
| $t_{HZCE}$ | $\overline{CE}_1$ HIGH and $CE_2$ LOW to High Z [19, 20] | – | 20 | – | 18 | ns |
| $t_{PU}$ | $\overline{CE}_1$ LOW and $CE_2$ HIGH to power-up | 0 | – | 0 | – | ns |
| $t_{PD}$ | $\overline{CE}_1$ HIGH and $CE_2$ LOW to power-down | – | 55 | – | 45 | ns |
| $t_{DBE}$ | BLE / BHE LOW to data valid | – | 55 | – | 45 | ns |
| $t_{LZBE}$ | $\overline{BLE}$ / $\overline{BHE}$ LOW to Low Z [19] | 5 | – | 5 | – | ns |
| $t_{HZBE}$ | $\overline{BLE}$ / $\overline{BHE}$ HIGH to High Z [19, 20] | – | 20 | – | 18 | ns |
| **Write Cycle** [21,22] | | | | | | |
| $t_{WC}$ | Write cycle time | 55 | – | 45 | – | ns |
| $t_{SCE}$ | $\overline{CE}_1$ LOW and $CE_2$ HIGH to write end | 40 | – | 35 | – | ns |
| $t_{AW}$ | Address setup to write end | 40 | – | 35 | – | ns |
| $t_{HA}$ | Address hold from write end | 0 | – | 0 | – | ns |
| $t_{SA}$ | Address setup to write start | 0 | – | 0 | – | ns |
| $t_{PWE}$ | $\overline{WE}$ pulse width | 40 | – | 35 | – | ns |
| $t_{BW}$ | $\overline{BLE}$ / $\overline{BHE}$ LOW to write end | 40 | – | 35 | – | ns |
| $t_{SD}$ | Data setup to write end | 25 | – | 25 | – | ns |
| $t_{HD}$ | Data hold from write end | 0 | – | 0 | – | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High Z [19, 20] | – | 20 | – | 18 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low Z [19] | 10 | – | 10 | – | ns |

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**Notes**

18. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to $V_{CC}$ (for $V_{CC} < 3$ V). Test conditions for the read cycle use output loading shown in AC Test Loads and Waveforms section, unless specified otherwise.
19. At any temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZBE}$ is less than $t_{LZBE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any device.
20. $t_{HZOE}$, $t_{HZCE}$, $t_{HZBE}$, and $t_{HZWE}$ transitions are measured when the outputs enter a high impedance state.
21. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both = $V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write. Any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write
22. The minimum write cycle pulse width for the Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to the sum of $t_{SD}$ and $t_{HZWE}$.

## Switching Waveforms

**Figure 6. Read Cycle No. 1 of CY62157G (Address Transition Controlled) [23, 24]**

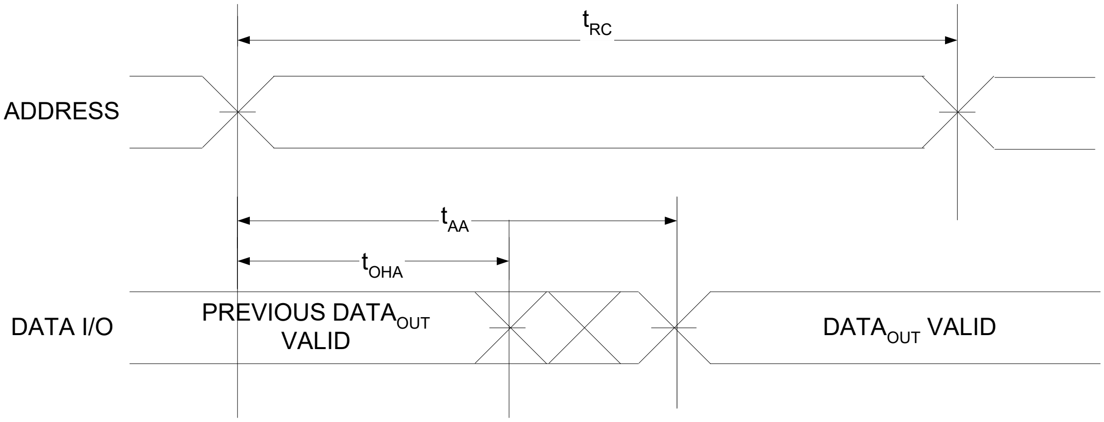
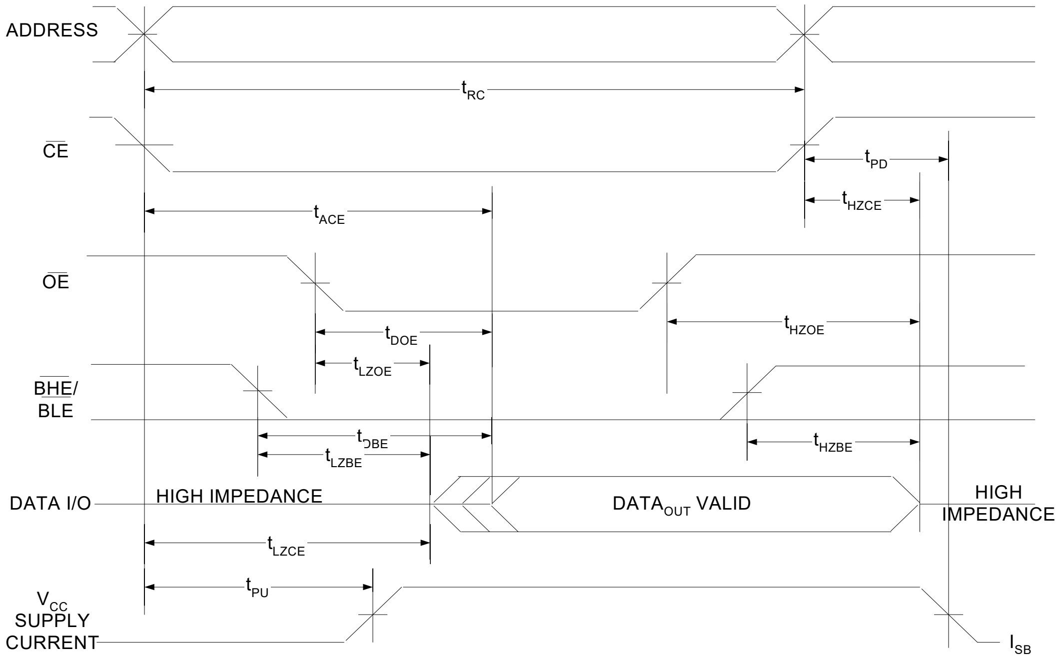


**Figure 7. Read Cycle No. 2 ($\overline{OE}$ Controlled) [24, 25, 26]**



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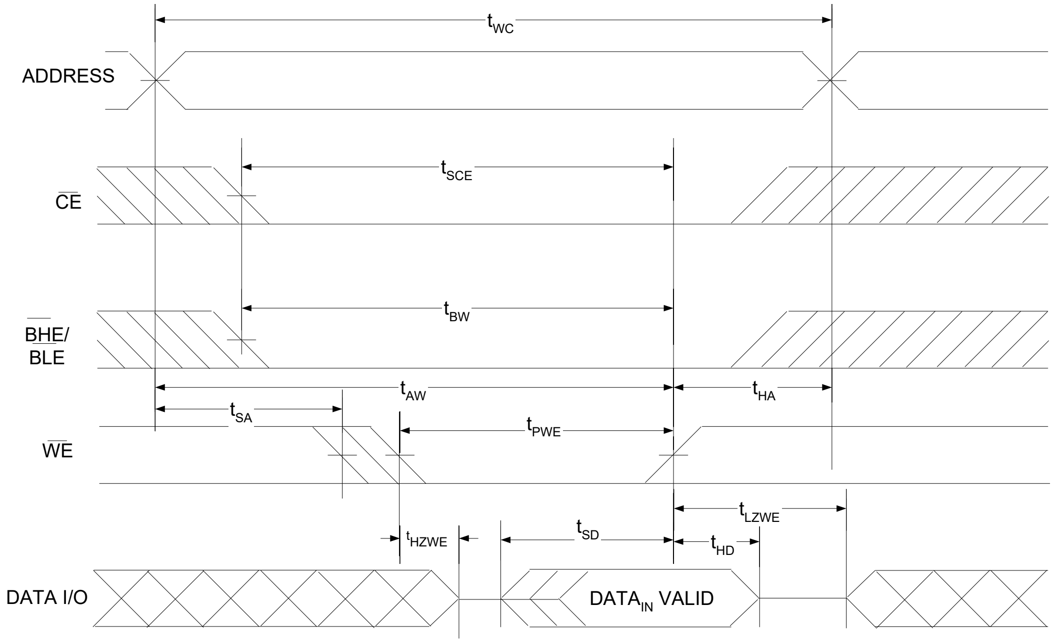
**Notes**

23. The device is continuously selected. $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both = $V_{IL}$.
24. $\overline{WE}$ is HIGH for read cycle.
25. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and $CE_2$. When $\overline{CE}_1$ is LOW and $CE_2$ is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or $CE_2$ is LOW, $\overline{CE}$ is HIGH.
26. Address valid prior to or coincident with $\overline{CE}$ LOW transition.

## Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 ($\overline{WE}$ Controlled) [27, 28, 29]

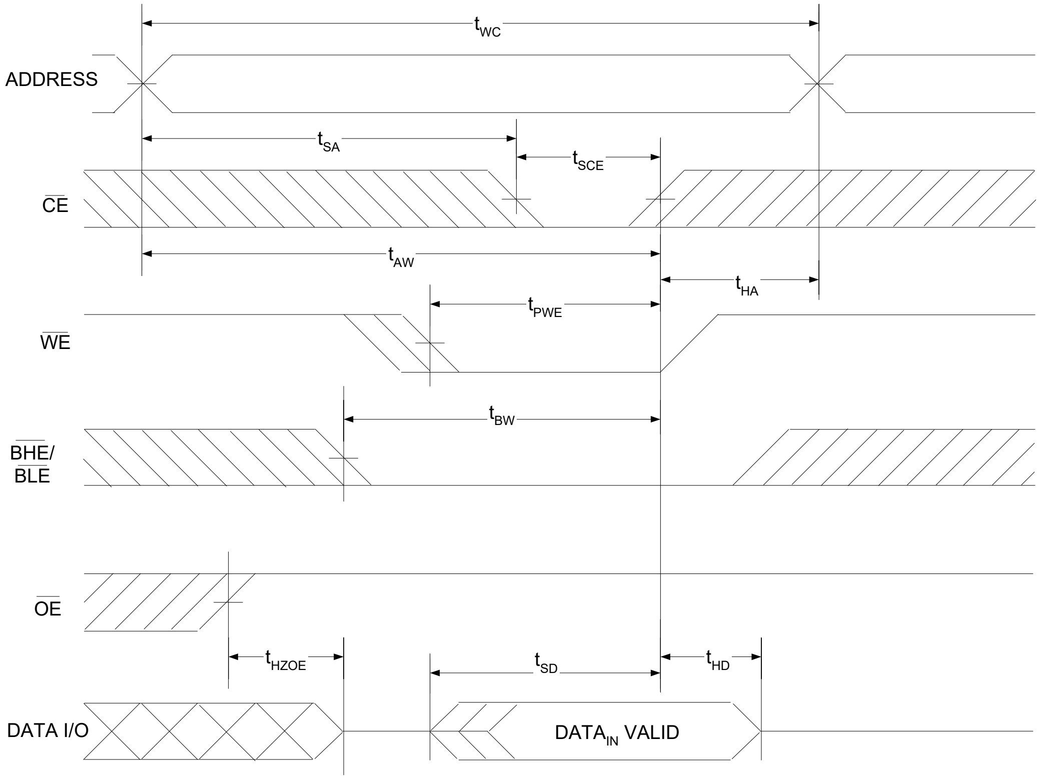


**Notes**

27. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and $CE_2$. When $\overline{CE}_1$ is LOW and $CE_2$ is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or $CE_2$ is LOW, $\overline{CE}$ is HIGH.
28. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both = $V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
29. Data I/O is in HI-Z state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.

## Switching Waveforms (continued)

**Figure 9. Write Cycle No. 2 ($\overline{CE}$ Controlled) [30, 31, 32]**



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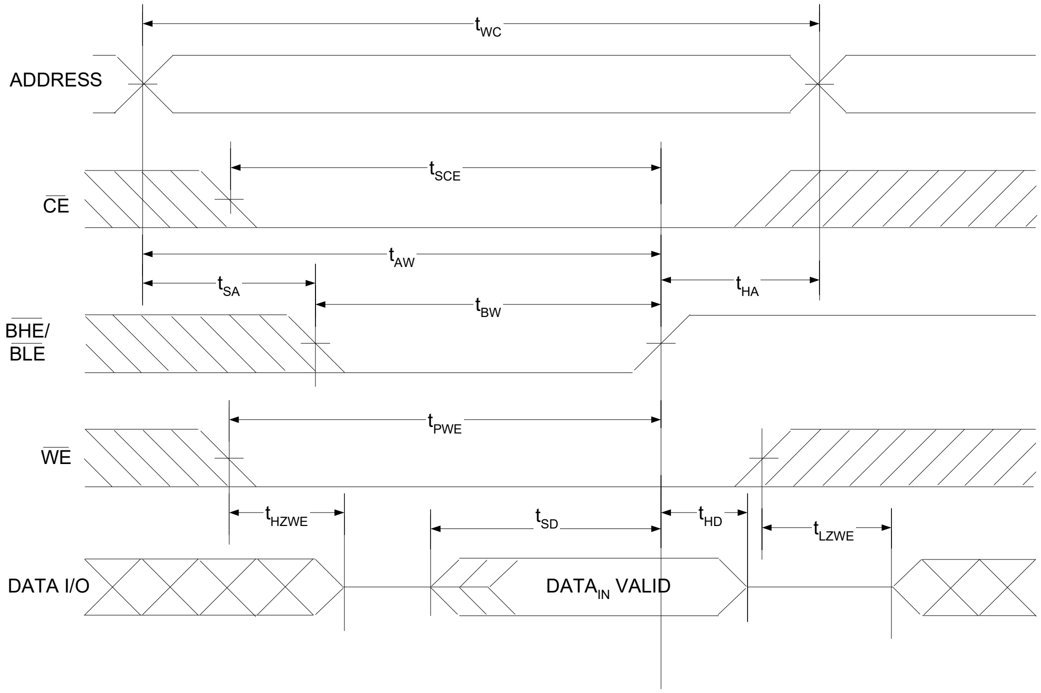
**Notes**

30. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE_1}$ and $CE_2$. When $\overline{CE_1}$ is LOW and $CE_2$ is HIGH, $\overline{CE}$ is LOW; when $\overline{CE_1}$ is HIGH or $CE_2$ is LOW, $\overline{CE}$ is HIGH.
31. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE_1} = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both = $V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
32. Data I/O is in high impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.

## Switching Waveforms (continued)

Figure 10. Write Cycle No. 3 ($\overline{BHE}/\overline{BLE}$ controlled, $\overline{OE}$ LOW) [33, 34, 35]



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**Notes**

33. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and $CE_2$. When $\overline{CE}_1$ is LOW and $CE_2$ is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or $CE_2$ is LOW, $\overline{CE}$ is HIGH.
34. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ or $\overline{BLE}$ or both = $V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
35. Data I/O is in high impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or $\overline{BHE}$, and/or $\overline{BLE} = V_{IH}$.

## Truth Table – CY62157G

| $\overline{CE_1}$ | $CE_2$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{BHE}$ | $\overline{BLE}$ | Inputs/Outputs | Mode | Power |
|---|---|---|---|---|---|---|---|---|
| H | X[36] | X | X | X | X | HI-Z | Deselect/Power-down | Standby ($I_{SB}$) |
| X[36] | L | X | X | X | X | HI-Z | Deselect/Power-down | Standby ($I_{SB}$) |
| X[36] | X[36] | X | X | H | H | HI-Z | Deselect/Power-down | Standby ($I_{SB}$) |
| L | H | H | L | L | L | Data Out ($I/O_0$–$I/O_{15}$) | Read | Active ($I_{CC}$) |
| L | H | H | L | H | L | Data Out ($I/O_0$–$I/O_7$);<br>HI-Z ($I/O_8$–$I/O_{15}$) | Read | Active ($I_{CC}$) |
| L | H | H | L | L | H | HI-Z ($I/O_0$–$I/O_7$);<br>Data Out ($I/O_8$–$I/O_{15}$) | Read | Active ($I_{CC}$) |
| L | H | H | H | X | X | HI-Z | Output disabled | Active ($I_{CC}$) |
| L | H | L | X | L | L | Data In ($I/O_0$–$I/O_{15}$) | Write | Active ($I_{CC}$) |
| L | H | L | X | H | L | Data In ($I/O_0$–$I/O_7$);<br>HI-Z ($I/O_8$–$I/O_{15}$) | Write | Active ($I_{CC}$) |
| L | H | L | X | L | H | HI-Z ($I/O_0$–$I/O_7$);<br>Data In ($I/O_8$–$I/O_{15}$) | Write | Active ($I_{CC}$) |

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**Note**

[36] The ‘X’ (Don’t care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

## Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|---|---|---|---|---|
| 45 | CY62157G30-45ZSXA | 51-85087 | 44-pin TSOP II (Pb-free) | Automotive-A |
| | CY62157G30-45BVXA | 51-85150 | 48-ball VFBGA (6 × 8 × 1.0 mm) (Pb-free) | Automotive-A |
| | CY62157G30-45ZXA | 51-85183 | 48-pin TSOP I (Pb-free) | Automotive-A |

### Ordering Code Definitions

CY 621 5 7 H XX - XX XX X X

Temperature Grade: X = E or A
E = Automotive-E; A = Automotive-A

Pb-free

Package Type: XX = ZS or BV or Z
ZS = 44-pin TSOP II; BV = 48-ball VFBGA; Z = 48-pin TSOP I

Speed Grade: XX = 55 or 45
55 = 55 ns; 45 = 45 ns

Voltage Range: 30 = 3 V typ

Process Technology: G = 65 nm

Bus width: 7 = × 16

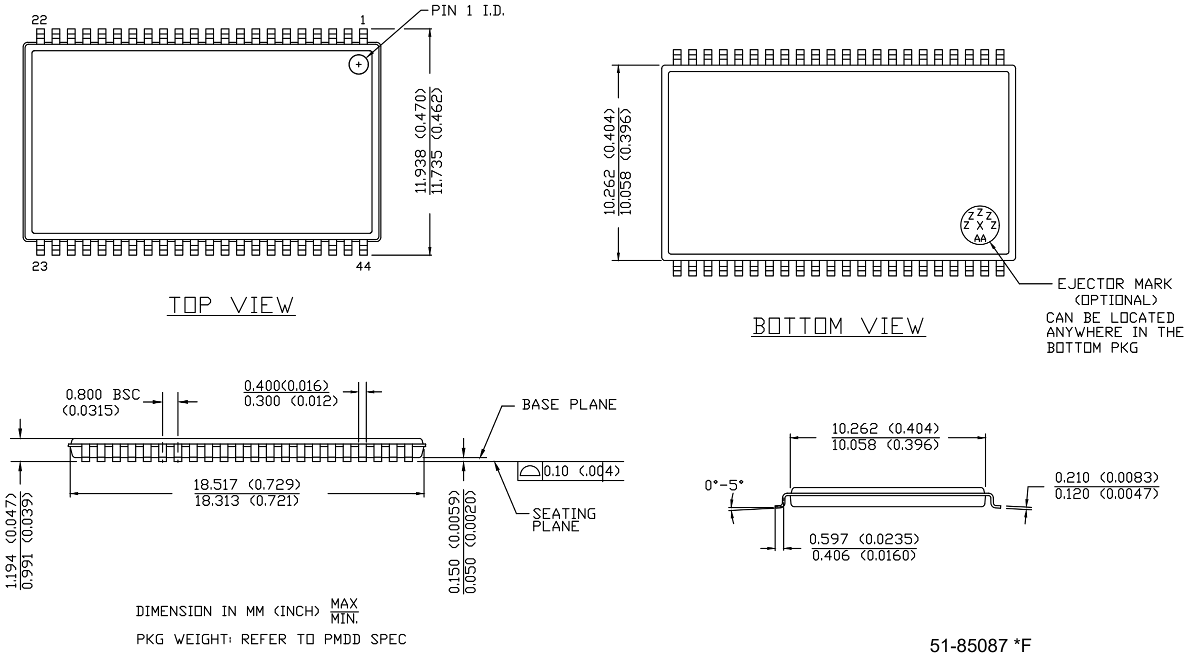
Density: 5 = 8-Mbit

Family Code: 621 = MoBL SRAM family

Company ID: CY = Cypress

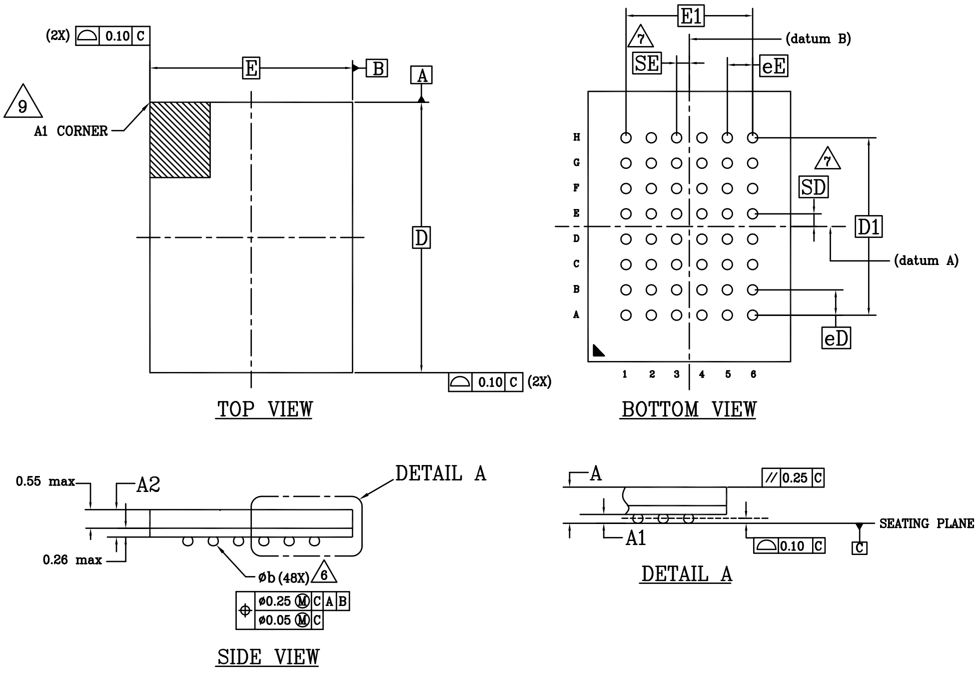
## Package Diagrams

**Figure 11. 44-pin TSOP II Package Outline, 51-85087**



## Package Diagrams (continued)

**Figure 12. 48-ball VFBGA (6 × 8 × 1.0 mm) Package Outline, 51-85150**



| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | - | - | 1.00 |
| A1 | 0.16 | - | - |
| A2 | - | - | 0.81 |
| D | | 8.00 BSC | |
| E | | 6.00 BSC | |
| D1 | | 5.25 BSC | |
| E1 | | 3.75 BSC | |
| MD | | 8 | |
| ME | | 6 | |
| n | | 48 | |
| Ø b | 0.25 | 0.30 | 0.35 |
| eE | | 0.75 BSC | |
| eD | | 0.75 BSC | |
| SD | | 0.375 BSC | |
| SE | | 0.375 BSC | |

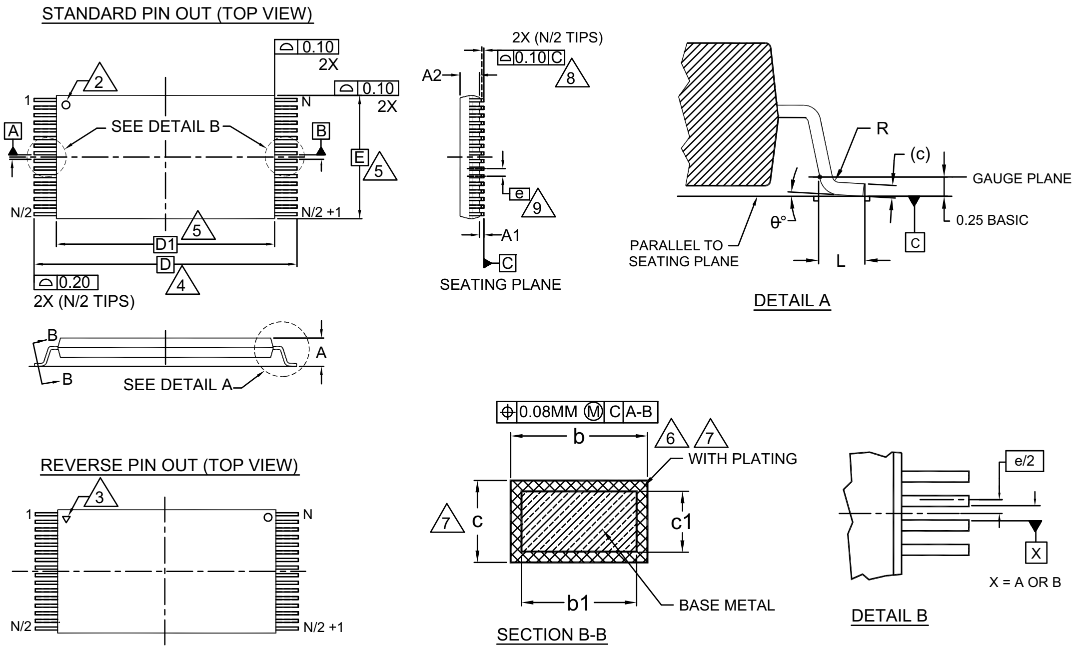
NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.

51-85150 *I

## Package Diagrams (continued)

**Figure 13. 48-pin TSOP I (18.4 × 12 × 1.2 mm) Package Outline, 51-85183**



| SYMBOL | DIMENSIONS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.20 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| b1 | 0.17 | 0.20 | 0.23 |
| b | 0.17 | 0.22 | 0.27 |
| c1 | 0.10 | — | 0.16 |
| c | 0.10 | — | 0.21 |
| D | 20.00 BASIC | | |
| D1 | 18.40 BASIC | | |
| E | 12.00 BASIC | | |
| e | 0.50 BASIC | | |
| L | 0.50 | 0.60 | 0.70 |
| θ | 0° | — | 8 |
| R | 0.08 | — | 0.20 |
| N | 48 | | |

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS (mm).
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C- . THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm .
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
10. JEDEC SPECIFICATION NO. REF: MO-142(D)DD.

51-85183 *F

## Acronyms

**Table 1. Acronyms Used in this Document**

| Acronym | Description |
|---|---|
| $\overline{\text{BHE}}$ | byte high enable |
| $\overline{\text{BLE}}$ | byte low enable |
| $\overline{\text{CE}}$ | chip enable |
| CMOS | complementary metal oxide semiconductor |
| I/O | input/output |
| $\overline{\text{OE}}$ | output enable |
| SRAM | static random access memory |
| TTL | Transistor-transistor logic |
| VFBGA | very fine-pitch ball grid array |
| $\overline{\text{WE}}$ | write enable |

## Document Conventions

### Units of Measure

**Table 2. Units of Measure**

| Symbol | Unit of Measure |
|---|---|
| °C | degree Celsius |
| MHz | megahertz |
| µA | microamperes |
| µs | microseconds |
| mA | milliamperes |
| mm | millimeters |
| ns | nanoseconds |
| Ω | ohms |
| % | percent |
| pF | picofarads |
| V | volts |
| W | watts |

## Document History Page

| Document Title: CY62157G Automotive, 8-Mbit (512K words × 16-bit) Static RAM with Error-Correcting Code (ECC)<br>Document Number: 002-27989 | | | |
|---|---|---|---|
| **Rev.** | **ECN No.** | **Submission Date** | **Description of Change** |
| *D | 6937006 | 09/09/2020 | Changed datasheet status to Final. |