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8-Mbit (512K words × 16-bit) Static RAM with Error-Correcting Code (ECC)

Features

- Ultra-low standby current
 - Typical standby current: 5.5 μ A
 - Maximum standby current: 16 μ A
- High speed: 45 ns
- Voltage range: 2.2 V to 3.6 V
- Embedded Error-Correcting Code (ECC) for single-bit error correction
- 1.0 V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Available in Pb-free 48-ball VFBGA and 48-pin TSOP I packages

Functional Description

CY62157H is a high-performance CMOS low-power (MoBL) SRAM device with Embedded Error-Correcting Code. ECC logic can detect and correct single bit error in accessed location.

This device is offered in dual chip enable option. Dual chip enable devices are accessed by asserting both chip enable inputs – \overline{CE}_1 as LOW and CE_2 as HIGH.

Data writes are performed by asserting the Write Enable input (\overline{WE} LOW), and providing the data and address on device data (I/O_0 through I/O_{15}) and address (A_0 through A_{18}) pins respectively. The Byte High/Low Enable (\overline{BHE} , \overline{BLE}) inputs control byte writes, and write data on the corresponding I/O lines to the memory location specified. \overline{BHE} controls I/O_8 through I/O_{15} and \overline{BLE} controls I/O_0 through I/O_7 .

Data reads are performed by asserting the Output Enable (\overline{OE}) input and providing the required address on the address lines. Read data is accessible on I/O lines (I/O_0 through I/O_{15}). Byte accesses can be performed by asserting the required byte enable signal (\overline{BHE} , \overline{BLE}) to read either the upper byte or the lower byte of data from the specified address location.

All I/O s (I/O_0 through I/O_{15}) are placed in a high impedance state when the device is deselected (CE_1 HIGH / CE_2 LOW for dual chip enable device), or control signals are de-asserted (\overline{OE} , \overline{BLE} , \overline{BHE}).

These devices also have a unique “Byte Power down” feature, where, if both the Byte Enables (\overline{BHE} and \overline{BLE}) are disabled, the devices seamlessly switch to standby mode irrespective of the state of the chip enable(s), thereby saving power.

The CY62157H device is available in a Pb-free 48-ball VFBGA and 48-pin TSOP I packages. The logic block diagram is on page 2.

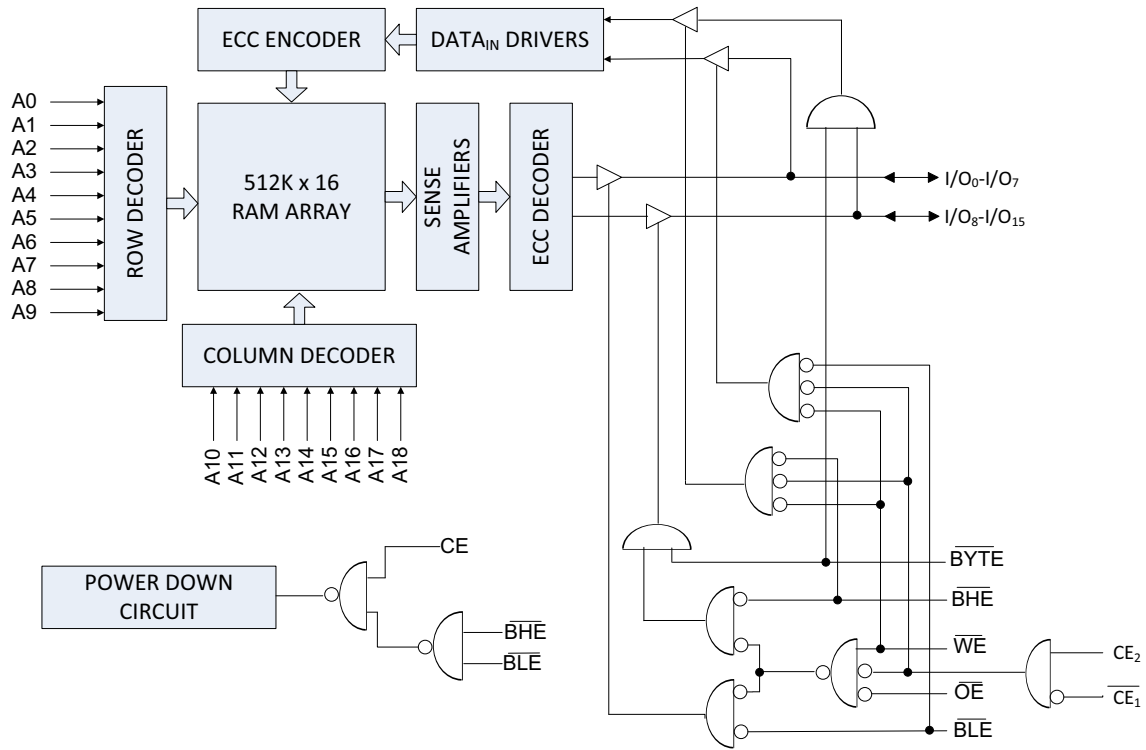
Product Portfolio

| Product | Features and Options (see the Pin Configurations section) | Range | V_{CC} Range (V) | Speed (ns) | Power Dissipation | | | |
|------------|---|------------|--------------------|------------|-------------------------|-----|-------------------------------|-----|
| | | | | | Operating I_{CC} (mA) | | Standby, I_{SB2} (μ A) | |
| | | | | | $f = f_{max}$ | | | |
| | | | | | Typ ^[1] | Max | Typ ^[1] | Max |
| CY62157H30 | Dual Chip Enable | Industrial | 2.2 V–3.6 V | 45 | 29 | 36 | 5.5 | 16 |

Note

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = 3$ V (for V_{CC} range of 2.2 V–3.6 V), $T_A = 25$ °C.

Logic Block Diagram



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Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

| | |
|--|-----------------------------------|
| Storage temperature | -65 °C to + 150 °C |
| Ambient temperature with power applied | -55 °C to + 125 °C |
| Supply voltage to ground potential | -0.2 V to V _{CC} + 0.3 V |
| DC voltage applied to outputs in High Z state ^[4] | -0.2 V to V _{CC} + 0.3 V |

| | |
|---|-----------------------------------|
| DC input voltage ^[4] | -0.2 V to V _{CC} + 0.3 V |
| Output current into outputs (LOW) | 20 mA |
| Static discharge voltage (MIL-STD-883, Method 3015) | >2001 V |
| Latch-up current | >140 mA |

Operating Range

| Grade | Ambient Temperature | V _{CC} |
|------------|---------------------|-----------------|
| Industrial | -40 °C to +85 °C | 2.2 V to 3.6 V |

DC Electrical Characteristics

Over the Operating Range of -40 °C to 85 °C

| Parameter | Description | | Test Conditions | 45 ns | | | Unit | |
|---------------------------------|--|----------------|--|----------------------|--------------------|-----------------------|------|----|
| | | | | Min | Typ ^[5] | Max | | |
| V _{OH} | Output HIGH voltage | 2.2 V to 2.7 V | V _{CC} = Min, I _{OH} = -0.1 mA | 2 | - | - | V | |
| | | 2.7 V to 3.6 V | V _{CC} = Min, I _{OH} = -1.0 mA | 2.4 | - | - | | |
| V _{OL} | Output LOW voltage | 2.2 V to 2.7 V | V _{CC} = Min, I _{OL} = 0.1 mA | - | - | 0.4 | V | |
| | | 2.7 V to 3.6 V | V _{CC} = Min, I _{OL} = 2.1 mA | - | - | 0.4 | | |
| V _{IH} | Input HIGH voltage | 2.2 V to 2.7 V | - | 1.8 | - | V _{CC} + 0.3 | V | |
| | | 2.7 V to 3.6 V | - | 2 | - | V _{CC} + 0.3 | | |
| V _{IL} | Input LOW voltage ^[4] | 2.2 V to 2.7 V | - | -0.3 | - | 0.6 | V | |
| | | 2.7 V to 3.6 V | - | -0.3 | - | 0.8 | | |
| I _{IX} | Input leakage current | | GND ≤ V _{IN} ≤ V _{CC} | -1 | - | +1 | μA | |
| I _{OZ} | Output leakage current | | GND ≤ V _{OUT} ≤ V _{CC} , Output disabled | -1 | - | +1 | μA | |
| I _{CC} | V _{CC} operating supply current | | V _{CC} = Max, I _{OUT} = 0 mA, CMOS levels | f = f _{MAX} | - | 29.0 | 36.0 | mA |
| | | | | f = 1 MHz | - | 7.0 | 9.0 | mA |
| I _{SB1} ^[6] | Automatic power down current – CMOS inputs; V _{CC} = 2.2 to 3.6 V | | $\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$, $(\overline{BHE}$ and $\overline{BLE}) \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \leq 0.2 \text{ V}$, $f = f_{max}$ (address and data only), $f = 0$ (\overline{OE} , and \overline{WE}), $V_{CC} = V_{CC(max)}$ | - | 5.5 | 16.0 | μA | |
| I _{SB2} ^[6] | Automatic power down current – CMOS inputs V _{CC} = 2.2 to 3.6 V | | $\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$, $(\overline{BHE}$ and $\overline{BLE}) \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$, $f = 0$, $V_{CC} = V_{CC(max)}$ | 25 °C ^[7] | - | 5.5 | 6.5 | μA |
| | | | | 40 °C ^[7] | - | 6.3 | 8.0 | |
| | | | | 85 °C | - | 12.0 ^[7] | 16.0 | |

Notes

- V_{IL(min)} = -2.0 V and V_{IH(max)} = V_{CC} + 2 V for pulse durations of less than 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), T_A = 25 °C.
- Chip enables (CE₁ and CE₂) must be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
- The I_{SB2} limits at 25 °C, 70 °C, 40 °C and typical limit at 85 °C are guaranteed by design and not 100% tested.

Capacitance

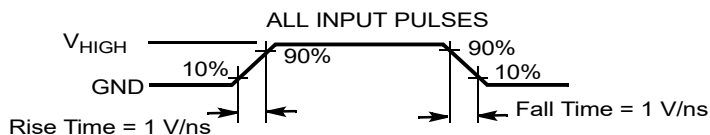
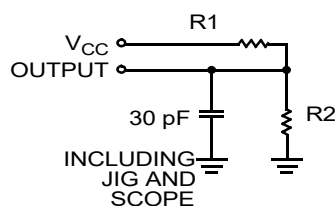
| Parameter [8] | Description | Test Conditions | Max | Unit |
|------------------|--------------------|---|-----|------|
| C _{IN} | Input capacitance | T _A = 25 °C, f = 1 MHz, V _{CC} = V _{CC(typ)} | 10 | pF |
| C _{OUT} | Output capacitance | | 10 | pF |

Thermal Resistance

| Parameter [8] | Description | Test Conditions | 48-pin TSOP I | 48-ball VFBGA | Unit |
|-----------------|--|--|---------------|---------------|------|
| θ _{JA} | Thermal resistance (junction to ambient) | Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board | 57.99 | 31.50 | °C/W |
| θ _{JC} | Thermal resistance (junction to case) | | 13.42 | 15.75 | °C/W |

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



| Parameters | 2.5 V | 3.0 V | Unit |
|-----------------|-------|-------|------|
| R1 | 16667 | 1103 | Ω |
| R2 | 15385 | 1554 | Ω |
| R _{TH} | 8000 | 645 | Ω |
| V _{TH} | 1.20 | 1.75 | V |

Note

8. Tested initially and after any design or process changes that may affect these parameters.

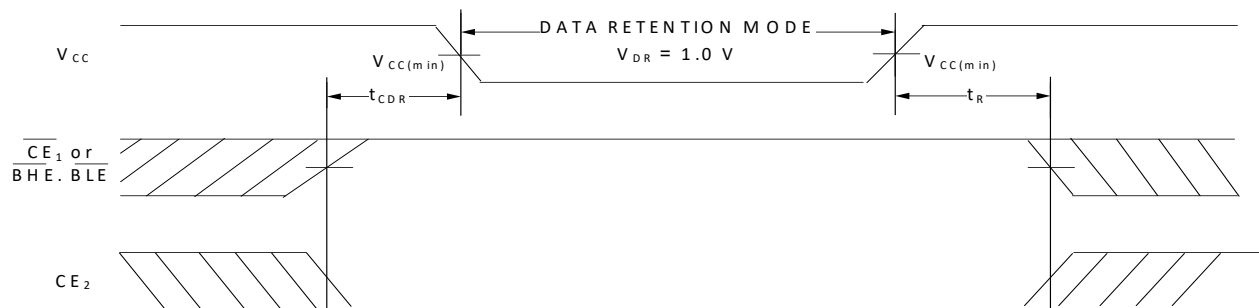
Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | Min | Typ ^[9] | Max | Unit |
|--------------------------------|--------------------------------------|--|-----|--------------------|------|---------------|
| V_{DR} | V_{CC} for data retention | | 1 | – | – | V |
| I_{CCDR} ^[10, 11] | Data retention current | $2.2\text{ V} < V_{CC} \leq 3.6\text{ V}$, $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$, $(\overline{BHE}$ and $\overline{BLE}) \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ | – | 5.5 | 16.0 | μA |
| t_{CDR} ^[12] | Chip deselect to data retention time | | 0 | – | – | – |
| t_R ^[13] | Operation recovery time | | 45 | – | – | ns |

Data Retention Waveform

Figure 4. Data Retention Waveform^[14]



Notes

9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = 3\text{ V}$ (for V_{CC} range of 2.2 V–3.6 V), $T_A = 25\text{ }^\circ\text{C}$.
10. Chip enables (\overline{CE}_1 and CE_2) must be tied to CMOS levels to meet the $I_{SB1} / I_{SB2} / I_{CCDR}$ spec. Other inputs can be left floating.
11. I_{CCDR} is guaranteed only after the device is first powered up to $V_{CC(\text{min})}$ and then brought down to V_{DR} .
12. Tested initially and after any design or process changes that may affect these parameters.
13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(\text{min})} \geq 100\text{ }\mu\text{s}$.
14. $\overline{BHE.BLE}$ is the AND of both \overline{BHE} and \overline{BLE} . Deselect the chip by either disabling the chip enable signals or by disabling both \overline{BHE} and \overline{BLE} .

Switching Characteristics

| Parameter ^[15] | Description | 45 ns | | Unit |
|--|--|-------|-----|------|
| | | Min | Max | |
| Read Cycle | | | | |
| t_{RC} | Read cycle time | 45 | – | ns |
| t_{AA} | Address to data valid | – | 45 | ns |
| t_{OHA} | Data hold from address change | 10 | – | ns |
| t_{ACE} | \overline{CE}_1 LOW and CE_2 HIGH to data valid | – | 45 | ns |
| t_{DOE} | \overline{OE} LOW to data valid | – | 22 | ns |
| t_{LZOE} | \overline{OE} LOW to Low-Z ^[16] | 5 | – | ns |
| t_{HZOE} | \overline{OE} HIGH to High-Z ^[16, 17] | – | 18 | ns |
| t_{LZCE} | \overline{CE}_1 LOW and CE_2 HIGH to Low-Z ^[16] | 10 | – | ns |
| t_{HZCE} | \overline{CE}_1 HIGH and CE_2 LOW to High-Z ^[16, 17] | – | 18 | ns |
| t_{PU} | \overline{CE}_1 LOW and CE_2 HIGH to power-up | 0 | – | ns |
| t_{PD} | \overline{CE}_1 HIGH and CE_2 LOW to power-down | – | 45 | ns |
| t_{DBE} | \overline{BLE} / \overline{BHE} LOW to data valid | – | 45 | ns |
| t_{LZBE} | \overline{BLE} / \overline{BHE} LOW to Low-Z ^[16] | 5 | – | ns |
| t_{HZBE} | \overline{BLE} / \overline{BHE} HIGH to High-Z ^[16, 17] | – | 18 | ns |
| Write Cycle ^[18, 19] | | | | |
| t_{WC} | Write cycle time | 45 | – | ns |
| t_{SCE} | \overline{CE}_1 LOW and CE_2 HIGH to write end | 35 | – | ns |
| t_{AW} | Address setup to write end | 35 | – | ns |
| t_{HA} | Address hold from write end | 0 | – | ns |
| t_{SA} | Address setup to write start | 0 | – | ns |
| t_{PWE} | \overline{WE} pulse width | 35 | – | ns |
| t_{BW} | \overline{BLE} / \overline{BHE} LOW to write end | 35 | – | ns |
| t_{SD} | Data setup to write end | 25 | – | ns |
| t_{HD} | Data hold from write end | 0 | – | ns |
| t_{HZWE} | \overline{WE} LOW to High-Z ^[16, 17] | – | 18 | ns |
| t_{LZWE} | \overline{WE} HIGH to Low-Z ^[16] | 10 | – | ns |

Notes

15. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$ V). Test conditions for the read cycle use output loading shown in AC Test Loads and Waveforms section, unless specified otherwise.
16. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
17. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
18. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, \overline{BHE} or \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
19. The minimum write cycle pulse width for Write Cycle No. 1 (\overline{WE} Controlled, \overline{OE} LOW) should be equal to the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 5. Read Cycle No. 1 of CY62157H (Address Transition Controlled) [20, 21]

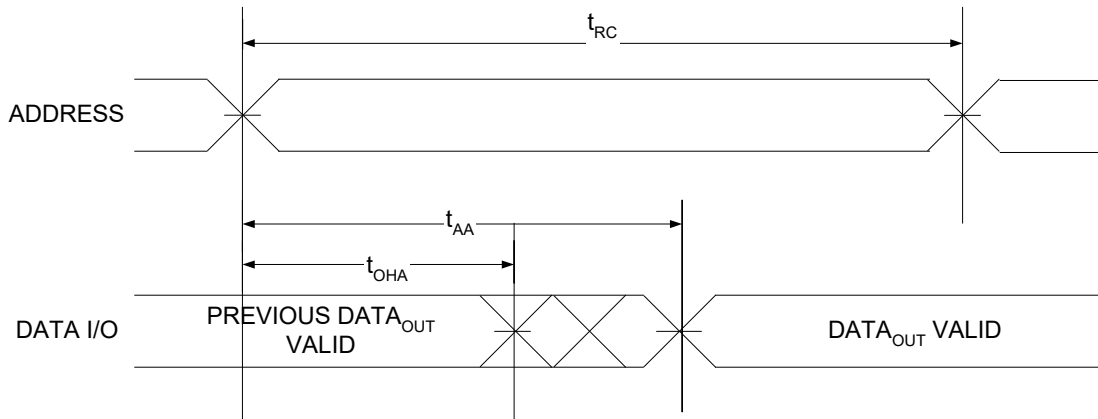
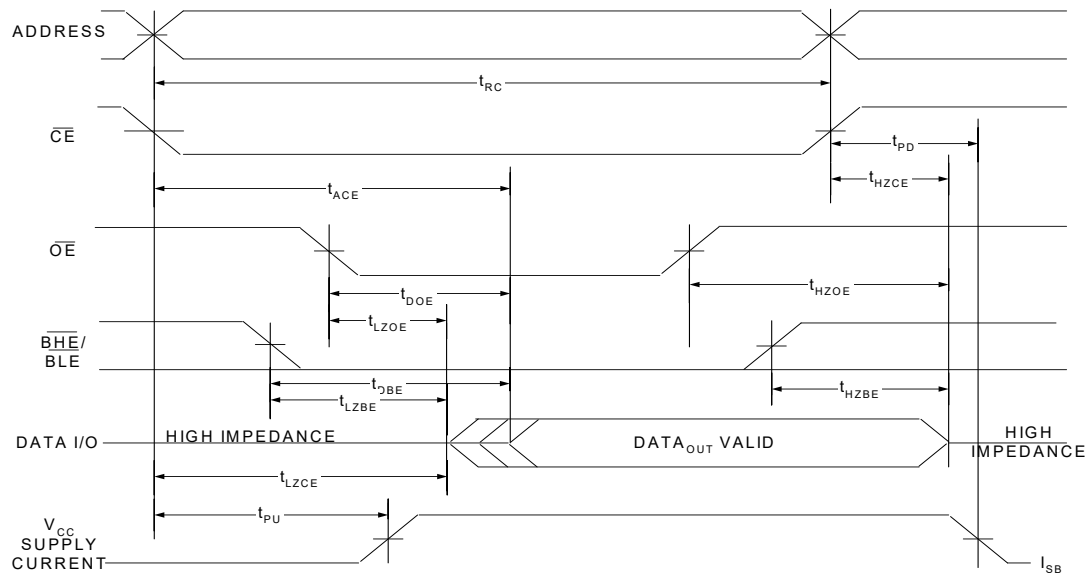


Figure 6. Read Cycle No. 2 (\overline{OE} Controlled) [21, 22, 23]

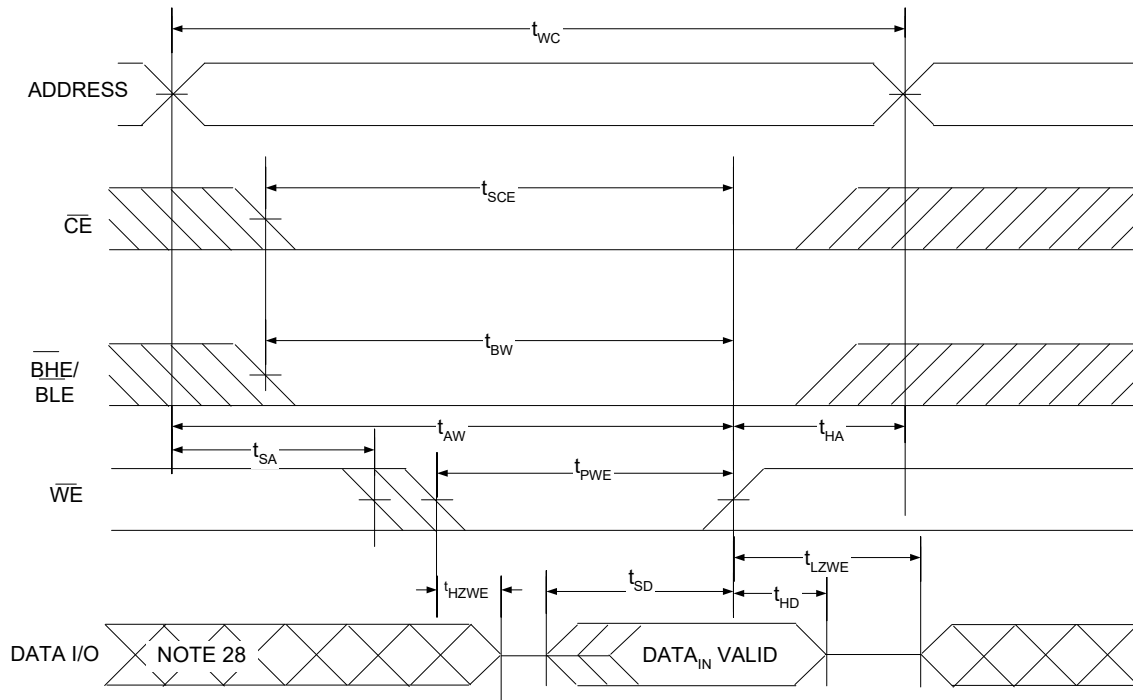


Notes

- 20. The device is continuously selected. $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$, \overline{BHE} or \overline{BLE} or both = V_{IL} .
- 21. \overline{WE} is HIGH for read cycle.
- 22. For all dual chip enable devices, \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.
- 23. Address valid prior to or coincident with \overline{CE} LOW transition.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 1 (\overline{WE} Controlled, \overline{OE} LOW) [24, 25, 26, 27]

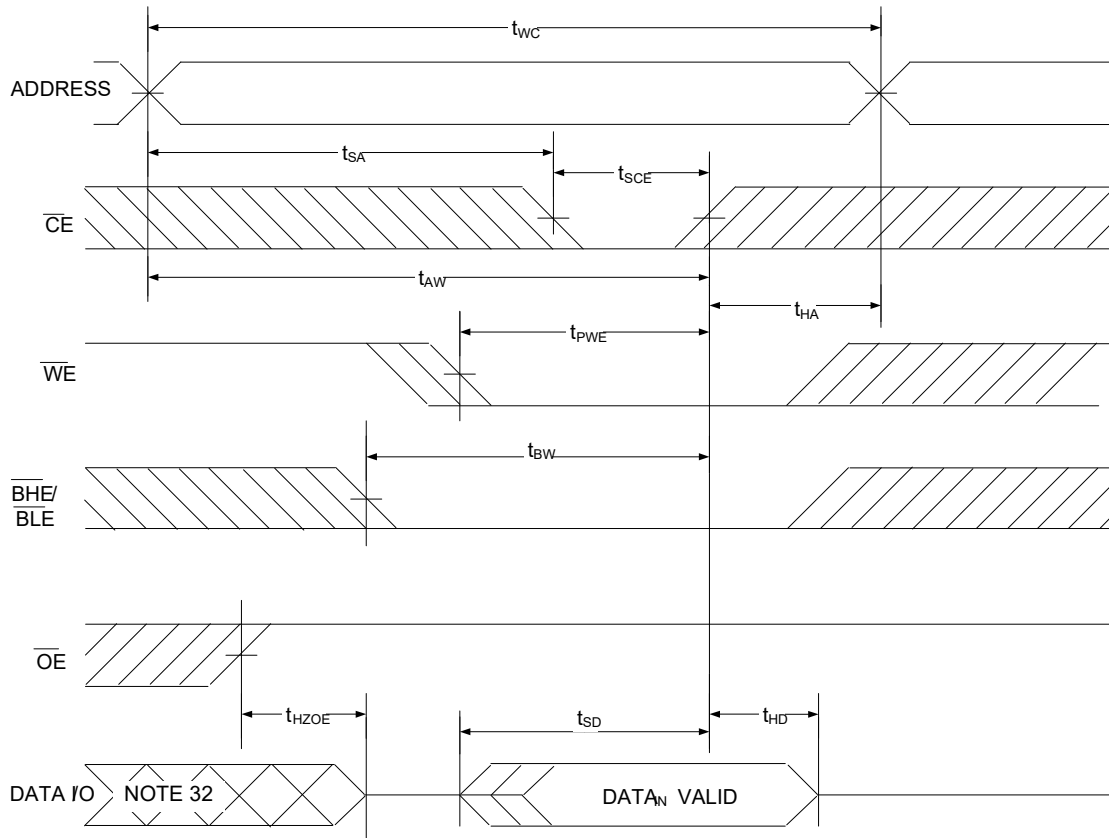


Notes

24. For all dual chip enable devices, \overline{CE} is the logical combination of \overline{CE}_1 and CE_2 . When \overline{CE}_1 is LOW and CE_2 is HIGH, \overline{CE} is LOW; when \overline{CE}_1 is HIGH or CE_2 is LOW, \overline{CE} is HIGH.
25. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, \overline{BHE} or \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
26. Data I/O is in high impedance state if $\overline{CE} = V_{IH}$, or $\overline{OE} = V_{IH}$ or \overline{BHE} , and/or $\overline{BLE} = V_{IH}$.
27. The minimum write cycle pulse width for Write Cycle No. 1 (\overline{WE} Controlled, \overline{OE} LOW) should be equal to the sum of t_{HZWE} and t_{SD} .
28. During this period the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled) [29, 30, 31]



Notes

29. For all dual chip enable devices, $\overline{\text{CE}}$ is the logical combination of $\overline{\text{CE}}_1$ and CE_2 . When $\overline{\text{CE}}_1$ is LOW and CE_2 is HIGH, $\overline{\text{CE}}$ is LOW; when $\overline{\text{CE}}_1$ is HIGH or CE_2 is LOW, $\overline{\text{CE}}$ is HIGH.

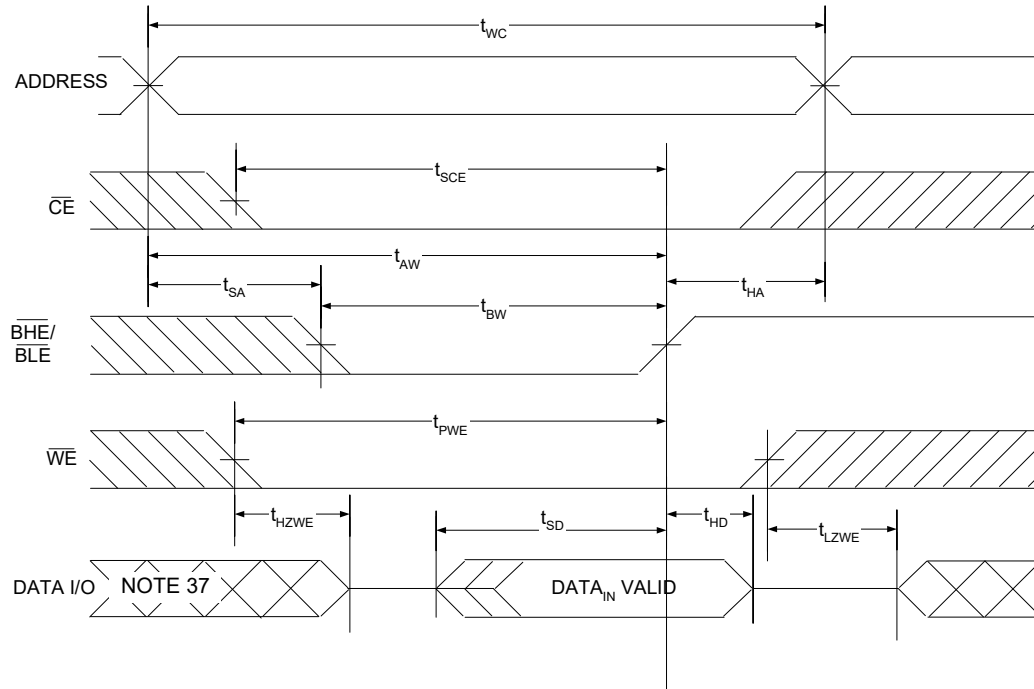
30. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{\text{IL}}$, $\overline{\text{CE}}_1 = V_{\text{IL}}$, $\overline{\text{BHE}}$ or $\overline{\text{BLE}}$ or both = V_{IL} , and $\text{CE}_2 = V_{\text{IH}}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

31. Data I/O is in high impedance state if $\overline{\text{CE}} = V_{\text{IH}}$, or $\overline{\text{OE}} = V_{\text{IH}}$ or $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}} = V_{\text{IH}}$.

32. During this period the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 3 ($\overline{\text{BHE}}/\overline{\text{BLE}}$ controlled, $\overline{\text{OE}}$ LOW) [33, 34, 35, 36]

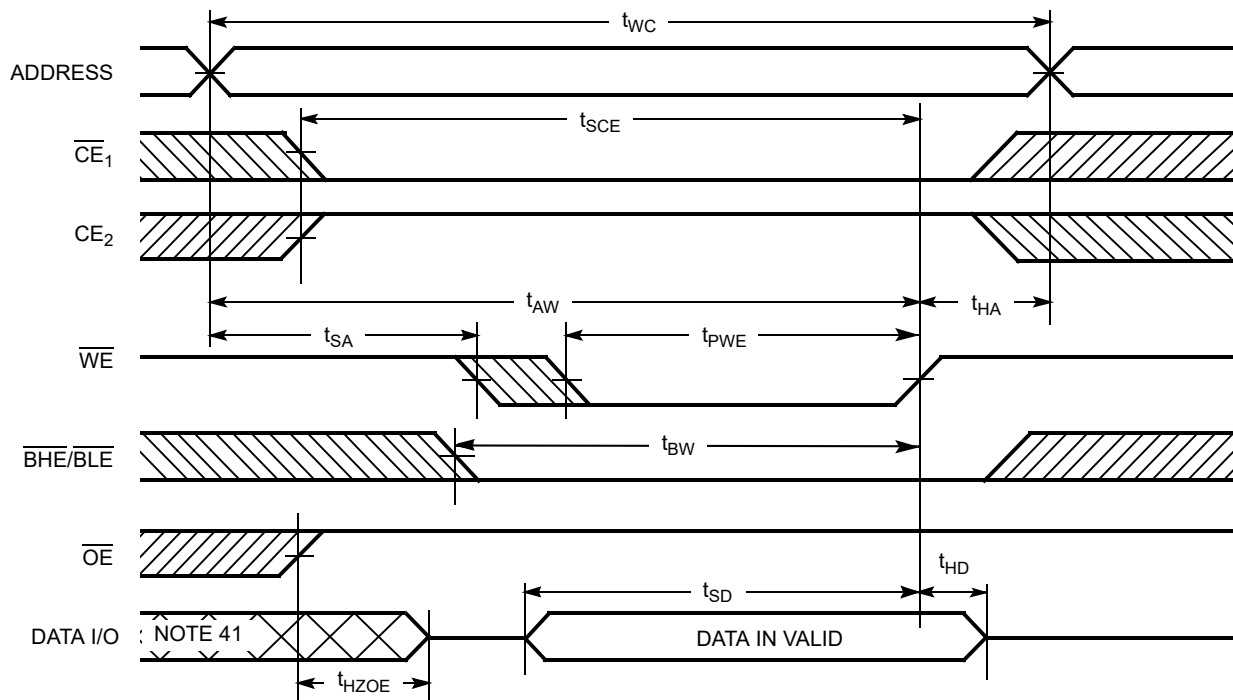


Notes

- 33. For all dual chip enable devices, $\overline{\text{CE}}$ is the logical combination of $\overline{\text{CE}}_1$ and CE_2 . When $\overline{\text{CE}}_1$ is LOW and CE_2 is HIGH, $\overline{\text{CE}}$ is LOW; when $\overline{\text{CE}}_1$ is HIGH or CE_2 is LOW, $\overline{\text{CE}}$ is HIGH.
- 34. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{IL}$, $\overline{\text{CE}}_1 = V_{IL}$, $\overline{\text{BHE}}$ or $\overline{\text{BLE}}$ or both = V_{IL} , and $\text{CE}_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
- 35. Data I/O is in high impedance state if $\overline{\text{CE}} = V_{IH}$, or $\overline{\text{OE}} = V_{IH}$ or $\overline{\text{BHE}}$, and/or $\overline{\text{BLE}} = V_{IH}$.
- 36. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{\text{BHE}}/\overline{\text{BLE}}$ Controlled, $\overline{\text{OE}}$ LOW) should be equal to the sum of t_{HZWE} and t_{SD} .
- 37. During this period the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 10. Write Cycle No. 4 (\overline{WE} Controlled) [38, 39, 40]



Notes

- 38. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} or \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
- 39. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 40. If \overline{CE}_1 goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 41. During this period the I/Os are in output state. Do not apply input signals.

Truth Table – CY62157H

| \overline{CE}_1 | CE_2 | \overline{WE} | \overline{OE} | \overline{BHE} | \overline{BLE} | Inputs/Outputs | Mode | Power |
|-------------------|-------------------|-----------------|-----------------|------------------|------------------|--|---------------------|----------------------|
| H | X ^[42] | X | X | X | X | High-Z | Deselect/Power-down | Standby (I_{SB}) |
| X ^[42] | L | X | X | X | X | High-Z | Deselect/Power-down | Standby (I_{SB}) |
| X ^[42] | X ^[42] | X | X | H | H | High-Z | Deselect/Power-down | Standby (I_{SB}) |
| L | H | H | L | L | L | Data Out (I/O_0 – I/O_{15}) | Read | Active (I_{CC}) |
| L | H | H | L | H | L | Data Out (I/O_0 – I/O_7); High-Z (I/O_8 – I/O_{15}) | Read | Active (I_{CC}) |
| L | H | H | L | L | H | High Z (I/O_0 – I/O_7); Data Out (I/O_8 – I/O_{15}) | Read | Active (I_{CC}) |
| L | H | L | X | L | L | Data In (I/O_0 – I/O_{15}) | Write | Active (I_{CC}) |
| L | H | L | X | H | L | Data In (I/O_0 – I/O_7); High-Z (I/O_8 – I/O_{15}) | Write | Active (I_{CC}) |
| L | H | L | X | L | H | High-Z (I/O_0 – I/O_7); Data In (I/O_8 – I/O_{15}) | Write | Active (I_{CC}) |
| L | H | H | L | X | X | Data Out (I/O_0 – I/O_7) | Read | Active (I_{CC}) |
| L | H | H | H | X | X | High-Z | Output disabled | Active (I_{CC}) |
| L | H | L | X | X | X | Data In (I/O_0 – I/O_7) | Write | Active (I_{CC}) |

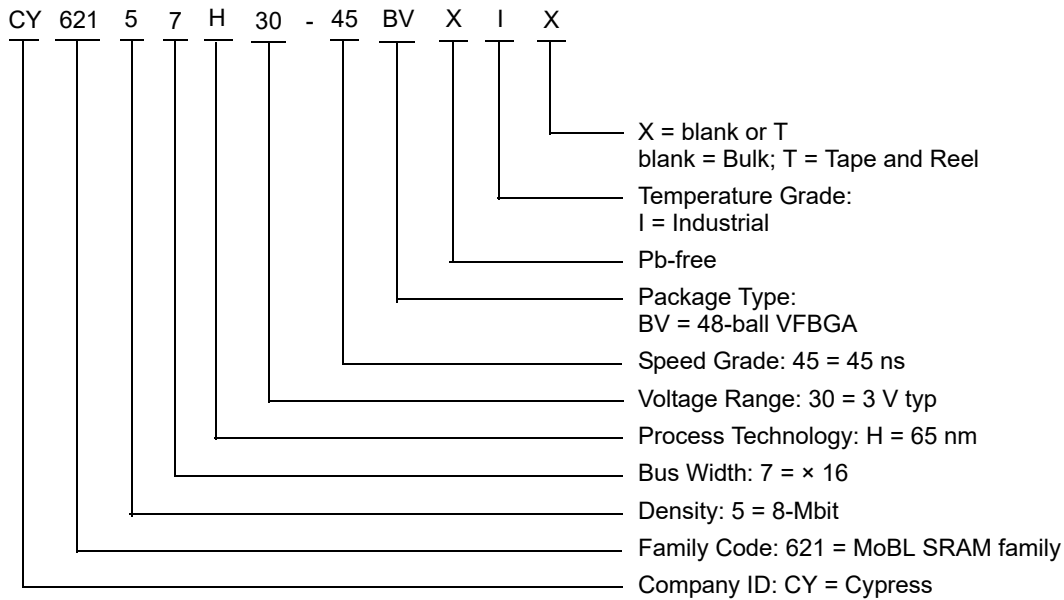
Note

42. The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

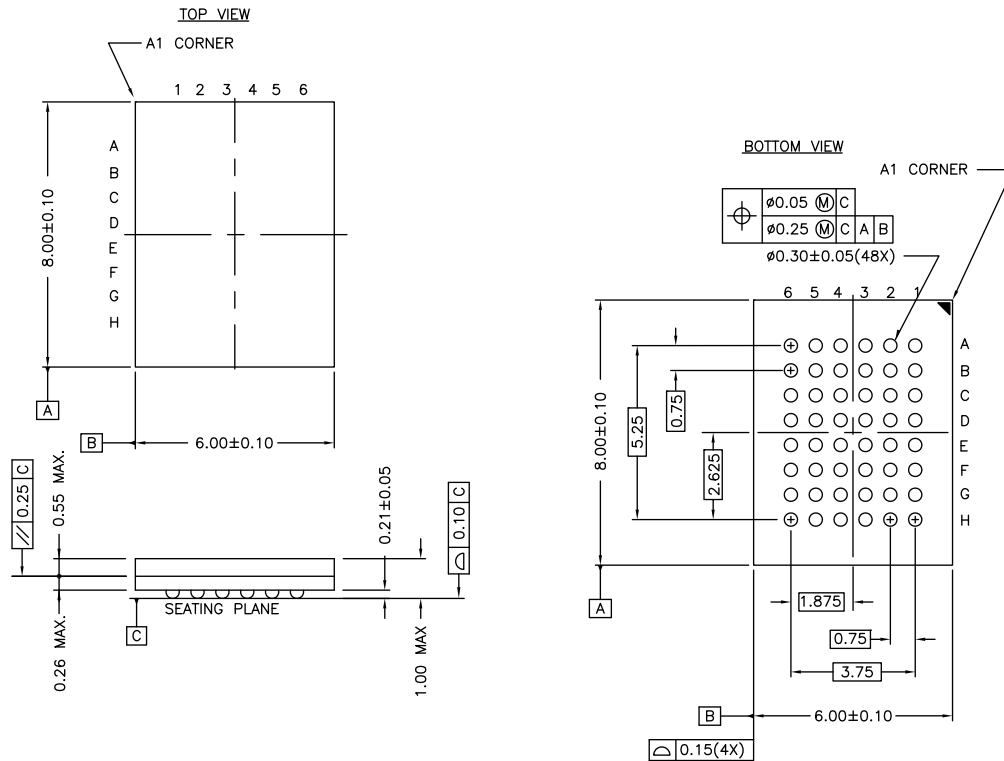
| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|------------|--------------------|-----------------|---|-----------------|
| 45 | CY62157H30-45BVXI | 51-85150 | 48-ball VFBGA (6 × 8 × 1 mm) (Pb-free), Package Code: BZ48 | Industrial |
| | CY62157H30-45BVXIT | | | |

Ordering Code Definitions



Package Diagrams

Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) Package Outline, 51-85150

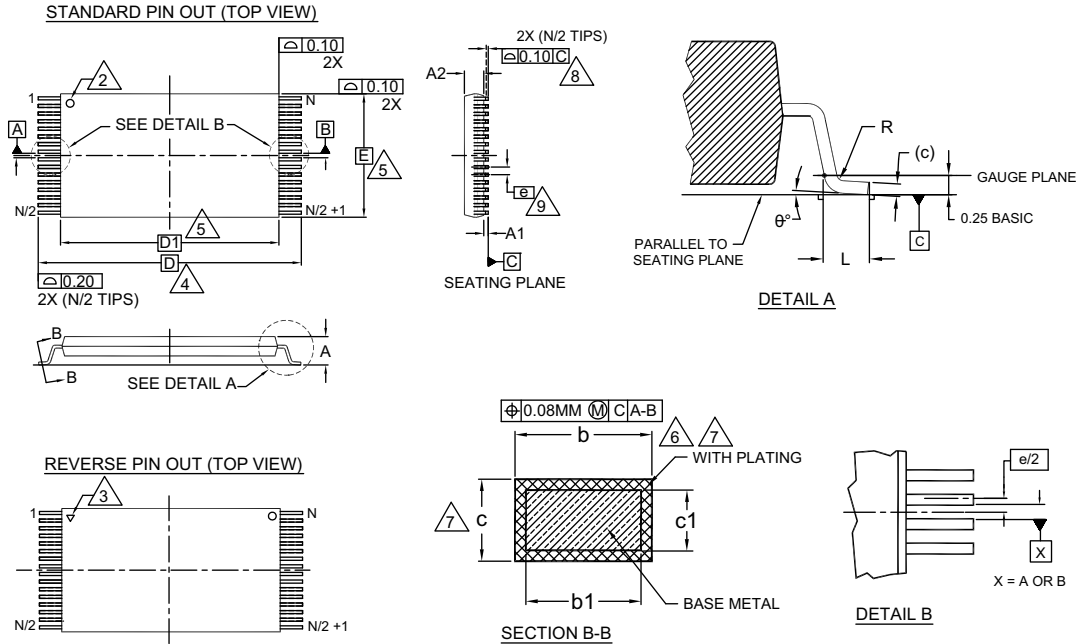


NOTE:
 PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Package Diagrams (continued)

Figure 12. 48-pin TSOP I (12 × 18.4 × 1.0 mm) Package Outline, 51-85183



| SYMBOL | DIMENSIONS | | |
|--------|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.20 |
| A1 | 0.05 | — | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 |
| b1 | 0.17 | 0.20 | 0.23 |
| b | 0.17 | 0.22 | 0.27 |
| c1 | 0.10 | — | 0.16 |
| c | 0.10 | — | 0.21 |
| D | 20.00 BASIC | | |
| D1 | 18.40 BASIC | | |
| E | 12.00 BASIC | | |
| e | 0.50 BASIC | | |
| L | 0.50 | 0.60 | 0.70 |
| θ | 0° | — | 8 |
| R | 0.08 | — | 0.20 |
| N | 48 | | |

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS (mm).
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE \square -C-. THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm .
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
10. JEDEC SPECIFICATION NO. REF: MO-142(D)DD.

51-85183 *F

Acronyms

| Acronym | Description |
|-------------------------|---|
| $\overline{\text{BHE}}$ | byte high enable |
| $\overline{\text{BLE}}$ | byte low enable |
| $\overline{\text{CE}}$ | chip enable |
| CMOS | complementary metal oxide semiconductor |
| I/O | input/output |
| $\overline{\text{OE}}$ | output enable |
| SRAM | static random access memory |
| VFBGA | very fine-pitch ball grid array |
| $\overline{\text{WE}}$ | write enable |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | Degrees Celsius |
| MHz | megahertz |
| μA | microamperes |
| μs | microseconds |
| mA | milliamperes |
| mm | millimeters |
| ns | nanoseconds |
| Ω | ohms |
| % | percent |
| pF | picofarads |
| V | volts |
| W | watts |

Document History Page

| Document Title: CY62157H MoBL®, 8-Mbit (512K words × 16-bit) Static RAM with Error-Correcting Code (ECC) Document Number: 001-88316 | | | | |
|--|---------|-----------------|-----------------|---|
| Rev. | ECN No. | Orig. of Change | Submission Date | Description of Change |
| *B | 4983842 | NILE | 10/23/2015 | Changed status from Preliminary to Final. |
| *C | 5109716 | NILE | 01/27/2016 | Updated DC Electrical Characteristics : Changed minimum value of V _{OH} parameter from 2.2 V to 2.4 V corresponding to V _{CC} Operating Range “2.7 V to 3.6 V” and Test Condition “V _{CC} = Min, I _{OH} = -1.0 mA”. |
| *D | 5427485 | VINI | 09/06/2016 | Updated Maximum Ratings : Updated Note 4 (Replaced “2 ns” with “20 ns”). Updated DC Electrical Characteristics : Changed minimum value of V _{IH} parameter from 2.0 V to 1.8 V corresponding to the Operating Range “2.2 V to 2.7 V”. Updated Ordering Information : Updated part numbers. Updated to new template. Completing Sunset Review. |
| *E | 6063494 | VINI | 02/08/2018 | Updated Package Diagrams : spec 51-85183 – Changed revision from *D to *F. Updated to new template. |