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USB-I²C Single Channel Bridge Controller

Features

- USB 2.0-compliant, Full-Speed (12 Mbps)
 - Supports communication driver class (CDC), personal health care device class (PHDC), and vendor-device class
 - Battery charger detection (BCD) compliant with USB Battery Charging Specification, Rev. 1.2 (Peripheral Detect only)
 - Integrated USB termination resistors
- Single-channel configurable I²C interface
 - Master/Slave up to 400 kHz and by default the part is configured as I²C Slave
 - 256 bytes each transmit and receive buffer
 - Supports multi-master I²C
- General-purpose input/output (GPIO) pins: 8
- 512-byte flash for storing configuration parameters
- Configuration utility (Windows) to configure the following:
 - Vendor ID (VID), Product ID (PID), and Product and Manufacturer descriptors
 - I²C
 - Charger detection
 - GPIO
- Driver support for VCOM and DLL
 - Windows 10: 32- and 64-bit versions
 - Windows 8.1: 32- and 64-bit versions
 - Windows 8: 32- and 64-bit versions
 - Windows 7: 32- and 64-bit versions
 - Windows Vista: 32- and 64-bit versions
 - Windows XP: 32- and 64-bit versions
 - Mac OS-X: 10.6, 10.7
 - Linux: Kernel version 2.6.35 onwards.
- Clocking: Integrated 48-MHz clock oscillator
- Supports bus-/self-powered configurations
- USB Suspend mode for low power
- Operating voltage: 1.71 to 5.5 V
- Operating temperature
 - Commercial: 0 °C to 70 °C
 - Industrial: -40 °C to 85 °C
- ESD protection: 2.2-kV HBM

- RoHS-compliant package
 - 24-pin QFN (4.0 mm × 4.0 mm, 0.55 mm, 0.5 mm pitch)
- Ordering part number
 - CY7C65216-24LTXI
 - CY7C65216-24LTXIT

Applications

- Medical/healthcare devices
- Point-of-Sale (POS) terminals
- Test and measurement system
- Gaming systems
- Set-top box PC-USB interface
- Industrial
- Networking
- Enabling USB connectivity in legacy peripherals

Functional Description

For a complete list of related resources, click [here](#).

USB-Compliant

USB-I²C Single Channel Bridge Controller is fully compliant with the USB 2.0 Specification and Battery Charger Specification v1.2.

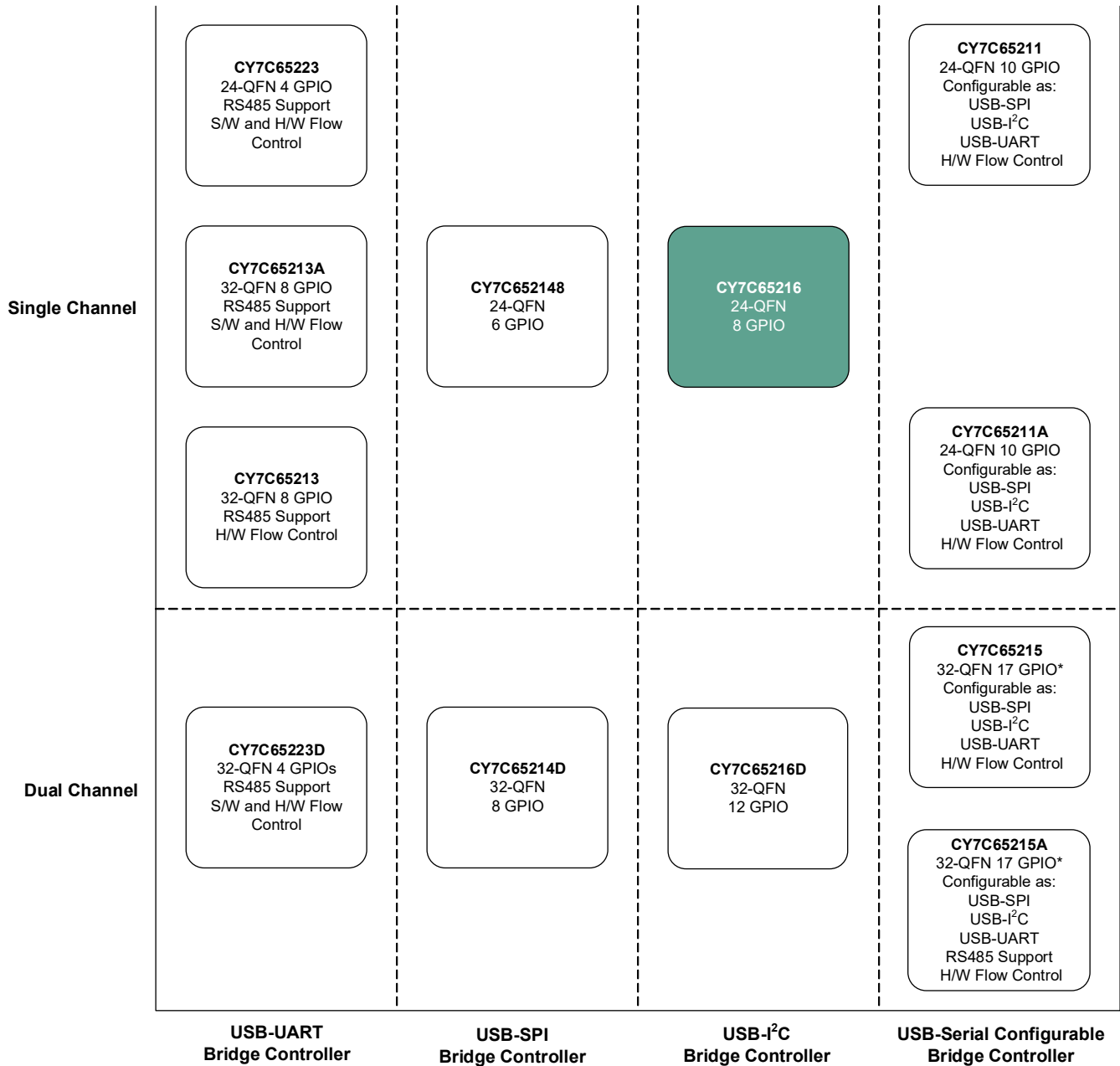


Errata: For information on silicon errata, see “Errata” on page 25. Details include trigger conditions, devices affected, and proposed workaround.

USB Serial Bridge Controller Family

USB Serial bridge Controllers are a family of configurable products for most common applications requiring no firmware changes. Configuration utility is provided to Configure USB-VID, USB-PID, USB Product and Manufacturer Descriptors. The same configuration utility can be used to configure UART, I²C, SPI, Battery Charger Detection, GPIOs, Power mode, and so on.

Figure 1. USB Serial Bridge Controller Family



Errata: For information on silicon errata, see "Errata" on page 25. Details include trigger conditions, devices affected, and proposed workaround.

Table 1. USB Serial Family Feature Comparison

| MPN | # of Channels | GPIO | USB-UART | | | | USB-SPI | | USB-I ² C |
|------------------|---------------|----------|---------------|-----------------------|-----------------------|---------------|-----------------------------|------------------|-------------------------------|
| | | | RS485 Support | Software Flow Control | Hardware Flow Control | UART Pins** | SPI Serial Data Width (bit) | SPI Master/Slave | I ² C Master/Slave |
| CY7C65213 | 1 | 8 | N | N | Y | 8 | – | – | – |
| CY7C65213A | 1 | 8 | Y | N | Y | 8 | – | – | – |
| CY7C65223 | 1 | 4 | Y | Y | Y | 2 / 4 / 6 | – | – | – |
| CY7C65223D | 2 | 4 | Y | Y | Y | 2 / 4 / 6 / 8 | – | – | – |
| CY7C652148 | 1 | 6 | – | – | – | – | 4-16 bits | Master/Slave | – |
| CY7C65214D | 2 | 8 | – | – | – | – | 4-16 bits | Master/Slave | – |
| CY7C65216 | 1 | 8 | – | – | – | – | – | – | Master/Slave |
| CY7C65216D | 2 | 12 | – | – | – | – | – | – | Master/Slave |
| CY7C65211 | 1 | 10* | N | N | Y | 2 / 4 / 6 | 4-16 bits | Master/Slave | Master/Slave |
| CY7C65211A | 1 | 10* | Y | N | Y | 2 / 4 / 6 | 4-16 bits | Master/Slave | Master/Slave |
| CY7C65215 | 2 | 17* | N | N | Y | 2 / 4 / 6 | 4-16 bits | Master/Slave | Master/Slave |
| CY7C65215A | 2 | 17* | Y | N | Y | 2 / 4 / 6 / 8 | 4-16 bits | Master/Slave | Master/Slave |

Legend

* Represents the total GPIO count offered by the part. This count can dynamically change based on UART / SPI / I²C pin configuration.

** UART Pins

| **UART Pins | UART Signal |
|-------------|---|
| 2 | RxD and TxD |
| 4 | RxD, TxD, RTS#, CTS# |
| 6 | RxD, TxD, RTS#, CTS#, DTR#, DSR# |
| 8 | RxD, TxD, RTS#, CTS#, DTR#, DSR#, DCD#, RI# |

Table 2. Default Serial Channel Configuration

| MPN | # of Channels | GPIO | USB Protocol | USB- UART | | USB-SPI | USB-I ² C |
|------------------|---------------|----------|------------------|------------------|-----------|-------------------|--------------------------------|
| | | | | Is RS485 Enabled | UART Pins | SPI Master/ Slave | I ² C Master/ Slave |
| CY7C65213 | 1 | 4 | CDC** | N | 8 | – | – |
| CY7C65213A | 1 | 4 | CDC** | N | 8 | – | – |
| CY7C65223 | 1 | 4 | CDC** | Y | 4 | – | – |
| CY7C65223D | 2 | 4 | CDC** | Y | 4 | – | – |
| CY7C652148 | 1 | 6 | Vendor*** | – | – | Master | – |
| CY7C65214D | 2 | 8 | Vendor*** | – | – | Master | – |
| CY7C65216 | 1 | 8 | Vendor*** | – | – | – | Slave |
| CY7C65216D | 2 | 12 | Vendor*** | – | – | – | Master |
| CY7C65211 | 1 | 3 | CDC** | N | 6 | – | – |
| CY7C65211A | 1 | 3 | CDC** | N | 6 | – | – |
| CY7C65215 | 2 | 4 | CDC** | N | 6 | – | – |
| CY7C65215A | 2 | 4 | CDC** | N | 6 | – | – |

** USB CDC Protocol allows the USB host Operating System to detect the device as Virtual COM Port Device.

*** USB Vendor Protocol allows the USB host operating system to detect the device as general USB device. This device is accessible using Cypress Application Library.

More Information

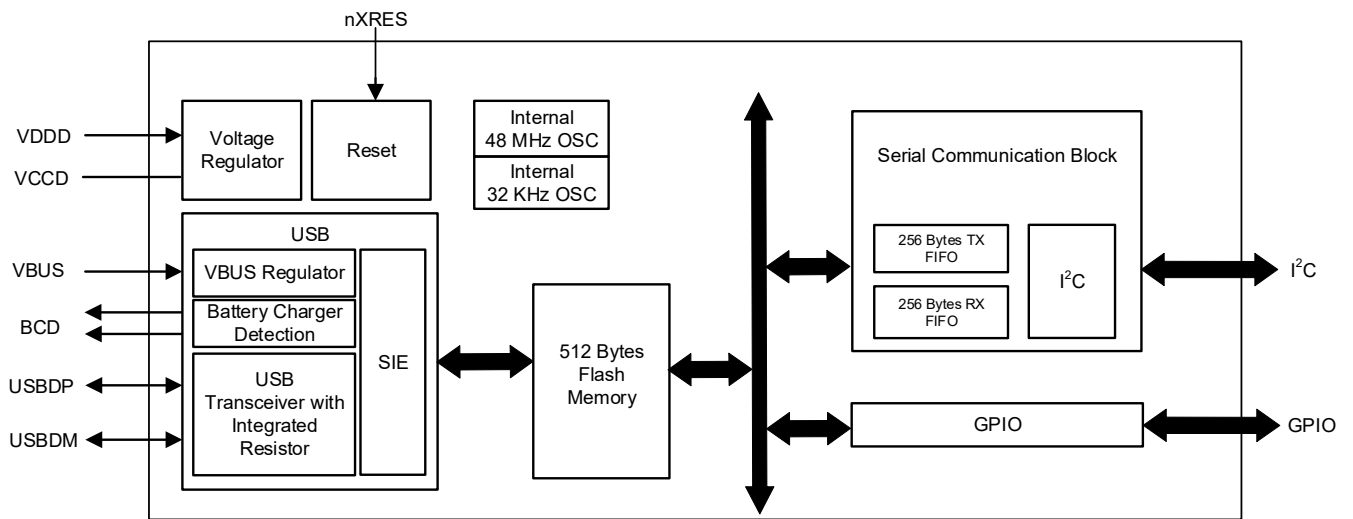
Cypress provides a wealth of data at www.cypress.com to help you to select the right device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the document [USB-Serial Bridge Controller Product Overview](#).

- Overview: [USB Portfolio](#), [USB Roadmap](#)
- USB 2.0 Product Selectors: [USB-Serial Bridge Controller](#), [USB to UART Controller \(Gen I\)](#)
- Knowledge Base Articles: Cypress offers a large number of USB knowledge base articles covering a broad range of topics, from basic to advanced level. Recommended knowledge base articles for getting started with USB-Serial Bridge Controller are:
 - [KBA85909](#) – Key Features of the Cypress® USB-Serial Bridge Controller
 - [KBA85920](#) – USB-UART and USB-Serial
 - [KBA85921](#) – Replacing FT232R with CY7C65213 USB-UART LP Bridge Controller
 - [KBA85913](#) – Voltage supply range for USB-Serial
 - [KBA89355](#) – USB Serial Cypress Default VID and PID
 - [KBA92641](#) – USB-Serial Bridge Controller Managing I/Os using API
 - [KBA92442](#) – Non-Standard Baud Rates in USB-Serial Bridge Controllers
 - [KBA91366](#) – Binding a USB-Serial Device to a Microsoft® CDC Driver
 - [KBA92551](#) – Testing a USB-Serial Bridge Controller Configured as USB-UART with Linux®
 - [KBA91299](#) – Interfacing an External I²C Device with the CYUSBS234/236 DVK

For complete list of knowledge base articles, click [here](#).

- Code Examples: [USB Full-Speed](#)
- Development Kits:
 - [CYUSBS232](#), Cypress USB-UART LP Reference Design Kit
 - [CYUSBS234](#), Cypress USB-Serial (Single Channel) Development Kit
 - [CYUSBS236](#), Cypress USB-Serial (Dual Channel) Development Kit
- Models: [IBIS](#)

Block Diagram



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Functional Overview

The CY7C65216 is a Full-Speed USB controller that enables seamless PC connectivity for peripherals with I²C interface. CY7C65216 is compliant to BCD specification rev 1.2. It integrates a voltage regulator, an oscillator, and flash memory for storing configuration parameters, offering a cost-effective solution. CY7C65216 supports bus-powered and self-powered modes and enables efficient system power management with suspend and remote wake-up signals. It is available in a 24-pin QFN package.

USB and Charger Detect

USB

CY7C65216 has a built-in USB 2.0 Full-Speed transceiver. The transceiver incorporates the internal USB series termination resistors on the USB data lines and a 1.5-k Ω pull-up resistor on USBDP.

Charger Detection

CY7C65216 supports BCD for Peripheral Detect only and complies with the USB Battery Charging Specification, Rev. 1.2. It supports the following charging ports:

- Standard Downstream Port (SDP): Allows the system to draw up to 500 mA current from the host
- Charging Downstream Port (CDP): Allows the system to draw up to 1.5 A current from the host
- Dedicated Charging Port (DCP): Allows the system to draw up to 1.5 A of current from the wall charger

Serial Communication

CY7C65216 has a serial communication block (SCB). Each SCB can implement I²C interface. A 256-byte buffer is available in both the TX and RX lines.

I²C Interface

The I²C interface implements full multi-master/slave modes and supports up to 400 kHz. The configuration utility tool is used to set the I²C address in the slave mode. The tool enables only even slave addresses. For further details on the protocol, refer to the NXP I²C specification, Rev. 5.

Notes

- I²C ports are not tolerant of higher voltages. Therefore, they cannot be hot-swapped or powered up independently when chip is not powered.
- The minimum fall time of the SCL is met (as per NXP I²C specification Rev. 5) when V_{DD} is between 1.71 V and 3.0 V. When V_{DD} is within the range of 3.0 V to 3.6 V, it is recommended to add a 50 pF capacitor on the SCL signal.

Default Configuration

CY7C65216 is configured as I²C slave device with default I²C slave 7-bit address as 0x30.

Memory

CY7C65216 has a 512-byte flash. Flash is used to store USB parameters, such as VID/PID, serial number, product and manufacturer descriptors, which can be programmed by the configuration utility.

System Resources

Power System

CY7C65216 supports the USB Suspend mode to control power usage. CY7C65216 operates in bus-powered or self-powered modes over a range of 3.15 to 5.5 V.

Clock System

CY7C65216 has a fully integrated clock with no external components required. The clock system is responsible for providing clocks to all subsystems.

Internal 48-MHz Oscillator

The internal 48-MHz oscillator is the primary source of internal clocking in CY7C65216.

Internal 32-kHz Oscillator

The internal 32-kHz oscillator is primarily used to generate clocks for peripheral operation in the USB Suspend mode.

Reset

The reset block ensures reliable power-on reset and brings the device back to the default known state. The nXRES (active low) pin can be used by the external devices to reset the CY7C65216.

Suspend and Resume

The CY7C65216 device asserts the SUSPEND pin when the USB bus enters the suspend state. This helps in meeting the stringent suspend current requirement of the USB 2.0 specification, while using the device in bus-powered mode. The device resumes from the suspend state under either of the two following conditions:

1. Any activity is detected on the USB bus
2. The WAKEUP pin is asserted to generate remote wakeup to the host

WAKEUP

The WAKEUP pin is used to generate the remote wakeup signal on the USB bus. The remote wakeup signal is sent only if the host enables this feature through the SET_FEATURE request. The device communicates support for the remote wakeup to the host through the configuration descriptor during the USB enumeration process. The CY7C65216 device allows enabling/disabling and polarity of the remote wakeup feature through the configuration utility.

Software

Cypress delivers a complete set of software drivers and a configuration utility to enable configuration of the product during system development.

Drivers for Linux Operating Systems

Cypress provides a User Mode USB driver library (*libcyusbserial.so*) that abstracts vendor commands for the I²C interface and provides a simplified API interface for user applications. This library uses the standard open-source libUSB library to enable USB communication. The Cypress serial library supports the USB plug-and-play feature using the Linux 'udev' mechanism.

CY7C65216 binds to Linux USB Inbox driver, which is part of Linux Kernel distribution.

Drivers for Mac OSx

Cypress delivers a dynamically linked shared library (*CyUSB-Serial.dylib*) based on libUSB, which enables communication to the CY7C65216 device.

In addition, CY7C65216 binds to Mac OSx native driver.

Drivers for Windows Operating Systems

For Windows operating systems (XP, Vista, Win7, Win 8, Win 8.1, and Windows 10), Cypress delivers a user-mode dynamically linked library-CyUSBSerial DLL-that abstracts a vendor-specific interface of the CY7C65216 devices and provides convenient APIs to the user. It provides interface APIs for vendor-specific I²C and class-specific APIs for PHDC.

USB-I²C Bridge Controller works with Cypress provided USB vendor class driver. The Cypress Windows drivers are MS logo certified drivers.

These drivers are bound to device through WU (Windows Update) services.

Cypress drivers also support Windows plug-and-play and power management and USB Remote Wake-up.

Device Configuration Utility (Windows only)

A Windows-based configuration utility is available to configure device initialization parameters. This graphical user application provides an interactive interface to define the boot parameters stored in the device flash.

This utility allows the user to save a user-selected configuration to text or xml formats. It also allows users to load a selected configuration from text or xml formats. The configuration utility allows the following operations:

- View current device configuration
- Select and configure I²C, battery charging, and GPIOs
- Configure USB VID, PID, and string descriptors
- Save or Load configuration

You can download the free configuration utility and drivers at www.cypress.com.

Internal Flash Configuration

The internal flash memory can be used to store the configuration parameters shown in the following table. A free configuration utility is provided to configure the parameters listed in the table to meet application-specific requirements over the USB interface. The configuration utility can be downloaded at www.cypress.com/usbserial.

Table 3. Internal Flash Configuration for CY7C65216

| Parameter | Default Value | Description |
|--------------------------|-----------------------------|--|
| USB Configuration | | |
| USB Vendor ID (VID) | 0x04B4 | Default Cypress VID. Can be configured to customer VID. |
| USB Product ID (PID) | 0x0004 | Default Cypress PID. Can be configured to customer PID. |
| Manufacturer string | Cypress | Can be configured with any string up-to 64 characters |
| Product string | USB-Serial (Single Channel) | Can be configured with any string up-to 64 characters |
| Serial string | - | Can be configured with any string up-to 64 characters |
| Power mode | Bus powered | Can be configured to bus-powered or self-powered mode |
| Max current draw | 100 mA | Can be configured to any value from 0 to 500 mA. The configuration descriptor will be updated based on this. |
| Remote wakeup | Enabled | Can be disabled. Remote wakeup is initiated by asserting the WAKEUP pin. |
| USB interface protocol | Vendor | Can be configured to function in CDC, PHDC, or Cypress vendor class |
| BCD | Disabled | Charger detect is disabled by default. When BCD is enabled, three of the GPIOs must be configured for BCD. |

Electrical Specifications

Absolute Maximum Ratings

Exceeding maximum ratings^[1] may shorten the useful life of the device.

Storage temperature -55 °C to +100 °C

Ambient temperature with power supplied (Industrial) -40 °C to +85 °C

Supply voltage to ground potential

V_{DDD} 6.0 V

V_{BUS} 6.0 V

V_{CCD} 1.95 V

V_{GPIO} V_{DDD} + 0.5 V

Static discharge voltage ESD protection levels:

- 2.2-KV HBM per JESD22-A114

Latch-up current 140 mA

Current per GPIO 25 mA

Operating Conditions

T_A (ambient temperature under bias)

Industrial -40 °C to +85 °C

V_{BUS} supply voltage 3.15 V to 5.25 V

V_{DDD} supply voltage 1.71 V to 5.50 V

V_{CCD} supply voltage 1.71 V to 1.89 V

Device-Level Specifications

All specifications are valid for -40 °C ≤ T_A ≤ 85 °C, T_J ≤ 100 °C, and 1.71 V to 5.50 V, except where noted.

Table 4. DC Specifications

| Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------------|-----------------------------------|------|------|------|-------|--|
| V _{BUS} | V _{BUS} supply voltage | 3.15 | 3.30 | 3.45 | V | Set and configure the correct voltage range using a configuration utility for V _{BUS} . Default 5 V. |
| | | 4.35 | 5.00 | 5.25 | V | |
| V _{DDD} | V _{DDD} supply voltage | 1.71 | 1.80 | 1.89 | V | Used to set I/O and core voltage. Set and configure the correct voltage range using a configuration utility for V _{DDD} . Default 3.3 V. |
| | | 2.0 | 3.3 | 5.5 | V | |
| V _{CCD} | Output voltage (for core logic) | – | 1.80 | – | V | Do not use this supply to drive the external device. <ul style="list-style-type: none"> • 1.71 V ≤ V_{DDD} ≤ 1.89 V: Short the V_{CCD} pin with the V_{DDD} pin • V_{DDD} > 2 V – connect a 1-μF capacitor (C_{efc}) between the V_{CCD} pin and ground |
| C _{efc} | External regulator voltage bypass | 1.00 | 1.30 | 1.60 | μF | X5R ceramic or better |
| I _{DD1} | Operating supply current | – | 20 | – | mA | USB 2.0 FS, no GPIO switching |
| I _{DD2} | USB Suspend supply current | – | 5 | – | μA | Does not include current through a pull-up resistor on USBDP. In USB suspend mode, the D+ voltage can go up to a maximum of 3.8 V. |

Table 5. AC Specifications

| Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------------------|------------------------------|-----|-----|-----|-------|--------------------|
| Z _{out} | USB driver output impedance | 28 | – | 44 | Ω | – |
| T _{wakeup} | Wakeup from USB Suspend mode | – | 25 | – | μs | – |

Note

1. Usage above the Absolute Maximum conditions may cause permanent damage to the device. Exposure to Absolute Maximum conditions for extended periods of time may affect device reliability. When used below Absolute Maximum conditions but above normal operating conditions, the device may not operate to specification.

GPIO
Table 6. GPIO DC Specifications

| Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|----------------|--|----------------------|-----|---------------------|------------|--|
| $V_{IH}^{[2]}$ | Input voltage high threshold | $0.7 \times V_{DD}$ | – | – | V | CMOS Input |
| V_{IL} | Input voltage low threshold | – | – | $0.3 \times V_{DD}$ | V | CMOS Input |
| $V_{IH}^{[2]}$ | LVTTL input, $V_{DD} < 2.7$ V | $0.7 \times V_{DD}$ | – | – | V | – |
| V_{IL} | LVTTL input, $V_{DD} < 2.7$ V | – | – | $0.3 \times V_{DD}$ | V | – |
| $V_{IH}^{[2]}$ | LVTTL input, $V_{DD} \geq 2.7$ V | 2 | – | – | V | – |
| V_{IL} | LVTTL input, $V_{DD} \geq 2.7$ V | – | – | 0.8 | V | – |
| V_{OH} | CMOS output voltage high level | $V_{DD} - 0.4$ | – | – | V | $I_{OH} = 4$ mA, $V_{DD} = 5$ V +/- 10% |
| V_{OH} | CMOS output voltage high level | $V_{DD} - 0.6$ | – | – | V | $I_{OH} = 4$ mA, $V_{DD} = 3.3$ V +/- 10% |
| V_{OH} | CMOS output voltage high level | $V_{DD} - 0.5$ | – | – | V | $I_{OH} = 1$ mA, $V_{DD} = 1.8$ V +/- 5% |
| V_{OL} | CMOS output voltage low level | – | – | 0.4 | V | $I_{OL} = 8$ mA, $V_{DD} = 5$ V +/- 10% |
| V_{OL} | CMOS output voltage low level | – | – | 0.6 | V | $I_{OL} = 8$ mA, $V_{DD} = 3.3$ V +/- 10% |
| V_{OL} | CMOS output voltage low level | – | – | 0.6 | V | $I_{OL} = 4$ mA, $V_{DD} = 1.8$ V +/- 5% |
| Rpullup | Pull-up resistor | 3.5 | 5.6 | 8.5 | k Ω | – |
| Rpulldown | Pull-down resistor | 3.5 | 5.6 | 8.5 | k Ω | – |
| I_{IL} | Input leakage current (absolute value) | – | – | 2 | nA | 25 °C, $V_{DD} = 3.0$ V |
| C_{IN} | Input capacitance | – | – | 7 | pF | – |
| Vhysttl | Input hysteresis LVTTL; $V_{DD} > 2.7$ V | 25 | 40 | C | mV | – |
| Vhyscmos | Input hysteresis CMOS | $0.05 \times V_{DD}$ | – | – | mV | – |

Note

 2. V_{IH} must not exceed $V_{DD} + 0.2$ V.

Table 7. GPIO AC Specifications

| Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-----------------|------------------------|-----|-----|-----|-------|--|
| $T_{RiseFast1}$ | Rise Time in Fast mode | 2 | – | 12 | ns | $V_{DD} = 3.3$ V/ 5.5 V, Clod = 25 pF |
| $T_{FallFast1}$ | Fall Time in Fast mode | 2 | – | 12 | ns | $V_{DD} = 3.3$ V/ 5.5 V, Clod = 25 pF |
| $T_{RiseSlow1}$ | Rise Time in Slow mode | 10 | – | 60 | ns | $V_{DD} = 3.3$ V/ 5.5 V, Clod = 25 pF |
| $T_{FallSlow1}$ | Fall Time in Slow mode | 10 | – | 60 | ns | $V_{DD} = 3.3$ V/ 5.5 V, Clod = 25 pF |
| $T_{RiseFast2}$ | Rise Time in Fast mode | 2 | – | 20 | ns | $V_{DD} = 1.8$ V, Clod = 25 pF |
| $T_{FallFast2}$ | Fall Time in Fast mode | 20 | – | 100 | ns | $V_{DD} = 1.8$ V, Clod = 25 pF |
| $T_{RiseSlow2}$ | Rise Time in Slow mode | 2 | – | 20 | ns | $V_{DD} = 1.8$ V, Clod = 25 pF |
| $T_{FallSlow2}$ | Fall Time in Slow mode | 20 | – | 100 | ns | $V_{DD} = 1.8$ V, Clod = 25 pF |

nXRES
Table 8. nXRES DC Specifications

| Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|----------------------|------------------------------|------------------------|-----|------------------------|-------|--------------------|
| V _{IH} | Input voltage high threshold | 0.7 × V _{DDD} | – | – | V | – |
| V _{IL} | Input voltage low threshold | – | – | 0.3 × V _{DDD} | V | – |
| R _{pullup} | Pull-up resistor | 3.5 | 5.6 | 8.5 | kΩ | – |
| C _{IN} | Input capacitance | – | 5 | – | pF | – |
| V _{hysxres} | Input voltage hysteresis | – | 100 | – | mV | – |

Table 9. nXRES AC Specifications

| Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-------------------------|-------------------|-----|-----|-----|-------|--------------------|
| T _{resetwidth} | Reset pulse width | 1 | – | – | μs | – |

I²C Specifications
Table 10. I²C Specifications

| Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------------|----------------------------|-----|-----|-----|-------|--------------------|
| F _{I2C} | I ² C frequency | 1 | – | 400 | kHz | – |

Flash Memory Specifications
Table 11. Flash Memory Specifications

| Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------------|--|------|-----|-----|--------|--------------------|
| F _{end} | Flash endurance | 100K | – | – | cycles | – |
| F _{ret} | Flash retention. T _A ≤ 85 °C, 10 K program/erase cycles | 10 | – | – | years | – |

Pin Description

| Pin ^[3] | Type | Name | Default | Description |
|--------------------|----------|-----------|----------|---|
| 1 | GPIO | GPIO_6 | GPIO IN | GPIO Input Pin (see Table 12 and Table 13) |
| 2 | GPIO | GPIO_7 | GPIO OUT | GPIO Output Pin (see Table 12 and Table 13) |
| 3 | Power | VSSD | | Digital Ground |
| 4 | GPIO | GPIO_8 | GPIO OUT | GPIO Output Pin (see Table 12 and Table 13) |
| 5 | GPIO | GPIO_9 | GPIO OUT | GPIO Output Pin (see Table 12 and Table 13) |
| 6 | GPIO | GPIO_10 | GPIO OUT | GPIO Output Pin (see Table 12 and Table 13) |
| 7 | Output | POWER# | | Signal to external logic to indicate USB Unconfigured state and USB Suspend |
| 8 | Output | Suspend | | Indicates device in suspend mode. Can be configured as active low/high using the configuration utility. |
| 9 | Input | Wakeup | | Wakeup device from suspend mode. Can be configured as active low/high using the configuration utility. |
| 10 | USBIO | USBDP | | USB Data Signal Plus, integrates termination resistor and a 1.5-kΩ pull-up resistor |
| 11 | USBIO | USBDM | | USB Data Signal Minus, integrates termination resistor |
| 12 | Power | VCCD | | This pin should be decoupled to ground using a 1-μF capacitor or by connecting a 1.8-V supply (Internal LDO Output) |
| 13 | Power | VSSD | | Digital Ground |
| 14 | Reset | nXRES | | Chip Reset active, low. Can be left unconnected or have a pull up resistor connected when not in use. |
| 15 | Power | VBUS | | VBUS Supply, 3.15 V to 5.25 V |
| 16 | Power | VSSD | | Digital Ground |
| 17 | Power | VSSA | | Analog Ground |
| 18 | GPIO | Rx/Tx LED | | Notification LED I ² C Tx/Rx |
| 19 | GPIO | GPIO_1 | GPIO IN | GPIO Input Pin (see Table 12 and Table 13) |
| 20 | GPIO | GPIO_2 | GPIO IN | GPIO Input Pin (see Table 12 and Table 13) |
| 21 | SCB/GPIO | SCL | | I ² C Clock |
| 22 | SCB/GPIO | SDA | | I ² C Data |
| 23 | GPIO | GPIO_5 | GPIO IN | GPIO Input Pin (see Table 12 and Table 13) |
| 24 | Power | VDDD | | VDDD Core |

Note

3. Any pin acting as an Input pin should not be left unconnected.

Figure 2. 24-pin QFN Pinout

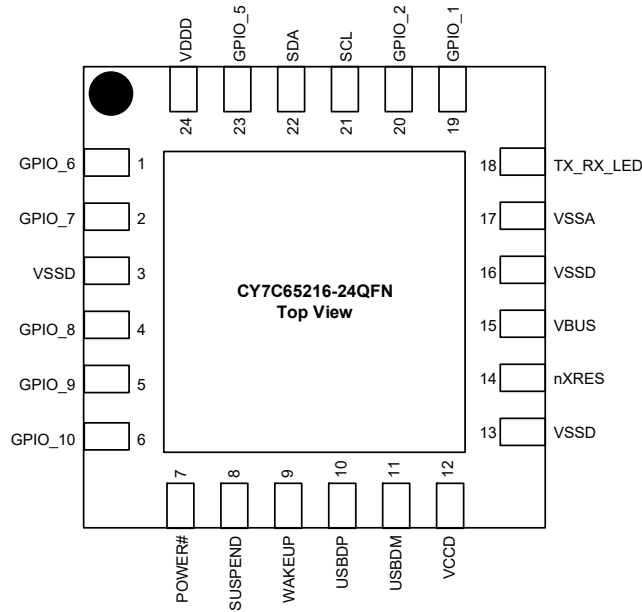


Table 12. Serial Communication Block Configurations

| Pin | Serial Port | Mode 0 ^[4] | Mode 1 |
|-----|-------------|------------------------|-------------------------|
| | | I ² C Slave | I ² C Master |
| 1 | SCB_0 | GPIO_6 | GPIO_6 |
| 20 | SCB_1 | GPIO_2 | GPIO_2 |
| 21 | SCB_2 | SCL_IN | SCL_OUT |
| 22 | SCB_3 | SDA | SDA |
| 23 | SCB_4 | GPIO_5 | GPIO_5 |
| 2 | SCB_5 | GPIO_7 | GPIO_7 |

Note

4. The device is configured in Mode 0 as the default. Other modes can be configured using the configuration utility provided by Cypress.

Legend

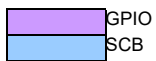


Table 13. GPIO Configurations^[5]

| GPIO Configuration Option | Description |
|---------------------------|--|
| TRISTATE | I/O tristated |
| DRIVE 1 | Output static 1 |
| DRIVE 0 | Output static 0 |
| POWER# | This output is used to control power to an external logic through a switch to cut power off during an unconfigured USB device and USB suspend. 0 - USB device in Configured state 1 - USB device in Unconfigured state or during USB suspend mode |
| TXLED# | Drives LED during USB transmit |
| RXLED# | Drives LED during USB receive |
| TX or RX LED# | Drives LED during USB transmit or receive |
| BCD0 BCD1 | Configurable battery charger detect pins to indicate the type of USB charger (SDP, CDP, or DCP) Configuration example: 00 - Draw up to 100 mA (unconfigured state) 01 - SDP (up to 500 mA) 10 - CDP/DCP (up to 1.5 A) 11 - Suspend (up to 2.5 mA) This truth table can be configured using a configuration utility |
| BUSDETECT | VBUS detection. Connect the VBUS to this pin through a resistor network for VBUS detection when using the BCD feature (refer to Figure 8 , Figure 9 , and Figure 10). |

Note

5. These signal options can be configured on any of the available GPIO pins using the configuration utility provided by Cypress.

USB Power Configurations

The following section describes possible USB power configurations for the CY7C65216. Refer to the [Pin Description on page 13](#) for signal details.

USB Bus-Powered Configuration

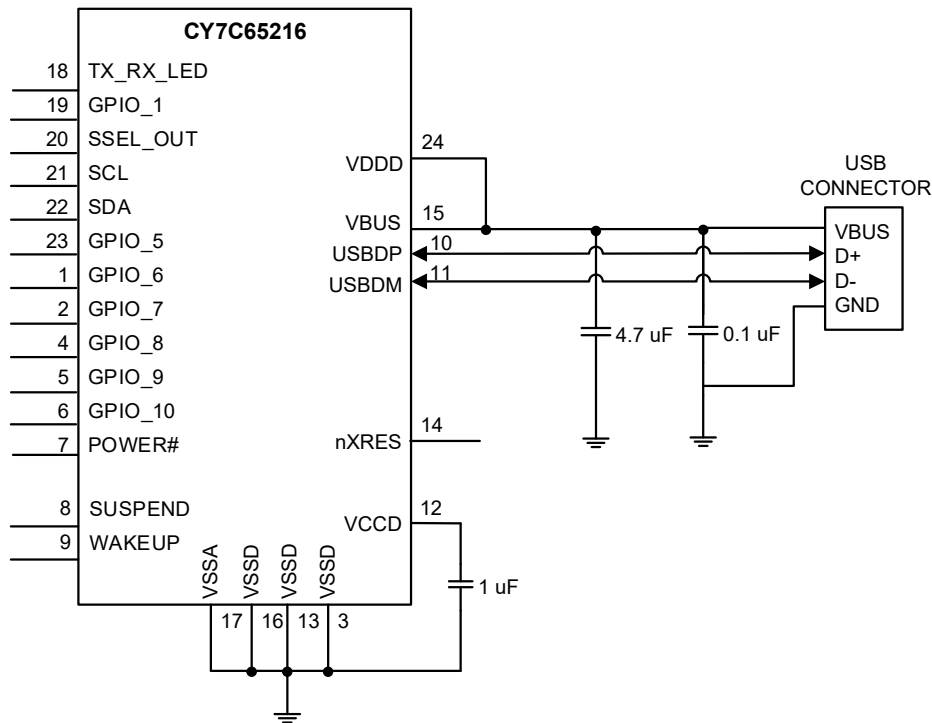
Figure 3 shows an example of the CY7C65216 in a bus-powered design. The VBUS is connected directly to the CY7C65216 because it has an internal regulator.

The USB bus-powered system must comply with the following requirements:

1. The system should not draw more than 100 mA prior to USB enumeration (Unconfigured state).
2. The system should not draw more than 2.5 mA during the USB Suspend mode.
3. A high-power bus-powered system (can draw more than 100 mA when operational) must use POWER# (configured over GPIO) to keep the current consumption below 100 mA prior to USB enumeration, and 2.5 mA during USB Suspend state.
4. The system should not draw more than 500 mA from the USB host.

The configuration descriptor in the CY7C65216 flash should be updated to indicate bus power and the maximum current required by the system using the configuration utility.

Figure 3. Bus-Powered Configuration



Self-Powered Configuration

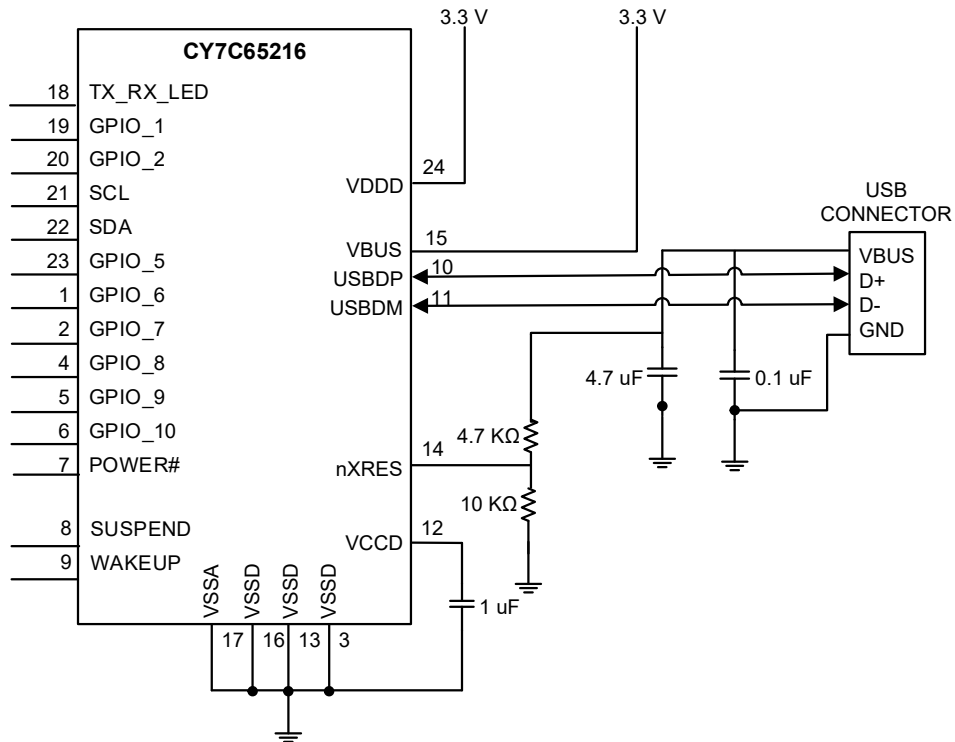
Figure 4 shows an example of CY7C65216 in a self-powered design. A self-powered system does not use the VBUS from the host to power the system, but it has its own power supply. A self-powered system has no restriction on current consumption because it does not draw any current from the VBUS.

When the VBUS is present, CY7C65216 enables an internal, 1.5-kΩ pull-up resistor on USBDP. When the VBUS is absent (USB host is powered down), CY7C65216 removes the 1.5-kΩ pull-up resistor on USBDP. This ensures that no current flows from the USBDP to the USB host through a 1.5-kΩ pull-up resistor, to comply with the USB 2.0 specification.

When reset is asserted to CY7C65216, all the I/O pins are tristated.

The configuration descriptor in the CY7C65216 flash should be updated to indicate self-power using the configuration utility.

Figure 4. Self-Powered Configuration



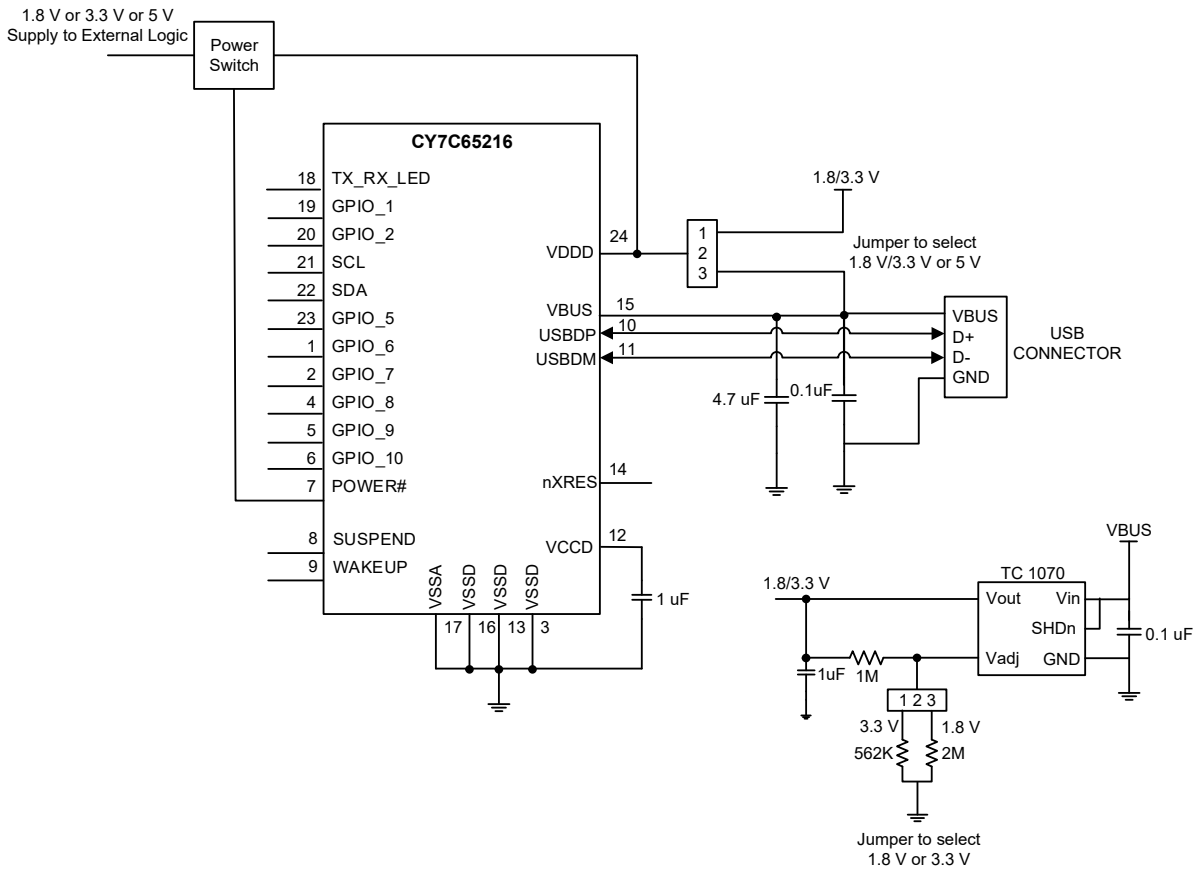
USB Bus-Powered with Variable I/O Voltage

Figure 5 shows CY7C65216 in a bus-powered system with variable I/O voltage. A low dropout (LDO) regulator is used to supply 1.8 V or 3.3 V, using a jumper switch the input of which is 5 V from the VBUS. Another jumper switch is used to select 1.8/3.3 V or 5 V from the VBUS for the VDDD pin of CY7C65216. This allows I/O voltage and supply to external logic to be selected among 1.8 V, 3.3 V, or 5 V.

The USB bus-powered system must comply with the following conditions:

- The system should not draw more than 100 mA prior to USB enumeration (unconfigured state)
- The system should not draw more than 2.5 mA during USB Suspend mode
- A high-power bus-powered system (can draw more than 100 mA when operational) must use POWER# (configured over GPIO) to keep the current consumption below 100 mA prior to USB enumeration and 2.5 mA during the USB Suspend state

Figure 5. USB Bus-Powered with 1.8-V, 3.3-V, or 5-V Variable I/O Voltage^[6]



Note

6. $1.71\text{ V} \leq V_{DDD} \leq 1.89\text{ V}$ - Short VCCA pin with VDDD pin; $V_{DDD} > 2\text{ V}$ - connect a 1- μF decoupling capacitor to the VCCA pin.

Application Examples

The following section provides CY7C65216 application examples.

USB to I²C Bridge

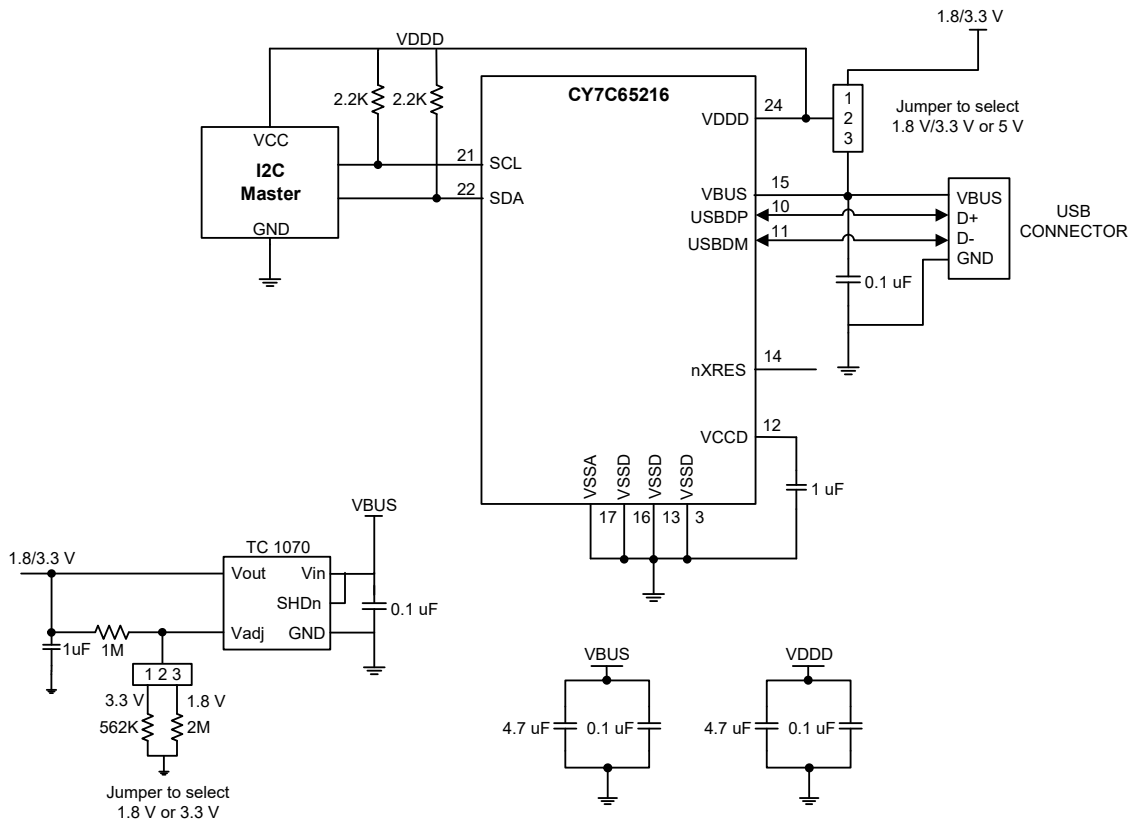
In Figure 6, CY7C65216 is configured as a USB to I²C Bridge. The CY7C65216 I²C can be configured as a master or a slave using the configuration utility. CY7C65216 supports I²C data rates up to 100 kbps in the standard mode (SM) and 400 kbps in the fast mode (FM).

In the master mode, SCL is output from CY7C65216. In the slave mode, SCL is input to CY7C65216. The I²C slave address for CY7C65216 can be configured using the configuration utility. The SDA data line is bi-directional in the master/slave modes. The drive modes of the SCL and SDA port pins are always open drain.

GPIO8 and GPIO9 are configured as RXLED# and TXLED# to drive two LEDs to indicate USB receive and transmit.

Refer to the NXP I²C specification for further details on the protocol.

Figure 6. USB to I²C Bridge



Battery-Operated, Bus-Powered USB to MCU with Battery Charge Detection

Figure 7 illustrates CY7C65216 as a USB-to-microcontroller interface. The TXD and RXD lines are used for data transfer, and the RTS# and CTS# lines are used for handshaking. The SUSPEND pin indicates to the MCU if the device is in USB Suspend, and the WAKEUP pin is used to wake up CY7C65216, which in turn issues a remote wakeup to the USB host.

This application illustrates a battery-operated system, which is bus-powered. CY7C65216 implements the battery charger detection functionality based on the USB Battery Charging Specification, Rev. 1.2.

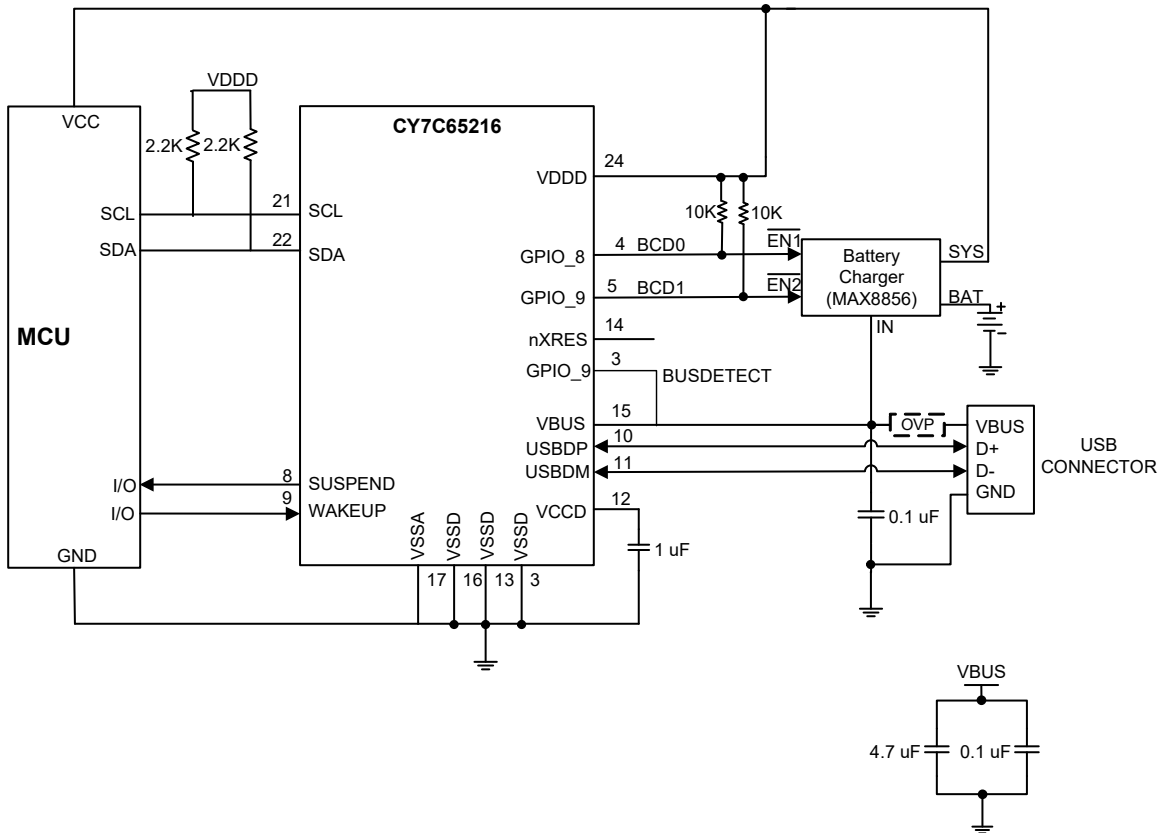
Battery-operated bus power systems must comply with the following conditions:

- The system can be powered from the battery (if not discharged) and can be operational if the VBUS is not connected or powered down.
- The system should not draw more than 100 mA from the VBUS prior to USB enumeration and USB Suspend.
- The system should not draw more than 500 mA for SDP and 1.5 A for CDP/DCP

To comply with the first requirement, the VBUS from the USB host is connected to the battery charger as well as to CY7C65216, as shown in Figure 7. When the VBUS is connected, CY7C65216 initiates battery charger detection and indicates the type of USB charger over BCD0 and BCD1. If the USB charger is SDP or CDP, CY7C65216 enables a 1.5-kΩ pull-up resistor on the USBDP for Full-Speed enumeration. When the VBUS is disconnected, CY7C65216 indicates an absence of the USB charger over BCD0 and BCD1, and removes the 1.5-kΩ pull-up resistor on USBDP. Removing this resistor ensures that no current flows from the supply to the USB host through the USBDP, to comply with the USB 2.0 specification.

To comply with the second and third requirements, two signals (BCD0 and BCD1) are configured over GPIO to communicate the type of USB host charger and the amount of current it can draw from the battery charger. BCD0 and BCD1 signals can be configured using the configuration utility.

Figure 7. USB to MCU Interface with Battery Charge Detection^[7, 8, 9]

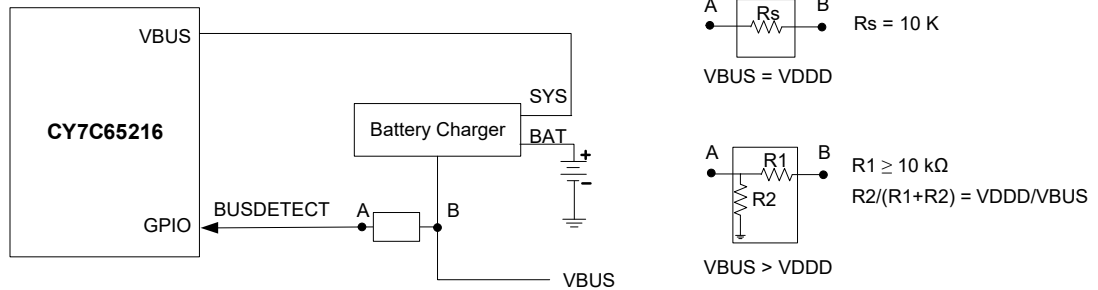


Notes

7. Add a 100-kΩ pull-down resistor on the V_{BUS} pin for quick discharge.
8. Refer Figure 8, Figure 9, Figure 10 and the corresponding descriptions for handling VBUS Over Voltage Protection (OVP).
9. BCD and BUSDETECT functionality are not enabled by default. USB-Serial Configuration Utility is provided to enable BCD and BUSDETECT functionality.

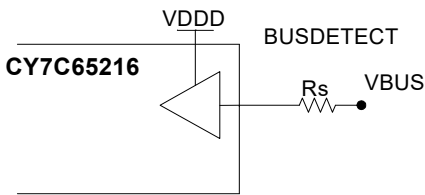
In a battery charger system, a 9-V spike on the VBUS is possible. The CY7C65216 VBUS pin is intolerant to voltage above 6 V. In the absence of over-voltage protection (OVP) on the VBUS line, the VBUS should be connected to BUSDETECT (GPIO configured) using the resistive network and the output of the battery charger to the VBUS pin of CY7C65216, as shown in Figure 8.

Figure 8. 9 V Tolerant



When the VBUS and VDDD are at the same voltage potential, the VBUS can be connected to the GPIO using a series resistor (R_s) (see Figure 9). If there is a charger failure and the VBUS becomes 9 V, then the 10-k Ω resistor plays two roles. It reduces the amount of current flowing into the forward-biased diodes in the GPIO, and it reduces the voltage seen on the pad.

Figure 9. GPIO VBUS Detection, VBUS = VDDD



When the VBUS > VDDD, a resistor voltage divider is required to reduce the voltage from the VBUS down to VDDD for the GPIO sensing the VBUS voltage (see Figure 10).

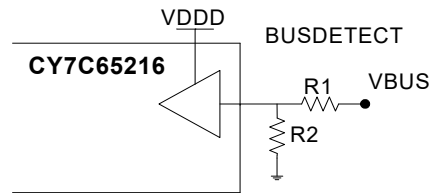
The resistors should be sized as follows:

$$R_1 \geq 10 \text{ k}$$

$$R_2 / (R_1 + R_2) = V_{DDD} / V_{BUS}$$

The first condition limits the voltage and current for the charger failure situation, as described in the previous paragraph, while the second condition allows for normal-operation VBUS detection.

Figure 10. GPIO VBUS detection, VBUS > VDDD



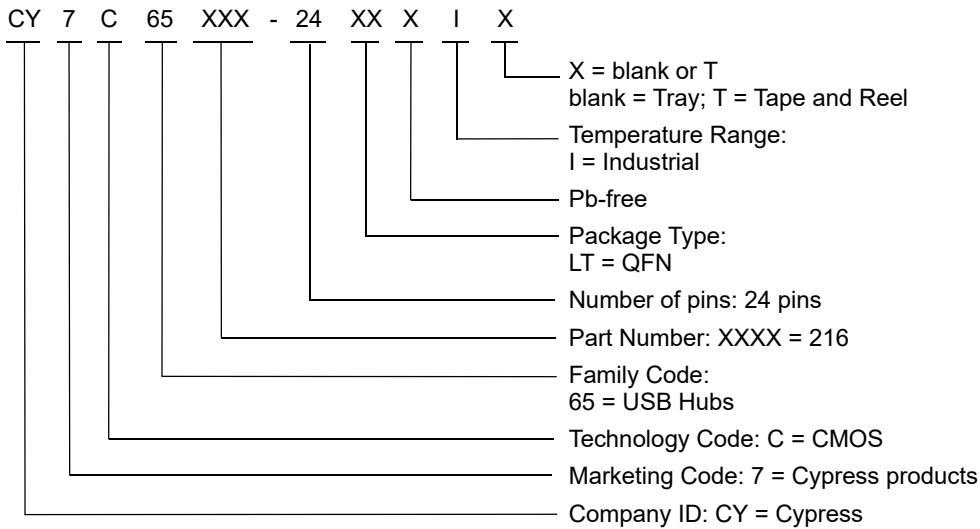
Ordering Information

Table 14 lists the key package features and ordering codes of the CY7C65216. For more information, contact your local sales representative.

Table 14. Key Features and Ordering Information

| Package | Ordering Code | Operating Range |
|---|-------------------|-----------------|
| 24-pin QFN (4.00 × 4.00 × 0.55 mm, 0.5 mm pitch) (Pb-free) | CY7C65216-24LTXI | Industrial |
| 24-pin QFN (4.00 × 4.00 × 0.55 mm, 0.5 mm pitch) (Pb-free) – Tape and Reel | CY7C65216-24LTXIT | Industrial |

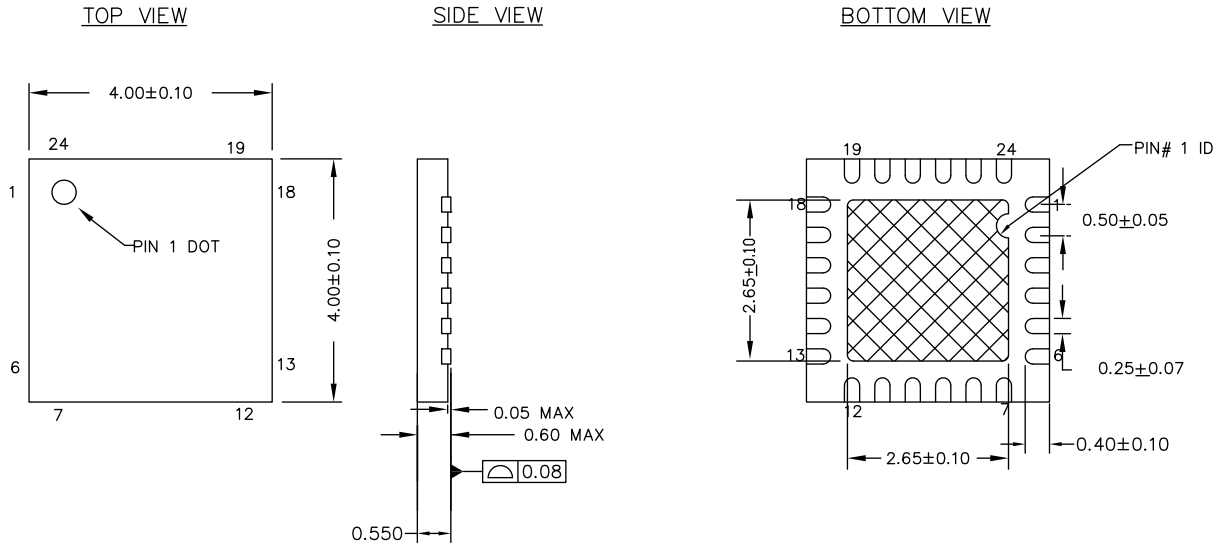
Ordering Code Definitions



Package Information

Support currently is planned for the 24-pin QFN package.

Figure 11. 24-pin QFN 4 mm × 4 mm × 0.55 mm LQ24A 2.65 × 2.65 EPAD (Sawn)



NOTES :

1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT : 29 ± 3 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 *H

Table 15. Package Characteristics

| Parameter | Description | Min | Typ | Max | Units |
|----------------|-------------------------------|-----|------|-----|-------|
| T _A | Operating ambient temperature | -40 | 25 | 85 | °C |
| THJ | Package θ _{JA} | – | 18.4 | – | °C/W |

Table 16. Solder Reflow Peak Temperature

| Package | Maximum Peak Temperature | Maximum Time at Peak Temperature |
|------------|--------------------------|----------------------------------|
| 24-pin QFN | 260 °C | 30 seconds |

Table 17. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

| Package | MSL |
|------------|-------|
| 24-pin QFN | MSL 3 |

Acronyms

Table 18. Acronyms Used in this Document

| Acronym | Description |
|------------------|-----------------------------------|
| BCD | battery charger detection |
| CDC | communication driver class |
| CDP | charging downstream port |
| DCP | dedicated charging port |
| DLL | dynamic link library |
| ESD | electrostatic discharge |
| GPIO | general purpose input/output |
| HBM | human-body model |
| I ² C | inter-integrated circuit |
| MCU | microcontroller unit |
| OSC | oscillator |
| PHDC | personal health care device class |
| PID | product identification |
| SCB | serial communication block |
| SCL | I ² C serial clock |
| SDA | I ² C serial data |
| SDP | standard downstream port |
| SIE | serial interface engine |
| VCOM | virtual communication port |
| USB | Universal Serial Bus |
| VID | vendor identification |

Document Conventions

Units of Measure

Table 19. Units of Measure

| Symbol | Unit of Measure |
|--------|---|
| °C | degree Celsius |
| DMIPS | Dhrystone million instructions per second |
| kΩ | kilo-ohm |
| KB | kilobyte |
| kHz | kilohertz |
| kV | kilovolt |
| Mbps | megabits per second |
| MHz | megahertz |
| mm | millimeter |
| V | volt |

Errata

This section describes the errata for the CY7C65216 USB-Serial family. Details include errata trigger conditions, scope of impact, and available workaround.

Contact your local Cypress Sales Representative if you have questions.

Part Numbers Affected

| Part Number | Device Characteristics |
|-------------|------------------------|
| CY7C65216 | All Variants |

Qualification Status

Production

Errata Summary

The following table defines the errata applicability to available USB-Serial devices.

| Items | Affected Part Number | Fix Status |
|--|----------------------|------------|
| [1.] I2C Reads are slower when USB-Serial is configured as I2C Master. | CY7C65216 | No Fix |

| 1. I ² C Reads are slower when USB-Serial is configured as I ² C Master. | |
|--|---|
| Problem Definition | I ² C reads done by USB-Serial configured as I ² C Master are observed to be slower. This is because of significant delay between the I ² C read initiation and the reception of data from the I ² C Slave. |
| <p>The diagram illustrates the I²C read sequence. It is divided into two main phases: READ INITIATION and DATA RETURNED FROM THE SLAVE, separated by a DELAY.</p> <p>READ INITIATION: This phase starts with a START signal. The Device (Slave) Address (7 bits) is transmitted, followed by the R/W bit (0 for read). This is followed by the Register Address N (8 bits), ending with an ACK signal.</p> <p>DATA RETURNED FROM THE SLAVE: This phase begins with a Repeated START signal. The Device (Slave) Address (7 bits) is transmitted, followed by the R/W bit (1 for write). This is followed by the Data Byte From Register N (8 bits), ending with a NACK signal and a STOP signal.</p> <p>The DELAY is indicated by a large gap between the end of the read initiation sequence and the start of the data return sequence.</p> | |
| Parameters Affected | NA |
| Trigger Condition(s) | No specific trigger condition. The delay is observed between every I ² C Read initiation from the master and reception of slave data. |
| Scope of Impact | I ² C read operations from the master are slower. |
| Workaround | KBA227320 mentions the steps needed to be taken for reducing this delay. |
| Fix Status | No fix. Workaround is proven. |

Document History Page

| Document Title: CY7C65216, USB-I ² C Single Channel Bridge Controller | | | |
|--|---------|-----------------|-------------------------|
| Document Number: 002-31602 | | | |
| Revision | ECN | Submission Date | Description of Change |
| ** | 7021631 | 11/26/2020 | Final datasheet to NSO. |