

# PSoC<sup>®</sup> Programmable System-on-Chip™ CapSense<sup>®</sup> Controller with SmartSense™ Auto-tuning 1–21 Buttons, 0–4 Sliders, Proximity

## Features

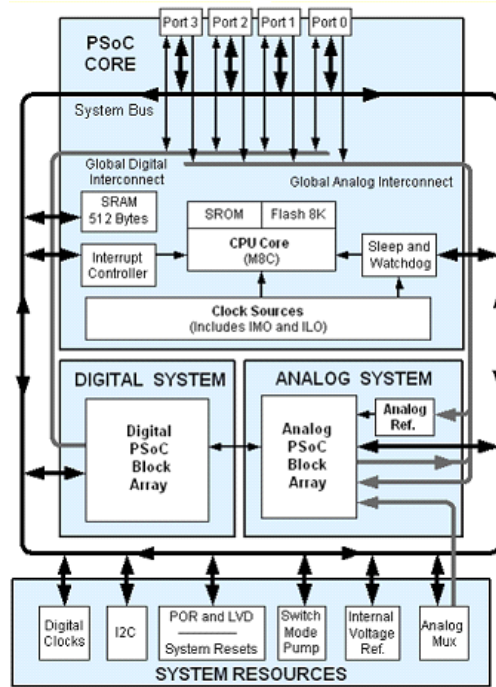
- **Advanced CapSense<sup>®</sup> block with SmartSense™ Auto-Tuning**
  - Patented CSD sensing algorithm
  - SmartSense\_EMC Auto-Tuning
    - Sets and maintains optimal sensor performance during run time
    - Eliminates system tuning during development and production
    - Compensates for variations in manufacturing process
- **Driven shield**
  - Delivers best-in class water tolerant designs
  - Robust proximity sensing in the presence of metal objects
  - Supports longer trace lengths
- **Powerful Harvard-architecture processor**
  - M8C processor speeds up to 24 MHz
  - Low power at high speed
  - Operating voltage: 2.4 V to 5.25 V
  - Operating voltages down to 1.0 V using on-chip switch mode pump (SMP)
  - Industrial temperature range: -40 °C to 85 °C
- **Advanced peripherals (PSoC<sup>®</sup> blocks)**
  - Four analog Type E PSoC blocks provide:
    - Two comparators with digital-to-analog converter (DAC) references
    - Single or dual 10-bit 28 channel analog-to-digital converters (ADC)
  - Four digital PSoC blocks provide:
    - 8- to 32-bit timers, counters, and pulse width modulators (PWMs)
    - Cyclical redundancy check (CRC) and pseudo random sequence (PRS) modules
    - Full-duplex universal asynchronous receiver transmitter (UART), serial peripheral interface (SPI) master or slave
    - Connectable to all general purpose I/O (GPIO) pins
  - Implement a combination up to 21 buttons or 4 sliders using 4 analog blocks and 3 digital blocks
  - Complex peripherals by combining blocks
- **Flexible on-chip memory**
  - 8-KB Flash /512-B SRAM
  - 50,000 erase/write cycles
  - In-system serial programming (ISSP)
  - Partial flash updates
  - Flexible protection modes
  - EEPROM emulation in flash
- **Complete development tools**
  - Free development software (PSoC Designer™)
  - Full-featured, in-circuit emulator (ICE) and programmer
  - Full-speed emulation
  - Complex breakpoint structure
  - 128-KB trace memory
- **Precision, programmable clocking**
  - Internal ±2.5% 24- / 48-MHz main oscillator<sup>[1]</sup>
  - Internal oscillator for watchdog and sleep
- **Programmable pin configurations**
  - 25-mA sink, 10-mA source on all GPIOs
  - Pull-up, pull-down, high-Z, strong, or open-drain drive modes on all GPIOs
  - Up to eight analog inputs on GPIOs
  - Configurable interrupt on all GPIOs
- **Versatile analog mux**
  - Common internal analog bus
  - Simultaneous connection of I/O combinations
  - Capacitive sensing application capability
- **Additional system resources**
  - I<sup>2</sup>C<sup>[2]</sup> master, slave, and multi-master to 400 kHz
  - Watchdog and sleep timers
  - User-configurable low-voltage detection (LVD)
  - Integrated supervisory circuit
  - On-chip precision voltage reference
- **Package options**
  - 16-pin SOIC
  - 20-pin, 28-pin, 56-pin SSOP
  - 32-pin QFN

**Errata:** For information on silicon errata, see "Errata" on page 48. Details include trigger conditions, devices affected, and proposed workaround.

### Notes

1. **Errata:** The worst case IMO frequency deviation when operated below 0 °C and above +70 °C and within the upper and lower datasheet temperature range is ±5%.
2. **Errata:** The I<sup>2</sup>C block exhibits occasional data and bus corruption errors when the I<sup>2</sup>C master initiates transactions while the device is transitioning in to or out of sleep mode.

### Logic Block Diagram



## More Information

Cypress provides a wealth of data at [www.cypress.com](http://www.cypress.com) to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article “How to Design with PSoC® 1, PowerPSoC®, and PLC – KBA88292”. Following is an abbreviated list for PSoC 1:

- Overview: PSoC Portfolio, PSoC Roadmap
- Product Selectors: [PSoC 1](#), [PSoC 3](#), [PSoC 4](#), [PSoC 5LP](#)
- In addition, PSoC Designer includes a device selection tool.
- Application notes: Cypress offers a large number of PSoC application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with PSoC 1 are:
  - [Getting Started with PSoC® 1 – AN75320](#)
  - [PSoC® 1 - Getting Started with GPIO – AN2094](#)
  - [PSoC® 1 Analog Structure and Configuration – AN74170](#)
  - [PSoC® 1 Switched Capacitor Analog Blocks – AN2041](#)
  - [Selecting Analog Ground and Reference – AN2219](#)

**Note:** For CY8C21x34B devices related Application note please click [here](#).

- Development Kits:
  - [CY3210-PSocEval1](#) supports all PSoC 1 Mixed-Signal Array families, including automotive, except CY8C25/26xxx devices. The kit includes an LCD module, potentiometer, LEDs, and breadboarding space.
  - [CY3214-PSocEvalUSB](#) features a development board for the CY8C24x94 PSoC device. Special features of the board include USB and CapSense development and debugging support.

**Note:** For CY8C21x34B devices related Development Kits please click [here](#).

The [MiniProg1](#) and [MiniProg3](#) devices provide interfaces for flash programming and debug.

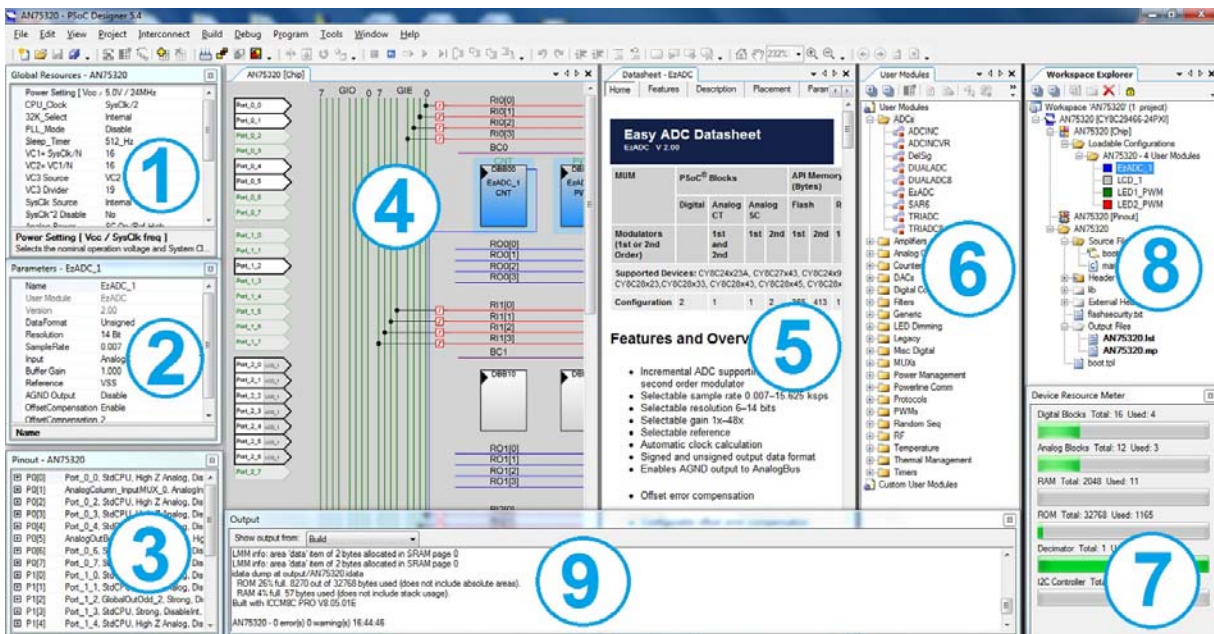
## PSoC Designer

[PSoC Designer](#) is a free Windows-based Integrated Design Environment (IDE). Develop your applications using a library of pre-characterized analog and digital peripherals in a drag-and-drop design environment. Then, customize your design leveraging the dynamically generated API libraries of code. [Figure 1](#) shows PSoC Designer windows. **Note:** This is not the default view.

1. **Global Resources** – all device hardware settings.
2. **Parameters** – the parameters of the currently selected User Modules.
3. **Pinout** – information related to device pins.
4. **Chip-Level Editor** – a diagram of the resources available on the selected chip.
5. **Datasheet** – the datasheet for the currently selected UM
6. **User Modules** – all available User Modules for the selected device.
7. **Device Resource Meter** – device resource usage for the current project configuration.
8. **Workspace** – a tree level diagram of files associated with the project.
9. **Output** – output from project build and debug operations.

**Note:** For detailed information on PSoC Designer, go to **PSoC® Designer > Help > Documentation > Designer Specific Documents > IDE User Guide**.

Figure 1. PSoC Designer Layout



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## PSoC Functional Overview

The PSoC family consists of many devices with on-chip controllers. These devices are designed to replace multiple traditional MCU-based system components with one low-cost single-chip programmable component. A PSoC device includes configurable blocks of analog and digital logic, and programmable interconnect. This architecture makes it possible for you to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast central processing unit (CPU), flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The PSoC architecture, shown in Figure 2, consists of four main areas: the core, the system resources, the digital system, and the analog system. Configurable global bus resources allow combining all of the device resources into a complete custom system. Each CY8C21x34B PSoC device includes four digital blocks and four analog blocks. Depending on the PSoC package, up to 28 GPIOs are also included. The GPIOs provide access to the global digital and analog interconnects.

### The PSoC Core

The PSoC core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and internal main oscillator (IMO) and internal low speed oscillator (ILO). The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a four-million instructions per second (MIPS) 8-bit Harvard-architecture microprocessor.

System resources provide these additional capabilities:

- Digital clocks for increased flexibility
- I<sup>2</sup>C functionality to implement an I<sup>2</sup>C master and slave
- An internal voltage reference, multi-master, that provides an absolute value of 1.3 V to a number of PSoC subsystems
- A SMP that generates normal operating voltages from a single battery cell
- Various system resets supported by the M8C

The digital system consists of an array of digital PSoC blocks that may be configured into any number of digital peripherals. The digital blocks are connected to the GPIOs through a series of global buses. These buses can route any signal to any pin, freeing designs from the constraints of a fixed peripheral controller.

The analog system consists of four analog PSoC blocks, supporting comparators, and analog-to-digital conversion up to 10 bits of precision.

## The Digital System

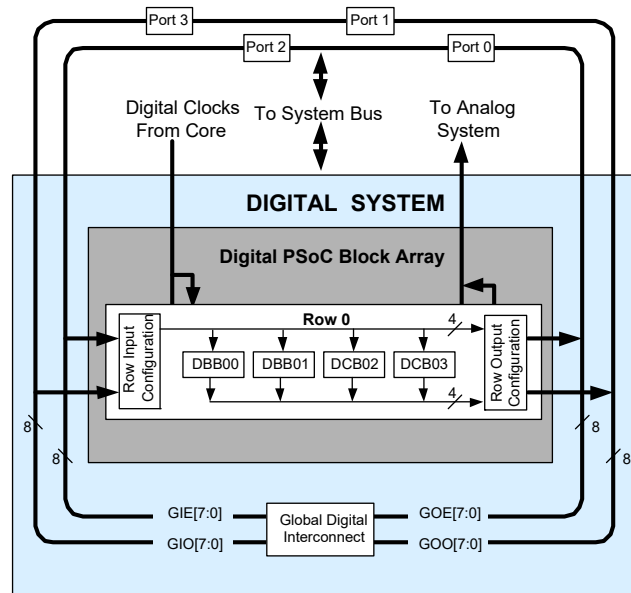
The digital system consists of four digital PSoC blocks. Each block is an 8-bit resource that is used alone or combined with other blocks to form 8-, 16-, 24-, and 32-bit peripherals, which are called user modules. Digital peripheral configurations include:

- PWMs (8- to 32-bit)
- PWMs with dead band (8- to 32-bit)
- Counters (8- to 32-bit)
- Timers (8- to 32-bit)
- UART 8- with selectable parity
- Serial peripheral interface (SPI) master and slave
- I<sup>2</sup>C slave and multi-master
- CRC/generator (8-bit)
- IrDA
- PRS generators (8-bit to 32-bit)

The digital blocks are connected to any GPIO through a series of global buses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by PSoC device family. This allows the optimum choice of system resources for your application. Family resources are shown in Table 1 on page 7.

Figure 2. Digital System Block Diagram



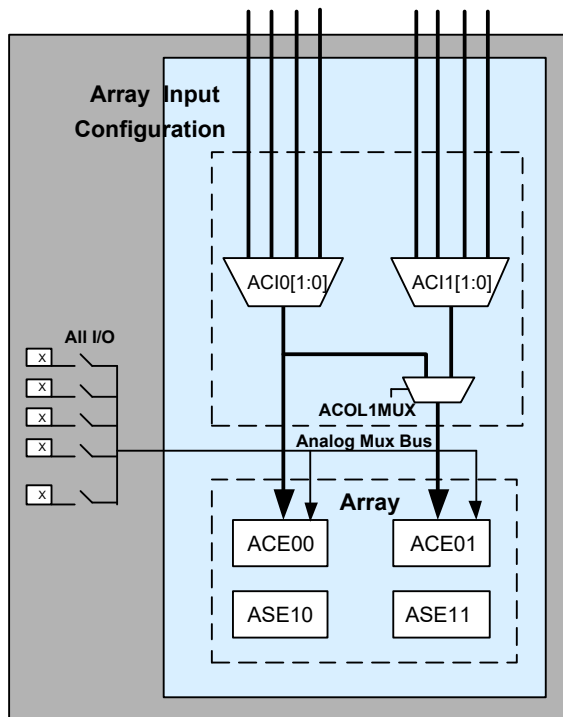
### The Analog System

The analog system consists of four configurable blocks that allow for the creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the common PSoC analog functions for this device (most available as user modules) are:

- ADCs (single or dual, with 8-bit or 10-bit resolution)
- Pin-to-pin comparator
- Single-ended comparators (up to two) with absolute (1.3 V) reference or 8-bit DAC reference
- 1.3-V reference (as a system resource)

In most PSoC devices, analog blocks are provided in columns of three, which includes one continuous time (CT) and two switched capacitor (SC) blocks. The CY8C21x34B devices provide limited functionality Type E analog blocks. Each column contains one CT Type E block and one SC Type E block. Refer to the *PSoC Technical Reference Manual* for detailed information on the CY8C21x34B's Type E analog blocks.

Figure 3. Analog System Block Diagram



### The Analog Multiplexer System

The analog mux bus can connect to every GPIO pin. Pins may be connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with comparators and analog-to-digital converters. An additional 8:1 analog input multiplexer provides a second path to bring Port 0 pins to the analog array.

Switch-control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Track pad, finger sensing
- Chip-wide mux that allows analog input from any I/O pin
- Crosspoint connection between any I/O pin combinations

### Additional System Resources

System resources, some of which are listed in the previous sections, provide additional capability useful to complete systems. Additional resources include a switch-mode pump, low-voltage detection, and power-on-reset (POR).

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks may be routed to both the digital and analog systems. Additional clocks can be generated using digital PSoC blocks as clock dividers.
- The I<sup>2</sup>C module provides 100- and 400-kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- LVD interrupts can signal the application of falling voltage levels, while the advanced POR circuit eliminates the need for a system supervisor.
- An internal 1.3-V reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch-mode pump generates normal operating voltages from a single 1.2-V battery cell, providing a low cost boost converter.
- Versatile analog multiplexer system.

## PSoC Device Characteristics

Depending on your PSoC device characteristics, the digital and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 4 analog blocks. Table 1 lists the resources available for specific PSoC device groups. The PSoC device covered by this datasheet is highlighted in Table 1.

**Table 1. PSoC Device Characteristics**

PSoC Part Number	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size	SmartSense Enabled
CY8C29x66	up to 64	4	16	up to 12	4	4	12	2K	32K	–
CY8C28xxx	up to 44	up to 3	up to 12	up to 44	up to 4	up to 6	up to 12 + 4 <sup>[3]</sup>	1K	16K	–
CY8C27x43	up to 44	2	8	up to 12	4	4	12	256	16K	–
CY8C24x94	up to 56	1	4	up to 48	2	2	6	1K	16K	–
CY8C24x23A	up to 24	1	4	up to 12	2	2	6	256	4K	–
CY8C23x33	up to 26	1	4	up to 12	2	2	4	256	8K	–
CY8C22x45	up to 38	2	8	up to 38	0	4	6 <sup>[3]</sup>	1 K	16K	–
CY8C21x45	up to 24	1	4	up to 24	0	4	6 <sup>[3]</sup>	512	8K	–
CY8C21x34	up to 28	1	4	up to 28	0	2	4 <sup>[3]</sup>	512	8K	–
CY8C21x34B	up to 28	1	4	up to 28	0	2	4 <sup>[3]</sup>	512	8K	Y
CY8C21x23	up to 16	1	4	up to 8	0	2	4 <sup>[3]</sup>	256	4K	–
CY8C20x34	up to 28	0	0	up to 28	0	0	3 <sup>[3,4]</sup>	512	8K	–
CY8C20xx6A	up to 36	0	0	up to 36	0	0	3 <sup>[3,4]</sup>	up to 2K	up to 32K	Y

### Notes

3. Limited analog functionality.
4. Two analog blocks and one CapSense®.

## Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I<sup>2</sup>C slaves and masters
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

### PSoC Designer Software Subsystems

#### *Design Entry*

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are ADCs, DACs, amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this allows you to use more than 100 percent of PSoC's resources for an application.

#### *Code Generation Tools*

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

**Assemblers.** The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and are linked with other software modules to get absolute addressing.

**C Language Compilers.** C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

#### *Debugger*

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also allows you to create a trace buffer of registers and memory locations of interest.

#### *Online Help System*

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an online support Forum to aid the designer.

#### *In-Circuit Emulator*

A low-cost, high-functionality [in-circuit emulator \(ICE\)](#) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.



## Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and by lowering inventory costs. These configurable resources, called PSoC Blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is summarized in four steps:

1. Select [User Modules](#).
2. Configure User Modules.
3. Organize and Connect.
4. Generate, Verify, and Debug.

### Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

### Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each 8 bits of resolution. The user module parameters permit you to establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These [user module datasheets](#) explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information you may need to successfully implement your design.

### Organize and Connect

You build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. You perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

## Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, you perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides application programming interfaces (APIs) with high-level functions to control and respond to hardware events at run-time and interrupt service routines that you can adapt as needed.

A complete code development environment allows you to develop and customize your applications in either C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer’s debugger (access by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer and allows you to define complex breakpoint events. These include monitoring address and data bus values, memory locations, and external signals.

### SmartSense

A key differentiation between the current offering of CY8C21x34 and CY8C21x34B, is the addition of the SmartSense user module in the ‘B’ version.

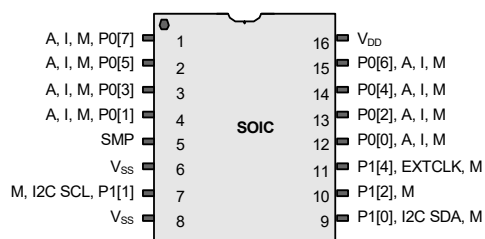
SmartSense is an innovative solution from Cypress that eliminates the manual tuning process from CapSense applications. This solution is easy to use and provides robust noise immunity. It is the only auto-tuning solution that establishes, monitors and maintains all required tuning parameters. SmartSense allows engineers to go from prototyping to mass production without re-tuning for manufacturing variations in PCB and/or overlay material properties.

## Pin Information

The CY8C21x34B PSoC device is available in a variety of packages which are listed in the following tables. Every port pin (labeled with a "P") is capable of Digital I/O and connection to the common analog bus. However, V<sub>SS</sub>, V<sub>DD</sub>, SMP, and XRES are not capable of Digital I/O.

### 16-pin Part Pinout

**Figure 4. CY8C21234B 16-pin PSoC Device**



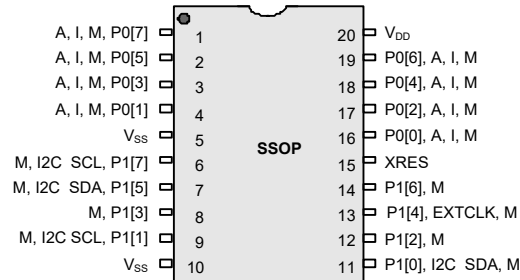
**Table 2. Pin Definitions – CY8C21234B 16-pin (SOIC)**

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P0[7]	Analog column mux input
2	I/O	I, M	P0[5]	Analog column mux input
3	I/O	I, M	P0[3]	Analog column mux input, integrating input
4	I/O	I, M	P0[1]	Analog column mux input, integrating input
5	Power		SMP	Switch-mode pump (SMP) connection to required external components
6	Power		V <sub>SS</sub>	Ground connection
7	I/O	M	P1[1]	I <sup>2</sup> C serial clock (SCL), ISSP-SCLK <sup>[5]</sup>
8	Power		V <sub>SS</sub>	Ground connection
9	I/O	M	P1[0]	I <sup>2</sup> C serial data (SDA), ISSP-SDATA <sup>[5]</sup>
10	I/O	M	P1[2]	
11	I/O	M	P1[4]	Optional external clock input (EXTCLK)
12	I/O	I, M	P0[0]	Analog column mux input
13	I/O	I, M	P0[2]	Analog column mux input
14	I/O	I, M	P0[4]	Analog column mux input
15	I/O	I, M	P0[6]	Analog column mux input
16	Power		V <sub>DD</sub>	Supply voltage

**LEGEND** A = Analog, I = Input, O = Output, and M = Analog Mux Input.

**Note**

5. These are the ISSP pins, which are not High Z at POR. See the *PSoC Technical Reference Manual* for details.

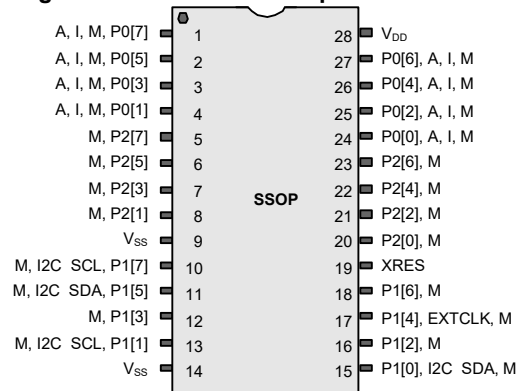
**20-pin Part Pinout**
**Figure 5. CY8C21334B 20-pin PSoC Device**

**Table 3. Pin Definitions – CY8C21334B 20-pin (SSOP)**

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P0[7]	Analog column mux input
2	I/O	I, M	P0[5]	Analog column mux input
3	I/O	I, M	P0[3]	Analog column mux input, integrating input
4	I/O	I, M	P0[1]	Analog column mux input, integrating input
5	Power		V <sub>SS</sub>	Ground connection
6	I/O	M	P1[7]	I <sup>2</sup> C SCL
7	I/O	M	P1[5]	I <sup>2</sup> C SDA
8	I/O	M	P1[3]	
9	I/O	M	P1[1]	I <sup>2</sup> C SCL, ISSP-SCLK <sup>[6]</sup>
10	Power		V <sub>SS</sub>	Ground connection.
11	I/O	M	P1[0]	I <sup>2</sup> C SDA, ISSP-SDATA <sup>[6]</sup>
12	I/O	M	P1[2]	
13	I/O	M	P1[4]	Optional external clock input (EXTCLK)
14	I/O	M	P1[6]	
15	Input		XRES	Active high external reset with internal pull-down
16	I/O	I, M	P0[0]	Analog column mux input
17	I/O	I, M	P0[2]	Analog column mux input
18	I/O	I, M	P0[4]	Analog column mux input
19	I/O	I, M	P0[6]	Analog column mux input
20	Power		V <sub>DD</sub>	Supply voltage

**LEGEND** A = Analog, I = Input, O = Output, and M = Analog Mux Input.

**Note**

6. These are the ISSP pins, which are not High Z at POR. See the *PSoC Technical Reference Manual* for details.

**28-pin Part Pinout**
**Figure 6. CY8C21534B 28-pin PSOC Device**

**Table 4. Pin Definitions – CY8C21534B 28-pin (SSOP)**

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P0[7]	Analog column mux input
2	I/O	I, M	P0[5]	Analog column mux input and column output
3	I/O	I, M	P0[3]	Analog column mux input and column output, integrating input
4	I/O	I, M	P0[1]	Analog column mux input, integrating input
5	I/O	M	P2[7]	
6	I/O	M	P2[5]	
7	I/O	I, M	P2[3]	Direct switched capacitor block input
8	I/O	I, M	P2[1]	Direct switched capacitor block input
9	Power		V <sub>SS</sub>	Ground connection
10	I/O	M	P1[7]	I <sup>2</sup> C SCL
11	I/O	M	P1[5]	I <sup>2</sup> C SDA
12	I/O	M	P1[3]	
13	I/O	M	P1[1]	I <sup>2</sup> C SCL, ISSP-SCLK <sup>7</sup>
14	Power		V <sub>SS</sub>	Ground connection
15	I/O	M	P1[0]	I <sup>2</sup> C SDA, ISSP-SDATA <sup>7</sup>
16	I/O	M	P1[2]	
17	I/O	M	P1[4]	Optional external clock input (EXTCLK)
18	I/O	M	P1[6]	
19	Input		XRES	Active high external reset with internal pull-down
20	I/O	I, M	P2[0]	Direct switched capacitor block input
21	I/O	I, M	P2[2]	Direct switched capacitor block input
22	I/O	M	P2[4]	
23	I/O	M	P2[6]	
24	I/O	I, M	P0[0]	Analog column mux input
25	I/O	I, M	P0[2]	Analog column mux input
26	I/O	I, M	P0[4]	Analog column mux input
27	I/O	I, M	P0[6]	Analog column mux input
28	Power		V <sub>DD</sub>	Supply voltage

**LEGEND** A: Analog, I: Input, O = Output, and M = Analog Mux Input.

**Note**

7. These are the ISSP pins, which are not high Z at POR. See the *PSOC Technical Reference Manual* for details.

32-pin Part Pinout

Figure 7. CY8C21434B 32-pin PSoC Device

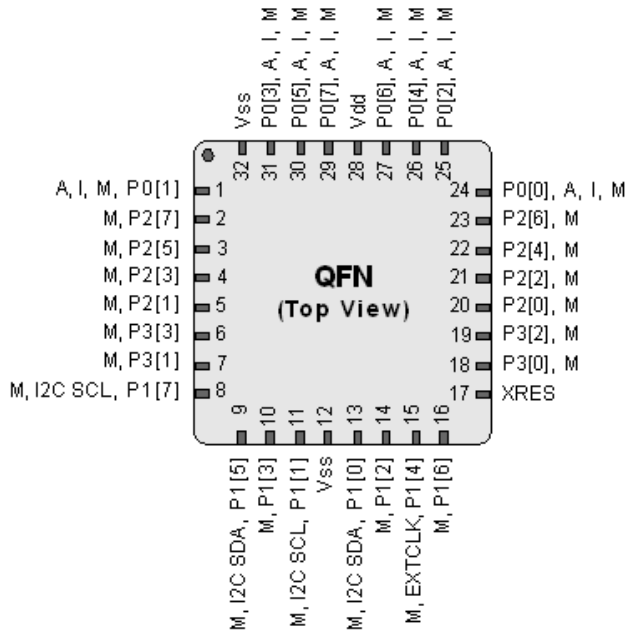


Figure 8. CY8C21634B 32-pin PSoC Device

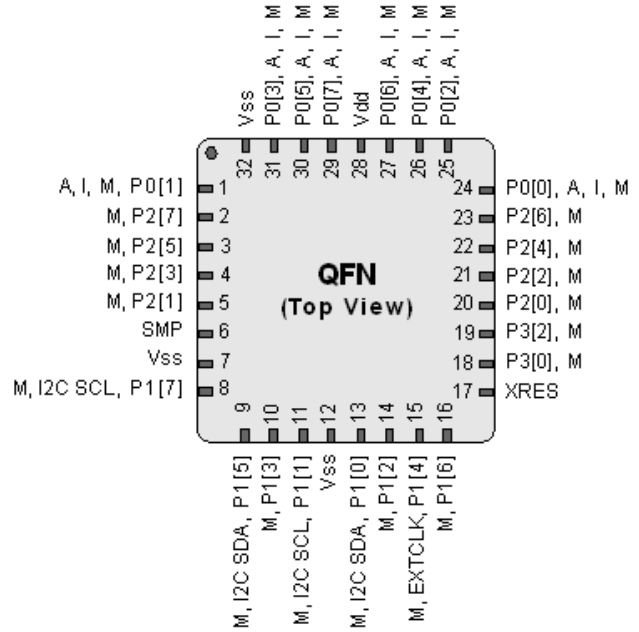


Figure 9. CY8C21434B 32-pin Sawn PSoC Device Sawn

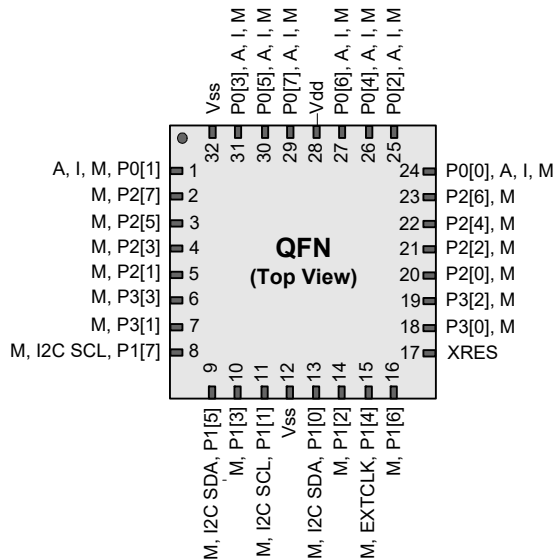
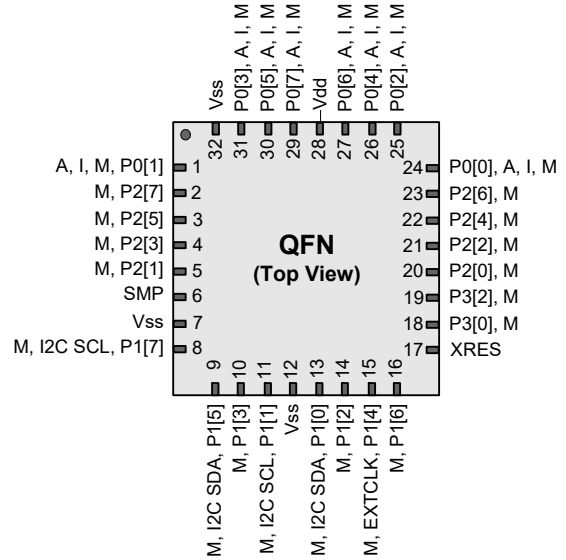


Figure 10. CY8C21634B 32-pin Sawn PSoC Device Sawn



**Table 5. Pin Definitions - CY8C21434B/CY8C21634B 32-pin (QFN)<sup>[8]</sup>**

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I, M	P0[1]	Analog column mux input, integrating input
2	I/O	M	P2[7]	
3	I/O	M	P2[5]	
4	I/O	M	P2[3]	
5	I/O	M	P2[1]	
6	I/O	M	P3[3]	In CY8C21434B part
6	Power		SMP	SMP connection to required external components in CY8C21634B part
7	I/O	M	P3[1]	In CY8C21434B part
7	Power		V <sub>SS</sub>	Ground connection in CY8C21634B part
8	I/O	M	P1[7]	I <sup>2</sup> C SCL
9	I/O	M	P1[5]	I <sup>2</sup> C SDA
10	I/O	M	P1[3]	
11	I/O	M	P1[1]	I <sup>2</sup> C SCL, ISSP-SCLK <sup>[9]</sup>
12	Power		V <sub>SS</sub>	Ground connection
13	I/O	M	P1[0]	I <sup>2</sup> C SDA, ISSP-SDATA <sup>[9]</sup>
14	I/O	M	P1[2]	
15	I/O	M	P1[4]	Optional external clock input (EXTCLK)
16	I/O	M	P1[6]	
17	Input		XRES	Active high external reset with internal pull-down
18	I/O	M	P3[0]	
19	I/O	M	P3[2]	
20	I/O	M	P2[0]	
21	I/O	M	P2[2]	
22	I/O	M	P2[4]	
23	I/O	M	P2[6]	
24	I/O	I, M	P0[0]	Analog column mux input
25	I/O	I, M	P0[2]	Analog column mux input
26	I/O	I, M	P0[4]	Analog column mux input
27	I/O	I, M	P0[6]	Analog column mux input
28	Power		V <sub>DD</sub>	Supply voltage
29	I/O	I, M	P0[7]	Analog column mux input
30	I/O	I, M	P0[5]	Analog column mux input
31	I/O	I, M	P0[3]	Analog column mux input, integrating input
32	Power		V <sub>SS</sub>	Ground connection

**LEGEND** A = Analog, I = Input, O = Output, and M = Analog Mux Input.

**Notes**

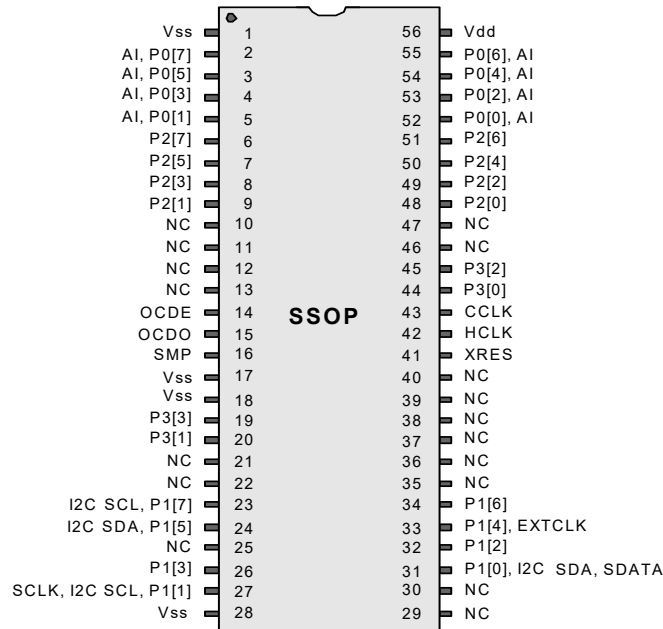
- The center pad on the QFN package must be connected to ground (V<sub>SS</sub>) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
- These are the ISSP pins, which are not high Z at POR. See the *PSoC Technical Reference Manual* for details.

**56-pin Part Pinout**

The 56-Pin SSOP part is for the CY8C21001 on-chip debug (OCD) PSoC device.

**Note** This part is only used for in-circuit debugging. It is NOT available for production.

**Figure 11. CY8C21001 56-pin PSoC Device**



**Table 6. Pin Definitions – CY8C21001 56-pin (SSOP)**

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	Power		V <sub>SS</sub>	Ground connection
2	I/O	I	P0[7]	Analog column mux input
3	I/O	I	P0[5]	Analog column mux input and column output
4	I/O	I	P0[3]	Analog column mux input and column output
5	I/O	I	P0[1]	Analog column mux input
6	I/O		P2[7]	
7	I/O		P2[5]	
8	I/O	I	P2[3]	Direct switched capacitor block input
9	I/O	I	P2[1]	Direct switched capacitor block input
10			NC	No connection
11			NC	No connection
12			NC	No connection
13			NC	No connection
14	OCD		OCDE	OCD even data I/O
15	OCD		OCDO	OCD odd data output
16	Power		SMP	SMP connection to required external components
17	Power		V <sub>SS</sub>	Ground connection
18	Power		V <sub>SS</sub>	Ground connection

**Table 6. Pin Definitions – CY8C21001 56-pin (SSOP) (continued)**

Pin No.	Type		Pin Name	Description
	Digital	Analog		
19	I/O		P3[3]	
20	I/O		P3[1]	
21			NC	No connection
22			NC	No connection
23	I/O		P1[7]	I <sup>2</sup> C SCL
24	I/O		P1[5]	I <sup>2</sup> C SDA
25			NC	No connection
26	I/O		P1[3]	I <sub>FMTEST</sub>
27	I/O		P1[1]	I <sup>2</sup> C SCL, ISSP-SCLK <sup>[10]</sup>
28	Power		V <sub>SS</sub>	Ground connection
29			NC	No connection
30			NC	No connection
31	I/O		P1[0]	I <sup>2</sup> C SDA, ISSP-SDATA <sup>[10]</sup>
32	I/O		P1[2]	V <sub>FMTEST</sub>
33	I/O		P1[4]	Optional external clock input (EXTCLK)
34	I/O		P1[6]	
35			NC	No connection
36			NC	No connection
37			NC	No connection
38			NC	No connection
39			NC	No connection
40			NC	No connection
41	Input		XRES	Active high external reset with internal pull-down
42	OCD		HCLK	OCD high-speed clock output
43	OCD		CCLK	OCD CPU clock output
44	I/O		P3[0]	
45	I/O		P3[2]	
46			NC	No connection
47			NC	No connection
48	I/O	I	P2[0]	
49	I/O	I	P2[2]	
50	I/O		P2[4]	
51	I/O		P2[6]	
52	I/O	I	P0[0]	Analog column mux input
53	I/O	I	P0[2]	Analog column mux input and column output
54	I/O	I	P0[4]	Analog column mux input and column output
55	I/O	I	P0[6]	Analog column mux input
56	Power		V <sub>DD</sub>	Supply voltage

**LEGEND:** A = Analog, I = Input, O = Output, and OCD = On-Chip Debug.

**Note**

10. These are the ISSP pins, which are not High Z at POR. See the [PSoC Technical Reference Manual](#) for details.



## Register Reference

This chapter lists the registers of the CY8C21x34B PSoC device. For detailed register information, see the [PSoC Technical Reference Manual](#).

### Register Conventions

The register conventions specific to this section are listed in [Table 7](#).

**Table 7. Register Conventions**

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

### Register Mapping Tables

The PSoC device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks, Bank 0 and Bank 1. The XOI bit in the Flag register (CPU\_F) determines which bank the user is currently in. When the XOI bit is set to 1, the user is in Bank 1.

**Note** In the following register mapping tables, blank fields are reserved and must not be accessed.

Table 8. Register Map 0 Table: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASE10CR0	80	RW		C0	
PRT0IE	01	RW		41			81			C1	
PRT0GS	02	RW		42			82			C2	
PRT0DM2	03	RW		43			83			C3	
PRT1DR	04	RW		44		ASE11CR0	84	RW		C4	
PRT1IE	05	RW		45			85			C5	
PRT1GS	06	RW		46			86			C6	
PRT1DM2	07	RW		47			87			C7	
PRT2DR	08	RW		48			88			C8	
PRT2IE	09	RW		49			89			C9	
PRT2GS	0A	RW		4A			8A			CA	
PRT2DM2	0B	RW		4B			8B			CB	
PRT3DR	0C	RW		4C			8C			CC	
PRT3IE	0D	RW		4D			8D			CD	
PRT3GS	0E	RW		4E			8E			CE	
PRT3DM2	0F	RW		4F			8F			CF	
	10			50			90		CUR_PP	D0	RW
	11			51			91		STK_PP	D1	RW
	12			52			92			D2	
	13			53			93		IDX_PP	D3	RW
	14			54			94		MVR_PP	D4	RW
	15			55			95		MVW_PP	D5	RW
	16			56			96		I2C_CFG	D6	RW
	17			57			97		I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99		I2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W	AMUXCFG	61	RW		A1		INT_MSK1	E1	RW
DBB00DR2	22	RW	PWM_CR	62	RW		A2		INT_VC	E2	RC
DBB00CR0	23	#		63			A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4			E4	
DBB01DR1	25	W		65			A5			E5	
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#	ADC0_CR	68	#		A8			E8	
DCB02DR1	29	W	ADC1_CR	69	#		A9			E9	
DCB02DR2	2A	RW		6A			AA			EA	
DCB02CR0	2B	#		6B			AB			EB	
DCB03DR0	2C	#	TMP_DR0	6C	RW		AC			EC	
DCB03DR1	2D	W	TMP_DR1	6D	RW		AD			ED	
DCB03DR2	2E	RW	TMP_DR2	6E	RW		AE			EE	
DCB03CR0	2F	#	TMP_DR3	6F	RW		AF			EF	
	30			70		RDI0RI	B0	RW		F0	
	31			71		RDI0SYN	B1	RW		F1	
	32		ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34			74		RDI0LT1	B4	RW		F4	
	35			75		RDI0RO0	B5	RW		F5	
	36		ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACE01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD		DAC_D	FD	RW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are reserved and must not be accessed.

# Access is bit specific.

Table 9. Register Map 1 Table: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASE10CR0	80	RW		C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43			83			C3	
PRT1DM0	04	RW		44		ASE11CR0	84	RW		C4	
PRT1DM1	05	RW		45			85			C5	
PRT1IC0	06	RW		46			86			C6	
PRT1IC1	07	RW		47			87			C7	
PRT2DM0	08	RW		48			88			C8	
PRT2DM1	09	RW		49			89			C9	
PRT2IC0	0A	RW		4A			8A			CA	
PRT2IC1	0B	RW		4B			8B			CB	
PRT3DM0	0C	RW		4C			8C			CC	
PRT3DM1	0D	RW		4D			8D			CD	
PRT3IC0	0E	RW		4E			8E			CE	
PRT3IC1	0F	RW		4F			8F			CF	
	10			50			90		GDI_O_IN	D0	RW
	11			51			91		GDI_E_IN	D1	RW
	12			52			92		GDI_O_OU	D2	RW
	13			53			93		GDI_E_OU	D3	RW
	14			54			94			D4	
	15			55			95			D5	
	16			56			96			D6	
	17			57			97			D7	
	18			58			98		MUX_CR0	D8	RW
	19			59			99		MUX_CR1	D9	RW
	1A			5A			9A		MUX_CR2	DA	RW
	1B			5B			9B		MUX_CR3	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW	CMP_GO_EN	64	RW		A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5		ADC0_TR	E5	RW
DBB01OU	26	RW	AMD_CR1	66	RW		A6		ADC1_TR	E6	RW
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68			A8		IMO_TR	E8	W
DCB02IN	29	RW		69			A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B		CLK_CR3	6B	RW		AB		ECO_TR	EB	W
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30			70		RD10RI	B0	RW		F0	
	31			71		RD10SYN	B1	RW		F1	
	32		ACE00CR1	72	RW	RD10IS	B2	RW		F2	
	33		ACE00CR2	73	RW	RD10LT0	B3	RW		F3	
	34			74		RD10LT1	B4	RW		F4	
	35			75		RD10RO0	B5	RW		F5	
	36		ACE01CR1	76	RW	RD10RO1	B6	RW		F6	
	37		ACE01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA		FLS_PR1	FA	RW
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD		DAC_CR	FD	RW
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are reserved and must not be accessed.

# Access is bit specific.

## Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C21x34B PSoC device. For up-to-date electrical specifications, visit the Cypress web site at <http://www.cypress.com>.

Specifications are valid for  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$  and  $T_J \leq 100\text{ }^{\circ}\text{C}$  as specified, except where noted.

Refer to [Table 23 on page 27](#) for the electrical specifications for the IMO using SLIMO mode.

Figure 12. Voltage versus CPU Frequency

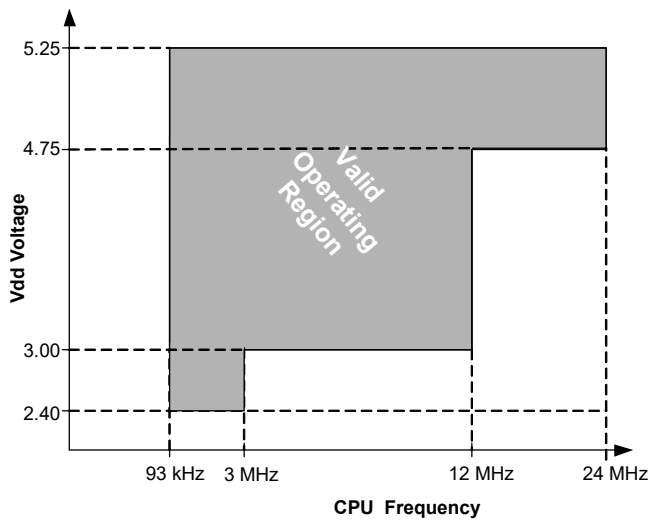
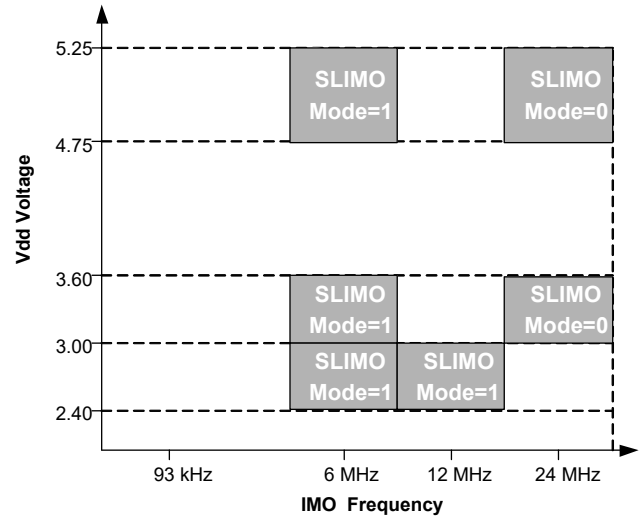


Figure 13. IMO Frequency Trim Options



## Absolute Maximum Ratings

Table 10. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T <sub>STG</sub>	Storage temperature	-55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 65 °C degrade reliability.
T <sub>BAKETEMP</sub>	Bake temperature	-	125	See package label	°C	
t <sub>BAKETIME</sub>	Bake time	See package label	-	72	Hours	
T <sub>A</sub>	Ambient temperature with power applied	-40	-	+85	°C	
V <sub>DD</sub>	Supply voltage on V <sub>DD</sub> relative to V <sub>SS</sub>	-0.5	-	+6.0	V	
V <sub>IO</sub>	DC input voltage	V <sub>SS</sub> - 0.5	-	V <sub>DD</sub> + 0.5	V	
V <sub>IOZ</sub>	DC voltage applied to tri-state	V <sub>SS</sub> - 0.5	-	V <sub>DD</sub> + 0.5	V	
I <sub>MIO</sub>	Maximum current into any port pin	-25	-	+50	mA	
ESD	Electrostatic discharge voltage	2000	-	-	V	Human body model ESD.
LU	Latch-up current	-	-	200	mA	

## Operating Temperature

**Table 11. Operating Temperature**

Symbol	Description	Min	Typ	Max	Units	Notes
T <sub>A</sub>	Ambient temperature	-40	-	+85	°C	
T <sub>J</sub>	Junction temperature	-40	-	+100	°C	The temperature rise from ambient to junction is package specific. See <a href="#">Table 36 on page 38</a> . You must limit the power consumption to comply with this requirement.

## DC Electrical Characteristics

### DC Chip-Level Specifications

[Table 12](#) lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40\text{ °C} \leq T_A \leq 85\text{ °C}$ , 3.0 V to 3.6 V and  $-40\text{ °C} \leq T_A \leq 85\text{ °C}$ , or 2.4 V to 3.0 V and  $-40\text{ °C} \leq T_A \leq 85\text{ °C}$ , respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 12. DC Chip-level Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
V <sub>DD</sub>	Supply voltage	2.40	-	5.25	V	See <a href="#">Table 20 on page 25</a>
I <sub>DD</sub>	Supply current, IMO = 24 MHz	-	3	4	mA	Conditions are V <sub>DD</sub> = 5.0 V, T <sub>A</sub> = 25 °C, CPU = 3 MHz, 48 MHz disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz
I <sub>DD3</sub>	Supply current, IMO = 6 MHz using SLIMO mode.	-	1.2	2	mA	Conditions are V <sub>DD</sub> = 3.3 V, T <sub>A</sub> = 25 °C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz, VC2 = 23.4 kHz, VC3 = 0.091 kHz
I <sub>DD27</sub>	Supply current, IMO = 6 MHz using SLIMO mode.	-	1.1	1.5	mA	Conditions are V <sub>DD</sub> = 2.55 V, T <sub>A</sub> = 25 °C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz, VC2 = 23.4 kHz, VC3 = 0.091 kHz
I <sub>SB27</sub>	Sleep (mode) current with POR, LVD, sleep timer, WDT, and internal slow oscillator active. Mid temperature range.	-	2.6	4	μA	V <sub>DD</sub> = 2.55 V, 0 °C ≤ T <sub>A</sub> ≤ 40 °C
I <sub>SB</sub>	Sleep (mode) current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active.	-	2.8	5	μA	V <sub>DD</sub> = 3.3 V, -40 °C ≤ T <sub>A</sub> ≤ 85 °C
V <sub>REF</sub>	Reference voltage (Bandgap)	1.28	1.30	1.32	V	Trimmed for appropriate V <sub>DD</sub> V <sub>DD</sub> = 3.0 V to 5.25 V
V <sub>REF27</sub>	Reference voltage (Bandgap)	1.16	1.30	1.33	V	Trimmed for appropriate V <sub>DD</sub> V <sub>DD</sub> = 2.4 V to 3.0 V
AGND	Analog ground	V <sub>REF</sub> - 0.003	V <sub>REF</sub>	V <sub>REF</sub> + 0.003	V	

**DC General-Purpose I/O Specifications**

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , 3.0 V to 3.6 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , or 2.4 V to 3.0 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , respectively. Typical parameters are measured at 5 V, 3.3 V, and 2.7 V at 25 °C and are for design guidance only.

**Table 13. 5 V and 3.3 V DC GPIO Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
R <sub>PU</sub>	Pull-up resistor	4	5.6	8	kΩ	
R <sub>PD</sub>	Pull-down resistor	4	5.6	8	kΩ	
V <sub>OH</sub>	High output level	V <sub>DD</sub> - 1.0	–	–	V	I <sub>OH</sub> = 10 mA, V <sub>DD</sub> = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5]))
V <sub>OL</sub>	Low output level	–	–	0.75	V	I <sub>OL</sub> = 25 mA, V <sub>DD</sub> = 4.75 to 5.25 V (8 total loads, 4 on even port pins (for example, P0[2], P1[4]), 4 on odd port pins (for example, P0[3], P1[5]))
I <sub>OH</sub>	High level source current	10	–	–	mA	V <sub>OH</sub> = V <sub>DD</sub> - 1.0 V, see the limitations of the total current in the note for V <sub>OH</sub>
I <sub>OL</sub>	Low level sink current	25	–	–	mA	V <sub>OL</sub> = 0.75 V, see the limitations of the total current in the note for V <sub>OL</sub>
V <sub>IL</sub>	Input low level	–	–	0.8	V	V <sub>DD</sub> = 3.0 to 5.25
V <sub>IH</sub>	Input high level	2.1	–	–	V	V <sub>DD</sub> = 3.0 to 5.25
V <sub>H</sub>	Input hysteresis	–	60	–	mV	
I <sub>IL</sub>	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 μA
C <sub>IN</sub>	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent Temp = 25 °C
C <sub>OUT</sub>	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent Temp = 25 °C

**Table 14. 2.7 V DC GPIO Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
R <sub>PU</sub>	Pull-up resistor	4	5.6	8	kΩ	
R <sub>PD</sub>	Pull-down resistor	4	5.6	8	kΩ	
V <sub>OH</sub>	High output level	V <sub>DD</sub> - 0.4	–	–	V	I <sub>OH</sub> = 2.5 mA (6.25 Typ), V <sub>DD</sub> = 2.4 to 3.0 V (16 mA maximum, 50 mA Typ combined I <sub>OH</sub> budget)
V <sub>OL</sub>	Low output level	–	–	0.75	V	I <sub>OL</sub> = 10 mA, V <sub>DD</sub> = 2.4 to 3.0 V (90 mA maximum combined I <sub>OL</sub> budget)
I <sub>OH</sub>	High level source current	2.5	–	–	mA	V <sub>OH</sub> = V <sub>DD</sub> - 0.4 V, see the limitations of the total current in the note for V <sub>OH</sub>
I <sub>OL</sub>	Low level sink current	10	–	–	mA	V <sub>OL</sub> = 0.75 V, see the limitations of the total current in the note for V <sub>OL</sub>
V <sub>IL</sub>	Input low level	–	–	0.75	V	V <sub>DD</sub> = 2.4 to 3.0
V <sub>IH</sub>	Input high level	2.0	–	–	V	V <sub>DD</sub> = 2.4 to 3.0
V <sub>H</sub>	Input hysteresis	–	90	–	mV	
I <sub>IL</sub>	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 μA
C <sub>IN</sub>	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent Temp = 25 °C
C <sub>OUT</sub>	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent Temp = 25 °C

**DC Operational Amplifier Specifications**

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , 3.0 V to 3.6 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , or 2.4 V to 3.0 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 15. 5 V DC Operational Amplifier Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
$V_{OSOA}$	Input offset voltage (absolute value)	–	2.5	15	mV	
$TCV_{OSOA}$	Average input offset voltage drift	–	10	–	$\mu\text{V}/^{\circ}\text{C}$	
$I_{EBOA}$	Input leakage current (Port 0 analog pins 7-to-1)	–	200	–	pA	Gross tested to 1 $\mu\text{A}$
$I_{EBOA00}$	Input leakage current (Port 0, Pin 0 analog pin)	–	50	–	nA	Gross tested to 1 $\mu\text{A}$
$C_{INOA}$	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
$V_{CMOA}$	Common mode voltage range	0.0	–	$V_{DD} - 1.0$	V	
$G_{OLOA}$	Open loop gain	–	80	–	dB	
$I_{SOA}$	Amplifier supply current	–	10	30	$\mu\text{A}$	

**Table 16. 3.3 V DC Operational Amplifier Specifications**

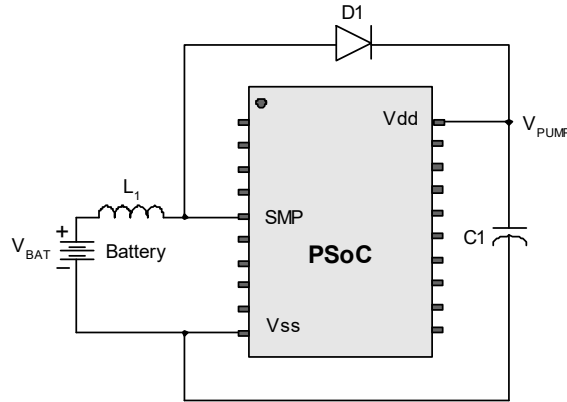
Symbol	Description	Min	Typ	Max	Units	Notes
$V_{OSOA}$	Input offset voltage (absolute value)	–	2.5	15	mV	
$TCV_{OSOA}$	Average input offset voltage drift	–	10	–	$\mu\text{V}/^{\circ}\text{C}$	
$I_{EBOA}$	Input leakage current (Port 0 analog pins)	–	200	–	pA	Gross tested to 1 $\mu\text{A}$
$I_{EBOA00}$	Input leakage current (Port 0, Pin 0 analog pin)	–	50	–	nA	Gross tested to 1 $\mu\text{A}$
$C_{INOA}$	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
$V_{CMOA}$	Common mode voltage range	0	–	$V_{DD} - 1.0$	V	
$G_{OLOA}$	Open loop gain	–	80	–	dB	
$I_{SOA}$	Amplifier supply current	–	10	30	$\mu\text{A}$	

**Table 17. 2.7 V DC Operational Amplifier Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
$V_{OSOA}$	Input offset voltage (absolute value)	–	2.5	15	mV	
$TCV_{OSOA}$	Average input offset voltage drift	–	10	–	$\mu\text{V}/^{\circ}\text{C}$	
$I_{EBOA}$	Input leakage current (Port 0 analog pins)	–	200	–	pA	Gross tested to 1 $\mu\text{A}$
$I_{EBOA00}$	Input leakage current (Port 0, Pin 0 analog pin)	–	50	–	nA	Gross tested to 1 $\mu\text{A}$
$C_{INOA}$	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C
$V_{CMOA}$	Common mode voltage range	0	–	$V_{DD} - 1.0$	V	
$G_{OLOA}$	Open loop gain	–	80	–	dB	
$I_{SOA}$	Amplifier supply current	–	10	30	$\mu\text{A}$	

**DC Switch Mode Pump Specifications**

Table 18 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , 3.0 V to 3.6 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , or 2.4 V to 3.0 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Figure 14. Basic Switch Mode Pump Circuit**

**Table 18. DC Switch Mode Pump (SMP) Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
$V_{PUMP5V}$	5 V output voltage from pump	4.75	5.0	5.25	V	Configured as in Note 11 Average, neglecting ripple SMP trip voltage is set to 5.0 V
$V_{PUMP3V}$	3.3 V output voltage from pump	3.00	3.25	3.60	V	Configured as in Note 11 Average, neglecting ripple. SMP trip voltage is set to 3.25 V
$V_{PUMP2V}$	2.6 V output voltage from pump	2.45	2.55	2.80	V	Configured as in Note 11 Average, neglecting ripple. SMP trip voltage is set to 2.55 V
$I_{PUMP}$	Available output current $V_{BAT} = 1.8\text{ V}, V_{PUMP} = 5.0\text{ V}$ $V_{BAT} = 1.5\text{ V}, V_{PUMP} = 3.25\text{ V}$ $V_{BAT} = 1.3\text{ V}, V_{PUMP} = 2.55\text{ V}$	5 8 8	– – –	– – –	mA mA mA	Configured as in Note 11 SMP trip voltage is set to 5.0 V SMP trip voltage is set to 3.25 V SMP trip voltage is set to 2.55 V
$V_{BAT5V}$	Input voltage range from battery	1.8	–	5.0	V	Configured as in Note 11 SMP trip voltage is set to 5.0 V
$V_{BAT3V}$	Input voltage range from battery	1.0	–	3.3	V	Configured as in Note 11 SMP trip voltage is set to 3.25 V
$V_{BAT2V}$	Input voltage range from battery	1.0	–	2.8	V	Configured as in Note 11 SMP trip voltage is set to 2.55 V
$V_{BATSTART}$	Minimum input voltage from battery to start pump	1.2	–	–	V	Configured as in Note 11 $0\text{ }^{\circ}\text{C} \leq T_A \leq 100$ . 1.25 V at $T_A = -40\text{ }^{\circ}\text{C}$
$\Delta V_{PUMP\_Line}$	Line regulation (over $V_i$ range)	–	5	–	% $V_O$	Configured as in Note 11 $V_O$ is the “ $V_{DD}$ Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 20 on page 25
$\Delta V_{PUMP\_Load}$	Load regulation	–	5	–	% $V_O$	Configured as in Note 11 $V_O$ is the “ $V_{DD}$ Value for PUMP Trip” specified by the VM[2:0] setting in the DC POR and LVD Specification, Table 20 on page 25
$\Delta V_{PUMP\_Ripple}$	Output voltage ripple (depends on cap/load)	–	100	–	mVpp	Configured as in Note 11 Load is 5 mA

**Note**

11.  $L_1 = 2\text{ mH}$  inductor,  $C_1 = 10\text{ mF}$  capacitor,  $D_1 =$  Schottky diode. See Figure 14.



**Table 18. DC Switch Mode Pump (SMP) Specifications (continued)**

Symbol	Description	Min	Typ	Max	Units	Notes
E <sub>3</sub>	Efficiency	35	50	–	%	Configured as in Note 11 Load is 5 mA. SMP trip voltage is set to 3.25 V
E <sub>2</sub>	Efficiency	35	80	–	%	For I <sub>load</sub> = 1 mA, V <sub>PUMP</sub> = 2.55 V, V <sub>BAT</sub> = 1.3 V, 10 μH inductor, 1 μF capacitor, and Schottky diode
F <sub>PUMP</sub>	Switching frequency	–	1.3	–	MHz	
DC <sub>PUMP</sub>	Switching duty cycle	–	50	–	%	

**DC Analog Mux Bus Specifications**

Table 19 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T<sub>A</sub> ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T<sub>A</sub> ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T<sub>A</sub> ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 19. DC Analog Mux Bus Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
R <sub>SW</sub>	Switch resistance to common analog bus	–	–	400 800	Ω	V <sub>DD</sub> ≥ 2.7 V 2.4 V ≤ V <sub>DD</sub> ≤ 2.7 V
R <sub>VDD</sub>	Resistance of initialization switch to V <sub>DD</sub>	–	–	800	Ω	

**DC POR and LVD Specifications**

Table 20 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T<sub>A</sub> ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T<sub>A</sub> ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T<sub>A</sub> ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 20. DC POR and LVD Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
V <sub>PPOR0</sub>	V <sub>DD</sub> value for PPOR trip PORLEV[1:0] = 00b	–	2.36	2.40	V	V <sub>DD</sub> must be greater than or equal to 2.5 V during startup, the reset from the XRES pin, or reset from watchdog
V <sub>PPOR1</sub>	PORLEV[1:0] = 01b	–	2.82	2.95	V	
V <sub>PPOR2</sub>	PORLEV[1:0] = 10b	–	4.55	4.70	V	
V <sub>LVD0</sub>	V <sub>DD</sub> value for LVD trip VM[2:0] = 000b	2.40	2.45	2.51 <sup>[12]</sup>	V	
V <sub>LVD1</sub>	VM[2:0] = 001b	2.85	2.92	2.99 <sup>[13]</sup>	V	
V <sub>LVD2</sub>	VM[2:0] = 010b	2.95	3.02	3.09	V	
V <sub>LVD3</sub>	VM[2:0] = 011b	3.06	3.13	3.20	V	
V <sub>LVD4</sub>	VM[2:0] = 100b	4.37	4.48	4.55	V	
V <sub>LVD5</sub>	VM[2:0] = 101b	4.50	4.64	4.75	V	
V <sub>LVD6</sub>	VM[2:0] = 110b	4.62	4.73	4.83	V	
V <sub>LVD7</sub>	VM[2:0] = 111b	4.71	4.81	4.95	V	
V <sub>PUMP0</sub>	V <sub>DD</sub> value for pump trip VM[2:0] = 000b	2.45	2.55	2.62 <sup>[14]</sup>	V	
V <sub>PUMP1</sub>	VM[2:0] = 001b	2.96	3.02	3.09	V	
V <sub>PUMP2</sub>	VM[2:0] = 010b	3.03	3.10	3.16	V	
V <sub>PUMP3</sub>	VM[2:0] = 011b	3.18	3.25	3.32 <sup>[15]</sup>	V	
V <sub>PUMP4</sub>	VM[2:0] = 100b	4.54	4.64	4.74	V	
V <sub>PUMP5</sub>	VM[2:0] = 101b	4.62	4.73	4.83	V	
V <sub>PUMP6</sub>	VM[2:0] = 110b	4.71	4.82	4.92	V	
V <sub>PUMP7</sub>	VM[2:0] = 111b	4.89	5.00	5.12	V	

**Notes**

12. Always greater than 50 mV above V<sub>PPOR</sub> (PORLEV = 00) for falling supply.
13. Always greater than 50 mV above V<sub>PPOR</sub> (PORLEV = 01) for falling supply.
14. Always greater than 50 mV above V<sub>LVD0</sub>.
15. Always greater than 50 mV above V<sub>LVD3</sub>.

### DC Programming Specifications

Table 21 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , 3.0 V to 3.6 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , or 2.4 V to 3.0 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 21. DC Programming Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
V <sub>DDP</sub>	V <sub>DD</sub> for programming and erase	4.5	5	5.5	V	This specification applies to the functional requirements of external programmer tools
V <sub>DDL</sub>	Low V <sub>DD</sub> for verify	2.4	2.5	2.6	V	This specification applies to the functional requirements of external programmer tools
V <sub>DDH</sub>	High V <sub>DD</sub> for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
V <sub>DDIWRITE</sub>	Supply voltage for flash write operation	2.7	–	5.25	V	This specification applies to this device when it is executing internal flash writes
I <sub>DDP</sub>	Supply current during programming or verify	–	5	25	mA	
V <sub>ILP</sub>	Input low voltage during programming or verify	–	–	0.8	V	
V <sub>IHP</sub>	Input high voltage during programming or verify	2.2	–	–	V	
I <sub>ILP</sub>	Input current when applying V <sub>ILP</sub> to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor
I <sub>IHP</sub>	Input current when applying V <sub>IHP</sub> to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor
V <sub>OLV</sub>	Output low voltage during programming or verify	–	–	V <sub>SS</sub> + 0.75	V	
V <sub>OHV</sub>	Output high voltage during programming or verify	V <sub>DD</sub> – 1.0	–	V <sub>DD</sub>	V	
Flash <sub>ENPB</sub>	Flash endurance (per block)	50,000 <sup>[16]</sup>	–	–	–	Erase/write cycles per block
Flash <sub>ENT</sub>	Flash endurance (total) <sup>[17]</sup>	1,800,000	–	–	–	Erase/write cycles
Flash <sub>DR</sub>	Flash data retention	10	–	–	Years	

### DC I<sup>2</sup>C Specifications

Table 22 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , 3.0 V to 3.6 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , or 2.4 V to 3.0 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 22. DC I<sup>2</sup>C Specifications<sup>[18]</sup>**

Symbol	Description	Min	Typ	Max	Units	Notes
V <sub>IL2C</sub>	Input low level	–	–	0.3 × V <sub>DD</sub>	V	2.4 V ≤ V <sub>DD</sub> ≤ 3.6 V
		–	–	0.25 × V <sub>DD</sub>	V	4.75 V ≤ V <sub>DD</sub> ≤ 5.25 V
V <sub>IH2C</sub>	Input high level	0.7 × V <sub>DD</sub>	–	–	V	2.4 V ≤ V <sub>DD</sub> ≤ 5.25 V

#### Notes

16. The 50,000 cycle flash endurance per block is only guaranteed if the flash is operating within one voltage range. Voltage ranges are 2.4 V to 3.0 V, 3.0 V to 3.6 V, and 4.75 V to 5.25 V.
17. A maximum of 36 × 50,000 block endurance cycles is allowed. This may be balanced between operations on 36 × 1 blocks of 50,000 maximum cycles each, 36 × 2 blocks of 25,000 maximum cycles each, or 36 × 4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36 × 50,000 and ensure that no single block ever sees more than 50,000 cycles). For the full industrial range, you must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs application note AN2015 (Design Aids - Reading and Writing PSoC® Flash) for more information.
18. All GPIO meet the DC GPIO VIL and VIH specifications found in the DC GPIO Specifications sections. The I<sup>2</sup>C GPIO pins also meet the above specs.

## AC Electrical Characteristics

### AC Chip-Level Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , 3.0 V to 3.6 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , or 2.4 V to 3.0 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 23. 5 V and 3.3 V AC Chip-Level Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
F <sub>IMO24</sub>	IMO frequency for 24 MHz	23.4	24	24.6 <sup>[19,20]</sup>	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See <a href="#">Figure 13 on page 20</a> . SLIMO mode = 0
F <sub>IMO6</sub>	IMO frequency for 6 MHz	5.5	6	6.5 <sup>[19,20]</sup>	MHz	Trimmed for 5 V or 3.3 V operation using factory trim values. See <a href="#">Figure 13 on page 20</a> . SLIMO mode = 1
F <sub>CPU1</sub>	CPU frequency (5 V nominal)	0.091	24	24.6 <sup>[19]</sup>	MHz	24 MHz only for SLIMO mode = 0
F <sub>CPU2</sub>	CPU frequency (3.3 V nominal)	0.091	12	12.3 <sup>[20]</sup>	MHz	SLIMO mode = 0
F <sub>BLK5</sub>	Digital PSoC block frequency (5 V nominal)	0	48	49.2 <sup>[19,21]</sup>	MHz	Refer to <a href="#">AC Digital Block Specifications on page 30</a>
F <sub>BLK33</sub>	Digital PSoC block frequency (3.3 V nominal)	0	24	24.6 <sup>[21]</sup>	MHz	
F <sub>32K1</sub>	ILO frequency	15	32	64	kHz	
F <sub>32K_U</sub>	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the system resets section of the <a href="#">PSoC Technical Reference Manual</a> for details on this timing
t <sub>XRST</sub>	External reset pulse width	10	–	–	μs	
DC <sub>24M</sub>	24 MHz duty cycle	40	50	60	%	
DC <sub>ILO</sub>	ILO duty cycle	20	50	80	%	
Step <sub>24M</sub>	24 MHz trim step size	–	50	–	kHz	
F <sub>out48M</sub>	48 MHz output frequency	46.8	48.0	49.2 <sup>[19,20]</sup>	MHz	Trimmed. Using factory trim values
F <sub>MAX</sub>	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
SR <sub>POWER_UP</sub>	Power supply slew rate	–	–	250	V/ms	V <sub>DD</sub> slew rate during power-up
t <sub>POWERUP</sub>	Time from end of POR to CPU executing code	–	16	100	ms	Power-up from 0 V. See the System Resets section of the <a href="#">PSoC Technical Reference Manual</a>
t <sub>jit_IMO</sub>	24-MHz IMO cycle-to-cycle jitter (RMS) <sup>[22]</sup>	–	200	700	ps	
	24-MHz IMO long term N cycle-to-cycle jitter (RMS) <sup>[22]</sup>	–	300	900	ps	N = 32
	24-MHz IMO period jitter (RMS) <sup>[22]</sup>	–	100	400	ps	

#### Notes

19. 4.75 V < V<sub>DD</sub> < 5.25 V.

20. 3.0 V < V<sub>DD</sub> < 3.6 V. See application note [AN2012](#) "Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation" for information on trimming for operation at 3.3 V.

21. See the individual user module datasheets for information on maximum frequencies for user modules.

22. Refer to Cypress Jitter Specifications Application Note [AN5054](#) "Understanding Datasheet Jitter Specifications for Cypress Timing Products" at [www.cypress.com](http://www.cypress.com) under Application Notes for more information.

**Table 24. 2.7 V AC Chip-Level Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
F <sub>IMO12</sub>	IMO frequency for 12 MHz	11.5	12	12.7 <sup>[23,24]</sup>	MHz	Trimmed for 2.7 V operation using factory trim values. See <a href="#">Figure 13 on page 20</a> . SLIMO mode = 1
F <sub>IMO6</sub>	IMO frequency for 6 MHz	5.5	6	6.5 <sup>[23,24]</sup>	MHz	Trimmed for 2.7 V operation using factory trim values. See <a href="#">Figure 13 on page 20</a> . SLIMO mode = 1
F <sub>CPU1</sub>	CPU frequency (2.7 V nominal)	0.093	3	3.15 <sup>[23]</sup>	MHz	12 MHz only for SLIMO mode = 0
F <sub>BLK27</sub>	Digital PSoC block frequency (2.7 V nominal)	0	12	12.5 <sup>[23,24]</sup>	MHz	Refer to <a href="#">AC Digital Block Specifications on page 30</a>
F <sub>32K1</sub>	ILO frequency	8	32	96	kHz	
F <sub>32K_U</sub>	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the System Resets section of the <a href="#">PSoC Technical Reference Manual</a> for details on this timing
t <sub>XRST</sub>	External reset pulse width	10	–	–	μs	
DC <sub>ILO</sub>	ILO duty cycle	20	50	80	%	
F <sub>MAX</sub>	Maximum frequency of signal on row input or row output.	–	–	12.3	MHz	
SR <sub>POWER_UP</sub>	Power supply slew rate	–	–	250	V/ms	V <sub>DD</sub> slew rate during power-up
t <sub>POWERUP</sub>	Time from end of POR to CPU executing code	–	16	100	ms	Power-up from 0 V. See the System Resets section of the <a href="#">PSoC Technical Reference Manual</a> .
t <sub>jit_IMO</sub>	12 MHz IMO cycle-to-cycle jitter (RMS) <sup>[25]</sup>	–	400	1000	ps	
	12 MHz IMO long term N cycle-to-cycle jitter (RMS) <sup>[25]</sup>	–	600	1300	ps	N = 32
	12 MHz IMO period jitter (RMS) <sup>[25]</sup>	–	100	500	ps	

**Note**

 23. 2.4 V < V<sub>DD</sub> < 3.0 V.

 24. See Application Note [AN2012](#) "Adjusting PSoC Microcontroller Trims for Dual Voltage-Range Operation" available at <http://www.cypress.com> for information on maximum frequency for user modules.

 25. Refer to Cypress Jitter Specifications Application Note [AN5054](#) "Understanding Datasheet Jitter Specifications for Cypress Timing Products" at [www.cypress.com](http://www.cypress.com) under Application Notes for more information.

### AC General Purpose I/O Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , 3.0 V to 3.6 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , or 2.4 V to 3.0 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

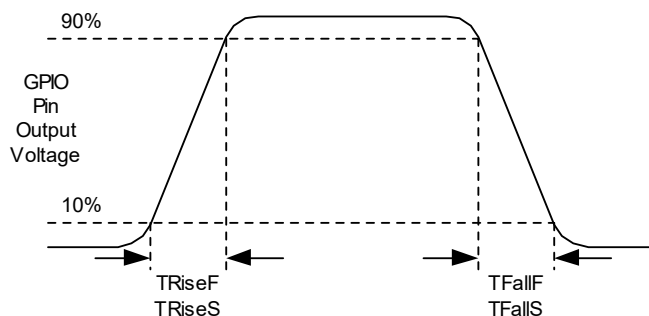
**Table 25. 5 V and 3.3 V AC GPIO Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
$F_{\text{GPIO}}$	GPIO operating frequency	0	–	12	MHz	Normal strong mode
$T_{\text{RiseF}}$	Rise time, normal strong mode, $C_{\text{load}} = 50\text{ pF}$	3	–	18	ns	$V_{\text{DD}} = 4.5\text{ to }5.25\text{ V}$ , 10% to 90%
$T_{\text{FallF}}$	Fall time, normal strong mode, $C_{\text{load}} = 50\text{ pF}$	2	–	18	ns	$V_{\text{DD}} = 4.5\text{ to }5.25\text{ V}$ , 10% to 90%
$T_{\text{RiseS}}$	Rise time, slow strong mode, $C_{\text{load}} = 50\text{ pF}$	7	27	–	ns	$V_{\text{DD}} = 3\text{ to }5.25\text{ V}$ , 10% to 90%
$T_{\text{FallS}}$	Fall time, slow strong mode, $C_{\text{load}} = 50\text{ pF}$	7	22	–	ns	$V_{\text{DD}} = 3\text{ to }5.25\text{ V}$ , 10% to 90%

**Table 26. 2.7 V AC GPIO Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
$F_{\text{GPIO}}$	GPIO operating frequency	0	–	3	MHz	Normal strong mode
$T_{\text{RiseF}}$	Rise time, normal strong mode, $C_{\text{load}} = 50\text{ pF}$	6	–	50	ns	$V_{\text{DD}} = 2.4\text{ to }3.0\text{ V}$ , 10% to 90%
$T_{\text{FallF}}$	Fall time, normal strong mode, $C_{\text{load}} = 50\text{ pF}$	6	–	50	ns	$V_{\text{DD}} = 2.4\text{ to }3.0\text{ V}$ , 10% to 90%
$T_{\text{RiseS}}$	Rise time, slow strong mode, $C_{\text{load}} = 50\text{ pF}$	18	40	120	ns	$V_{\text{DD}} = 2.4\text{ to }3.0\text{ V}$ , 10% to 90%
$T_{\text{FallS}}$	Fall time, slow strong mode, $C_{\text{load}} = 50\text{ pF}$	18	40	120	ns	$V_{\text{DD}} = 2.4\text{ to }3.0\text{ V}$ , 10% to 90%

**Figure 15. GPIO Timing Diagram**



### AC Operational Amplifier Specifications

Table 27 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , 3.0 V to 3.6 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , or 2.4 V to 3.0 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 27. AC Operational Amplifier Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
$T_{\text{COMP}}$	Comparator mode response time, 50 mV overdrive	–	–	100 200	ns ns	$V_{\text{DD}} \geq 3.0\text{ V}$ $2.4\text{ V} < V_{\text{DD}} < 3.0\text{ V}$

**AC Digital Block Specifications**

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , 3.0 V to 3.6 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , or 2.4 V to 3.0 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 28. 5 V and 3.3 V AC Digital Block Specifications**

Function	Description	Min	Typ	Max	Unit	Notes
All functions	Block input clock frequency					
	$V_{DD} \geq 4.75\text{ V}$	–	–	49.2	MHz	
	$V_{DD} < 4.75\text{ V}$	–	–	24.6	MHz	
Timer	Input clock frequency					
	No capture, $V_{DD} \geq 4.75\text{ V}$	–	–	49.2	MHz	
	No capture, $V_{DD} < 4.75\text{ V}$	–	–	24.6	MHz	
	With capture	–	–	24.6	MHz	
	Capture pulse width	50 <sup>[26]</sup>	–	–	ns	
Counter	Input clock frequency					
	No enable input, $V_{DD} \geq 4.75\text{ V}$	–	–	49.2	MHz	
	No enable input, $V_{DD} < 4.75\text{ V}$	–	–	24.6	MHz	
	With enable input	–	–	24.6	MHz	
	Enable input pulse width	50 <sup>[26]</sup>	–	–	ns	
Dead Band	Kill pulse width					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	50 <sup>[26]</sup>	–	–	ns	
	Disable mode	50 <sup>[26]</sup>	–	–	ns	
	Input clock frequency					
	$V_{DD} \geq 4.75\text{ V}$	–	–	49.2	MHz	
	$V_{DD} < 4.75\text{ V}$	–	–	24.6	MHz	
CRCPRS (PRS Mode)	Input clock frequency					
	$V_{DD} \geq 4.75\text{ V}$	–	–	49.2	MHz	
	$V_{DD} < 4.75\text{ V}$	–	–	24.6	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	24.6	MHz	
SPIM	Input clock frequency	–	–	8.2	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock (SCLK) frequency	–	–	4.1	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_negated between transmissions	50 <sup>[26]</sup>	–	–	ns	
Transmitter	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	$V_{DD} \geq 4.75\text{ V}$ , 2 stop bits	–	–	49.2	MHz	
	$V_{DD} \geq 4.75\text{ V}$ , 1 stop bit	–	–	24.6	MHz	
	$V_{DD} < 4.75\text{ V}$	–	–	24.6	MHz	
Receiver	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	$V_{DD} \geq 4.75\text{ V}$ , 2 stop bits	–	–	49.2	MHz	
	$V_{DD} \geq 4.75\text{ V}$ , 1 stop bit	–	–	24.6	MHz	
	$V_{DD} < 4.75\text{ V}$	–	–	24.6	MHz	

**Note**

26. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

**Table 29. 2.7 V AC Digital Block Specifications**

Function	Description	Min	Typ	Max	Units	Notes
All functions	Block input clock frequency	–	–	12.7	MHz	2.4 V < V <sub>DD</sub> < 3.0 V
Timer	Capture pulse width	100 <sup>[27]</sup>	–	–	ns	
	Input clock frequency, with or without capture	–	–	12.7	MHz	
Counter	Enable input pulse width	100	–	–	ns	
	Input clock frequency, no enable input	–	–	12.7	MHz	
	Input clock frequency, enable input	–	–	12.7	MHz	
Dead Band	Kill pulse width:					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	100	–	–	ns	
	Disable mode	100	–	–	ns	
CRCPRS (PRS Mode)	Input clock frequency	–	–	12.7	MHz	
	Input clock frequency	–	–	12.7	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	12.7	MHz	
SPIM	Input clock frequency	–	–	6.35	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock (SCLK) frequency	–	–	4.1	MHz	
	Width of SS_ Negated between transmissions	100	–	–	ns	
Transmitter	Input clock frequency	–	–	12.7	MHz	The baud rate is equal to the input clock frequency divided by 8.
Receiver	Input clock frequency	–	–	12.7	MHz	The baud rate is equal to the input clock frequency divided by 8.

**AC External Clock Specifications**

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , or 3.0 V to 3.6 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 30. 5 V AC External Clock Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
F <sub>OSCEXT</sub>	Frequency	0.093	–	24.6	MHz	
–	High period	20.6	–	5300	ns	
–	Low period	20.6	–	–	ns	
–	Power-up IMO to switch	150	–	–	μs	

**Note**

27. 100 ns minimum input pulse width is based on the input synchronizers running at 12 MHz (84 ns nominal period).

**Table 31. 3.3 V AC External Clock Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
F <sub>OSCEXT</sub>	Frequency with CPU clock divide by 1	0.093	–	12.3	MHz	Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements
F <sub>OSCEXT</sub>	Frequency with CPU clock divide by 2 or greater	0.186	–	24.6	MHz	If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met
–	High period with CPU clock divide by 1	41.7	–	5300	ns	
–	Low period with CPU clock divide by 1	41.7	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	

**Table 32. 2.7 V AC External Clock Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
F <sub>OSCEXT</sub>	Frequency with CPU clock divide by 1	0.093	–	3.08	MHz	Maximum CPU frequency is 3 MHz at 2.7 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements
F <sub>OSCEXT</sub>	Frequency with CPU clock divide by 2 or greater	0.186	–	6.35	MHz	If the frequency of the external clock is greater than 3 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider ensures that the fifty percent duty cycle requirement is met
–	High period with CPU clock divide by 1	160	–	5300	ns	
–	Low period with CPU clock divide by 1	160	–	–	ns	
–	Power-up IMO to switch	150	–	–	µs	



### AC Programming Specifications

Table 33 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , or 3.0 V to 3.6 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 33. AC Programming Specifications**

Symbol	Description	Min	Typ	Max	Units	Notes
$T_{RSCLK}$	Rise time of SCLK	1	–	20	ns	
$T_{FSCLK}$	Fall time of SCLK	1	–	20	ns	
$T_{SSCLK}$	Data setup time to falling edge of SCLK	40	–	–	ns	
$T_{HSCLK}$	Data hold time from falling edge of SCLK	40	–	–	ns	
$F_{SCLK}$	Frequency of SCLK	0	–	8	MHz	
$T_{ERASEB}$	Flash erase time (block)	–	10	–	ms	
$T_{WRITE}$	Flash block write time	–	40	–	ms	
$T_{DSCLK}$	Data out delay from falling edge of SCLK	–	–	45	ns	$3.6 < V_{DD}$
$T_{DSCLK3}$	Data out delay from falling edge of SCLK	–	–	50	ns	$3.0 \leq V_{DD} \leq 3.6$
$T_{DSCLK2}$	Data out delay from falling edge of SCLK	–	–	70	ns	$2.4 \leq V_{DD} \leq 3.0$
$T_{ERASEALL}$	Flash erase time (Bulk)	–	20	–	ms	Erase all blocks and protection fields at once
$T_{PROGRAM\_HOT}$	Flash block erase + flash block write time	–	–	100 <sup>[28]</sup>	ms	$0\text{ }^{\circ}\text{C} \leq T_j \leq 100\text{ }^{\circ}\text{C}$
$T_{PROGRAM\_COLD}$	Flash block erase + flash block write time	–	–	200 <sup>[28]</sup>	ms	$-40\text{ }^{\circ}\text{C} \leq T_j \leq 0\text{ }^{\circ}\text{C}$

### AC I<sup>2</sup>C Specifications

The following tables list the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , 3.0 V to 3.6 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , or 2.4 V to 3.0 V and  $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ , respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

**Table 34. AC Characteristics of the I<sup>2</sup>C SDA and SCL Pins for  $V_{DD} \geq 3.0\text{ V}$**

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
$F_{SCL2C}$	SCL clock frequency	0	100	0	400	kHz
$T_{HDSTA2C}$	Hold time (repeated) start condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	μs
$T_{LOW2C}$	Low period of the SCL clock	4.7	–	1.3	–	μs
$T_{HIGH2C}$	High period of the SCL clock	4.0	–	0.6	–	μs
$T_{SUSTA2C}$	Setup time for a repeated start condition	4.7	–	0.6	–	μs
$T_{HDDAT2C}$	Data hold time	0	–	0	–	μs
$T_{SUDAT2C}$	Data setup time	250	–	100 <sup>[29]</sup>	–	ns
$T_{SUSTOI2C}$	Setup time for stop condition	4.0	–	0.6	–	μs
$T_{BUFI2C}$	Bus free time between a stop and start condition	4.7	–	1.3	–	μs
$T_{SPI2C}$	Pulse width of spikes suppressed by the input filter.	–	–	0	50	ns

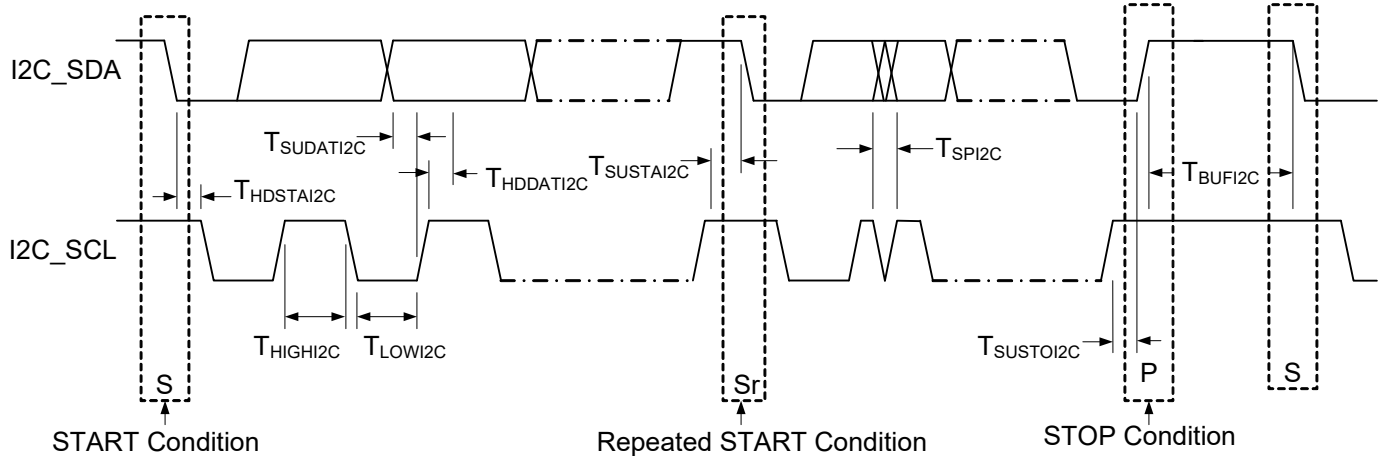
#### Notes

28. For the full industrial range, the user must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the Flash APIs application note AN2015 (Design Aids - Reading and Writing PSoC® Flash) for more information.
29. A Fast-Mode I<sup>2</sup>C-bus device may be used in a Standard-Mode I<sup>2</sup>C-bus system, but it must meet the requirement  $T_{SU,DAT} \geq 250\text{ ns}$ . This is automatically the case if the device does not stretch the LOW period of the SCL signal. If the device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line  $T_{rmax} + T_{SU,DAT} = 1000 + 250 = 1250\text{ ns}$  (according to the Standard-Mode I<sup>2</sup>C-bus specification) before the SCL line is released.

Table 35. 2.7 V AC Characteristics of the I<sup>2</sup>C SDA and SCL Pins (Fast Mode not Supported)

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
F <sub>SCL I2C</sub>	SCL clock frequency	0	100	–	–	kHz
T <sub>HDSTAI2C</sub>	Hold time (repeated) start condition. After this period, the first clock pulse is generated.	4.0	–	–	–	μs
T <sub>LOWI2C</sub>	Low period of the SCL clock	4.7	–	–	–	μs
T <sub>HIGHI2C</sub>	High period of the SCL clock	4.0	–	–	–	μs
T <sub>SUSTA I2C</sub>	Setup time for a repeated start condition	4.7	–	–	–	μs
T <sub>HDDATI2C</sub>	Data hold time	0	–	–	–	μs
T <sub>SUDATI2C</sub>	Data setup time	250	–	–	–	ns
T <sub>SUSTOI2C</sub>	Setup time for stop condition	4.0	–	–	–	μs
T <sub>BUFI2C</sub>	Bus free time between a stop and start condition	4.7	–	–	–	μs
T <sub>SPI2C</sub>	Pulse width of spikes are suppressed by the input filter.	–	–	–	–	ns

Figure 16. Definition for Timing for Fast/Standard Mode on the I<sup>2</sup>C Bus

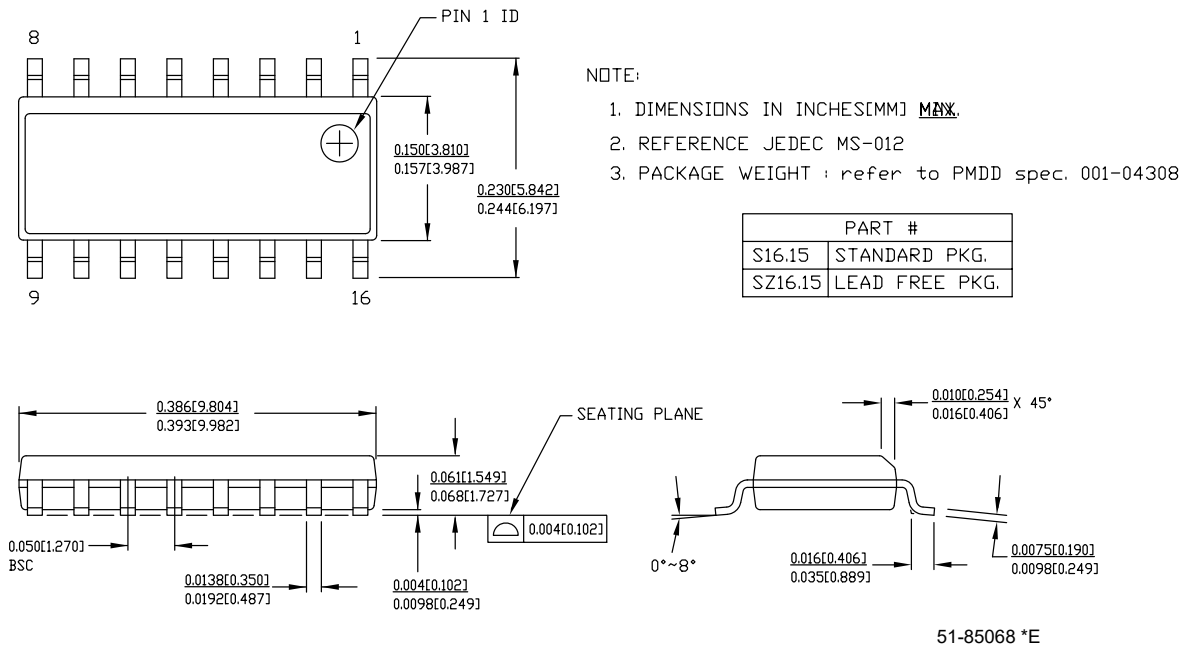


### Packaging Information

This section shows the packaging specifications for the CY8C21x34B PSoC device with the thermal impedances for each package.

**Important Note** Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at <http://www.cypress.com>.

**Figure 17. 16-pin SOIC (150 Mils) Package Outline, 51-85068**



**Figure 18. 20-pin SSOP (210 Mils) Package Outline, 51-85077**

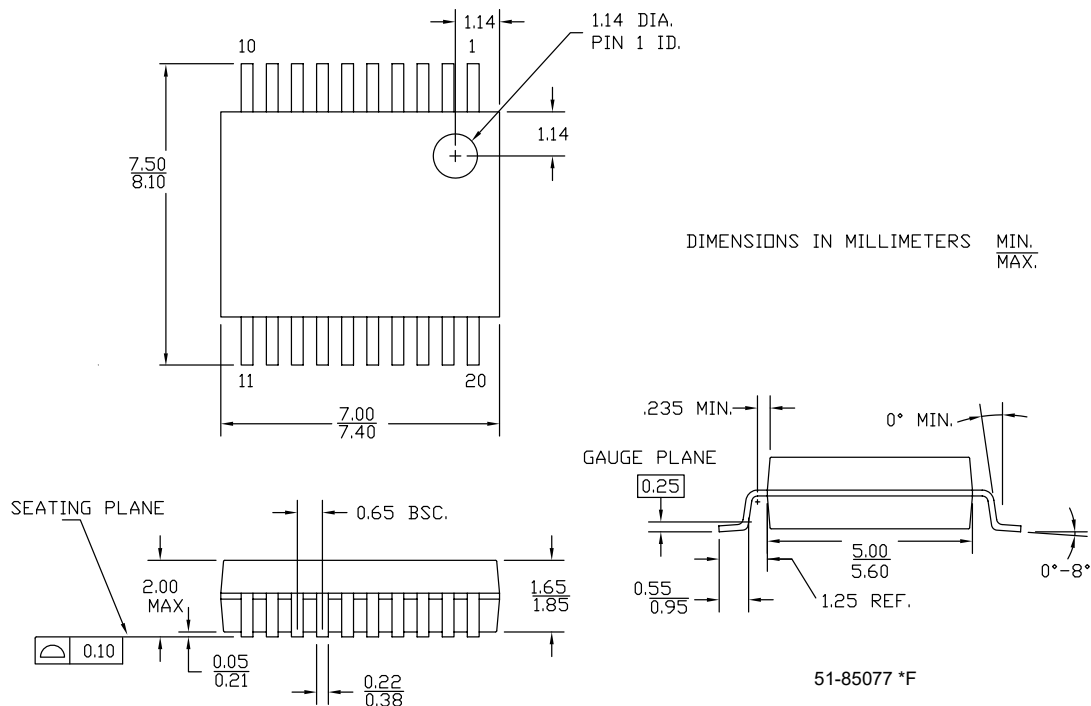


Figure 19. 28-pin SSOP (210 Mils) Package Outline, 51-85079

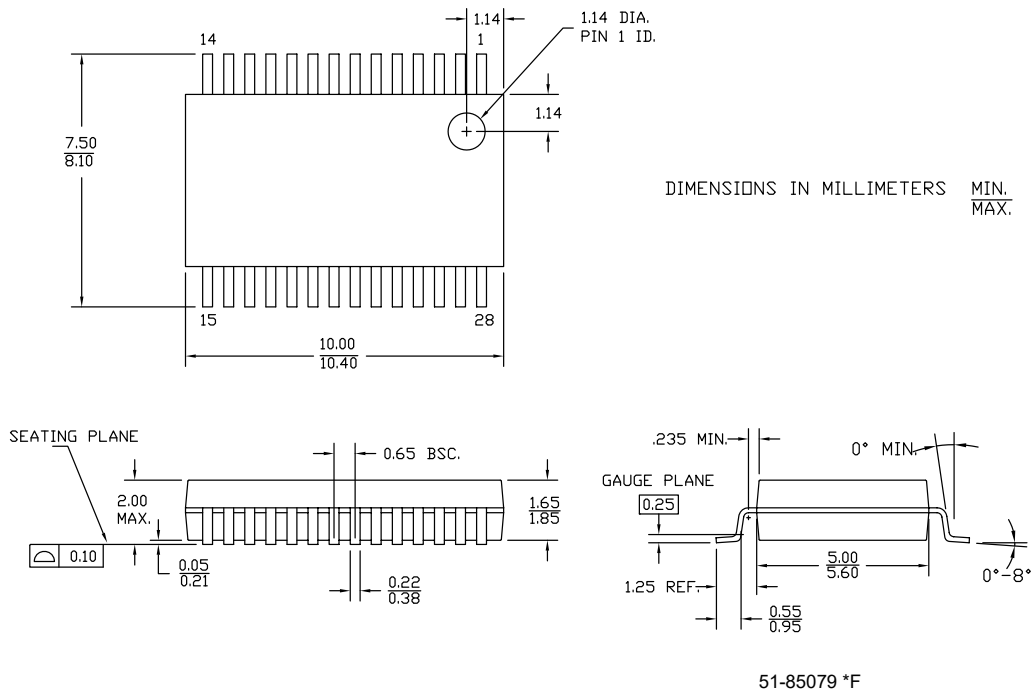


Figure 20. 32-pin QFN (5 × 5 × 1.0 mm) LT32B (3.5 × 3.5) E-Pad (Sawn) Package Outline, 001-30999

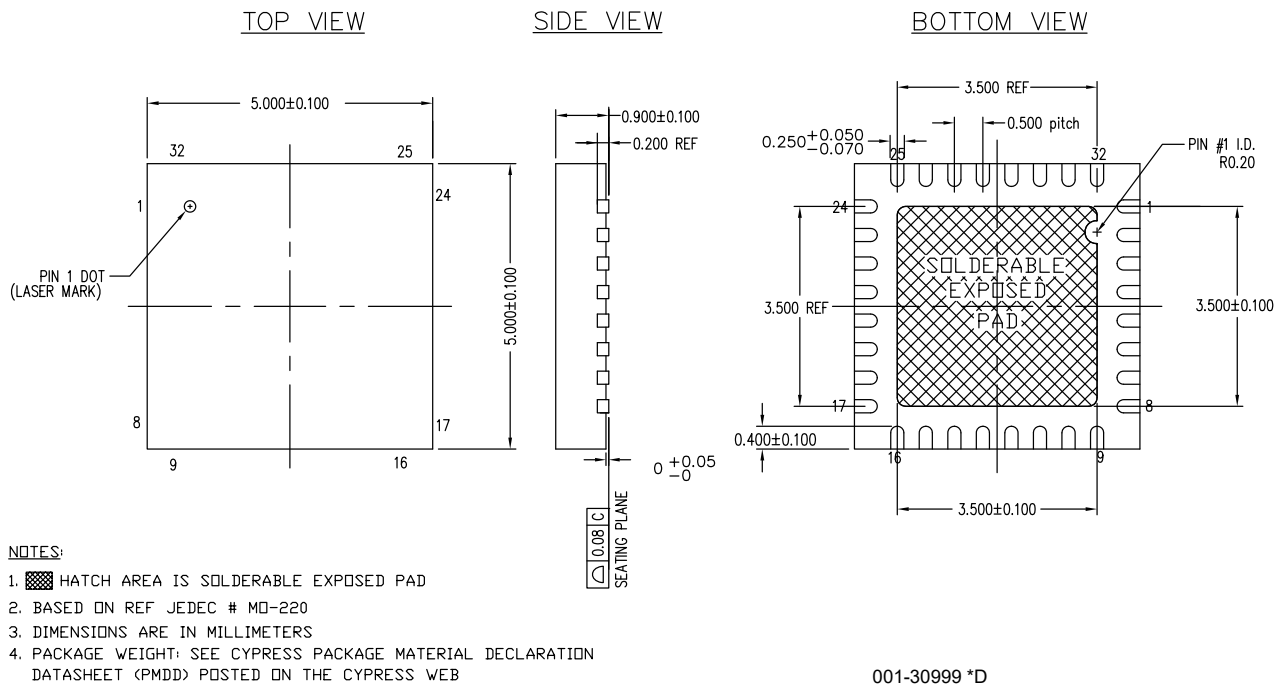
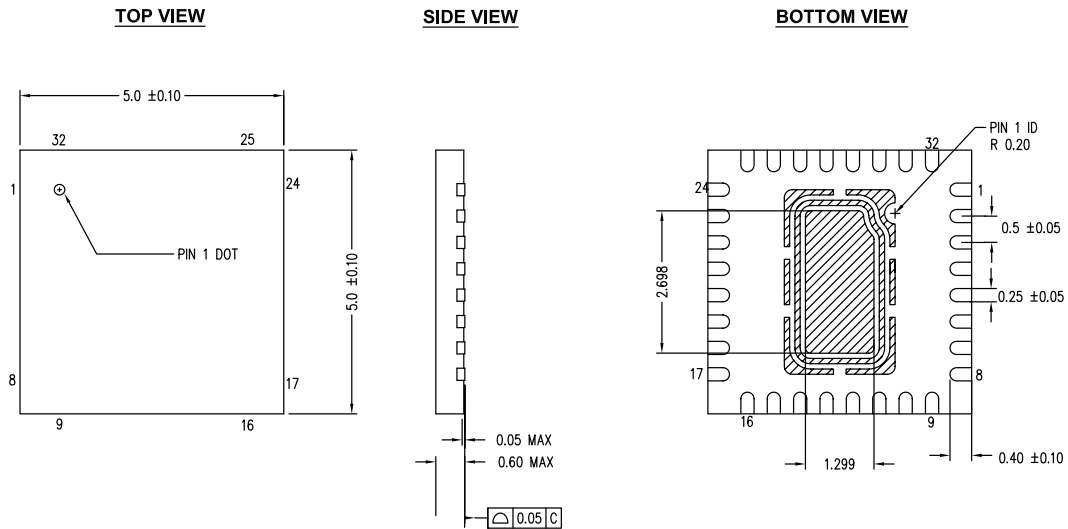


Figure 21. 32-pin QFN (5 × 5 × 0.55 mm) 1.3 × 2.7 E-Pad (Sawn Type) Package Outline, 001-48913



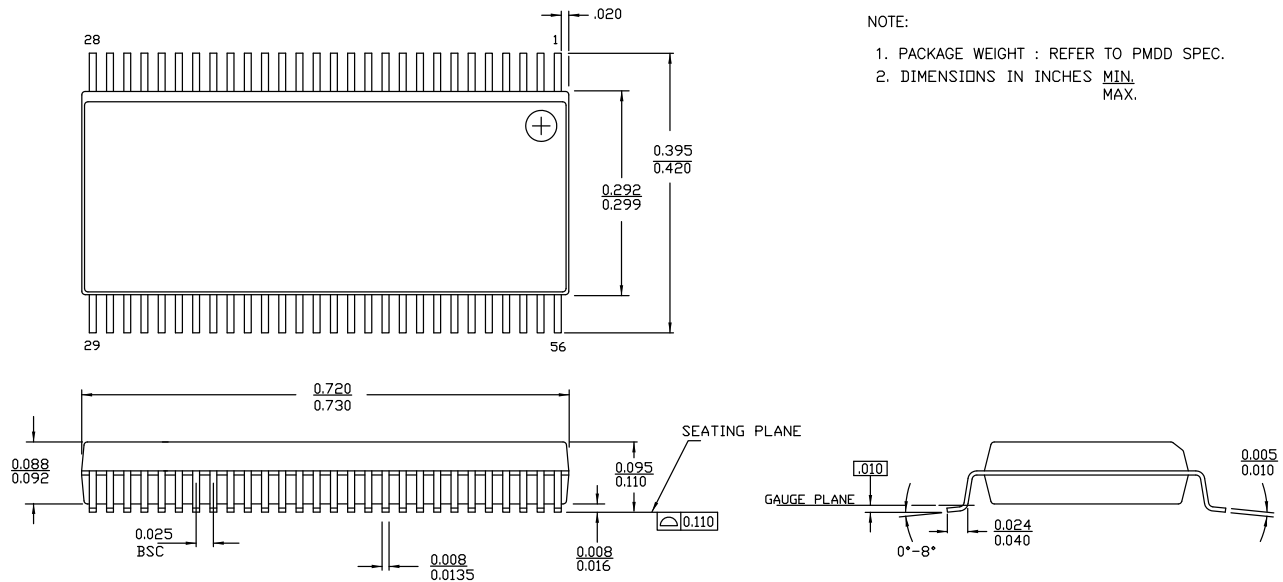
NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT:  $38\text{mg} \pm 4 \text{ mg}$
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-48913 \*D

**Important Note** For information on the preferred dimensions for mounting QFN packages, see the following application note, *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at <http://www.cypress.com>.

Figure 22. 56-pin SSOP (300 Mils) Package Outline, 51-85062



NOTE:

1. PACKAGE WEIGHT : REFER TO PMDD SPEC.
2. DIMENSIONS IN INCHES   
 MIN.   
 MAX.

51-85062 \*F

**Thermal Impedances**
**Table 36. Thermal Impedances per Package**

Package	Typical $\theta_{JA}$ <sup>[30]</sup>	Typical $\theta_{JC}$
16-pin SOIC	123 °C/W	55 °C/W
20-pin SSOP	117 °C/W	41 °C/W
28-pin SSOP	96 °C/W	39 °C/W
32-pin QFN <sup>[31]</sup> 5 × 5 mm 0.60 Max	27 °C/W	15 °C/W
32-pin QFN <sup>[31]</sup> 5 × 5 mm 0.93 Max	22 °C/W	12 °C/W
56-pin SSOP	48 °C/W	24 °C/W

**Solder Reflow Peak Temperature**

Table 37 lists the maximum solder reflow peak temperatures to achieve good solderability. Thermal ramp rate during preheat should be 3 °C/s or lower.

**Table 37. Solder Reflow Peak Temperature**

Package	Maximum Peak Temperature	Time at Maximum Temperature
16-pin SOIC	260 °C	30 s
20-pin SSOP	260 °C	30 s
28-pin SSOP	260 °C	30 s
32-pin QFN	260 °C	30 s
56-pin SSOP	260 °C	30 s

**Notes**

30.  $T_J = T_A + \text{Power} \times \theta_{JA}$

31. To achieve the thermal impedance specified for the QFN package, refer to *Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845* available at <http://www.cypress.com>.

32. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

## Development Tool Selection

This section presents the development tools available for all current PSoC device families including the CY8C21x34B family.

### Software

#### *PSoC Designer™*

At the core of the PSoC development software suite is PSoC Designer, used to generate PSoC firmware applications. PSoC Designer is available free of cost at <http://www.cypress.com> and includes a free C compiler.

#### *PSoC Programmer*

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or operates directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC programmer is available free of charge at <http://www.cypress.com>.

### Development Kits

All development kits can be purchased from the Cypress Online Store.

#### CY3280-BK1 Universal CapSense Controller - Basic Kit 1

The [CY3280-BK1](#) Universal CapSense Controller Kit is designed for easy prototyping and debug of CapSense designs with pre-defined control circuitry and plug-in hardware. The kit comes with controller boards for the CY8C20x34 and CY8C21x34 PSoC devices as well as a breadboard module and a button(5) / slider module.

#### CY3215-DK Basic Development Kit

The [CY3215-DK](#) is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation, and the software interface allows you to run, halt, and single step the processor, and view the content of specific memory locations. Advance emulation features also supported through PSoC Designer. The kit includes:

- PSoC Designer software CD
- ICE-Cube in-circuit emulator
- ICE Flex-Pod for CY8C29x66 family
- Cat-5 adapter
- Mini-Eval programming board
- 110 ~ 240 V power supply, Euro-Plug adapter
- iMAGEcraft C compiler
- ISSP cable
- USB 2.0 cable and Blue Cat-5 cable
- Two CY8C29466-24PXI 28-PDIP chip samples

### Evaluation Tools

All evaluation tools can be purchased from the Cypress Online Store.

#### *CY3210-MiniProg1*

The [CY3210-MiniProg1 kit](#) allows you to program PSoC devices through the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC through a provided USB 2.0 cable. The kit includes:

- MiniProg programming unit
- MiniEval socket programming and evaluation board
- 28-Pin CY8C29466-24PXI PDIP PSoC device sample
- 28-Pin CY8C27443-24PXI PDIP PSoC device sample
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

#### *CY3210-PSoCEval1*

The [CY3210-PSoCEval1 kit](#) features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- Evaluation board with LCD module
- MiniProg programming unit
- Two 28-Pin CY8C29466-24PXI PDIP PSoC device samples
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable

#### *CY3214-PSoCEvalUSB*

The [CY3214-PSoCEvalUSB evaluation kit](#) features a development board for the CY8C24794-24LFXI PSoC device. The board includes both USB and capacitive sensing development and debugging support. This evaluation board also includes an LCD module, potentiometer, LEDs, an enunciator and plenty of breadboarding space to meet all of your evaluation needs. The kit includes:

- PSoCEvalUSB board
- LCD module
- MiniProg programming unit
- Mini USB cable
- PSoC Designer and example projects CD
- Getting Started guide
- Wire pack

## Device Programmers

All device programmers can be purchased from the Cypress Online Store.

### *CY3216 Modular Programmer*

The [CY3216 Modular Programmer kit](#) features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- MiniProg programming unit
- PSoC Designer software CD
- Getting Started guide
- USB 2.0 cable
- Modular programmer base
- Three programming module cards

## Accessories (Emulation and Programming)

**Table 38. Emulation and Programming Accessories**

Part Number	Pin Package	Flex-Pod Kit <sup>[33]</sup>	Foot Kit <sup>[34]</sup>	Adapter
CY8C21234B-24SXI	16-Pin SOIC	CY3250-21X34	CY3250-16SOIC-FK	Adapters can be found at <a href="http://www.emulation.com">http://www.emulation.com</a> .
CY8C21334B-24PVXI	20-Pin SSOP	CY3250-21X34	CY3250-20SSOP-FK	
CY8C21534B-24PVXI	28-Pin SSOP	CY3250-21X34	CY3250-28SSOP-FK	

### Notes

33. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.  
 34. Foot kit includes surface mount feet that can be soldered to the target PCB.



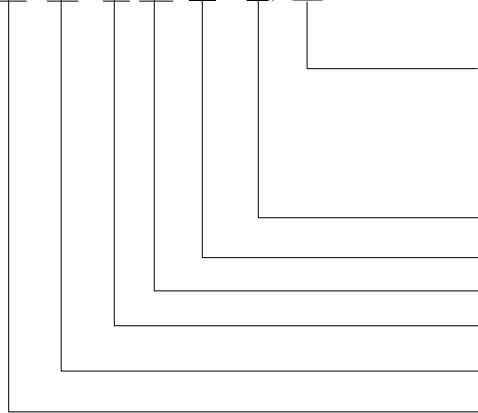
### Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	Switch Mode Pump	Temperature Range	Digital Blocks	Analog Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
16-Pin (150-Mil) SOIC	CY8C21234B-24SXI	8K	512	Yes	-40 °C to +85 °C	4	4	12	12 <sup>[35]</sup>	0	No
16-Pin (150-Mil) SOIC (Tape and Reel)	CY8C21234B-24SXIT	8K	512	Yes	-40 °C to +85 °C	4	4	12	12 <sup>[35]</sup>	0	No
20-Pin (210-Mil) SSOP	CY8C21334B-24PVXI	8K	512	No	-40 °C to +85 °C	4	4	16	16 <sup>[35]</sup>	0	Yes
20-Pin (210-Mil) SSOP (Tape and Reel)	CY8C21334B-24PVXIT	8K	512	No	-40 °C to +85 °C	4	4	16	16 <sup>[35]</sup>	0	Yes
28-Pin (210-Mil) SSOP	CY8C21534B-24PVXI	8K	512	No	-40 °C to +85 °C	4	4	24	24 <sup>[35]</sup>	0	Yes
28-Pin (210-Mil) SSOP (Tape and Reel)	CY8C21534B-24PVXIT	8K	512	No	-40 °C to +85 °C	4	4	24	24 <sup>[35]</sup>	0	Yes
32-Pin (5 × 5 mm 1.00 max) Sawn QFN	CY8C21434B-24LTXI	8K	512	No	-40 °C to +85 °C	4	4	28	28 <sup>[35]</sup>	0	Yes
32-Pin (5 × 5 mm 1.00 max) Sawn QFN <sup>[36]</sup> (Tape and Reel)	CY8C21434B-24LTXIT	8K	512	No	-40 °C to +85 °C	4	4	28	28 <sup>[35]</sup>	0	Yes
32-Pin (5 × 5 mm 0.60 max) Thin Sawn QFN (Tape and Reel)	CY8C21434B-24LQXIT	8K	512	No	-40 °C to +85 °C	4	4	28	28 <sup>[35]</sup>	0	Yes
56-Pin OCD SSOP	CY8C21001-24PVXI	8K	512	Yes	-40 °C to +85 °C	4	4	26	26 <sup>[35]</sup>	0	Yes

**Note** For Die sales information, contact a local Cypress sales office or Field Applications Engineer (FAE).

### Ordering Code Definitions

CY 8 C 21xxx-24 xx



- Package Type:  
 PX = PDIP Pb-free  
 SX = SOIC Pb-free  
 PVX = SSOP Pb-free  
 LFX/LKX/LTX/LQX = QFN Pb-free
- Speed: 24 MHz
- Part Number
- Family Code
- Technology Code: C = CMOS
- Marketing Code: 8 = Cypress PSoC
- Company ID: CY = Cypress

- Thermal Rating:  
 C = Commercial  
 I = Industrial  
 E = Extended

**Notes**

35. All Digital I/O Pins also connect to the common analog mux.  
 36. Refer to the section 32-pin Part Pinout on page 13 for pin differences.

## Acronyms

Table 39 lists the acronyms that are used in this document.

**Table 39. Acronyms Used in this Datasheet**

Acronym	Description	Acronym	Description
AC	alternating current	MIPS	million instructions per second
ADC	analog-to-digital converter	OCD	on-chip debug
API	application programming interface	PCB	printed circuit board
CMOS	complementary metal oxide semiconductor	PDIP	plastic dual-in-line package
CPU	central processing unit	PGA	programmable gain amplifier
CRC	cyclic redundancy check	PLL	phase-locked loop
CT	continuous time	POR	power on reset
DAC	digital-to-analog converter	PPOR	precision power on reset
DC	direct current	PRS	pseudo-random sequence
DTMF	dual-tone multi-frequency	PSoC®	Programmable System-on-Chip
ECO	external crystal oscillator	PWM	pulse width modulator
EEPROM	electrically erasable programmable read-only memory	QFN	quad flat no leads
GPIO	general purpose I/O	RTC	real time clock
ICE	in-circuit emulator	SAR	successive approximation
IDE	integrated development environment	SC	switched capacitor
ILO	internal low speed oscillator	SLIMO	slow IMO
IMO	internal main oscillator	SMP	switch-mode pump
I/O	input/output	SOIC	small-outline integrated circuit
IrDA	infrared data association	SPI™	serial peripheral interface
ISSP	in-system serial programming	SRAM	static random access memory
LCD	liquid crystal display	SROM	supervisory read only memory
LED	light-emitting diode	SSOP	shrink small-outline package
LPC	low power comparator	UART	universal asynchronous receiver / transmitter
LVD	low voltage detect	USB	universal serial bus
MAC	multiply-accumulate	WDT	watchdog timer
MCU	microcontroller unit	XRES	external reset

## Reference Documents

CY8CPLC20, CY8CLED16P01, CY8C29x66, CY8C27x43, CY8C24x94, CY8C24x23, CY8C24x23A, CY8C22x13, CY8C21x34B, CY8C21x23, CY7C64215, CY7C603xx, CY8CNP1xx, and CYWUSB6953 PSoC® Programmable System-on-Chip Technical Reference Manual (TRM) (001-14463)

Design Aids – Reading and Writing PSoC® Flash - AN2015 (001-40459)

Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845 (001-72845) available at <http://www.cypress.com>.

## Document Conventions

### Units of Measure

Table 40 lists the units of measures.

**Table 40. Units of Measure**

Symbol	Unit of Measure	Symbol	Unit of Measure
kB	1024 bytes	μH	microhenry
dB	decibels	μs	microsecond
°C	degree Celsius	ms	millisecond
μF	microfarad	ns	nanosecond
fF	femto farad	ps	picosecond
pF	picofarad	μV	microvolts
kHz	kilohertz	mV	millivolts
MHz	megahertz	mVpp	millivolts peak-to-peak
rt-Hz	root hertz	nV	nanovolts
kΩ	kilohm	V	volts
Ω	ohm	μW	microwatts
μA	microampere	W	watt
mA	milliampere	mm	millimeter
nA	nanoampere	ppm	parts per million
pA	pikoampere	%	percent
mH	millihenry		

### Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h' or 'b' are decimals.

### Glossary

active high	<ol style="list-style-type: none"> <li>1. A logic signal having its asserted state as the logic 1 state.</li> <li>2. A logic signal having the logic 1 state as the higher voltage of the two states.</li> </ol>
analog blocks	The basic programmable opamp circuits. These are SC (switched capacitor) and CT (continuous time) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
Application programming interface (API)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	<ol style="list-style-type: none"> <li>1. The frequency range of a message or information processing system measured in hertz.</li> <li>2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.</li> </ol>

**Glossary** (continued)

bias	<ol style="list-style-type: none"><li>1. A systematic deviation of a value from a reference value.</li><li>2. The amount by which the average of a set of values departs from a reference value.</li><li>3. The electrical, mechanical, magnetic, or other force (field) applied to a device to establish a reference level to operate the device.</li></ol>
block	<ol style="list-style-type: none"><li>1. A functional unit that performs a single function, such as an oscillator.</li><li>2. A functional unit that may be configured to perform one of several functions, such as a digital PSoC block or an analog PSoC block.</li></ol>
buffer	<ol style="list-style-type: none"><li>1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for IO operations, into which data is read, or from which data is written.</li><li>2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device.</li><li>3. An amplifier used to lower the output impedance of a system.</li></ol>
bus	<ol style="list-style-type: none"><li>1. A named connection of nets. Bundling nets together in a bus makes it easier to route nets with similar routing patterns.</li><li>2. A set of signals performing a common function and carrying similar data. Typically represented using vector notation; for example, address[7:0].</li><li>3. One or more conductors that serve as a common connection for a group of related devices.</li></ol>
clock	The device that generates a periodic signal with a fixed frequency and duty cycle. A clock is sometimes used to synchronize different logic blocks.
comparator	An electronic circuit that produces an output voltage or current whenever two input levels simultaneously satisfy predetermined amplitude requirements.
compiler	A program that translates a high level language, such as C, into machine language.
configuration space	In PSoC devices, the register space accessed when the XIO bit, in the CPU_F register, is set to '1'.
crystal oscillator	An oscillator in which the frequency is controlled by a piezoelectric crystal. Typically a piezoelectric crystal is less sensitive to ambient temperature than other circuit components.
cyclic redundancy check (CRC)	A calculation used to detect errors in data communications, typically performed using a linear feedback shift register. Similar calculations may be used for a variety of other purposes such as data compression.
data bus	A bi-directional set of signals used by a computer to convey information from a memory location to the central processing unit and vice versa. More generally, a set of signals used to convey data between digital functions.
debugger	A hardware and software system that allows you to analyze the operation of the system under development. A debugger usually allows the developer to step through the firmware one step at a time, set break points, and analyze memory.
dead band	A period of time when neither of two or more signals are in their active state or in transition.
digital blocks	The 8-bit logic blocks that can act as a counter, timer, serial receiver, serial transmitter, CRC generator, pseudo-random number generator, or SPI.
digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.

**Glossary** (continued)

duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.
External Reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
Flash	An electrically programmable and erasable, non-volatile technology that provides you the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is OFF.
Flash block	The smallest amount of Flash ROM space that may be programmed at one time and the smallest amount of Flash space that may be protected. A Flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I <sup>2</sup> C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I2C uses only two bi-directional pins, clock and data, both running at +5V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows you to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	<ol style="list-style-type: none"><li>1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams.</li><li>2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.</li></ol>
low-voltage detect (LVD)	A circuit that senses V <sub>dd</sub> and provides an interrupt to the system when V <sub>dd</sub> falls below a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the Flash, SRAM, and register space.
master device	A device that controls the timing for data exchanges between two devices. Or when devices are cascaded in width, the master device is the one that controls the timing for data exchanges between the cascaded devices and an external interface. The controlled device is called the <b>slave device</b> .

## Glossary (continued)

microcontroller	An integrated circuit chip that is designed primarily for control systems and products. In addition to a CPU, a microcontroller typically includes memory, timing circuits, and IO circuitry. The reason for this is to permit the realization of a controller with a minimal quantity of chips, thus achieving maximal possible miniaturization. This in turn, reduces the volume and the cost of the controller. The microcontroller is normally not used for general-purpose computation as is a microprocessor.
mixed-signal	The reference to a circuit containing both analog and digital techniques and components.
modulator	A device that imposes a signal on a carrier.
noise	<ol style="list-style-type: none"><li>1. A disturbance that affects a signal and that may distort the information carried by the signal.</li><li>2. The random variations of one or more characteristics of any entity such as voltage, current, or data.</li></ol>
oscillator	A circuit that may be crystal controlled and is used to generate a clock frequency.
parity	A technique for testing transmitting data. Typically, a binary digit is added to the data to make the sum of all the digits of the binary data either always even (even parity) or always odd (odd parity).
Phase-locked loop (PLL)	An electronic circuit that controls an <b>oscillator</b> so that it maintains a constant phase angle relative to a reference signal.
pinouts	The pin number assignment: the relation between the logical inputs and outputs of the PSoC device and their physical counterparts in the printed circuit board (PCB) package. Pinouts involve pin numbers as a link between schematic and PCB design (both being computer generated files) and may also involve pin names.
port	A group of pins, usually eight.
Power on reset (POR)	A circuit that forces the PSoC device to reset when the voltage is below a pre-set level. This is one type of hardware reset.
PSoC®	Cypress Semiconductor's PSoC® is a registered trademark and Programmable System-on-Chip™ is a trademark of Cypress.
PSoC Designer™	The software for Cypress' Programmable System-on-Chip technology.
pulse width modulator (PWM)	An output in the form of duty cycle which varies as a function of the applied measurement
RAM	An acronym for random access memory. A data-storage device from which data can be read out and new data can be written in.
register	A storage device with a specific capacity, such as a bit or byte.
reset	A means of bringing a system back to a know state. See hardware reset and software reset.
ROM	An acronym for read only memory. A data-storage device from which data can be read out, but new data cannot be written in.
serial	<ol style="list-style-type: none"><li>1. Pertaining to a process in which all events occur one after the other.</li><li>2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.</li></ol>
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.

**Glossary** (continued)

shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform Flash operations. The functions of the SROM may be accessed in normal user code, operating from Flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	<ol style="list-style-type: none"><li>1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal.</li><li>2. A system whose operation is synchronized by a clock signal.</li></ol>
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level <b>API (Application Programming Interface)</b> for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V <sub>DD</sub>	A name for a power net meaning 'voltage drain'. The most positive power supply signal. Usually 5 V or 3.3 V.
V <sub>SS</sub>	A name for a power net meaning 'voltage source'. The most negative power supply signal.
watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

## Errata

This section describes the errata for the PSoC® Programmable System-on-Chip CY8C21X34. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability.

Contact your local Cypress Sales Representative if you have questions.

### Part Numbers Affected

Part Number	Ordering Information
CY8C21X34	CY8C21234-24SXI
	CY8C21234-24SXIT
	CY8C21334-24PVXI
	CY8C21334-24PVXIT
	CY8C21534-24PVXI
	CY8C21534-24PVXIT
	CY8C21434-24LFXI
	CY8C21434-24LFXIT
	CY8C21434-24LKXI
	CY8C21434-24LKXIT
	CY8C21634-24LFXI
	CY8C21634-24LFXIT
	CY8C21434-24LTXI
	CY8C21434-24LTXIT
	CY8C21434-24LQXI
	CY8C21434-24LQXIT
	CY8C21634-24LTXI
	CY8C21634-24LTXIT
	CY8C21001-24PVXI

### CY8C21X34 Qualification Status

Product Status: Production



## CY8C21X34 Errata Summary

The following table defines the errata applicability to available CY8C21X34 family devices. An "X" indicates that the errata pertains to the selected device.

**Note** Errata items, in the table below, are hyperlinked. Click on any item entry to jump to its description.

Items	Part Number	Silicon Revision	Fix Status
<a href="#">[1]. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes</a>	CY8C21X34	A	No fix is currently planned.
<a href="#">[2]. I2C Errors</a>	CY8C21X34	A	No fix is currently planned.

### 1. Internal Main Oscillator (IMO) Tolerance Deviation at Temperature Extremes

#### ■ Problem Definition

Asynchronous Digital Communications Interfaces may fail framing beyond 0 °C to 70 °C. This problem does not affect end-product usage between 0 °C and 70 °C.

#### ■ Parameters Affected

The IMO frequency tolerance. The worst case deviation when operated below 0 °C and above +70 °C and within the upper and lower datasheet temperature range is ±5%.

#### ■ Trigger Condition(S)

The asynchronous Rx/Tx clock source IMO frequency tolerance may deviate beyond the datasheet limit of ±2.5% when operated beyond the temperature range of 0 °C to +70 °C.

#### ■ Scope of Impact

This problem may affect UART, IrDA, and FSK implementations.

#### ■ Workaround

Implement a quartz crystal stabilized clock source on at least one end of the asynchronous digital communications interface.

#### ■ Fix Status

No fix is currently planned.

### 2. I<sup>2</sup>C Errors

#### ■ Problem Definition

The I<sup>2</sup>C block exhibits occasional data and bus corruption errors when the I<sup>2</sup>C master initiates transactions while the device is transitioning in to or out of sleep mode.

#### ■ Parameters Affected

Affects reliability of I<sup>2</sup>C communication to device, between I<sup>2</sup>C master, and third party I<sup>2</sup>C slaves.

#### ■ Trigger Condition(S)

Triggered by transitions into and out of the device's sleep mode.

#### ■ Scope of Impact

This problem may affect UART, IrDA, and FSK implementations.

#### ■ Workaround

Firmware workarounds are available in firmware. Generally the workaround consists of disconnecting the I<sup>2</sup>C block from the bus prior to going to sleep modes. I<sup>2</sup>C transactions during sleep are supported by a protocol in which the master wakes the device prior to the I<sup>2</sup>C transaction

#### ■ Fix Status

Will not be fixed.

**Document History Page**

Document Title: CY8C21x34B, PSoC® Programmable System-on-Chip™ CapSense® Controller with SmartSense™ Auto-tuning 1–21 Buttons, 0–4 Sliders, Proximity Document Number: 001-67345				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3169205	YVA	02/16/2011	New data sheet.
*A	3247292	YVA	05/11/2011	Updated <a href="#">Packaging Information</a> spec 51-85077 – Changed Revision from *D to *E. spec 51-85079 – Changed Revision from *D to *E. Removed spec 51-85188 Rev. *D.  Post to external web.
*B	3846480	SRLI	12/19/2012	Updated <a href="#">Features</a> .  Updated <a href="#">Packaging Information</a> : spec 51-85062 – Changed Revision from *D to *F. spec 001-48913 – Changed Revision from *B to *C. spec 001-44368 – Changed Revision from *B to *C. spec 001-30999 – Changed Revision from *C to *D. spec 51-85068 – Changed Revision from *D to *E.  Updated <a href="#">Ordering Information</a> (Updated part numbers).
*C	3894458	SRLI	02/09/2013	Updated Document Title to read as “CY8C21x34B, PSoC® Programmable System-on-Chip™ CapSense® Controller with SmartSense™ Auto-tuning 1–21 Buttons, 0–4 Sliders, Proximity”.  Updated <a href="#">Packaging Information</a> (Updated <a href="#">Solder Reflow Peak Temperature</a> (Changed Time at Maximum Temperature from 20 s to 30 s in <a href="#">Table 37</a> )).
*D	4297481	DCHE	03/04/2014	Updated <a href="#">Development Tools</a> : Added hyperlink for “PSoC Designer™”. Updated <a href="#">PSoC Designer Software Subsystems</a> : Updated <a href="#">In-Circuit Emulator</a> : Added hyperlink for “in-circuit emulator” in description.  Updated <a href="#">Development Tool Selection</a> : Updated <a href="#">Software</a> : Updated <a href="#">PSoC Designer™</a> : Updated hyperlinks in description. Updated <a href="#">PSoC Programmer</a> : Updated hyperlinks in description. Updated <a href="#">Development Kits</a> : Updated description. Updated <a href="#">Evaluation Tools</a> : Updated <a href="#">CY3210-MiniProg1</a> : Updated hyperlinks in description. Updated <a href="#">CY3214-PSoCEvalUSB</a> : Updated hyperlinks in description. Updated <a href="#">Device Programmers</a> : Updated <a href="#">CY3216 Modular Programmer</a> : Updated hyperlinks in description.  Updated <a href="#">Packaging Information</a> : spec 001-44368 – Changed Revision from *C to *D. spec 001-48913 – Changed Revision from *C to *D.  Updated to new template.  Completing Sunset Review.

Document History Page (continued)

Document Title: CY8C21x34B, PSoC <sup>®</sup> Programmable System-on-Chip <sup>™</sup> CapSense <sup>®</sup> Controller with SmartSense <sup>™</sup> Auto-tuning 1–21 Buttons, 0–4 Sliders, Proximity Document Number: 001-67345				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*E	4476297	DCHE / ASRI	08/28/2014	Replaced references of “Application Notes for Surface Mount Assembly of Amkor’s MicroLeadFrame (MLF) Packages” with “Design Guidelines for Cypress Quad Flat No Extended Lead (QFN) Packaged Devices – AN72845” in all instances across the document. Added <a href="#">More Information</a> . Added <a href="#">PSoC Designer</a> . Removed “Getting Started”. Updated <a href="#">Electrical Specifications</a> : Updated <a href="#">AC Electrical Characteristics</a> : Updated <a href="#">AC Operational Amplifier Specifications</a> : Updated <a href="#">Table 27</a> : Replaced V <sub>CC</sub> with V <sub>DD</sub> . Updated <a href="#">Packaging Information</a> : Removed spec 001-44368 *D. Updated <a href="#">Development Tool Selection</a> : Updated <a href="#">Device Programmers</a> : Removed “CY3207ISSP In-System Serial Programmer (ISSP)”. Updated <a href="#">Ordering Information</a> (Updated part numbers).
*F	4670626	DCHE	02/25/2015	Added <a href="#">Errata</a> and references to errata items on page 1.
*G	5617615	DCHE	02/03/2017	Updated <a href="#">Packaging Information</a> : spec 51-85077 – Changed Revision from *E to *F. spec 51-85079 – Changed Revision from *E to *F. Updated <a href="#">Reference Documents</a> : Removed spec 001-17397 and spec 001-14503 as both specs are obsolete. Updated to new template. Completing Sunset Review.
*H	6012190	DCHE	01/03/2018	Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated to new template. Completing Sunset Review.