PSoC™ Automotive Multitouch Generation 6XL

Datasheet

Features

- Automotive Electronics Council (AEC) AEC-Q100 qualified
- Multitouch capacitive touchscreen controller
  - 32-bit Arm® Cortex® CPU
  - Register-configurable
  - Noise-suppression technologies for display and EMI
    - Effective 20-V drive for higher signal-to-noise ratio (SNR)[1]
    - AutoArmor improves both electromagnetic emissions and immunity
    - External display synchronization
  - Water rejection and wet-finger tracking using DualSense
  - Multitouch glove with automatic mode switching
    - Ten fingers with thin glove (≤ 1-mm thick)
    - Two fingers with thick glove (≤ 5-mm thick)
  - Fingernail tracking
  - Large object rejection
  - Automatic baseline tracking to environmental changes
  - Field upgrades via bootloader
  - Manufacturing Test Kit (MTK)
  - Touchscreen sensor self-test
  - Low power wakeup button (< 50 µA)
- System performance (configuration dependent)
  - Screen sizes up to 15-inch diagonal
    - 6.0-mm electrode pitch; 16:10 aspect ratio
  - Up to 88 sense pins, 1836 intersections; 16:10 aspect ratio (34 TX × 54 RX)
  - Reports up to ten fingers
  - Small finger support down to 5 mm
  - Refresh rate up to 250 Hz; other rates configurable
  - TX frequency up to 350 kHz

Note
1. Effective voltage when using 17 multi-phase TX and 5-V V_{CCTX} supply.

Features

- Power (configuration-dependent)
  - 1.71 V to 1.95 V and 3.0 V to 5.5 V logic and digital I/Os supply
  - 3.0 V to 5.5 V analog supply
  - 30-mW average power
  - 30-µW typical deep-sleep power
- Sensor and system design (configuration-dependent)
  - Supports a variety of touchscreen sensors and stackups
    - Manhattan, diamond
    - Sensor-on-Lens (SOL)
    - Plastic (PET) and glass-sensor substrates
    - LCD, AMOLED, and IPS displays
    - Metal mesh
- Communication interface
  - I^2C slave at 100 kbps and 400 kbps
  - SPI slave bit rates up to 8 Mbps
- Package
  - 100-pin TQFP 14 × 14 × 1.4 mm (0.5-mm pitch)
  - 128-pin TQFP 14 × 20 × 1.4 mm (0.5-mm pitch)
- Ambient temperature range
  - Automotive-A: –40°C to 85°C
  - Automotive-S: –40°C to 105°C

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1 Touchscreen system overview

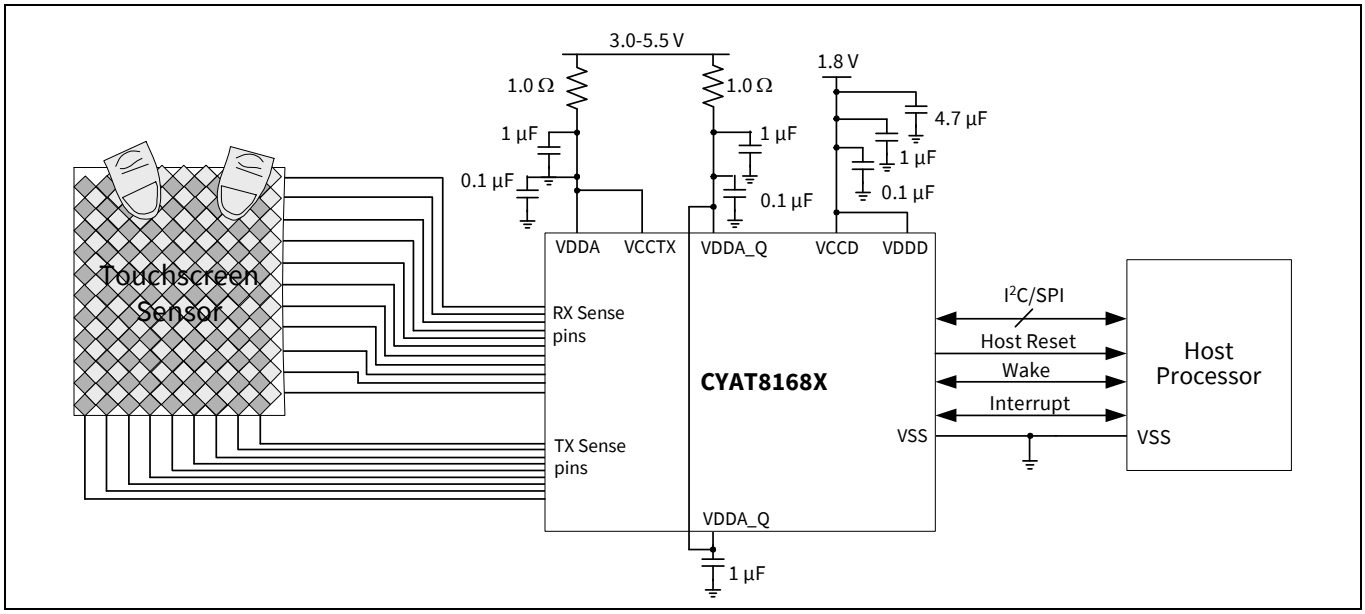


Figure 1 CYAT8168X typical system diagram

2 CYAT8168X overview

A capacitive touchscreen detects changes in capacitance to determine the location of one or more fingers on the surface of the touchscreen. A typical touchscreen system consists of a capacitive touchscreen sensor, an FPC bonded to the sensor, and the touchscreen controller mounted on the FPC. The FPC connects the touchscreen controller to the host processor. Users can interact with the displayed user interface through finger movements and gestures on the surface of the touchscreen.

CYAT8168X is a capacitive touchscreen controller with the sensing and processing technology to resolve the locations and report the positions of up to ten fingers on the touchscreen. The touchscreen controller converts an array of sensor capacitances into an array of digital values, which are processed by touch-detection and position-resolution algorithms in the controller. These algorithms determine the location and signal magnitude of each finger on the touchscreen.

Infineon provides:

- Application firmware
- Design guidance for the sensor and FPC
- Touchscreen sensor MTK

The CYAT8168X functional block diagram is shown in **Figure 2**. This device contains a high-performance Arm® 32-bit CPU with an integrated hardware multiply unit. This CPU controls all sensing and processing of measured capacitance results to allow tracking and reporting touches. The controller is optimized for low power and fast response time, with built-in support for manufacturing test. The touchscreen controller communicates with a host through an I^2C slave interface at up to 400 kbps or an SPI interface at up to 8 Mbps.

CYAT8168X collects the touchscreen sensor information using the touch subsystem. This touch subsystem consists of a 5-V TX pump, TX drivers, RX channels, and a programmable transmit/receive (TX/RX) multiplexer. The multiplexer electrically connects the analog front end of each RX channel and TX driver to the appropriate row and column electrodes of the touchscreen sensor.

The controller TX/RX multiplexer allows flexibility of chip placement on the FPC. All pins connecting to the touchscreen sensor are programmable as either TX or RX. Infineon reference documents are available under NDA through your local Infineon sales representative. You can also direct your requests to **automotive@infineon.com**.

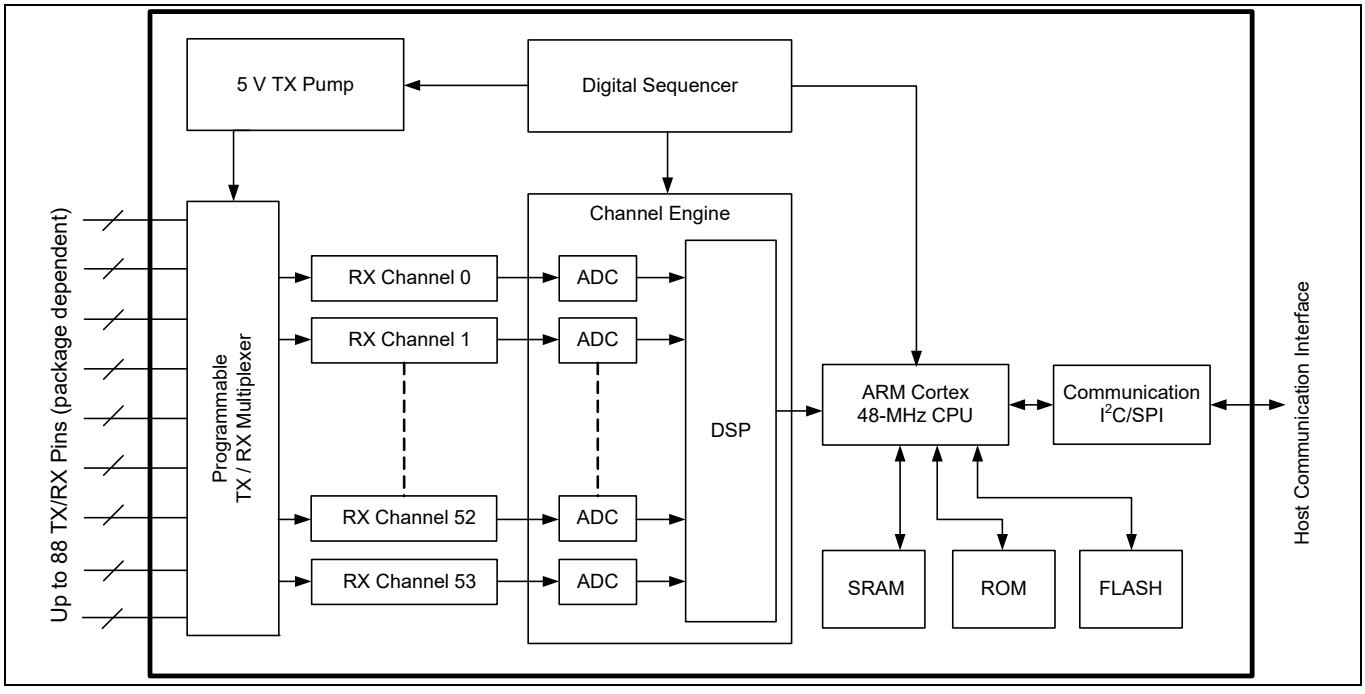


Figure 2 CYAT8168X functional block diagram

3 Features overview

3.1 AutoArmor

AutoArmor improves both electromagnetic emissions and immunity. It ensures no false finger touches when CYAT8168X is exposed to electromagnetic waves.

3.2 Water rejection

Water droplets can cause false touches to be reported. However, CYAT8168X continues to operate in the presence of water droplets or condensation. CYAT8168X enables water rejection using DualSense, Infineon's patented self- and mutual-capacitance sensing ability.

3.3 Wet-finger tracking

In a touchscreen system, moisture on fingers can cause false touches to be reported and make tracking of fingers across the screen difficult. CYAT8168X can detect and track fingers that are wet and enable more robust functionality of the touchscreen, using DualSense. This includes sweaty fingers touching the screen or fingers moving across a mist-covered screen.

3.4 Glove

CYAT8168X detects and tracks gloved fingers. Glove support allows navigating the touchscreen without having to remove gloves or without the use of expensive conductive gloves. Tracking of gloved fingers is supported by automatic mode switching, which automatically transitions between tracking gloved fingers and other touch-tracking modes. Ten-finger glove-touch is supported for thin gloves (≤ 1-mm thick) and two-finger operation is supported for thick gloves (≤ 5-mm thick).

3.5 Automatic mode switching

CYAT8168X supports automatic mode switching which detects and tracks a new touch object type without requiring manual selection of the touch type from the user. Automatic mode switching allows an uninterrupted user experience when switching between a bare finger, gloved finger, fingernail, or wet finger.

3.6 Large finger tracking

A well-designed touchscreen system must correctly report a large finger or thumb as only a single touch. If this is not supported, a large finger can incorrectly be reported as two or more touches, hampering the user experience. When an object, such as a thumb, is pressed against the touchscreen sensor, CYAT8168X ensures that only one touch is reported at the center of the object.

3.7 Large object detection and rejection

It is important to be able to detect the presence of a large object on the touchscreen sensor. Common example is touching a palm on the screen when typing. CYAT8168X can determine the presence of a large object, such as a fist or palm, from the touchscreen data. This presence may either be rejected or reported to the host.

3.8 Look-for-Touch

Look-for-touch is a low-power and fast-wakeup mode, in which the touchscreen sensor is measured for an increase in self-capacitance. An increase in self-capacitance indicates that a touch is present. Because it is only necessary to detect a finger's presence, and not location, the sensing can be done at a much lower SNR, requiring less time and power. Look-for-touch sensing is used to implement multiple functions, including wake-on-touch and fast first-touch response.

3.9 Low power wake-up button

Low-power wake-up button is a special mode for one dedicated button. In this mode, the host can send CYAT8168X to DeepSleep mode. Then, CYAT8168X regularly transitions to scan this single button. On detection of touch on this button, a WAKE pin is set to HIGH. The system can use this signal to control power switches and wake-up the whole system.

4 Touchscreen system specifications

This section specifies the touchscreen system performance delivered by CYAT8168X. For definitions, justification of parameters, and test methodologies, refer to the Infineon specification **PSoC™ Automotive Multitouch Touchscreen Controller User Interface Performance Definitions (001-49389)**[2].

4.1 System performance specifications

The system performance specifications in **Table 1**[3] and **Table 2**[4] are valid under these conditions: $-40°C \le T_A \le 85°C$[5] for Grade-A devices, $-40°C \le T_A \le 105°C$[5] for Grade-S devices; $1.71\ V \le V_{DDD} \le 1.95\ V$ or $3.0\ V \le V_{DDD} \le 5.5\ V$, $1.71\ V \le V_{CCD} \le 1.95\ V$, $3.0\ V \le V_{DDA} \le 5.5\ V$, unless otherwise noted. Typical values are specified at $T_A = 25°C$, $V_{DDD} = V_{CCD} = 1.8\ V$, core low dropout regulator (LDO) disabled, and $V_{DDA} = 3\ V$, unless otherwise noted. Data is validated using a 10.1-inch sensor with 4.2-mm electrode pitch. Contact the Infineon sales representative for information on the system performance conditions to guarantee the specifications provided in **Table 1**. The performance conditions and specifications are valid only for sensors approved by Infineon for use with CYAT8168X and produced by qualified Infineon partners. Contact **automotive@infineon.com** to discuss any deviations.

Table 1 Typical system performance specifications (Configuration dependent)

Category	Conditions	Core	Unit
Accuracy	5–12 mm diameter finger	0.5	mm
	Glove (≤ 1 mm thick)	2	
	Glove (1 < thick ≤ 5 mm)	4	
Linearity	5–12 mm diameter finger	0.25	
	Glove (≤ 1 mm thick)	2	
	Glove (1< thick ≤ 5 mm)	4	

Notes
2. Infineon reference documents are available under NDA through your local Infineon sales representative. You can also direct your requests to **automotive@infineon.com**.
3. Typical, as represented by 85% of the sample data measured. Accuracy is measured at points across the entire panel at 1.1-mm intervals. Linearity is measured on lines drawn across the panel (vertically, horizontally, and diagonally) separated by 1.1 mm.
4. Typical, as represented by the average values from the Infineon specification, PSoC™ Automotive Multitouch Touchscreen Controller User Interface Performance Definitions (001-49389).
5. System performance specifications are dependent on the combination of touch controller, display, touchscreen, and environment noise and temperature. Infineon guarantees the performance of the touch controller over this temperature range, but system performance may be impacted by the response of these other elements.

Table 2 System performance specifications (Configuration dependent)

Category	Description	Conditions	Min	Typ	Max	Unit
Jitter	Delta in reported X, Y position, for non-moving finger	5–12 mm diameter finger	–	0.4	–	mm
Refresh rate	–	One finger on panel	100	120	250[6]	Hz
Response time	Active response time	First finger down	–	–	30	ms
Low power wake-up button	Power consumption	3.3 V, 100 ms scan rate	–	50	–	µA
Power	In Active state	1 finger, 120-Hz refresh rate	–	–	120	mW
	In Active look-for-touch state	–	–	–	30	
	Average power[7]	Active state for 25% of touch activity and in deepsleep state for 75% of touch activity	–	30	–	
	In deepsleep state	–	–	30	–	µW

Notes
6. Requires setting TX pulses for mutual-cap and self-cap to 8 and no noise in the environment.
7. See **"Power States summary"** on page 16 for power state transition details and refresh interval configuration for each state. Average power is the power consumed during the active and deep sleep states, and is calculated using this equation: 0.25 × 120 mW + 0.75 × 0.030 mW = 30 mW.

5 System design options

5.1 CAPSENSE™ button/FPC support

The CYAT8168X controller supports a maximum of ten physical CAPSENSE™ buttons.

Detailed FPC development guidelines, including EMI shielding, are available in the **PSoC™ Automotive Multitouch Touchscreen Controller Module Design Best Practices (001-50467)**.

5.2 Sensors

Infineon supports the following sensor patterns:

- Single-solid diamond (SSD)
- Dual-solid diamond (DSD)
- Manhattan-3 (MH3)

Figure 3 through **Figure 5** show examples of SSD, DSD, and MH3 sensor patterns and unit cells.

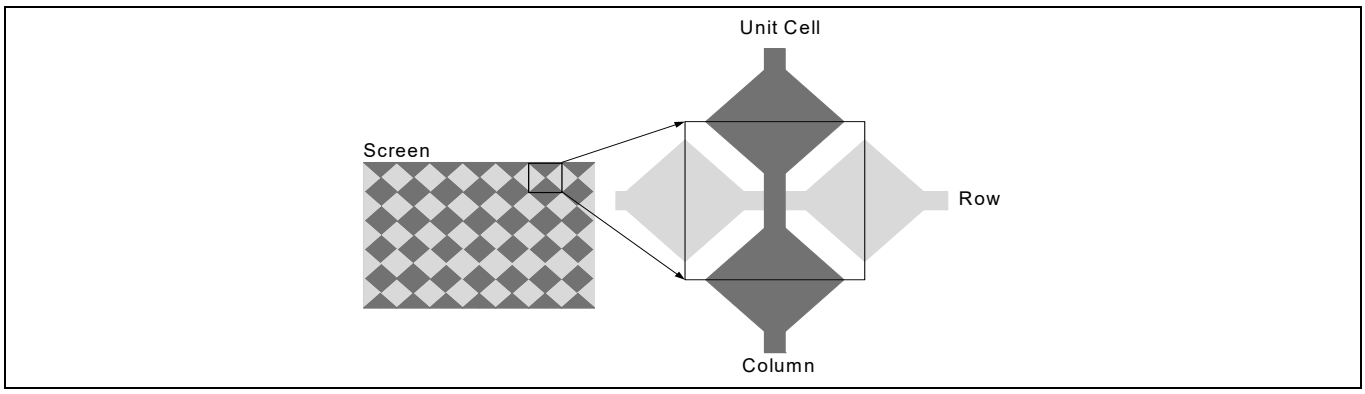


Figure 3 Single-solid diamond pattern and unit cell

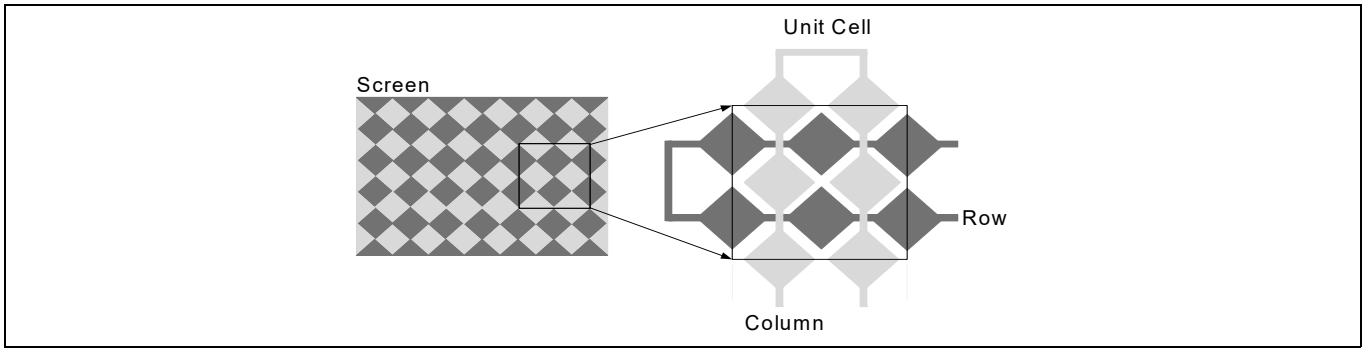


Figure 4 Dual-solid diamond unit cell

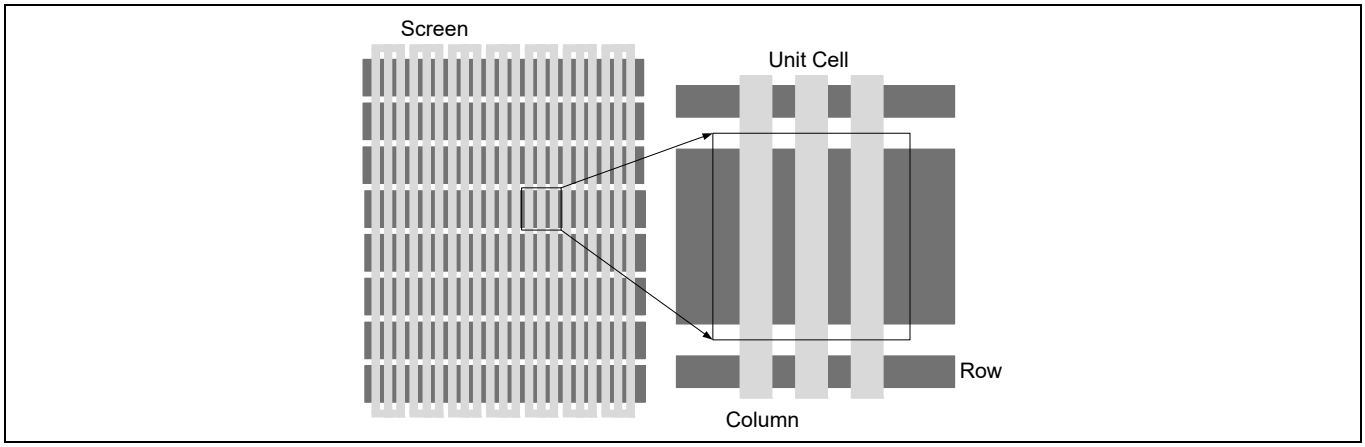


Figure 5 Manhattan-3 pattern and unit cell

Infineon continues to develop additional patterns and materials to increase performance and decrease system cost.

The specific sensor pattern used varies based on the mechanical, electrical, optical, and cost constraints; all of these factors must be considered for an optimal solution.

For example:

- Overlays/lens thickness < 1 mm should not use SSD due to large signal disparity (SD).
- DCVCOM LCDs, with strong image-related noise, require an air gap, a shield layer, or a self-shielding pattern such as MH3.

To learn more about how to design sensors using stackups and materials, see the **PSoC™ Automotive Multitouch Touchscreen Controller Module Design Best Practices (001-50467)**.

6 Power supply information

CYAT8168X contains five external power domains: VDDA, VDDA_Q, VDDD, VCCD, and VCCTX. VDDA supplies power to the chip's TX pump and drivers. VDDA_Q supplies power to the RX analog circuitry. VDDD supplies power to the digital I/Os, core LDO regulator, supply monitors, and external reset circuitry (XRES). VCCD supplies power to the CPU core, and may be configured as an input or output, depending on if a 1.71–1.95-V V_{DDD} supply is used.

6.1 Required external components

The touch controller device requires external components for proper device operation. Quantities are dependent on the power supply configuration used. External capacitors require an X5R dielectric characteristic or better. It is recommended to use an X7R dielectric characteristic or better for high-frequency 0.1-µF/0.22-µF capacitors.

VDDA:

- 1.0-Ω, 5% tolerance resistor
- 0.1-µF capacitor
- 1-µF capacitor

VDDA_Q:

- 0.1-µF capacitor (only required on one of the VDDA_Q pins)
- Two 1.0-µF capacitors (one at each end of the package)
- 1.0-Ω, 5% tolerance resistor

VDDD:

- 1-µF capacitor if VCCD and VDDD are connected (shown in **Figure 6** and **Figure 7**) or 0.1-µF capacitor if VDDD ≥ 3.0 V (shown in **Figure 8**, **Figure 9**, and **Figure 10**).

VCCD:

- 1-µF capacitor if VCCD and VDDD are connected (shown in **Figure 6** and **Figure 7**)
- 100-nF capacitor

VCCTX:

- 0.22-µF capacitor (configurations with the VCCTX pump enabled)

6.2 Voltage coefficient

The actual capacitance of external capacitors may be reduced with higher bias voltage. Check the capacitor datasheet for the voltage coefficient. Capacitors used for power supply decoupling or filtering are operated under a continuous DC-bias. Many capacitors used with DC power across them provide less than their target capacitance, and their capacitance is not constant across their working voltage range. When selecting capacitors for use with this device verify that the selected components provide the required capacitance under the specific operating conditions of temperature and voltage used in your design. While the temperature ratings of a capacitor are normally found as part of its catalog part number (for example, X7R, C0G, Y5V), the matching voltage coefficient may only be available on the component datasheet or direct from the manufacturer. Use of components that do not provide the required capacitance under the actual operating conditions may cause the device to perform to less than the datasheet specifications.

The available power configurations, with the TX pump enabled, are shown in **Figure 6** and **Figure 8**. **Figure 7**, **Figure 9** and **Figure 10** show power supply configurations with the TX pump disabled.

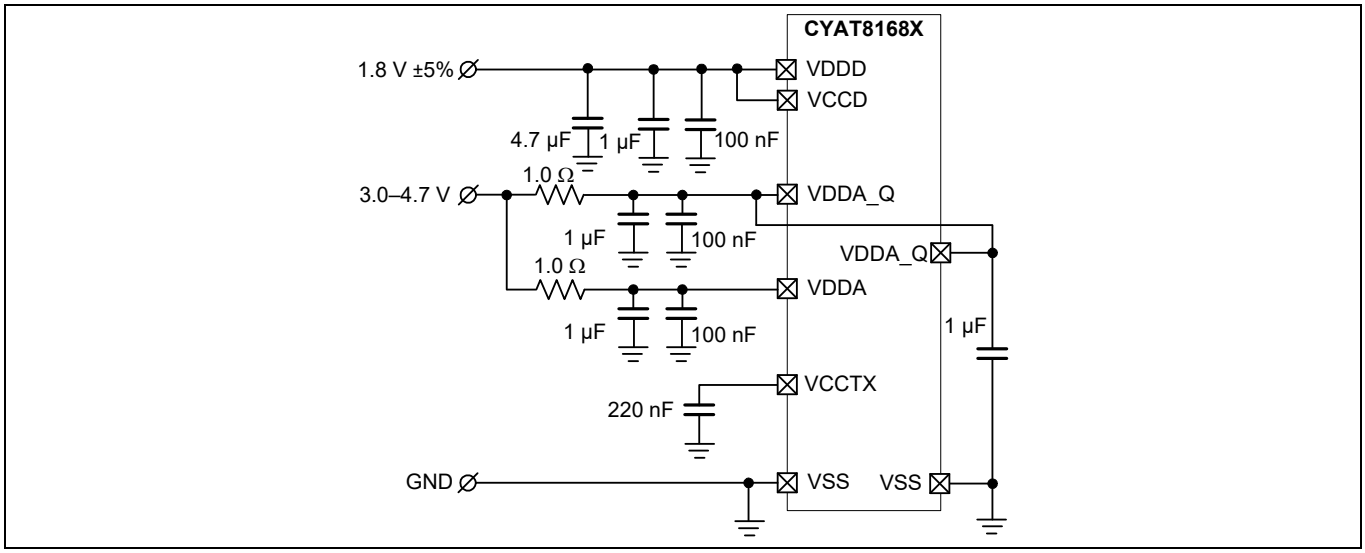


Figure 6 Dual supplies (inc. 1.8 V), TX pump enabled

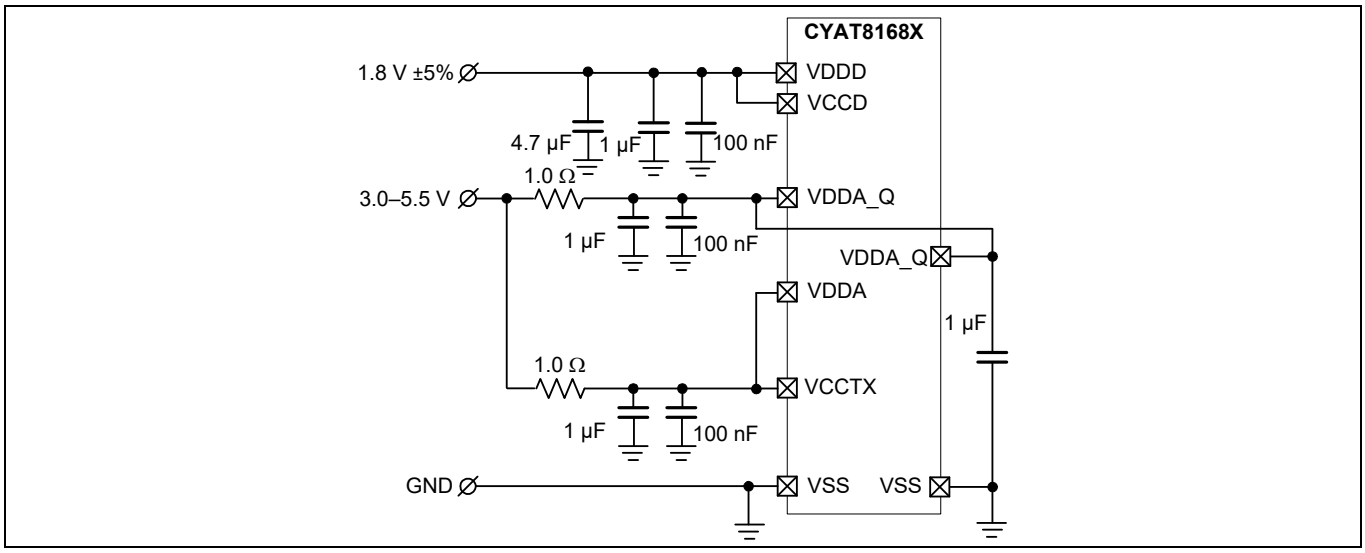


Figure 7 Dual supplies (inc. 1.8 V), TX pump disabled

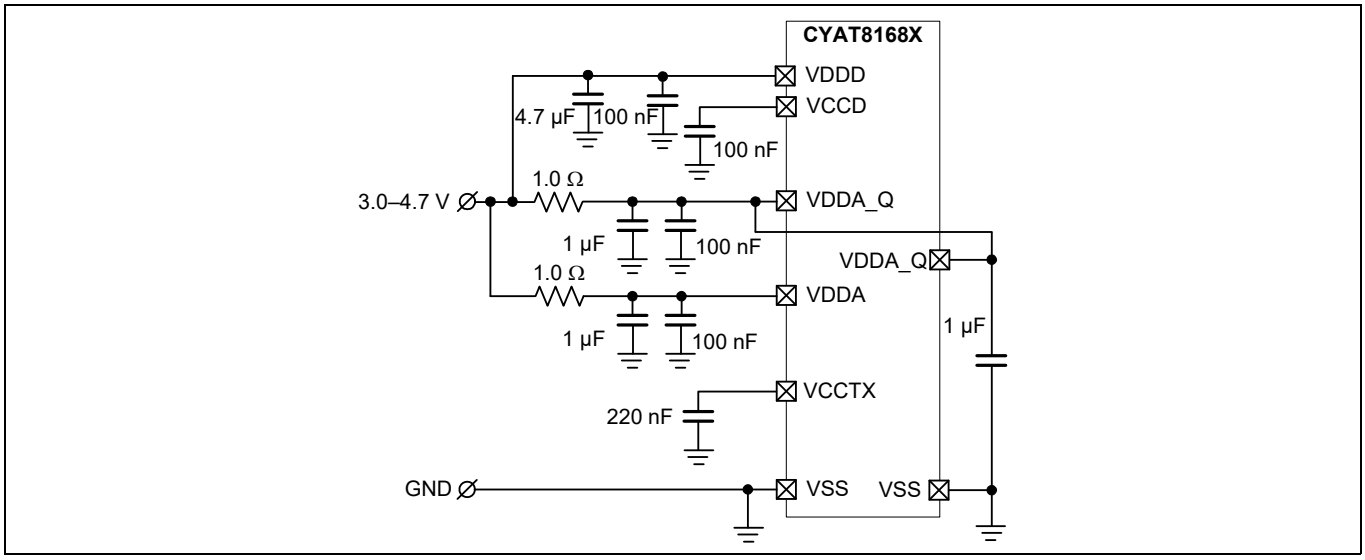


Figure 8 Single supply, TX pump enabled[8]

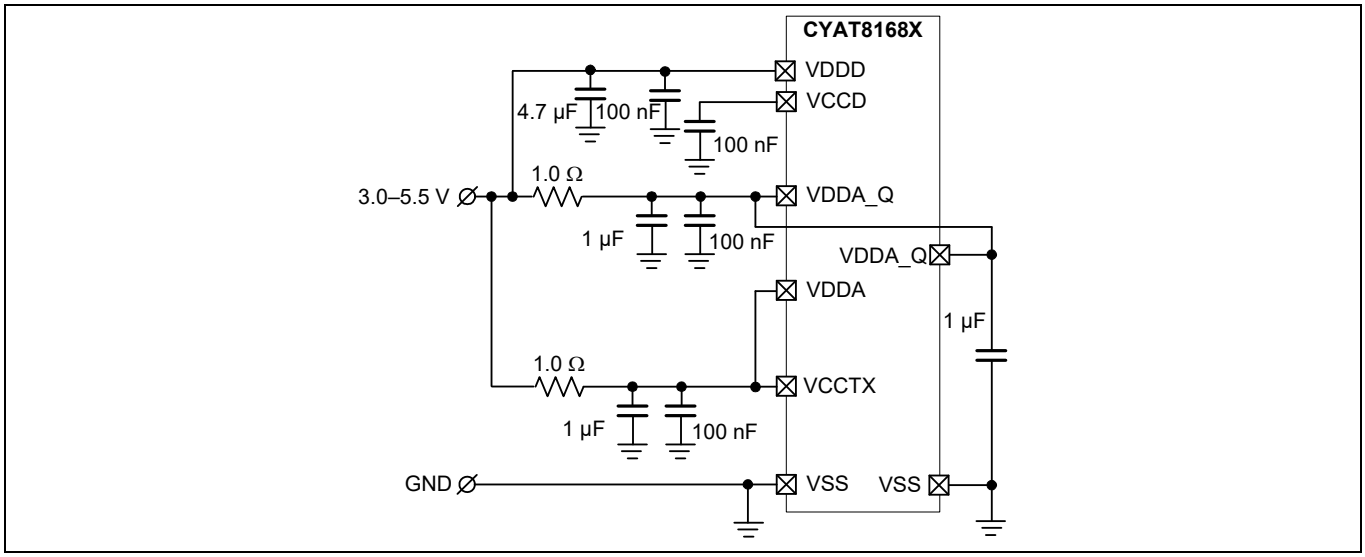


Figure 9 Single supply, TX pump disabled[8]

Note
8. 1.8-V communication is possible by using the 1.8-V mode for the digital inputs P0/P1/P2, when $V_{DDD} \geq 3.0$ V.

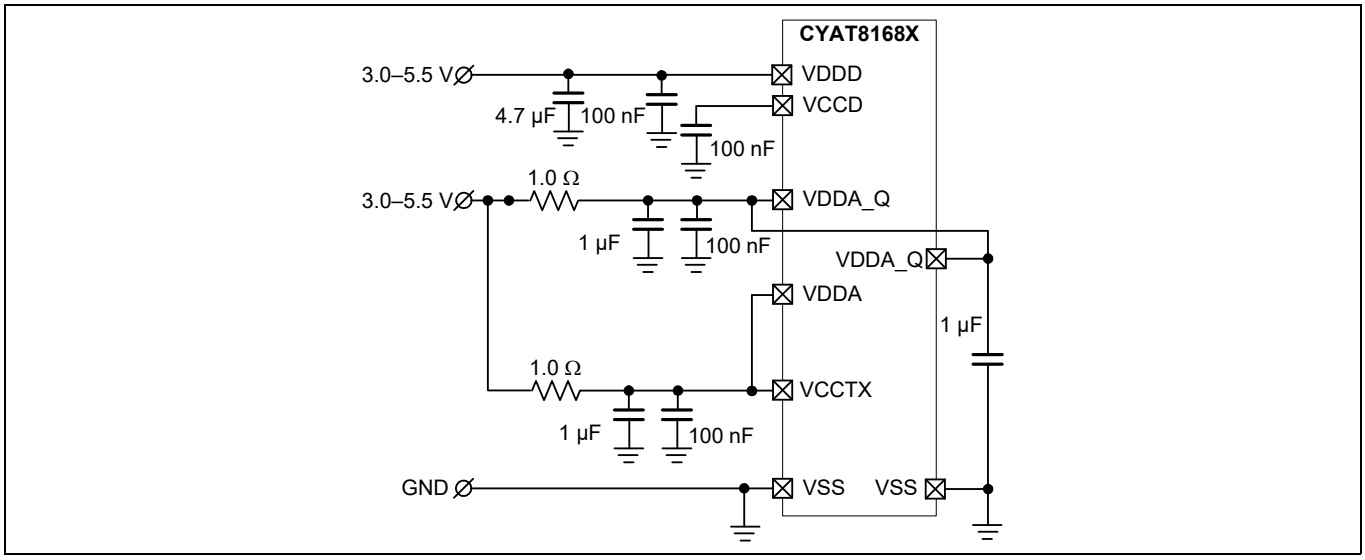


Figure 10 Dual supplies (no 1.8 V), TX pump disabled[9]

Note

9. V_{DDD} should be set to communication voltage (for example, 3.3 V) and V_{DDA} to some higher voltage (for example, 5 V).

7 Power States summary

The CYAT8168X controller has four power states, as illustrated in **Figure 11**:

- Active, where the touchscreen is actively scanned to determine the presence of a touch and identify the touch coordinates.
- Active look-for-touch, where the device performs fast self-capacitive scan to determine if a touch exists.
- Low power, where the touchscreen is scanned for touch presence at a much slower rate.
- Deepsleep, where the touchscreen is not scanned and CYAT8168X is in a low power state with no processing.

The CYAT8168X controller automatically manages transitions between three power states (Active, Active Look-for-touch, and Low Power). The host can force transition in and out of the fourth power state (Deepsleep).

The active state emphasizes low refresh time for accurate finger tracking, the active look-for-touch state allows fast first-touch response, and the low power state enables low power consumption during periods of no touch activity. In all three states, the CYAT8168X controller periodically scans the panel to determine the presence of a touch. If a touch is present, the controller either enters or remains in the active state where it identifies the touch coordinates. These tasks occur at different rates in the three states and the detection of touches affects transitions between the states. Transition from active to active look-for-touch occurs when no touch is detected.

Host can request to disable low power thus forcing CYAT8168X controller to stay out of the Low-Power state at all times for the fastest response to the first touch on the panel.

The following parameters configure power states, which can be configured by the host:

- Refresh interval (register ACT_INTRVL) sets the minimum time between the start of subsequent touchscreen scans in the active state.
- Active Look-for-touch interval (register ACT_LFT_INTRVL) sets the minimum refresh time in the active look-for-touch state.
- Active Mode Timeout (register TCH_TMOUT) sets the period of time in which no touch is detected during the Active Look-for-touch state before transitioning to the low power state.
- Low-Power interval (register LP_INTRVL) sets the time in the low power state between touchscreen scans.
- Deep Sleep is entered via a command from the host to move the device into the Deepsleep state. Automatic entry into the low power state is enabled by setting the LOW_POWER_ENABLE parameter.

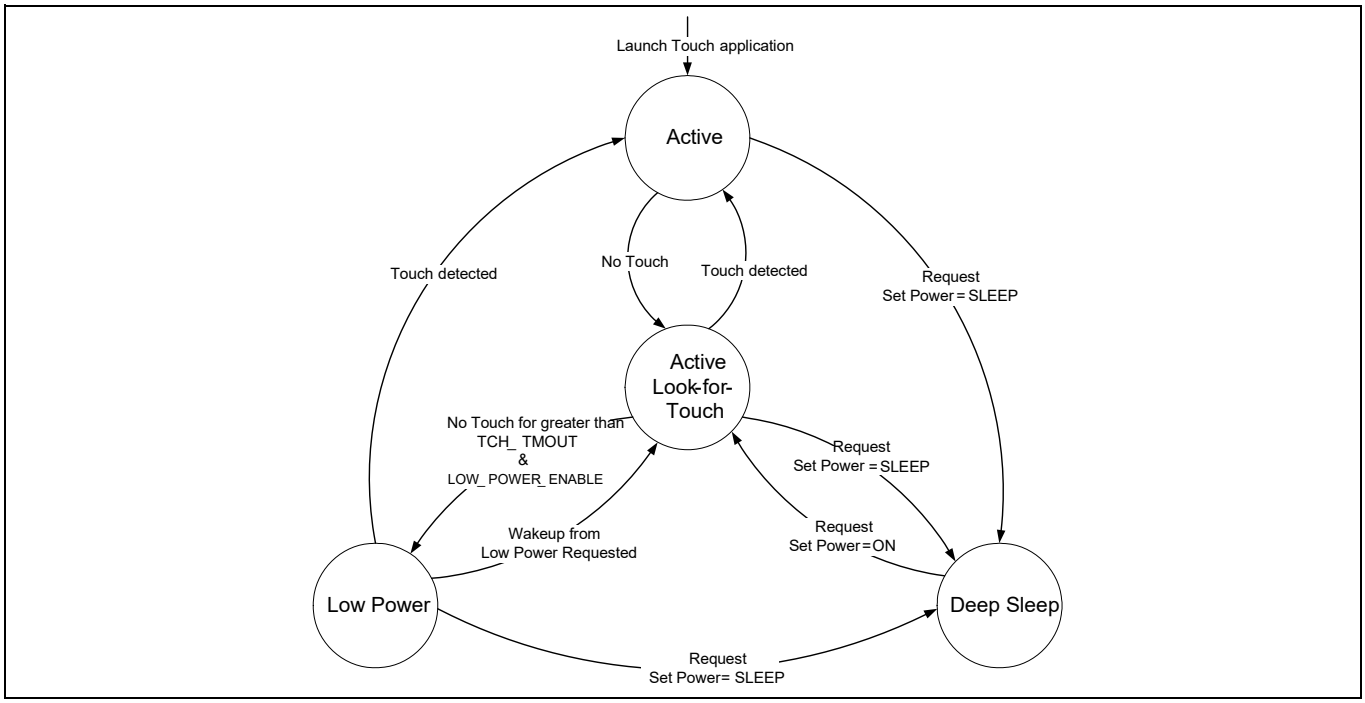


Figure 11 CYAT8168X power states and transitions

8 Pin information

CYAT8168X is available in both the 128-pin TQFP and 100-pin TQFP packages. This section lists pin names, descriptions, and mappings to the physical package. Input and output pins may have more than one possible configuration. Guidance for each configuration option is provided below:

XY: XY pins may be configured as either transmit (TX) drive or receive (RX) sense, allowing each design to be optimized based on the sensor pattern and layout. See **PSoC™ Automotive Multitouch Touchscreen Controller Module Design Best Practices (001-50467)**, for guidelines. Unused XY pins should be left unconnected. TX and RX pins are tied to VSS internally during the Deepsleep power state.

P0/P1/P2: Unused port 0, port 1, and port 2 pins should be left unconnected.

External Reset ($\overline{\text{XRES}}$): If the $\overline{\text{XRES}}$ pin is unused, it must be connected to V_{DDD} (either directly or through an external resistor).

SWD: Serial wire debug (SWD) is the recommended programming mode for all designs. If SWD is not used on the target board, use the bootloader to upgrade firmware.

Do Not Use (DNU): DNU pins must be left unconnected to ensure proper device operation.

COMM_INT: The COMM_INT pin is required. This interrupt pin is used for the host communication. If resistive mode is used, note that all I/Os are Hi-Z during chip initialization (after XRES or Bootloader Exit), so an additional external resistor is recommended.

P1[0] (WAKE): Wake pin indicates the status of the low-power wake-up button.

P1[1] (HOST RESET): The Host reset pin is used to send a reset pulse to the host controller on specific predefined conditions on the low-power wake-up button.

Pin configurations: Multiple pin configurations are supported using Touch Tuning Host Emulator (TTHE) software. Pins are configured using the TTHE Pin Configuration Wizard.

Table 3 128-pin TQFP, 88 sense I/O CYAT8168X[10]

Pin No.	Name	Digital	Analog	Description
1	XY32	–	I/O	TX or RX channel 15
2	XY31	–	I/O	TX or RX channel 14
3	XY30	–	I/O	TX or RX channel 13
4	XY29	–	I/O	TX or RX channel 12
5	XY28	–	I/O	TX or RX channel 11
6	DNU	–	–	Do not use
7	DNU	–	–	Do not use
8	XY27	–	I/O	TX or RX channel 10
9	XY26	–	I/O	TX or RX channel 9
10	XY25	–	I/O	TX or RX channel 8
11	XY24	–	I/O	TX or RX channel 7
12	XY23	–	I/O	TX or RX channel 6
13	XY22	–	I/O	TX or RX channel 5
14	XY21	–	I/O	TX or RX channel 4
15	XY20	–	I/O	TX or RX channel 3
16	XY19	–	I/O	TX or RX channel 2
17	XY18	–	I/O	TX or RX channel 1
18	XY17	–	I/O	TX or RX channel 0
19	XY16	–	I/O	TX or RX channel 26
20	XY15	–	I/O	TX or RX channel 25
21	XY14	–	I/O	TX or RX channel 24
22	XY13	–	I/O	TX or RX channel 23
23	XY12	–	I/O	TX or RX channel 22
24	XY11	–	I/O	TX or RX channel 21
25	XY10	–	I/O	TX or RX channel 20
26	XY09	–	I/O	TX or RX channel 19
27	XY08	–	I/O	TX or RX channel 18
28	XY07	–	I/O	TX or RX channel 17
29	XY06	–	I/O	TX or RX channel 16
30	XY05	–	I/O	TX or RX channel 15
31	XY04	–	I/O	TX or RX channel 14
32	XY03	–	I/O	TX or RX channel 13
33	XY02	–	I/O	TX or RX channel 12
34	XY01	–	I/O	TX or RX channel 11
35	XY00	–	I/O	TX or RX channel 10

Note
10.See **“Pin information”** on page 18 for details on pin configuration.

Table 3 128-pin TQFP, 88 sense I/O CYAT8168X[10] (continued)

Pin No.	Name	Digital	Analog	Description
36	VSS	Power		Connect to ground
37	DNU	–	–	Do not use
38	DNU	–	–	Do not use
39	XRES	–	–	External active LOW reset
40	P0[0]	I/O	–	I2C SCL / SPI SCLK
41	P0[1]	I/O	–	I2C SDA / SPI MOSI
42	P1[0]	I/O	–	COMM_INT / SPI MISO / WAKE
43	P1[1]	I/O	–	COMM_INT / SPI SS
44	P1[2]	I/O	–	EXT_SYNC (External sync signal output)
45	P1[3]	I/O	–	EXT_START (External start signal LCD display V-/H- sync)
46	P1[4]	I/O	–	ERROR - Set HIGH when internal error is detected
47	P1[5]	I/O	–	Reserved
48	P1[6]	I/O	–	COMM_INT
49	P2[0]	I/O	–	SWDIO
50	P2[1]	I/O	–	SWDCLK
51	VCCD	Power		Digital core power supply input/output
52	VDDD	Power		Digital power supply input
53	VDDD	Power		Digital power supply input
54	VDDD	Power		Digital power supply input
55	VSS	Power		Connect to ground
56	VSS	Power		Connect to ground
57	VSS	Power		Connect to ground
58	VSS	Power		Connect to ground
59	VSS	Power		Connect to ground
60	VSS	Power		Connect to ground
61	VDDA	Power		TX analog power supply input
62	VDDA_Q	Power		RX analog power supply input
63	VCCTX	Power		TX pump reservoir and filter capacitor connection point
64	XY87	–	I/O	TX or RX channel 43
65	XY86	–	I/O	TX or RX channel 42
66	XY85	–	I/O	TX or RX channel 41
67	XY84	–	I/O	TX or RX channel 40
68	DNU	–	–	Do not use
69	DNU	–	–	Do not use
70	XY83	–	I/O	TX or RX channel 39
71	XY82	–	I/O	TX or RX channel 38

Note
10.See **"Pin information"** on page 18 for details on pin configuration.

Table 3 128-pin TQFP, 88 sense I/O CYAT8168X[10] (continued)

Pin No.	Name	Digital	Analog	Description
72	XY81	–	I/O	TX or RX channel 37
73	XY80	–	I/O	TX or RX channel 36
74	XY79	–	I/O	TX or RX channel 35
75	XY78	–	I/O	TX or RX channel 34
76	XY77	–	I/O	TX or RX channel 33
77	VSS	Power		Connect to ground
78	XY76	–	I/O	TX or RX channel 32
79	XY75	–	I/O	TX or RX channel 31
80	XY74	–	I/O	TX or RX channel 30
81	XY73	–	I/O	TX or RX channel 29
82	XY72	–	I/O	TX or RX channel 28
83	XY71	–	I/O	TX or RX channel 27
84	XY70	–	I/O	TX or RX channel 53
85	XY69	–	I/O	TX or RX channel 52
86	XY68	–	I/O	TX or RX channel 51
87	XY67	–	I/O	TX or RX channel 50
88	XY66	–	I/O	TX or RX channel 49
89	XY65	–	I/O	TX or RX channel 48
90	XY64	–	I/O	TX or RX channel 47
91	XY63	–	I/O	TX or RX channel 46
92	XY62	–	I/O	TX or RX channel 45
93	XY61	–	I/O	TX or RX channel 44
94	DNU	–	–	Do not use
95	DNU	–	–	Do not use
96	DNU	–	–	Do not use
97	DNU	–	–	Do not use
98	XY60	–	I/O	TX or RX channel 43
99	XY59	–	I/O	TX or RX channel 42
100	XY58	–	I/O	TX or RX channel 41
101	XY57	–	I/O	TX or RX channel 40
102	XY56	–	I/O	TX or RX channel 39
103	XY55	–	I/O	TX or RX channel 38
104	XY54	–	I/O	TX or RX channel 37
105	XY53	–	I/O	TX or RX channel 36
106	XY52	–	I/O	TX or RX channel 35
107	XY51	–	I/O	TX or RX channel 34

Note
10.See **"Pin information"** on page 18 for details on pin configuration.

Table 3 128-pin TQFP, 88 sense I/O CYAT8168X[10] (continued)

Pin No.	Name	Digital	Analog	Description
108	XY50	–	I/O	TX or RX channel 33
109	XY49	–	I/O	TX or RX channel 32
110	XY48	–	I/O	TX or RX channel 31
111	XY47	–	I/O	TX or RX channel 30
112	XY46	–	I/O	TX or RX channel 29
113	XY45	–	I/O	TX or RX channel 28
114	XY44	–	I/O	TX or RX channel 27
115	VDDA_Q	Power		RX analog power supply input
116	VSS	Power		Connect to ground
117	VSS	Power		Connect to ground
118	XY43	–	I/O	TX or RX channel 26
119	XY42	–	I/O	TX or RX channel 25
120	XY41	–	I/O	TX or RX channel 24
121	XY40	–	I/O	TX or RX channel 23
122	XY39	–	I/O	TX or RX channel 22
123	XY38	–	I/O	TX or RX channel 21
124	XY37	–	I/O	TX or RX channel 20
125	XY36	–	I/O	TX or RX channel 19
126	XY35	–	I/O	TX or RX channel 18
127	XY34	–	I/O	TX or RX channel 17
128	XY33	–	I/O	TX or RX channel 16

Note
10.See **“Pin information”** on page 18 for details on pin configuration.

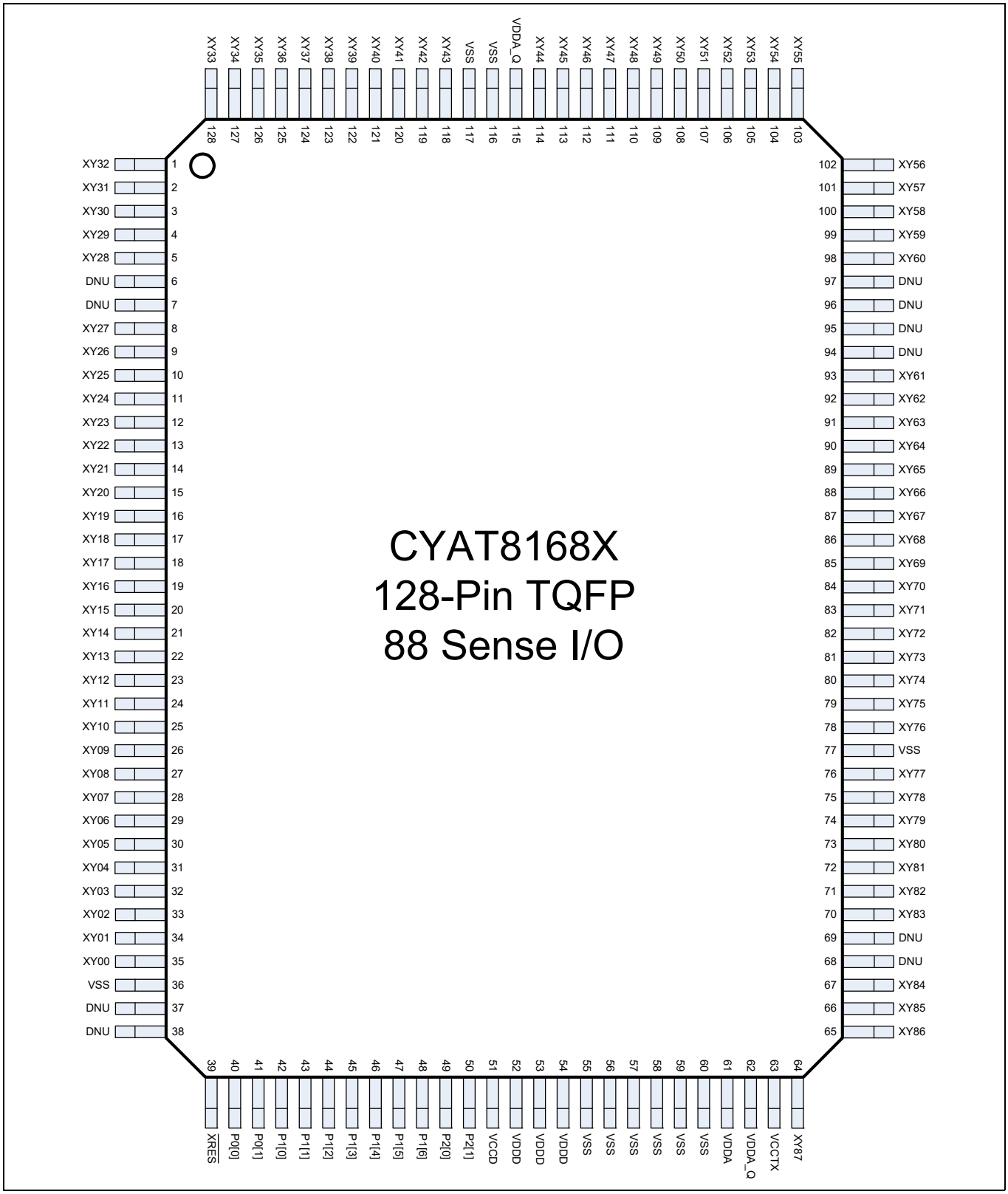


Figure 12 128-pin TQFP, 88 sense I/O CYAT8168X

Table 4 100-pin TQFP, 77 sense I/O CYAT8168X[11]

Pin No.	Name	Digital	Analog	Description
1	XY26	–	I/O	TX or RX channel 9
2	XY25	–	I/O	TX or RX channel 8
3	XY24	–	I/O	TX or RX channel 7
4	XY23	–	I/O	TX or RX channel 6
5	XY22	–	I/O	TX or RX channel 5
6	XY21	–	I/O	TX or RX channel 4
7	XY20	–	I/O	TX or RX channel 3
8	XY19	–	I/O	TX or RX channel 2
9	XY18	–	I/O	TX or RX channel 1
10	XY17	–	I/O	TX or RX channel 0
11	XY16	–	I/O	TX or RX channel 26
12	XY15	–	I/O	TX or RX channel 25
13	XY14	–	I/O	TX or RX channel 24
14	XY13	–	I/O	TX or RX channel 23
15	XY12	–	I/O	TX or RX channel 22
16	XY11	–	I/O	TX or RX channel 21
17	XY10	–	I/O	TX or RX channel 20
18	XY09	–	I/O	TX or RX channel 19
19	XY08	–	I/O	TX or RX channel 18
20	XY07	–	I/O	TX or RX channel 17
21	XY06	–	I/O	TX or RX channel 16
22	XY05	–	I/O	TX or RX channel 15
23	XY04	–	I/O	TX or RX channel 14
24	XY03	–	I/O	TX or RX channel 13
25	XY02	–	I/O	TX or RX channel 12
26	XY01	–	I/O	TX or RX channel 11
27	XY00	–	I/O	TX or RX channel 10
28	VSS	Power		Connect to ground
29	XRES	I	–	External active LOW reset
30	P0[0]	I/O	–	I2C SCL / SPI SCLK
31	P0[1]	I/O	–	I2C SDA / SPI MOSI
32	P1[0]	I/O	–	COMM_INT / SPI MISO / WAKE
33	P1[1]	I/O	–	COMM_INT / SPI SS
34	P1[2]	I/O	–	EXT_SYNC (External sync signal output)
35	P1[3]	I/O	–	EXT_START (External start signal LCD display V-/H- sync)
36	P1[4]	I/O	–	ERROR - Set HIGH when internal error is detected

Note
11.See “**Pin information**” on page 11 for details on pin configuration.

Table 4 100-pin TQFP, 77 sense I/O CYAT8168X[11] (continued)

Pin No.	Name	Digital	Analog	Description
37	P1[5]	I/O	–	Reserved
38	P1[6]	I/O	–	COMM_INT
39	P2[0]	I/O	–	SWDIO
40	P2[1]	I/O	–	SWDCLK
41	VCCD	Power		Digital core power supply input/output
42	VDDD	Power		Digital power supply input
43	VSS	Power		Connect to ground
44	VSS	Power		Connect to ground
45	VDDA	Power		TX analog power supply input
46	VDDA_Q	Power		RX analog power supply input
47	VCCTX	Power		TX pump reservoir and filter capacitor connection point
48	XY76	–	I/O	TX or RX channel 42
49	XY75	–	I/O	TX or RX channel 41
50	XY74	–	I/O	TX or RX channel 40
51	XY73	–	I/O	TX or RX channel 39
52	XY72	–	I/O	TX or RX channel 38
53	XY71	–	I/O	TX or RX channel 37
54	XY70	–	I/O	TX or RX channel 36
55	XY69	–	I/O	TX or RX channel 35
56	XY68	–	I/O	TX or RX channel 34
57	XY67	–	I/O	TX or RX channel 33
58	VSS	Power		Connect to ground
59	XY66	–	I/O	TX or RX channel 32
60	XY65	–	I/O	TX or RX channel 31
61	XY64	–	I/O	TX or RX channel 30
62	XY63	–	I/O	TX or RX channel 29
63	XY62	–	I/O	TX or RX channel 28
64	XY61	–	I/O	TX or RX channel 27
65	XY60	–	I/O	TX or RX channel 53
66	XY59	–	I/O	TX or RX channel 52
67	XY58	–	I/O	TX or RX channel 51
68	XY57	–	I/O	TX or RX channel 50
69	XY56	–	I/O	TX or RX channel 49
70	XY55	–	I/O	TX or RX channel 48
71	XY54	–	I/O	TX or RX channel 47
72	XY53	–	I/O	TX or RX channel 46
73	XY52	–	I/O	TX or RX channel 45

Note
11.See “**Pin information**” on page 11 for details on pin configuration.

Table 4 100-pin TQFP, 77 sense I/O CYAT8168X[11] (continued)

Pin No.	Name	Digital	Analog	Description
74	XY51	–	I/O	TX or RX channel 44
75	XY50	–	I/O	TX or RX channel 43
76	XY49	–	I/O	TX or RX channel 42
77	XY48	–	I/O	TX or RX channel 41
78	XY47	–	I/O	TX or RX channel 40
79	XY46	–	I/O	TX or RX channel 39
80	XY45	–	I/O	TX or RX channel 38
81	XY44	–	I/O	TX or RX channel 37
82	XY43	–	I/O	TX or RX channel 36
83	XY42	–	I/O	TX or RX channel 35
84	XY41	–	I/O	TX or RX channel 34
85	VDDA_Q	Power		RX analog power supply input
86	VSS	Power		Connect to ground
87	XY40	–	I/O	TX or RX channel 23
88	XY39	–	I/O	TX or RX channel 22
89	XY38	–	I/O	TX or RX channel 21
90	XY37	–	I/O	TX or RX channel 20
91	XY36	–	I/O	TX or RX channel 19
92	XY35	–	I/O	TX or RX channel 18
93	XY34	–	I/O	TX or RX channel 17
94	XY33	–	I/O	TX or RX channel 16
95	XY32	–	I/O	TX or RX channel 15
96	XY31	–	I/O	TX or RX channel 14
97	XY30	–	I/O	TX or RX channel 13
98	XY29	–	I/O	TX or RX channel 12
99	XY28	–	I/O	TX or RX channel 11
100	XY27	–	I/O	TX or RX channel 10

Note
11.See “**Pin information**” on page 11 for details on pin configuration.

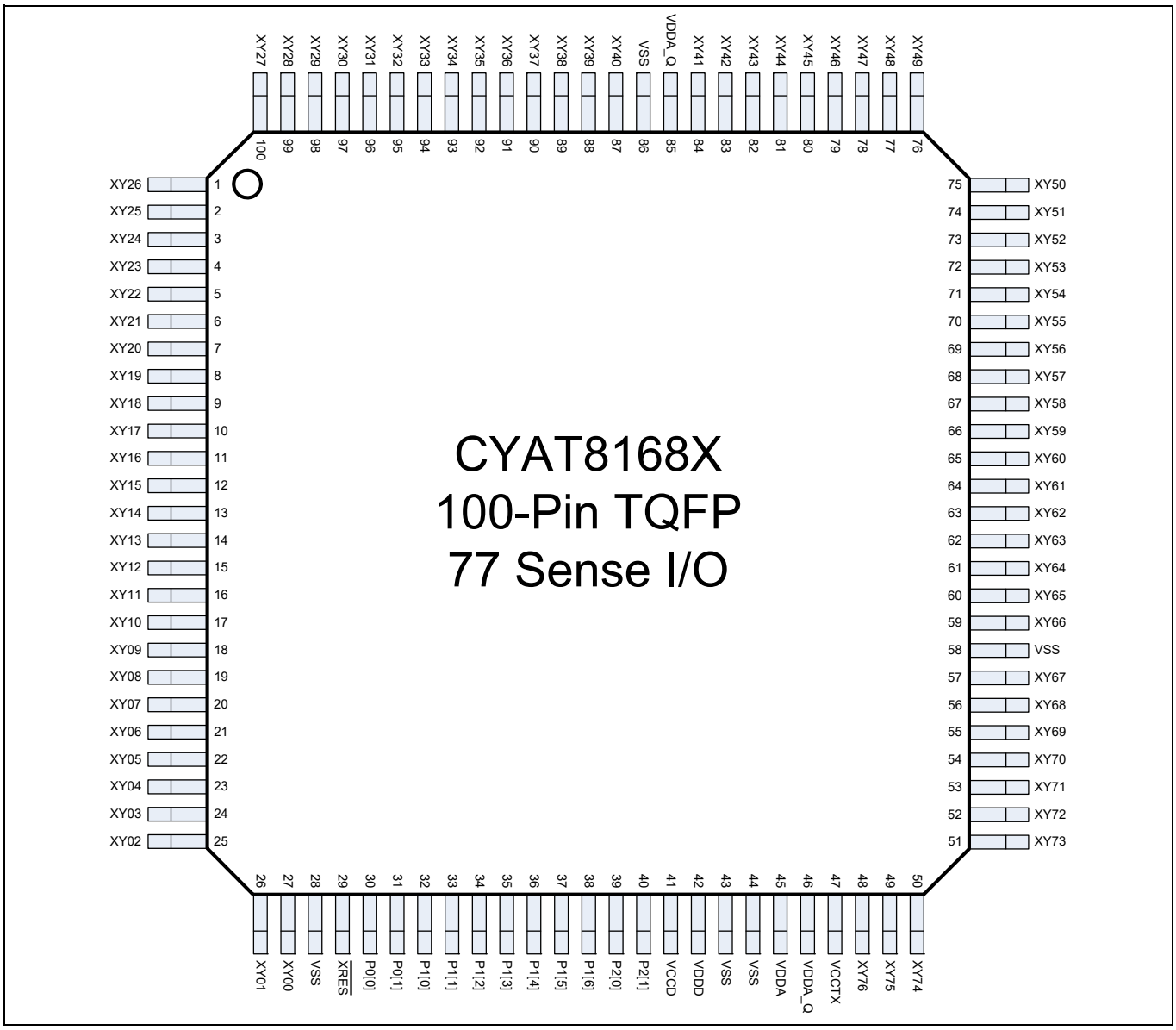


Figure 13 100-pin TQFP, 77 sense I/O CYAT8168X

Table 5 100-pin TQFP, 71 sense I/O CYAT8168X[12]

Pin No.	Name	Digital	Analog	Description
1	XY20	–	I/O	TX or RX channel 9
2	XY19	–	I/O	TX or RX channel 8
3	XY18	–	I/O	TX or RX channel 7
4	XY17	–	I/O	TX or RX channel 6
5	XY16	–	I/O	TX or RX channel 5
6	XY15	–	I/O	TX or RX channel 4
7	XY14	–	I/O	TX or RX channel 3
8	XY13	–	I/O	TX or RX channel 2
9	XY12	–	I/O	TX or RX channel 1
10	XY11	–	I/O	TX or RX channel 0
11	XY10	–	I/O	TX or RX channel 26
12	XY09	–	I/O	TX or RX channel 25
13	XY08	–	I/O	TX or RX channel 24
14	XY07	–	I/O	TX or RX channel 23
15	XY06	–	I/O	TX or RX channel 22
16	XY05	–	I/O	TX or RX channel 21
17	XY04	–	I/O	TX or RX channel 20
18	XY03	–	I/O	TX or RX channel 19
19	XY02	–	I/O	TX or RX channel 18
20	XY01	–	I/O	TX or RX channel 17
21	XY00	–	I/O	TX or RX channel 16
22	DNU	–	–	Do not use
23	DNU	–	–	Do not use
24	DNU	–	–	Do not use
25	DNU	–	–	Do not use
26	DNU	–	–	Do not use
27	DNU	–	–	Do not use
28	VSS	Power		Connect to ground
29	XRES	I	–	External active LOW reset
30	P0[0]	I/O	–	I2C SCL / SPI SCLK
31	P0[1]	I/O	–	I2C SDA / SPI MOSI
32	P1[0]	I/O	–	COMM_INT / SPI MISO / WAKE
33	P1[1]	I/O	–	COMM_INT / SPI SS
34	P1[2]	I/O	–	EXT_SYNC (External sync signal output)
35	P1[3]	I/O	–	EXT_START (External start signal LCD display V-/H- sync)
36	P1[4]	I/O	–	ERROR - Set HIGH when internal error is detected

Note
12.See “**Pin information**” on page 11 for details on pin configuration.

Table 5 100-pin TQFP, 71 sense I/O CYAT8168X[12] (continued)

Pin No.	Name	Digital	Analog	Description
37	P1[5]	I/O	–	Reserved
38	P1[6]	I/O	–	COMM_INT
39	P2[0]	I/O	–	SWDIO
40	P2[1]	I/O	–	SWDCLK
41	VCCD	Power		Digital core power supply input/output
42	VDDD	Power		Digital power supply input
43	VSS	Power		Connect to ground
44	VSS	Power		Connect to ground
45	VDDA	Power		TX analog power supply input
46	VDDA_Q	Power		RX analog power supply input
47	VCCTX	Power		TX pump reservoir and filter capacitor connection point
48	XY70	–	I/O	TX or RX channel 42
49	XY69	–	I/O	TX or RX channel 41
50	XY68	–	I/O	TX or RX channel 40
51	XY67	–	I/O	TX or RX channel 39
52	XY66	–	I/O	TX or RX channel 38
53	XY65	–	I/O	TX or RX channel 37
54	XY64	–	I/O	TX or RX channel 36
55	XY63	–	I/O	TX or RX channel 35
56	XY62	–	I/O	TX or RX channel 34
57	XY61	–	I/O	TX or RX channel 33
58	VSS	Power		Connect to ground
59	XY60	–	I/O	TX or RX channel 32
60	XY59	–	I/O	TX or RX channel 31
61	XY58	–	I/O	TX or RX channel 30
62	XY57	–	I/O	TX or RX channel 29
63	XY56	–	I/O	TX or RX channel 28
64	XY55	–	I/O	TX or RX channel 27
65	XY54	–	I/O	TX or RX channel 53
66	XY53	–	I/O	TX or RX channel 52
67	XY52	–	I/O	TX or RX channel 51
68	XY51	–	I/O	TX or RX channel 50
69	XY50	–	I/O	TX or RX channel 49
70	XY49	–	I/O	TX or RX channel 48
71	XY48	–	I/O	TX or RX channel 47
72	XY47	–	I/O	TX or RX channel 46
73	XY46	–	I/O	TX or RX channel 45

Note
12.See “**Pin information**” on page 11 for details on pin configuration.

Table 5 100-pin TQFP, 71 sense I/O CYAT8168X[12] (continued)

Pin No.	Name	Digital	Analog	Description
74	XY45	–	I/O	TX or RX channel 44
75	XY44	–	I/O	TX or RX channel 43
76	XY43	–	I/O	TX or RX channel 42
77	XY42	–	I/O	TX or RX channel 41
78	XY41	–	I/O	TX or RX channel 40
79	XY40	–	I/O	TX or RX channel 39
80	XY39	–	I/O	TX or RX channel 38
81	XY38	–	I/O	TX or RX channel 37
82	XY37	–	I/O	TX or RX channel 36
83	XY36	–	I/O	TX or RX channel 35
84	XY35	–	I/O	TX or RX channel 34
85	VDDA_Q	Power		RX analog power supply input
86	VSS	Power		Connect to ground
87	XY34	–	I/O	TX or RX channel 23
88	XY33	–	I/O	TX or RX channel 22
89	XY32	–	I/O	TX or RX channel 21
90	XY31	–	I/O	TX or RX channel 20
91	XY30	–	I/O	TX or RX channel 19
92	XY29	–	I/O	TX or RX channel 18
93	XY28	–	I/O	TX or RX channel 17
94	XY27	–	I/O	TX or RX channel 16
95	XY26	–	I/O	TX or RX channel 15
96	XY25	–	I/O	TX or RX channel 14
97	XY24	–	I/O	TX or RX channel 13
98	XY23	–	I/O	TX or RX channel 12
99	XY22	–	I/O	TX or RX channel 11
100	XY21	–	I/O	TX or RX channel 10

Note
12.See “**Pin information**” on page 11 for details on pin configuration.

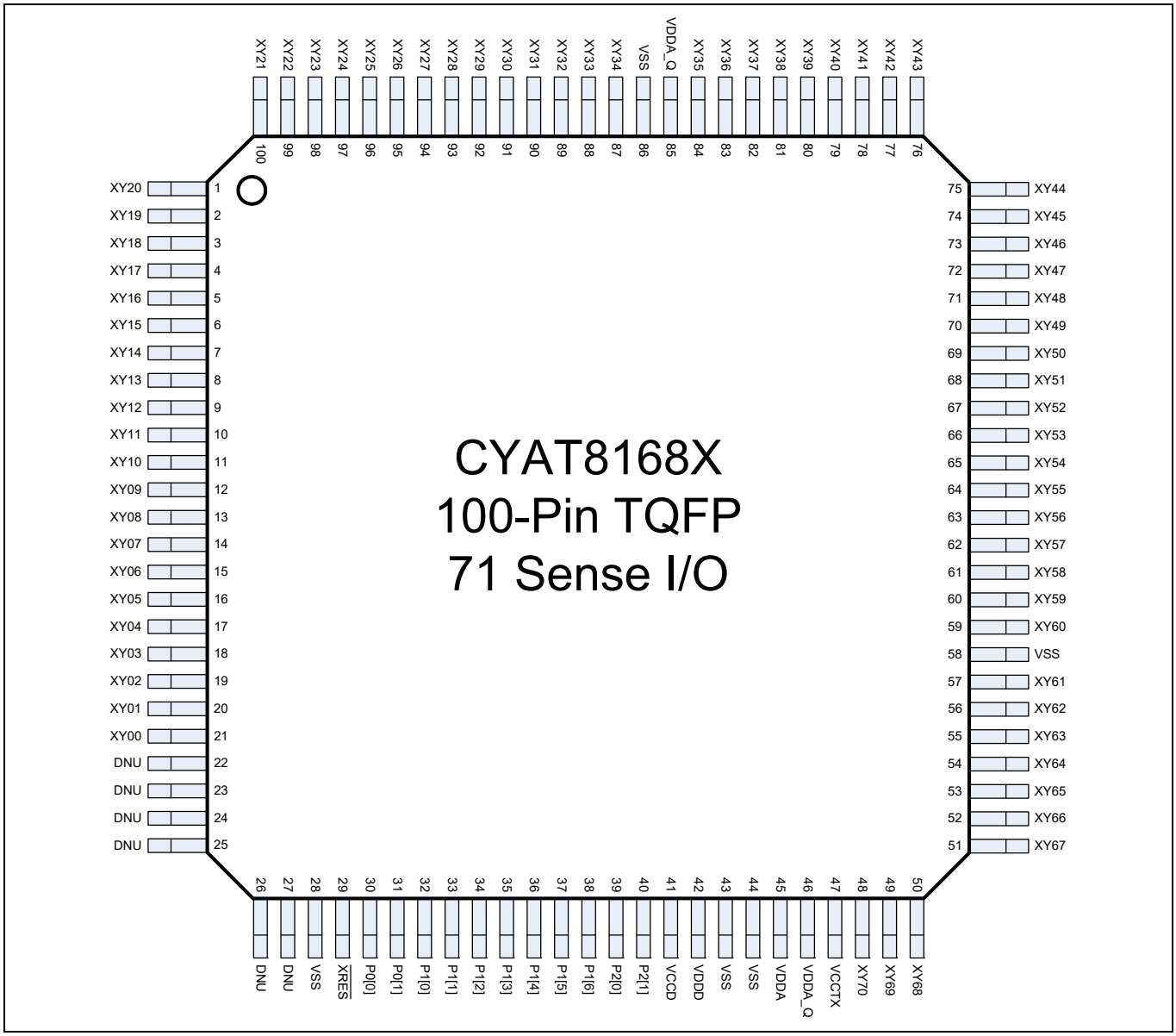


Figure 14 100-pin TQFP, 71 sense I/O CYAT8168X

Table 6 100-pin TQFP, 61 sense I/O CYAT8168X[13]

Pin No.	Name	Digital	Analog	Description
1	XY15	–	I/O	TX or RX channel 9
2	XY14	–	I/O	TX or RX channel 8
3	XY13	–	I/O	TX or RX channel 7
4	XY12	–	I/O	TX or RX channel 6
5	XY11	–	I/O	TX or RX channel 5
6	XY10	–	I/O	TX or RX channel 4
7	XY09	–	I/O	TX or RX channel 3
8	XY08	–	I/O	TX or RX channel 2
9	XY07	–	I/O	TX or RX channel 1
10	XY06	–	I/O	TX or RX channel 0
11	XY05	–	I/O	TX or RX channel 26
12	XY04	–	I/O	TX or RX channel 25
13	XY03	–	I/O	TX or RX channel 24
14	XY02	–	I/O	TX or RX channel 23
15	XY01	–	I/O	TX or RX channel 22
16	XY00	–	I/O	TX or RX channel 21
17	DNU	–	–	Do not use
18	DNU	–	–	Do not use
19	DNU	–	–	Do not use
20	DNU	–	–	Do not use
21	DNU	–	–	Do not use
22	DNU	–	–	Do not use
23	DNU	–	–	Do not use
24	DNU	–	–	Do not use
25	DNU	–	–	Do not use
26	DNU	–	–	Do not use
27	DNU	–	–	Do not use
28	VSS	Power		Connect to ground
29	XRES	I	–	External active LOW reset
30	P0[0]	I/O	–	I2C SCL / SPI SCLK
31	P0[1]	I/O	–	I2C SDA / SPI MOSI
32	P1[0]	I/O	–	COMM_INT / SPI MISO / WAKE
33	P1[1]	I/O	–	COMM_INT / SPI SS
34	P1[2]	I/O	–	EXT_SYNC (External sync signal output)
35	P1[3]	I/O	–	EXT_START (External start signal LCD display V-/H- sync)
36	P1[4]	I/O	–	ERROR - Set HIGH when internal error is detected

Note
13.See “**Pin information**” on page 11 for details on pin configuration.

Table 6 100-pin TQFP, 61 sense I/O CYAT8168X[13] (continued)

Pin No.	Name	Digital	Analog	Description
37	P1[5]	I/O	–	Reserved
38	P1[6]	I/O	–	COMM_INT
39	P2[0]	I/O	–	SWDIO
40	P2[1]	I/O	–	SWDCLK
41	VCCD	Power		Digital core power supply input/output
42	VDDD	Power		Digital power supply input
43	VSS	Power		Connect to ground
44	VSS	Power		Connect to ground
45	VDDA	Power		TX analog power supply input
46	VDDA_Q	Power		RX analog power supply input
47	VCCTX	Power		TX pump reservoir and filter capacitor connection point
48	DNU	–	–	Do not use
49	DNU	–	–	Do not use
50	DNU	–	–	Do not use
51	DNU	–	–	Do not use
52	DNU	–	–	Do not use
53	XY60	–	I/O	TX or RX channel 37
54	XY59	–	I/O	TX or RX channel 36
55	XY58	–	I/O	TX or RX channel 35
56	XY57	–	I/O	TX or RX channel 34
57	XY56	–	I/O	TX or RX channel 33
58	VSS	Power		Connect to ground
59	XY55	–	I/O	TX or RX channel 32
60	XY54	–	I/O	TX or RX channel 31
61	XY53	–	I/O	TX or RX channel 30
62	XY52	–	I/O	TX or RX channel 29
63	XY51	–	I/O	TX or RX channel 28
64	XY50	–	I/O	TX or RX channel 27
65	XY49	–	I/O	TX or RX channel 53
66	XY48	–	I/O	TX or RX channel 52
67	XY47	–	I/O	TX or RX channel 51
68	XY46	–	I/O	TX or RX channel 50
69	XY45	–	I/O	TX or RX channel 49
70	XY44	–	I/O	TX or RX channel 48
71	XY43	–	I/O	TX or RX channel 47
72	XY42	–	I/O	TX or RX channel 46
73	XY41	–	I/O	TX or RX channel 45

Note
13.See “**Pin information**” on page 11 for details on pin configuration.

Table 6 100-pin TQFP, 61 sense I/O CYAT8168X[13] (continued)

Pin No.	Name	Digital	Analog	Description
74	XY40	–	I/O	TX or RX channel 44
75	XY39	–	I/O	TX or RX channel 43
76	XY38	–	I/O	TX or RX channel 42
77	XY37	–	I/O	TX or RX channel 41
78	XY36	–	I/O	TX or RX channel 40
79	XY35	–	I/O	TX or RX channel 39
80	XY34	–	I/O	TX or RX channel 38
81	XY33	–	I/O	TX or RX channel 37
82	XY32	–	I/O	TX or RX channel 36
83	XY31	–	I/O	TX or RX channel 35
84	XY30	–	I/O	TX or RX channel 34
85	VDDA_Q	Power		RX analog power supply input
86	VSS	Power		Connect to ground
87	XY29	–	I/O	TX or RX channel 23
88	XY28	–	I/O	TX or RX channel 22
89	XY27	–	I/O	TX or RX channel 21
90	XY26	–	I/O	TX or RX channel 20
91	XY25	–	I/O	TX or RX channel 19
92	XY24	–	I/O	TX or RX channel 18
93	XY23	–	I/O	TX or RX channel 17
94	XY22	–	I/O	TX or RX channel 16
95	XY21	–	I/O	TX or RX channel 15
96	XY20	–	I/O	TX or RX channel 14
97	XY19	–	I/O	TX or RX channel 13
98	XY18	–	I/O	TX or RX channel 12
99	XY17	–	I/O	TX or RX channel 11
100	XY16	–	I/O	TX or RX channel 10

Note
13.See “**Pin information**” on page 11 for details on pin configuration.

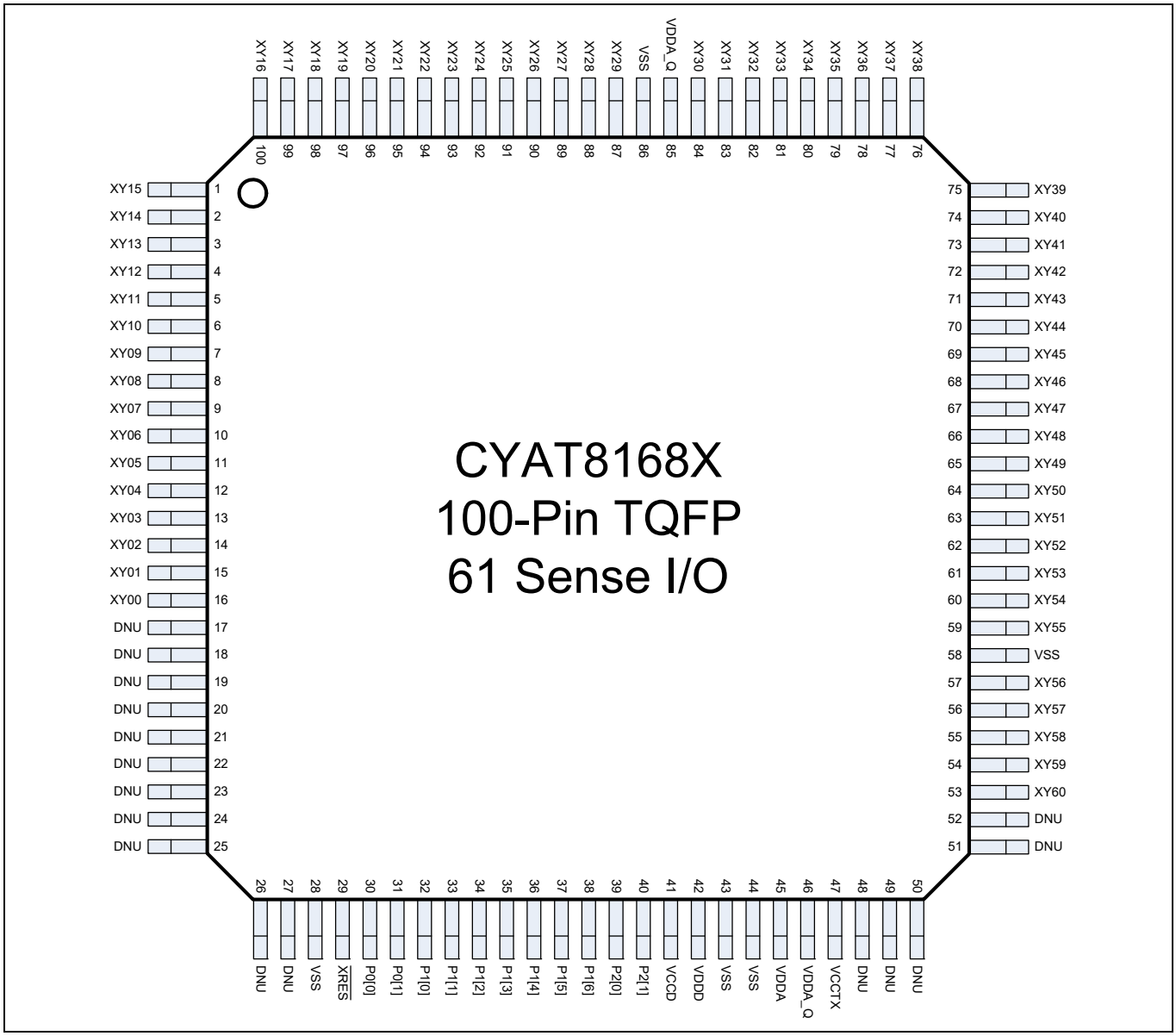


Figure 15 100-pin TQFP, 61 sense I/O CYAT8168X

9 Electrical specifications

This section lists CYAT8168X DC and AC electrical specifications.

9.1 Absolute maximum ratings

Table 7 Absolute maximum ratings

Symbol	Description	Conditions	Min	Typ	Max	Unit
T_{STG}	Storage temperature	–	–55	25	125	°C
V_{DDD}	Digital supply voltage	–	V_{SS} – 0.5	–	6	V
V_{DDA}	Analog supply voltage	–	V_{SS} – 0.5	–	6	V
V_{DDDR}	Amplitude (V_{PP}) of digital (V_{DDD}) supply ripple riding on the DC voltage	DC to 20 MHz	–	–	100	mV
V_{DDAR}[14]	Amplitude (V_{PP}) of analog (V_{DDA}) supply ripple riding on the DC voltage (TX pump enabled)	DC to 20 MHz	–	–	100	mV
	Amplitude (V_{PP}) of analog (V_{DDA}) supply ripple riding on the DC voltage (TX pump disabled)	DC to 150 kHz[15]	–	–	15	
		150 kHz[15] to 20 MHz	–	–	15 + 20 dB/decade > 150 kHz[15]	
V_{CCD}	Core supply voltage	–	V_{SS} – 0.5	–	2.3	V
V_{GPIO}	Port 0 pin voltage	Driver enabled	V_{SS} – 0.5	–	6	V
	Port 0 pin voltage	Driver disabled	V_{SS} – 0.5	–	7	
	Port 1 / Port 2 pin voltage	–	V_{SS} – 0.5	–	V_{DDD} + 0.5	
I_{IO}	Current into I/O pin	–	–25	–	50	mA
ESD_{CDM}	Electrostatic discharge voltage, charge device model	–	750	–	–	V
ESD_{HBM}	Electrostatic discharge voltage, human body model	100-pin TQFP	6000	–	–	V
		128-pin TQFP	4000	–	–	

9.2 Operating temperature

Table 8 Operating temperature

Symbol	Description	Conditions	Min	Typ	Max	Unit
T_A	Ambient temperature (A-grade)	–	–40	–	85	°C
T_A	Ambient temperature (S-grade)	–	–40	–	105	

Notes
14. Analog supply ripple specifications are valid for the supply presented to the external resistor (for example label “V” in **Figure 6**), not at the device VDDA and VDDA_Q pin.
15. If a 2.2-µF capacitor is used in place of a 1-µF capacitor, the threshold is 80 kHz.

9.3 DC specifications

The specifications in this section are valid under these conditions:
–40°C ≤ T_A ≤ 85°C for Grade-A devices, –40°C ≤ T_A ≤ 105°C for Grade-S devices.

9.3.1 Flash specifications

The specifications in **Table 9** are valid under these conditions: 1.71 V ≤ V_{DDD} ≤ 1.95 V or 3.0 V ≤ V_{DDD} ≤ 5.5 V, 1.71 V ≤ V_{CCD} ≤ 1.95 V, and 3.0 V ≤ V_{DDA} ≤ 5.5 V. Typical values are specified at T_A = 25°C, V_{DDD} = V_{CCD} = 1.8 V, core LDO disabled, and V_{DDA} = 3.0 V.

Table 9 Flash specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
$Flash_{ENPB}$	Flash write endurance	Erase/write cycles per block	10,000	–	–	cycles
$Flash_{DR}$	Flash data retention	Following maximum flash write cycles ($Flash_{ENPB}$), T_A ≤ 55°C	20[16]	–	–	years
		Following maximum flash write cycles ($Flash_{ENPB}$), T_A > 55°C	10[16]	–	–	

Note
16. Storing programmed devices at or above the ambient temperature specified by $Flash_{DR}$ may reduce flash data retention time. Infineon provides a retention calculator to calculate the retention lifetime based on customer's individual temperature profiles for operation over the ambient temperature range for the device's temperature rating. For more information, contact our support team at **support@infineon.com**.

9.3.2 Chip-level DC specifications

The specifications in **Table 10** are valid under these conditions: 1.71 V ≤ V_{DDD} ≤ 1.95 V or 3.0 V ≤ V_{DDD} ≤ 5.5 V, 1.71V ≤ V_{CCD} ≤ 1.95 V, and 3.0 V ≤ V_{DDA} ≤ 5.5 V. Typical values are specified at T_A = 25°C, V_{DDD} = V_{CCD} = 1.8 V, core LDO disabled, and V_{DDA} = 3.0 V.

Table 10 Chip-level DC specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{DDD}	Digital supply voltage	Core LDO enabled (V_{CCD} output)	3.0	–	5.5	V
		Core LDO disabled (V_{CCD} input)[17]	1.71	1.8	1.95	
V_{CCD}	Digital core supply voltage	Core LDO enabled (V_{CCD} output)	–	1.8	–	
		Core LDO disabled (V_{CCD} input)[17]	1.71	1.8	1.95	
V_{DDA}[17]	Analog supply voltage	TX pump enabled	3.0	–	4.7	
		TX pump disabled	3.0	–	5.5	
V_{CCTX}	V_{CCTX} supply operating voltage range	Input to external low-pass filter, external V_{CCTX} configuration	3.0	–	5.5	
PSA_{RAMP}	V_{DDA} ramp rate from ground to minimum voltage	–	–	–	100	V/ms
PSD_{RAMP}	V_{DDD} ramp rate from ground to minimum voltage	–	1[18]	–	40	
$PSD_{RAMPDOWN}$	V_{DDD} ramp down rate from 1.5 V to 1.0 V	–	1[18]	–	40	
I_{DDD_ACT}	V_{DDD} active current	–	–	20	50	mA
I_{DDA_ACT}	V_{DDA} active current	–	–	15	20	
I_{DDD_DS}	V_{DDD} deepsleep current	–	–	3	–	µA
I_{DDA_DS}	V_{DDA} deepsleep current	–	–	2	–	
I_{DDD_XR}	V_{DDD} current, $\overline{XRES}$ = LOW	1.71 V ≤ V_{DDD} ≤ 1.95 V	–	5	–	
		3.0 V ≤ V_{DDD} ≤ 5.5 V	–	1	–	
I_{DDA_XR}	V_{DDA} current, $\overline{XRES}$ = LOW	–	–	25	–	
I_{DDD_P}	V_{DDD} flash programming and flash verify current	–	–	5	25	mA

Notes

17. These min and max limits are inclusive of noise. For proper operation, V_{DDA} or V_{DDD} with combined noise cannot go below or above the specified min or max limits.
18. If minimum ramp rate cannot be met, XRES should be asserted during voltage ramp (1.5 V > VDDD > 1.0 V for ramp-down or until voltage is stable for ramp-up). Note that a glitch on the I^2C bus could occur during voltage ramp in this case.

9.3.3 I/O port 0 (P0[0:1]) DC specifications

The port 0 specifications in **Table 11** are valid under these conditions: 1.71 V ≤ V_{DDD} ≤ 1.95 V or 3.0 V ≤ V_{DDD} ≤ 5.5 V, 1.71 V ≤ V_{CCD} ≤ 1.95 V, and 3.0 V ≤ V_{DDA} ≤ 5.5 V. Typical values are specified at T_A = 25°C, V_{DDD} = V_{CCD} = 1.8 V, core LDO disabled, and V_{DDA} = 3.0 V.

Table 11 I/O port 0 (P0[0:1]) DC specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Input high voltage	CMOS mode	0.7 × V_{DDD}	–	–	V
		1.8-V mode, V_{EXT}[19] = 1.8 V, 3.0 V ≤ V_{DDD} ≤ 5.5 V	0.7 × V_{EXT}	–	–	
V_{IL}	Input low voltage	CMOS mode	–	–	0.3 × V_{DDD}	
		1.8-V mode, V_{EXT}[19] = 1.8 V, 3.0 V ≤ V_{DDD} ≤ 5.5 V	–	–	0.3 × V_{EXT}	
V_{OH}	High output voltage	Reference to V_{DDD}, I_{OH} = 1 mA, V_{DDD} = 1.8 V	V_{DDD} – 0.5	–	–	
		Reference to V_{DDD}, I_{OH} = 4 mA, V_{DDD} = 3.0 V	V_{DDD} – 0.6	–	–	
V_{OL}	Low output voltage	V_{DDD} ≥ 1.71 V, I_{OL} = 10 mA	–	–	0.6	
		V_{DDD} ≥ 1.71 V, I_{OL} = 3 mA	–	–	0.4	
V_H	Input hysteresis	–	0.1 × V_{DDD}	–	–	
T_{RISE_OV}	Output rise time Fast-Strong	25 pF load, 10%–90% V_{DDD} = 3.3 V	2	–	12	ns
	Output rise time Slow-Strong	25 pF load, 10%–90% V_{DDD} = 3.3 V	10	–	60	
T_{FALL_OV}	Output fall time Fast-Strong	25 pF load, 10%–90% V_{DDD} = 3.3 V	1.5	–	12	
	Output fall time Slow-Strong	25 pF load, 10%–90% V_{DDD} = 3.3 V	10	–	60	
I_{IL}[20]	Input leakage current (absolute value)	T_A = 25°C, V_{DDD} = 3.0 V	–	–	14	nA
		T_A = 25°C, V_{DDD} = 0.0 V	–	–	10	µA
C_{IN}	Input pin capacitance	Package and pin dependent T_A = 25°C	–	–	7	pF
C_{OUT}	Output pin capacitance	Package and pin dependent T_A = 25°C	–	–	7	
R_{INT}	Internal pull-up / pull-down resistance	Pin configured for internal pull-up or pull-down; note that all I/Os are Hi-Z during chip initialization (after XRES or Bootloader Exit)	3.5	5.6	8.5	kΩ

Notes
19. V_{EXT} is the external supply used to bias the pull-up resistor when used on an I^2C bus.
20. Gang tested with all I/Os to 1 µA.

9.3.4 I/O port 1 (P1[0:6]), port 2 (P2[0:1]), and $\overline{\text{XRES}}$ DC specifications

The specifications in **Table 12** are valid under these conditions: 1.71 V ≤ V_{DDD} ≤ 1.95 V or 3.0 V ≤ V_{DDD} ≤ 5.5 V, 1.71 V ≤ V_{CCD} ≤ 1.95 V, and 3.0 V ≤ V_{DDA} ≤ 5.5 V. Typical values are specified at T_A = 25°C, V_{DDD} = V_{CCD} = 1.8 V, core LDO disabled, and V_{DDA} = 3.0 V.

Table 12 I/O port 1 (P1[0:6]), Port 2 (P2[0:1]), and $\overline{\text{XRES}}$ DC specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	Input voltage high threshold	1.8-V configuration	1.26	–	–	V
		CMOS configuration	0.7 × V_{DDD}	–	–	
		XRES	1.35	–	–	
V_{IL}	Input voltage low threshold	1.8-V configuration	–	–	0.54	
		CMOS configuration	–	–	0.3 × V_{DDD}	
		XRES	–	–	0.45	
V_{OH}	High output voltage	I_{OH} = 4 mA, V_{DDD} = 3.0 V	V_{DDD} – 0.6	–	–	
		I_{OH} = 1 mA, V_{DDD} = 1.8 V	V_{DDD} – 0.5	–	–	
V_{OL}	Low output Voltage	I_{OL} = 8 mA, V_{DDD} = 3.3 V	–	–	0.6	
		I_{OL} = 4 mA, V_{DDD} = 1.8 V	–	–	0.6	
V_H	Input hysteresis voltage	–	0.1 × V_{DDD}	–	–	
T_{RISE_G}	Output rise time fast-strong	25 pF load, 10%–90% V_{DDD} = 3.3 V	2	–	12	ns
	Output rise time slow-strong	25 pF load, 10%–90% V_{DDD} = 3.3 V	–	–	60	
T_{FALL_G}	Output fall time fast-strong	25 pF load, 10%–90% V_{DDD} = 3.3 V	2	–	12	
	Output fall time slow-strong	25 pF load, 10%–90% V_{DDD} = 3.3 V	–	–	60	
I_{IL}[21]	Input leakage (absolute value)	–	–	–	2	nA
C_{IN}	Input pin capacitance	Package and pin dependent T_A = 25°C	–	–	7	pF
C_{OUT}	Output pin capacitance	Package and pin dependent T_A = 25°C	–	–	7	
R_{INT}[22]	Internal pull-up/pull-down resistance	Pin configured for internal pull-up or pull-down	3.5	5.6	8.5	kΩ

Notes
21. Gang tested with all I/Os to 1 µA.
22. XRES is input only with no internal pull-up or pull-down resistor.

9.4 AC specifications

The specifications in this section are valid under these conditions:
$-40°C \le T_A \le 85°C$ for Grade-A devices, $-40°C \le T_A \le 105°C$ for Grade-S devices.

9.4.1 SWD interface AC specifications

The specifications in **Table 13** are valid under these conditions: $1.71\ V \le V_{DDD} \le 1.95\ V$ or $3.0\ V \le V_{DDD} \le 5.5\ V$, $1.71\ V \le V_{CCD} \le 1.95\ V$, $3.0\ V \le V_{DDA} \le 5.5\ V$, and $C_{LOAD} = 25\ pF$. Typical values are specified at $T_A = 25°C$, $V_{DDD} = V_{CCD} = 1.8\ V$, core LDO disabled, and $V_{DDA} = 3.0\ V$.

Table 13 SWD interface AC specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
f_{SWDCLK}	SWDCLK frequency	$3.3\ V \le V_{DDD} \le 5\ V$	–	–	14	MHz
		$1.71\ V \le V_{DDD} < 3.3\ V$	–	–	8	
T_{SWDI_SETUP}	SWDIO input setup before SWDCLK HIGH	$T = 1 / f_{SWDCLK}$	T / 4	–	–	ns
T_{SWDI_HOLD}	SWDCIO input hold after SWDCLK HIGH	$T = 1 / f_{SWDCLK}$	T / 4	–	–	
T_{SWDO_VALID}	SWDCLK HIGH to SWDIO output valid	$T = 1 / f_{SWDCLK}$	–	–	T / 2	
T_{SWDO_HOLD}	SWDIO output hold after SWDCLK HIGH	$T = 1 / f_{SWDCLK}$	1	–	–	

9.4.2 Chip-level AC specifications

The specifications in **Table 14** are valid under these conditions: 1.71 V ≤ V_{DDD} ≤ 1.95 V or 3.0 V ≤ V_{DDD} ≤ 5.5 V, 1.71 V ≤ V_{CCD} ≤ 1.95 V, and 3.0 V ≤ V_{DDA} ≤ 5.5 V. Typical values are specified at T_A = 25°C, V_{DDD} = V_{CCD} = 1.8 V, core LDO disabled, and V_{DDA} = 3.0 V.

Table 14 Chip-level AC specifications

Symbol	Description	Conditions	Min	Typ	Max	Unit
T_{XRST}	External reset ($\overline{XRES}$) pulse width	After V_{DDD} is valid	10	–	–	µs
T_{READY}	Time from deassertion of $\overline{XRES}$ to COMM_INT	–	–	–	35	ms
T_{CAL}	Calibration routine execution time	–	–	2500	–	
$F_{IMOTOL1}$	Frequency variation at 37 MHz and 48 MHz	–	–	–	±2	%
$T_{COMM\_EXIT\_CRC}$	Time from EXIT BTLDR command (with CRC checking) to SYS INFO MODE	POST_SHORT_OPEN_CTRL - “Disabled All”[23].	–	40	–	ms

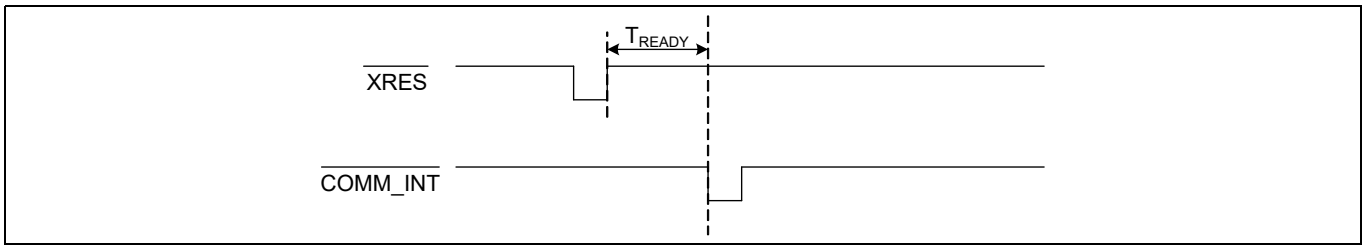


Figure 16 COMM_INT timing diagram

Note
23.For POST_SHORT_OPEN_CTRL - “Enabled All”, there will be an additional 600 ms (Typ) during startup.

9.4.3 I²C specifications

The specifications in **Table 15** are valid under these conditions: 1.71 V ≤ V_{DDD} ≤ 1.95 V or 3.0 V ≤ V_{DDD} ≤ 5.5 V, 1.71 V ≤ V_{CCD} ≤ 1.95 V, and 3.0 V ≤ V_{DDA} ≤ 5.5 V. Typical values are specified at T_A = 25°C, V_{DDD} = V_{CCD} = 1.8V, core LDO disabled, and V_{DDA} = 3.0 V. CYAT8168X does not require a clock-stretch capable host, but is fully compatible with systems that perform clock-stretching.

Important Note: The P0[0] and P0[1] pins have I/O cells optimized for use on multi-drop buses. When the touch device is powered OFF, the pin drivers do not load the attached bus, such that other devices attached to them may continue to communicate.

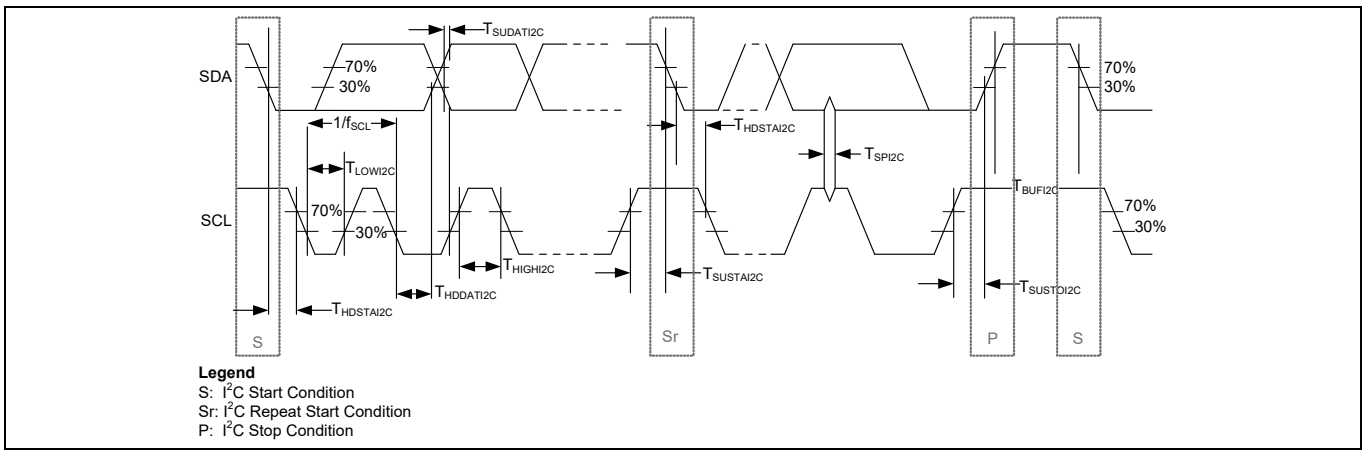


Figure 17 I²C Bus timing diagram for fast/standard mode

Table 15 AC characteristics of the I²C SDA and SCL pins

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
f_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz
$T_{HDSTAI2C}$	Hold time (repeated) start condition. After this period, the first clock pulse is generated.	4	–	0.6	–	µs
T_{LOWI2C}	LOW period of SCL clock	4.7	–	1.3	–	
$T_{HIGHI2C}$	HIGH period of SCL clock	4	–	0.6	–	
$T_{SUSTAI2C}$	Setup time for repeated start condition	4.7	–	0.6	–	
$T_{HDDATI2C}$	Data hold time	0	–	0	–	
$T_{SUDATI2C}$	Data setup time	250	–	100	–	ns
$T_{VDDATI2C}$	Data valid time	–	3.45	–	0.9	µs
$T_{VDACKI2C}$	Data acknowledge time	–	3.45	–	0.9	
$T_{SUSTOI2C}$	Setup time for stop condition	4	–	0.6	–	
V_{HH}	Input hysteresis high voltage, $1.71\ V \le V_{DDD} \le 1.95\ V$ or $3.0\ V \le V_{DDD} \le 5.5\ V$	$0.1 \times V_{DDD}$	–	$0.1 \times V_{DDD}$	–	V
T_{BUFI2C}	Bus free time between a stop and start condition	4.7	–	1.3	–	µs
T_{SPI2C}	Pulse width of spikes that are suppressed by input filter	–	–	50	–	ns
C_{BUS}	Capacitance load for SDA or SCL	–	400	–	400	pF
V_{IL_I2C}	Input low voltage	–0.5	$0.3 \times V_{DDD}$	–0.5	$0.3 \times V_{DDD}$	V
V_{IH_I2C}	Input high voltage	$0.7 \times V_{DDD}$	–	$0.7 \times V_{DDD}$	–	
$V_{OL\_I2C\_L}$	Output low voltage ($V_{DDD} \le 2$ V, 3 mA sink)	–	$0.2 \times V_{DDD}$	–	$0.2 \times V_{DDD}$	
$V_{OL\_I2C\_H}$	Output low voltage ($V_{DDD} > 3$ V, 3 mA sink)	–	0.4	–	0.4	
I_{OL_I2C}	Output low current	–	3	–	3	mA
	Output low current $V_{OL} = 0.6$ V	–	–	–	6	
V_{H_I2C}	Input hysteresis	$0.1 \times V_{DDD}$	–	$0.1 \times V_{DDD}$	–	mV

9.4.4 SPI specifications

The specifications listed in **Table 16** are valid under these conditions: 1.71 V ≤ V_{DDD} ≤ 1.95 V or 3.0 V ≤ V_{DDD} ≤ 5.5 V, 1.71V ≤ V_{CCD} ≤ 1.95 V, 3.0 V ≤ V_{DDA} ≤ 5.5 V, and C_{LOAD} = 25 pF. Typical values are specified at T_A = 25°C, V_{DDD} = V_{CCD} = 1.8 V, core LDO disabled, and V_{DDA} = 3.0 V.

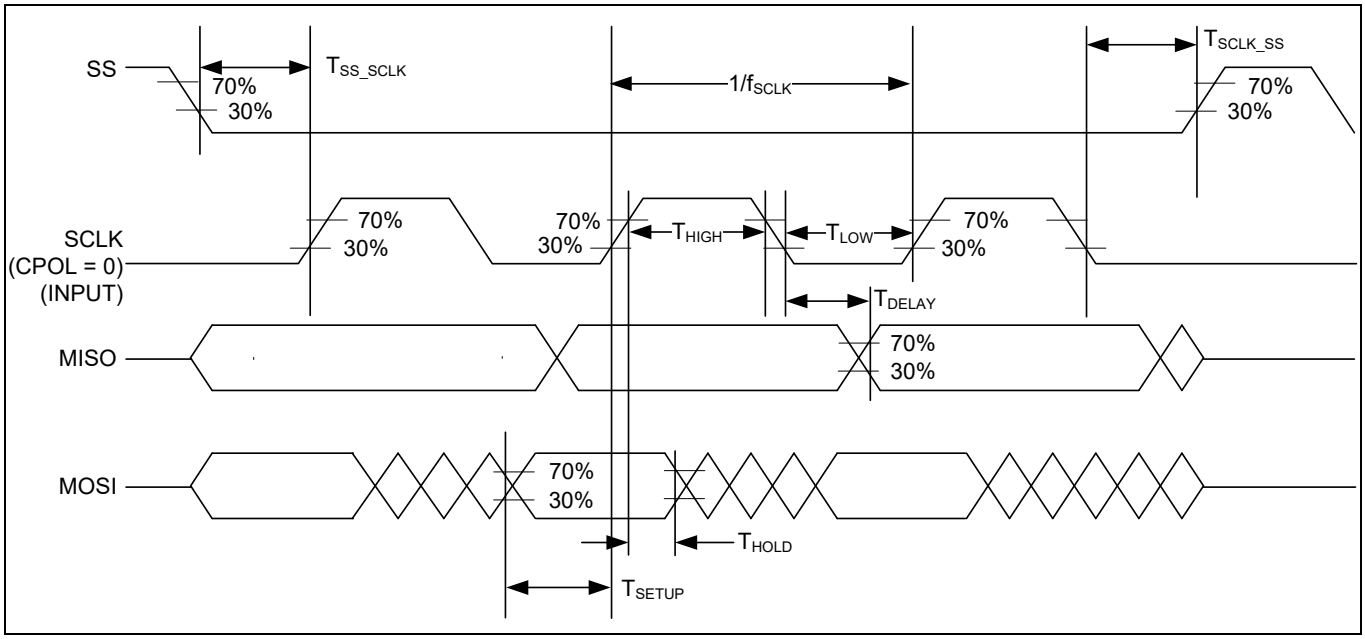


Figure 18 SPI timing diagram

Table 16 AC characteristics of SPI pins

Parameter	Description	Conditions	Min	Typ	Max	Unit
f_{SCLK}	SCLK clock frequency	–	–	–	8	MHz
$1/f_{SCLK}$	SPI SCLK cycle time (period)	–	125	–	–	ns
SDR_{SPI}	Sustained data rate for SPI transaction	–	–	–	8	Mbps
$T_{IDLESPI}$	Time between consecutive SPI transactions (duration between SS deactivation and the following SS activation)	–	125	–	–	ns
T_{LOW}	SCLK LOW time	–	50	–	–	ns
T_{HIGH}	SCLK HIGH time	–	50	–	–	
T_{SETUP}	MOSI setup to SCLK	–	30	–	–	
T_{HOLD}	MOSI hold from SCLK	–	30	–	–	
T_{DELAY}	MISO delay (hold) high voltage	$V_{DDD} \geq 3$ V	0	–	45	
	MISO delay (hold) low voltage	$V_{DDD} < 2$ V	0	–	65	
T_{SS_SCLK}	Time from SS LOW to first SCLK	–	125	–	–	
T_{SCLK_SS}	Time from last SCLK to SS HIGH	–	125	–	–	

9.5 System resources

9.5.1 Power-on reset (POR)

Table 17 Power-on reset (PRES)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID185[24]	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.5	V	–
SID186[24]	$V_{FALLIPOR}$	Falling trip voltage	0.70	–	1.4		–

9.5.2 Brown-out detect (BOD) for V_{CCD}

Table 18 Brown-out detect (BOD) for V_{CCD}

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/ conditions
SID190[24]	$V_{FALLPPOR}$	BOD trip voltage in active and sleep modes	1.48	–	1.62	V	–
SID192[24]	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep	1.11	–	1.5		–

Note
24.Guaranteed by characterization.

10 Packaging diagrams

This section provides the CYAT8168X device packaging specifications.

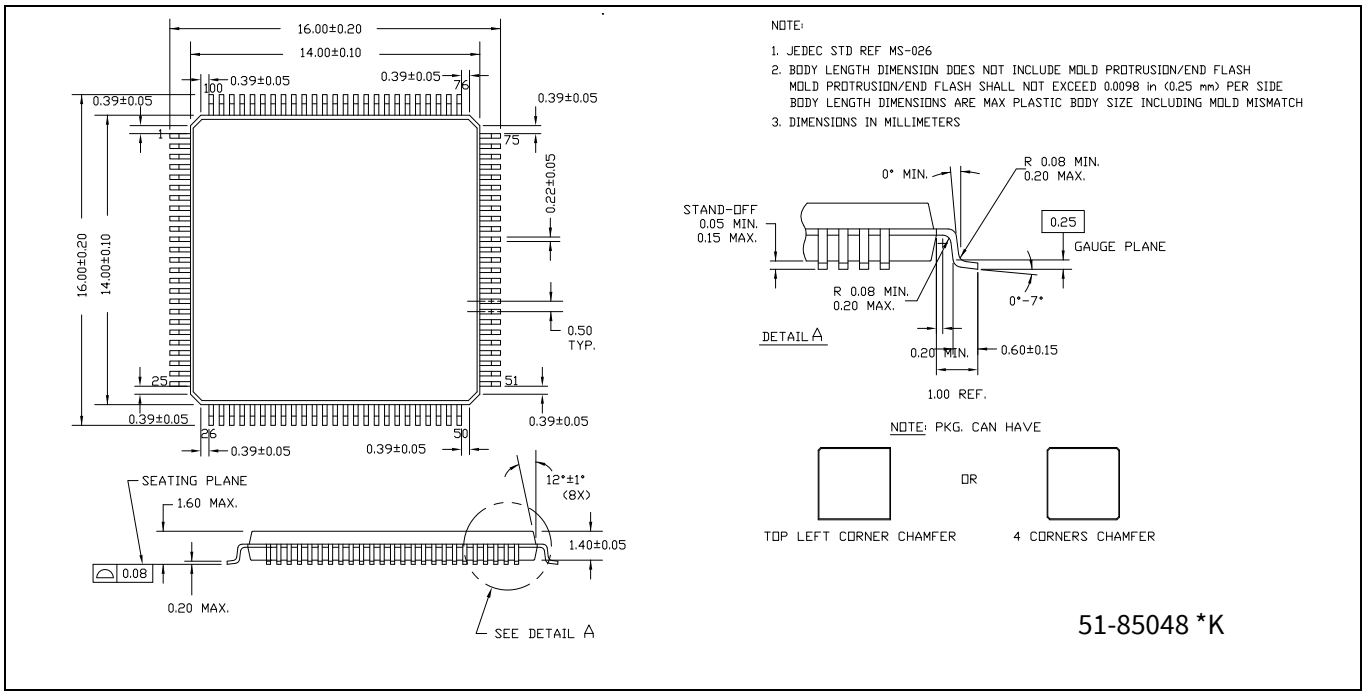


Figure 19 100-pin TQFP (14 × 14 × 1.4 mm) A100SA/AZ0AB package outline, 51-85048

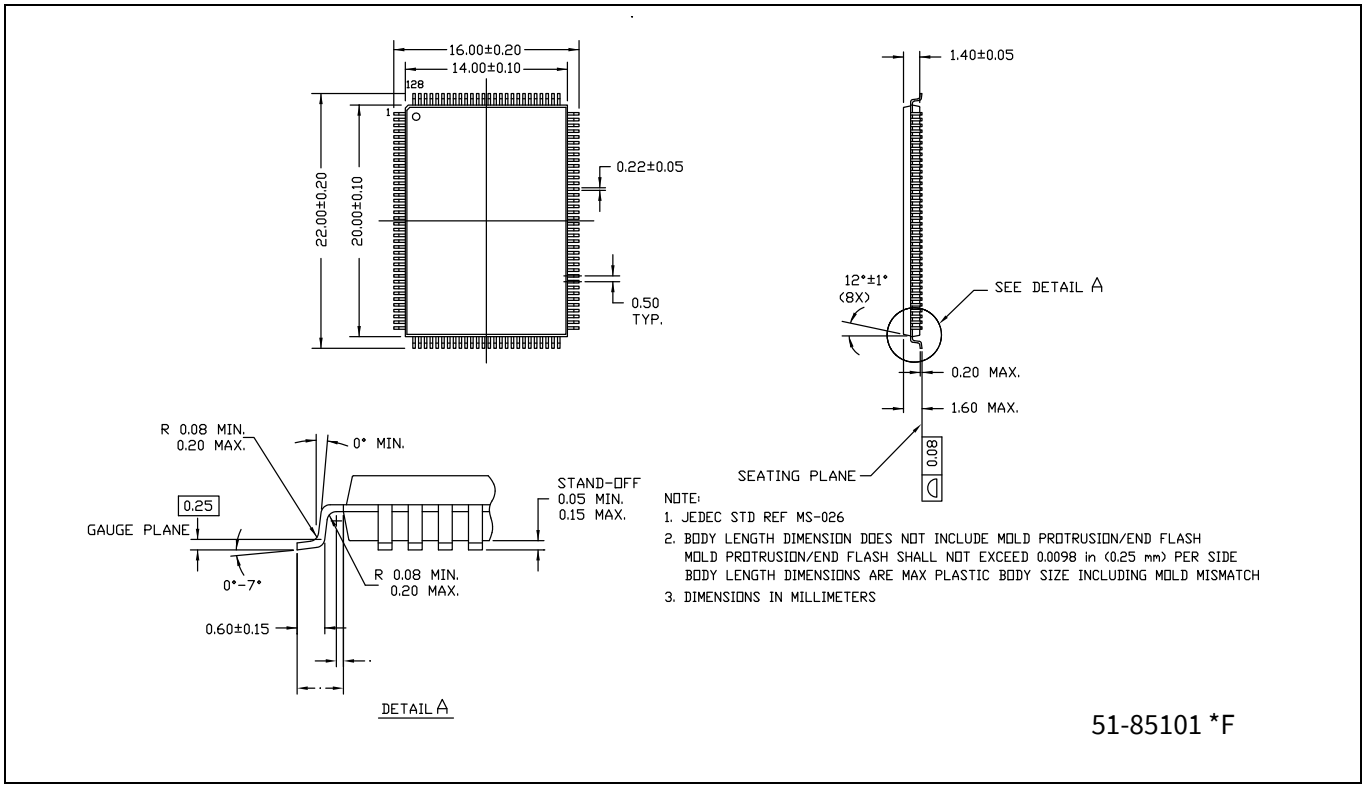


Figure 20 128-pin TQFP (14 × 20 × 1.4 mm) A128RA package outline, 51-85101

10.1 Thermal impedance and moisture sensitivity

Table 19 Thermal impedance and moisture sensitivity

Package	Typical θ_{JMAX}	Typical θ_{JA}	Typical θ_{JC}	Moisture sensitivity level
100-pin TQFP	150°C	46°C/W [25]	6°C/W [25]	3
128-pin TQFP	150°C	42°C/W [25]	5°C/W [25]	3

10.2 Solder reflow specifications

Table 20 lists the maximum solder reflow peak temperature.

Note

Thermal ramp rate during preheat should be 3°C/s or lower. The packaged device supports Pb-free solder reflow profile as per section 5.6 of J-STD-020.D1.

Table 20 Solder reflow specifications

Package	Maximum peak temperature	Time at maximum temperature
All packages	260°C	30 seconds

Note

25.Measured at 25°C ambient on a 4-layer PCB.

11 Ordering information

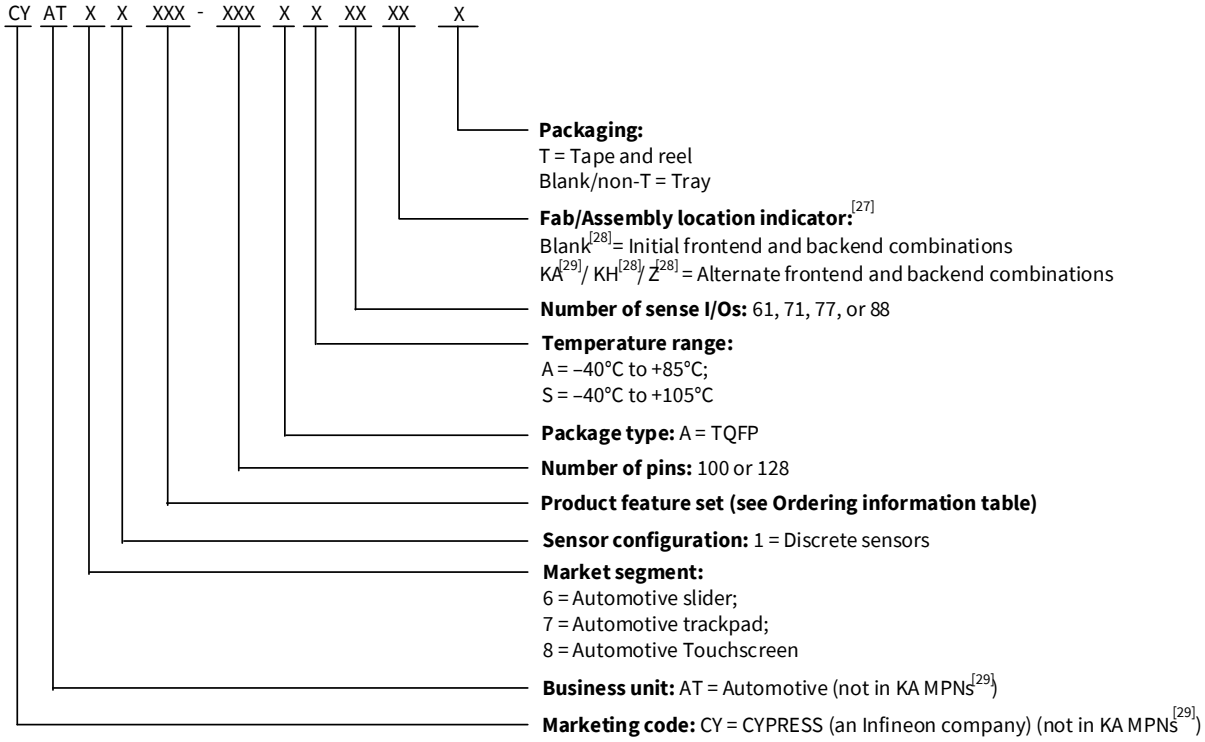
Table 21 lists the CYAT8168X touchscreen controllers.

Table 21 Ordering information[26]

MPN	Number of sense pins	Number of fingers	Wake-up button support	CapSense buttons	Water rejection	Thin glove support	Display Armor	Gesture	Thick overlay/ thick glove support	5-V TX	Package
CYAT81682-100AA61Z	61	10	–	✔	✔	✔	✔	–	–	–	100-pin TQFP
CYAT81682-100AS61Z	61	10	–	✔	✔	✔	✔	–	–	–	
CYAT81682-100AA71Z	71	10	–	✔	✔	✔	✔	–	–	–	
CYAT81682-100AS71Z	71	10	–	✔	✔	✔	✔	–	–	–	
CYAT81682-100AA77Z	77	10	–	✔	✔	✔	✔	–	–	–	
CYAT81682-100AS77Z	77	10	–	✔	✔	✔	✔	–	–	–	
CYAT81682-128AA88Z	88	10	–	✔	✔	✔	✔	–	–	–	128-pin TQFP
CYAT81682-128AS88Z	88	10	–	✔	✔	✔	✔	–	–	–	
CYAT81685-100AA61Z	61	10	–	✔	✔	✔	✔	✔	–	–	100-pin TQFP
CYAT81685-100AS61Z	61	10	–	✔	✔	✔	✔	✔	–	–	
CYAT81685-100AA71Z	71	10	–	✔	✔	✔	✔	✔	–	–	
CYAT81685-100AS71Z	71	10	–	✔	✔	✔	✔	✔	–	–	
CYAT81685-100AA77Z	77	10	–	✔	✔	✔	✔	✔	–	–	
CYAT81685-100AS77Z	77	10	–	✔	✔	✔	✔	✔	–	–	
CYAT81685-128AA88Z	88	10	–	✔	✔	✔	✔	✔	–	–	128-pin TQFP
CYAT81685-128AS88Z	88	10	–	✔	✔	✔	✔	✔	–	–	
CYAT81688-100AA61Z	61	10	–	✔	✔	✔	✔	✔	✔	✔	100-pin TQFP
CYAT81688-100AS61Z	61	10	–	✔	✔	✔	✔	✔	✔	✔	
CYAT81688-100AA71Z	71	10	–	✔	✔	✔	✔	✔	✔	✔	
CYAT81688-100AS71Z	71	10	–	✔	✔	✔	✔	✔	✔	✔	
CYAT81688-100AA77Z	77	10	–	✔	✔	✔	✔	✔	✔	✔	
CYAT81688-100AS77Z	77	10	–	✔	✔	✔	✔	✔	✔	✔	
CYAT81688-128AA88Z	88	10	–	✔	✔	✔	✔	✔	✔	✔	128-pin TQFP
CYAT81688-128AS88Z	88	10	–	✔	✔	✔	✔	✔	✔	✔	
CYAT81689-100AA61Z	61	10	✔	✔	✔	✔	✔	✔	✔	✔	100-pin TQFP
CYAT81689-100AS61Z	61	10	✔	✔	✔	✔	✔	✔	✔	✔	
CYAT81689-100AS71Z	71	10	✔	✔	✔	✔	✔	✔	✔	✔	
CYAT81689-100AA77Z	77	10	✔	✔	✔	✔	✔	✔	✔	✔	
CYAT81689-100AS77Z	77	10	✔	✔	✔	✔	✔	✔	✔	✔	
CYAT81689-128AA88Z	88	10	✔	✔	✔	✔	✔	✔	✔	✔	128-pin TQFP
CYAT81689-128AS88Z	88	10	✔	✔	✔	✔	✔	✔	✔	✔	

Note
26. All devices have the following base features: Water Rejection, DisplayArmor™, AutoArmor™, DualSense™, CAPSENSE™ buttons, and Large Object Detection and Rejection.

11.1 Ordering code definitions



Notes
27.All manufacturing locations (Blank / KA / KH / Z) have the same silicon ID.
28.Example Blank/KH/Z MPNs: CYAT81688-100AS61, CYAT81688-100AS61KH, and CYAT81688-100AS61Z.
29.Example KA MPN: 81688-100AS61KAT.

12 Acronyms

Table 22 Acronyms used in this document

Acronym	Description
CPU	central processing unit
DNU	do not use
DSD	dual-solid diamond pattern (**Figure 4**)
EMI	electromagnetic interference
ESD	electrostatic discharge
FPC	flexible printed circuit
I^2C	inter-integrated circuit
I/O	input/output
ITO	indium tin oxide
LCD	liquid crystal display
LDO	low dropout regulator
MH3	Manhattan-3 pattern (**Figure 5**)
MTK	manufacturing test kit
PCB	printed circuit board
PET	polyethylene terephthalate
PSoC™	programmable system-on-chip
SCL	serial I^2C clock
SD	signal disparity
SDA	serial I^2C data
SOL	sensor-on-lens
SNR	signal-to-noise ratio
SSD	single-solid diamond pattern (**Figure 3**)
SWD	serial wire debug
SWDCLK	serial wire debug clock
TRM	technical reference manual
TTHE	touch tuning host emulator
V_{PP}	volts peak-to-peak

13 Reference documents

Infineon has created a collection of documents to support the design of PSoC™ Automotive Multitouch touchscreen controllers.

The following list will guide you in identifying the proper document for your task:

- PCB/FPC schematic and layout design
- ITO panel design
- Driver development
- Manufacturing (MFG)
- System performance evaluation

Infineon's PSoC™ Automotive Multitouch technology is Infineon confidential information and is protected through a Non-Disclosure Agreement (NDA). These documents are not publicly available on the Infineon website. Contact your local Infineon office to request any of these documents pursuant to the aforementioned NDA. You can also direct your requests to **automotive@infineon.com**.

Table 23 Reference specifications

Document number	Document title	Description	PCB FPC	ITO Panel	Driver	MFG	System
Solution specifications							
001-49389	PSoC™ Automotive Multitouch Touchscreen Controller User Interface Performance Definitions	Contains Infineon touchscreen performance parameter definitions, justification for parameters, and parameter test methodologies.	–	✔	–	–	✔
001-50467	PSoC™ Automotive Multitouch Touchscreen Controller Module Design Best Practices	A system-level design guide for building a capacitive touchscreen module, covering topics such as touchscreen traces, shielding, mechanical design, FPC/PCB design, and LCD considerations.	✔	✔	–	–	–
001-83948	Touch Tuning Host Emulator User Guide	Describes the Touch Tuning Host Emulator Software	–	–	–	–	✔
001-63571	CY3295-MTK PSoC™ Multitouch Manufacturing Test Kit User Guide	Describes the CY3295-MTK Manufacturing Test Kit	–	–	–	✔	–
001-81891	The Touch Driver for Android (TTDA) User Guide	Contains information on the example Android touch driver	–	–	✔	–	–
External specifications: These specifications are not created or owned by Infineon, but directions on how to acquire or access them can be provided upon request by contacting **automotive@infineon.com**.							
UM10204	I^2C-bus specification and user manual		✔	–	–	–	✔
ISO11452	Component test methods for electrical disturbances in road vehicles package		✔	–	–	–	✔
CISPR25	Vehicles, boats and internal combustion engines – Radio disturbance characteristics – Limits and methods of measurement for the protection of on-board receivers		✔	–	–	–	✔
J-STD-020D.1	Moisture/reflow sensitivity	Classification for nonhermetic surface mount devices	✔	–	–	–	✔

14 Document conventions

14.1 Units of measure

Table 24 Units of measure

Symbol	Unit of measure
°C	degrees Celsius
µA	microampere
µF	microfarad
µs	microsecond
µW	microwatt
Ω	ohm
Hz	hertz
kΩ	kilo-ohm
kbps	kilobits per second
kHz	kilohertz
mA	milliampere
mm	millimeter
ms	millisecond
mV	millivolt
mW	milliwatt
Mbps	megabits per second
MHz	megahertz
nA	nanoampere
ns	nanosecond
pF	picofarad
s	second

14.2 Port nomenclature

Px[y] describes a particular bit “y” available within an I/O port “x.” For example, P4[2] reads “port 4, bit 2.”

Px[y:z] describes a particular range of bits “y to z” within an I/O port named “Px.” For example, P4[0:5] refers to bits 0 through 5 within an I/O port named P4.

15 Glossary

Table 25 Glossary

Term	Definition
accuracy	The maximum position error across the touchscreen, measured in millimeters, along a straight line between the actual finger position and the reported finger position. Accuracy is measured across the core and full panel. See Infineon's **PSoC™ Automotive Multitouch Touchscreen Controller Performance Parameters (001-49389)**[30] specification for more information.
All-Points	Infineon brand name for PSoC™ Automotive Multitouch devices capable of tracking the motion of multiple fingers.
AMOLED/OLED	Type of display using Active Matrix (AM) Organic Light Emitting Diodes (OLED).
conversion	The process of measuring the capacitance of an electrode connected to a pin (self capacitance) or the capacitance between a pair of electrodes connected to different pins (mutual capacitance). The result is a number that can be processed by the channel engine and CPU.
core	That portion of the touchscreen, responsive to touch, less a perimeter area whose width is the larger of 3.5 mm or half the width of the finger (for example, less a perimeter band 4.5-mm wide for a 9-mm finger).
core LDO	Low Drop Out Regulator that sources power to the digital core when enabled. Input to the LDO is VDDD. Output of the LDO is connected to the digital supply pin VCCD. When the core LDO is disabled, power must be externally applied to the digital core supply pin VCCD.
cover lens	The top layer in the touchscreen stackup that provides mechanical stability and protection for the touchscreen sensor.
DCVCOM	Type of Liquid Crystal Display where the common electrode (VCOM) is driven by DC voltage.
linearity	The deviation of the position data from a best-fit straight line across the touchscreen, measured in millimeters. Linearity is measured across the core and full panel. See Infineon's **PSoC™ Automotive Multitouch Touchscreen Controller Performance Parameters (001-49389)**[30] specification for more information.
mutual capacitance	The capacitance between two touchscreen electrodes.
refresh rate	The frequency at which consecutive frames of touchscreen data are made available in a data buffer while a finger is present on the touchscreen. See Infineon's **PSoC™ Automotive Multitouch Touchscreen Controller Performance Parameters (001-49389)**[30] specification for more information.
RX	Receive. A touchscreen electrode or touchscreen controller sense pin, mapped or switched to a charge sensing circuit within the controller (known as a receive channel).
scan	The conversion of all sensor capacitances to digital values.
sense pin	A pin that can be multiplexed to RX or TX.
signal-to-noise ratio (SNR)	The ratio between a capacitive finger signal and system noise.

Note
30. Infineon reference documents are available under NDA through your local Infineon sales representative. You can also direct your requests to **automotive@infineon.com**.

Table 25 Glossary (continued)

Term	Definition
signal disparity (SD)	The ratio of maximum measured signal when the touchscreen is grounded and maximum measured signal when the touchscreen is isolated from ground.
stackup	Layers of materials, in defined assembly order, that make up a touchscreen sensor.
TX	Transmit. A touchscreen electrode or touchscreen controller sense pin, mapped or switched to a charge forcing circuit within the controller. This charge forcing circuit drives a periodic waveform onto one or more touchscreen electrodes, which are coupled through mutual capacitance to adjacent receive electrodes.

Revision history

Document revision	Date	Description of changes
*E	2016-05-13	Changed status from Preliminary to Final.
*F	2016-08-18	Updated **Electrical specifications**: Updated **DC specifications**: Updated **Chip-level DC specifications**: Updated **Table 10**: Replaced “V/µs” with “V/ms” in “Units” column corresponding to PSA_{RAMP} parameter. Updated to new template.
*G	2016-10-25	Updated **Power supply information**: Updated **Required external components**: Updated **Figure 6**. Updated **Figure 7**. Updated **Figure 8**. Updated **Figure 9**. Updated **Figure 10**. Updated **Ordering information**: Updated part numbers (Prefixed all MPNs with “Z”). Updated to new template.
*H	2017-03-04	Updated **Power supply information**: Updated **Required external components**: Updated **Figure 6**. Updated **Figure 7**. Updated **Figure 8**. Updated **Figure 9**. Updated **Figure 10**. Updated to new template. Completing Sunset Review.
*I	2017-06-28	Updated **Touchscreen system overview**: Updated **Figure 1**. Updated **Electrical specifications**: Updated **Chip-level AC specifications**: Updated **Table 14**: Changed maximum value of T_{READY} parameter from 16 ms to 35 ms. Added $T_{COMM\_EXIT\_CRC}$ parameter and its corresponding details. Added Note 23 and referred the same note in “Conditions” column corresponding to $T_{COMM\_EXIT\_CRC}$ parameter.

Revision history

Document revision	Date	Description of changes
*I (cont.)	2017-06-28	Updated **Packaging diagrams**: Updated **Thermal impedance and moisture sensitivity**: Updated **Table 19**: Added "Typical θ_{JC}" column and added details. Updated **Ordering information**: No change in part numbers. Updated **Ordering code definitions**. Added Note 27 and referred the same note in "Fab location indicator". Updated **Reference documents**: Updated **Table 23**: Removed spec 001-81514 and its details (spec is obsolete).
*J	2017-08-04	Updated **Packaging diagrams**: No change in revisions of diagrams. Updated **Thermal impedance and moisture sensitivity**: Updated **Table 19**: Updated details in "Typical θ_{JA}" and "Typical θ_{JC}" columns. Updated **Ordering information**: Updated part numbers.
*K	2017-09-05	Updated **Ordering information**: No change in part numbers. Updated **Ordering code definitions**.
*L	2018-01-10	Updated **Electrical specifications**: Updated **Absolute maximum ratings**: Updated **Table 7**: Updated details in "Min" columns corresponding to ESD_{CDM} and ESD_{HBM} parameters. Updated **Flash specifications**: Updated **Table 9**: Updated details in "Conditions" column corresponding to $FLASH_{DR}$ parameter. Updated **Chip-level AC specifications**: Updated **Table 14**: Updated details in "Typ" column corresponding to T_{CAL} parameter. Updated **I2C specifications**: Updated **Table 15**: Updated details in "Min" and "Max" columns corresponding to $V_{OL\_I2C\_L}$ and $V_{OL\_I2C\_H}$ parameters. Added **System resources**. Updated **Ordering information**: Updated part numbers. Updated to new template.

Revision history

Document revision	Date	Description of changes
*M	2018-09-03	Updated **Electrical specifications**: Updated **Chip-level AC specifications**: Updated **Table 14**: Updated details in “Typ” and “Max” columns corresponding to $T_{COMM\_EXIT\_CRC}$ parameter. Updated Note 23. Updated **System resources**: Updated **Table 17**: Removed SR_POWER_UP parameter and its details. Updated **Packaging diagrams**: spec 51-85048 – Changed revision from *J to *K.
*N	2019-05-30	Updated **Ordering information**: Updated part numbers.
*O	2020-11-30	Updated **Electrical specifications**: Updated **Chip-level DC specifications**: Updated **Table 10**: Updated details in description column corresponding to PSD_{RAMP} parameter. Updated **Packaging diagrams**: No change in revisions of diagrams. Updated **Thermal impedance and moisture sensitivity**: Updated **Table 19**. Updated **Ordering information**: No change in part numbers. Removed references to Grip Suppression. Changed touchpad references to trackpad. Updated **Ordering code definitions**.
*P	2021-08-18	Updated **Pin information**: Updated description. Updated **Electrical specifications**: Updated **Absolute maximum ratings**: Updated **Table 7**. Updated **Chip-level DC specifications**: Updated **Table 10**. Updated **I/O port 0 (P0[0:1]) DC specifications**: Updated **Table 11**. Updated **Packaging diagrams**: No change in revisions of diagrams. Updated **Thermal impedance and moisture sensitivity**: Updated **Table 19**. Updated **Ordering information**: No change in part numbers. Updated **Ordering code definitions**.
*Q	2022-05-19	Updated to the PSoC™ Automotive Multitouch branding guidelines. Updated **Electrical specifications**: Updated **Absolute maximum ratings**: Updated **Table 7**. Updated **Ordering information**: Updated part numbers. Updated **Ordering code definitions**: Added notes 28 and 29 and referred the same notes in appropriate places in ordering code definitions.

Revision history

Document revision	Date	Description of changes
*R	2022-06-14	Updated **Ordering information**: No change in part numbers. Updated **Ordering code definitions**: Replaced KG with KH in all instances. Completing Sunset Review.
*S	2022-08-17	Updated Document Title to read as “CYAT8168X, PSoC™ Automotive Multitouch Generation 6XL Datasheet”. Migrated to Infineon template.
*T	2023-05-09	Updated **Touchscreen system specifications**: Updated **System performance specifications**: Updated description. Updated **Electrical specifications**: Updated **DC specifications**: Added description. Updated **Flash specifications**: Updated description. Updated **Table 9**. Updated Note 16. Updated **Chip-level DC specifications**: Updated description. Updated **I/O port 0 (P0[0:1]) DC specifications**: Updated description. Updated **Table 11**. Updated **I/O port 1 (P1[0:6]), port 2 (P2[0:1]), and XRES DC specifications**: Updated description. Updated **Table 12**. Updated **AC specifications**: Added description. Updated **SWD interface AC specifications**: Updated description. Updated **Chip-level AC specifications**: Updated description. Updated **I2C specifications**: Updated description. Updated **SPI specifications**: Updated description. Updated to new template.