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EZ-PD™ BCR Datasheet

USB Type-C Port Controller for Power Sinks

General Description

EZ-PD™ BCR is Cypress' highly-integrated pre-programmed USB Type-C port controller targeting electronic devices that have legacy barrel connectors (up to 100W) or USB micro-B connectors for power such as drones, smart speakers, power tools, and other rechargeable devices. EZ-PD BCR complies with the latest USB Type-C and USB Power Delivery (PD) standards and enables users to quickly convert their devices from being powered through a barrel connector to being powered via the USB-C connector with few external components and no firmware development is required. EZ-PD BCR integrates a complete USB Type-C transceiver, USB PD policy manager, a load switch controller with a soft start, all termination resistors required for a USB Type-C port, and system-level ESD protection. It is available in a 24-pin QFN package.

Features

USB Type-C and USB-PD Support

- Supports USB PD3.0 Revision 2.0 Version 1.3
- Configurable resistor R_D
- Supports one USB Type-C port

5V Legacy Charging

- Supports 5-V operation when connected to USB Type-A ports

System-Level Fault Protection

- VBUS to CC Short Protection
- On-chip overvoltage protection (OVP)

Clocks and Oscillators

- Integrated oscillator eliminating the need for external clock

Power

- 3.0-V to 24.5-V operation (30-V tolerant)

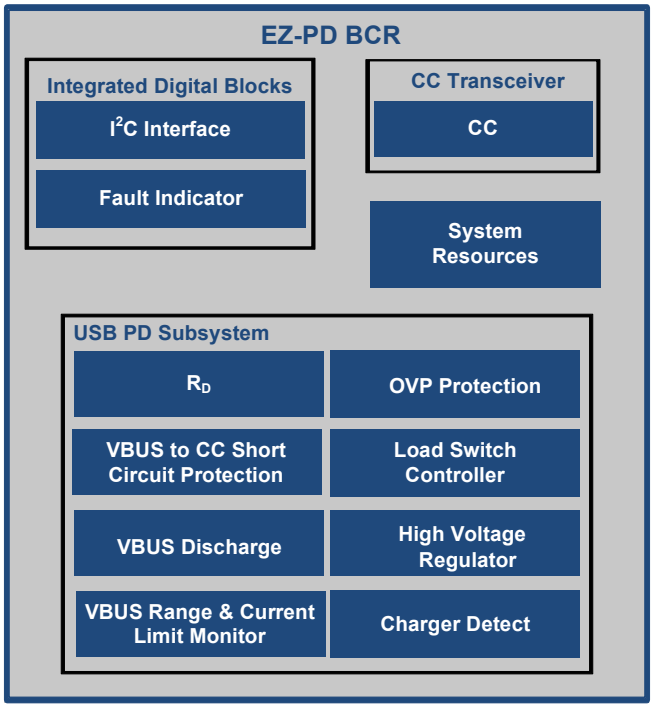
System-Level ESD Protection

- On CC, VBUS_IN, DC_OUT, D+, D-, HPI_SDA and HPI_SCL pins
- ± 8-kV contact discharge and ±15-kV air gap discharge based on IEC61000-4-2 level 4C

Packages

- 24-pin QFN package
- Supports extended industrial temperature range (–40°C to +105°C)

Logic Block Diagram



Contents

Functional Overview

USB-PD Subsystem

The USB-PD subsystem provides the interface to the USB Type-C USB port. This subsystem comprises a high-voltage regulator, OVP, and supply switch blocks. This subsystem also includes all ESD protection required and supported on the USB Type-C port.

USB-PD Physical Layer

The USB-PD Physical Layer consists of a transmitter and receiver that communicate BMC-encoded data over the CC channel based on the USB PD 3.0 standard. All communication is half-duplex. The Physical Layer or PHY practices collision avoidance to minimize communication errors on the channel.

The USB-PD block includes the termination resistor R_D and its switch as required by the USB-PD spec. R_D resistor is required to implement connection detection, plug orientation detection, and for establishing USB UFP role.

According to the USB Type-C spec, a USB Type-C controller such as the EZ-PD BCR device must present certain termination resistors depending on its role in its unpowered state. The Sink role requires R_D resistor to be present on the CC pins even in an unpowered state. To implement this function, EZ-PD BCR has a dead battery R_D resistor bonded to both the CC pins.

VBUS Overvoltage Protection

The EZ-PD BCR device has an integrated hardware block for VBUS OVP with configurable thresholds and response times on the USB Type-C port.

VBUS Short Protection

The EZ-PD BCR device provides VBUS short protection on CC1 an CC2 pins. These pins are protected from accidental shorts to high-voltage VBUS. Accidental shorts may occur because the CC1 and CC2 pins are placed next to the VBUS pins in the USB Type-C connector. A USB-PD controller without the high-voltage VBUS short protection will be damaged in the event of accidental shorts. When the protection circuit is triggered, the EZ-PD BCR device can handle up to 17 V forever and between 17 V to 22 VDC for 1000 hours on the CC1 and CC2 pins. When a VBUS short event occurs on the CC pins, a temporary high-ringing voltage is observed due to the RLC elements in the USB Type-C cable. Without the EZ-PD BCR device connected, this ringing voltage can be twice (44 V) the maximum VBUS voltage (21.5 V). However, when the EZ-PD BCR device is connected, it is capable of clamping temporary high-ringing voltage and protecting the CC pin using IEC ESD protection diodes.

Sink Load Switch Controller on VBUS Path

The EZ-PD BCR device has an integrated load switch controller to drive external PFETs on the VBUS sink path. This load switch controller has a soft start feature that limits the in-rush current flowing through the sink power path when the system is connected to an external load and powered on.

SAFE_PWR_EN Gate Driver

The EZ-PD BCR device has a SAFE_PWR_EN gate driver that can be used to drive an alternate load switch/FET. It is enabled whenever the EZ-PD BCR device is unable to negotiate the requested power contract. In such a scenario, the EZ-PD BCR device negotiates a 5-V/900-mA contract which can be delivered through the SAFE_PWR_EN FET to an alternate power rail in the system. This allows the system to operate in a limited mode when the requested power is unavailable through the USB Type-C port.

VBUS Discharge FETs

The EZ-PD BCR device also has an integrated VBUS discharge FET used to discharge VBUS to meet the USB-PD specification timing on a detach condition.

Integrated I^2C Blocks

The EZ-PD BCR device has an I^2C slave interface that can be connected to an I^2C host. The slave address is 0x08. Contact Cypress Technical Support for further details related with EZ-PD BCR HPI specification.

The I^2C interface is capable of operating at speeds of up to 1 Mbps (Fast-mode Plus). The I^2C interface is also compatible with the I^2C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I^2C-bus specification and user manual (UM10204). The I^2C bus I/Os are implemented with GPIO in open-drain modes.

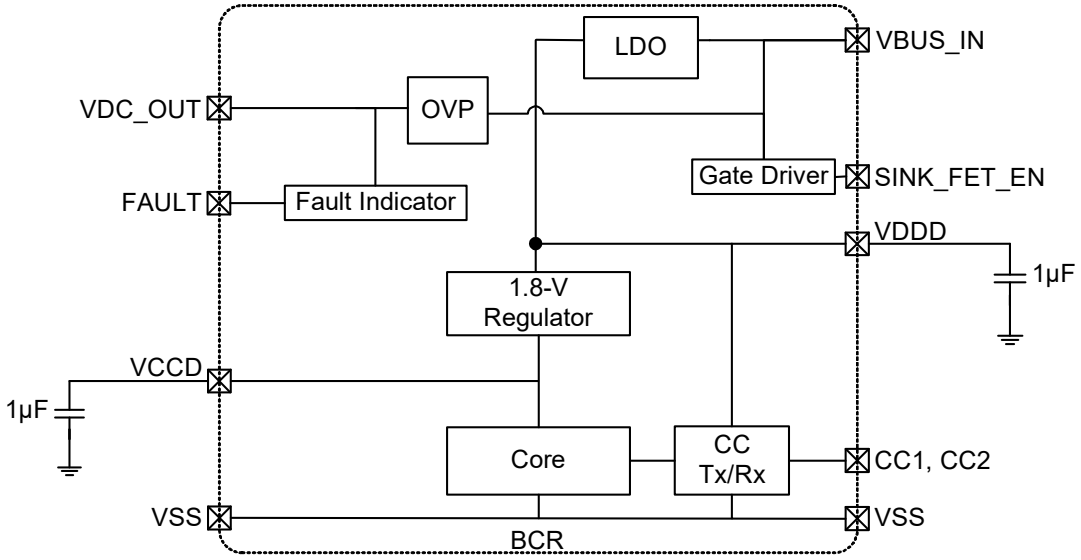
The I^2C interface is not completely compliant with the I^2C spec in the following aspects:

- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8-mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the bus load.

Power Systems Overview

The EZ-PD BCR device can operate from two possible external supply sources: VBUS_IN (3.0 V–24.5 V) or VDDD (2.7 V–5.5 V). When powered through VBUS_IN, the internal regulator generates VDDD of 3.3 V for chip operation. The regulated supply, VDDD, is either used directly inside some analog blocks or further regulated down to VCCD (1.8 V), which powers majority of the core using the regulators. Refer to the application diagram (see Figure 3) for capacitor connections.

Figure 1. Power System Requirement Block Diagram



Pinouts

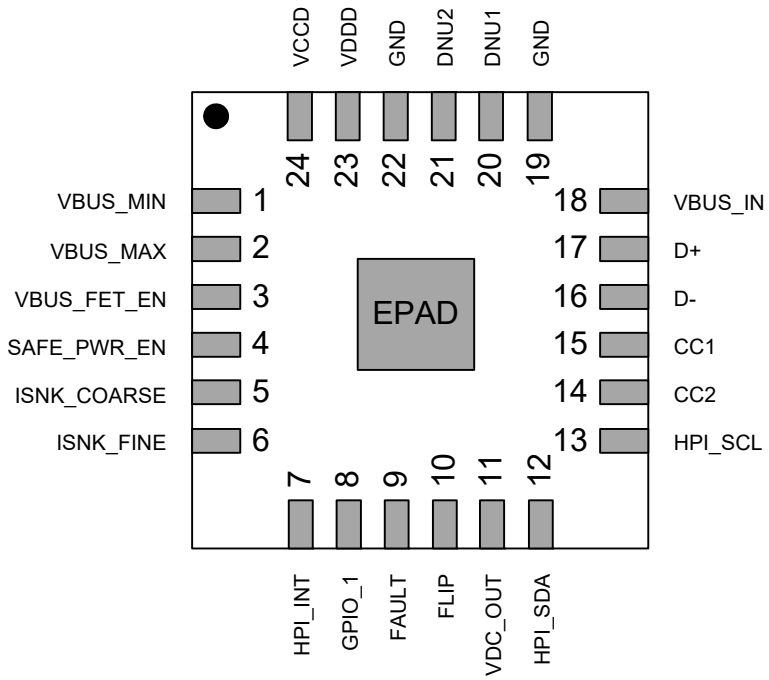
Table 1. EZ-PD BCR Pin Descriptions

24-Pin QFN	Pin Name	Description
1	VBUS_MIN	Connect a resistor divider on this to 3.3 V (from the VDDD pin) to indicate the minimum voltage needed by the system from the attached power adapter. Refer to Table 2 for recommended resistor values.
2	VBUS_MAX	Connect a resistor divider on this to 3.3 V (from the VDDD pin) to indicate the maximum voltage needed by the system from the attached power adapter. Refer to Table 2 for recommended resistor values.
3	VBUS_FET_EN	Connect this signal to the gate of a FET through a series resistor. This pin is the output of a PMOS FET gate driver that is slew-rate controlled. This signal is enabled when the EZ-PD BCR device successfully negotiates a power contract within the requested range.
4	SAFE_PWR_EN	Connect this signal to the gate of a FET through a series resistor. This pin is the output of a PMOS FET gate driver. This signal is enabled when the EZ-PD BCR device fails to negotiate for higher power and defaults to 5 V.
5	ISNK_COARSE	Connect a resistor divider on these pins to 3.3 V (from the VDDD pin) to set the operating current requested from the power adapter. Refer toTable 3 and Table 4 for recommended resistor values.
6	ISNK_FINE	
7	HPI_INT	Active LOW HPI Interrupt pin
8	GPIO_1	Additional GPIO that can be set up over the HPI interface.
9	FAULT	The EZ-PD BCR device pulls this line high if the power adapter cannot supply the required voltage or current or if an OVP event was detected. The pin is low otherwise.
10	FLIP	The EZ-PD BCR device pulls this line low if no device is attached or if CC polarity is un-flipped (CC1 connected). If a device is attached on CC2 (polarity is flipped), the EZ-PD BCR device pulls this line high. This is an open drain I/O that requires an external pull-up resistor. The presence or the value of the pull-up resistor connected to this pin determines the data capability reported in the UFP Vendor Data Object (VDO) by the BCR device to the Downstream Facing Port (DFP). If there is no pull-up resistor on this pin or if its value is less than or equal to 4.7 kΩ, then the UFP VDO data capability bit is set to 1, which correlates to the port being data capable. If the value of the pull-up resistor is 50 kΩ, then the UFP VDO data capability bit is set to 0, which correlates to the port not being data capable.
11	VDC_OUT	Connect this pin to the output of the PFETs controlled by the VBUS_FET_EN. This is used for monitoring the VBUS output. This is the power output of the system.
12	HPI_SDA	This is an I^2C slave interface provided for a host processor to control and monitor the EZ-PD BCR device. For more details, refer to the HPI Specification for EZ-PD BCR device.
13	HPI_SCL	
14	CC2	Communication Channel 2 pin used to negotiate a voltage/current with the attached adapter
15	CC1	Communication Channel 1 pin used to negotiate a voltage/current with the attached adapter
16	D-	Leave this pin unconnected
17	D+	Leave this pin unconnected
18	VBUS_IN	Connect to VBUS of USB Type-C connector. Used to supply power to the EZ-PD BCR device and monitor incoming voltage.
19	GND	System Ground pin
20	DNU1	Leave this pin unconnected
21	DNU2	Leave this pin unconnected
22	VSS	Ground pin, connect to USB Type-C connector GND.

Table 1. EZ-PD BCR Pin Descriptions *(continued)*

24-Pin QFN	Pin Name	Description
23	VDDD	Output of internal 3.3-V regulator. Connect 1 µF and 2x 100-nF capacitors.
24	VCCD	Output of internal 1.8-V regulator. Connect a 1-µF decoupling capacitor.
–	EPAD	Ground

Figure 2. Pinout of 24-QFN Package (Top View)

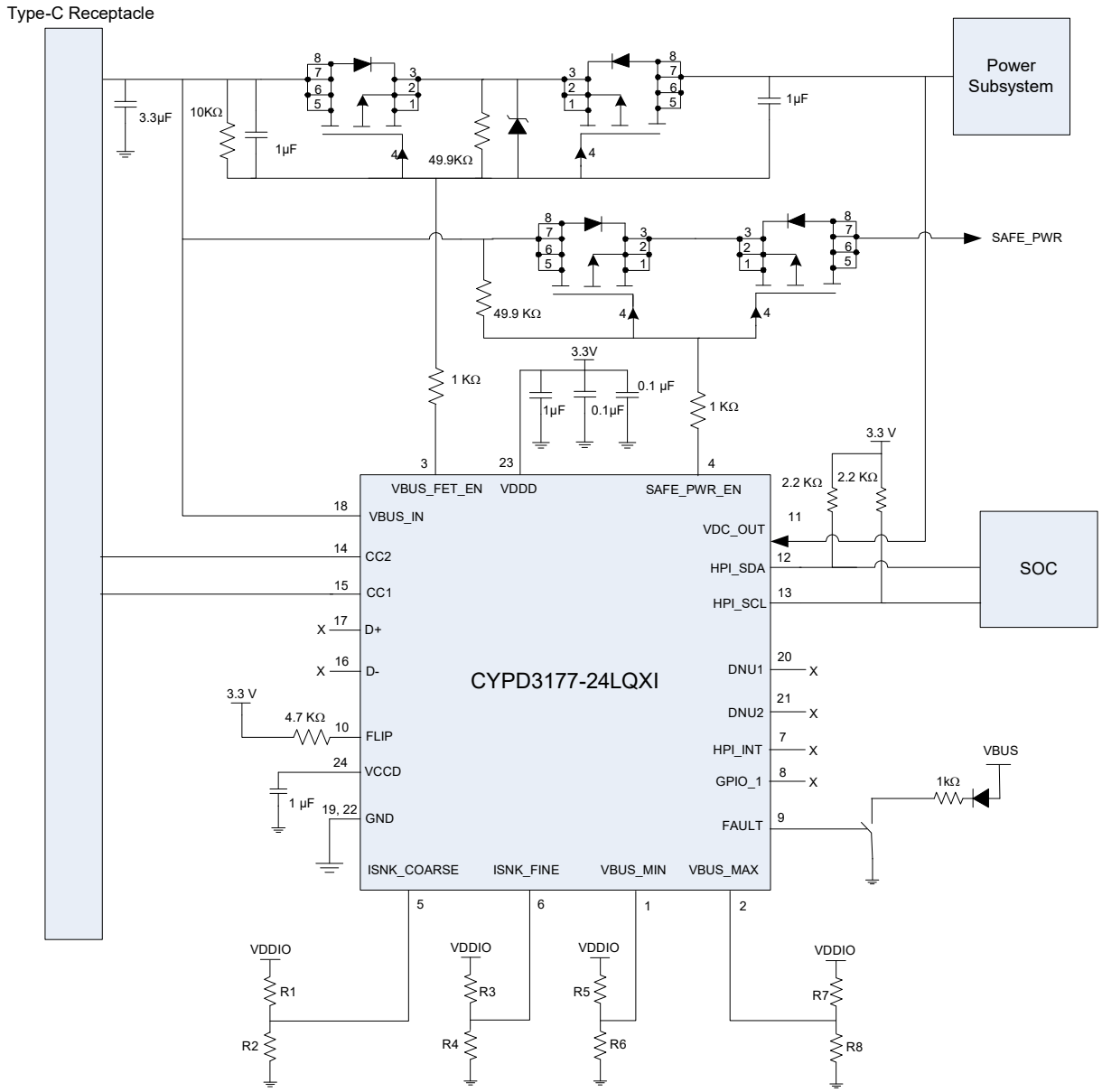


Application Overview

Figure 3 shows the EZ-PD BCR-based application diagram using the 24-pin QFN part. It has three main parts: USB Type-C receptacle to provide the input power to the application, the Power Subsystem used as the output power, and four sets of resistor divider networks to select the desired output voltage and current values.

The 'Fault' pin is used to indicate any voltage faults. When a fault condition is enabled, the output voltage of this application will go down to 0V and the EZ-PD BCR device will attempt a protocol reset to recover from fault. For a detailed reference schematic, refer to the CY4533 EZ-PD BCR EVK schematic.

Figure 3. EZ-PD BCR based Application Diagram (for Electronic Systems Requiring 12 V to 15 V Input at 2 A)



Notes
1. Refer to Table 2, Table 3, and Table 4 for values of these resistor divider networks.
2. FLIP pin is in LOW state when TypeC Plug is upside-up, and in Hi-Z state when upside-down.
3. Use a 50-kΩ resistor on the FLIP pin to set the UFP VDO data capability bit to 0.

The four sets of resistor divider networks are used to determine the voltage and current range that the EZ-PD BCR device will negotiate with the USB Type-C power adapter. Table 2, Table 3, and Table 4 show the values of pull-up and pull-down resistors on each pin applicable for a desired VBUS_MIN, VBUS_MAX, ISNK_COARSE or ISNK_FINE value.

Note 1: If VBUS_MIN is more than VBUS_MAX, the setting on VBUS_MAX is used as both minimum and maximum VBUS setting for the system.

Note 2: EZ-PD BCR device does not monitor the current on VBUS_IN and enforce it within ISNK limits. It is the responsibility of the system to not consume more current than what the power adapter can provide.

Note 3: VBUS_MIN and VBUS_MAX can be set to the same value to select one specific voltage level from the Type-C power adapter.

Note 4: Ensure that the board layout design does not inject any noise into the VBUS_MIN, VBUS_MAX, ISNK_COARSE, ISNK_FINE pins.

Table 2. Resistor Divider Values for Minimum or Maximum Voltage Requested on VBUS

Voltage Requested (V)	Resistor Ratio Relative to VDDD = 3.3 V	Suggested Pull-up Resistor value (kΩ)	Suggested Pull-down Resistor value (kΩ)	Voltage Range on Pin (mV)
5	0/6	Open	0	0–248
9	1/6	5.1	1	249–786
12	2/6	5.1	2.4	787–1347
15	3/6	5.1	5.1	1348–1920
19	4/6	5.1	10	1921–2778
20	≥ 5/6	0	Open	≥ 2779

Table 3. Resistor Divider Values for Coarse Setting on Operating Current (For VDDD = 3.3 V)

Operating Current Requested for Coarse Setting (A)	Resistor Ratio Relative to VDDD = 3.3 V	Suggested Pull-up Resistor Value (kΩ)	Suggested Pull-down Resistor Value (kΩ)	Voltage Range on Pin (mV)
0	0/6	Open	0	0–248
1	1/6	5.1	1	249–786
2	2/6	5.1	2.4	787–1347
3	3/6	5.1	5.1	1348–1920
4	4/6	5.1	10	1921–2778
5	≥ 5/6	0	Open	≥ 2779

Table 4. Resistor Divider Values for Fine Setting on Operating Current (For VDDD = 3.3 V)

Operating Current Requested for Fine Setting (A)	Resistor Ratio Relative to VDDD = 3.3 V	Suggested Pull-up Resistor Value (kΩ)	Suggested Pull-down Resistor Value (kΩ)	Voltage Range on Pin (mV)
+0	0/6	Open	0	0–248
+250	1/6	5.1	1	249–786
+500	2/6	5.1	2.4	787–1347
+750	3/6	5.1	5.1	1348–1920
+900	≥ 4/6	0	Open	≥ 1921

FAULT Pin Behavior

FAULT is driven to Logic HIGH if at least one of the following conditions is met:

- Type-C power adapter cannot supply a voltage within VBUS_MIN and VBUS_MAX settings and/or supply a current of at least ISNK_COARSE + ISNK_FINE value.
- Voltage on VBUS_IN is 20% below the VBUS_MIN setting or 20% above the VBUS_MAX setting.

FAULT is driven to Logic LOW otherwise.

SAFE_PWR_EN pin Behavior

SAFE_PWR_EN is a PFET gate driver that can be used to provide power to the system when an incompatible power adapter is attached to the system. SAFE_PWR_EN is driven to 0V when the Type-C power adapter cannot supply a voltage within VBUS_MIN and VBUS_MAX settings and/or supply a current of at least ISNK_COARSE + ISNK_FINE value. In this case, the EZ-PD BCR device negotiates for a 5V@ I_{SNK} contract with the USB-PD Power Adapter when possible.

SAFE_PWR_EN pin is left floating (High-Z) in all other conditions.

VBUS_FET_EN pin Behavior

The VBUS_FET_EN pin is a PFET gate driver that drives to either 0 V or VBUS_IN depending on the state of the Type-C connection. Contact Cypress Technical Support for more details on how to use this pin for specific applications.

Electrical Specifications

Absolute Maximum Ratings

Table 5. Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
V_{BUS_MAX}	Max supply voltage relative to V_{SS} on VBUS_IN and VDC_OUT pins	–	–	30	V	Absolute max
V_{DDD_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	
$V_{CC\_PIN\_ABS}$	Max voltage on CC1, CC2 pins	–	–	22[1]	V	
V_{GPIO_ABS}	GPIO voltage	–0.5	–	V_{DDD} +0.5	V	
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	
$I_{GPIO\_injection}$	GPIO injection current, Max for $V_{IH} > V_{DDD}$, and Min for $V_{IL} < V_{SS}$	–0.5	–	0.5	mA	Absolute max, current injected per pin
$V_{GPIO\_OVT\_ABS}$	OVT GPIO voltage	–0.5	–	6	V	Applicable to pins HPI_INT and GPIO_1
ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
LU	Pin current for latch-up	–100	–	100	mA	–
ESD_IEC_CON	Electrostatic discharge IEC61000-4-2	8000	–	–	V	Contact discharge on CC1, CC2, VBUS_IN, HPI_SDA and HPI_SCL pins
ESD_IEC_AIR	Electrostatic discharge IEC61000-4-2	15000	–	–	V	Air discharge for D+, D-, CC1, CC2, VBUS_IN, HPI_SDA and HPI_SCL pins

Device-Level Specifications

All specifications are valid for –40 °C ≤ T_A ≤ 105°C and T_J ≤ 120°C, except where noted.

Table 6. DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.PWR#2	V_{DDD}	Power supply input voltage	2.7	–	5.5	V	Sink mode, –40°C ≤ T_A ≤ 105°C.
SID.PWR#2_A	V_{DDD}	Power supply input voltage	3.0	–	5.5	V	Source mode, –40°C ≤ T_A ≤ 105°C.
SID.PWR#3	V_{BUS_IN}	Power supply input voltage	3.0	–	24.5	V	–40 °C ≤ T_A ≤ 105°C.
SID.PWR#5	V_{CCD}	Output voltage for core Logic	–	1.8	–	V	–
SID.PWR#13	C_{exc}	Power supply decoupling capacitor for V_{DDD}	0.8	1	–	µF	X5R ceramic or better
SID.PWR#14	C_{exv}	Power supply decoupling capacitor for VBUS_IN_DISH-CARGE	–	0.1	–	µF	X5R ceramic or better

Note
1. As per USB PD specification, maximum allowed VBUS = 21.5 V.

Table 6. DC Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
Active Mode. Typical values measured at V_{DDD} = 5.0 V or V_{BUS} = 5.0 V and T_A = 25°C.							
SID.PWR#8	I_{DD_A}	Supply current from V_{BUS} or V_{DDD}	–	10	–	mA	V_{DDD} = 5 V OR V_{BUS} = 5 V, T_A = 25°C. CC1/CC2 in Tx or Rx, no I/O sourcing current, 2 SCBs at 1 Mbps, EA/ADC/CSA/UVOV ON, CPU at 24 MHz.
Sleep Mode. Typical values measured at V_{DD} = 3.3 V and T_A = 25°C.							
SID25A	I_{DD_S}	CC, I^2C, WDT wakeup on. IMO at 24 MHz.	–	3	–	mA	V_{DDD} = 3.3 V, T_A = 25°C, All blocks except CPU are on, CC IO on, EA/ADC/CSA/UVOV On.
Deep Sleep Mode. Typical values measured at T_A = 25°C.							
SID_P-B_DS_A_SNK	$I_{DD\_PB\_DS\_A\_SNK}$	V_{BUS} 4.0 to 24.5 V. CC, I^2C, WDT Wakeup on	–	500	–	µA	For sink applications, V_{BUS} = 24.5 V, T_A = 25 °C, Part is in deep sleep. Attached, CC I/O on, ADC/CSA/UVOV on.

Table 7. AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.PWR#17	T_{SLEEP}	Wakeup from sleep mode	–	0	–	µs	–
SID.PWR#18	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	–	35	µs	–
SYS.FES#1	$T_{\_PWR\_RDY}$	Power-up to “Ready to accept I^2C/CC command”	–	5	25	ms	–
SID.PWR#18A	$T_{POR\_HIZ\_T}$	Power-on I/O Initialization Time	–	3	–	ms	–

I/O

Table 8. I/O DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.GIO#37	V_{IH_CMOS}	Input voltage HIGH threshold	0.7 × V_{DDD}	–	–	V	CMOS input
SID.GIO#38	V_{IL_CMOS}	Input voltage LOW threshold	–	–	0.3 × V_{DDD}	V	CMOS input
SID.GIO#33	V_{OH_3V}	Output voltage HIGH level	V_{DDD} –0.6	–	–	V	I_{OH} = 4 mA at 3-V V_{DDD}
SID.GIO#36	V_{OL_3V}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 10 mA at 3-V V_{DDD}
SID.GIO#16	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	+25°C T_A, 3-V V_{DDD}
SID.GIO#17	C_{PIN_A}	Max pin capacitance	–	–	22	pF	Capacitance on D+, D- pins. Guaranteed by characterization.
SID.GIO#17A	C_{PIN}	Max pin capacitance	–	3	7	pF	–40°C to +85°C T_A, All V_{DDD}, all other I/O_S. Guaranteed by characterization.
SID.GIO#44	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDD}	–	–	mV	V_{DDD} < 4.5 V. Guaranteed by characterization.

Table 8. I/O DC Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID69	I_{DIODE}	Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	Guaranteed by design.
SID.GIO#45	I_{TOT_GPIO}	Maximum total sink chip current	–	–	85	mA	Guaranteed by design.
OVT							
SID.GIO#46	I_{IHS}	Input current when Pad > V_{DDD} for OVT inputs	–	–	10.00	µA	Per I^2C specification

Table 9. I/O AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID70	T_{RISEF}	Rise time in Fast Strong mode	2	–	12	ns	3.3-V V_{DDD}, C_{load} = 25 pF
SID71	T_{FALLF}	Fall time in Fast Strong mode	2	–	12	ns	3.3-V V_{DDD}, C_{load} = 25 pF

Table 10. HPI Pins DC Specifications (Applicable to pins HPI_SDA and HPI_SCL only)

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.GPIO_20VT#4	GPIO_20VT_I_LU	GPIO_20VT Latch up current limits	–140	–	140	mA	Max / min current in to any input or output, pin-to-pin, pin-to-supply
SID.GPIO_20VT#5	GPIO_20VT_RPU	GPIO_20VT Pull-up resistor value	1	–	25	kΩ	+25°C T_A, 1.4 V to GPIO_20VT_Voh(min)
SID.GPIO_20VT#6	GPIO_20VT_RPD	GPIO_20VT Pull-down resistor value	2.5	–	20	kΩ	+25°C T_A, 1.4-V to V_{DDD}
SID.GPIO_20VT#16	GPIO_20VT_IIL	GPIO_20VT Input leakage current (absolute value)	–	–	2	nA	+25°C T_A, 3-V V_{DDD}
SID.GPIO_20VT#17	GPIO_20VT_CPIN	GPIO_20VT pin capacitance	15	–	25	pF	–40°C to +85°C T_A, All V_{DDD}, F = 1 MHz
SID.GPIO_20VT#36	GPIO_20VT_Vol	GPIO_20VT Output Voltage low level	–	–	0.4	V	I_{OL} = 2 mA
SID.GPIO_20VT#69	GPIO_20VT_IDIODE	GPIO_20VT Current through protection diode to V_{DDD}/V_{SS}	–	–	100	µA	–

Table 11. HPI Pins AC Specifications (Applicable to pins HPI_SDA and HPI_SCL only)

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.GPIO_20VT#70	GPIO_20VT_TriseF	GPIO_20VT Rise time in Fast Strong Mode	1	–	45	ns	All V_{DDD}, C_{load} = 25 pF
SID.GPIO_20VT#71	GPIO_20VT_TfallF	GPIO_20VT Fall time in Fast Strong Mode	2	–	15	ns	All V_{DDD}, C_{load} = 25 pF

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

I^2C

Table 12. Fixed I^2C DC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID149	I_{I2C1}	Block current consumption at 100 kHz	–	–	100	µA	–
SID150	I_{I2C2}	Block current consumption at 400 kHz	–	–	135	µA	–
SID152	I_{I2C4}	I^2C enabled in Deep Sleep mode	–	1.4	–	µA	–

Table 13. Fixed I^2C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	400	kbps	–

System Resources

Power-on-Reset (POR) with Brown Out SWD Interface

Table 14. Imprecise Power On Reset (PRES) (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID185	$V_{RISEIPOR}$	Power-on Reset (POR) rising trip voltage	0.80	–	1.50	V	–
SID186	$V_{FALLIPOR}$	POR falling trip voltage	0.70	–	1.4	V	–

Table 15. Precise Power On Reset (POR)

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID190	$V_{FALLPPOR}$	Brown-out Detect (BOD) trip voltage in active/sleep modes	1.48	–	1.62	V	–
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep mode	1.1	–	1.5	V	–

Table 16. USB PD DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.PD.4	Rd	UFP CC termination	4.59	5.1	5.61	kΩ	–
SID.PD.5	Rd_DB	UFP (Power Bank) Dead Battery CC Termination on CC1 and CC2	4.08	5.1	6.12	kΩ	All supplies forced to 0V and 1.32 V applied at CC1 or CC2
SID.PD.6	Vgndoffset	Ground offset tolerated by BMC receiver	–500	–	500	mV	Relative to the remote BMC transmitter

Gate Driver Specifications

Table 17. Gate Driver DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.GD.1	R_{PD}	Pull-down resistance	–	–	3	kΩ	Applicable on VBUS_P_CTRL and VBUS_C_CTRL to turn ON external PFET.
SID.GD.2	R_{PU}	Pull-up resistance	–	–	4	kΩ	Applicable on VBUS_P_CTRL to turn OFF external PFET.
SID.GD.3	I_{PD0}	Pull-down current sink at drive strength of 1	25	–	75	µA	I-mode (current mode) pull down at 5 V. Applicable on VBUS_P_CTRL and VBUS_C_CTRL to turn ON external PFET.
SID.GD.4	I_{PD1}	Pull-down current sink at drive strength of 2	50	–	150	µA	
SID.GD.5	I_{PD2}	Pull-down current sink at drive strength of 4	140	–	300	µA	
SID.GD.6	I_{PD3}	Pull-down current sink at drive strength of 8	280	–	580	µA	
SID.GD.7	I_{PD4}	Pull-down current sink at drive strength of 16	560	–	1200	µA	
SID.GD.8	I_{PD5}	Pull-down current sink at drive strength of 32	1120	–	2300	µA	
SID.GD.9	I_leak_p1	Pin leakage on VBUS_P_CTRL	–	0.003	–	µA	+25°C T_J, 5-V V_{DDD}, 20-V V_{BUS}
SID.GD.10	I_leak_c1	Pin leakage on VBUS_C_CTRL	–	0.003	–	µA	+25°C T_J, 5-V V_{DDD}, 20-V V_{BU}
SID.GD.11	I_leak_p2	Pin leakage on VBUS_P_CTRL	–	–	2	µA	+85°C T_J, 5-V V_{DDD}, 20-V V_{BU}
SID.GD.12	I_leak_c2	Pin leakage on VBUS_C_CTRL	–	–	2	µA	+85°C T_J, 5-V V_{DDD}, 20-V V_{BU}
SID.GD.13	I_leak_p3	Pin leakage on VBUS_P_CTRL	–	–	7	µA	+125°C T_J, 5-V V_{DDD}, 20-V V_{BU}
SID.GD.14	I_leak_c3	Pin leakage on VBUS_C_CTRL	–	–	7	µA	+125°C T_J, 5-V V_{DDD}, 20-V V_{BU}

Table 18. Gate Driver AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.GD.15	T_{PD1}	Pull down delay on SAFE_PWR_EN	–	–	2	µs	Cload = 2 nF, Delay to VBUS –1.5 V from initiation of falling edge, VBUS = 5 V to 20 V, 50 kΩ tied between VBUS_C_CTRL and VBUS
SID.GD.16	$T_{r\_discharge}$	Discharge rate of output node on SAFE_PWR_EN	–	–	5	V/µs	80% to 20%, 50 kΩ tied between VBUS_C_CTRL and VBUS, Cload = 2 nF, Vinitial = 24 V
SID.GD.17	T_{PD2}	Pull down delay on VBUS_FET_EN	–	–	2	µs	Cload = 2 nF, Delay to VBUS –1.5 V from initiation of falling edge, V_{BUS} = 5 V to 20 V, 50 kΩ tied between VBUS_C_CTRL and VBUS
SID.GD.18	T_{PU}	Pull up delay on VBUS_FET_EN	–	–	18	µs	Cload = 2 nF, Delay to VBUS–1.5 V from initiation of falling edge, VBUS = 5 V to 20 V, 50 kΩ tied between VBUS_C_CTRL and VBUS
SID.GD.19	SR_{PU}	Output slew rate on VBUS_FET_EN	–	–	5	V/µs	Cload = 2 nF, 20% to 80% of VBUS_P_CTRL range
SID.GD.20	SR_{PD}	Output slew rate on VBUS_FET_EN	–	–	5	V/µs	Cload = 2 nF, 80% to 20% of VBUS_P_CTRL range

Table 19. VBUS Discharge Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.VBUS.DISC.6	I1	20-V NMOS ON current for DS = 1	0.15	–	1	mA	Measured at 0.5 V
SID.VBUS.DISC.7	I2	20-V NMOS ON current for DS = 2	0.4	–	2	mA	
SID.VBUS.DISC.8	I4	20-V NMOS ON current for DS = 4	0.9	–	4	mA	
SID.VBUS.DISC.9	I8	20-V NMOS ON current for DS = 8	2	–	8	mA	
SID.VBUS.DISC.10	I16	20-V NMOS ON current for DS = 16	4	–	10	mA	
SID.VBUS.DISC.11	VBUS_Stop_Error	Error percentage of final V_{BUS} value from setting	–	–	10	%	When V_{BUS} is discharged to 5 V. Guaranteed by Characterization.

Table 20. Voltage (VBUS) Regulation DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.DC.VR.1	$V_{\_IN\_3}$	V(pad_in) at 3-V target	2.85	3	3.15	V	Active mode shunt regulator at 3 V with bandgap
SID.DC.VR.2	$V_{\_IN\_5}$	V(pad_in) at 5-V target	4.75	5	5.25	V	Active mode shunt regulator at 5 V
SID.DC.VR.3	$V_{\_IN\_9}$	V(pad_in) at 9-V target	8.55	9	9.45	V	Active mode shunt regulator at 9 V
SID.DC.VR.4	$V_{\_IN\_15}$	V(pad_in) at 15-V target	14.25	15	15.75	V	Active mode shunt regulator at 15 V
SID.DC.VR.5	$V_{\_IN\_20}$	V(pad_in) at 20-V target	19	20	21	V	Active mode shunt regulator at 20 V
SID.DC.VR.6	$V_{\_IN\_3\_DS}$	V(pad_in) at 3-V target	2.7	3	3.3	V	Deep Sleep mode shunt regulator at 3 V with bandgap
SID.DC.VR.7	$V_{\_IN\_5\_DS}$	V(pad_in) at 5-V target	4.5	5	5.5	V	Deep Sleep mode shunt regulator at 5 V
SID.DC.VR.8	$V_{\_IN\_9\_DS}$	V(pad_in) at 9-V target	8.1	9	9.1	V	Deep Sleep mode shunt regulator at 9 V
SID.DC.VR.9	$V_{\_IN\_15\_DS}$	V(pad_in) at 15-V target	13.5	15	16.5	V	Deep Sleep mode shunt regulator at 15 V
SID.DC.VR.10	$V_{\_IN\_20\_DS}$	V(pad_in) at 20-V target	18	20	22	V	Deep Sleep mode shunt regulator at 20 V
SID.DC.VR.11	I_{KA_OFF}	Off-state cathode current	–	–	10	µA	–
SID.DC.VR.12	I_{KA_ON}	Current through cathode pin	–	–	10	mA	–

Table 21. VBUS Short Protection Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.VSP.1	V_SHORT_TRIGGER	Short-to-VBUS system-side clamping voltage on the CC/P2.2/P2.3 pins	–	9	–	V	Guaranteed by Characterization.

Table 22. VBUS DC Regulator Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.VREG.2	VBUS_DETECT	VBUS detect threshold voltage	1.08	–	2.62	V	–

Table 23. VBUS AC Regulator Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.VREG.3	T_{start}	Total startup time for the regulator supply outputs	–	–	200	µs	Guaranteed by Characterization.

Analog to Digital Converter (Used for Determining VBUS_MIN,

Table 24. ADC DC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	Bits	–
SID.ADC.2	INL	Integral non-linearity	–2.5	–	2.5	LSB	Reference voltage generated from VDDD
SID.ADC.2A	INL	Integral non-linearity	–1.5	–	1.5	LSB	Reference voltage generated from bandgap
SID.ADC.3	DNL	Differential non-linearity	–2.5	–	2.5	LSB	Reference voltage generated from VDDD
SID.ADC.3A	DNL	Differential non-linearity	–1.5	–	1.5	LSB	Reference voltage generated from bandgap
SID.ADC.4	Gain Error	Gain error	–1.5	–	1.5	LSB	–
SID.ADC.6	V_{REF_ADC2}	ADC reference voltage when generated from band gap.	1.96	2.0	2.04	V	Reference voltage generated from bandgap

VBUS_MAX, ISNK_COARSE, ISNK_FINE Values)

Table 25. ADC AC Specifications (Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.ADC.7	SLEW_Max	Rate of change of sampled voltage signal	–	–	3	V/ms	–

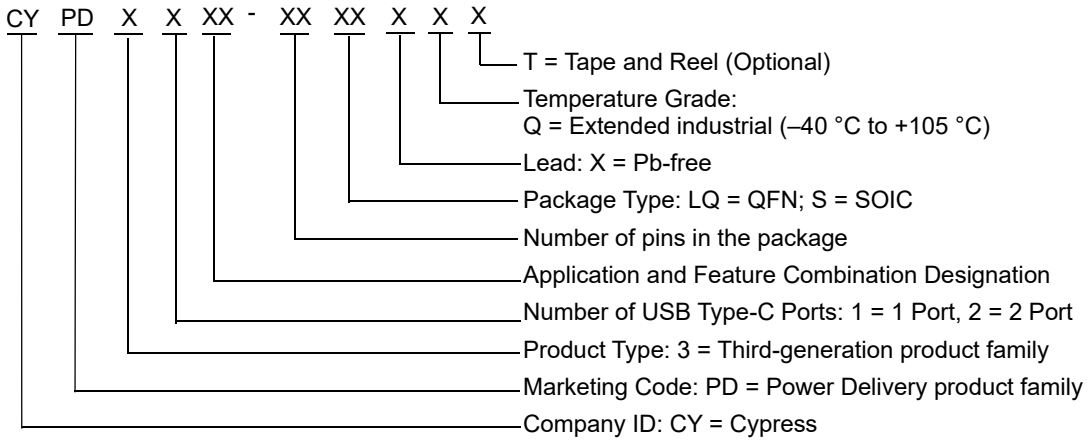
Ordering Information

Table 26 lists the EZ-PD BCR part numbers and features.

Table 26. EZ-PD BCR Ordering Information

MPN	Application	Termination Resistor	Role	Package Type	Si ID
CYPD3177-24LQXQ	Barrel Connector Replacement or Generic UFP Sink	R_D, $R_{D\text{-}DB}$	UFP	24-Pin QFN	2004

Ordering Code Definitions



Packaging

Table 27. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Operating ambient temperature	Extended Industrial	–40	25	105	°C
T_J	Operating junction temperature	Extended Industrial	–40	25	120	°C
T_{JA}	Package θ_{JA} (24-QFN)	–	–	–	19.98	°C/W
T_{JC}	Package θ_{JC} (24-QFN)	–	–	–	4.78	°C/W

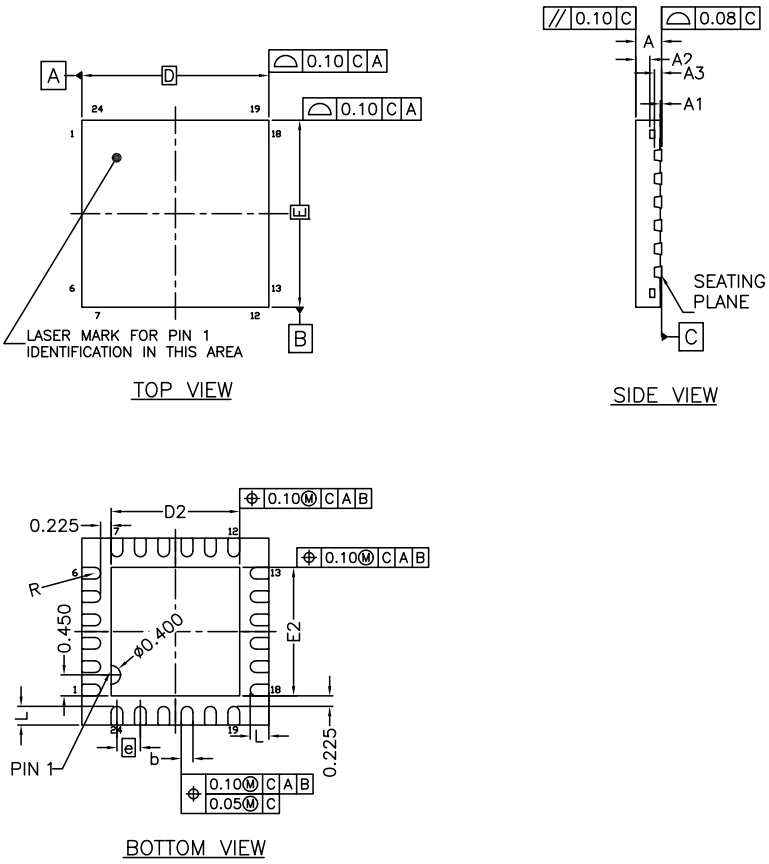
Table 28. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time within 5 °C of Peak Temperature
24-pin QFN	260 °C	30 seconds

Table 29. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
24-pin QFN	MSL3

Figure 4. 24-pin QFN Package Outline



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	0.60
A_1	0.00	—	0.05
A_2	—	0.40	0.425
A_3	0.152 REF		
b	0.18	0.25	0.30
D	4.00 BSC		
D_2	2.65	2.75	2.85
E	4.00 BSC		
E_2	2.65	2.75	2.85
L	0.30	0.40	0.50
e	0.50 BSC		
R	0.09	—	—

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6. PACKAGE WARPAGE MAX 0.08 mm.
7. APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8. APPLIED ONLY TO TERMINALS.
9. JEDEC SPECIFICATION NO. REF: N.A.

002-16934 *C

Acronyms

Table 30. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
Arm®	advanced RISC machine, a CPU architecture
CC	configuration channel
CPU	central processing unit
CS	current sense
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
ESD	electrostatic discharge
GPIO	general-purpose input/output
IC	integrated circuit
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
I/O	input/output, see also GPIO
LDO	low-dropout regulator
MCU	microcontroller unit
NC	no connect
OVP	overvoltage protection
OVT	overvoltage tolerant
PD	power delivery
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse-width modulator
RISC	reduced-instruction-set computing
RX	receive
SCL	I^2C serial clock
SDA	I^2C serial data
SWD	serial wire debug, a test protocol
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
USB	Universal Serial Bus

Document Conventions

Units of Measure

Table 31. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	mega samples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
W	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

Document History Page

Document Title: EZ-PD™ BCR Datasheet, USB Type-C Port Controller for Power Sinks Document Number: 002-25383			
Revision	**ECN**	**Submission Date**	**Description of Change**
*A	6643829	08/01/2019	Release to web.
*B	7138986	05/18/2021	Updated USB PD 3.0 version details. Updated Pin 10 description in Pinouts. Added a note in Figure 3. Updated 24-pin QFN package drawing.