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General Description

EZ-PD™ CCG3PA Automotive (EZ-PD™ CYPD319X) devices are Cypress' highly integrated USB Type-C port controllers that comply with the latest USB Type-C and Power Delivery (PD) standards and are targeted for automotive charger applications such as rear seat chargers, infotainment head unit chargers, and rear seat entertainment chargers. In such applications, CYPD319X devices provide additional functionalities and BOM integration advantages. CYPD319X uses Cypress' proprietary M0S8 technology with a 32-bit Arm® Cortex®-M0 processor, 64-KB flash, a complete Type-C USB-PD transceiver, all termination resistors required for a Type-C port, an integrated feedback control circuitry for voltage (VBUS) regulation, and system-level ESD protection. They are available in 24-pin QFN wettable flank packages. The inclusion of a fully programmable MCU with analog and digital peripherals allows the implementation of custom system management functions such as power throttling, load sharing, and temperature monitoring.

Features

Type-C Support and USB-PD Support

- Supports USB PD3.0 Version 1.1 including Programmable Power Supply Mode
- Configurable resistors R_P and R_D
- Supports one USB Type-C port and one Type-A port

2x Legacy/Proprietary Charging Blocks

- Supports QC 4.0, Apple charging 2.4A, AFC, BC 1.2
- Integrates all required terminations on DP/DM lines

Integrated Voltage (VBUS) Regulation and Current Sense Amplifier

- Integrated shunt regulator function for VBUS control
- Constant current or constant voltage mode
- Supports current sensing for constant current control

System-Level Fault Protection

- VBUS-to-CC Short Protection
- On-chip VBUS, OVP, OCP, UVP, and SCP
- Supports OTP through integrated ADC circuit and internal temperature sensor

32-bit MCU Subsystem

- Arm Cortex-M0 CPU
- 64-KB Flash
- 8-KB SRAM

Clocks and Oscillators

- Integrated oscillator eliminating the need for external clock

Power

- 3.0-V to 24.5-V operation (30-V tolerant)

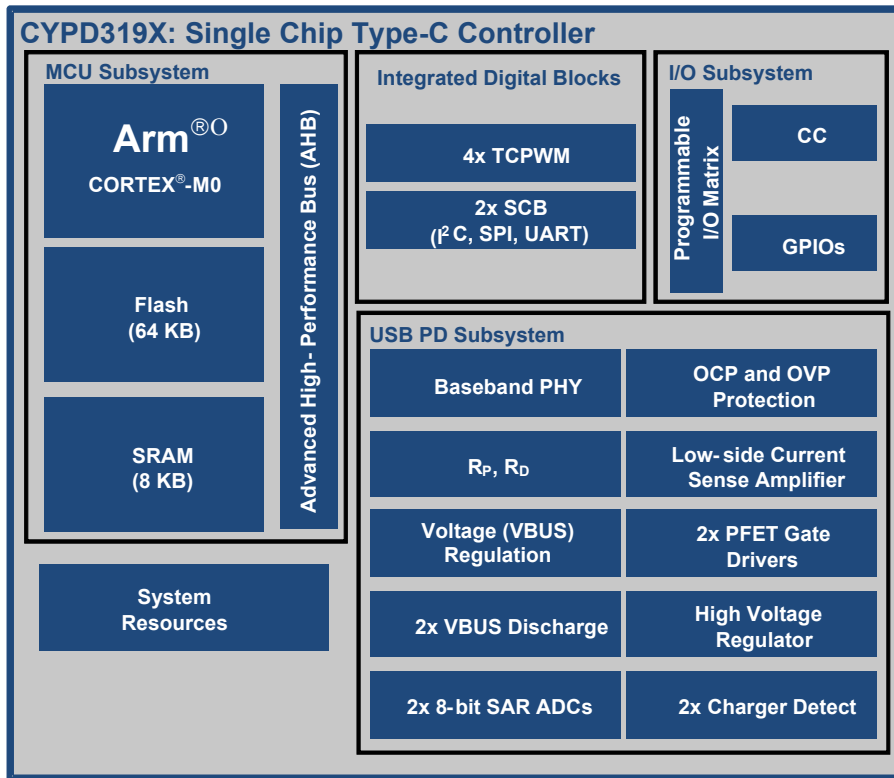
System-Level ESD Protection

- On CC, VBUS_C_MON_DISCHARGE, DP0, DM0, P2.2, and P2.3 pins
- ±8-kV Contact Discharge and ±15-kV Air Gap Discharge based on IEC61000-4-2 level 4C

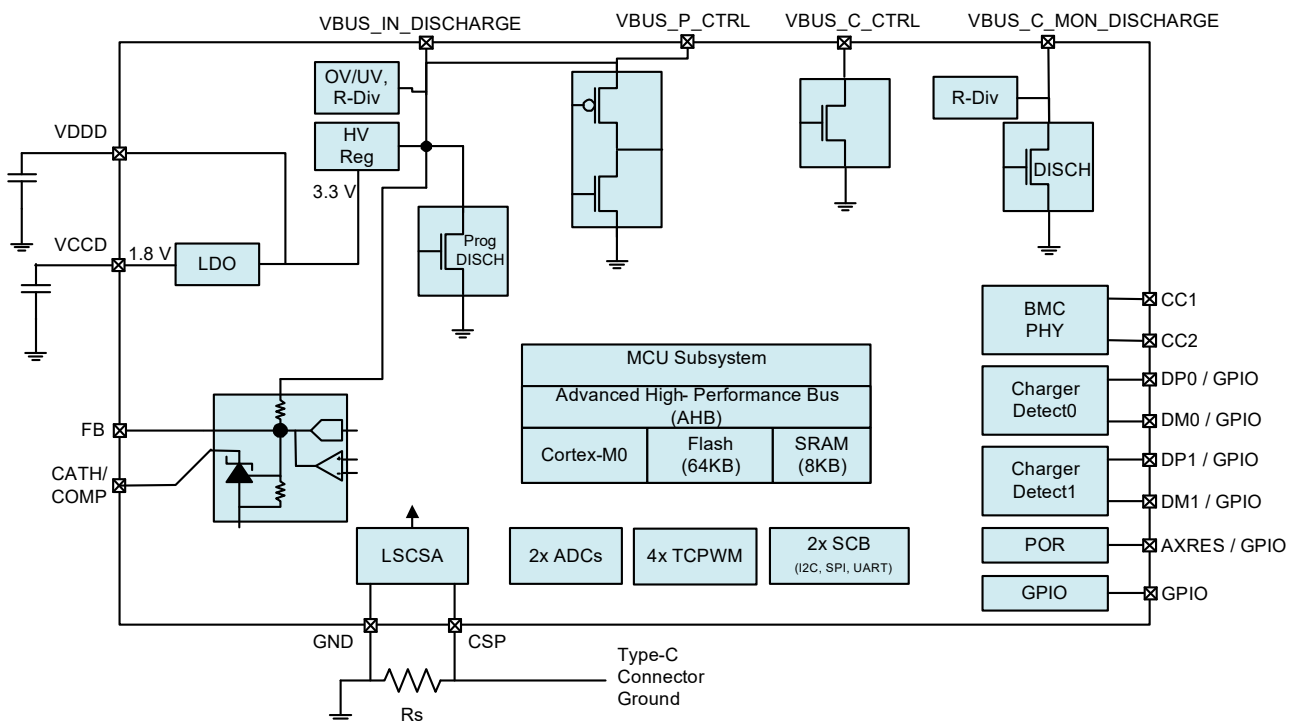
Packages

- 24-pin QFN, wettable flank, AEC-Q100
- Supports automotive temperature range (−40 °C to +105 °C)

Logic Block Diagram



Internal Block Diagram



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Functional Overview

MCU Subsystem

CPU

The Cortex-M0 CPU in CYPD319X devices is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating.

The CPU also includes a serial wire debug (SWD) interface, which is a two-wire form of JTAG. The debug configuration used for CYPD319X devices has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

CYPD319X devices have a flash module with one bank of 64-KB flash, a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

USB-PD Subsystem (SS)

The USB-PD subsystem provides the interface to the Type-C USB port. This subsystem comprises a current sense amplifier, a high-voltage regulator, overvoltage protection (OVP), overcurrent protection (OCP), and supply switch blocks. This subsystem also includes all ESD required and supported on the Type-C port.

USB-PD Physical Layer

The USB-PD Physical Layer consists of a transmitter and receiver that communicate BMC-encoded data over the CC channel based on the PD 3.0 standard. All communication is half-duplex. The Physical Layer or PHY practices collision avoidance to minimize communication errors on the channel.

The USB-PD block includes all termination resistors (R_P and R_D) and their switches as required by the USB-PD specification. R_P and R_D resistors are required to implement connection detection and plug orientation detection, and establish USB DFP/UFP roles. The R_P resistor is implemented as a current source.

According to the USB Type-C specification, Type-C controllers such as CYPD319X devices must present certain termination resistors depending on its role in its unpowered state. As a car charger, CYPD319X devices are in a DFP role (as a power source), which requires both CC lines to be open.

ADC

The ADC is a low-footprint 8-bit SAR ADC that is available for general-purpose A/D conversion applications in the device. This ADC can be accessed from all GPIOs and the DP/DM pins through an on-chip analog mux. CYPD319X devices contain two instances of the ADC.

The voltage reference for the ADCs is generated either from the VDDD supply or from internal bandgap. When sensing the GPIO pin voltage with an ADC, the pin voltage cannot exceed the VDDIO supply value.

Charger Detection

The two charger detection blocks connected to the two pairs of DP/DM pins allow CYPD319X devices in DFP mode to detect conventional battery chargers conforming to BC 1.2, and the following proprietary charger specifications: Apple, Qualcomm's QuickCharge 4.0, and Samsung AFC.

VBUS Overcurrent and Overvoltage Protection

CYPD319X devices have an integrated hardware block for VBUS OVP/OCP with configurable thresholds and response times on the Type-C port.

VBUS Short Protection

CYPD319X devices provide four VBUS short protection pins: CC1, CC2, P2.2, and P2.3. These pins are protected from accidental shorts to high-voltage VBUS. Accidental shorts may occur because the CC1 and CC2 pins are placed next to the VBUS pins in the USB Type-C connector. A Power Delivery controller without the high-voltage VBUS short protection will be damaged in the event of accidental shorts. When the protection circuit is triggered, CYPD319X devices can handle up to 17 V forever and between 17 V to 22 VDC for 1000 hours on the OVT pins. When a VBUS short event occurs on the CC pins, a temporary high-ringing voltage is observed due to the RLC elements in the USB Type-C cable. Without the CYPD319X devices connected, this ringing voltage can be twice (44 V) the maximum VBUS voltage (21.5 V). However, when CYPD319X devices are connected, they are capable of clamping temporary high-ringing voltage and protecting the CC pin using IEC ESD protection diodes.

Current Sense Amplifier (CSA)

CYPD319X devices also have an integrated current sense amplifier that is capable of detecting current in the order of 100 mA across a 5-m Ω external resistor. It also supports constant current mode of operation in charging applications.

PFET Gate Drivers on VBUS Path

CYPD319X devices have two integrated PFET gate drivers to drive external PFETs on the VBUS provider and consumer path. The VBUS_P_CTRL gate driver has an active pull-up, and thus can drive high, low, or High-Z.

The VBUS_C_CTRL gate driver can drive only low or high-Z, thus requiring an external pull-up. These pins are VBUS voltage-tolerant.

VBUS Discharge FETs

CYPD319X devices also have two integrated VBUS discharge FETs used to discharge VBUS to meet the USB-PD specification timing on a detach condition. The VBUS discharge FET on the provider side can be used to accelerate the ramp down of VBUS to the default 5 V on the secondary side.

Voltage (VBUS) Regulation

CYPD319X devices contain an integrated feedback control circuitry with analog regulation of the feedback pin to achieve the appropriate voltage on VBUS pin according to the negotiated contract with the peer device over Type-C.

Integrated Digital Blocks

Serial Communication Blocks (SCB)

CYPD319X devices have two SCBs, which can be configured to implement an I²C, SPI, or UART interface. The hardware I²C blocks implement full multi-master and slave interfaces capable of multimaster arbitration. In the SPI mode, the SCB blocks can be configured to act as master or slave.

In the I²C mode, the SCB blocks are capable of operating at speeds of up to 1 Mbps (Fast-mode Plus) and have flexible buffering options to reduce interrupt overhead and latency for the CPU. These blocks also support I²C that creates a mailbox address range in the memory of CYPD319X devices and effectively reduces I²C communication to reading from and writing to an array in memory. In addition, the blocks support 8-deep FIFOs for receive and transmit which, by increasing the time given for the CPU to read data, greatly reduce the need for clock stretching caused by the CPU not having read the data on time.

The I²C peripherals are compatible with the I²C Standard-mode, Fast-mode, and Fast-mode Plus devices as defined in the NXP I²C-bus specification and user manual (UM10204). The I²C bus I/Os are implemented with GPIO in open-drain modes.

The I²C port on the SCB blocks of CYPD319X devices is not completely compliant with the I²C specification in the following aspects:

- GPIO cells for the SCB 1 I²C port are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independent of the rest of the I²C system.
- Fast-mode Plus has an I_{OL} specification of 20 mA at a V_{OL} of 0.4 V. The GPIO cells can sink a maximum of 8-mA I_{OL} with a V_{OL} maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the bus load.

Timer/Counter/PWM Block (TCPWM)

CYPD319X devices have four TCPWM blocks. Each implements a 16-bit timer, counter, pulse-width modulator (PWM), and quadrature decoder functionality. The block can be used to measure the period and pulse width of an input signal (timer), find the number of times a particular event occurs (counter), generate PWM signals, or decode quadrature signals.

I/O Subsystem

CYPD319X devices have up to 12 GPIOs some of which can be re-purposed to support SCB functions (I²C, UART, SPI). GPIO pins P0.0 and P0.1 are overvoltage-tolerant (OVT) (up to 7 V).

The GPIO block implements the following:

- Seven drive strength modes:
 - Input only
 - Weak pull-up with strong pull-down
 - Strong pull-up with weak pull-down
 - Open drain with strong pull-down
 - Open drain with strong pull-up
 - Strong pull-up with strong pull-down
 - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Hold mode to latch previous state (used to retain the I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control to improve EMI

During power-on and reset, I/O pins are forced to the disable state so as to not crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin.

Port pins P1.0 and P1.1 can be configured to indicate a fault for OCP/SCP/OVP/UVF conditions. Any two fault conditions can be mapped to two GPIOs, or all four faults can be OR'ed to indicate over one GPIO.

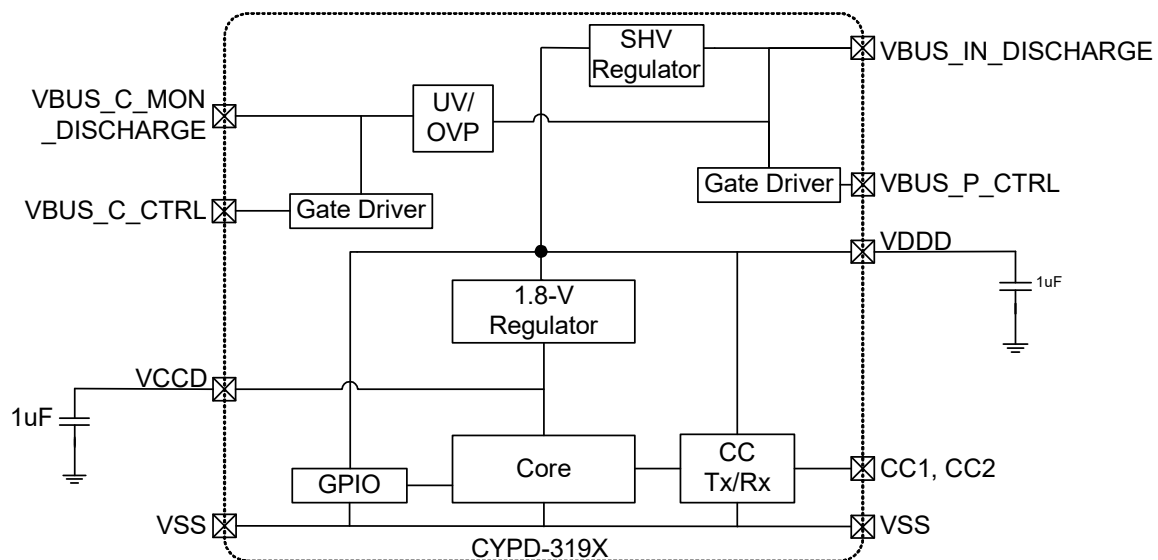
Power Systems Overview

CYPD319X devices can operate from two possible external supply sources: VBUS_IN_DISCHARGE (3.0 V–24.5 V) or VDDD (2.7 V–5.5 V). When powered through VBUS_IN_DISCHARGE, the internal regulator generates VDDD of 3.3 V for device operation. The regulated supply, VDDD, is either used directly inside some analog blocks or further regulated down to VCCD (1.8 V), which powers majority of the core using the regulators. CYPD319X devices have three different power modes: Active, Sleep, and Deep Sleep. Transitions between these power modes are managed by the power system. When powered through the VBUS_IN_DISCHARGE pin, VDDD cannot be used to power external devices and should be connected to a 1-μF capacitor for regulator stability only. These pins are not supported as power supplies. Refer to the application diagrams for capacitor connections.

Table 1. CYPD319X Power Modes

| Mode | Description |
|----------------------|---|
| Power-On Reset (POR) | Power is valid and an internal reset source is asserted, or SleepController is sequencing the system out of reset. |
| ACTIVE | Power is valid and CPU is executing instructions. |
| SLEEP | Power is valid and CPU is not executing instructions. All logic that is not operating is clock-gated to save power. |
| DEEP SLEEP | Main regulator and most blocks are shut off. DeepSleep regulator powers logic, but only low-frequency clock is available. |

Figure 1. Power System Requirement Block Diagram

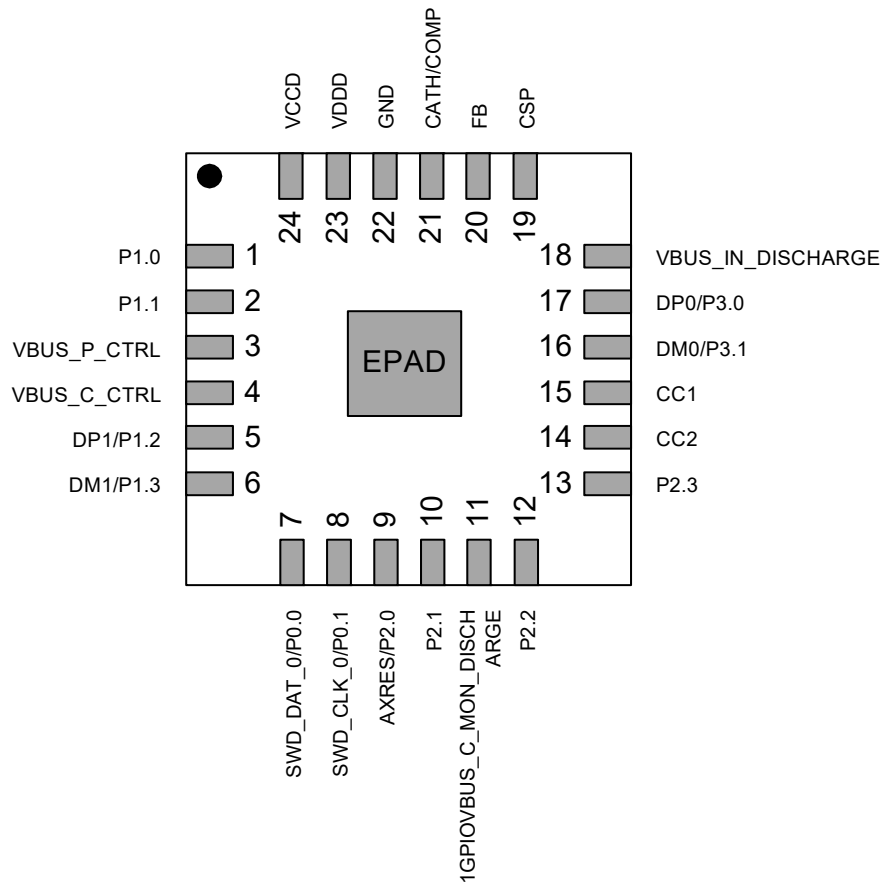


Pinouts

Table 2. Pin Descriptions

| 24-Pin QFN | Pin Name | Description |
|------------|-----------------------|---|
| 1 | P1.0 | Port 1 pin 0: GPIO/UART_1_CTS/I2C_SDA_1 / TCPWM_line_0, Programmable SCP/OCP/OVP/UVF Fault indication |
| 2 | P1.1 | Port 1 pin 1: GPIO/UART_1_RTS/I2C_SCL_1 / TCPWM_line_1, Programmable SCP/OCP/OVP/UVF Fault indication |
| 3 | VBUS_P_CTRL | Provider (PMOS) FET control (30-V tolerant) 0: Path ON 1: Path OFF |
| 4 | VBUS_C_CTRL | VBUS consumer (PMOS) FET control (30-V tolerant) 0: Path ON Z: Path OFF |
| 5 | DP1/P1.2 | USB D+/Port 1 pin 2: GPIO/UART_1_TX1/AFC/QC/BC 1.2/Apple Charging/No IEC |
| 6 | DM1/P1.3 | USB D-/Port 1 pin 3: GPIO/UART_1_RX1/AFC/QC/BC 1.2/Apple Charging/No IEC |
| 7 | SWD_DAT_0/P0.0 | Port 0 pin 0: GPIO/OVT/I2C_SDA_0/TCPWM_line_0/UART_0_CTS |
| 8 | SWD_CLK_0/P0.1 | Port 0 pin 1: GPIO/OVT/I2C_SCL_0/TCPWM_line_1/UART_0_RTS |
| 9 | AXRES/P2.0 | Port 2 pin 0: GPIO/Alternate XRES/TCPWM_line_0//UART_0_TX0 |
| 10 | P2.1 | Port 2 pin 1: GPIO/TCPWM_line_1//UART_0_RX0 |
| 11 | VBUS_C_MON_DIS-CHARGE | Type-C VBUS Monitor with Internal Discharge FET |
| 12 | P2.2 | Port 2 pin 2: GPIO with open drain with pull-up assist. Configurable as GPIO_20VT/I2C_SDA_1/IEC. Tolerant to temporary short to VBUS pin. |
| 13 | P2.3 | Port 2 pin 3: GPIO with open drain with pull-up assist. Configurable as GPIO_20VT/I2C_SCL_1/IEC. Tolerant to temporary short to VBUS pin. |
| 14 | CC2 | Communication Channel 2 with Dead-battery Rd Bonding Option/IEC. Tolerant to temporary short to VBUS pin. |
| 15 | CC1 | Communication Channel 1 with Dead-battery Rd Bonding Option/IEC. Tolerant to temporary short to VBUS pin. |
| 16 | DM0/P3.1 | USB D-/Port 3 pin 1: GPIO/UART_1_RX0/AFC/QC/BC 1.2/Apple Charging/IEC |
| 17 | DP0/P3.0 | USB D+/Port 3 pin 0: GPIO/UART_1_TX0/AFC/QC/BC 1.2/Apple Charging/IEC |
| 18 | VBUS_IN_DISCHARGE | VBUS power IN (3.0 V–24.5 V) with internal discharge FET |
| 19 | CSP | CS+: Current sense input |
| 20 | FB | Voltage regulation feedback pin |
| 21 | CATH/COMP | Cathode of voltage regulation and compensation for other applications |
| 22 | GND | Ground |
| 23 | VDDD | Power input: 2.7 V–5.5 V |
| 24 | VCCD | 1.8-V core voltage pin (not intended for use as a power source) |
| – | EPAD | Ground |

Figure 2. 24-QFN Package Pinout (Top View)



CYPD319X Programming and Bootloading

There are two ways to program the application firmware into a CYPD319X device:

- Programming the device flash over the SWD Interface
- Application firmware update over the CC interface

Generally, CYPD319X devices are programmed over the SWD interface only during development or during the manufacturing process of the end product. After the end product is manufactured, the CYPD319X device's application firmware can be updated via the CC bootloader interface.

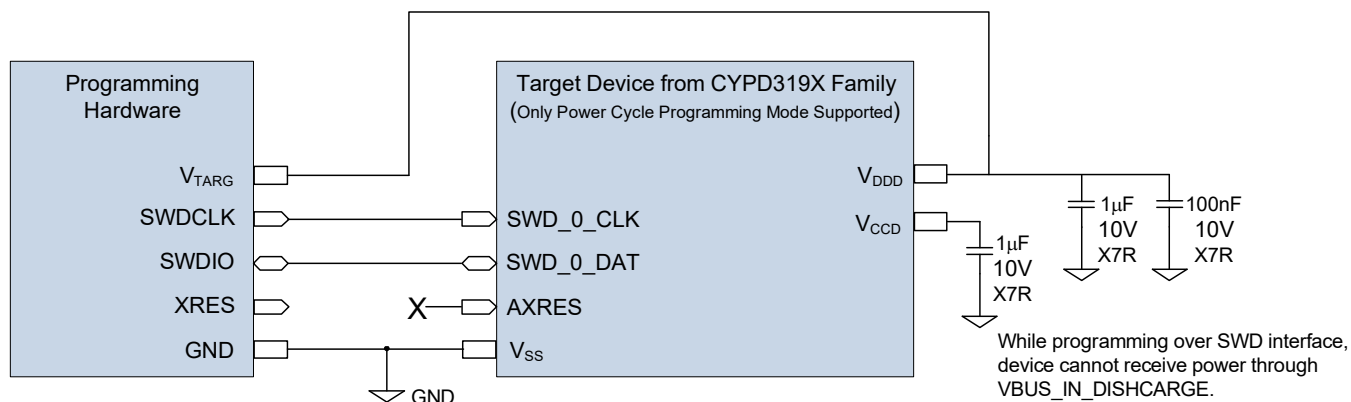
Programming the Device Flash over SWD Interface

CYPD319X devices can be programmed using the SWD interface. Cypress provides a programming kit, [CY8CKIT-002 MiniProg3 Kit](#) and [PSoC Programmer Software](#), which can be used to program the flash as well as debug firmware. The flash is programmed by downloading the information from a hex file. This hex file is a binary file generated as an output of building the firmware project in [PSoC Creator Software](#). Click [here](#) for more information on how to use the MiniProg3 programmer. There are many third-party programmers that support mass programming in a manufacturing environment.

As shown in the block diagram in [Figure 3](#), the SWD_0_DAT and SWD_0_CLK pins are connected to the host programmer's SWDIO (data) and SWDCLK (clock) pins respectively. During SWD programming, CYPD319X devices must be powered by the host programmer by connecting its VTARG (power supply to the target device) to the VDDD pin of a CYPD319X device. While programming over the SWD interface, the CYPD319X device cannot receive power through VBUS_IN_DISCHARGE.

CYPD319X devices do not have an XRES pin. Due to that, the XRES line from the host programmer remains unconnected; therefore, programming using Reset mode is not supported. In other words, CYPD319X devices are supported by Power Cycle programming mode only because the XRES line is not used. Contact Cypress for further details on CYPD3XXX Programming Specifications.

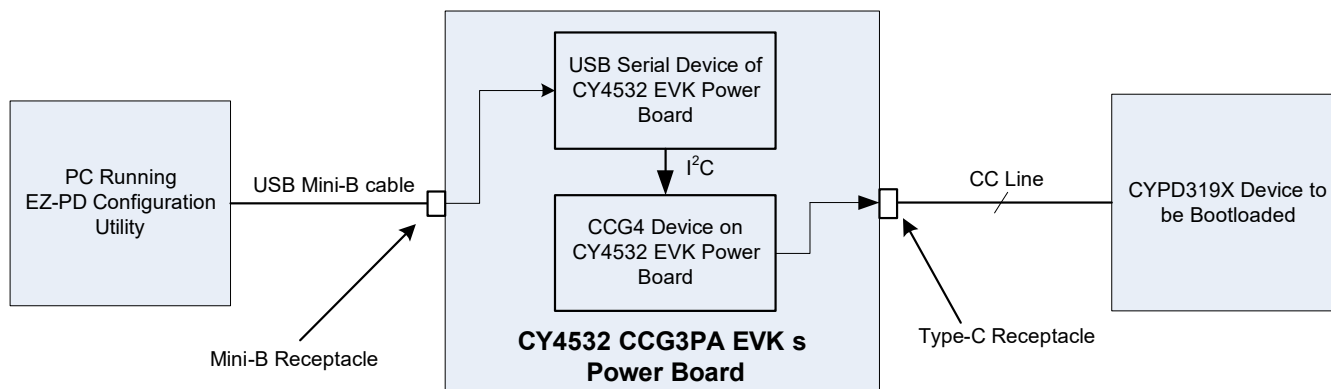
Figure 3. Connecting the Programmer to CYPD319X Device



Application Firmware Update over CC Interface

For bootloading CYPD319X device-based applications, the CY4532 CCG3PA EVK can be used to send programming and configuration data as Cypress-specific Vendor Defined Messages (VDMs) over the CC line. To bootload the CYPD319X device, the CY4532 CCG3PA EVK's power board is connected to the system containing the CYPD319X device on one end and a Windows PC running the EZ-PD™ Configuration Utility on the other end, as shown in [Figure 4](#).

Figure 4. Application Firmware Update over CC Interface

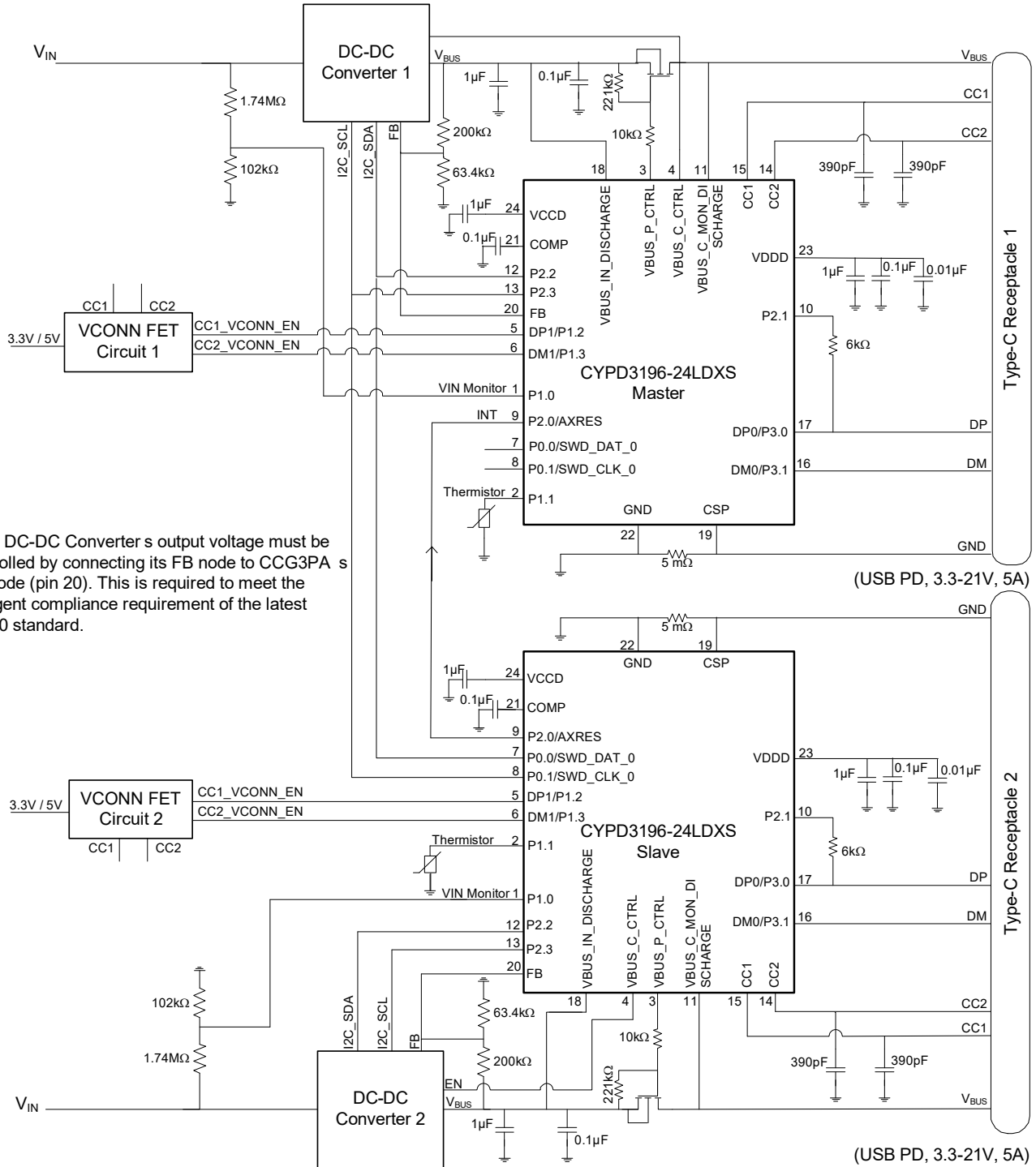


Application Firmware (FW) update feature over CC interface is intended for use during development and manufacturing. Cypress strongly recommends customers to use the [EZ-PD Configuration Utility](#) to turn off the Application FW Update over CC interface in the firmware that is updated into the CYPD319X device's flash before mass production. This prevents unauthorized firmware from being updated over CC-interface in the field. Refer to the knowledge base article [KBA230192](#) on how to configure this in EZ-PD Configuration Utility.

If you desire to retain the Application Firmware update over CC interface feature post-production for on-field firmware updates, contact [Cypress Sales](#) for further guidelines.

Application Diagrams

Figure 5. Dual Port USB-PD Charge Only Application Diagram Using CYPD3196-24LDXS

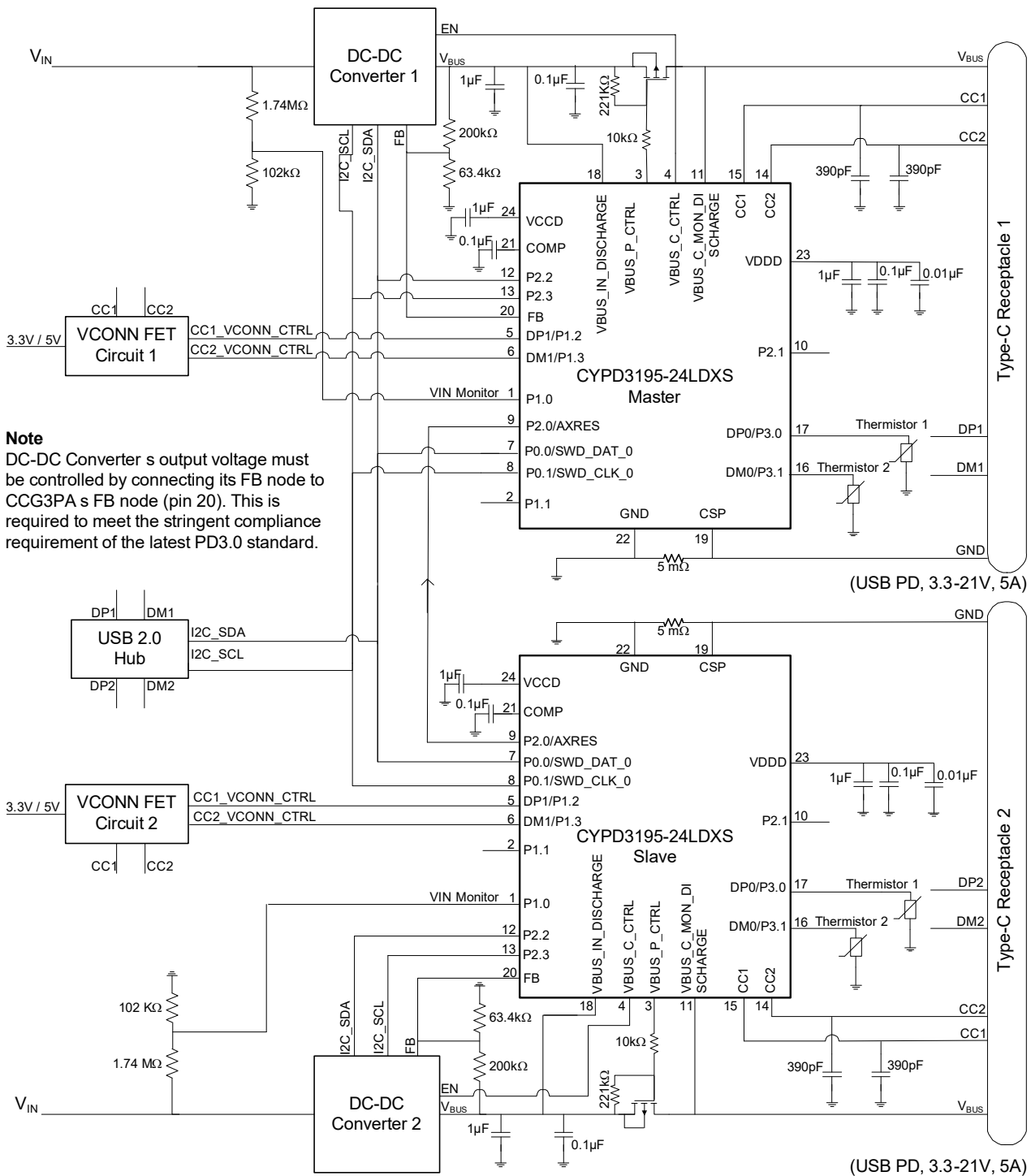


Note Refer to Cypress 2x100W Auto reference design files for a detailed schematic and layout.

Table 3. Pin Descriptions Specific to Application Diagram in Figure 5

| 24-Pin QFN | Pin Name | Description |
|------------|----------------------|---|
| 1 | P1.0 | VIN Monitoring GPIO |
| 2 | P1.1 | Thermistor |
| 3 | VBUS_P_CTRL | Provider (PMOS) FET control (30-V tolerant) |
| 4 | VBUS_C_CTRL | Enable DC-DC regulator. This is an optional connection; leave this pin floating if the DC-DC converter is always enabled. |
| 5 | DP1/P1.2 | Enables CC1 VCONN FET |
| 6 | DM1/P1.3 | Enables CC2 VCONN FET |
| 7 | P0.0/SWD_DAT_0 | Master: Free Slave: I2C Slave SDA for Load Sharing Connect to the host programmer's SWDIO (data) for programming the CCG3PA device |
| 8 | P0.1/SWD_CLK_0 | Master: Free Slave: I2C Slave SCL for Load Sharing Connect to the host programmer's SWDCLK (clock) for programming the CCG3PA |
| 9 | P2.0/AXRES | Interrupt from Slave CCG3PA to Master CCG3PA |
| 10 | P2.1 | GPIO drives 3.3-V output. Connect a 6-K resistor from this pin to DP to realize Apple charging. A 6-k resistor should be used if VDDD is 3.3 V and an 18-K resistor should be used if it is 5 V. |
| 11 | VBUS_C_MON_DISCHARGE | Type-C VBUS Monitor with Internal Discharge FET |
| 12 | P2.2/SWD_DAT_1 | Master: I2C Master data for DC/DC regulator and for communicating with CCG3PA Slave for Load Sharing Slave: I2C Master data for DC/DC regulator |
| 13 | P2.3/SWD_CLK_1 | Master: I2C Master clock for DC/DC regulator and for communicating with CCG3PA slave for Load Sharing Slave: I2C Master clock for DC/DC regulator |
| 14 | CC2 | Communication Channel 2 or VCONN |
| 15 | CC1 | Communication Channel 1 or VCONN |
| 16 | DM0/P3.1 | USB D- of Type-C port. Supports BC 1.2, QC, Apple Charging and AFC. |
| 17 | DP0/P3.0 | USB D+ of Type-C port. Supports BC 1.2, QC, Apple Charging and AFC |
| 18 | VBUS_IN_DISCHARGE | VBUS power IN (3.0 V–24.5 V) with internal discharge FET |
| 19 | CSP | CS+: Current sense input |
| 20 | FB | Voltage regulation feedback pin. Must be connected to the feedback node of DC-DC Converter. The pull-up resistor of the resistor divider network must be 200K; the pull-down resistor must be selected such that default VBUS upon power up is 5 V. |
| 21 | COMP | Compensation capacitor must be connected to this pin for PPS constant current loop. |
| 22 | GND | Ground |
| 23 | VDDD | Power input: 2.7 V–5.5 V |
| 24 | VCCD | 1.8-V core voltage pin. Connect to a 1-uF capacitor. |

Figure 6. Dual Port USB-PD Head Unit Application Diagram Using CYPD3195-24LDSX (Power and Data Connectivity)



Note
DC-DC Converter's output voltage must be controlled by connecting its FB node to CCG3PA's FB node (pin 20). This is required to meet the stringent compliance requirement of the latest PD3.0 standard.

Table 4. Pin Descriptions Specific to Application Diagram in Figure 6

| 24-Pin QFN | Pin Name | Description |
|------------|----------------------|---|
| 1 | P1.0 | VIN Monitoring GPIO |
| 2 | P1.1 | Free |
| 3 | VBUS_P_CTRL | Provider (PMOS) FET control (30-V tolerant) |
| 4 | VBUS_C_CTRL | Enable DC-DC regulator. This is an optional connection; leave this pin floating if the DC-DC converter is always enabled. |
| 5 | DP1/P1.2 | Enables CC1 VCONN FET |
| 6 | DM1/P1.3 | Enables CC2 VCONN FET |
| 7 | P0.0/SWD_DAT_0 | Master: I2C Slave SDA for communicating with the USB 2.0 Hub Slave: I2C Slave SDA for Load Sharing and for communicating with the USB 2.0 Hub Connect to the host programmer's SWDIO (data) for programming the CCG3PA device |
| 8 | P0.1/SWD_CLK_0 | Master: I2C Slave SCL for communicating with the USB 2.0 Hub Slave: I2C Slave SCL for Load Sharing and for communicating with the USB 2.0 Hub Connect to the host programmer's SWDCLK (clock) for programming the CCG3PA |
| 9 | P2.0/AXRES | Interrupt from Slave CCG3PA to Master CCG3PA |
| 10 | P2.1 | Free |
| 11 | VBUS_C_MON_DISCHARGE | Type-C VBUS Monitor with Internal Discharge FET |
| 12 | P2.2/SWD_DAT_1 | Master: I2C Master data for DC/DC regulator and for communicating with CCG3PA Slave for Load Sharing Slave: I2C Master data for DC/DC regulator |
| 13 | P2.3/SWD_CLK_1 | Master: I2C Master clock for DC/DC regulator and for communicating with CCG3PA Slave for Load Sharing Slave: I2C Master clock for DC/DC regulator |
| 14 | CC2 | Communication Channel 2 or VCONN |
| 15 | CC1 | Communication Channel 1 or VCONN |
| 16 | DM0/P3.1 | Thermistor 1 |
| 17 | DP0/P3.0 | Thermistor 2 |
| 18 | VBUS_IN_DISCHARGE | VBUS power IN (3.0 V–24.5 V) with internal discharge FET |
| 19 | CSP | CS+: Current sense input |
| 20 | FB | Voltage regulation feedback pin. Must be connected to the feedback node of DC-DC Converter. The pull-up resistor of the resistor divider network must be 200K; the pull-down resistor must be selected such that default VBUS upon power up is 5 V. |
| 21 | COMP | Compensation capacitor must be connected to this pin for PPS constant current loop. |
| 22 | GND | Ground |
| 23 | VDDD | Power input: 2.7 V–5.5 V |
| 24 | VCCD | 1.8-V core voltage pin. Connect to a 1-uF capacitor. |

Figure 7. Dual Port (Type-C and Type-A) USB-PD Car Charger Application Diagram Using CYPD3196-24LDXS

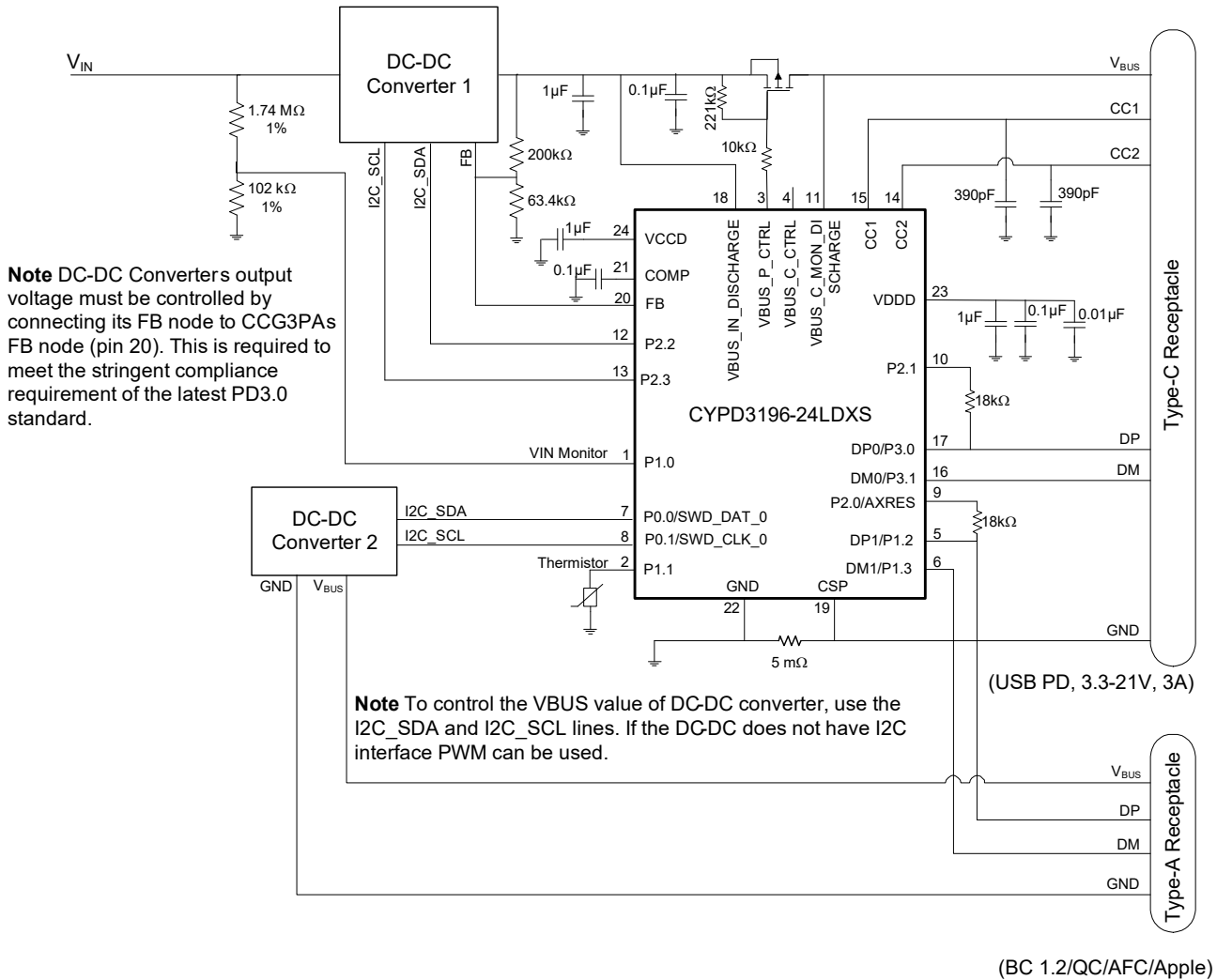


Table 5. Pin Descriptions Specific to Application Diagram in Figure 7

| 24-Pin QFN | Pin Name | Description |
|------------|----------------------|---|
| 1 | P1.0 | VIN monitoring GPIO |
| 2 | P1.1 | Thermistor |
| 3 | VBUS_P_CTRL | Provider (PMOS) FET control (30-V tolerant) |
| 4 | VBUS_C_CTRL | Enable DC-DC regulator. This is an optional connection; leave this pin floating if the DC-DC converter is always enabled. |
| 5 | DP1/P1.2 | USB D+ of Type-A port. Supports BC 1.2, QC, Apple Charging and AFC. |
| 6 | DM1/P1.3 | USB D- of Type-A port. Supports BC 1.2, QC, Apple Charging and AFC. |
| 7 | P0.0/SWD_DAT_0 | I2C Master SDA for controlling the DC/DC Converter for Type-A port |
| 8 | P0.1/SWD_CLK_0 | I2C Master SCL for controlling the DC/DC Converter for Type-A port |
| 9 | P2.0/AXRES | GPIO drives 3.3-V output. Connect an 18-k resistor from this pin to DP to realize Apple charging. A 6-k resistor should be used if VDDD is 3.3 V and an 18-k resistor should be used if it is 5 V. |
| 10 | P2.1 | GPIO drives 3.3-V output. Connect an 18-k resistor from this pin to DP to realize Apple charging. A 6-k resistor should be used if VDDD is 3.3 V and an 18-k resistor should be used if it is 5 V. |
| 11 | VBUS_C_MON_DISCHARGE | Type-C VBUS Monitor with Internal Discharge FET |
| 12 | P2.2/SWD_DAT_1 | I2C Master data for DC/DC regulator |
| 13 | P2.3/SWD_CLK_1 | I2C Master clock for DC/DC regulator |
| 14 | CC2 | Communication Channel 2 |
| 15 | CC1 | Communication Channel 1 |
| 16 | DM0/P3.1 | USB D- of Type-C port. Supports BC 1.2, QC, Apple Charging and AFC. |
| 17 | DP0/P3.0 | USB D+ of Type-C port. Supports BC 1.2, QC, Apple Charging and AFC. |
| 18 | VBUS_IN_DISCHARGE | VBUS power IN (3.0 V–24.5 V) with internal discharge FET |
| 19 | CSP | CS+: Current sense input |
| 20 | FB | Voltage regulation feedback pin. Must be connected to the feedback node of DC-DC Converter. The pull-up resistor of the resistor divider network must be 200K; the pull-down resistor must be selected such that default VBUS upon power up is 5 V. |
| 21 | COMP | Compensation capacitor must be connected to this pin for PPS constant current loop. |
| 22 | GND | Ground |
| 23 | VDDD | Power input: 2.7 V–5.5 V |
| 24 | VCCD | 1.8-V core voltage pin. Connect to a 1-μF capacitor. |

Electrical Specifications

Absolute Maximum Ratings

Table 6. Absolute Maximum Ratings

| Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-----------------------------|--|-------|-----|-----------------------|-------|--|
| V _{BUS_MAX} | Max supply voltage relative to V _{SS} on VBUS_IN_DISCHARGE and VBUS_C_MON_DISCHARGE pins | – | – | 30 | V | Absolute max |
| V _{DDD_MAX} | Max supply voltage relative to V _{SS} | – | – | 6 | V | |
| V _{CC_PIN_ABS} | Max voltage on CC1, CC2 pins and port pins P2.2 and P2.3 for applicable devices | – | – | 22 ^[1] | V | |
| V _{GPIO_ABS} | GPIO voltage | –0.5 | – | V _{DDD} +0.5 | V | |
| I _{GPIO_ABS} | Maximum current per GPIO | –25 | – | 25 | mA | |
| I _{GPIO_injection} | GPIO injection current, Max for V _{IH} > V _{DDD} , and Min for V _{IL} < V _{SS} | –0.5 | – | 0.5 | mA | Absolute max, current injected per pin |
| V _{GPIO_OVT_ABS} | OVT GPIO voltage | –0.5 | – | 6 | V | Applicable to port pins P0.0 and P0.1 |
| ESD_HBM | Electrostatic discharge human body model | 2200 | – | – | V | – |
| ESD_CDM | Electrostatic discharge charged device model | 500 | – | – | V | – |
| LU | Pin current for latch-up | –100 | – | 100 | mA | – |
| ESD_IEC_CON | Electrostatic discharge IEC61000-4-2 | 8000 | – | – | V | Contact discharge on CC1, CC2, VBUS, P2.2, and P2.3 pins |
| ESD_IEC_AIR | Electrostatic discharge IEC61000-4-2 | 15000 | – | – | V | Air discharge for DPLUS, DMINUS, CC1, CC2, VBUS, P2.2, and P2.3 pins |

Note

1. As per USB PD specification, maximum allowed VBUS = 21.5 V.

Device-Level Specifications

All specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 105\text{ }^{\circ}\text{C}$ and $T_J \leq 120\text{ }^{\circ}\text{C}$, except where noted.

Table 7. DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---|------------------------------|---|-----|-----|------|-------|---|
| SID.PWR#2 | V _{DDD} | Power Supply Input Voltage | 2.7 | – | 5.5 | V | Sink mode, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 105\text{ }^{\circ}\text{C}$. |
| SID.PWR#2_A | V _{DDD} | Power Supply Input Voltage | 3.0 | – | 5.5 | V | Source mode, $-40\text{ }^{\circ}\text{C} \leq T_A \leq 105\text{ }^{\circ}\text{C}$. |
| SID.PWR#3 | V _{BUS_IN} | Power Supply Input Voltage | 3.0 | – | 24.5 | V | $-40\text{ }^{\circ}\text{C} \leq T_A \leq 105\text{ }^{\circ}\text{C}$. |
| SID.PWR#5 | V _{CCD} | Output Voltage for core Logic | – | 1.8 | – | V | – |
| SID.PWR#13 | C _{exc} | Power supply decoupling capacitor for V _{DDD} | 0.8 | 1 | – | μF | X5R ceramic or better |
| SID.PWR#14 | C _{exv} | Power supply decoupling capacitor for V _{BUS_IN_DISH-CHARGE} | – | 0.1 | – | μF | X5R ceramic or better |
| Active Mode. Typical values measured at V_{DDD} = 5.0V or V_{BUS} = 5.0 V and T_A = 25 °C. | | | | | | | |
| SID.PWR#8 | I _{DD_A} | Supply current from V _{BUS} or V _{DDD} | – | 10 | – | mA | V _{DDD} = 5 V OR V _{BUS} = 5 V, T _A = 25 °C. CC1/CC2 in Tx or Rx, no I/O sourcing current, 2 SCBs at 1 Mbps, EA/ADC/CSA/UVOV ON, CPU at 24 MHz. |
| Sleep Mode. Typical values measured at V_{DD} = 3.3 V and T_A = 25 °C. | | | | | | | |
| SID25A | I _{DD_S} | CC, I ² C, WDT wakeup on. IMO at 24 MHz. | – | 3 | – | mA | V _{DDD} = 3.3 V, T _A = 25 °C, All blocks except CPU are on, CC IO on, EA/ADC/CSA/UVOV On. |
| Deep Sleep Mode. Typical values measured at T_A = 25 °C. | | | | | | | |
| SID_PA_DS_UA | I _{DD_PA_DS_UA} | V _{BUS} = 4.5 to 5.5 V. CC Attach, I ² C, WDT Wakeup on | – | 100 | – | μA | Power Adapter/Charger application Power Source = V _{BUS} = 5 V, T _A = 25 °C, Type-C Not Attached. CC Attach, I ² C and WDT enabled for Wakeup. |
| SID_PA_DS_A | I _{DD_PA_DS_A} | V _{BUS} = 3.0 to 24.5 V. CC, I ² C, WDT Wakeup on | – | 500 | – | μA | Power Adapter/Charger application V _{BUS} = 24.5 V, T _A = 25 °C, Part is in deep sleep. Attached, CC I/O on, ADC/CSA/UVOV On |
| SID_PB_DS_UA | I _{DD_PB_DS_UA} | V _{DDD} = 3.0 to 5.5 V. CC Attach, I ² C, WDT Wakeup on | – | 100 | – | μA | Power Bank application Power Source = V _{DDD} = 5 V, T _A = 25 °C, Type-C Not Attached. CC Attach, I ² C and WDT enabled for Wakeup. |
| SID_P-B_DS_A_SRC | I _{DD_P-B_DS_A_SRC} | V _{DDD} = 3.0 to 5.5 V. CC, I ² C, WDT Wakeup on | – | 500 | – | μA | Power Bank Source application V _{DDD} = 5 V, T _A = 25 °C, Part is in deep sleep. Attached, CC I/O on, ADC/CSA/UVOV On. |
| SID_P-B_DS_A_SNK | I _{DD_P-B_DS_A_SNK} | V _{BUS} 4.0 to 24.5 V. CC, I ² C, WDT Wakeup on | – | 500 | – | μA | Power Bank Sink application V _{BUS} = 24.5 V, T _A = 25 °C, Part is in deep sleep. Attached, CC I/O on, ADC/CSA/UVOV On |

Table 8. AC Specifications (Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-------------|------------------------|---|-----|-----|-----|-------|----------------------|
| SID.CLK#4 | F _{CPU} | CPU input frequency | DC | – | 48 | MHz | All V _{DDD} |
| SID.PWR#17 | T _{SLEEP} | Wakeup from sleep mode | – | 0 | – | μs | – |
| SID.PWR#18 | T _{DEEPSLEEP} | Wakeup from Deep Sleep mode | – | – | 35 | μs | – |
| SYS.FES#1 | T _{PWR_RDY} | Power-up to “Ready to accept I ² C/CC command” | – | 5 | 25 | ms | – |
| SID.PWR#18A | T _{POR_HIZ_T} | Power-on I/O Initialization Time | – | 3 | – | ms | – |

I/O

Table 9. I/O DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-------------|--------------------------|---|-------------------------|-----|------------------------|-------|--|
| SID.GIO#37 | V _{IH_CMOS} | Input voltage HIGH threshold | 0.7 × V _{DDD} | – | – | V | CMOS input |
| SID.GIO#38 | V _{IL_CMOS} | Input voltage LOW threshold | – | – | 0.3 × V _{DDD} | V | CMOS input |
| SID.GIO#39 | V _{IH_VDDD2.7-} | LVTTL input, V _{DDD} < 2.7 V | 0.7 × V _{DDD} | – | – | V | – |
| SID.GIO#40 | V _{IL_VDDD2.7-} | LVTTL input, V _{DDD} < 2.7 V | – | – | 0.3 × V _{DDD} | V | – |
| SID.GIO#41 | V _{IH_VDDD2.7+} | LVTTL input, V _{DDD} ≥ 2.7 V | 2.0 | – | – | V | – |
| SID.GIO#42 | V _{IL_VDDD2.7+} | LVTTL input, V _{DDD} ≥ 2.7 V | – | – | 0.8 | V | – |
| SID.GIO#33 | V _{OH_3V} | Output voltage HIGH level | V _{DDD} – 0.6 | – | – | V | I _{OH} = 4 mA at 3-V V _{DDD} |
| SID.GIO#36 | V _{OL_3V} | Output voltage LOW level | – | – | 0.6 | V | I _{OL} = 10 mA at 3-V V _{DDD} |
| SID.GIO#5 | R _{PU} | Pull-up resistor value | 3.5 | 5.6 | 8.5 | kΩ | +25 °C T _A , all V _{DDD} |
| SID.GIO#6 | R _{PD} | Pull-down resistor value | 3.5 | 5.6 | 8.5 | kΩ | +25 °C T _A , all V _{DDD} |
| SID.GIO#16 | I _{IL} | Input leakage current (absolute value) | – | – | 2 | nA | +25 °C T _A , 3-V V _{DDD} |
| SID.GIO#17 | C _{PIN_A} | Max pin capacitance | – | – | 22 | pF | Capacitance on DP0, DM0, DP1, DM1, SBU1, SBU2 pins. Guaranteed by characterization. |
| SID.GIO#17A | C _{PIN} | Max pin capacitance | – | 3 | 7 | pF | –40°C to +85°C T _A , All V _{DDD} , all other I/Os. Guaranteed by characterization. |
| SID.GIO#43 | V _{HYSTTL} | Input hysteresis, LVTTL V _{DDD} > 2.7 V | 15 | 40 | – | mV | Guaranteed by characterization. |
| SID.GIO#44 | V _{HYS CMOS} | Input hysteresis CMOS | 0.05 × V _{DDD} | – | – | mV | V _{DDD} < 4.5 V. Guaranteed by characterization. |
| SID69 | I _{DIODE} | Current through protection diode to V _{DDD} /V _{SS} | – | – | 100 | μA | Guaranteed by design. |
| SID.GIO#45 | I _{TOT_GPIO} | Maximum total sink chip current | – | – | 85 | mA | Guaranteed by design. |
| OVT | | | | | | | |
| SID.GIO#46 | I _{IHS} | Input current when Pad > V _{DDD} for OVT inputs | – | – | 10.00 | μA | Per I ² C specification |

Table 10. I/O AC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|--------------------|-------------------------------|-----|-----|-----|-------|--|
| SID70 | T _{RISEF} | Rise time in Fast Strong mode | 2 | – | 12 | ns | 3.3-V V _{DDD} , C _{load} = 25 pF |
| SID71 | T _{FALLF} | Fall time in Fast Strong mode | 2 | – | 12 | ns | 3.3-V V _{DDD} , C _{load} = 25 pF |

Table 11. GPIO_20VT DC Specifications (Applicable to port pins P2.2 and P2.3 only)

(Guaranteed by Characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|------------------|---------------------|---|------|-----|-----|-------|--|
| SID.GPIO_20VT#4 | GPIO_20VT_I_LU | GPIO_20VT Latch up current limits | –140 | – | 140 | mA | Max / min current in to any input or output, pin-to-pin, pin-to-supply |
| SID.GPIO_20VT#5 | GPIO_20VT_RPU | GPIO_20VT Pull-up resistor value | 1 | – | 25 | kΩ | +25 °C T _A , 1.4 V to GPIO_20VT_Voh(min) |
| SID.GPIO_20VT#6 | GPIO_20VT_RPD | GPIO_20VT Pull-down resistor value | 2.5 | – | 20 | kΩ | +25 °C T _A , 1.4-V to V _{DDD} |
| SID.GPIO_20VT#16 | GPIO_20VT_IIL | GPIO_20VT Input leakage current (absolute value) | – | – | 2 | nA | +25 °C T _A , 3-V V _{DDD} |
| SID.GPIO_20VT#17 | GPIO_20VT_CPIN | GPIO_20VT pin capacitance | 15 | – | 25 | pF | –40 °C to +85 °C T _A , All V _{DDD} , F = 1 MHz |
| SID.GPIO_20VT#33 | GPIO_20VT_Voh | GPIO_20VT Output Voltage high level. | 2 | – | – | V | I _{OH} = –0.5 mA |
| SID.GPIO_20VT#36 | GPIO_20VT_Vol | GPIO_20VT Output Voltage low level. | – | – | 0.4 | V | I _{OL} = 2 mA |
| SID.GPIO_20VT#41 | GPIO_20VT_Vih_LVTTL | GPIO_20VT LVTTTL Input Voltage high level. | 2 | – | – | V | V _{DDD} ≥ 2.7 V |
| SID.GPIO_20VT#42 | GPIO_20VT_Vil_LVTTL | GPIO_20VT LVTTTL Input Voltage low level. | – | – | 0.8 | V | V _{DDD} ≥ 2.7 V |
| SID.GPIO_20VT#43 | GPIO_20VT_Vhysttl | GPIO_20VT Input hysteresis LVTTTL | 15 | 40 | – | mV | V _{DDD} ≥ 2.7 V |
| SID.GPIO_20VT#69 | GPIO_20VT_IDIODE | GPIO_20VT Current through protection diode to V _{DDD} /V _{SS} | – | – | 100 | μA | – |

Table 12. GPIO_20VT AC Specifications (Applicable to port pins P2.2 and P2.3 only)

(Guaranteed by Characterization)

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|------------------|------------------|---|-----|-----|-----|-------|--|
| SID.GPIO_20VT#70 | GPIO_20VT_TriseF | GPIO_20VT Rise time in Fast Strong Mode | 1 | – | 45 | ns | All V _{DDD} , C _{load} = 25 pF |
| SID.GPIO_20VT#71 | GPIO_20VT_TfallF | GPIO_20VT Fall time in Fast Strong Mode | 2 | – | 15 | ns | All V _{DDD} , C _{load} = 25 pF |

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Pulse Width Modulation (PWM) for GPIO Pins

Table 13. PWM AC Specifications (Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|--------------|-----------------------|------------------------------|------------------|-----|----------------|-------|---|
| SID.TCPWM.3 | T _{CPWMFREQ} | Operating frequency | – | – | F _c | MHz | F _c max = CLK_SYS. Maximum = 48 MHz. |
| SID.TCPWM.4 | T _{PWMENEXT} | Input trigger pulse width | 2/F _c | – | – | ns | For all trigger events |
| SID.TCPWM.5 | T _{PWMEXT} | Output trigger pulse width | 2/F _c | – | – | ns | Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs |
| SID.TCPWM.5A | T _{CRES} | Resolution of counter | 1/F _c | – | – | ns | Minimum time between successive counts |
| SID.TCPWM.5B | PWM _{RES} | PWM resolution | 1/F _c | – | – | ns | Minimum pulse width of PWM output |
| SID.TCPWM.5C | Q _{RES} | Quadrature inputs resolution | 1/F _c | – | – | ns | Minimum pulse width between quadrature-phase inputs |

I²C

Table 14. Fixed I²C DC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|---|-----|-----|-----|-------|--------------------|
| SID149 | I _{I2C1} | Block current consumption at 100 kHz | – | – | 100 | μA | – |
| SID150 | I _{I2C2} | Block current consumption at 400 kHz | – | – | 135 | μA | – |
| SID151 | I _{I2C3} | Block current consumption at 1 Mbps | – | – | 310 | μA | – |
| SID152 | I _{I2C4} | I ² C enabled in Deep Sleep mode | – | – | 1.4 | μA | – |

Table 15. Fixed I²C AC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|-------------|-----|-----|-----|-------|--------------------|
| SID153 | F _{I2C1} | Bit rate | – | – | 1 | Mbps | – |

Table 16. Fixed UART DC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|--------------------|---|-----|-----|-----|-------|--------------------|
| SID160 | I _{UART1} | Block current consumption at 100 kbps | – | – | 20 | μA | – |
| SID161 | I _{UART2} | Block current consumption at 1000 kbps | – | – | 312 | μA | – |

Table 17. Fixed UART AC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|-------------|-----|-----|-----|-------|--------------------|
| SID162 | F _{UART} | Bit rate | – | – | 1 | Mbps | – |

Table 18. Fixed SPI DC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|-------------------------------------|-----|-----|-----|-------|--------------------|
| SID163 | I _{SPI1} | Block current consumption at 1 Mb/s | – | – | 360 | μA | – |
| SID164 | I _{SPI2} | Block current consumption at 4 Mb/s | – | – | 560 | μA | – |
| SID165 | I _{SPI3} | Block current consumption at 8 Mb/s | – | – | 600 | μA | – |

Table 19. Fixed SPI AC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|------------------|---|-----|-----|-----|-------|--------------------|
| SID166 | F _{SPI} | SPI Operating frequency (Master; 6X oversampling) | – | – | 8 | MHz | – |

Table 20. Fixed SPI Master Mode AC Specifications (Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|------------------|---------------------------------------|-----|-----|-----|-------|----------------------------------|
| SID167 | T _{DMO} | MOSI Valid after SClk driving edge | – | – | 15 | ns | – |
| SID168 | T _{DSI} | MISO Valid before SClk capturing edge | 20 | – | – | ns | Full clock, late MISO sampling |
| SID169 | T _{HMO} | Previous MOSI data hold time | 0 | – | – | ns | Referred to slave capturing edge |

Table 21. Fixed SPI Slave Mode AC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|----------------------|---|-----|-----|---------------------------|-------|---------------------------------------|
| SID170 | T _{DMI} | MOSI Valid before Sclck capturing edge | 40 | – | – | ns | – |
| SID171 | T _{DSO} | MISO Valid after Sclck driving edge | – | – | 42 + 3 × T _{CPU} | ns | T _{CPU} = 1/F _{CPU} |
| SID171A | T _{DSO_EXT} | MISO Valid after Sclck driving edge in Ext Clk mode | – | – | 48 | ns | – |
| SID172 | T _{HSO} | Previous MISO data hold time | 0 | – | – | ns | – |
| SID172A | T _{SSELSCK} | SSEL Valid to first SCK Valid edge | 100 | – | – | ns | – |

System Resources
Power-on-Reset (POR) with Brown Out SWD Interface
Table 22. Imprecise Power On Reset (PRES) (Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-----------------------|--|------|-----|------|-------|--------------------|
| SID185 | V _{RISEIPOR} | Power-on Reset (POR) rising trip voltage | 0.80 | – | 1.50 | V | – |
| SID186 | V _{FALLIPOR} | POR falling trip voltage | 0.70 | – | 1.4 | V | – |

Table 23. Precise Power On Reset (POR)

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|------------------------|---|------|-----|------|-------|--------------------|
| SID190 | V _{FALLPPOR} | Brown-out Detect (BOD) trip voltage in active/sleep modes | 1.48 | – | 1.62 | V | – |
| SID192 | V _{FALLDPSLP} | BOD trip voltage in Deep Sleep mode | 1.1 | – | 1.5 | V | – |

Table 24. SWD Interface Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-----------|--------------|-------------------------------|-----------------|-----|-----------------|-------|---------------------------------------|
| SID.SWD#1 | F_SWDCLK1 | $3.3V \leq V_{DDD} \leq 5.5V$ | – | – | 14 | MHz | SWDCLK \leq 1/3 CPU clock frequency |
| SID.SWD#2 | F_SWDCLK2 | $2.7V \leq V_{DDD} \leq 3.3V$ | – | – | 7 | MHz | SWDCLK \leq 1/3 CPU clock frequency |
| SID.SWD#3 | T_SWDI_SETUP | $T = 1/f$ SWDCLK | $0.25 \times T$ | – | – | ns | – |
| SID.SWD#4 | T_SWDI_HOLD | $T = 1/f$ SWDCLK | $0.25 \times T$ | – | – | ns | – |
| SID.SWD#5 | T_SWDO_VALID | $T = 1/f$ SWDCLK | – | – | $0.50 \times T$ | ns | – |
| SID.SWD#6 | T_SWDO_HOLD | $T = 1/f$ SWDCLK | 1 | – | – | ns | – |

Internal Main Oscillator
Table 25. IMO DC Specifications

(Guaranteed by Design)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|-------------------|---------------------------------|-----|-----|------|-------|--------------------|
| SID218 | I _{IMO1} | IMO operating current at 48 MHz | – | – | 1000 | μA | – |

Table 26. IMO AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------|-------------------------|---|-----|-----|-----|-------|---|
| SID.CLK#13 | F _{IMOTOL} | Frequency variation at 24, 36, and 48 MHz (trimmed) | – | – | ±2 | % | – |
| SID226 | T _{STARTIMO} | IMO start-up time | – | – | 7 | μs | Guaranteed by characterization. |
| SID228 | T _{JITRMSIMO2} | RMS jitter at 24 MHz | – | 145 | – | ps | Guaranteed by characterization. |
| SID.CLK#1 | F _{IMO} | IMO frequency | 24 | 36 | 48 | MHz | Only 3 frequencies supported: 24 MHz, 36 MHz, and 48 MHz. |

Internal Low-Speed Oscillator Power Down

Table 27. ILO DC Specifications

(Guaranteed by Design)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------|----------------------|-----------------------------------|-----|-----|------|-------|--------------------|
| SID231 | I _{ILO1} | I _{LO} operating current | – | 0.3 | 1.05 | μA | – |
| SID233 | I _{ILOLEAK} | I _{LO} leakage current | – | 2 | 15 | nA | – |

Table 28. ILO AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-----------|------------------------|-------------------------------|-----|-----|-----|-------|--------------------------------|
| SID234 | T _{STARTILO1} | I _{LO} start-up time | – | – | 2 | ms | Guaranteed by Characterization |
| SID238 | T _{ILODUTY} | I _{LO} duty cycle | 40 | 50 | 60 | % | Guaranteed by Characterization |
| SID.CLK#5 | F _{ILO} | I _{LO} frequency | 20 | 40 | 80 | kHz | – |

Table 29. PD DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|----------|------------------------|---|------|-----|-------|-------|--|
| SID.PD.1 | R _{p_std} | DFP CC termination for default USB Power | 64 | 80 | 96 | μA | – |
| SID.PD.2 | R _{p_1.5A} | DFP CC termination for 1.5A power | 166 | 180 | 194.4 | μA | – |
| SID.PD.3 | R _{p_3.0A} | DFP CC termination for 3.0A power | 304 | 330 | 356.4 | μA | – |
| SID.PD.4 | R _d | UFP CC termination | 4.59 | 5.1 | 5.61 | kΩ | – |
| SID.PD.5 | R _{d_DB} | UFP (Power Bank) Dead Battery CC Termination on CC1 and CC2 | 4.08 | 5.1 | 6.12 | kΩ | All supplies forced to 0V and 1.32 V applied at CC1 or CC2 |
| SID.PD.6 | V _{gndoffset} | Ground offset tolerated by BMC receiver | –500 | – | 500 | mV | Relative to the remote BMC transmitter. |

Table 30. LS-CSA Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|--------------|--------------------------|--|-------|-----|------|-------|--------------------------------|
| SID.LSCSA.1 | C _{in_inp} | CSP Input capacitance | 7 | – | 10 | pF | Guaranteed by characterization |
| SID.LSCSA.2 | C _{sa_Acc1} | CSA accuracy 5 mV < V _{sense} < 10 mV | –15 | – | 15 | % | Active Mode |
| SID.LSCSA.3 | C _{sa_Acc2} | CSA accuracy 10 mV < V _{sense} < 15 mV | –10 | – | 10 | % | |
| SID.LSCSA.4 | C _{sa_Acc3} | CSA accuracy 15 mV < V _{sense} < 20 mV | –6 | – | 6 | % | |
| SID.LSCSA.5 | C _{sa_Acc4} | CSA accuracy 20 mV < V _{sense} < 30 mV | –5 | – | 5 | % | |
| SID.LSCSA.6 | C _{sa_Acc5} | CSA accuracy 30 mV < V _{sense} < 50 mV | –4 | – | 4 | % | |
| SID.LSCSA.7 | C _{sa_Acc6} | CSA accuracy 50 mV < V _{sense} | –4 | – | 4 | % | |
| SID.LSCSA.8 | C _{sa_SCP_Acc1} | CSA SCP 80 mV | –16.5 | – | 16.5 | % | |
| SID.LSCSA.9 | C _{sa_SCP_Acc2} | CSA SCP 100 mV | –13.4 | – | 13.4 | % | |
| SID.LSCSA.10 | C _{sa_SCP_Acc3} | CSA SCP 150 mV | –9.4 | – | 9.4 | % | |
| SID.LSCSA.11 | C _{sa_SCP_Acc4} | CSA SCP 200 mV | –7.5 | – | 7.5 | % | |
| SID.LSCSA.12 | A _v | Nominal Gain values supported: 5, 10, 20, 35, 50, 75, 125, 150 | 5 | – | 150 | V/V | |
| SID.LSCSA.24 | A _{v1_E_Trim} | Gain Error | –3 | – | 3 | % | Guaranteed by characterization |

Table 30. LS-CSA Specifications (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|--------------|-----------|-------------------------|------|-----|-----|-------|--------------------------------|
| SID.LSCSA.31 | Av_E_SCP | Gain Error of SCP stage | -3.5 | - | 3.5 | % | Guaranteed by characterization |

Table 31. LS-CSA AC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|----------------|-----------------------|--|-----|-----|-----|-------|---------------------------|
| SID.LSCSA.AC.1 | T _{OCP_GPIO} | Delay from OCP threshold trip to output GPIO toggle | - | - | 20 | µs | Available on P1.0 or P1.1 |
| SID.LSCSA.AC.2 | T _{OCP_Gate} | Delay from OCP threshold trip to external PFET Power Gate Turn off | - | - | 50 | µs | - |
| SID.LSCSA.AC.3 | T _{SCP_GPIO} | Delay from SCP threshold trip to output GPIO toggle | - | - | 15 | µs | Available on P1.0 or P1.1 |
| SID.LSCSA.AC.4 | T _{SCP_Gate} | Delay from SCP threshold trip to external PFET Power Gate Turn off | - | - | 50 | µs | - |
| SID.LSCSA.AC.5 | T _{SR_GPIO} | Delay from SR threshold trip to output GPIO toggle | - | - | 20 | µs | Available on P1.0 or P1.1 |

Table 32. UV/OV Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------|--------------------|---|------|-----|-----|-------|--------------------|
| SID.UVOV.1 | V _{THOV1} | Overvoltage Threshold Accuracy, 4.0 V to 11.0 V | -3 | - | 3 | % | Active Mode |
| SID.UVOV.2 | V _{THOV2} | Overvoltage Threshold Accuracy, 11 V to 27.4 V | -3.2 | - | 3.2 | % | |
| SID.UVOV.3 | V _{THUV1} | Undervoltage Threshold Accuracy, 2.7 V to 3.3 V | -4 | - | 4 | % | |
| SID.UVOV.4 | V _{THUV2} | Undervoltage Threshold Accuracy, 3.3 V to 4.0 V | -3.5 | - | 3.5 | % | |
| SID.UVOV.5 | V _{THUV3} | Undervoltage Threshold Accuracy, 4.0 V to 11.0 V | -3 | - | 3 | % | |
| SID.UVOV.6 | V _{THUV4} | Undervoltage Threshold Accuracy, 11.0 V to 22.0 V | -2.9 | - | 2.9 | % | |

Table 33. UV/OV AC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|---------------|----------------------|---|-----|-----|-----|-------|---------------------------|
| SID.UVOV.AC.1 | T _{OV_GPIO} | Delay from UV threshold trip to output GPIO toggle | - | - | 20 | µs | Available on P1.0 or P1.1 |
| SID.UVOV.AC.2 | T _{OV_GATE} | Delay from UV threshold trip to external PFET power gate turn off | - | - | 50 | µs | - |
| SID.UVOV.AC.3 | T _{UV_GPIO} | Delay from UV threshold trip to output GPIO toggle | - | - | 20 | µs | Available on P1.0 or P1.1 |

Gate Driver Specifications
Table 34. Gate Driver DC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-----------|----------------------|--|------|-----|-------|-------|--|
| SID.GD.1 | R _{PD} | Pull-down resistance | – | – | 3 | kΩ | Applicable on VBUS_P_CTRL and VBUS_C_CTRL to turn ON external PFET. |
| SID.GD.2 | R _{PU} | Pull-up resistance | – | – | 4 | kΩ | Applicable on VBUS_P_CTRL to turn OFF external PFET |
| SID.GD.3 | I _{PD0} | Pull-down current sink at drive strength of 1 | 25 | – | 75 | μA | I-mode (current mode) pull down at 5 V. Applicable on VBUS_P_CTRL and VBUS_C_CTRL to turn ON external PFET |
| SID.GD.4 | I _{PD1} | Pull-down current sink at drive strength of 2 | 50 | – | 150 | μA | |
| SID.GD.5 | I _{PD2} | Pull-down current sink at drive strength of 4 | 140 | – | 300 | μA | |
| SID.GD.6 | I _{PD3} | Pull-down current sink at drive strength of 8 | 280 | – | 580 | μA | |
| SID.GD.7 | I _{PD4} | Pull-down current sink at drive strength of 16 | 560 | – | 1200 | μA | |
| SID.GD.8 | I _{PD5} | Pull-down current sink at drive strength of 32 | 1120 | – | 2300 | μA | |
| SID.GD.9 | I _{leak_p1} | Pin leakage on VBUS_P_CTRL | – | – | 0.003 | μA | +25 °C T _J , 5-V V _{DDD} , 20-V V _{BUS} |
| SID.GD.10 | I _{leak_c1} | Pin leakage on VBUS_C_CTRL | – | – | 0.003 | | +25 °C T _J , 5-V V _{DDD} , 20-V V _{BU} |
| SID.GD.11 | I _{leak_p2} | Pin leakage on VBUS_P_CTRL | – | – | 2 | | +85 °C T _J , 5-V V _{DDD} , 20-V V _{BU} |
| SID.GD.12 | I _{leak_c2} | Pin leakage on VBUS_C_CTRL | – | – | 2 | | +85 °C T _J , 5-V V _{DDD} , 20-V V _{BU} |
| SID.GD.13 | I _{leak_p3} | Pin leakage on VBUS_P_CTRL | – | – | 7 | | +125 °C T _J , 5-V V _{DDD} , 20-V V _{BU} |
| SID.GD.14 | I _{leak_c3} | Pin leakage on VBUS_C_CTRL | – | – | 7 | | +125 °C T _J , 5-V V _{DDD} , 20-V V _{BU} |

Table 35. Gate Driver AC Specifications

(Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-----------|--------------------------|--|-----|-----|-----|-------|---|
| SID.GD.15 | T _{PD1} | Pull down delay on VBUS_C_CTRL | – | – | 2 | μs | Clload = 2 nF, Delay to VBUS–1.5 V from initiation of falling edge, VBUS = 5 V to 20 V, 50 KΩ tied between VBUS_C_CTRL and VBUS |
| SID.GD.16 | T _{r_discharge} | Discharge rate of output node on VBUS_C_CTRL | – | – | 5 | V/μs | 80% to 20%, 50 KΩ tied between VBUS_C_CTRL and VBUS, Clload = 2 nF, Vinitial = 24 V |
| SID.GD.17 | T _{PD2} | Pull down delay on VBUS_P_CTRL | – | – | 2 | μs | Clload = 2 nF, Delay to VBUS–1.5 V from initiation of falling edge, V _{BUS} = 5 V to 20 V, 50 KΩ tied between VBUS_C_CTRL and VBUS |
| SID.GD.18 | T _{PU} | Pull up delay on VBUS_P_CTRL | – | – | 18 | μs | Clload = 2 nF, Delay to VBUS–1.5 V from initiation of falling edge, VBUS = 5 V to 20 V, 50 KΩ tied between VBUS_C_CTRL and VBUS |
| SID.GD.19 | SR _{PU} | Output slew rate on VBUS_P_CTRL | – | – | 5 | V/μs | Clload = 2 nF, 20% to 80% of VBUS_P_CTRL range |

Table 35. Gate Driver AC Specifications (continued)

(Guaranteed by Characterization) (continued)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-----------|------------------|---------------------------------|-----|-----|-----|-------|--|
| SID.GD.20 | SR _{PD} | Output slew rate on VBUS_P_CTRL | – | – | 5 | V/μs | Clload = 2 nF, 80% to 20% of VBUS_P_CTRL range |

Table 36. VBUS Discharge Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|------------------|-----------------|---|------|-----|-----|-------|---|
| SID.VBUS.DISC.6 | I1 | 20-V NMOS ON current for DS = 1 | 0.15 | – | 1 | mA | Measured at 0.5 V |
| SID.VBUS.DISC.7 | I2 | 20-V NMOS ON current for DS = 2 | 0.4 | – | 2 | mA | |
| SID.VBUS.DISC.8 | I4 | 20-V NMOS ON current for DS = 4 | 0.9 | – | 4 | mA | |
| SID.VBUS.DISC.9 | I8 | 20-V NMOS ON current for DS = 8 | 2 | – | 8 | mA | |
| SID.VBUS.DISC.10 | I16 | 20-V NMOS ON current for DS = 16 | 4 | – | 10 | mA | |
| SID.VBUS.DISC.11 | VBUS_Stop_Error | Error percentage of final V _{BUS} value from setting | – | – | 10 | % | When V _{BUS} is discharged to 5 V. Guaranteed by Characterization. |

Table 37. Voltage (VBUS) Regulation DC Specifications

| Spec ID# | Parameter | Description | Min | Typ | Max | Units | Details / Conditions |
|--------------|---------------------|-----------------------------|-------|-----|-------|-------|---|
| SID.DC.VR.1 | V_IN_3 | V(pad_in) at 3-V target | 2.85 | 3 | 3.15 | V | Active mode shunt regulator at 3 V with bandgap |
| SID.DC.VR.2 | V_IN_5 | V(pad_in) at 5-V target | 4.75 | 5 | 5.25 | V | Active mode shunt regulator at 5 V |
| SID.DC.VR.3 | V_IN_9 | V(pad_in) at 9-V target | 8.55 | 9 | 9.45 | | Active mode shunt regulator at 9 V |
| SID.DC.VR.4 | V_IN_15 | V(pad_in) at 15-V target | 14.25 | 15 | 15.75 | | Active mode shunt regulator at 15 V |
| SID.DC.VR.5 | V_IN_20 | V(pad_in) at 20-V target | 19 | 20 | 21 | | Active mode shunt regulator at 20 V |
| SID.DC.VR.6 | V_IN_3_DS | V(pad_in) at 3-V target | 2.7 | 3 | 3.3 | V | Deep Sleep mode shunt regulator at 3 V with bandgap |
| SID.DC.VR.7 | V_IN_5_DS | V(pad_in) at 5-V target | 4.5 | 5 | 5.5 | V | Deep Sleep mode shunt regulator at 5 V |
| SID.DC.VR.8 | V_IN_9_DS | V(pad_in) at 9-V target | 8.1 | 9 | 9.1 | V | Deep Sleep mode shunt regulator at 9 V |
| SID.DC.VR.9 | V_IN_15_DS | V(pad_in) at 15-V target | 13.5 | 15 | 16.5 | V | Deep Sleep mode shunt regulator at 15 V |
| SID.DC.VR.10 | V_IN_20_DS | V(pad_in) at 20-V target | 18 | 20 | 22 | V | Deep Sleep mode shunt regulator at 20 V |
| SID.DC.VR.11 | I _{KA_OFF} | Off-state cathode current | – | – | 10 | μA | – |
| SID.DC.VR.12 | I _{KA_ON} | Current through cathode pin | – | – | 10 | mA | – |

Table 38. VBUS Short Protection Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-----------|-----------------|---|-----|-----|-----|-------|---------------------------------|
| SID.VSP.1 | V_SHORT_TRIGGER | Short-to-VBUS system-side clamping voltage on the CC/P2.2/P2.3 pins | – | 9 | – | V | Guaranteed by Characterization. |

Table 39. VBUS DC Regulator Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------|-------------|-------------------------------|------|-----|------|-------|--------------------|
| SID.VREG.2 | VBUS_DETECT | VBUS detect threshold voltage | 1.08 | – | 2.62 | V | – |

Table 40. VBUS AC Regulator Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|------------|--------------------|---|-----|-----|-----|-------|---------------------------------|
| SID.VREG.3 | T _{start} | Total startup time for the regulator supply outputs | – | – | 200 | µs | Guaranteed by Characterization. |

Analog to Digital Converter

Table 41. ADC DC Specifications (Guaranteed by Characterization)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-----------|-----------------------|----------------------------|--------------------|-----|--------------------|-------|--|
| SID.ADC.1 | Resolution | ADC resolution | – | 8 | – | Bits | – |
| SID.ADC.2 | INL | Integral non-linearity | –2.5 | – | 2.5 | LSB | – |
| SID.ADC.3 | DNL | Differential non-linearity | –2.5 | – | 2.5 | LSB | – |
| SID.ADC.4 | Gain Error | Gain error | –1.5 | – | 1.5 | LSB | – |
| SID.ADC.5 | V _{REF_ADC1} | Reference voltage of ADC | V _{DDmin} | – | V _{DDmax} | V | Reference voltage generated from V _{DD} |
| SID.ADC.6 | V _{REF_ADC2} | Reference voltage of ADC | 1.96 | 2.0 | 2.04 | V | Reference voltage generated from bandgap |

Table 42. ADC AC Specifications (Guaranteed by Design)

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-----------|-----------|--|-----|-----|-----|-------|--------------------|
| SID.ADC.7 | SLEW_Max | Rate of change of sampled voltage signal | – | – | 3 | V/ms | – |

Memory

Table 43. Flash AC Specifications

| Spec ID | Parameter | Description | Min | Typ | Max | Units | Details/Conditions |
|-----------|------------------------|--|-----|-----|------|-------|---|
| SID.MEM#3 | FLASH_ERASE | Row erase time | – | – | 15.5 | ms | –40 °C ≤ T _A ≤ 85 °C, all V _{DDD} |
| SID.MEM#4 | FLASH_WRITE | Row (Block) write time (erase and program) | – | – | 20 | ms | –40 °C ≤ T _A ≤ 85 °C, all V _{DDD} |
| SID.MEM#8 | FLASH_ROW_PGM | Row program time after erase | – | – | 7 | ms | 25 °C ≤ T _A ≤ 55 °C, all V _{DDD} |
| SID178 | T _{BULKERASE} | Bulk erase time (32 KB) | – | – | 35 | ms | – |
| SID180 | T _{DEVPROG} | Total device program time | – | – | 7.5 | s | – |
| SID182 | F _{RET1} | Flash retention, T _A ≤ 55 °C, 100K P/E cycles | 20 | – | – | years | – |
| SID182A | F _{RET2} | Flash retention, T _A ≤ 85 °C, 10K P/E cycles | 10 | – | – | years | – |
| SID182B | F _{RET3} | Flash retention, T _A ≤ 105 °C, 10K P/E cycles | 3 | – | – | years | – |

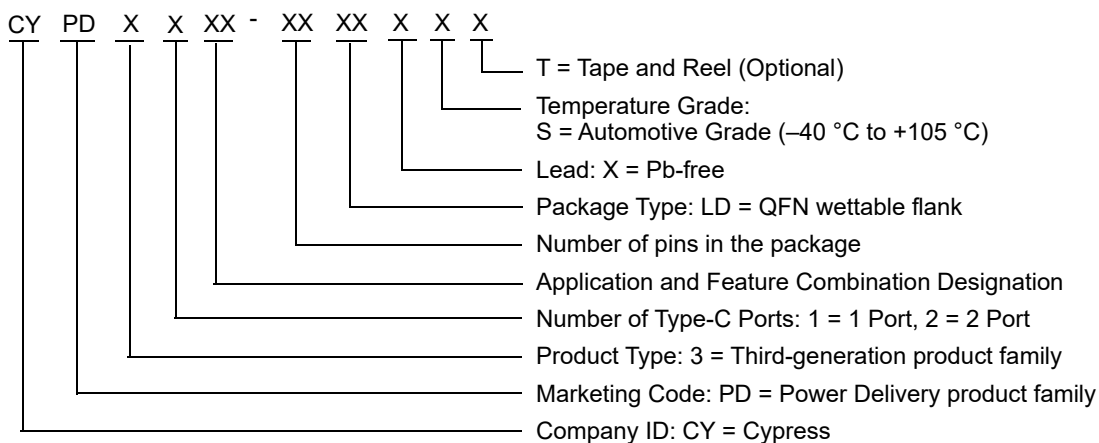
Ordering Information

Table 44 lists the CYPD319X part numbers and features.

Table 44. CYPD319X Ordering Information

| MPN | Application | Termination Resistor | Role | Preloaded Bootloader | Package Type |
|-----------------|-------------------------|----------------------|----------------------------|-----------------------------|--------------|
| CYPD3195-24LDXS | Head Units/Infotainment | R _P | DFP (Power Source Only) | I ² C Bootloader | 24-pin QFN |
| CYPD3196-24LDXS | Charge Only Ports | | | CC Bootloader | |
| CYPD3194-24LDXS | Rear Seat Entertainment | | | None | |

Ordering Code Definitions



Packaging

Table 45. Package Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|-----------------|--------------------------------|--------------------|-----|-----|-------|-------|
| T _A | Operating ambient temperature | Automotive S-Grade | -40 | 25 | 105 | °C |
| T _J | Operating junction temperature | Automotive S-Grade | -40 | 25 | 120 | °C |
| T _{JA} | Package θ_{JA} (24-QFN) | – | – | – | 19.98 | °C/W |
| T _{JC} | Package θ_{JC} (24-QFN) | – | – | – | 4.78 | °C/W |

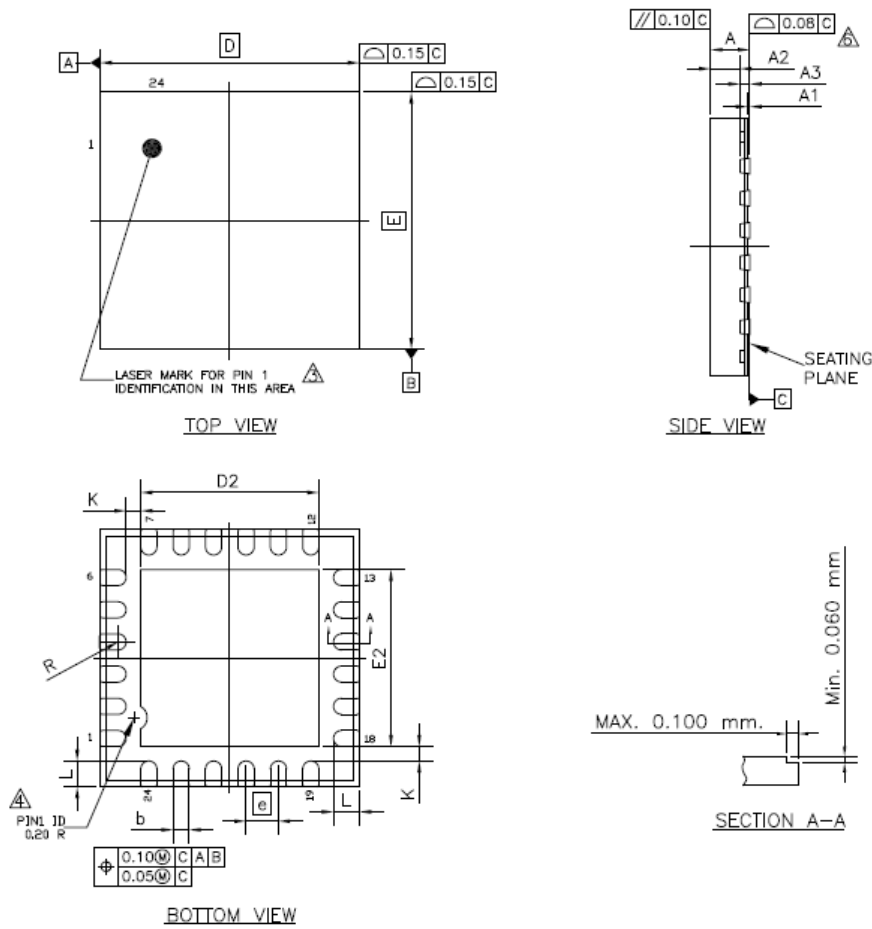
Table 46. Solder Reflow Peak Temperature

| Package | Maximum Peak Temperature | Maximum Time within 5° C of Peak Temperature |
|------------|--------------------------|--|
| 24-pin QFN | 260 °C | 30 seconds |

Table 47. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

| Package | MSL |
|------------|------|
| 24-pin QFN | MSL3 |

Figure 8. 24-pin QFN Package Outline



| SYMBOL | DIMENSIONS | | |
|--------|------------|-------|-------|
| | MIN | NOM | MAX |
| A | — | — | 0.60 |
| A1 | 0.00 | — | 0.05 |
| A2 | — | 0.400 | 0.425 |
| A3 | 0.152 REF | | |
| b | 0.18 | 0.25 | 0.30 |
| D | 4.00 BSC | | |
| E | 4.00 BSC | | |
| D2 | 2.65 | 2.75 | 2.85 |
| E2 | 2.65 | 2.75 | 2.85 |
| e | 0.50 BSC | | |
| L | 0.30 | 0.40 | 0.50 |
| K | 0.225 | — | — |
| R | 0.09 | — | — |

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
3. THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
4. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
5. PACKAGE WARPAGE MAX 0.08 mm.
6. APPLIED FOR EXPOSED PAD AND TERMINALS.
7. JEDEC SPECIFICATION NO. REF. : N/A.

002-23807 Rev **

Acronyms

Table 48. Acronyms Used in this Document

| Acronym | Description |
|--------------------------|---|
| ADC | analog-to-digital converter |
| AES | advanced encryption standard |
| API | application programming interface |
| Arm® | advanced RISC machine, a CPU architecture |
| CC | configuration channel |
| CCG3 | Cable Controller Generation 3 |
| CPU | central processing unit |
| CRC | cyclic redundancy check, an error-checking protocol |
| CS | current sense |
| DFP | downstream facing port |
| DIO | digital input/output, GPIO with only digital capabilities, no analog. See GPIO. |
| DRP | dual role port |
| EEPROM | electrically erasable programmable read-only memory |
| EMCA | electronically marked cable assembly, a USB cable that includes an IC that reports cable characteristics (such as current rating) to the Type-C ports |
| EMI | electromagnetic interference |
| ESD | electrostatic discharge |
| FS | full-speed |
| GPIO | general-purpose input/output |
| IC | integrated circuit |
| IDE | integrated development environment |
| I ² C, or IIC | Inter-Integrated Circuit, a communications protocol |
| ILO | internal low-speed oscillator, see also IMO |
| IMO | internal main oscillator, see also ILO |
| I/O | input/output, see also GPIO |
| LDO | low-dropout regulator |
| LVD | low-voltage detect |
| LVTTTL | low-voltage transistor-transistor logic |
| MCU | microcontroller unit |
| NC | no connect |
| NMI | nonmaskable interrupt |
| NVIC | nested vectored interrupt controller |
| opamp | operational amplifier |
| OCP | overcurrent protection |

Table 48. Acronyms Used in this Document (continued)

| Acronym | Description |
|---------|--|
| OTP | over temperature protection |
| OVP | overvoltage protection |
| OVT | overvoltage tolerant |
| PCB | printed circuit board |
| PD | power delivery |
| PGA | programmable gain amplifier |
| PHY | physical layer |
| POR | power-on reset |
| PRES | precise power-on reset |
| PSoC® | Programmable System-on-Chip™ |
| PWM | pulse-width modulator |
| RAM | random-access memory |
| RISC | reduced-instruction-set computing |
| RMS | root-mean-square |
| RTC | real-time clock |
| RX | receive |
| SAR | successive approximation register |
| SCL | I ² C serial clock |
| SCP | short circuit protection |
| SDA | I ² C serial data |
| S/H | sample and hold |
| SHA | secure hash algorithm |
| SPI | Serial Peripheral Interface, a communications protocol |
| SRAM | static random access memory |
| SWD | serial wire debug, a test protocol |
| TX | transmit |
| Type-C | a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power |
| UART | Universal Asynchronous Transmitter Receiver, a communications protocol |
| USB | Universal Serial Bus |
| USBIO | USB input/output, CCG2 pins used to connect to a USB port |
| UVP | undervoltage protection |
| XRES | external reset I/O pin |

Document Conventions

Units of Measure

Table 49. Units of Measure

| Symbol | Unit of Measure |
|--------|-------------------------|
| °C | degrees Celsius |
| Hz | hertz |
| KB | 1024 bytes |
| kHz | kilohertz |
| kΩ | kilo ohm |
| Mbps | megabits per second |
| MHz | megahertz |
| MΩ | mega-ohm |
| Msps | mega samples per second |
| μA | microampere |
| μF | microfarad |
| μs | microsecond |
| μV | microvolt |
| μW | microwatt |
| mA | milliampere |
| ms | millisecond |
| mV | millivolt |
| nA | nanoampere |
| ns | nanosecond |
| Ω | ohm |
| pF | picofarad |
| ppm | parts per million |
| ps | picosecond |
| s | second |
| sps | samples per second |
| V | volt |

Document History Page

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|--|---------|-----------------|--|
| Revision | ECN | Submission Date | Description of Change |
| ** | 6245648 | 11/09/2018 | New data sheet. |
| *A | 6653121 | 08/13/2019 | Changed status from Advance to Final. Updated Application Diagrams : Updated Figure 5 , Figure 6 , and Figure 7 . Updated Electrical Specifications : Updated Device-Level Specifications : Added Table 7 through Table 12 . Added Digital Peripherals . Added System Resources . |
| *B | 6739962 | 12/10/2019 | Added " CONFIDENTIAL - RELEASED ONLY UNDER NONDISCLOSURE AGREEMENT (NDA) " across the document. Updated Ordering Information : Updated part numbers. Updated to new template. |
| *C | 6878026 | 06/15/2020 | Updated Application Firmware Update over CC Interface section. Added reference to KBA230192 . Updated Ordering Information . Updated Sales, Solutions, and Legal Information . |