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EZ-PD™ CCG6

USB Type-C Port Controller

General Description

EZ-PD™ CCG6 is a one-port USB Type-C controller that complies with the latest USB Type-C and PD specifications. CCG6 provides a complete USB Type-C and USB-Power Delivery port control solution for PCs and notebooks. CCG6 includes a VBUS provider path load switch controller, True Random Number Generator for authentication, a 32-bit, 48-MHz Arm® Cortex®-M0 processor with 128-KB flash integrates a complete Type-C Transceiver including the Type-C termination resistors Rp, Rd, and dead battery Rd termination. CCG6 is available in a 40-pin QFN package.

Applications

- PCs and Notebooks
- Thunderbolt hosts, non-Thunderbolt hosts and devices/docks

Features

USB-PD

- Supports latest USB PD 3.0 specification
- Fast Role Swap (FRS)
- Extended Data Messaging

Type-C

- Integrated current sources for DFP[1] role (Rp).
  - Default current at 500 / 900 mA
  - 1.5 A
  - 3 A
- Integrated Rd resistor for UFP[2] role
- Integrated VCONN FETs to power EMCA cables
- Integrated dead battery termination
- Integrated high-voltage protection on CC and SBU pins to protect against accidental shorts to the VBUS pin on the Type-C connector

Legacy Charging (source and sink)

- BCv1.2
- Apple

Mux

- Integrated USB2.0 Analog Mux for USB 2.0 HS data and UART data
- Integrated SBU analog Mux for alternate modes (Display port and Thunderbolt)

Integrated VBUS Load Switch Controller

- Supports up to 20 V on VBUS Provider path
- Slew rate controlled Gate Driver, tolerant to 24 V, to drive external VBUS PFET on the provider path
- Gate Driver, tolerant to 24 V, to drive external VBUS PFET on the consumer path
- Configurable hardware-controlled VBUS overvoltage, undervoltage, overcurrent, short circuit, and reverse current protection
- VBUS high-side current sense amplifier capable of measuring current across 5-mΩ series resistance
- In response to Fast Role Swap request, turns off consumer PFET and turns on provider PFET

LDO

- Integrated high-voltage LDO operational up to 21.5 V for dead battery mode operation

32-bit MCU Subsystem

- 48-MHz Arm Cortex-M0 CPU
- 128-KB Flash
- 12-KB SRAM

Integrated Digital Blocks

- Two integrated timers and counters to meet response times required by the USB-PD protocol
- Four run-time serial communication blocks (SCBs) with reconfigurable I^2C, SPI, or UART functionality

Authentication

- True Random Number Generator

Clocks and Oscillators

- Integrated oscillator eliminating the need for an external clock

Operating Range

- VSYS (2.75 V–5.5 V)
- VBUS (4 V–21.5 V)

Hot-Swappable I/Os

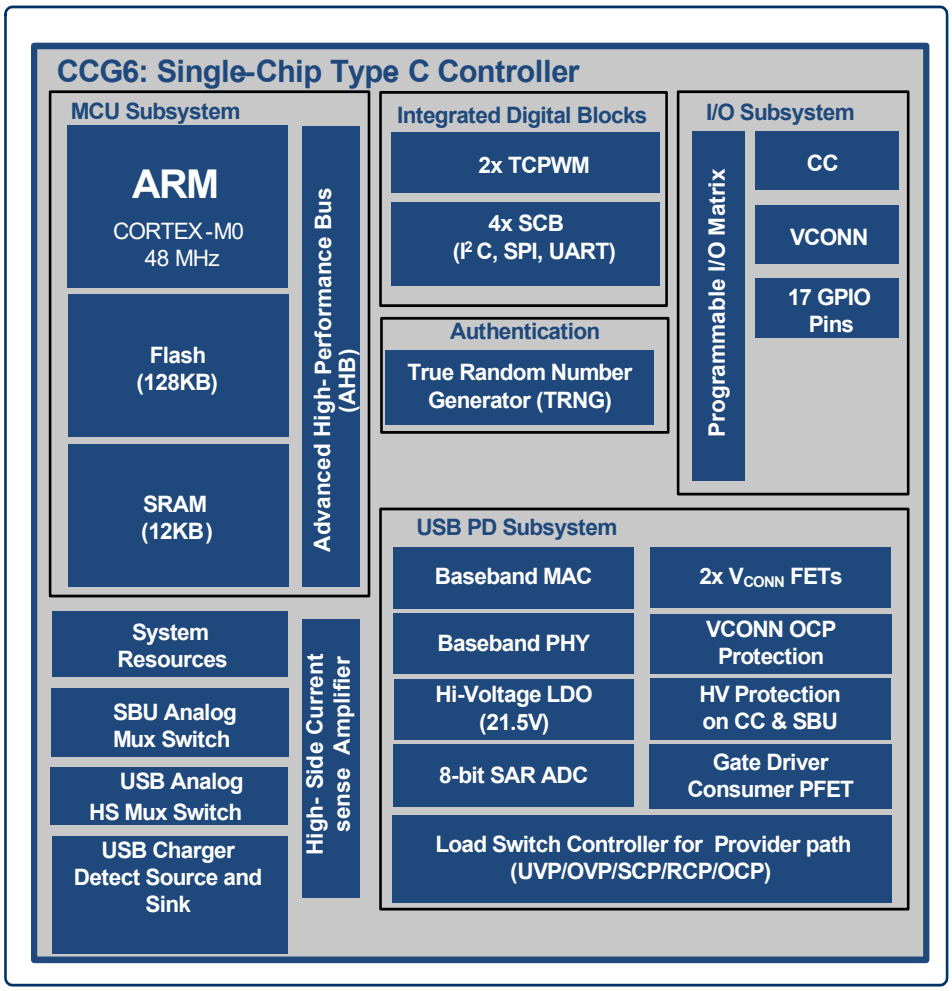
- I^2C pins from SCB1 are hot-swappable

Packages

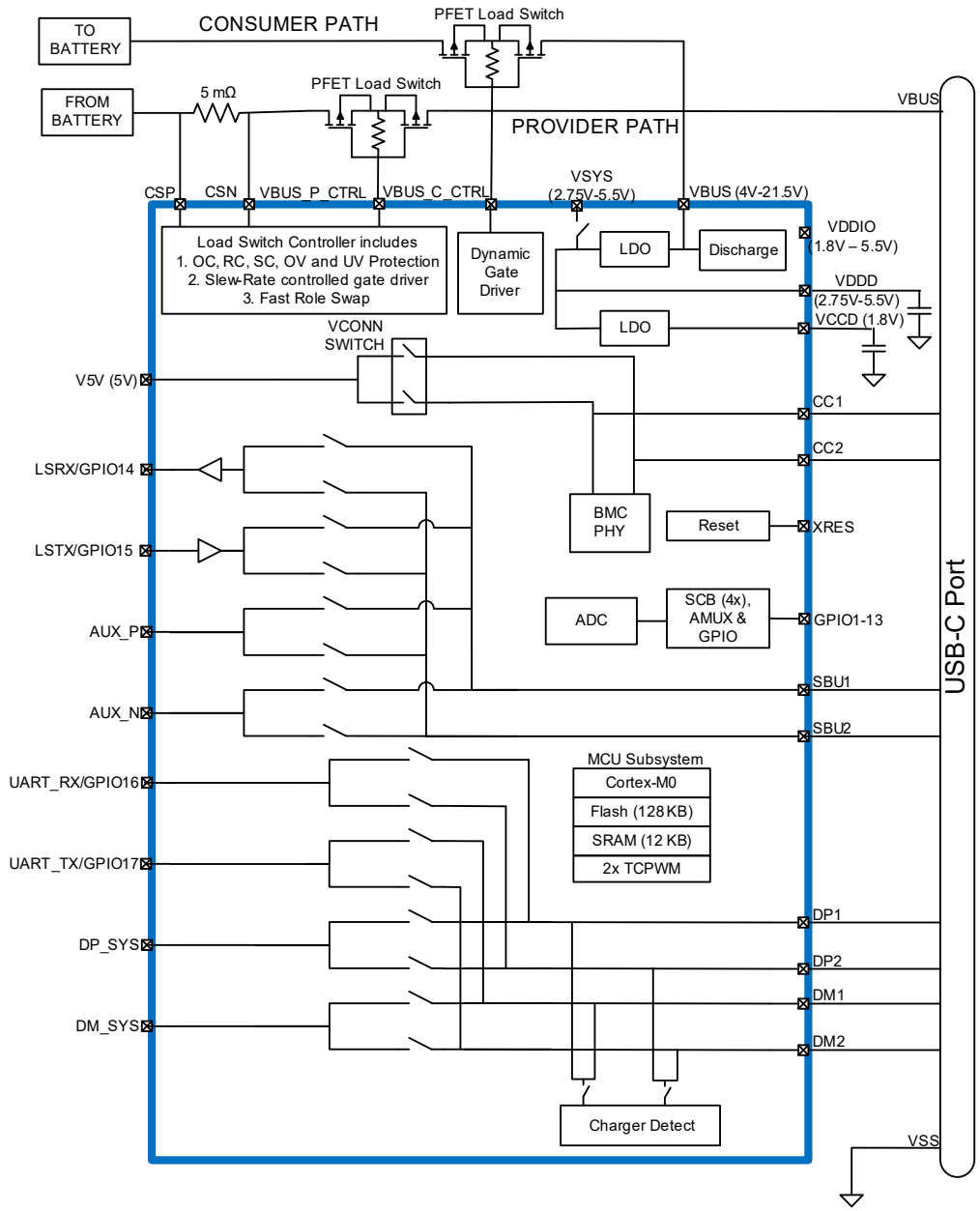
- 6.0 mm × 6.0 mm, 0.6 mm, 40-pin QFN
- Supports industrial temperature range (–40 °C to +85 °C)

Notes
1. DFP refers to power source.
2. UFP refers to power sink.

Logic Block Diagram



CCG6 Functional Diagram



Contents

Functional Overview

USB-PD Subsystem (SS)

USB-PD Physical Layer

The CCG6 USB-PD subsystem, as shown in Figure 1, consists of the USB-PD physical layer (PHY) block and supporting circuits. The PHY consists of a transmitter and receiver that communicates using BMC and 4b/5b encoded/decoded data over the CC channel based on the PD 3.0 specification. All communication is half-duplex. The PHY practices collision avoidance to minimize communication errors on the channel.

In addition, the CCG6 USB-PD block includes all termination resistors (Rp and Rd) and their switches as required by the USB Type-C specification. Rp and Rd resistors are required for connection detection, plug orientation detection, and for establishing the USB source/sink roles.

The integrated Rp resistor enables CCG6 to be configured as a Source. The Rp resistor is implemented as a current source and can be programmed to support the complete range of current capacity on the VBUS defined in the USB Type-C Spec.

The Rd resistor is used to identify CCG6 as a Sink in a DRP application. The dead battery Rd resistor on CC pins is required when the part is not powered for dead battery termination detection and charging.

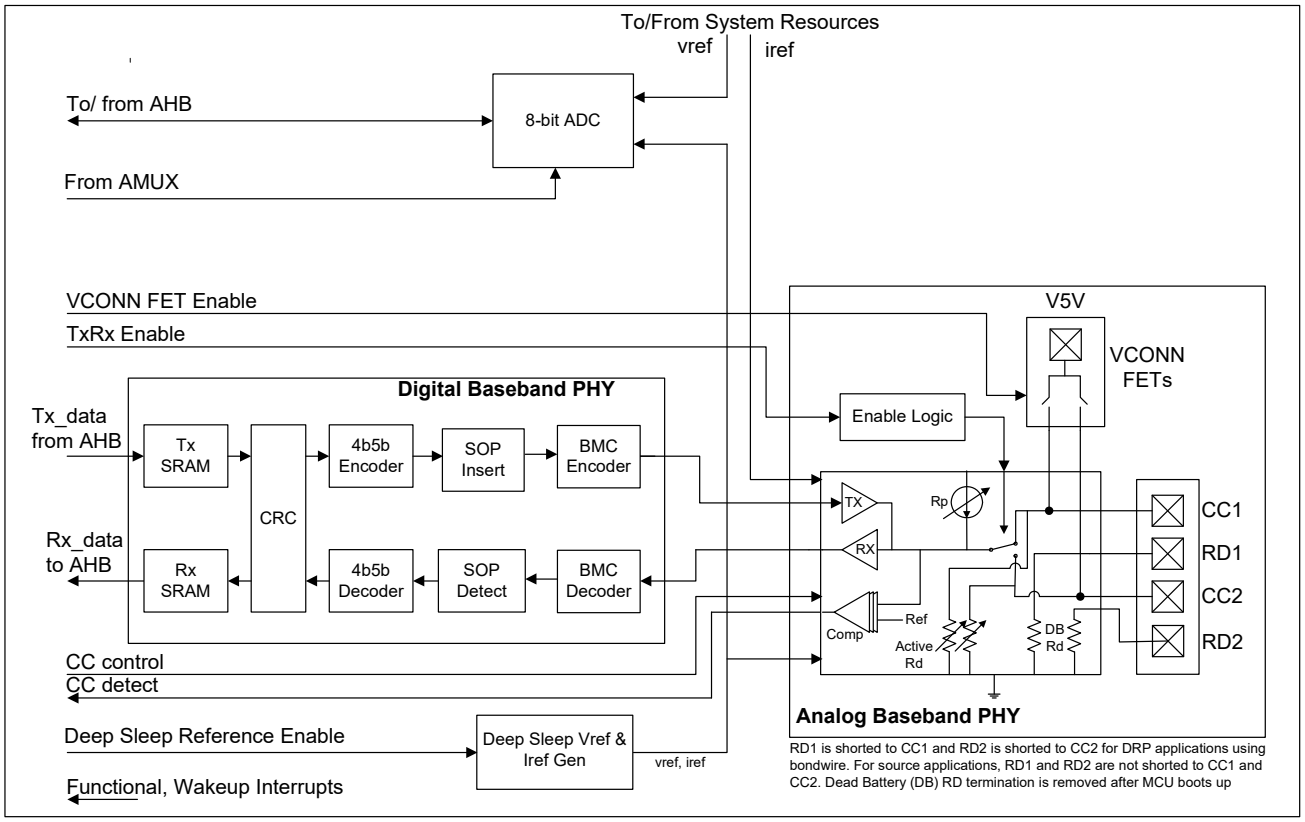
To support the latest USB-PD 3.0 specification, CCG6 includes Fast Role Swap (FRS). The FRS feature enables externally powered docks and hubs to rapidly switch to bus power when their external power supply is removed. CCG6 also supports FRS detection in DeepSleep mode.

For more details about FRS, refer to Section 6.3.17 in the USB-PD 3.0 specification.

CCG6 is designed to be fully interoperable with revision 3.0 of the USB Power Delivery specification as well as revision 2.0 of the USB Power Delivery specification.

CCG6 supports Extended Messages containing data of up to 260 bytes. The Extended Messages will be larger than expected by the USB-PD 2.0 hardware. To accommodate Revision 2.0 based systems, a Chunking mechanism is implemented such that messages are limited to Revision 2.0 sizes unless it is discovered that both systems support longer message lengths.

Figure 1. USB-PD Subsystem



VCONN FET

CCG6 has a power supply input, V5V, for providing power to EMCA cables through integrated VCONN FETs. There are two VCONN FETs to power either CC1 or CC2 pins. These FETs can provide 1.5-W power over VCONN on the CC1 and CC2 pins for the active EMCA cables. CCG6 also includes overcurrent protection (OCP) on VCONN.

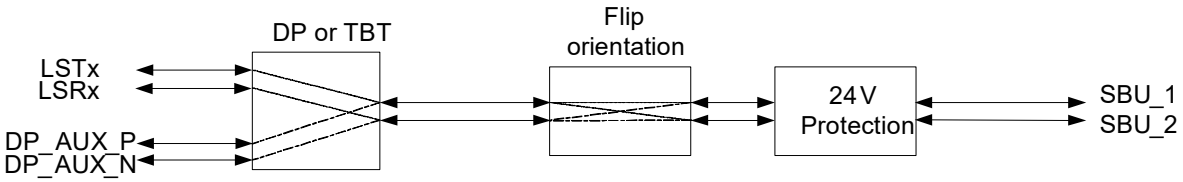
ADC

The USB-PD subsystem contains one 8-bit successive approximation register analog-to-digital converter (SAR ADC). The ADC includes an 8-bit DAC and a comparator. The DAC output forms the positive input of the comparator. The negative input of the comparator is from a 4-input multiplexer. The four inputs of the multiplexer are a pair of global analog multiplex busses, an internal bandgap voltage, and an internal voltage proportional to the absolute temperature. All GPIOs on the chip have access to the ADC through the chip-wide analog mux bus. The CC1 and CC2 pins are not available to connect to the mux bus.

SBU Mux

CCG6 integrates SBU 4x2 Mux that enables selection between the Display Port or Thunderbolt alternate mode and Type-C orientation as shown in Figure 2. Type-C facing SBU pins are protected from accidental short to high-voltage VBUS.

Figure 2. CCG6 SBU Crossbar Switch Block Diagram



SBU Cross Bar Switch Internal Block Diagram

USB 2.0 Mux

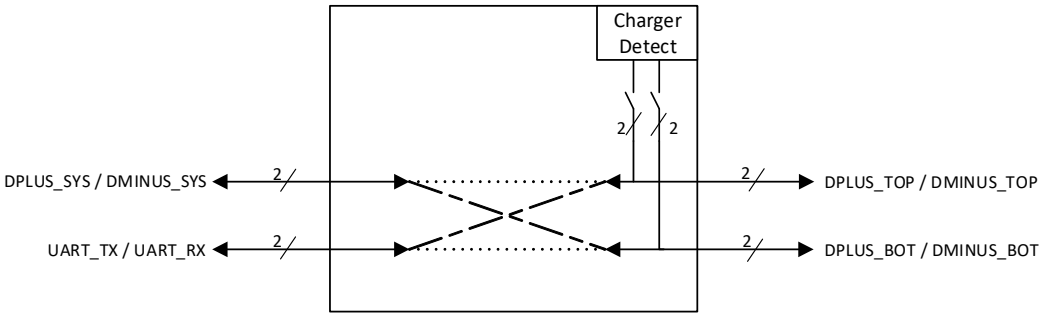
The HS mux contains a 2 × 2 cross bar switch to route the system DPLUS and DMINUS lines to the Type-C top or bottom port based on the CC (Type-C plug) orientation. The unused DPLUS and DMINUS top or bottom lines can be connected to a UART (Debug) port. The maximum operating frequency of UART must be 1 Mbps.

The USB 2.0 mux also contains charger detection/emulation for detecting USB BC1.2 and Apple terminations. The charger detection block is connected to the DPLUS and DMINUS from the system as shown in Figure 3.

To meet the HS eye diagram requirements with sufficient margin, follow these guidelines:

- It is recommended to keep the total USB HS signal trace lengths (USB 2.0 host to CCG6 + CCG6 to Type-C connector pins) to 4 inches.
- Total USB HS signal trace lengths can be increased up to 8 inches by adjusting the drive strength on the USB 2.0 host.
- The differential impedance across the DPLUS/DMINUS signal traces shall be 90 Ω.
- Trace width shall be 6 mils.
- Air Gap (distance between lines) shall be 8 mils.

Figure 3. CCG6 DPLUS/DMINUS Switch Block Diagram



VBUS Discharge

CCG6 also has integrated VBUS discharge circuit. It is used to discharge VBUS to meet the USB-PD specification timing on a detach condition and negative voltage transition.

VBUS Regulator

CCG6 can operate from two power supplies – VSYS and VBUS. CCG6 integrates the regulator (that supports up to 21.5 V) to derive operating supply voltage. The VSYS always takes priority over VBUS. In the absence of VSYS, the regulator powers CCG6 from VBUS.

Gate Driver for VBUS PFET on Consumer Path

CCG6 has an integrated PFET gate driver to drive external PFETs on the VBUS consumer path. The gate driver can drive only low or high-Z, thus requiring an external pull-up. This pin is VBUS voltage-tolerant.

Charger Detect

CCG6 integrates battery charger emulation and detection for USB BC.1.2 and Apple charge.

High-Voltage Tolerant SBU and CC Lines

The chip supports high-voltage tolerant SBU and CC lines. In the case of SBU/CC short to VBUS through connectors, these lines will be protected internally.

VBUS Load Switch Controller for Provider Path

The load switch controller supports up to 20 V on the VBUS Provider Path.

RCP

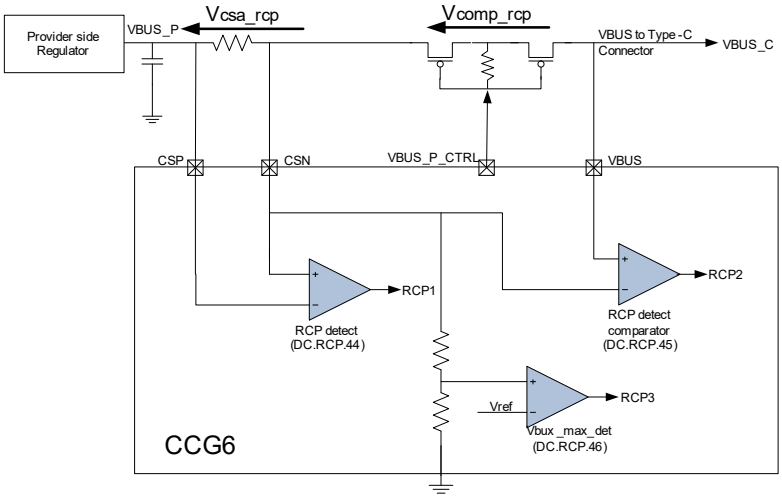
CCG6 integrates the Reverse Current Protection (RCP) circuitry that has the capability of sensing reverse current that lasts for more than 10 µs and protects the system by shutting down the Gate automatically upon detection of such events.

CCG6 provides RCP circuitry that can detect reverse current flow from connector VBUS_C to provider VBUS_P.

The RCP event is recognized whenever VBUS_C > VBUS_P while provider FET is ON, causing current to flow from connector VBUS to provider VBUS. After recognizing the RCP event, the provider FET is shut down thus isolating the provider and connector VBUS.

CCG6 has three distinct mechanisms to detect the reverse current as shown in Figure 4.

Figure 4. RCP Mechanism



- **Mechanism 1:** A comparator senses the voltage drop across external Rsense through pins CSP and CSN. This comparator signals an RCP event whenever CSN > CSP by the Vcsa_rcp voltage given in Table 36. The output of this comparator RCP1 is shown in Figure 4.
- **Mechanism 2:** A comparator senses the voltage drop across provider FET through CSN and VBUS pin of CCG6. This comparator signals an RCP event whenever VBUS > CSN by the Vcomp_rcp voltage given in Table 36. The output of this comparator RCP2 is shown in Figure 4.
- **Mechanism 3:** A comparator senses the 20% voltage of the CSN pin and compares it against Vref = 1.15 V for 5-V provider VBUS application. This comparator signals an RCP event whenever CSN voltage goes above Vbus_max_det voltage given in Table 36 for a 5-V application. The output of this comparator RCP3 is shown in Figure 4. Note that Vref Is programmable and the voltage divider has an option to use 10% or 20% value. For a higher voltage of the provider, the VBUS device automatically adjusts this threshold.

When any one of the three comparator outputs show an RCP event, then the provider FET is turned OFF. The firmware has an option to enable or disable the individual mechanism depending on the application.

CSA

The CCG6 chip has an integrated high-side current sense amplifier that is capable of detecting current in the order of 100 mA across a 5-mΩ external resistor in the provider path. This is used to monitor the current load and detect system faults such as OCP and SCP while sourcing VBUS to the Sink on the Type C port so that the PD controller can shut down the Provider FET to protect devices.

Slew-Rate Controllable Gate Driver

CCG6 has a programmable slew-rate controllable Gate Driver, which can help in limiting the in-rush currents during connect events.

Overvoltage and Undervoltage Protection on VBUS

CCG6 implements an undervoltage/overvoltage (UVOV) detection circuit for the VBUS supply. The threshold for OV and UV detection can be set independently. Both UV and OV detectors have programmable thresholds and are controlled by the firmware. The inputs to the OV comparator are a division (8% or 10%) of VBUS supply voltage and a reference voltage. The reference voltage is configurable in the range (200 mV to 2190 mV) in steps of 10 mV.

The inputs to the UV comparator are a division (10% or 20%) of VBUS supply voltage and a reference voltage. The reference voltage is configurable in the range (200 mV to 2190 mV) in steps of 10 mV.

Overcurrent Protection on VBUS

CCG6 integrates a high-side current sense amplifier to detect overcurrent on the VBUS. Overcurrent protection is sensed using an external 5-mΩ sense resistor connected between the “CSP” and “CSN” pins. The OCP detector threshold is programmable and controlled by the firmware.

True Random Number Generator

In notebook designs, CCG6’s TRNG block is used to authenticate connected devices such as Power Adapter or Dock that include support for USB Type-C Authentication Specification (USBTCAS). CCG6, within the notebook application, will implement the initiator-role as defined in USBTCAS while the connected device implements the responder-role. USBTCAS provides a means for authenticating Type-C devices with regard to identification and configuration.

CPU and Memory Subsystem

CPU

The Cortex-M0 CPU in EZ-PD CCG6 is part of the 32-bit MCU subsystem, which is optimized for low-power operation with extensive clock gating.

The CPU also includes a serial wire debug (SWD) interface, which is a 2-wire form of JTAG. The debug configuration used for EZ-PD CCG6 has four break-point (address) comparators and two watchpoint (data) comparators.

Flash

The EZ-PD CCG6 device has a 128-KB flash module with a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block. The flash block is designed to deliver two wait-states (WS) access time at 48 MHz. The flash accelerator delivers 85% of single-cycle SRAM access performance on average. Part of the flash module can be used to emulate EEPROM operation if required.

SROM

A supervisory ROM that contains boot and configuration routines is provided.

SRAM

CCG6 supports 12-KB SRAM.

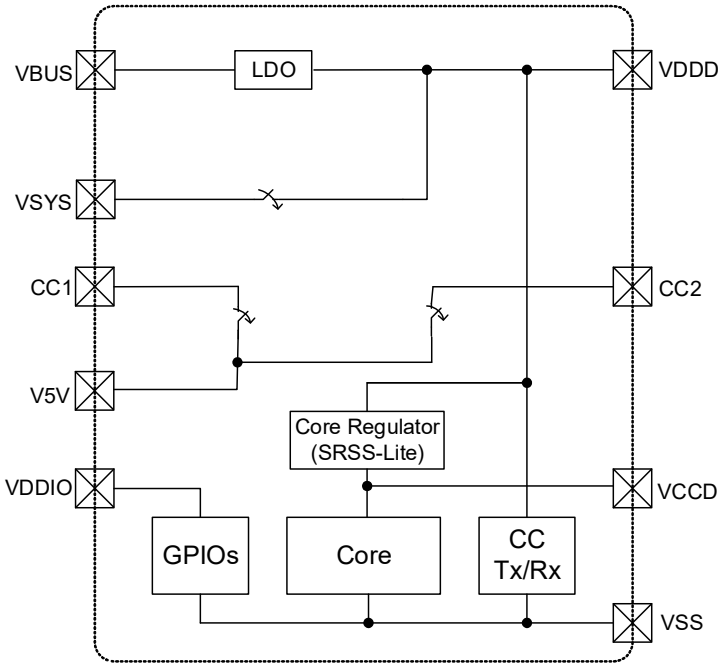
Power System Overview

Figure 5 provides an overview of the EZ-PD CCG6 power system. CCG6 can operate from two possible external supply sources: VBUS (4 V to 21.5 V) or VSYS (2.75 V to 5.5 V). The VBUS supply is regulated inside the chip with a LDO. The switched supply, VDDD, is used directly inside some analog blocks and further regulated down to VCCD, which powers majority of the core. CCG6 has two different power modes: Active and Deep Sleep. Transitions between these power modes are managed by the power system. A separate power domain, VDDIO, is provided for the GPIOs. The VDDD and VCCD pins, both outputs of regulators, are brought out for connecting a 1-µF and 0.1-µF capacitor respectively for the regulator stability only. The VCCD pin is not supported as a power supply. VDDD can source 2 mA (max) for external load. In CCG6, VDDD shall be shorted to VDDIO on PCB.

Table 1. CCG6 Power Modes

Mode	Description
RESET	Power is valid and XRES is not asserted. An internal reset source is asserted or Sleep Controller is sequencing the system out of reset.
ACTIVE	Power is valid and CPU is executing instructions.
DEEP SLEEP	Main regulator and most blocks are shut off. DeepSleep regulator powers logic, but only the low-frequency clock is available.

Figure 5. EZ-PD CCG6 Power System



Peripherals

CCG6 has four SCBs, which can each implement an I²C, UART, or SPI interface.

I²C Mode: The hardware I²C block implements a full multi-master and slave interface (it is capable of multimaster arbitration). This block is capable of operating at speeds of up to 1 Mbps (Fast Mode Plus) and has flexible buffering options to reduce interrupt overhead and latency for the CPU. The FIFO mode is available in all channels and is very useful in the absence of DMA.

The I²C peripheral is compatible with the I²C Standard-mode, Fast-mode, and Fast-Mode Plus devices as defined in the NXP I²C bus specification and user manual (UM10204). The I²C bus I/O is implemented with GPIO in open-drain modes. The I²C bus uses open-drain drivers for clock and data with pull-up resistors on the bus for clock and data connected to all nodes. The required Rise and Fall times for different I²C speeds are guaranteed by using appropriate pull-up resistor values depending on VDDD, Bus Capacitance, and resistor tolerance.

For detailed information on how to calculate the optimum pull-up resistor value for your design, refer to the UM10204 I²C bus specification and user manual (the latest revision is available at www.nxp.com).

CCG6 is not completely compliant with the I²C spec for the following:

- Only SCB1 is overvoltage-tolerant. SCB2, SCB3, and SCB4 GPIO cells are not overvoltage-tolerant and, therefore, cannot be hot-swapped or powered up independently of the rest of the I²C system.
- Fast-mode Plus has an IOL specification of 20 mA at a VOL of 0.4 V. The GPIO cells can sink a maximum of 8-mA IOL with a VOL maximum of 0.6 V.
- Fast-mode and Fast-mode Plus specify minimum Fall times, which are not met with the GPIO cell; Slow strong mode can help meet this spec depending on the Bus Load.

One of the SCB (typically SCB1) blocks is used to implement the Host Processor Interface (HPI) slave, which allows an external MCU to control the firmware operation.

The HPI I2C Slave address is configurable using the I2C_CFG_EC pin as shown in the following table.

Table 2. I²C Slave Address Configuration

I2C_CFG_EC Configuration	I²C Slave
Floating	0x08
Pulled up with 1 kΩ	0x42
Pulled down with 1 kΩ	0x40

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI SSP (essentially adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO.

Timer/Counter/PWM Block (TCPWM)

CCG6 has two TCPWM blocks. Each TCPWM block consists of four 16-bit counters with user-programmable period length. There is a Capture register to record the count value at the time of an event (which may be an I/O event), a period register which is used to either stop or auto-reload the counter when its count is equal to the period register, and compare registers to generate compare value signals which are used as PWM duty cycle outputs. The block also provides true and complementary outputs with programmable offset between them to allow use as deadband programmable complementary PWM outputs. It also has a Kill input to force outputs to a predetermined state; for example, this is used in motor drive systems when an overcurrent state is indicated and the PWMs driving the FETs need to be shut off immediately with no time for software intervention.

GPIO

CCG6 has 17 GPIOs that includes the SCB and SWD pins, which can also be used as GPIOs. The I²C pins from only SCB 1 are overvoltage-tolerant. The GPIO block implements the following:

- Seven drive strength modes:
  - Input only
  - Weak pull-up with strong pull-down
  - Strong pull-up with weak pull-down
  - Open drain with strong pull-down
  - Open drain with strong pull-up
  - Strong pull-up with strong pull-down
  - Weak pull-up with weak pull-down
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output buffer enabling/disabling in addition to the drive strength modes
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode)
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves. Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (6 for CCG6 since it has 6 ports).

Pinouts

Table 3. Pinout for CYPD6125-40LQXIT and CYPD6137-40LQXIT

Group Name	Pin Name	Port	Pin	Description
USB Type-C	CC1	Analog	9	Connect to Type-C CC1 pin. Filter noise with 390-pF cap to GND.
	CC2	Analog	7	Connect to Type-C CC2 pin. Filter noise with 390-pF cap to GND.
Mux	DPLUS_SYS	Analog	23	Connect to USB 2.0 DP from Host side.
	DMINUS_SYS	Analog	24	Connect to USB 2.0 DM from Host side.
	UART_TX/GPIO	P4.0	29	Connect to Debug port UART_TX (optional) from host side or can be used as GPIO. If unused, leave floating.
	UART_RX/GPIO	P4.1	30	Connect to Debug port UART_RX (optional) from host side or can be used as GPIO. If unused, leave floating.
	DPLUS_BOT	Analog	26	Connect to Type-C DP1 pin. Keep trace length less than 2".
	DMINUS_BOT	Analog	25	Connect to Type-C DM1 pin. Keep trace length less than 2".
	DMINUS_TOP	Analog	27	Connect to Type-C DM2 pin. Keep trace length less than 2".
	DPLUS_TOP	Analog	28	Connect to Type-C DP2 pin. Keep trace length less than 2".
	SBU2	Analog	34	Connect to Type-C SBU2 pin.
	SBU1	Analog	35	Connect to Type-C SBU1 pin.
	AUX_P	Analog	36	Connect to Auxiliary signal P from Display Port Controller. If not used, leave floating.
	AUX_N	Analog	37	Connect to Auxiliary signal N from Display Port Controller. If not used, leave floating.
	LSTX/GPIO	P0.0	38	Connect to UART_TX (LSTX) signal from Thunderbolt Port Controller or can be used as GPIO. If not used, leave floating
	LSRX/GPIO	P0.1	39	Connect to UART_RX (LSRX) signal from Thunderbolt Port Controller or can be used as GPIO. If not used, leave floating
VBUS Control	VBUS_P_CTRL	Analog	11	Slew Rate controlled I/O for enabling/disabling Provider side PFET 0: Path ON High Z: Path OFF
	VBUS_C_CTRL	Analog	12	Pin for enabling/disabling Consumer side PFET 0: Path ON High Z: Path OFF
VBUS OCP	CSP	Analog	1	Current Sense Positive Input
	CSN	Analog	40	Current Sense Negative Input

Table 3. Pinout for CYPD6125-40LQXIT and CYPD6137-40LQXIT *(continued)*

Group Name	Pin Name	Port	Pin	Description
GPIOs and Serial Interfaces	SWD_IO/TBT_RST/GPIO	P1.4	6	SWD I/O/GPIO
	SWD_CLK/I2C_CFG_EC/ GPIO	P1.0	2	SWD Clock/ I^2C config line. I^2C config line is used to select the I^2C address of HPI interface. The state of line decides the 7 bit I^2C address for HPI. I^2C Config Line Floating: 0x08 Pulled up with 1 KΩ: 0x42 Pulled down with 1 KΩ: 0x40
	I2C_SDA_SCB2_TBT/GPIO	P1.1	3	SCB2 I^2C Data/GPIO
	I2C_SCL_SCB2_TBT/GPIO	P1.2	4	SCB2 I^2C Clock/GPIO
	I2C_INT_TBT/GPIO	P1.3	5	TBT interrupt for port 1/GPIO
	OVP_TRIP/I2C_SDA_SCB4/GPIO	P2.1	14	VBUS overvoltage output indicator/SCB4 I^2C Data
	UV_OCP_TRIP/I2C_SCL_SCB4/GPIO	P2.0	13	VBUS undervoltage or OCP Output Indicator/SCB4 I^2C Clock/GPIO
	I2C_SDA_SCB1_EC/GPIO	P5.0	16	SCB1 I^2C Data/GPIO
	I2C_SCL_SCB1_EC/GPIO	P5.1	17	SCB1 I^2C Clock/GPIO
	I2C_INT_EC/GPIO	P2.2	15	Embedded Controller interrupt/GPIO
	HPD/GPIO	P3.0	18	Hot Plug Detect I/O/GPIO
	I2C_SDA_SCB3 / GPIO / VSEL_2	P3.1	20	SCB3 I^2C Data or GPIO or voltage selection control for VBUS
	I2C_SCL_SCB3 / GPIO /VSEL_1	P3.2	21	SCB3 I^2C Clock or GPIO or voltage selection control for VBUS
Reset	XRES	Analog	10	Reset input (Active LOW)
Power	VBUS	Power	22	Supply input (4 V–21.5 V) for VBUS to 3.3-V Regulator. This pin also discharges VBUS using internal pull-down and also has monitors for overvoltage and undervoltage conditions.
	VSYS	Power	19	Supply input (2.75 V–5.5 V) for PD subsystem and System resources.
	VDDD	Power	31	Output of VBUS to 3.3-V regulator or connected to VSYS using switch. Bypass with cap to gnd. This pin can drive 2-mA external load.
	VDDIO	Power	32	This pin can be shorted to VDDD or an independent supply can be given.
	VCCD	Power	33	1.8-V regulator output for filter capacitor. This pin cannot drive external load.
	V5V	Power	8	4.85-V to 5.5-V supply input to power EMCA cables. Connected to CC1 or CC2 using low impedance switches.
Ground	VSS	Ground	EPAD	Ground

Figure 6. 40-Pin QFN Pin Map (Top View) for CYPD6125-40LQXIT and CYPD6137-40LQXIT

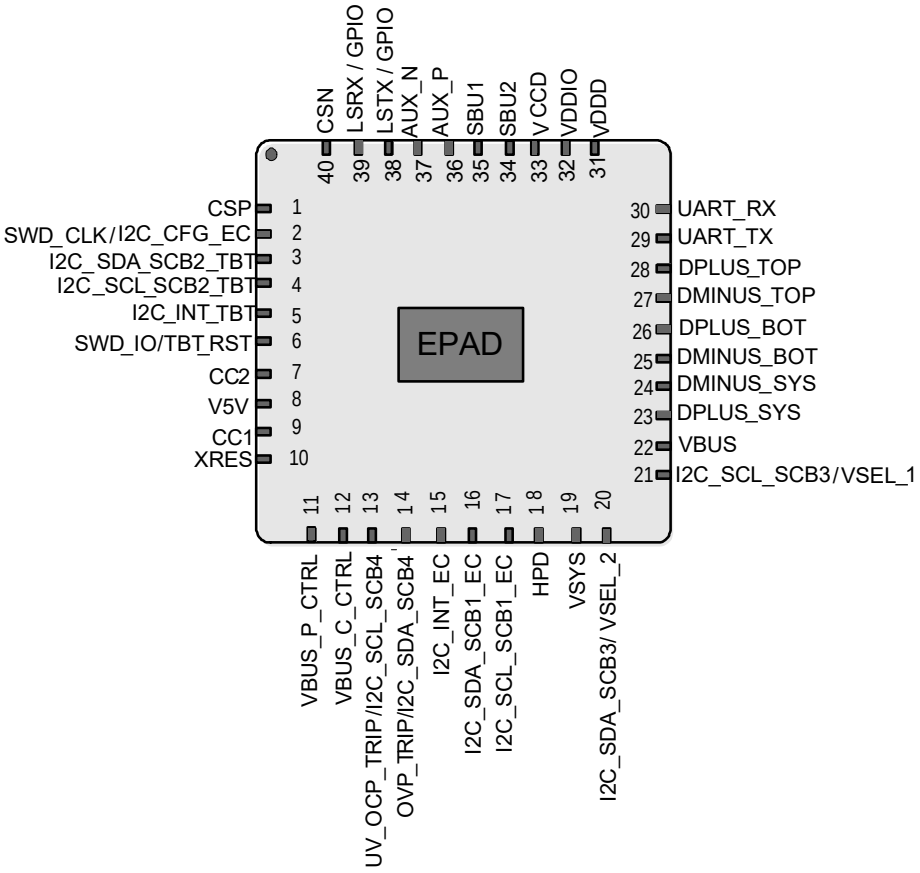


Table 4 through Table 7 provide the various configuration options for the serial interfaces.

Table 4. Serial Communication Block (SCB1) Configuration

QFN Pin	UART	SPI	I2C	GPIO Functionality
16	UART_RTS_SCB1	SPI_MOSI_SCB1	I2C_SDA_SCB1	GPIO
17	UART_TX_SCB1	SPI_MISO_SCB1	I2C_SCL_SCB1	GPIO
18	UART_RX_SCB1	SPI_CLK_SCB1	–	HPD/GPIO
15	UART_CTS_SCB1	SPI_SEL_SCB1	–	I2C_INT_EC/GPIO

Table 5. Serial Communication Block (SCB2) Configuration

QFN Pin	UART	SPI Master	I2C Slave	GPIO Functionality
2	UART_RX_SCB2	SPI_SEL_SCB2	–	SWD_CLK/I2C_CFG_EC/GPIO
3	UART_TX_SCB2	SPI_MOSI_SCB2	I2C_SDA_SCB2	I2C_SDA_SCB2_TBT/GPIO
4	UART_CTS_SCB2	SPI_MISO_SCB2	I2C_SCL_SCB2	I2C_SCL_SCB2_TBT/GPIO
5	UART_RTS_SCB2	SPI_CLK_SCB2	–	I2C_INT_TBT/GPIO

Table 6. Serial Communication Block (SCB3) Configuration

QFN Pin	UART	SPI Master	I2C Slave	GPIO Functionality
20	UART_CTS_SCB3	SPI_SEL_SCB3	I2C_SDA_SCB3	VSEL_2/GPIO
21	UART_RTS_SCB3	SPI_MOSI_SCB3	I2C_SCL_SCB3	VSEL_1/GPIO
29	UART_TX_SCB3	SPI_MISO_SCB3	–	UART_TX/GPIO
30	UART_RX_SCB3	SPI_CLK_SCB3	–	UART_RX/GPIO

Table 7. Serial Communication Block (SCB4) Configuration

QFN Pin	UART	SPI Master	I2C Slave	GPIO Functionality
13	UART_CTS_SCB4	SPI_SEL_SCB4	I2C_SCL_SCB4	GPIO
14	UART_RTS_SCB4	SPI_MOSI_SCB4	I2C_SDA_SCB4	GPIO
38	UART_TX_SCB4	SPI_MISO_SCB4	–	LSTX/GPIO
39	UART_RX_SCB4	SPI_CLK_SCB4	–	LSRX/GPIO

Application Diagrams

Figure 7 illustrates a Type-C port Thunderbolt Notebook DRP application diagram using CCG6. The Type-C port can be used as a power provider or a power consumer.

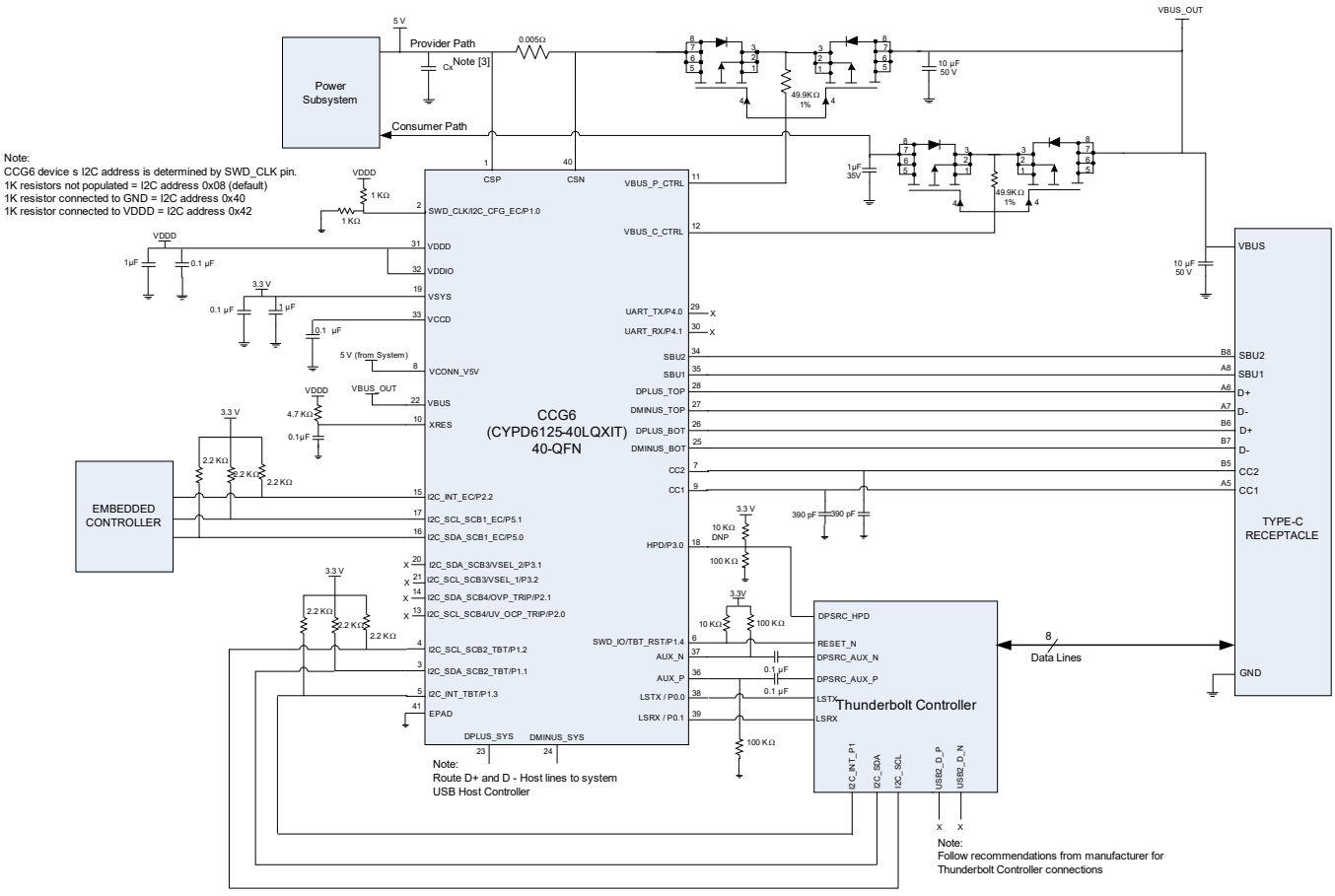
The CCG6 device communicates with the embedded controller (EC), which manages the Battery Charger Controller (BCC) to control the charging and discharging of the internal battery. It also updates the Thunderbolt Controller via I^2C to route the HighSpeed signals coming from the Type-C port to the USB host (during normal mode) or the Graphics processor unit (during Display port Alternate mode) or the Thunderbolt Host (during Thunderbolt Alternate mode) based on the alternate mode negotiation.

The CCG6 device controls the transfer of USB 2.0 DPLUS and DMINUS lines from the top and bottom of the Type-C receptacle to the DPLUS and DMINUS lines of the USB Host controller. CCG6 also handles the routing of SBU1 and SBU2 lines from the Type-C receptacle to the Thunderbolt controller for the Link management. CCG6 offers VBUS Short protection on SBU and CC lines.

The CCG6 device has integrated VCONN FETs for applications that need to provide power for accessories and cables using the VCONN pin of the Type-C receptacle. VBUS FETs are also used for providing power over VBUS and for consuming power over VBUS. The 5-mΩ resistor between the 5-V supply and provider FETs is used for overcurrent detection on the VBUS. The VBUS_P_CTRL pin of CCG6 has an in-built VBUS monitoring circuit that can detect OVP and UVP on VBUS.

Figure 7 illustrates a Single Port Thunderbolt Notebook DRP application diagram using CYPD6125-40LQXIT.

Figure 7. CCG6 in a Single Port Notebook Application using CYPD6125-40LQXIT



Note
3. Refer to AN210403 for the capacitor guidelines.

Electrical Specifications

Absolute Maximum Ratings

Table 8. Absolute Maximum Ratings[4]

Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
V_{SYS_MAX}	Supply relative to V_{SS}	–	–	6	V	–
V_{5V_MAX}	Max supply voltage relative to V_{SS}	–	–	6	V	
V_{BUS_MAX}	Max V_{BUS} voltage relative to Vss	–	–	24	V	
V_{DDIO_MAX}	Max supply voltage relative to V_{SS}	–	–	V_{DDD}	V	
V_{GPIO_ABS}	Inputs to GPIO, DP/DM mux (UART, SYS, DP/DM_top/bot pins), SBU mux (SBU1/2 pins)	–0.5	–	V_{DDIO} + 0.5	V	
I_{GPIO_ABS}	Maximum current per GPIO	–25	–	25	mA	–
$I_{GPIO\_INJECTION}$	GPIO injection current, Max for $V_{IH} > V_{DDD}$, and Min for $V_{IL} < V_{SS}$	–0.5	–	0.5	mA	Absolute max, current injected per pin
ESD_HBM	Electrostatic discharge human body model	2200	–	–	V	–
ESD_HBM_SBU	Electrostatic discharge human body model for SBU1, SBU2 pins	1100	–	–	V	Only applicable to SBU1, SBU2 pins
ESD_CDM	Electrostatic discharge charged device model	500	–	–	V	–
LU	Pin current for latch-up	–200	–	200	mA	–
VCC_PIN_ABS	Max voltage on CC1 and CC2 pins	–	–	24	V	–
VSBU_PIN_ABS	Max voltage on SBU1 and SBU2 pins	–	–	24	V	
VGPIO_OVT_ABS	OVT pins (16, 17) voltage	–0.5	–	6	V	–

Note

4. Usage above the absolute maximum conditions listed in Table 8 may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods of time may affect device reliability. The maximum storage temperature is 150 °C in compliance with JEDEC Standard JESD22-A103, High Temperature Storage Life. When used below absolute maximum conditions but above normal operating conditions, the device may not operate to specification.

Device-Level Specifications

All specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 3.0 V to 5.5 V except where noted.

DC Specifications

Table 9. DC Specifications (Operating Conditions)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.PWR#23	V_{SYS}		2.75	–	5.5	V	UFP applications
SID.PWR#23_A	V_{SYS}		3	–	5.5	V	DFP/DRP applications
SID.PWR#22	V_{BUS}		4	–	21.5	V	–
SID.PWR#1	V_{DDD}	Regulated output voltage when V_{SYS} powered	V_{SYS} – 0.05	–	V_{SYS}	V	–
SID.PWR#1_A	V_{DDD}	Regulated output voltage when V_{BUS} powered	3	–	3.65	V	–
SID.PWR#26	V_{5V}		4.85	–	5.5	V	–
SID.PWR#13	V_{DDIO}		V_{DDD}	–	V_{DDD}	V	At system-level short the V_{DDIO} to V_{DDD}
SID.PWR#24	V_{CCD}	Regulated output voltage (for Core Logic)	–	1.8	–	V	–
SID.PWR#15	C_{EFC}	Regulator bypass capacitor for V_{CCD}	–	100	–	nF	X5R ceramic
SID.PWR#16	C_{EXC}	Regulator bypass capacitor for V_{DDD}	–	1	–	µF	
Active Mode, V_{SYS} = 2.75 V to 5.5 V. Typical values measured at V_{SYS} = 3.3 V							
SID.PWR#4	I_{DD12}	Supply current	–	10	–	mA	T_A = 25 °C, CC I/O IN Transmit or Receive, no I/O sourcing current, CPU at 24 MHz, PD port active
Deep Sleep Mode, V_{SYS} = 2.75 V to 3.6 V							
SID34	I_{DD29}	V_{SYS} = 2.75 to 3.6 V, I^2C, wakeup and WDT on.	–	150	–	µA	V_{SYS} = 3.3 V, T_A = 25 °C,
SID_DS1	I_{DD_DS1}	V_{SYS} = 3.3 V, CC wakeup on, Type-C not connected.	–	100	–	µA	Power source = V_{SYS}, Type-C not attached, CC enabled for wakeup, Rp and Rd connected at 70-ms intervals by CPU.
SID_DS3	I_{DD_DS2}	V_{SYS} = 3.3 V, CC wakeup on, DP/DM, SBU ON with ADC/CSA/UVOV On	–	500	–	µA	IDD_DS1 + DP/DM, SBU, CC ON, ADC/CSA/UVOV ON
XRES Current							
SID307	I_{DD_XR}	Supply current while XRES asserted	–	50	–	µA	Power Source = V_{SYS} = 3.3 V, Type-C Not Attached, T_A = 25 °C

CPU

Table 10. CPU Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.CLK#4	F_{CPU}	CPU input frequency	–	–	48	MHz	All V_{DDD}
SID.PWR#21	$T_{DEEPSLEEP}$	Wakeup from Deep Sleep mode	–	35	–	µs	Guaranteed by characterization
SYS.XRES#5	T_{XRES}	External reset pulse width	5	–	–	µs	
SYS.FES#1	$T_{\_PWR\_RDY}$	Power-up to “Ready to accept I^2C/CC command”	–	5	25	ms	

GPIO

Table 11. GPIO DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.GIO#37	V_{IH_CMOS}	Input voltage HIGH threshold	0.7 × V_{DDIO}	–	–	V	CMOS input
SID.GIO#38	V_{IL_CMOS}	Input voltage LOW threshold	–	–	0.3 × V_{DDIO}	V	CMOS input
SID.GIO#39	$V_{IH\_VDDIO2.7-}$	LVTTL input, V_{DDIO} < 2.7 V	0.7 × V_{DDIO}	–	–	V	–
SID.GIO#40	$V_{IL\_VDDIO2.7-}$	LVTTL input, V_{DDIO} < 2.7 V	–	–	0.3 × V_{DDIO}	V	–
SID.GIO#41	$V_{IH\_VDDIO2.7+}$	LVTTL input, $V_{DDIO} \geq$ 2.7 V	2.0	–	–	V	–
SID.GIO#42	$V_{IL\_VDDIO2.7+}$	LVTTL input, $V_{DDIO} \geq$ 2.7 V	–	–	0.8	V	–
SID.GIO#33	V_{OH}	Output voltage HIGH level	V_{DDIO} – 0.6	–	–	V	I_{OH} = –4 mA at 3-V V_{DDIO}
SID.GIO#34	V_{OH}	Output voltage HIGH level	V_{DDIO} – 0.5	–	–	V	I_{OH} = –1mA at 1.8-V V_{DDIO}
SID.GIO#35	V_{OL}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 4 mA at 1.8-V V_{DDIO}
SID.GIO#35A	$V_{OL\_I2C\_2}$	Output low voltage			0.4	V	I_{OL} = 3 mA, V_{DDIO} > 2 V
SID.GIO#35B	$V_{OL\_I2C\_3}$	Output low voltage			0.6[5]	V	I_{OL} = 6 mA, V_{DDIO} > 1.71 V
SID.GIO#35C	V_{OL1_20mA}	Output low voltage			0.4	V	I_{OL} = 20 mA, V_{DDIO} > 3.0 V, Applicable for overvoltage-tolerant pins only
SID.GIO#36	V_{OL}	Output voltage LOW level	–	–	0.6	V	I_{OL} = 10 mA (IOL_LED) at 3-V V_{DDIO}
SID.GIO#5	Rpu	Pull-up resistor when enabled	3.5	5.6	8.5	kΩ	+25 °C T_A, All V_{DDIO}
SID.GIO#6	Rpd	Pull-down resistor when enabled	3.5	5.6	8.5	kΩ	+25 °C T_A, All V_{DDIO}
SID.GIO#16	I_{IL}	Input leakage current (absolute value)	–	–	2	nA	+25 °C T_A, 3-V V_{DDIO}
SID.GIO#17	C_{PIN}	Max pin capacitance	–	3	7	pF	–
SID.GIO#43	V_{HYSTTL}	Input hysteresis, LVTTL	15	40	–	mV	V_{DDIO} > 2.7 V. Guaranteed by characterization.
SID.GIO#44	$V_{HYSCMOS}$	Input hysteresis CMOS	0.05 × V_{DDIO}	–	–	mV	V_{DDIO} < 4.5 V

Note
5. To drive full bus load at 400 kHz, 6-mA I_{OL} is required at 0.6-V V_{OL}. Parts not meeting this specification can still function, but not at 400 kHz and 400 pF.

Table 11. GPIO DC Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.GIO#44A	$V_{HYSCMOS55}$	Input hysteresis CMOS	200	–	–	mV	V_{DDIO} > 4.5 V

Table 12. GPIO AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID70	T_{RISEF}	Rise time in Fast Strong mode	2	–	12	ns	3.3-V V_{DDIO}, C_{load} = 25 pF
SID71	T_{FALLF}	Fall time in Fast Strong mode	2	–	12	ns	3.3-V V_{DDIO}, C_{load} = 25 pF
SID.GIO#46	T_{RISES}	Rise time in Slow Strong mode	10	–	60	ns	3.3-V V_{DDIO}, C_{load} = 25 pF
SID.GIO#47	T_{FALLS}	Fall time in Slow Strong mode	10	–	60	ns	3.3-V V_{DDIO}, C_{load} = 25 pF
SID.GIO#48	F_{GPIO_OUT1}	GPIO F_{OUT}; 3.3 V≤V_{DDIO}≤5.5 V. Fast Strong mode.	–	–	16	MHz	90/10%, 25-pF load
SID.GIO#49	F_{GPIO_OUT2}	GPIO F_{OUT}; 1.7 V≤V_{DDIO}≤3.3 V. Fast Strong mode.	–	–	16	MHz	90/10%, 25-pF load
SID.GIO#50	F_{GPIO_OUT3}	GPIO F_{OUT}; 3.3 V≤V_{DDIO}≤5.5 V. Slow Strong mode.	–	–	7	MHz	90/10%, 25-pF load
SID.GIO#51	F_{GPIO_OUT4}	GPIO F_{OUT}; 1.7 V≤V_{DDIO}≤3.3 V. Slow Strong mode.	–	–	3.5	MHz	90/10%, 25-pF load
SID.GIO#52	F_{GPIO_IN}	GPIO input operating frequency; 1.7 V≤V_{DDIO}≤5.5 V.	–	–	16	MHz	90/10% V_{IO}

XRES

Table 13. XRES DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.XRES#1	V_{IH}	Input voltage HIGH threshold	0.7 × V_{DDIO}	–	–	V	CMOS input
SID.XRES#2	V_{IL}	Input voltage LOW threshold	–	–	0.3 × V_{DDIO}	V	CMOS input
SID.XRES#3	C_{IN}	Input capacitance	–	–	7	pF	–
SID.XRES#4	$V_{HYSXRES}$	Input voltage hysteresis	–	0.05 × V_{DDIO}	–	mV	Guaranteed by characterization

Digital Peripherals

The following specifications apply to the Timer/Counter/PWM peripherals in the Timer mode.

Pulse Width Modulation (PWM) for GPIO Pins

Table 14. PWM AC Specifications (Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.TCPWM.3	$T_{CPWMFREQ}$	Operating frequency	–	–	Fc	MHz	Fc max = CLK_SYS. Maximum = 48 MHz.
SID.TCPWM.4	$T_{PWMENEXT}$	Input trigger pulse width	2/Fc	–	–	ns	For all trigger events
SID.TCPWM.5	T_{PWMEXT}	Output trigger pulse width	2/Fc	–	–	ns	Minimum possible width of Overflow, Underflow, and CC (Counter equals Compare value) outputs
SID.TCPWM.5A	T_{CRES}	Resolution of counter	1/Fc	–	–	ns	Minimum time between successive counts
SID.TCPWM.5B	PWM_{RES}	PWM resolution	1/Fc	–	–	ns	Minimum pulse width of PWM output
SID.TCPWM.5C	Q_{RES}	Quadrature inputs resolution	1/Fc	–	–	ns	Minimum pulse width between quadrature-phase inputs

I^2C

Table 15. Fixed I^2C AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID153	F_{I2C1}	Bit rate	–	–	1	Mbps	–

UART

Table 16. Fixed UART AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID162	F_{UART}	Bit rate	–	–	1	Mbps	–

SPI

Table 17. Fixed SPI AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID166	F_{SPI}	SPI operating frequency (Master; 6X oversampling)	–	–	8	MHz	–

Table 18. Fixed SPI Master Mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID167	T_{DMO}	MOSI valid after SClock driving edge	–	–	15	ns	–
SID168	T_{DSI}	MISO valid before SClock capturing edge	20	–	–	ns	Full clock, late MISO sampling
SID169	T_{HMO}	Previous MOSI data hold time	0	–	–	ns	Referred to slave capturing edge

Table 19. Fixed SPI Slave Mode AC Specifications

(Guaranteed by Characterization)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID170	T_{DMI}	MOSI valid before Sclock capturing edge	40	–	–	ns	–
SID171	T_{DSO}	MISO valid after Sclock driving edge	–	–	48 + (3 × T_{SCB})	ns	$T_{SCB} = T_{CPU}$
SID171A	T_{DSO_EXT}	MISO valid after Sclock driving edge in Ext Clk mode	–	–	48	ns	–
SID172	T_{HSO}	Previous MISO data hold time	0	–	–	ns	–
SID172A	$T_{SSELSCK}$	SSEL valid to first SCK Valid edge	100	–	–	ns	–

Memory

Table 20. Flash AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.MEM#4	T_{ROW_WRITE}	Row (Block) write time (erase and program)	–	–	20	ms	–
SID.MEM#3	T_{ROW_ERASE}	Row erase time	–	–	13	ms	–
SID.MEM#8	$T_{ROWPROGRAM}$	Row program time after erase	–	–	7	ms	25 °C to 55 °C, All V_{DDD}
SID178	$T_{BULKERASE}$	Bulk erase time (128 KB)	–	–	35	ms	Guaranteed by design
SID180	$T_{DEVPROG}$	Total device program time	–	–	25	s	Guaranteed by design
SID.MEM#6	F_{END}	Flash endurance	100k	–	–	cycles	–
SID182	F_{RET1}	Flash retention, $T_A \le 55$ °C, 100K P/E cycles	20	–	–	years	–
SID182A	F_{RET2}	Flash retention, $T_A \le 85$ °C, 10K P/E cycles	10	–	–	years	–
SID182B	F_{RET3}	Flash retention, $T_A \le 105$ °C, 10K P/E cycles	3	–	–	years	–

System Resources

Power-on-Reset (POR) with Brown Out

Table 21. Imprecise Power On Reset (IPOR)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID185	$V_{RISEIPOR}$	Rising trip voltage	0.80	–	1.50	V	Guaranteed by characterization
SID186	$V_{FALLIPOR}$	Falling trip voltage	0.70	–	1.4	V	

Table 22. Precise Power On Reset (POR)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID190	$V_{FALLPPOR}$	Brown-out Detect (BOD) trip voltage in active/sleep modes	1.48	–	1.62	V	Guaranteed by characterization
SID192	$V_{FALLDPSLP}$	BOD trip voltage in Deep Sleep mode	1.1	–	1.5	V	

SWD Interface

Table 23. SWD Interface Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.SWD#1	F_SWDCLK1	3.3 V ≤ V_{DDIO} ≤ 5.5 V	–	–	14	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#2	F_SWDCLK2	1.8 V ≤ V_{DDIO} ≤ 3.3 V	–	–	7	MHz	SWDCLK ≤ 1/3 CPU clock frequency
SID.SWD#3	T_SWDI_SETUP	T = 1/f SWDCLK	0.25 × T	–	–	ns	Guaranteed by characterization
SID.SWD#4	T_SWDI_HOLD	T = 1/f SWDCLK	0.25 × T	–	–	ns	
SID.SWD#5	T_SWDO_VALID	T = 1/f SWDCLK	–	–	0.50 × T	ns	
SID.SWD#6	T_SWDO_HOLD	T = 1/f SWDCLK	1	–	–	ns	

Internal Main Oscillator

Table 24. IMO AC Specifications

(Guaranteed by Design)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.CLK#13	F_{IMOTOL}	Frequency variation at 48 MHz (trimmed)	–	–	±2	%	2.7 V ≤ V_{DDD} < 5.5 V. – 25 °C ≤ T_A ≤ 85 °C
SID226	$T_{STARTIMO}$	IMO start-up time	–	–	7	µs	–
SID.CLK#1	F_{IMO}	IMO frequency	–	48	–	MHz	–

Internal Low-speed Oscillator

Table 25. ILO AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID234	$T_{STARTILO1}$	I_{LO} start-up time	–	–	2	ms	Guaranteed by characterization
SID238	$T_{ILODUTY}$	I_{LO} duty cycle	40	50	60	%	
SID.CLK#5	F_{ILO}	I_{LO} frequency	20	40	80	kHz	–

PD

Table 26. PD DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.DC.cc_shvt.1	vSwing	Transmitter Output High Voltage	1.05	–	1.2	V	–
SID.DC.cc_shvt.2	vSwing_low	Transmitter Output Low Voltage		–	0.075	V	–
SID.DC.cc_shvt.3	zDriver	Transmitter output impedance	33	–	75	Ω	–
SID.DC.cc_shvt.4	zBmcRx	Receiver Input Impedance	10	–		MΩ	Guaranteed by design
SID.DC.cc_shvt.5	Idac_std	Source current for USB standard advertisement	64	–	96	µA	–
SID.DC.cc_shvt.6	Idac_1p5a	Source current for 1.5A at 5 V advertisement	165.6	–	194.4	µA	–
SID.DC.cc_shvt.7	Idac_3a	Source current for 3A at 5 V advertisement	303.6	–	356.4	µA	–
SID.DC.cc_shvt.8	Rd	Pull down termination resistance when acting as UFP (upstream facing port)	4.59	–	5.61	kΩ	–
SID.DC.cc_shvt.9	Rd_db	Pull down termination resistance when acting as UFP, with dead battery	4.08	–	6.12	kΩ	–
SID.DC.cc_shvt.10	zOPEN	CC impedance to ground when disabled	108	–		kΩ	–
SID.DC.cc_shvt.11	DFP_default_0p2	CC voltages on DFP side-Standard USB	0.15	–	0.25	V	–
SID.DC.cc_shvt.12	DFP_1.5A_0p4	CC voltages on DFP side-1.5A	0.35	–	0.45	V	–
SID.DC.cc_shvt.13	DFP_3A_0p8	CC voltages on DFP side-3A	0.75	–	0.85	V	–
SID.DC.cc_shvt.14	DFP_3A_2p6	CC voltages on DFP side-3A	2.45	–	2.75	V	–
SID.DC.cc_shvt.15	UFP_default_0p66	CC voltages on UFP side-Standard USB	0.61	–	0.7	V	–
SID.DC.cc_shvt.16	UFP_1.5A_1p23	CC voltages on UFP side-1.5A	1.16	–	1.31	V	–
SID.DC.cc_shvt.17	Vattach_ds	Deep sleep attach threshold	0.3	–	0.6	%	–
SID.DC.cc_shvt.18	Rattach_ds	Deep sleep pull-up resistor	10	–	50	kΩ	–
SID.DC.cc_shvt.30	FS_0p53	Voltage threshold for Fast Swap Detect	0.49	–	0.58	V	–

Analog-to-Digital Converter

Table 27. ADC DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.ADC.1	Resolution	ADC resolution	–	8	–	Bits	–
SID.ADC.2	INL	Integral non-linearity	–1.5	–	1.5	LSB	–
SID.ADC.3	DNL	Differential non-linearity	–2.5	–	2.5	LSB	–
SID.ADC.4	Gain Error	Gain error	–1.5	–	1.5	LSB	–
SID.ADC.5	VREF_ADC1	Reference voltage of ADC	V_{DDDmin}	–	V_{DDDmax}	V	Reference voltage generated from V_{DDD}
SID.ADC.6	VREF_ADC2	Reference voltage of ADC	1.96	2.0	2.04	V	Reference voltage generated from deep sleep reference

Charger Detect

Table 28. Charger Detect DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
DC.CHGDET.1	VDAT_REF	Data detect voltage in charger detect mode	250	–	400	mV	–
DC.CHGDET.2	VDM_SRC	Dn voltage source in charger detect mode	500	–	700	mV	–
DC.CHGDET.3	VDP_SRC	Dp voltage source in charger detect mode	500	–	700	mV	–
DC.CHGDET.4	IDM_SINK	Dn sink current in charger detect mode	25	–	175	µA	–
DC.CHGDET.5	IDP_SINK	Dp sink current in charger detect mode	25	–	175	µA	–
DC.CHGDET.6	IDP_SRC	Data contact detect current source	7	–	13	µA	–
DC.CHGDET.32	RDM_UP	Dp/Dn pull-up resistance	0.9	–	1.575	kΩ	–
DC.CHGDET.31	RDM_DWN	Dp/Dn pull-down resistance	14.25	–	24.8	kΩ	–
DC.CHGDET.29	RDAT_LKG	Data line leakage on Dp/Dn	300	–	500	kΩ	–
DC.CHGDET.34	VSETH	Logic Threshold	1.26	–	1.54	V	–
DC.ccg6.dpdm.14	RDCP_DAT	Dedicated charging port resistance across DP and DN	–	–	40	Ω	

V_{SYS} Switch

Table 29. V_{SYS} Switch Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.DC.VDDDSW.1	Res_sw	Resistance from supply input to output supply V_{DDD}	–	–	1.5	Ω	Measured with a load current of 5 mA to 10 mA on V_{DDD}.

CSA

Table 30. CSA DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
DC.csa_scp.42	SCP_6A	Short circuit current detect @ 6A	–	±10	–	%	–
DC.csa_scp.43	SCP_10A	Short circuit current detect @10A	–	±10	–	%	–
OP.csa_scp.11	Rsense	External sense register	–	5	–	mΩ	1% accuracy
DC.csa_scp.44	Iocp_1A	OCP Trip threshold for 1A with Rsense = 5 mΩ	–	130 ±20%	–	%	1A PD contracts OCP set at 130% of contract value or user programmable
	Iocp_1A	OCP Trip threshold for 1A with Rsense = 10 mΩ	–	130 ±10%	–	%	1A PD contracts OCP set at 130% of contract value or user programmable
DC.csa_scp.45	Iocp_5A	OCP Trip threshold for 2A, 3A, 4A and 5A contracts with Rsense = 5/10 mΩ	–	130 ±10%	–	%	2A, 3A, 4A, and 5A PD contracts OCP set at 130% of contract value OR user programmable
DC.rcp_scp.7a	I_csainn_lk	CSP pin input leakage when RCP and CSA blocks are OFF			10	µA	For provider V_{BUS} = 5 V
DC.rcp_scp.6a	I_csainp_lk	CSN pin input leakage when RCP and CSA blocks are OFF			80	µA	For provider V_{BUS} = 5 V

Table 30. CSA DC Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
DC.sys.1	I_CSP_RCP_ON _CSA_OFF	CSP pin current when RCP block is ON and SCP is OFF			20	µA	For provider V_{BUS} = 5 V
DC.sys.2	I_CSN_RCP_ON _CSA_OFF	CSN pin current when RCP block is ON and SCP is OFF			100	µA	For provider V_{BUS} = 5 V
DC.sys.3	I_CSP_CSA_ON	CSP pin current when RCP block is OFF and SCP is ON			30	µA	For provider V_{BUS} = 5 V
DC.sys.4	I_CSN_CSA_ON	CSN pin current when RCP block is OFF and SCP is ON			100	µA	For provider V_{BUS} = 5 V
DC.sys.5	I_CSP_RCP_ON _CSA_ON	CSP pin current when RCP block is ON and SCP is ON			50	µA	For provider V_{BUS} = 5 V. Guaranteed by design.
DC.sys.6	I_CSP_RCP_ON _CAS_ON	CSN pin current when RCP block is ON and SCP is ON			120	µA	For provider V_{BUS} = 5 V. Guaranteed by design.

V_{BUS} UV/OV

Table 31. V_{BUS} UV/OV Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.UVOV.1	$V_{THUVOV1}$	Voltage threshold accuracy in active mode using bandgap reference	–	±3	–	%	–
SID.UVOV.2	$V_{THUVOV2}$	Voltage threshold accuracy in deep sleep mode using deep sleep reference	–	±5	–	%	–
SID.COMP_ACC	COMP_ACC	Comparator input offset at 4s	–15	–	15	mV	–

Consumer Side PFET Gate Driver

Table 32. Consumer Side PFET Gate Driver DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.DC.PGDO.1	Rpd	Resistance when “pull_dn” enabled	–	–	5	kΩ	–
DC.pgdo_pd_isnk.12	iout_0	Sink current through iref_out at iref_ctrl_lv < 11 ≥ LOW and iref_ctrl_lv < 10:0 ≥ 1	–	2	–	µA	–
DC.pgdo_pd_isnk.13	iout_1	Sink current through iref_out at iref_ctrl_lv < 11 ≥ LOW and iref_ctrl_lv < 10:0 ≥ 2	–	4	–	µA	–
DC.pgdo_pd_isnk.14	iout_2	Sink current through iref_out at iref_ctrl_lv < 11 ≥ LOW and iref_ctrl_lv < 10:0 ≥ 4	–	8	–	µA	–
DC.pgdo_pd_isnk.15	iout_3	Sink current through iref_out at iref_ctrl_lv < 11 ≥ LOW and iref_ctrl_lv < 10:0 ≥ 8	–	16	–	µA	–
DC.pgdo_pd_isnk.16	iout_4	Sink current through iref_out at iref_ctrl_lv < 11 ≥ LOW and iref_ctrl_lv < 10:0 ≥ 16	–	32	–	µA	–
DC.pgdo_pd_isnk.17	iout_5	Sink current through iref_out at iref_ctrl_lv < 11 ≥ LOW and iref_ctrl_lv < 10:0 ≥ 32	–	63	–	µA	–
DC.pgdo_pd_isnk.18	iout_6	Sink current through iref_out at iref_ctrl_lv < 11 ≥ LOW and iref_ctrl_lv < 10:0 ≥ 64	–	126	–	µA	–

Table 32. Consumer Side PFET Gate Driver DC Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
DC.pgdo_pd_isnk.19	iout_7	Sink current through iref_out at iref_ctrl_lv < 11 ≥ LOW and iref_ctrl_lv < 10:0 ≥ 128	–	252	–	µA	–
DC.pgdo_pd_isnk.20	iout_8	Sink current through iref_out at iref_ctrl_lv < 11 ≥ LOW and iref_ctrl_lv < 10:0 ≥ 256	–	504	–	µA	–
DC.pgdo_pd_isnk.21	iout_9	Sink current through iref_out at iref_ctrl_lv < 11 ≥ LOW and iref_ctrl_lv < 10:0 ≥ 512	–	1008	–	µA	–
DC.pgdo_pd_isnk.22	iout_10	Sink current through iref_out at iref_ctrl_lv < 11 ≥ LOW and iref_ctrl_lv < 10:0 ≥ 1024	–	2016	–	µA	–

Table 33. Consumer Side PFET Gate Driver AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.ac.pgdo.2	Tr_discharge	Discharge Rate of output node	–	–	5	V/µs	Guaranteed by design
SID.ac.pgdo.sys_1	Tsoft_on	Consumer FET turn-ON delay for soft start	–	5	–	ms	–

Provider Side PFET Gate Driver

Table 34. Provider Side PFET Gate Driver DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
DC.pgdo_pu_1	Rpd	Pull-down resistance when enabled using strongest pull-down strength, using the “STRONG_EN =1” field in the USBPD_PGDO_PD_ISNK_CFG register	–	–	2	kΩ	
DC.pgdo_pu.2	Rpu	Pull-up resistance	–	1	2	kΩ	–
DC.pgdo_pd_isnk.1	Rpd_0	Resistance of iref_out to ground, en_lv = HIGH, iref_ctrl_lv < 11 ≥ HIGH and iref_ctrl_lv < 10:0 ≥ 1	–	6830	–	Ω	–
DC.pgdo_pd_isnk.2	Rpd_1	Resistance of iref_out to ground, en_lv = HIGH, iref_ctrl_lv < 11 ≥ HIGH and iref_ctrl_lv < 10:0 ≥ 2	–	3760	–	Ω	–
DC.pgdo_pd_isnk.3	Rpd_2	Resistance of iref_out to ground, en_lv = HIGH, iref_ctrl_lv < 11 ≥ HIGH and iref_ctrl_lv < 10:0 ≥ 4	–	1900	–	Ω	–
DC.pgdo_pd_isnk.4	Rpd_3	Resistance of iref_out to ground, en_lv = HIGH, iref_ctrl_lv < 11 ≥ HIGH and iref_ctrl_lv < 10:0 ≥ 8	–	1000	–	Ω	–
DC.pgdo_pd_isnk.5	Rpd_4	Resistance of iref_out to ground, en_lv = HIGH, iref_ctrl_lv < 11 ≥ HIGH and iref_ctrl_lv < 10:0 ≥ 16	–	660	–	Ω	–
DC.pgdo_pd_isnk.6	Rpd_5	Resistance of iref_out to ground, en_lv = HIGH, iref_ctrl_lv < 11 ≥ HIGH and iref_ctrl_lv < 10:0 ≥ 32	–	1700	–	Ω	–
DC.pgdo_pd_isnk.7	Rpd_6	Resistance of iref_out to ground, en_lv = HIGH, iref_ctrl_lv < 11 ≥ HIGH and iref_ctrl_lv < 10:0 ≥ 64	–	900	–	Ω	–

Table 34. Provider Side PFET Gate Driver DC Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
DC.pgdo_pd_isnk.8	Rpd_7	Resistance of iref_out to ground, en_lv = HIGH, iref_ctrl_lv < 11 ≥ HIGH and iref_ctrl_lv < 10:0 ≥ 128	–	630	–	Ω	–
DC.pgdo_pd_isnk.9	Rpd_8	Resistance of iref_out to ground, en_lv = HIGH, iref_ctrl_lv < 11 ≥ HIGH and iref_ctrl_lv < 10:0 ≥ 256	–	560	–	Ω	–
DC.pgdo_pd_isnk.10	Rpd_9	Resistance of iref_out to ground, en_lv = HIGH, iref_ctrl_lv < 11 ≥ HIGH and iref_ctrl_lv < 10:0 ≥ 512	–	530	–	Ω	–
DC.pgdo_pd_isnk.11	Rpd_10	Resistance of iref_out to ground, en_lv = HIGH, iref_ctrl_lv < 11 ≥ HIGH and iref_ctrl_lv < 10:0 ≥ 1024	–	520	–	Ω	–

Table 35. Provider Side PFET Gate Driver AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
AC.pgdo_pu.1	Tpu	Pull-up delay	–	10	35	µs	For pull-up load of 4-nF capacitor and 50-kΩ resistor
AC.pgdo_pu.2	Tpd	Pull-down delay	–	–	2	µs	–
AC.pgdo_pu.3	SRpu	Output slew rate measured from 20% to 80% of output rising waveform.	–	–	8	V/µs	Cload = 4 nF, Vout = 0 V to 24 V, external pull-up of 50 kΩ
AC.pgdo_pu.4	SRpd	Output slew rate measured from 80% to 20% of output falling waveform.	–	–	8	V/µs	Cload = 4 nF, Vout = 24 V to 0 V, external pull-up of 50 kΩ
AC.pgdo.sys_1	Tsoft_on	Provider FET turn-ON delay for soft start	–	5	–	ms	–

Provider Side PFET RCP

Table 36. Provider Side PFET RCP DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
DC.RCP.44	Vcsa_rcp	Voltage across external Rsense between CSP/CSN for which RCP condition detected (CSN higher than CSP by Vcsa_rcp)	–	2	6	mV	–
DC.RCP.45	Vcomp_rcp	Voltage across V_{BUS} and CSN pins for which RCP condition is detected	20	–	130	mV	–
DC.RCP.46	Vbus_max_det	Voltage on CSN pin during provider FET ON (source) for which RCP condition is detected (this threshold is user programmable	5.55	5.75	5.95	V	This spec is for 5-V provider V_{BUS} voltage. For higher voltages, firmware changes this threshold based on V_{BUS} contract voltage.

Table 37. Provider Side PFET RCP, SCP AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
AC.RCP_SYS.1	Toff_scp	Provider PFET switching off after short circuit current detect through provider PFET	–	10	–	µs	Provider FET turns off with gate pull-up of 50 kΩ and total gate cap of 4 nF.
AC.RCP_SYS.1	Toff_rcp	Provider PFET switching off after reverse current detect through provider PFET	–	10	–	µs	Provider FET turns off with gate pull-up of 50 kΩ and total gate cap of 4 nF.
AC.RCP_SYS.2	Ton	Recovery time to turn-ON PFET RCP condition is removed	–	55	80	µs	–

Table 38. V_{BUS} Provider Transition Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
AC.tr.1	Ton	V_{BUS} Low to High (10% to 90%) for provider FET	–	5	–	ms	0 to 5-V transition, system-level with external PFET with gate pull-up of 50 kΩ and total gate cap of 4 nF
AC.tr.2	FR_Ton	V_{BUS} Low to High (10% to 90%) during FR swap	–	50	150	µs	0 to 5-V transition, system-level with external PFET with gate pull-up of 50 kΩ and total gate cap of 4 nF
AC.tr.3	Toff	VBUS_P_CTRL High to Low (90% to 10%) using internal active pull-up	–	11	–	µs	5 to 0-V transition, system-level with external PFET with gate pull-up of 50 kΩ and total gate cap of 4 nF

SBU Switch

Table 39. SBU Switch DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
DC.ccg6.20sbu.1	Ron1	On resistance of AUXP/N to SBU1/2 switch @ 3.3-V input	–	4	7	Ω	–
DC.ccg6.20sbu.2	Ron2	On resistance of AUXP/N to SBU1/2 switch @ 1-V input	–	3	5	Ω	–
DC.ccg6.20sbu.3	Isb	Block leakage current (V_{PUMP} + V_{DDD} + V_{CCD})	–	–	15	µA	–
DC.ccg6.20sbu.15	icc	Block ICC when switch fully ON	–	15	125	µA	–
DC.ccg6.20sbu.16	OVP_threshold	Overvoltage protection detection threshold above V_{DDIO}	200	–	1200	mV	–
DC.ccg6.20sbu.17	lsx_ron_3p3	On resistance of LSTX/LSRX to SBU1/2 switch @ 3.3-V input	–	8.5	17	Ω	–
DC.ccg6.20sbu.18	lsx_ron_1	On resistance of LSTX/LSRX to SBU1/2 switch @ 1-V input	–	5.5	11	Ω	–
DC.ccg6.20sbu.19	aux_ron_flat_fs	Switch On flat resistance of AUX_P/N to SBU1/2 switch (from 0 to 3.3 V)	–	–	2.5	Ω	–
DC.ccg6.20sbu.20	aux_ron_flat_hs	Switch On flat resistance of AUX_P/N to SBU1/2 switch (from 0 to 1 V)	–	–	0.5	Ω	–

Table 39. SBU Switch DC Specifications *(continued)*

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
DC.ccg6.20sbu.21	Isx_ron_flat_fs	Switch On flat resistance of LSTX/LSRX to SBU1/2 switch (from 0 to 3.3 V)	–	–	5	Ω	–
DC.ccg6.20sbu.22	Isx_ron_flat_hs	Switch On flat resistance of LSTX/LSRX to SBU1/2 switch (from 0 to 1 V)	–	–	0.5	Ω	–

Table 40. SBU Switch AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
AC.ccg6.20sbu.1	Con	Switch On capacitance	–	–	120	pF	–
AC.ccg6.20sbu.2	Coff	Switch Off capacitance- Connector side	–	–	80	pF	Guaranteed by design
AC.ccg6.20sbu.3	Off_isolation	Switch isolation at F = 1 MHz	–50	–	–	dB	Guaranteed by design
AC.ccg6.20sbu.4	TON	SBU switch turn-on time	–	–	200	µs	–
AC.ccg6.20sbu.5	TOFF	SBU switch turn-off time	–	–	400	µs	–
AC.ccg6.20sbu.3_aux	Off_isolation_AC_aux	Switch isolation at F = 1 MHz, from AUX to SBU pins	–50	–	–	dB	Guaranteed by design
AC.ccg6.20sbu.6	Off_isolation_tran_dB	Coupling on sbu1, 2 terminated to 50 Ω, switch-OFF, 1-MHz rail-to-rail toggling on LSTX/LSRX	–40	–	–	dB	Guaranteed by design
AC.ccg6.20sbu.6_aux	Off_isolation_tran_dB_aux	Coupling on sbu1, 2 terminated to 50 Ω, switch-OFF, 1-MHz rail-to-rail toggling on AUX_P/AUX_N	–30	–	–	dB	Guaranteed by design
AC.ccg6.20sbu.7	X_talk_AC	Cross talk of Switch at F = 1 MHz SBU1/2 to SBU2/1 when is data transferred from LSTX/RX	–50	–	–	dB	Guaranteed by design
AC.ccg6.20sbu.7_aux	X_talk_AC_aux	Cross talk of Switch at F = 1 MHz SBU1/2 to SBU2/1 when is data transferred from AUXP/AUXN	–50	–	–	dB	Guaranteed by design
AC.ccg6.20sbu.8	X_talk_tran_dB	Coupling on SBU2 (1) When Data is transferred from LSX to SBU1 (2) Rail-to-rail data on SBU1(2), static signal on SBU2(1)	–30	–	–	dB	Guaranteed by design
AC.ccg6.20sbu.8_aux	X_talk_tran_dB_aux	Coupling on SBU2 (1) When Data is transferred from AUX to SBU1 (2) Rail-to-rail data on SBU1(2), static signal on SBU2(1)	–30	–	–	dB	Guaranteed by design

DP/DM Switch

Table 41. DP/DM Switch DC Specifications

(Charger Detect Block is Disconnected from DPLUS_TOP, DMINUS_TOP, DPLUS_BOT, and DMINUS_BOT through Switch)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
DC.ccg6.dpdm.1	RON_HS	DP/DM On resistance (0 to 0.5 V) - HS mode	–	–	8	Ω	–
DC.ccg6.dpdm.2	RON_FS	DP/DM On resistance (0 to 3.3 V) - FS mode	–	–	12	Ω	–
DC.ccg6.dpdm.5	Con_FS	Switch On capacitance at 6 MHz - FS mode	–	–	50	pF	Guaranteed by design
DC.ccg6.dpdm.6	Con_HS	Switch on capacitance at 240 MHz - HS mode	–	–	10	pF	–
DC.ccg6.dpdm.9	ileak_pin	pin leakage at DP/DM connector side and host side	–	–	1	µA	–
DC.ccg6.dpdm.10	RON_UART	DP/DM On resistance for UART lines (0 to 3.3 V)	–	–	17	Ω	–
DC.ccg6.dpdm.11	RON_FLAT_HS	DP/DM On Flat resistance in HS mode (0 to 0.4 V)	–	–	0.5	Ω	Guaranteed by design
DC.ccg6.dpdm.12	RON_FLAT_FS	DP/DM On flat resistance in FS mode (0 to 3.3 V)	–	–	4	Ω	Guaranteed by design
DC.ccg6.dpdm.13	RON_FLAT_UART	DP/DM UART On flat resistance (0 to 3.3 V)	–	–	4	Ω	Guaranteed by design

Table 42. DP/DM Switch AC Specifications

(Charger Detect Block is Disconnected from DPLUS_TOP, DMINUS_TOP, DPLUS_BOT, and DMINUS_BOT through Switch)

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
AC.ccg6.dpdm.1	BW_3dB_HS	3-db bandwidth	700	–	–	MHz	Guaranteed by design
AC.ccg6.dpdm.2	BW_3dB_FS	3-db bandwidth	100	–	–	MHz	Guaranteed by design
AC.ccg6.dpdm.5	T_{ON}	DP/DM Switch turn-on time	–	–	200	µs	–
AC.ccg6.dpdm.6	T_{OFF}	DP/DM Switch turn-off time	–	–	0.4	µs	Guaranteed by design
AC.ccg6.dpdm.7	T_{ON_VPUMP}	DP/DM charge pump startup time	–	–	200	µs	Guaranteed by characterization
AC.ccg6.dpdm.8	Off_isolation_HS	Switch-off isolation for HS	–20	–	–	dB	Guaranteed by design
AC.ccg6.dpdm.9	Off_isolation_FS	Switch-off isolation for FS	–50	–	–	dB	Guaranteed by design
AC.ccg6.dpdm.10	X_talk	Cross talk of Switch From FS to HS at F=12 MHz	–50	–	–	dB	Guaranteed by design
AC.ccg6.dpdm.11	uart_coupling	peak to peak coupling of UART signal to DP lines. (UART signal 0 to 3.3 V)	–	–	20	mV	Guaranteed by design

VCONN Switch

Table 43. VCONN Switch DC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
DC.ccg6.20VCONN.1	Ron	Switch ON resistance at V5V = 5 V with 215-mA load current	–	0.7	1.3	Ω	–
DC.ccg6.20VCONN.9	I_{OCP}	Overcurrent detection range for CC1/CC2	550	–	–	mA	–
DC.ccg6.20VCONN.10	OVP_threshold	CC1, CC2 overvoltage protection detection threshold above V_{DDD} or V5V, whichever is higher	200	–	1200	mV	–
DC.ccg6.20VCONN.11	OVP_hysteresis	Overvoltage detection hysteresis	50	–	200	mV	Guaranteed by design
DC.ccg6.20VCONN.12	OCP_hysteresis	Overcurrent detection hysteresis	20	–	60	mA	–
DC.ccg6.20VCONN.14	OVP_threshold_on	Overvoltage detection threshold above V5V of CC1/2, with CC1 or CC2 switch enabled. Same threshold triggers reverse current protection circuit	200	–	700	mV	–

Table 44. VCONN Switch AC Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
AC.ccg6.20VCONN.1	T_{ON}	VCONN switch turn-on time	–	–	200	µs	–
AC.ccg6.20VCONN.2	T_{OFF}	VCONN switch turn-off time	–	–	3	µs	Guaranteed by design

V_{BUS}

Table 45. V_{BUS} Discharge Specifications

Spec ID	Parameter	Description	Min	Typ	Max	Unit	Details/Conditions
SID.VBUS.DISC.1	Ron1	20-V NMOS ON resistance	1500	–	3000	Ω	–
SID.VBUS.DISC.2	Ron2	20-V NMOS ON resistance	750	–	1500	Ω	–
SID.VBUS.DISC.3	Ron3	20-V NMOS ON resistance	500	–	1000	Ω	–
SID.VBUS.DISC.4	Ron4	20-V NMOS ON resistance	375	–	750	Ω	–
SID.VBUS.DISC.5	Ron5	20-V NMOS ON resistance	300	–	600	Ω	–

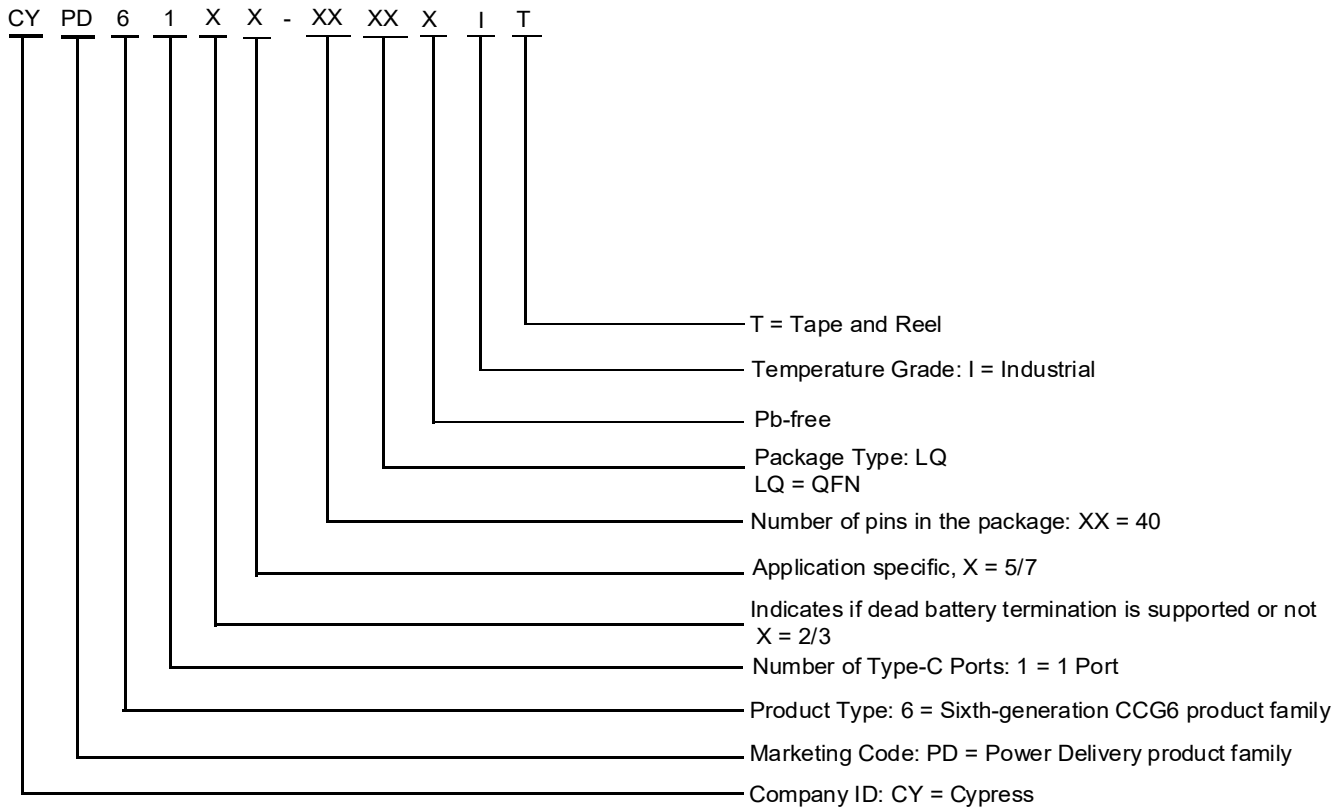
Ordering Information

Table 46 lists the EZ-PD CCG6 part numbers and features.

Table 46. EZ-PD CCG6 Ordering Information

Part Number	Application	Type-C Ports	Dead Battery Termination	Termination Resistor	Role	Package
CYPD6125-40LQXIT	Notebooks, Desktops	1	Yes	Rp[6], Rd[7]	DRP	40-pin QFN
CYPD6137-40LQXIT	Dock	1	No	Rp[6], Rd[7]	DRP	40-pin QFN

Ordering Code Definitions



Notes
6. Termination resistor denoting a Source.
7. Termination resistor denoting an accessory or Sink.

Packaging

Table 47. Package Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Operating ambient temperature	Industrial	–40	25	85	°C
T_J	Operating junction temperature	Industrial	–40	25	100	°C
T_{JA}	Package θ_{JA} (40-pin QFN)	–	–	–	19.3	°C/W
T_{JC}	Package θ_{JC} (40-pin QFN)	–	–	–	13.6	°C/W

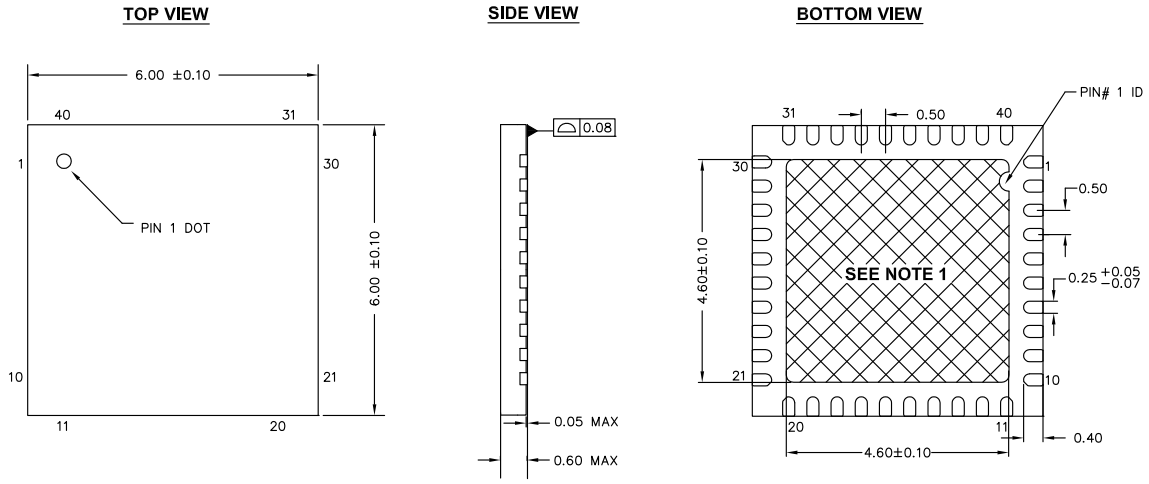
Table 48. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Maximum Time within 5 °C of Peak Temperature
40-pin QFN	260 °C	30 seconds

Table 49. Package Moisture Sensitivity Level (MSL), IPC/JEDEC J-STD-2

Package	MSL
40-pin QFN	MSL 3

Figure 8. 40-Pin QFN (6 × 6 × 0.6 mm), LR40A/LQ40A 4.6 × 4.6 E-PAD (Sawn) Package Outline, 001-80659



NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ±2 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-80659 *A

Acronyms

Table 50. Acronyms Used in this Document

Acronym	Description
ADC	analog-to-digital converter
API	application programming interface
Arm®	advanced RISC machine, a CPU architecture
CC	configuration channel
BOD	Brown out Detect
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
CS	current sense
CSA	current sense amplifier
DFP	downstream facing port
DP	DisplayPort, digital display interface developed by Video Electronics Standards Association
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DRP	dual role power
EEPROM	electrically erasable programmable read-only memory
EMCA	a USB cable that includes an IC that reports cable characteristics (e.g., current rating) to the Type-C ports
EMI	electromagnetic interference
ESD	electrostatic discharge
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output
IC	integrated circuit
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
I/O	input/output, see also GPIO
LVD	low-voltage detect
LVTTL	low-voltage transistor-transistor logic
MCU	microcontroller unit
NC	no connect
NMI	nonmaskable interrupt
NVIC	nested vectored interrupt controller

Table 50. Acronyms Used in this Document *(continued)*

Acronym	Description
opamp	operational amplifier
OCP	overcurrent protection
OVP	overvoltage protection
PCB	printed circuit board
PD	power delivery
PGA	programmable gain amplifier
PHY	physical layer
POR	power-on reset
PRES	precise power-on reset
PSoC®	Programmable System-on-Chip™
PWM	pulse-width modulator
RAM	random-access memory
RCP	reverse current protection
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RX	receive
SAR	successive approximation register
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SPI	Serial Peripheral Interface, a communications protocol
SRAM	static random access memory
SWD	serial wire debug, a test protocol
TBT	Thunderbolt, hardware interface standard for peripherals developed by Intel
TX	transmit
Type-C	a new standard with a slimmer USB connector and a reversible cable, capable of sourcing up to 100 W of power
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UFP	upstream facing port
USB	Universal Serial Bus
USBIO	USB input/output, CCG6 pins used to connect to a USB port
XRES	external reset I/O pin

Document Conventions

Units of Measure

Table 51. Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
Hz	hertz
KB	1024 bytes
kHz	kilohertz
kΩ	kilo ohm
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
mΩ	milliohm
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt

References and Links to Applications Collateral

Knowledge Base Articles

- Key Differences Among EZ-PD™ CCG1, CCG2, CCG3 and CCG5 - KBA210740
- Programming EZ-PD™ CCG2, EZ-PD™ CCG3 and EZ-PD™ CCG5 Using PSoC® Programmer and MiniProg3 - KBA96477
- CCGX Frequently Asked Questions (FAQs) - KBA97244
- Handling Precautions for CY4501 CCG1 DVK - KBA210560
- Cypress EZ-PD™ CCGx Hardware - KBA204102
- Difference between USB Type-C and USB-PD - KBA204033
- CCGx Programming Methods - KBA97271
- Getting started with Cypress USB Type-C Products - KBA04071
- Type-C to DisplayPort Cable Electrical Requirements
- Dead Battery Charging Implementation in USB Type-C Solutions - KBA97273
- Termination Resistors Required for the USB Type-C Connector – KBA97180
- VBUS Bypass Capacitor Recommendation for Type-C Cable and Type-C to Legacy Cable/Adapter Assemblies – KBA97270
- Need for Regulator and Auxiliary Switch in Type-C to DisplayPort (DP) Cable Solution - KBA97274
- Need for a USB Billboard Device in Type-C Solutions – KBA97146
- CCG1 Devices in Type-C to Legacy Cable/Adapter Assemblies – KBA97145
- Cypress USB Type-C Controller Supported Solutions – KBA97179
- Termination Resistors for Type-C to Legacy Ports – KBA97272
- Handling Instructions for CY4502 CCG2 Development Kit – KBA97916
- Thunderbolt™ Cable Application Using CCG3 Devices - KBA210976
- Power Adapter Application Using CCG3 Devices - KBA210975
- Methods to Upgrade Firmware on CCG3 Devices - KBA210974
- Device Flash Memory Size and Advantages - KBA210973
- Applications of EZ-PD™ CCG5 - KBA210739

Application Notes

- AN96527 - Designing USB Type-C Products Using Cypress's CCG1 Controllers
- AN95615 - Designing USB 3.1 Type-C Cables Using EZ-PD™ CCG2
- AN95599 - Hardware Design Guidelines for EZ-PD™ CCG2
- AN210403 - Hardware Design Guidelines for Dual Role Port Applications Using EZ-PD™ USB Type-C Controllers
- AN210771 - Getting Started with EZ-PD™ CCG4

Reference Designs

- EZ-PD™ CCG2 Electronically Marked Cable Assembly (EMCA) Paddle Card Reference Design
- EZ-PD™ CCG2 USB Type-C to DisplayPort Cable Solution
- CCG1 USB Type-C to DisplayPort Cable Solution
- CCG1 USB Type-C to HDMI/DVI/VGA Adapter Solution
- EZ-PD™ CCG2 USB Type-C to HDMI Adapter Solution
- CCG1 Electronically Marked Cable Assembly (EMCA) Paddle Card Reference Design
- CCG1 USB Type-C to Legacy USB Device Cable Paddle Card Reference Schematics
- EZ-USB GX3 USB Type-C to Gigabit Ethernet Dongle
- EZ-PD™ CCG2 USB Type-C Monitor/Dock Solution
- CCG2 20W Power Adapter Reference Design
- CCG2 18W Power Adapter Reference Design
- EZ-USB GX3 USB Type-A to Gigabit Ethernet Reference Design Kit

Kits

- CY4501 CCG1 Development Kit
- CY4502 EZ-PD™ CCG2 Development Kit
- CY4531 EZ-PD CCG3 Evaluation Kit
- CY4541 EZ-PD™ CCG4 Evaluation Kit

Datasheets

- CCG1 Datasheet: USB Type-C Port Controller with Power Delivery
- CYPD1120 Datasheet: USB Power Delivery Alternate Mode Controller on Type-C
- CCG2: USB Type-C Port Controller Datasheet
- CCG3: USB Type-C Controller Datasheet
- CCG5C: USB Type-C Controller Datasheet

Document History Page

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Revision	**ECN**	**Submission Date**	**Description of Change**
*B	6270794	08/01/2018	Post to external web.
*C	6391831	11/22/2018	Updated Features. Updated CCG6 DPLUS/DMINUS Switch Block Diagram. Updated Peripherals. Updated RCP section. Updated Pinouts and Application Diagrams. Updated Ordering Information.
*D	6403615	12/11/2018	Removed Preliminary status. Updated Applications and Logic Block Diagram. Updated Overvoltage and Undervoltage Protection on VBUS. Updated VBUS Load Switch Controller for Provider Path. Added a footnote for SID.GIO#35B. Updated Provider Side PFET RCP, SCP AC Specifications.
*E	6342385	02/19/2019	Updated Copyright information. Updated Type-C in Features. Updated USB 2.0 Mux. Updated Figure 7. Updated Table 33.
*F	6524858	04/04/2019	Updated Table 2: Updated I^2C Slave values for Floating and Pulled up with 1 kΩ. Updated Table 36: DC.RCP.45 Max value changed from 100 mV to 130 mV.
*G	7199318	26/07/2021	Updated package diagram title for Figure 8. Updated Sales, Solutions, and Legal Information and Copyright information.