EZ-USB FX3

SuperSpeed USB Controller

Features

- Universal serial bus (USB) integration
  - USB 3.2, Gen 1 and USB 2.0 peripherals compliant with USB 3.2 Specification Revision 1.0 (TID # 340800007)
  - 5-Gbps SuperSpeed PHY compliant with USB 3.2 Gen 1
  - High-speed On-The-Go (HS-OTG) host and peripheral compliant with OTG Supplement Version 2.0
  - Thirty-two physical endpoints
- General programmable interface (GPIF™ II)
  - Programmable 100-MHz GPIF II enables connectivity to a wide range of external devices
  - 8-, 16-, 24-, and 32-bit data bus
  - Up to 16 configurable control signals
- Fully accessible 32-bit CPU
  - ARM926EJ core with 200-MHz operation
  - 512-KB or 256-KB embedded SRAM
- Additional connectivity to the following peripherals
  - SPI master at up to 33 MHz
  - UART support of up to 4 Mbps
  - I^2C master controller at 1 MHz
  - I^2S master (transmitter only) at sampling frequencies of 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, 96 kHz and 192 kHz
- Selectable clock input frequencies
  - 19.2, 26, 38.4, and 52 MHz
  - 19.2-MHz crystal input support
- Ultra low-power in core power-down mode
  - Less than 60 µA with VBATT on and 20 µA with VBATT off
- Independent power domains for core and I/O
  - Core operation at 1.2 V
  - I2S, UART, and SPI operation at 1.8 to 3.3 V
  - I^2C operation at 1.2 V to 3.3 V
- Package options
  - 121-ball, 10- × 10-mm, 0.8-mm pitch Pb-free ball grid array (BGA)
  - See **Table 24** for details on the seven FX3 variants
- EZ-USB® software development kit (SDK) for code development of firmware and PC Applications
  - Includes RTOS Framework (using ThreadX Version 5)
  - Firmware examples covering all I/O modules
  - Visual Studio host examples using C++ and C#
- SuperSpeed explorer board available for rapid prototyping
  - Several accessory boards also available:
    - Adapter boards for Xilinx/Altera FPGA development
    - Adapter board for video development
    - CPLD board for concept testing and initial development

Applications

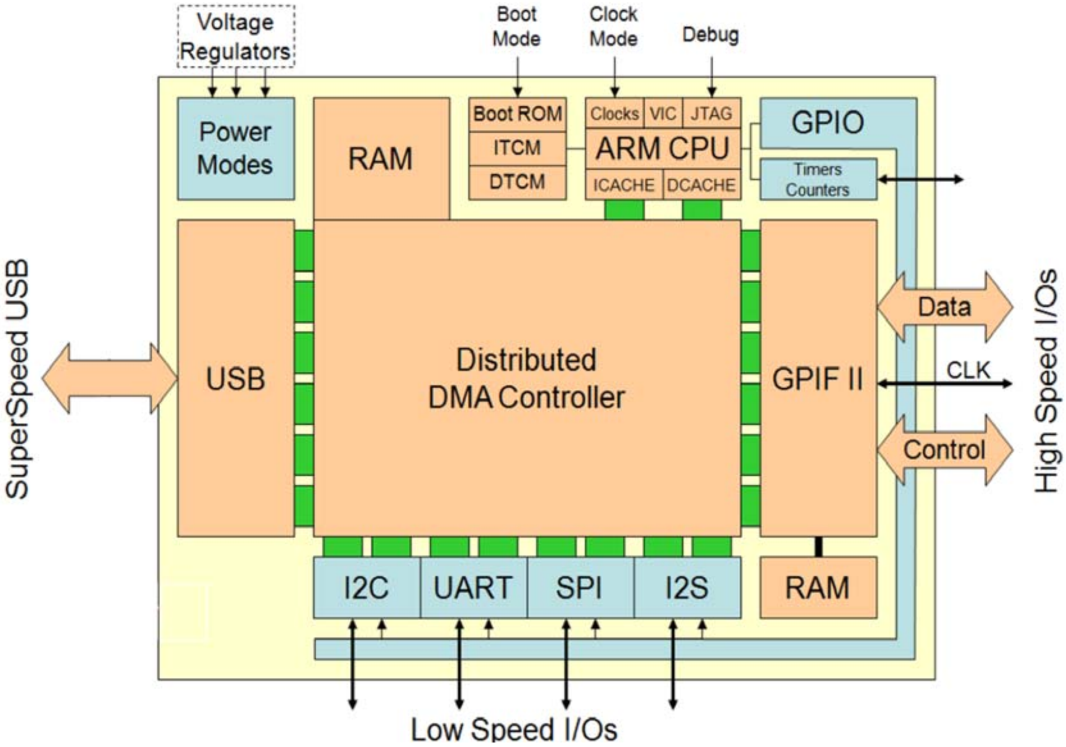
- Digital video camcorders
- Digital still cameras
- Printers
- Scanners
- Video capture cards
- Test and measurement equipment
- Surveillance cameras
- Personal navigation devices
- Medical imaging devices
- Video IP phones
- Portable media players
- Industrial cameras
- Data loggers
- Data acquisition
- High-performance human interface devices (gesture recognition)

Functional description

For a complete list of related documentation, click **here**.

Errata: For information on silicon errata, see **"Errata"** on page 70. Details include trigger conditions, devices affected, and proposed workaround.

Logic block diagram



1 More information

Infineon provides a wealth of data at **www.infineon.com** to help you to select the right USB SuperSpeed device for your design, and to help you to quickly and effectively integrate the device into your design.

- Overview: **USB Portfolio**, **USB Roadmap**
- USB 3.0 Product Selectors: **FX3**, **FX3S**, **CX3**, **HX3**, **SX3**
- Application notes: Infineon offers a large number of USB application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with FX3 are:
  - **AN75705** - Getting Started with EZ-USB FX3
  - **AN76405** - EZ-USB FX3 Boot Options
  - **AN70707** - EZ-USB FX3/FX3S/SX3 Hardware Design Guidelines and Schematic Checklist
  - **AN65974** - Designing with the EZ-USB FX3 Slave FIFO Interface
  - **AN75779** - How to Implement an Image Sensor Interface with EZ-USB FX3 in a USB Video Class (UVC) Framework
  - **AN86947** - Optimizing USB 3.0 Throughput with EZ-USB FX3
  - **AN84868** - Configuring an FPGA over USB Using Cypress EZ-USB FX3
  - **AN68829** - Slave FIFO Interface for EZ-USB FX3: 5-Bit Address Mode
  - **AN73609** - EZ-USB FX2LP/ FX3 Developing Bulk-Loop Example on Linux
  - **AN77960** - Introduction to EZ-USB FX3 High-Speed USB Host Controller
  - **AN76348** - Differences in Implementation of EZ-USB FX2LP and EZ-USB FX3 Applications
  - **AN89661** - USB RAID 1 Disk Design Using EZ-USB FX3S
- Code Examples:
  - **USB Hi-Speed**
  - **USB Full-Speed**
  - **USB SuperSpeed**
- Knowledge Base Articles (KBA):
  - **FX3 FAQs - KBA224051**
  - **Trouble Shooting Guide for the FX3/FX3S/CX3 Enumeration - KBA222372**
  - **EZ-USB™ FX3 Explorer kit as 16-channel 100 MHz logic analyzer with sigrok PulseView - KBA233652**
  - **EZ-USB™ FX3-based HDMI-to-USB3 Vision solution demo kit - KBA235421**
  - **EZ-USB™ FX3: Open source KiCad based schematic and BOM for FX3 camera kit - KBA236085**
- Technical Reference Manual (TRM):
  - EZ-USB FX3 **Technical Reference Manual**
- Development Kits:
  - **CYUSB3KIT-003**, EZ-USB FX3 SuperSpeed Explorer Kit
- Models: **IBIS**

1.1 EZ-USB FX3 Software Development Kit

Cypress delivers the complete software and firmware stack for FX3, in order to easily integrate SuperSpeed USB into any embedded application. The **Software Development Kit** (SDK) comes with tools, drivers and application examples, which help accelerate application development.

1.2 GPIF™ II Designer

The **GPIF II Designer** is a graphical software that allows designers to configure the GPIF II interface of the EZ-USB FX3 USB 3.0 Device Controller.

The tool allows users the ability to select from one of five Cypress supplied interfaces, or choose to create their own GPIF II interface from scratch. Cypress has supplied industry standard interfaces such as Asynchronous and Synchronous Slave FIFO, Asynchronous and Synchronous SRAM, and Asynchronous SRAM. Designers who already have one of these pre-defined interfaces in their system can simply select the interface of choice, choose from a set of standard parameters such as bus width (x8, 16, x32) endianess, clock settings, and compile the interface. The tool has a streamlined three step GPIF interface development process for users who need a customized interface. Users are able to first select their pin configuration and standard parameters. Secondly, they can design a virtual state machine using configurable actions. Finally, users can view output timing to verify that it matches the expected timing. Once the three step process is complete, the interface can be compiled and integrated with FX3.

Table of contents

2 Functional overview

Infineon's EZ-USB FX3 is a SuperSpeed peripheral controller, providing integrated and flexible features.

FX3 has a fully configurable, parallel, general programmable interface called GPIF II, which can connect to any processor, ASIC, or FPGA. GPIF II is an enhanced version of the GPIF in FX2LP, Infineon's flagship USB 2.0 product. It provides easy and glueless connectivity to popular interfaces, such as asynchronous SRAM, asynchronous and synchronous address data multiplexed interfaces, and parallel ATA.

FX3 has integrated the USB 3.2 Gen 1 and USB 2.0 physical layers (PHYs) along with a 32-bit ARM926EJ-S microprocessor for powerful data processing and for building custom applications. It implements an architecture that enables 375-MBps data transfer from GPIF II to the USB interface.

An integrated USB 2.0 OTG controller enables applications in which FX3 may serve dual roles; for example, EZ-USB FX3 may function as an OTG Host to MSC as well as HID-class devices.

FX3 contains 512 KB or 256 KB of on-chip SRAM (see **"Ordering information"** on page 67) for code and data. EZ-USB FX3 also provides interfaces to connect to serial peripherals such as UART, SPI, I^{2}C, and I^{2}S.

FX3 comes with application development tools. The software development kit comes with firmware and host application examples for accelerating time to market.

FX3 complies with the USB 3.2, Gen 1.0 specification and is also backward compatible with USB 2.0. It also complies with USB 2.0 OTG Specification v2.0.

2.1 Application examples

In a typical application (see **Figure 1**), the FX3 functions as the main processor running the application software that connects external hardware to the SuperSpeed USB connection. Additionally, FX3 can function as a coprocessor connecting via the GPIF II interface to an application processor (see **Figure 2**) and operates as a subsystem providing SuperSpeed USB connectivity to the application processor.

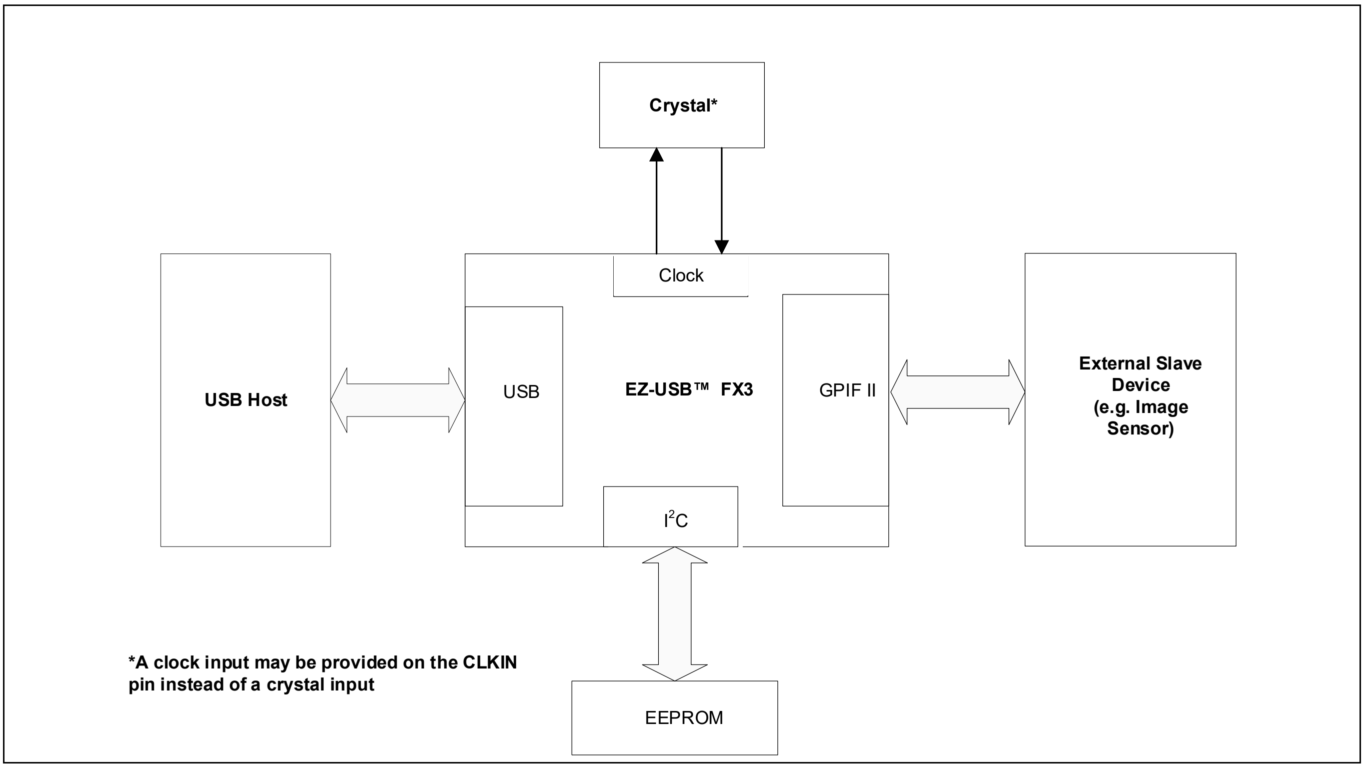


Figure 1 **EZ-USB FX3 as main processor**

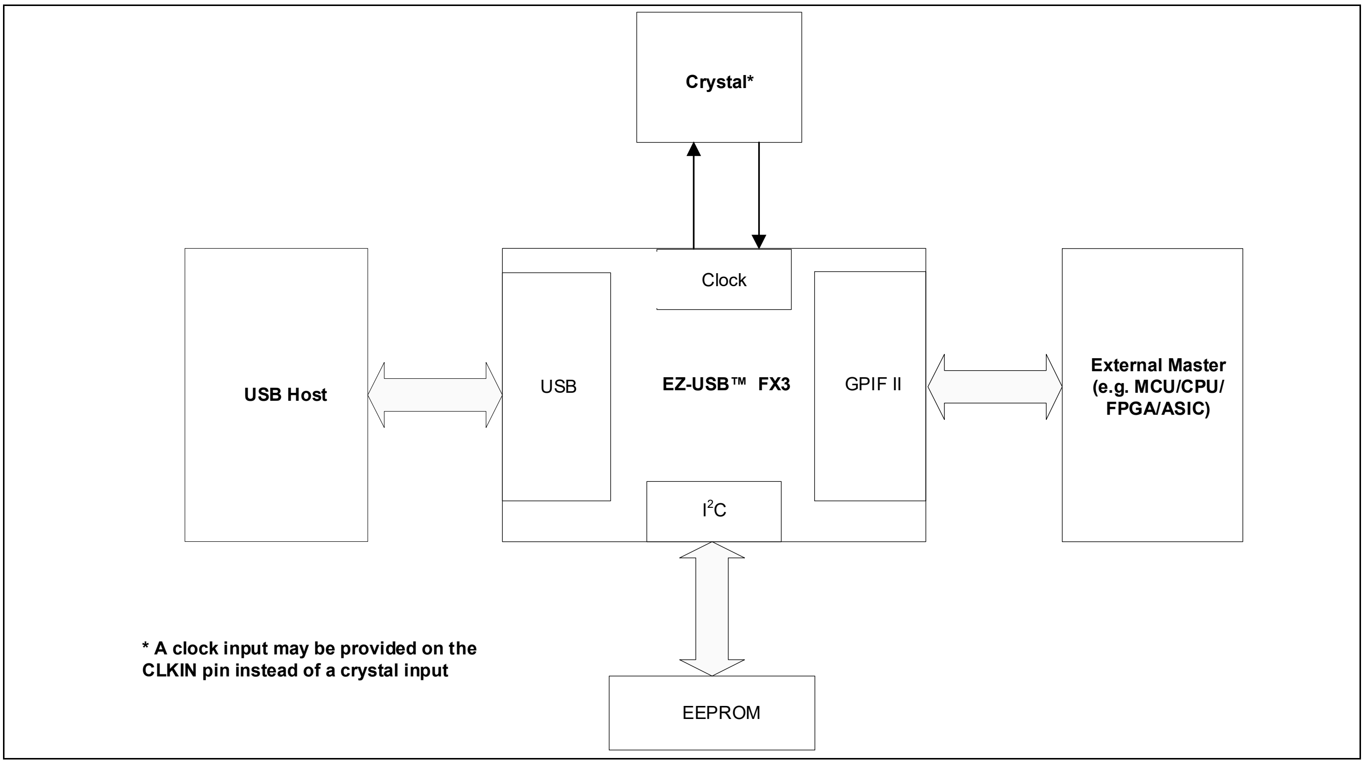


Figure 2 EZ-USB FX3 as a coprocessor

3 USB interface

FX3 complies with the following specifications and supports the following features:

- Supports USB peripheral functionality compliant with USB 3.2 Specification Revision 1.0 and is also backward compatible with the USB 2.0 Specification.
- FX3 Hi-Speed parts (CYUSB201X) only support USB 2.0.
- Complies with OTG Supplement Revision 2.0. It supports high-speed, full-speed, and low-speed OTG dual-role device capability. As a peripheral, FX3 is capable of SuperSpeed, high-speed, and full-speed. As a host, it is capable of high-speed, full-speed, and low-speed.
- Supports Carkit Pass-Through UART functionality on USB D+/D– lines based on the CEA-936A specification.
- Supports 16 IN and 16 OUT endpoints.
- Supports USB Attached SCSI (UAS) device-class to optimize mass-storage access performance.
- As a USB peripheral, application examples show that the FX3 supports UAS, USB Video Class (UVC), and Mass Storage Class (MSC) USB peripheral classes. All other device classes can be supported by customer firmware; a template example is provided as a starting point.
- As an OTG host, application examples show that FX3 supports MSC and HID device classes.

Note When the USB port is not in use, disable the PHY and transceiver to save power.

3.1 OTG

FX3 is compliant with the OTG Specification Revision 2.0. In OTG mode, FX3 supports both A and B device modes and supports Control, Interrupt, Bulk, and Isochronous data transfers.

FX3 requires an external charge pump (either standalone or integrated into a PMIC) to power VBUS in the OTG A-device mode.

The Target Peripheral List for OTG host implementation consists of MSC- and HID-class devices.

FX3 does not support Attach Detection Protocol (ADP).

3.1.1 OTG connectivity

In OTG mode, FX3 can be configured to be an A, B, or dual-role device. It can connect to the following:

- ACA device
- Targeted USB peripheral
- SRP-capable USB peripheral
- HNP-capable USB peripheral
- OTG host
- HNP-capable host
- OTG device

3.2 ReNumeration

Because of FX3's soft configuration, one chip can take on the identities of multiple distinct USB devices.

When first plugged into USB, FX3 enumerates automatically with the Infineon Vendor ID (0x04B4) and downloads firmware and USB descriptors over the USB interface. The downloaded firmware executes an electrical disconnect and connect. FX3 enumerates again, this time as a device defined by the downloaded information. This patented two-step process, called ReNumeration, happens instantly when the device is plugged in.

3.3 VBUS overvoltage protection

The maximum input voltage on FX3's VBUS pin is 6 V. A charger can supply up to 9 V on VBUS. In this case, an external overvoltage protection (OVP) device is required to protect FX3 from damage on VBUS. **Figure 3** shows the system application diagram with an OVP device connected on VBUS. Refer to **Table 8** for the operating range of VBUS and VBATT.

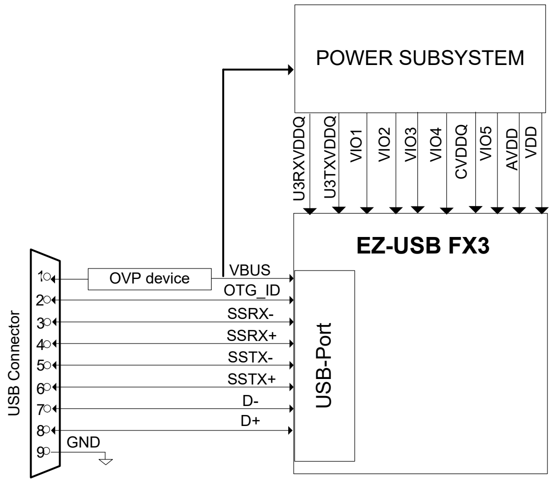


Figure 3 System diagram with OVP device for VBUS

3.4 Carkit UART Mode

The USB interface supports the Carkit UART mode (UART over D+/D–) for non-USB serial data transfer. This mode is based on the CEA-936A specification.

In the Carkit UART mode, the output signaling voltage is 3.3 V. When configured for the Carkit UART mode, TXD of UART (output) is mapped to the D– line, and RXD of UART (input) is mapped to the D+ line.

In the Carkit UART mode, FX3 disables the USB transceiver and D+ and D– pins serve as pass-through pins to connect to the UART of the host processor. The Carkit UART signals may be routed to the GPIF II interface or to GPIO[48] and GPIO[49], as shown in **Figure 4**.

In this mode, FX3 supports a rate of up to 9600 bps.

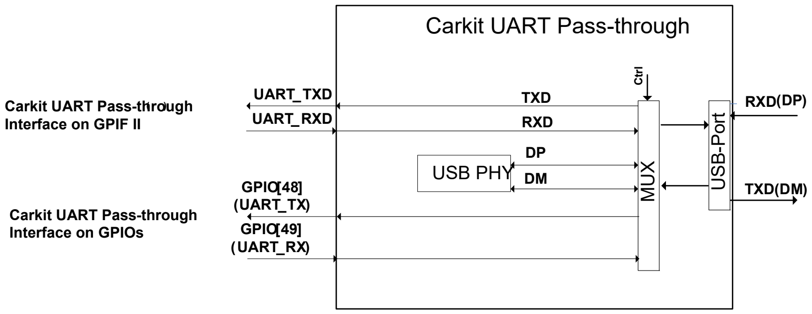


Figure 4 Carkit UART Pass-through block diagram

4 GPIF II

The high-performance GPIF II interface enables functionality similar to, but more advanced than, FX2LP's GPIF and Slave FIFO interfaces.

The GPIF II is a programmable state machine that enables a flexible interface that may function either as a master or slave in industry-standard or proprietary interfaces. Both parallel and serial interfaces may be implemented with GPIF II.

Here is a list of GPIF II features:

- Functions as master or slave
- Provides 256 firmware programmable states
- Supports 8-bit, 16-bit, 24-bit, and 32-bit parallel data bus
- Enables interface frequencies up to 100 MHz
- Supports 14 configurable control pins when a 32- bit data bus is used. All control pins can be either input/output or bidirectional.
- Supports 16 configurable control pins when a 16/8 data bus is used. All control pins can be either input/output or bi-directional.

GPIF II state transitions are based on control input signals. The control output signals are driven as a result of the GPIF II state transitions. The INT# output signal can be controlled by GPIF II. Refer to the GPIFII Designer tool. The GPIF II state machine's behavior is defined by a GPIF II descriptor. The GPIF II descriptor is designed such that the required interface specifications are met. 8 KB of memory (separate from the 256/512 KB of embedded SRAM) is dedicated to the GPIF II waveform where the GPIF II descriptor is stored in a specific format.

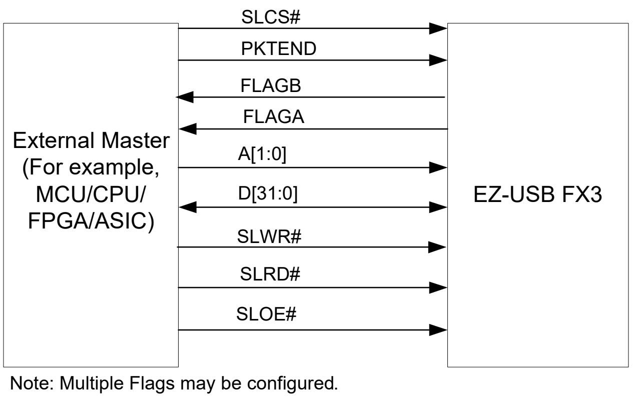
Infineon's GPIFII Designer Tool enables fast development of GPIF II descriptors and includes examples for common interfaces.

Example implementations of GPIF II are the asynchronous slave FIFO and synchronous slave FIFO interfaces.

4.0.1 Slave FIFO interface

The Slave FIFO interface signals are shown in **Figure 5**. This interface allows an external processor to directly access up to four buffers internal to FX3. Further details of the Slave FIFO interface are described on page 41.

Note Access to all 32 buffers is also supported over the slave FIFO interface. For details, contact Infineon applications support.



Note: Multiple Flags may be configured.

Figure 5 **Slave FIFO interface**

5 CPU

FX3 has an on-chip 32-bit, 200-MHz ARM926EJ-S core CPU. The core has direct access to 16 KB of instruction tightly coupled memory (TCM) and 8 KB of Data TCM. The ARM926EJ-S core provides a JTAG interface for firmware debugging.

FX3 offers the following advantages:

- Integrates 256/512 KB of embedded SRAM for code and data and 8 KB of instruction cache and data cache.
- Implements efficient and flexible DMA connectivity between the various peripherals (such as, USB, GPIF II, I^{2}S, SPI, UART, I^{2}C), requiring firmware only to configure data accesses between peripherals, which are then managed by the DMA fabric.
- Allows easy application development using industry-standard development tools for ARM926EJ-S.

Examples of the FX3 firmware are available with the Infineon EZ-USB FX3 Development Kit.

6 JTAG interface

FX3’s JTAG interface has a standard five-pin interface to connect to a JTAG debugger in order to debug firmware through the CPU-core’s on-chip-debug circuitry.

Industry-standard debugging tools for the ARM926EJ-S core can be used for the FX3 application development.

For ARM JTAG access, TCK frequency should not be more than 1/6 of the CPU clock frequency.

7 Other interfaces

FX3 supports the following serial peripherals:

- SPI
- UART
- I^2C
- I^2S

The SPI, UART, and I^2S interfaces are multiplexed on the serial peripheral port.

Table 7 shows details of how these interfaces are multiplexed. Note that when GPIF II is configured for a 32-bit data bus width (CYUSB3012 and CYUSB3014), then the SPI interface is not available.

7.1 SPI interface

FX3 supports an SPI Master interface on the Serial Peripherals port. The maximum operation frequency is 33 MHz.

The SPI controller supports four modes of SPI communication (see **"SPI timing specification"** on page 63 for details on the modes) with the Start-Stop clock. This controller is a single-master controller with a single automated SSN control. It supports transaction sizes ranging from four bits to 32 bits.

7.2 UART interface

The UART interface of FX3 supports full-duplex communication. It includes the signals noted in **Table 1**.

Table 1 UART interface signals

Signal	Description
TX	Output signal
RX	Input signal
CTS	Flow control
RTS	Flow control

The UART is capable of generating a range of baud rates, from 300 bps to 4608 Kbps, selectable by the firmware. If flow control is enabled, then FX3's UART only transmits data when the CTS input is asserted. In addition to this, FX3's UART asserts the RTS output signal, when it is ready to receive data.

7.3 I^2C interface

FX3's I^2C interface is compatible with the I^2C Bus Specification Revision 3. This I^2C interface is capable of operating only as I^2C master; therefore, it may be used to communicate with other I^2C slave devices. For example, FX3 may boot from an EEPROM connected to the I^2C interface, as a selectable boot option.

FX3's I^2C Master Controller also supports multi-master mode functionality.

The power supply for the I^2C interface is VIO5, which is a separate power domain from the other serial peripherals. This gives the I^2C interface the flexibility to operate at a different voltage than the other serial interfaces.

The I^2C controller supports bus frequencies of 100 kHz, 400 kHz, and 1 MHz. When VIO5 is 1.2 V, the maximum operating frequency supported is 100 kHz. When VIO5 is 1.8 V, 2.5 V, or 3.3 V, the operating frequencies supported are 400 kHz and 1 MHz. The I^2C controller supports clock-stretching to enable slower devices to exercise flow control.

The I^2C interface's SCL and SDA signals require external pull-up resistors. The pull-up resistors must be connected to VIO5.

7.4 I^{2}S interface

FX3 has an I^{2}S port to support external audio codec devices. FX3 functions as I^{2}S Master as transmitter only. The I^{2}S interface consists of four signals: clock line (I2S_CLK), serial data line (I2S_SD), word select line (I2S_WS), and master system clock (I2S_MCLK). FX3 can generate the system clock as an output on I2S_MCLK or accept an external system clock input on I2S_MCLK.

The sampling frequencies supported by the I^{2}S interface are 8 kHz, 16 kHz, 32 kHz, 44.1 kHz, 48 kHz, 96 kHz and 192 kHz.

8 Boot options

FX3 can load boot images from various sources, selected by the configuration of the PMODE pins. Following are the FX3 boot options:

- Boot from USB
- Boot from I^{2}C
- Boot from SPI
  - Infineon SPI Flash parts supported are S25FS064S (64-Mbit), S25FS128S (128-Mbit) and S25LFL064L (64-Mbit).
  - W25Q32FW (32-Mbit) is also supported.
- Boot from GPIF II Sync ADMux mode

Table 2 FX3 booting options

PMODE[2:0][1]	Boot from
F00	Sync ADMux (16-bit)
F11	USB boot
F1F	I^{2}C, On failure, USB boot is enabled
1FF	I^{2}C only
0F1	SPI, On failure, USB boot is enabled

9 Reset

9.1 Hard reset

A hard reset is initiated by asserting the Reset# pin on FX3. The specific reset sequence and timing requirements are detailed in **Figure 29** and **Table 23**. All I/Os are tristated during a hard reset. Note however, that the on-chip bootloader has control after a hard reset and it will configure I/O signals depending on the selected boot mode; see AN76405 - EZ-USB® FX3™ Boot Options for more details.

9.2 Soft reset

In a soft reset, the processor sets the appropriate bits in the PP_INIT control register. There are two types of soft reset:

- CPU reset – The CPU program counter is reset. Firmware does not need to be reloaded following a CPU reset.
- Whole device reset – This reset is identical to hard reset.
- The firmware must be reloaded following a whole device reset.

Note

1. F indicates floating.

10 Clocking

FX3 allows either a crystal to be connected between the XTALIN and XTALOUT pins or an external clock to be connected at the CLKIN pin. The XTALIN, XTALOUT, CLKIN, and CLKIN_32 pins can be left unconnected if they are not used.

Crystal frequency supported is 19.2 MHz, while the external clock frequencies supported are 19.2, 26, 38.4, and 52 MHz.

FX3 has an on-chip oscillator circuit that uses an external 19.2-MHz (±100 ppm) crystal (when the crystal option is used). An appropriate load capacitance is required with a crystal. Refer to the specification of the crystal used to determine the appropriate load capacitance. The FSLC[2:0] pins must be configured appropriately to select the crystal- or clock-frequency option. The configuration options are shown in **Table 3**.

Clock inputs to FX3 must meet the phase noise and jitter requirements specified in **Table 4**.

The input clock frequency is independent of the clock and data rate of the FX3 core or any of the device interfaces. The internal PLL applies the appropriate clock multiply option depending on the input frequency.

Table 3 **Crystal/clock frequency selection**

FSLC[2]	FSLC[1]	FSLC[0]	Crystal/clock frequency
0	0	0	19.2-MHz crystal
1	0	0	19.2-MHz input CLK
1	0	1	26-MHz input CLK
1	1	0	38.4-MHz input CLK
1	1	1	52-MHz input CLK

Table 4 **FX3 input clock specifications**

Parameter	Description	Specification		Units
		Min	Max	
Phase noise	100-Hz offset	–	–75	dB
	1-kHz offset	–	–104	
	10-kHz offset	–	–120	
	100-kHz offset	–	–128	
	1-MHz offset	–	–130	
Maximum frequency deviation	–	–	150	ppm
Duty cycle	–	30	70	%
Overshoot	–	–	3	
Undershoot	–	–	–3	
Rise time/fall time	–	–	3	ns

10.1 32-kHz watchdog timer clock input

FX3 includes a watchdog timer. The watchdog timer can be used to interrupt the ARM926EJ-S core, automatically wake up the FX3 in Standby mode, and reset the ARM926EJ-S core. The watchdog timer runs a 32-kHz clock, which may be optionally supplied from an external source on a dedicated FX3 pin.

The firmware can disable the watchdog timer. Requirements for the optional 32-kHz clock input are listed in **Table 5**.

Table 5 32-kHz clock input requirements

Parameter	Min	Max	Units
Duty cycle	40	60	%
Frequency deviation	–	±200	ppm
Rise time/fall time	–	200	ns

11 Power

FX3 has the following power supply domains:

- **IO_VDDQ**: This is a group of independent supply domains for digital I/Os. The voltage level on these supplies is 1.8 V to 3.3 V. FX3 provides six independent supply domains for digital I/Os listed as follows (see **Table 7** for details on each of the power domain signals):
  - VIO1: GPIF II I/O
  - VIO2: IO2
  - VIO3: IO3
  - VIO4: UART-/SPI/I^2S
  - VIO5: I^2C and JTAG (supports 1.2 V to 3.3 V)
  - **CVDDQ**: This is the supply voltage for clock and reset I/O. It should be either 1.8 V or 3.3 V based on the voltage level of the CLKIN signal.
  - **V_{DD}**: This is the supply voltage for the logic core. The nominal supply-voltage level is 1.2 V. This supplies the core logic circuits. The same supply must also be used for the following:
    - **AVDD**: This is the 1.2-V supply for the PLL, crystal oscillator, and other core analog circuits.
    - **U3TXVDDQ/U3RXVDDQ**: These are the 1.2-V supply voltages for the USB 3.0 interface.
- **VBATT/VBUS**: This is the 3.2-V to 6-V battery power supply for the USB I/O and analog circuits. This supply powers the USB transceiver through FX3's internal voltage regulator. VBATT is internally regulated to 3.3 V.

Note:

No specific power-up sequence for FX3 power domains. Minimum power on reset time of 1 ms should be met and the power domains must be stable for FX3 operation.

11.1 Power Modes

FX3 supports the following power modes:

- Normal mode: This is the full-functional operating mode. The internal CPU clock and the internal PLLs are enabled in this mode.
  - Normal operating power consumption does not exceed the sum of I_{CC} Core max and I_{CC} USB max (see **Table 8** for current consumption specifications).
  - The I/O power supplies VIO2, VIO3, VIO4, and VIO5 can be turned off when the corresponding interface is not in use. VIO1 cannot be turned off at any time if the GPIF II interface is used in the application.
- Low-power modes (see **Table 6**):
  - Suspend mode with USB 3.0 PHY enabled (L1)
  - Suspend mode with USB 3.0 PHY disabled (L2)
  - Standby mode (L3)
  - Core power-down mode (L4)

Table 6 Entry and Exit methods for Low-Power Modes

Low-Power Mode	Characteristics	Methods of Entry	Methods of Exit
Suspend Mode with USB 3.0 PHY Enabled (L1)	• The power consumption in this mode does not exceed ISB_1 • USB 3.0 PHY is enabled and is in U3 mode (one of the suspend modes defined by the USB 3.0 specification). This one block alone is operational with its internal clock while all other clocks are shut down • All I/Os maintain their previous state • Power supply for the wakeup source and core power must be retained. All other power domains can be turned on/off individually • The states of the configuration registers, buffer memory, and all internal RAM are maintained • All transactions must be completed before FX3 enters Suspend mode (state of outstanding transactions are not preserved) • The firmware resumes operation from where it was suspended (except when woken up by RESET# assertion) because the program counter does not reset	• Firmware executing on ARM926EJ-S core can put FX3 into suspend mode. For example, on USB suspend condition, firmware may decide to put FX3 into suspend mode • External Processor, through the use of mailbox registers, can put FX3 into suspend mode	• D+ transitioning to low or high • D– transitioning to low or high • Impedance change on OTG_ID pin • Resume condition on SSRX± • Detection of VBUS • Level detect on UART_CTS (programmable polarity) • GPIF II interface assertion of CTL[0] • Assertion of RESET#
Suspend Mode with USB 3.0 PHY Disabled (L2)	• The power consumption in this mode does not exceed ISB_2 • USB 3.0 PHY is disabled and the USB interface is in suspend mode • The clocks are shut off. The PLLs are disabled • All I/Os maintain their previous state • USB interface maintains the previous state • Power supply for the wakeup source and core power must be retained. All other power domains can be turned on/off individually • The states of the configuration registers, buffer memory and all internal RAM are maintained • All transactions must be completed before FX3 enters Suspend mode (state of outstanding transactions are not preserved) • The firmware resumes operation from where it was suspended (except when woken up by RESET# assertion) because the program counter does not reset	• Firmware executing on ARM926EJ-S core can put FX3 into suspend mode. For example, on USB suspend condition, firmware may decide to put FX3 into suspend mode • External Processor, through the use of mailbox registers can put FX3 into suspend mode	• D+ transitioning to low or high • D– transitioning to low or high • Impedance change on OTG_ID pin • Detection of VBUS • Level detect on UART_CTS (programmable polarity) • GPIF II interface assertion of CTL[0] • Assertion of RESET#

Table 6 **Entry and Exit methods for Low-Power Modes** (continued)

Low-Power Mode	Characteristics	Methods of Entry	Methods of Exit
Standby Mode (L3)	• The power consumption in this mode does not exceed ISB3 • All configuration register settings and program/data RAM contents are preserved. However, data in the buffers or other parts of the data path, if any, is not guaranteed. Therefore, the external processor should take care that the data needed is read before putting FX3 into this Standby Mode • The program counter is reset after waking up from Standby • GPIO pins maintain their configuration • Crystal oscillator is turned off • Internal PLL is turned off • USB transceiver is turned off • ARM926EJ-S core is powered down. Upon wakeup, the core re-starts and runs the program stored in the program/data RAM • Power supply for the wakeup source and core power must be retained. All other power domains can be turned on/off individually	• Firmware executing on ARM926EJ-S core or external processor configures the appropriate register	• Detection of VBUS • Level detect on UART_CTS (Programmable Polarity) • GPIF II interface assertion of CTL[0] • Assertion of RESET#
Core Power Down Mode (L4)	• The power consumption in this mode does not exceed ISB_4 • Core power is turned off • All buffer memory, configuration registers, and the program RAM do not maintain state. After exiting this mode, reload the firmware • In this mode, all other power domains can be turned on/off individually	• Turn off V_{DD}	• Reapply V_{DD} • Assertion of RESET#

Note: The power consumption depends on how the FX3 IOs are utilized in the application. Refer to **KBA85505** to estimate the current consumption by different power domains (VIO1–VIO5).

12 Digital I/Os

FX3 has internal firmware-controlled pull-up or pull-down resistors on all digital I/O pins. An internal 50-kΩ resistor pulls the pins high, while an internal 10-kΩ resistor pulls the pins low to prevent them from floating. The I/O pins may have the following states:

- Tristated (High-Z)
- Weak pull-up (via internal 50 kΩ)
- Pull-down (via internal 10 kΩ)
- Hold (I/O hold its value) when in low-power modes
- The JTAG TDI, TMS, and TRST# signals have fixed 50-kΩ internal pull-ups, and the TCK signal has a fixed 10-kΩ pull-down resistor.

All unused I/Os should be pulled high by using the internal pull-up resistors. All unused outputs should be left floating. All I/Os can be driven at full-strength, three-quarter strength, half-strength, or quarter-strength. These drive strengths are configured separately for each interface.

13 GPIOs

EZ-USB enables a flexible pin configuration both on the GPIF II and the serial peripheral interfaces. Any unused control pins (except CTL[15]) on the GPIF II interface can be used as GPIOs. Similarly, any unused pins on the serial peripheral interfaces may be configured as GPIOs. See **“Pin configurations”** on page 27 for pin configuration options.

All GPIF II and GPIO pins support an external load of up to 16 pF for every pin.

EMI

FX3 meets EMI requirements outlined by FCC 15B (USA) and EN55022 (Europe) for consumer electronics. FX3 can tolerate EMI, conducted by the aggressor, outlined by these specifications and continue to function as expected.

14 System-level ESD

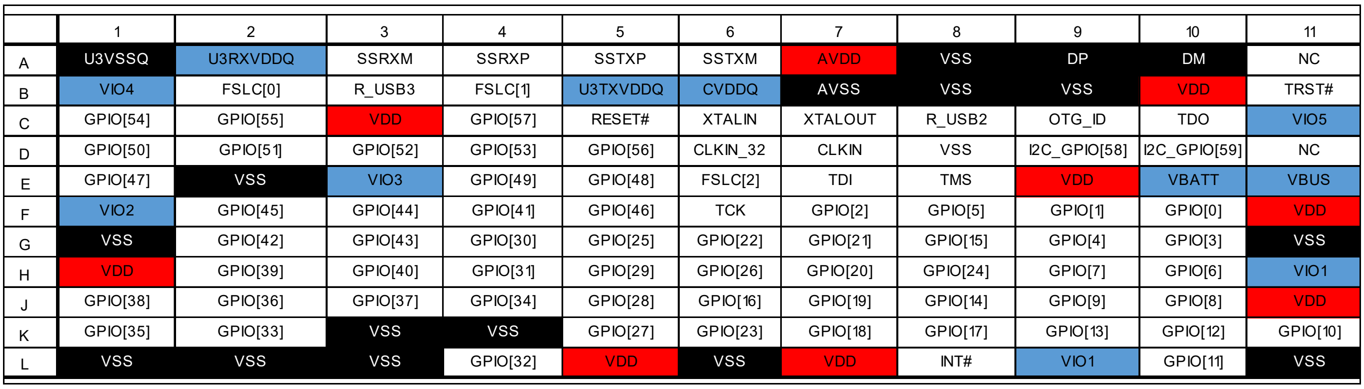
FX3 has built-in ESD protection on the D+, D–, and GND pins on the USB interface. The ESD protection levels provided on these ports are:

- ±2.2-kV human body model (HBM) based on JESD22-A114 Specification
- ±6-kV contact discharge and ±8-kV air gap discharge based on IEC61000-4-2 level 3A
- ± 8-kV Contact Discharge and ±15-kV Air Gap Discharge based on IEC61000-4-2 level 4C.

This protection ensures the device continues to function after ESD events up to the levels stated in this section.

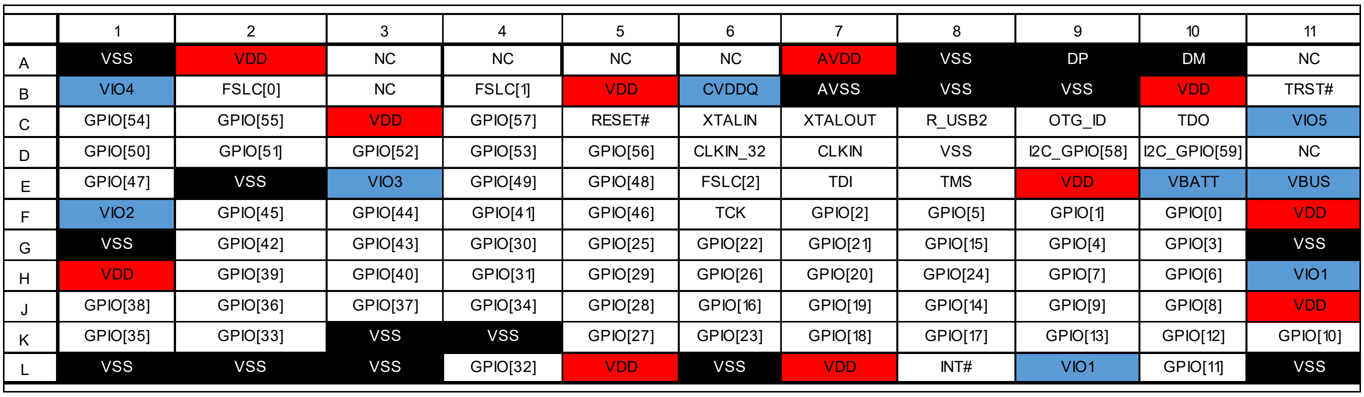
The SSRX+, SSRX–, SSTX+, and SSTX– pins only have up to ±2.2-kV HBM internal ESD protection.

15 Pin configurations



	1	2	3	4	5	6	7	8	9	10	11
A	U3VSSQ	U3RXVDDQ	SSRXM	SSRXP	SSTXP	SSTXM	AVDD	VSS	DP	DM	NC
B	VIO4	FSLC[0]	R_USB3	FSLC[1]	U3TXVDDQ	CVDDQ	AVSS	VSS	VSS	VDD	TRST#
C	GPIO[54]	GPIO[55]	VDD	GPIO[57]	RESET#	XTALIN	XTALOUT	R_USB2	OTG_ID	TDO	VIO5
D	GPIO[50]	GPIO[51]	GPIO[52]	GPIO[53]	GPIO[56]	CLKIN_32	CLKIN	VSS	I2C_GPIO[58]	I2C_GPIO[59]	NC
E	GPIO[47]	VSS	VIO3	GPIO[49]	GPIO[48]	FSLC[2]	TDI	TMS	VDD	VBATT	VBUS
F	VIO2	GPIO[45]	GPIO[44]	GPIO[41]	GPIO[46]	TCK	GPIO[2]	GPIO[5]	GPIO[1]	GPIO[0]	VDD
G	VSS	GPIO[42]	GPIO[43]	GPIO[30]	GPIO[25]	GPIO[22]	GPIO[21]	GPIO[15]	GPIO[4]	GPIO[3]	VSS
H	VDD	GPIO[39]	GPIO[40]	GPIO[31]	GPIO[29]	GPIO[26]	GPIO[20]	GPIO[24]	GPIO[7]	GPIO[6]	VIO1
J	GPIO[38]	GPIO[36]	GPIO[37]	GPIO[34]	GPIO[28]	GPIO[16]	GPIO[19]	GPIO[14]	GPIO[9]	GPIO[8]	VDD
K	GPIO[35]	GPIO[33]	VSS	VSS	GPIO[27]	GPIO[23]	GPIO[18]	GPIO[17]	GPIO[13]	GPIO[12]	GPIO[10]
L	VSS	VSS	VSS	GPIO[32]	VDD	VSS	VDD	INT#	VIO1	GPIO[11]	VSS

Figure 6 **FX3 121-ball BGA ball map (Top view)**



	1	2	3	4	5	6	7	8	9	10	11
A	VSS	VDD	NC	NC	NC	NC	AVDD	VSS	DP	DM	NC
B	VIO4	FSLC[0]	NC	FSLC[1]	VDD	CVDDQ	AVSS	VSS	VSS	VDD	TRST#
C	GPIO[54]	GPIO[55]	VDD	GPIO[57]	RESET#	XTALIN	XTALOUT	R_USB2	OTG_ID	TDO	VIO5
D	GPIO[50]	GPIO[51]	GPIO[52]	GPIO[53]	GPIO[56]	CLKIN_32	CLKIN	VSS	I2C_GPIO[58]	I2C_GPIO[59]	NC
E	GPIO[47]	VSS	VIO3	GPIO[49]	GPIO[48]	FSLC[2]	TDI	TMS	VDD	VBATT	VBUS
F	VIO2	GPIO[45]	GPIO[44]	GPIO[41]	GPIO[46]	TCK	GPIO[2]	GPIO[5]	GPIO[1]	GPIO[0]	VDD
G	VSS	GPIO[42]	GPIO[43]	GPIO[30]	GPIO[25]	GPIO[22]	GPIO[21]	GPIO[15]	GPIO[4]	GPIO[3]	VSS
H	VDD	GPIO[39]	GPIO[40]	GPIO[31]	GPIO[29]	GPIO[26]	GPIO[20]	GPIO[24]	GPIO[7]	GPIO[6]	VIO1
J	GPIO[38]	GPIO[36]	GPIO[37]	GPIO[34]	GPIO[28]	GPIO[16]	GPIO[19]	GPIO[14]	GPIO[9]	GPIO[8]	VDD
K	GPIO[35]	GPIO[33]	VSS	VSS	GPIO[27]	GPIO[23]	GPIO[18]	GPIO[17]	GPIO[13]	GPIO[12]	GPIO[10]
L	VSS	VSS	VSS	GPIO[32]	VDD	VSS	VDD	INT#	VIO1	GPIO[11]	VSS

Figure 7 **FX3 Hi-Speed 121-ball BGA ball map (Top view)**

Note: A2 and C3 need not be connected for FX3 Hi-Speed part.

16 Pin description

Table 7 CYUSB3011, CYUSB3012, CYUSB3013, CYUSB3014 and CYUSB2014 pin list

BGA	Power domain	I/O	Name	Description	
				GPIF II interface	**Slave FIFO interface** [2]
F10	VIO1	I/O	GPIO[0]	DQ[0]	DQ[0]
F9	VIO1	I/O	GPIO[1]	DQ[1]	DQ[1]
F7	VIO1	I/O	GPIO[2]	DQ[2]	DQ[2]
G10	VIO1	I/O	GPIO[3]	DQ[3]	DQ[3]
G9	VIO1	I/O	GPIO[4]	DQ[4]	DQ[4]
F8	VIO1	I/O	GPIO[5]	DQ[5]	DQ[5]
H10	VIO1	I/O	GPIO[6]	DQ[6]	DQ[6]
H9	VIO1	I/O	GPIO[7]	DQ[7]	DQ[7]
J10	VIO1	I/O	GPIO[8]	DQ[8]/A0 [3]	DQ[8]/A0 [3]
J9	VIO1	I/O	GPIO[9]	DQ[9]/A1 [3]	DQ[9]/A1 [3]
K11	VIO1	I/O	GPIO[10]	DQ[10]	DQ[10]
L10	VIO1	I/O	GPIO[11]	DQ[11]	DQ[11]
K10	VIO1	I/O	GPIO[12]	DQ[12]	DQ[12]
K9	VIO1	I/O	GPIO[13]	DQ[13]	DQ[13]
J8	VIO1	I/O	GPIO[14]	DQ[14] [4]	DQ[14] [4]
G8	VIO1	I/O	GPIO[15]	DQ[15] [4]	DQ[15] [4]
J6	VIO1	I/O	GPIO[16]	PCLK	CLK
K8	VIO1	I/O	GPIO[17]	CTL[0]	SLCS#
K7	VIO1	I/O	GPIO[18]	CTL[1]	SLWR#
J7	VIO1	I/O	GPIO[19]	CTL[2]	SLOE#
H7	VIO1	I/O	GPIO[20]	CTL[3]	SLRD#
G7	VIO1	I/O	GPIO[21]	CTL[4]	FLAGA
G6	VIO1	I/O	GPIO[22]	CTL[5]	FLAGB
K6	VIO1	I/O	GPIO[23]	CTL[6]	GPIO
H8	VIO1	I/O	GPIO[24]	CTL[7]	PKTEND#
G5	VIO1	I/O	GPIO[25]	CTL[8]	GPIO
H6	VIO1	I/O	GPIO[26]	CTL[9]	GPIO
K5	VIO1	I/O	GPIO[27]	CTL[10]	GPIO
J5	VIO1	I/O	GPIO[28]	CTL[11]	A1
H5	VIO1	I/O	GPIO[29]	CTL[12]	A0
G4	VIO1	I/O	GPIO[30]	PMODE[0]	PMODE[0]
H4	VIO1	I/O	GPIO[31]	PMODE[1]	PMODE[1]
L4	VIO1	I/O	GPIO[32]	PMODE[2]	PMODE[2]
L8	VIO1	I/O	INT#	INT#/CTL[15]	CTL[15]

Notes

2. Slave FIFO is an example configuration of GPIF II Interface. The Slave FIFO control signal assignments can be modified using GPIF-II designer tool.
3. For 8-bit data bus configuration, GPIO[8] and GPIO[9] act as address lines.
4. GPIF II can also be configured as a serial interface. The DQ[15] pin becomes a serial output and DQ[14] becomes a serial input in this mode.

Table 7 CYUSB3011, CYUSB3012, CYUSB3013, CYUSB3014 and CYUSB2014 pin list (continued)

BGA	Power domain	I/O	Name	Description					
				CYUSB3014 and CYUSB2014	CYUSB3011, CYUSB3012, CYUSB3013, CYUSB3014 and CYUSB2014				
				32-bit Data Bus	16-bit Data Bus + UART + SPI + I2S	16-bit Data Bus + UART + GPIO	16-bit Data Bus + SPI + GPIO	16-bit Data Bus + I2S + GPIO	GPIO only
K2	VIO2	I/O	GPIO[33]	DQ[16]	GPIO	GPIO	GPIO	GPIO	GPIO
J4	VIO2	I/O	GPIO[34]	DQ[17]	GPIO	GPIO	GPIO	GPIO	GPIO
K1	VIO2	I/O	GPIO[35]	DQ[18]	GPIO	GPIO	GPIO	GPIO	GPIO
J2	VIO2	I/O	GPIO[36]	DQ[19]	GPIO	GPIO	GPIO	GPIO	GPIO
J3	VIO2	I/O	GPIO[37]	DQ[20]	GPIO	GPIO	GPIO	GPIO	GPIO
J1	VIO2	I/O	GPIO[38]	DQ[21]	GPIO	GPIO	GPIO	GPIO	GPIO
H2	VIO2	I/O	GPIO[39]	DQ[22]	GPIO	GPIO	GPIO	GPIO	GPIO
H3	VIO2	I/O	GPIO[40]	DQ[23]	GPIO	GPIO	GPIO	GPIO	GPIO
F4	VIO2	I/O	GPIO[41]/A0 [5]	DQ[24]	GPIO	GPIO	GPIO	GPIO	GPIO
G2	VIO2	I/O	GPIO[42]/A1 [5]	DQ[25]	GPIO	GPIO	GPIO	GPIO	GPIO
G3	VIO2	I/O	GPIO[43]	DQ[26]	GPIO	GPIO	GPIO	GPIO	GPIO
F3	VIO2	I/O	GPIO[44]	DQ[27]	GPIO	GPIO	GPIO	GPIO	GPIO
F2	VIO2	I/O	GPIO[45]	GPIO	GPIO	GPIO	GPIO	GPIO	GPIO
F5	VIO3	I/O	GPIO[46]	DQ[28]	UART_RTS	GPIO	GPIO	GPIO	GPIO
E1	VIO3	I/O	GPIO[47]	DQ[29]	UART_CTS	GPIO	GPIO	GPIO	GPIO
E5	VIO3	I/O	GPIO[48]	DQ[30]	UART_TX	GPIO	GPIO	GPIO	GPIO
E4	VIO3	I/O	GPIO[49]	DQ[31]	UART_RX	GPIO	GPIO	GPIO	GPIO
D1	VIO3	I/O	GPIO[50]	I2S_CLK	I2S_CLK	GPIO	GPIO	GPIO	GPIO
D2	VIO3	I/O	GPIO[51]	I2S_SD	I2S_SD	GPIO	GPIO	GPIO	GPIO
D3	VIO3	I/O	GPIO[52]	I2S_WS	I2S_WS	GPIO	GPIO	GPIO	GPIO
D4	VIO4	I/O	GPIO[53]	UART_RTS	SPI_SCK	UART_RTS	SPI_SCK	GPIO	GPIO
C1	VIO4	I/O	GPIO[54]	UART_CTS	SPI_SSN	UART_CTS	SPI_SSN	I2S_CLK	GPIO
C2	VIO4	I/O	GPIO[55]	UART_TX	SPI_MISO	UART_TX	SPI_MISO	I2S_SD	GPIO
D5	VIO4	I/O	GPIO[56]	UART_RX	SPI_MOSI	UART_RX	SPI_MOSI	I2S_WS	GPIO
C4	VIO4	I/O	GPIO[57]	I2S_MCLK	I2S_MCLK	GPIO	GPIO	I2S_MCLK	GPIO
				USB Port					
				CYUSB301X			CYUSB201X		
A3	U3RXVDDQ	I	SSRXM	SSRX-			NC		
A4	U3RXVDDQ	I	SSRXP	SSRX+			NC		
A6	U3TXVDDQ	O	SSTXM	SSTX-			NC		
A5	U3TXVDDQ	O	SSTXP	SSTX+			NC		
B3	U3TXVDDQ	I/O	R_usb3	Precision resistor for USB 3.0 (Connect a 200 ±1% resistor between this pin and GND)			NC		
C9	VBUS/VBATT	I	OTG_ID	OTG_ID					
A9	VBUS/VBATT	I/O	DP	D+					
A10	VBUS/VBATT	I/O	DM	D–					
C8	VBUS/VBATT	I/O	R_usb2	Precision resistor for USB 2.0 (Connect a 6.04 k ±1% resistor between this pin and GND)					

Note

5. For 24-bit data bus configuration, GPIO[41] and GPIO[42] act as address lines.

Table 7 **CYUSB3011, CYUSB3012, CYUSB3013, CYUSB3014 and CYUSB2014 pin list** (continued)

BGA	Power domain	I/O	Name	Description
				Clock and Reset
B2	CVDDQ	I	FSLC[0]	FSLC[0]
C6	AVDD	I/O	XTALIN	XTALIN
C7	AVDD	I/O	XTALOUT	XTALOUT
B4	CVDDQ	I	FSLC[1]	FSLC[1]
E6	CVDDQ	I	FSLC[2]	FSLC[2]
D7	CVDDQ	I	CLKIN	CLKIN
D6	CVDDQ	I	CLKIN_32	CLKIN_32
C5	CVDDQ	I	RESET#	RESET#
				I2C and JTAG
D9	VIO5	I/O	I2C_GPIO[58]	I^{2}C_SCL
D10	VIO5	I/O	I2C_GPIO[59]	I^{2}C_SDA
E7	VIO5	I	TDI	TDI
C10	VIO5	O	TDO	TDO
B11	VIO5	I	TRST#	TRST#
E8	VIO5	I	TMS	TMS
F6	VIO5	I	TCK	TCK
D11	VIO5	O	O[60]	GPIO
				Power
E10		PWR	VBATT	
B10		PWR	VDD	
		PWR	VDD	
A1		PWR	U3VSSQ	
E11		PWR	VBUS	
D8		PWR	VSS	
H11		PWR	VIO1	
E2		PWR	VSS	
L9		PWR	VIO1	
G1		PWR	VSS	
		PWR	VIO1	
		PWR	VSS	
F1		PWR	VIO2	
G11		PWR	VSS	
		PWR	VIO2	
E3		PWR	VIO3	
L1		PWR	VSS	
B1		PWR	VIO4	
L6		PWR	VSS	
		PWR	VSS	
B6		PWR	CVDDQ	
B5		PWR	U3TXVDDQ	
A2		PWR	U3RXVDDQ	
C11		PWR	VIO5	
L11		PWR	VSS	
A7		PWR	AVDD	

Table 7 **CYUSB3011, CYUSB3012, CYUSB3013, CYUSB3014 and CYUSB2014 pin list** (continued)

BGA	Power domain	I/O	Name	Description
B7		PWR	AVSS	
C3		PWR	VDD	
B8		PWR	VSS	
E9		PWR	VDD	
B9		PWR	VSS	
F11		PWR	VDD	
		PWR	VSS	GND
		PWR	VDD	
		PWR	VSS	GND
		PWR	VSS	GND
H1		PWR	VDD	
L7		PWR	VDD	
J11		PWR	VDD	
L5		PWR	VDD	
K4		PWR	VSS	
L3		PWR	VSS	
K3		PWR	VSS	
L2		PWR	VSS	
A8		PWR	VSS	
			NC	No Connect
A11			NC	No Connect

17 Electrical specifications

17.1 Absolute maximum ratings

Exceeding maximum ratings may shorten the useful life of the device.

Storage temperature .... –65°C to +150°C

Ambient temperature with
power supplied (Industrial) .... –40°C to +85°C

Ambient temperature with
power supplied (Commercial) .... 0°C to +70°C

Supply voltage to ground potential
V_{DD}, A_{VDDQ} ....1.25 V

V_{IO1},V_{IO2}, V_{IO3}, V_{IO4}, V_{IO5} ....3.6 V

$U3TX_{VDDQ}$, $U3RX_{VDDQ}$ ....1.25 V

DC input voltage to any input pin ....V_{CC} + 0.3 V

DC voltage applied to
outputs in high Z state .... V_{CC} + 0.3 V

(VCC is the corresponding I/O voltage)

Static discharge voltage ESD protection levels:

- ± 2.2-kV HBM based on JESD22-A114
- Additional ESD protection levels on D+, D–, and GND pins, and serial peripheral pins
- ± 6-kV contact discharge, ± 8-kV air gap discharge based on IEC61000-4-2 level 3A, ± 8-kV contact discharge, and ± 15-kV air gap discharge based on IEC61000-4-2 level 4C

Latch-up current .... 180 mA

Maximum output short-circuit current
for all I/Os (cumulative) .... –100 mA

Maximum output current per I/O
(source or sink) .... 20 mA

17.2 Operating conditions

T_A (ambient temperature under bias)

Industrial .... –40°C to +85°C

Commercial .... 0°C to +70°C

V_{DD}, A_{VDDQ}, $U3TX_{VDDQ}$, $U3RX_{VDDQ}$
Supply voltage ....1.15 V to 1.25 V

V_{BATT} supply voltage ....3.2 V to 6 V

V_{IO1}, V_{IO2}, V_{IO3}, V_{IO4}, C_{VDDQ}
Supply voltage ....1.7 V to 3.6 V

V_{IO5} supply voltage .... 1.15 V to 3.6 V

17.3 DC specifications

Table 8 **DC specifications**

Parameter	Description	Min	Max	Units	Notes
V_{DD}	Core voltage supply	1.15	1.25	V	1.2-V typical
A_{VDD}	Analog voltage supply	1.15	1.25	V	1.2-V typical
V_{IO1}	GPIF II I/O power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{IO2}	IO2 power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{IO3}	IO3 power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{IO4}	UART/SPI/I2S power supply domain	1.7	3.6	V	1.8-, 2.5-, and 3.3-V typical
V_{BATT}	USB voltage supply	3.2	6	V	3.7-V typical
V_{BUS}	USB voltage supply	4.0	6	V	5-V typical
$U3TX_{VDDQ}$	USB 3.0 1.2-V supply	1.15	1.25	V	1.2-V typical. A 22-µF bypass capacitor is required on this power supply. N/A for CYUSB201X
$U3RX_{VDDQ}$	USB 3.0 1.2-V supply	1.15	1.25	V	1.2-V typical. A 22-µF bypass capacitor is required on this power supply. N/A for CYUSB201X
C_{VDDQ}	Clock voltage supply	1.7	3.6	V	1.8-, 3.3-V typical
V_{IO5}	I^2C and JTAG voltage supply	1.15	3.6	V	1.2-, 1.8-, 2.5-, and 3.3-V typical
V_{IH1}	Input HIGH voltage 1	$0.625 \times V_{CC}$	$V_{CC} + 0.3$	V	For $2.0\ V \le V_{CC} \le 3.6\ V$ (except USB port). VCC is the corresponding I/O voltage supply.
V_{IH2}	Input HIGH voltage 2	$V_{CC} - 0.4$	$V_{CC} + 0.3$	V	For $1.7\ V \le V_{CC} \le 2.0\ V$ (except USB port). VCC is the corresponding I/O voltage supply.
V_{IL}	Input LOW voltage	–0.3	$0.25 \times V_{CC}$	V	VCC is the corresponding I/O voltage supply.
V_{OH}	Output HIGH voltage	$0.9 \times V_{CC}$	–	V	I_{OH} (max) = –100 µA tested at quarter drive strength. VCC is the corresponding I/O voltage supply. Refer to**Table 9** for values of I_{OH} at various drive strength and VCC.
V_{OL}	Output LOW voltage	–	$0.1 \times V_{CC}$	V	I_{OL} (min) = +100 µA tested at quarter drive strength. VCC is the corresponding I/O voltage supply. Refer to **Table 9** for values of I_{OL} measured at various drive strength and VCC.
I_{IX}	Input leakage current for all pins except SSTXP/SSXM/SSRXP/SSRXM	–1	1	µA	All I/O signals held at V_{DDQ} (For I/Os with a pull-up or pull-down resistor connected, the leakage current increases by V_{DDQ}/R_{pu} or V_{DDQ}/R_{PD})

Table 8 DC specifications (continued)

Parameter	Description	Min	Max	Units	Notes
I_{OZ}	Output High-Z leakage current for all pins except SSTXP/ SSXM/ SSRXP/SSRXM	–1	1	µA	All I/O signals held at V_{DDQ}
I_{CC} Core	Core and analog voltage operating current	–	200	mA	Total current through A_{VDD}, V_{DD}
I_{CC} USB [6]	USB voltage supply operating current	–	60 [6]	mA	–
I_{SB1}	Total suspend current during suspend mode with USB 3.0 PHY enabled (L1)	–	–	mA	Core current: 1.5 mA I/O current: 20 µA USB current: 2 mA For typical PVT (typical silicon, all power supplies at their respective nominal levels at 25°C)
I_{SB2}	Total suspend current during suspend mode with USB 3.0 PHY disabled (L2)	–	–	mA	Core current: 250 µA I/O current: 20 µA USB current: 1.2 mA For typical PVT (Typical silicon, all power supplies at their respective nominal levels at 25°C)
I_{SB3}	Total standby current during standby mode (L3)	–	–	µA	Core current: 60 µA I/O current: 20 µA USB current: 40 µA For typical PVT (typical silicon, all power supplies at their respective nominal levels at 25°C)
I_{SB4}	Total standby current during core power-down mode (L4)	–	–	µA	Core current: 0 µA I/O current: 20 µA USB current: 40 µA For typical PVT (typical silicon, all power supplies at their respective nominal levels at 25°C)
V_{RAMP}	Voltage ramp rate on core and I/O supplies	0.2	50	V/ms	Voltage ramp must be monotonic
V_N	Noise level permitted on V_{DD} and I/O supplies	–	100	mV	Max p-p noise level permitted on all supplies except A_{VDD}
V_{N_AVDD}	Noise level permitted on A_{VDD} supply	–	20	mV	Max p-p noise level permitted on A_{VDD}

Note

6. For CYUSB2014 I_{CC} USB is typically 22 mA–23 mA.

Table 9 I_{OH}/I_{OL} values for different drive strength and V_{DDIO} values

V_{DDIO} (V)	V_{OH} (V)	V_{OL} (V)	Drive strength	$I_{OH\ max}$ (mA)	$I_{OL\ min}$ (mA)
1.7	1.53	0.17	Quarter	1.02	2.21
			Half	1.51	3.28
			Three-quarters	1.83	3.85
			Full	2.28	4.73
2.5	2.25	0.25	Quarter	5.03	3.96
			Half	7.38	5.84
			Three-quarters	8.89	6.89
			Full	11.07	8.61
3.6	3.24	0.36	Quarter	7.80	5.74
			Half	11.36	8.64
			Three-quarters	13.64	10.15
			Full	16.92	12.67

18 Thermal characteristics

Table 10 Thermal characteristics

Parameter	Description	Value	Unit
$T_{J\ MAX}$	Maximum junction temperature	125	°C
Θ_{JA}	Thermal resistance (Junction to ambient)	34.66	°C/W
Θ_{JB}	Thermal resistance (Junction to board)	27.03	°C/W
Θ_{JC}	Thermal resistance (Junction to case)	13.57	°C/W

19 AC timing parameters

19.1 GPIF II lines AC characteristics at 100 MHz

Table 11 GPIF II lines AC characteristics at 100 MHz

Symbol	Parameter	Min	Typ	Max	Unit
Tr	Rise time	–	–	2.5	ns
Tf	Fall time	–	–	2.5	ns
Tov	Overshoot	–	–	3	%
Tun	Undershoot	–	–	3	%

19.2 GPIF II PCLK jitter characteristics

Table 12 GPIF II PCLK jitter characteristics

Clk Freq (MHz)	Period jitter (ps)	C-C min (ps)	C-C max (ps)
10.08	354.44	–187.92	204.55
25.2	205.97	–153.54	126.53
50.4	144.62	–100.16	85.769
100.8	171.43	–155.13	157.14

Note

7. The clock jitter is measured using internally generated PCLK. ie. PCLK is configured as an output from GPIF. The data is measured over 10,000 clock cycles.

19.3 GPIF II timing

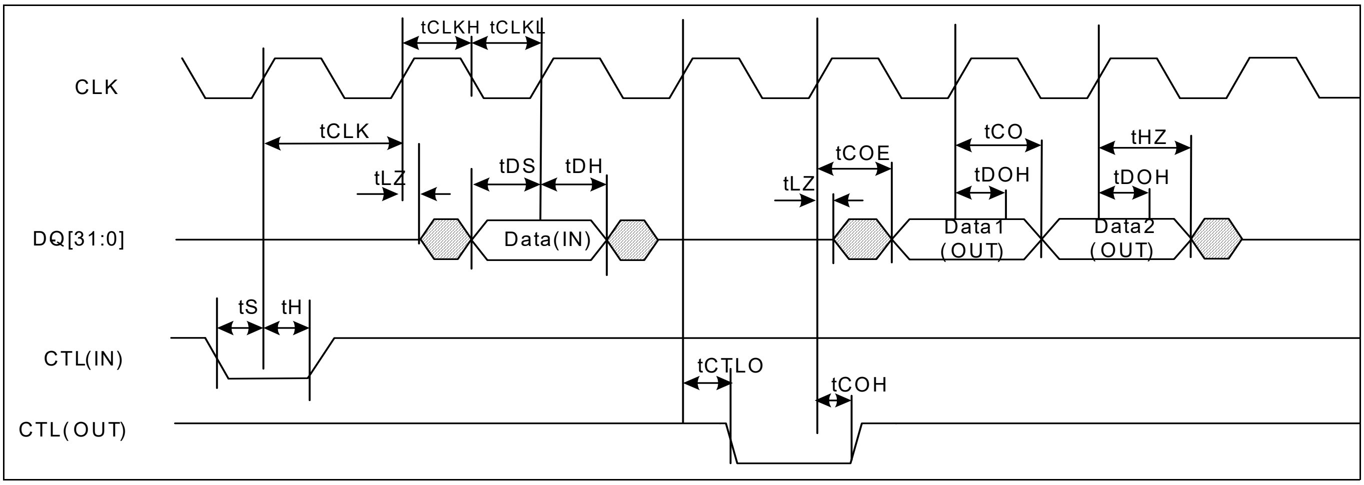


Figure 8 GPIF II timing in Synchronous Mode

Table 13 GPIF II timing parameters in Synchronous Mode [8]

Parameter	Description	Min	Max	Units
Frequency	Interface clock frequency	–	100	MHz
tCLK	Interface clock period	10	–	ns
tCLKH	Clock high time	4	–	ns
tCLKL	Clock low time	4	–	ns
tS	CTL input to clock setup time	2	–	ns
tH	CTL input to clock hold time	0.5	–	ns
tDS	Data in to clock setup time	2	–	ns
tDH	Data in to clock hold time	0.5	–	ns
tCO	Clock to data out propagation delay when DQ bus is already in output direction	–	7	ns
tCOE	Clock to data out propagation delay when DQ lines change to output from tristate and valid data is available on the DQ bus	–	9	ns
tCTLO	Clock to CTL out propagation delay	–	8	ns
tDOH	Clock to data out hold	2	–	ns
tCOH	Clock to CTL out hold	0	–	ns
tHZ	Clock to high-Z	–	8	ns
tLZ	Clock to low-Z	0	–	ns

Note

8. All parameters guaranteed by design and validated through characterization.

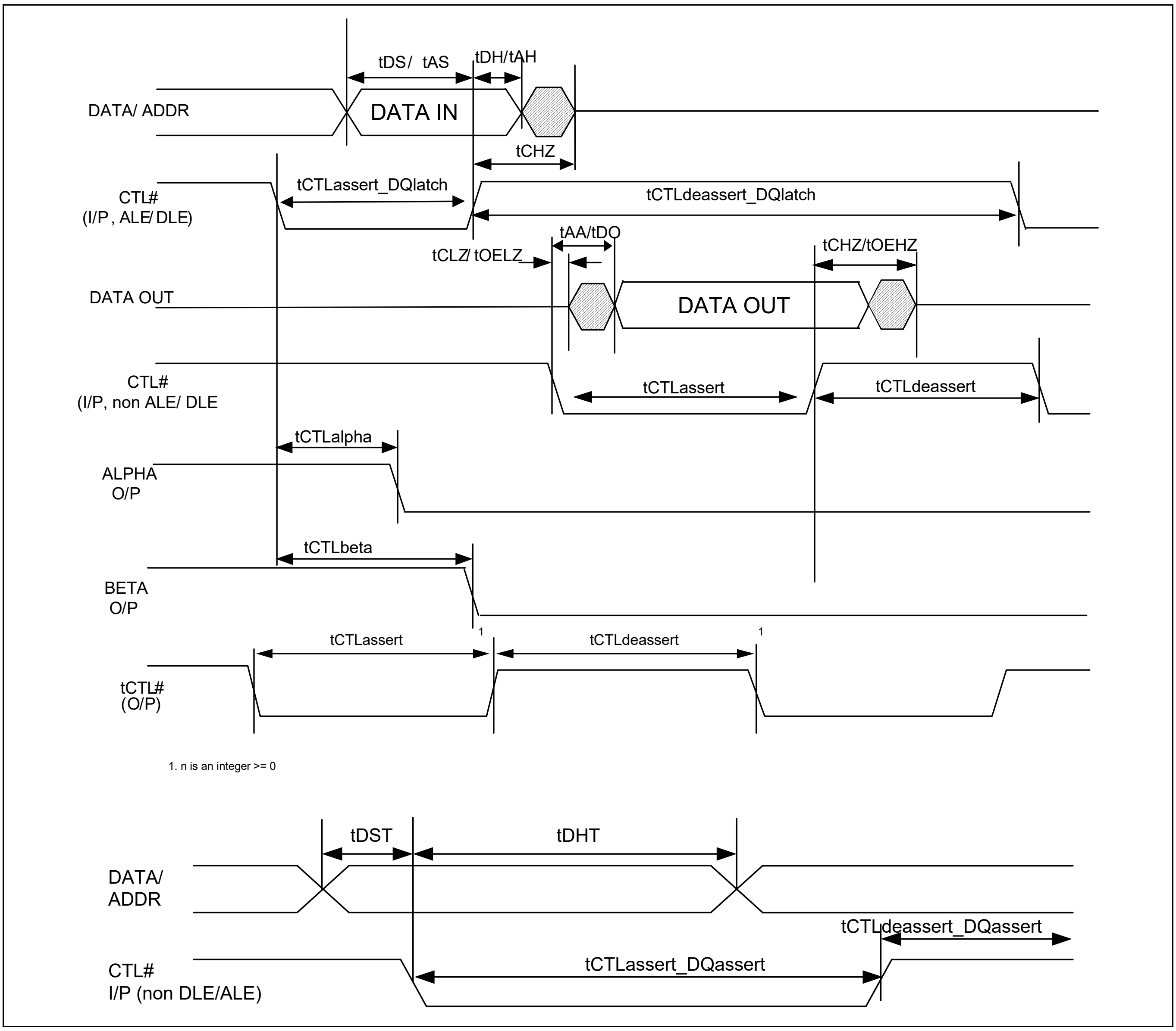


Figure 9 GPIF II timing in Asynchronous Mode

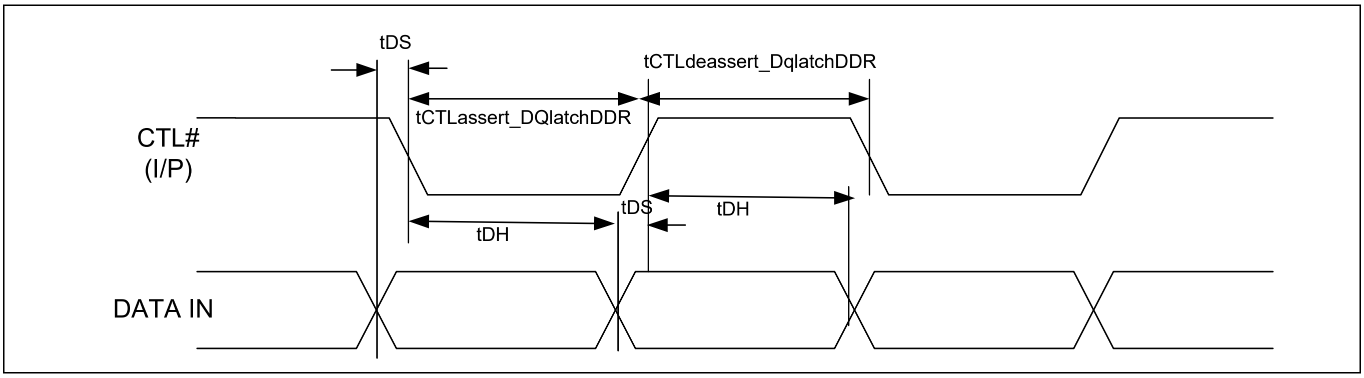


Figure 10 GPIF II timing in Asynchronous DDR Mode

Table 14 **GPIF II timing in Asynchronous Mode**[9, 10]

Note The following parameters assume one state transition

Parameter	Description	Min	Max	Units
tDS	Data In to DLE setup time. Valid in DDR async mode.	2.3	–	ns
tDH	Data In to DLE hold time. Valid in DDR async mode.	2	–	ns
tAS	Address In to ALE setup time	2.3	–	ns
tAH	Address In to ALE hold time	2	–	ns
tCTLassert	CTL I/O asserted width for CTRL inputs without DQ input association and for outputs.	7	–	ns
tCTLdeassert	CTL I/O deasserted width for CTRL inputs without DQ input association and for outputs.	7	–	ns
tCTLassert_DQassert	CTL asserted pulse width for CTL inputs that signify DQ inputs valid at the asserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	20	–	ns
tCTLdeassert_DQassert	CTL deasserted pulse width for CTL inputs that signify DQ input valid at the asserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	7	–	ns
tCTLassert_DQdeassert	CTL asserted pulse width for CTL inputs that signify DQ inputs valid at the deasserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	7	–	ns
tCTLdeassert_DQdeassert	CTL deasserted pulse width for CTL inputs that signify DQ inputs valid at the deasserting edge but do not employ in-built latches (ALE/DLE) for those DQ inputs.	20	–	ns
tCTLassert_DQlatch	CTL asserted pulse width for CTL inputs that employ in-built latches (ALE/DLE) to latch the DQ inputs. In this non-DDR case, in-built latches are always close at the deasserting edge.	7	–	ns
tCTLdeassert_DQlatch	CTL deasserted pulse width for CTL inputs that employ in-built latches (ALE/DLE) to latch the DQ inputs. In this non-DDR case, in-built latches always close at the deasserting edge.	10	–	ns
tCTLassert_DQlatchDDR	CTL asserted pulse width for CTL inputs that employ in-built latches (DLE) to latch the DQ inputs in DDR mode.	10	–	ns
tCTLdeassert_DQlatchDDR	CTL deasserted pulse width for CTL inputs that employ in-built latches (DLE) to latch the DQ inputs in DDR mode.	10	–	ns
tAA	DQ/CTL input to DQ output time when DQ change or CTL change needs to be detected and affects internal updates of input and output DQ lines.	–	30	ns
tDO	CTL to data out when the CTL change merely enables the output flop update whose data was already established.	–	25	ns

Notes

9. All parameters guaranteed by design and validated through characterization.
10. “alpha” output corresponds to “early output” and “beta” corresponds to “delayed output”. Please refer to the GPIFII Designer Tool for the use of these outputs.

Table 14 **GPIF II timing in Asynchronous Mode**[9, 10] (continued)

Note The following parameters assume one state transition

Parameter	Description	Min	Max	Units
tOELZ	CTL designated as OE to low-Z. Time when external devices should stop driving data.	0	–	ns
tOEHZ	CTL designated as OE to high-Z	8	8	ns
tCLZ	CTL (non-OE) to low-Z. Time when external devices should stop driving data.	0	–	ns
tCHZ	CTL (non-OE) to high-Z	30	30	ns
tCTLalpha	CTL to alpha change at output	–	25	ns
tCTLbeta	CTL to beta change at output	–	30	ns
tDST	Addr/data setup when DLE/ALE not used	2	–	ns
tDHT	Addr/data hold when DLE/ALE not used	20	–	ns

19.4 Slave FIFO interface

19.4.1 Synchronous Slave FIFO Read sequence description

- FIFO address is stable and SLCS is asserted
- FLAG indicates FIFO not empty status
- SLOE is asserted. SLOE is an output-enable only, whose sole function is to drive the data bus.
- SLRD is asserted

The FIFO pointer is updated on the rising edge of the PCLK, while the SLRD is asserted. This starts the propagation of data from the newly addressed location to the data bus. After a propagation delay of tco (measured from the rising edge of PCLK), the new data value is present. N is the first data value read from the FIFO. To have data on the FIFO data bus, SLOE must also be asserted.

The same sequence of events is applicable for a burst read.

FLAG Usage:

The FLAG signals are monitored for flow control by the external processor. FLAG signals are outputs from FX3 that may be configured to show empty, full, or partial status for a dedicated thread or the current thread that is addressed.

Socket Switching Delay (Tssd):

The socket-switching delay is measured from the time EPSWITCH# is asserted by the master, with the new socket address on the address bus, to the time the Current_Thread_DMA_Ready flag is asserted. For the Producer socket, the flag is asserted when it is ready to receive data in the DMA buffer. For the Consumer socket, the flag is asserted when it is ready to drive data out of the DMA buffer. For a synchronous slave FIFO interface, the switching delay is measured in the number of GPIF interface clock cycles; for an asynchronous slave FIFO interface, in PIB clock cycles. This is applicable only for the 5-bit Slave FIFO interface; there is no socket-switching delay in FX3’s 2-bit Slave FIFO interface, which makes use of thread switching in the GPIF™ II state machine.

Note For burst mode, the SLRD# and SLOE# are asserted during the entire duration of the read. When SLOE# is asserted, the data bus is driven (with data from the previously addressed FIFO). For each subsequent rising edge of PCLK, while the SLRD# is asserted, the FIFO pointer is incremented and the next data value is placed on the data bus.

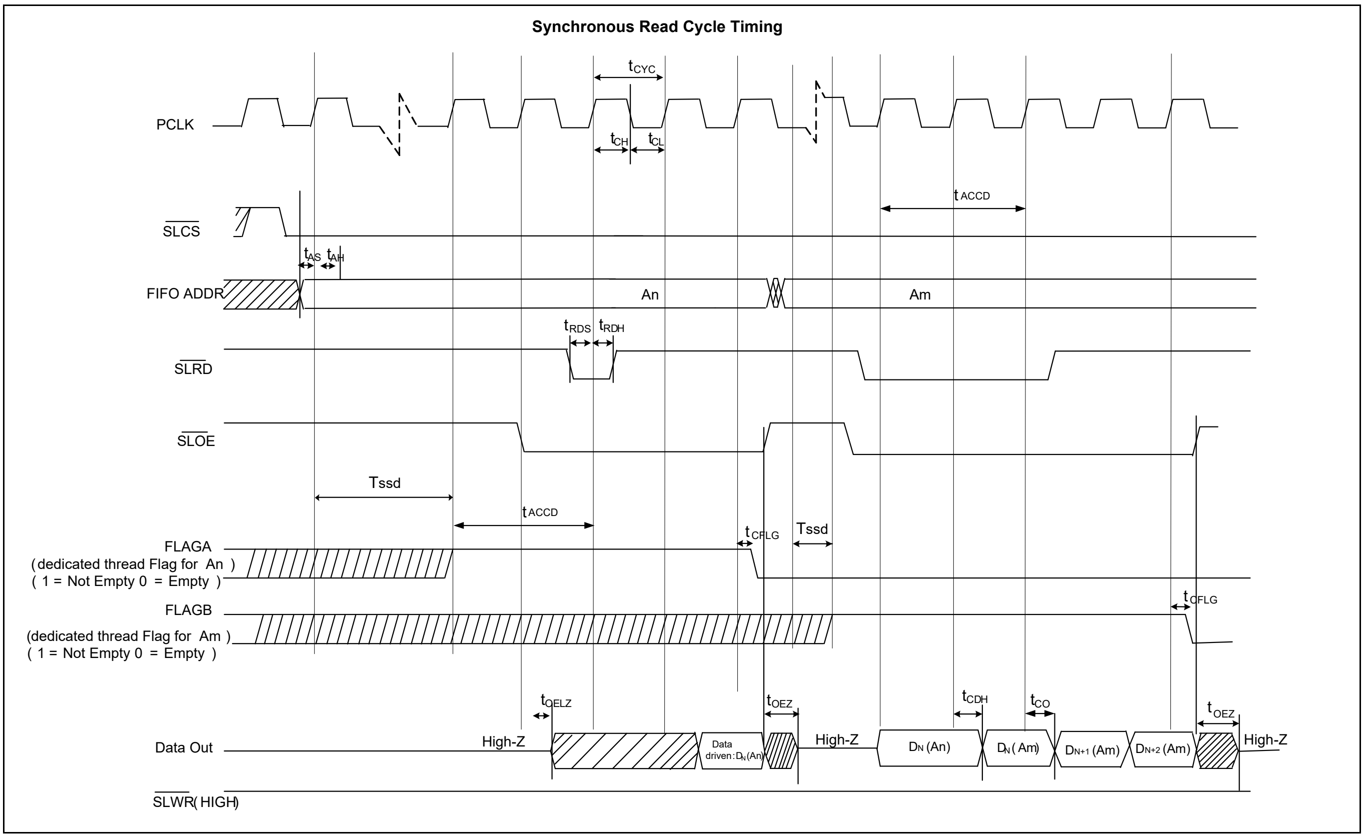


Figure 11 Synchronous Slave FIFO Read Mode

19.4.2 Synchronous Slave FIFO Write sequence description

- FIFO address is stable and the signal SLCS# is asserted
- External master or peripheral outputs the data to the data bus
- SLWR# is asserted
- While the SLWR# is asserted, data is written to the FIFO and on the rising edge of the PCLK, the FIFO pointer is incremented
- The FIFO flag is updated after a delay of t_{WFLG} from the rising edge of the clock

The same sequence of events is also applicable for burst write

Note For the burst mode, SLWR# and SLCS# are asserted for the entire duration, during which all the required data values are written. In this burst write mode, after the SLWR# is asserted, the data on the FIFO data bus is written to the FIFO on every rising edge of PCLK. The FIFO pointer is updated on each rising edge of PCLK.

Short Packet: A short packet can be committed to the USB host by using the PKTEND#. The external device or processor should be designed to assert the PKTEND# along with the last word of data and SLWR# pulse corresponding to the last word. The FIFOADDR lines must be held constant during the PKTEND# assertion.

Zero-Length Packet: The external device or processor can signal a Zero-Length Packet (ZLP) to FX3 simply by asserting PKTEND#, without asserting SLWR#. SLCS# and address must be driven as shown in **Figure 12**.

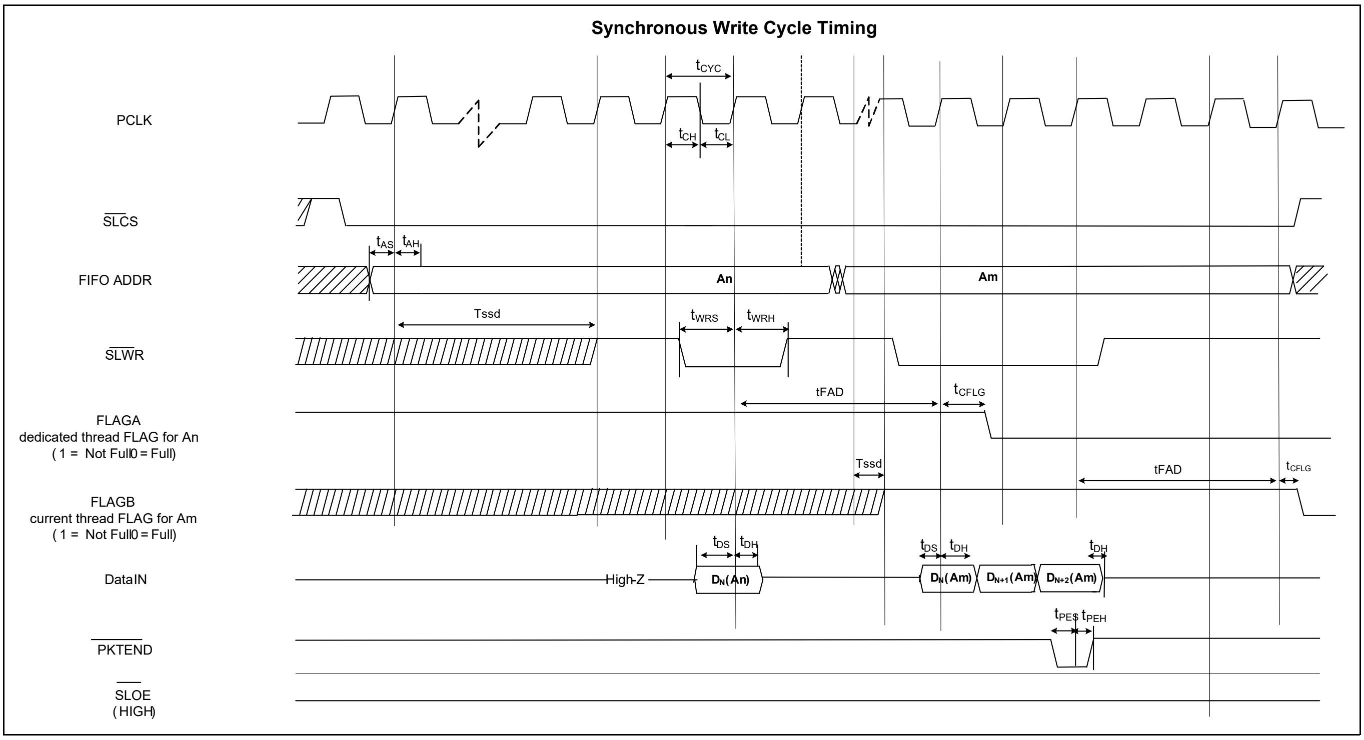


Figure 12 Synchronous Slave FIFO Write Mode

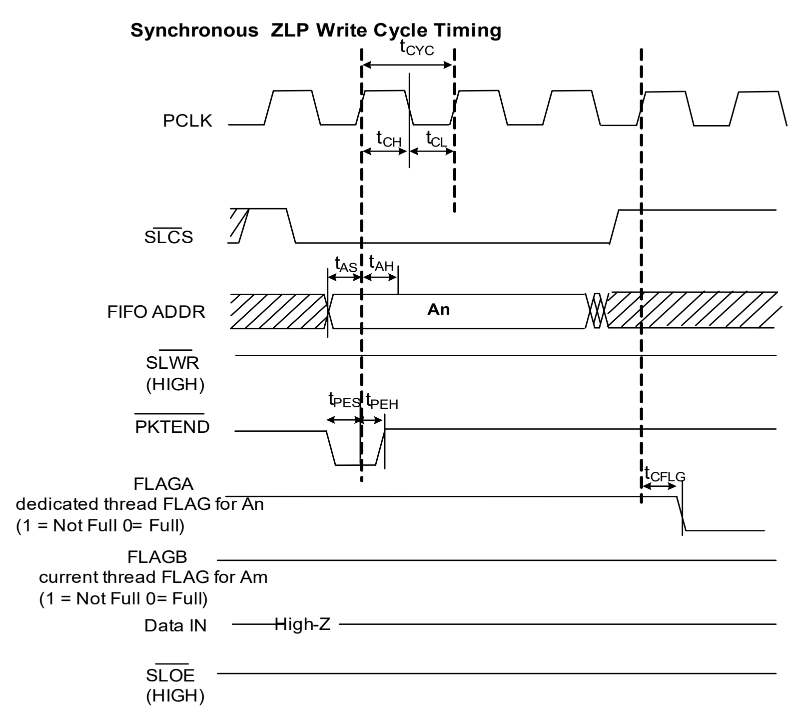


Figure 13 Synchronous Slave FIFO ZLP Write Cycle timing

Table 15 Synchronous Slave FIFO parameters[11]

Parameter	Description	Min	Max	Units
FREQ	Interface clock frequency	–	100	MHz
tCYC	Clock period	10	–	ns
tCH	Clock HIGH time	4	–	ns
tCL	Clock LOW time	4	–	ns
tRDS	SLRD# to CLK setup time	2	–	ns
tRDH	SLRD# to CLK hold time	0.5	–	ns
tWRS	SLWR# to CLK setup time	2	–	ns
tWRH	SLWR# to CLK hold time	0.5	–	ns
tCO	Clock to valid data	–	7	ns
tDS	Data input setup time	2	–	ns
tDH	CLK to data input hold	0.5	–	ns
tAS	Address to CLK setup time	2	–	ns
tAH	CLK to address hold time	0.5	–	ns
tOELZ	SLOE# to data low-Z	0	–	ns
tCFLG	CLK to flag output propagation delay	–	8	ns
tOEZ	SLOE# deassert to Data Hi Z	–	8	ns
tPES	PKTEND# to CLK setup	2	–	ns
tPEH	CLK to PKTEND# hold	0.5	–	ns
tCDH	CLK to data output hold	2	–	ns
tSSD	Socket switching delay	2	68	Clock cycles
tACCD	Latency from SLRD# to Data	2	2	Clock cycles
tFAD	Latency from SLWR# to FLAG	3	3	Clock cycles
Note Three-cycle latency from ADDR to DATA/FLAGS.				

Note

11.All parameters guaranteed by design and validated through characterization.

19.4.3 Asynchronous Slave FIFO Read sequence description

- FIFO address is stable and the SLCS# signal is asserted.
- SLOE# is asserted. This results in driving the data bus.
- SLRD # is asserted.
- Data from the FIFO is driven after assertion of SLRD#. This data is valid after a propagation delay of tRDO from the falling edge of SLRD#.
- FIFO pointer is incremented on deassertion of SLRD#

In **Figure 14**, data N is the first valid data read from the FIFO. For data to appear on the data bus during the read cycle, SLOE# must be in an asserted state. SLRD# and SLOE# can also be tied.

The same sequence of events is also shown for a burst read.

Note In the burst read mode, during SLOE# assertion, the data bus is in a driven state (data is driven from a previously addressed FIFO). After assertion of SLRD# data from the FIFO is driven on the data bus (SLOE# must also be asserted). The FIFO pointer is incremented after deassertion of SLRD#.

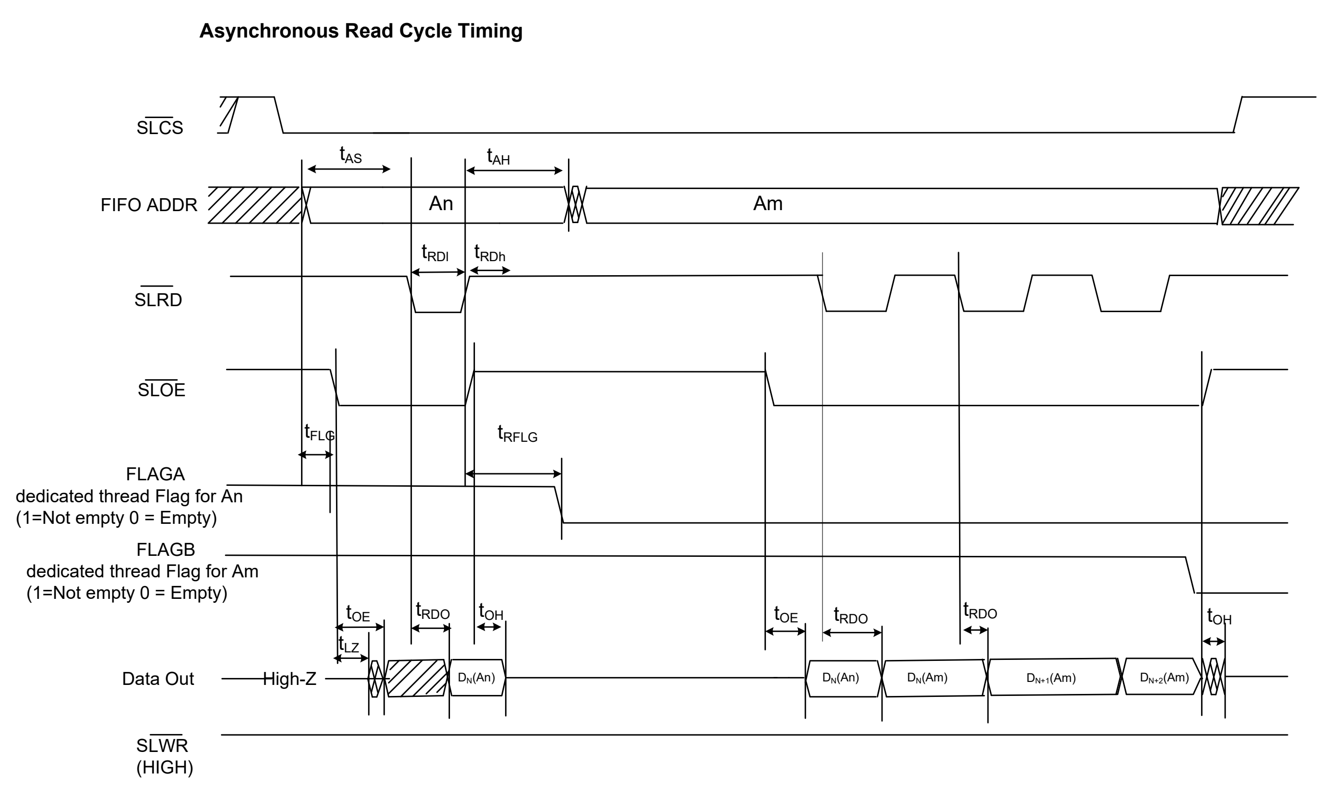


Figure 14 Asynchronous Slave FIFO Read Mode

19.4.4 Asynchronous Slave FIFO Write sequence description

- FIFO address is driven and SLCS# is asserted
- SLWR# is asserted. SLCS# must be asserted with SLWR# or before SLWR# is asserted
- Data must be present on the tWRS bus before the deasserting edge of SLWR#
- Deassertion of SLWR# causes the data to be written from the data bus to the FIFO, and then the FIFO pointer is incremented
- The FIFO flag is updated after the tWFLG from the deasserting edge of SLWR.

The same sequence of events is shown for a burst write.

Note that in the burst write mode, after SLWR# deassertion, the data is written to the FIFO, and then the FIFO pointer is incremented.

Short Packet: A short packet can be committed to the USB host by using the PKTEND#. The external device or processor should be designed to assert the PKTEND# along with the last word of data and SLWR# pulse corresponding to the last word. The FIFOADDR lines must be held constant during the PKTEND# assertion.

Zero-Length Packet: The external device or processor can signal a zero-length packet (ZLP) to FX3 simply by asserting PKTEND#, without asserting SLWR#. SLCS# and the address must be driven as shown in **Figure 16**.

FLAG Usage: The FLAG signals are monitored by the external processor for flow control. FLAG signals are FX3 outputs that can be configured to show empty, full, and partial status for a dedicated address or the current address.

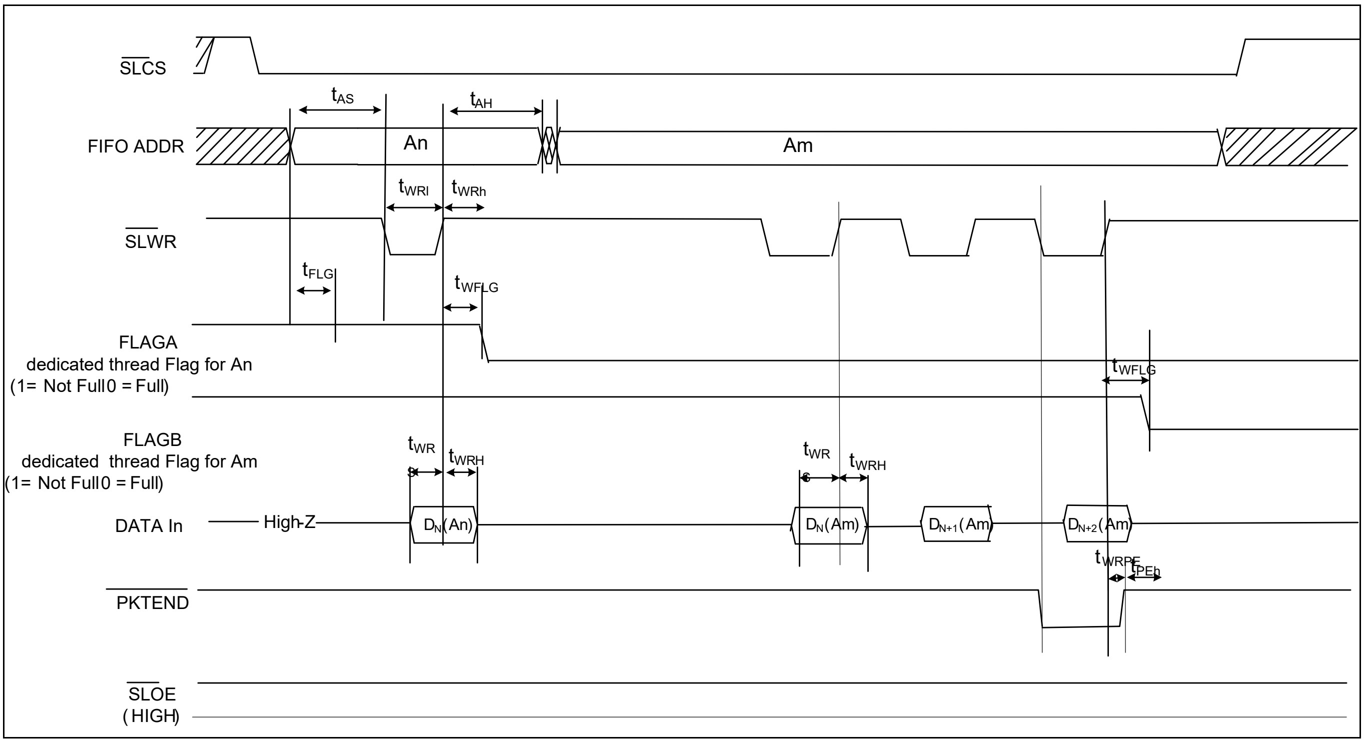


Figure 15 Asynchronous Slave FIFO Write Mode

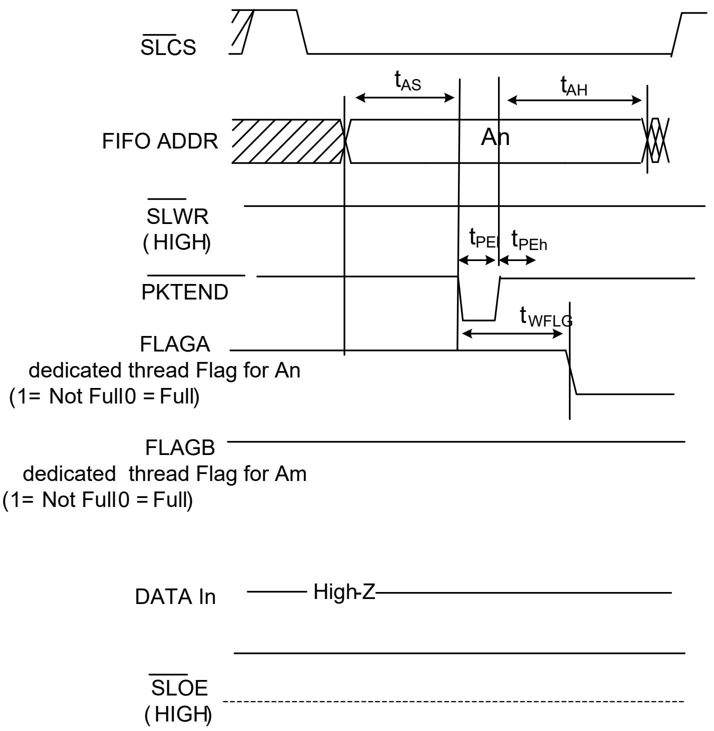


Figure 16 Asynchronous ZLP Write Cycle timing

Table 16 **Asynchronous Slave FIFO parameters**[12]

Parameter	Description	Min	Max	Units
tRDI	SLRD# LOW	20	–	ns
tRDh	SLRD# HIGH	10	–	ns
tAS	Address to SLRD#/SLWR# setup time	7	–	ns
tAH	SLRD#/SLWR#/PKTEND to address hold time	2	–	ns
tRFLG	SLRD# to FLAGS output propagation delay	–	35	ns
tFLG	ADDR to FLAGS output propagation delay	–	22.5	ns
tRDO	SLRD# to data valid	–	25	ns
tOE	OE# low to data valid	–	25	ns
tLZ	OE# low to data low-Z	0	–	ns
tOH	SLOE# deassert data output hold	–	22.5	ns
tWRI	SLWR# LOW	20	–	ns
tWRh	SLWR# HIGH	10	–	ns
tWRS	Data to SLWR# setup time	7	–	ns
tWRH	SLWR# to Data Hold time	2	–	ns
tWFLG	SLWR#/PKTEND to Flags output propagation delay	–	35	ns
tPEI	PKTEND LOW	20	–	ns
tPEh	PKTEND HIGH	7.5	–	ns
tWRPE	SLWR# deassert to PKTEND deassert	2	–	ns

Note

[12] All parameters guaranteed by design and validated through characterization.

19.5 Host Processor Interface (P-Port) timing

19.5.1 Asynchronous SRAM timing

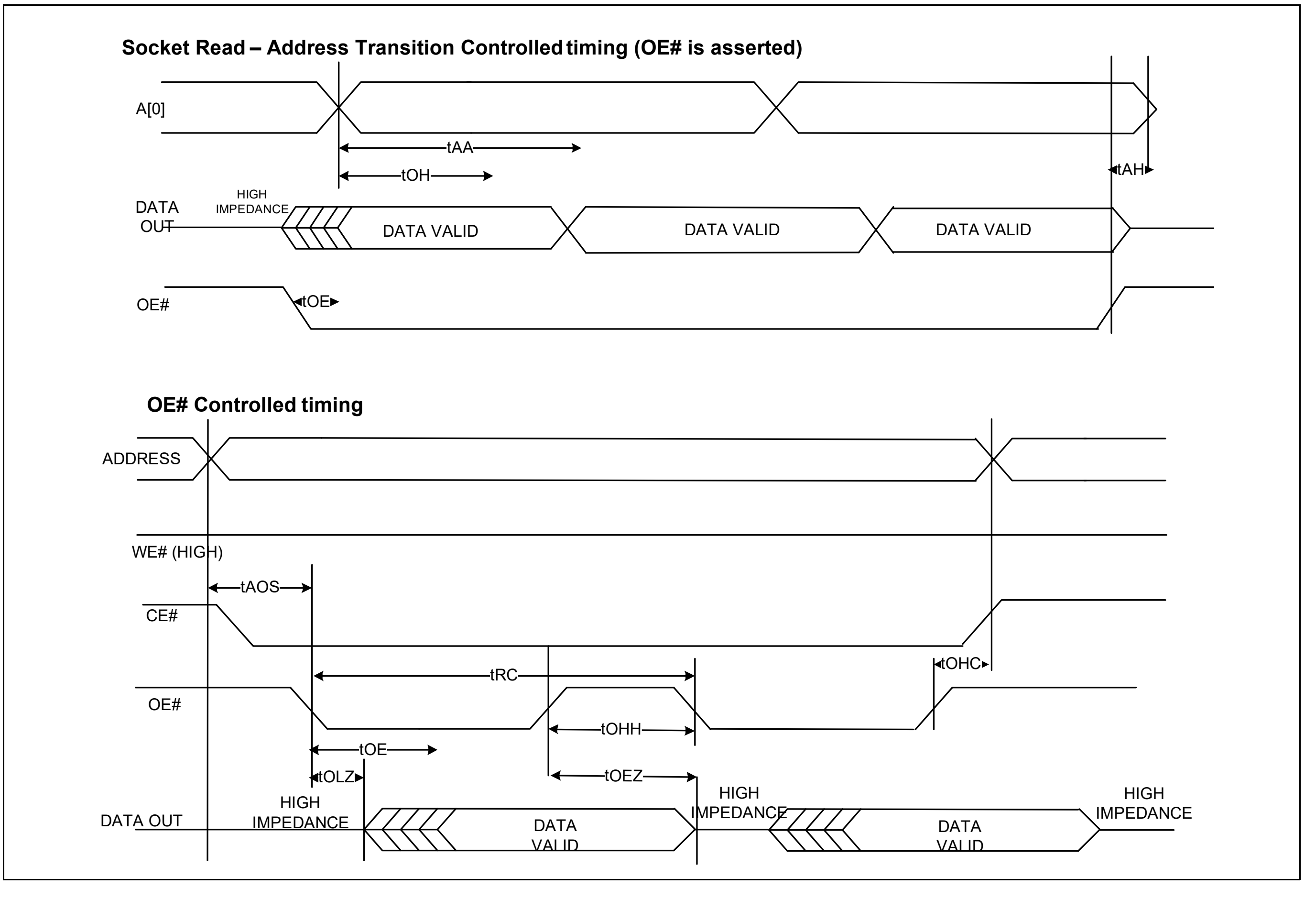


Figure 17 Non-multiplexed Asynchronous SRAM Read timing

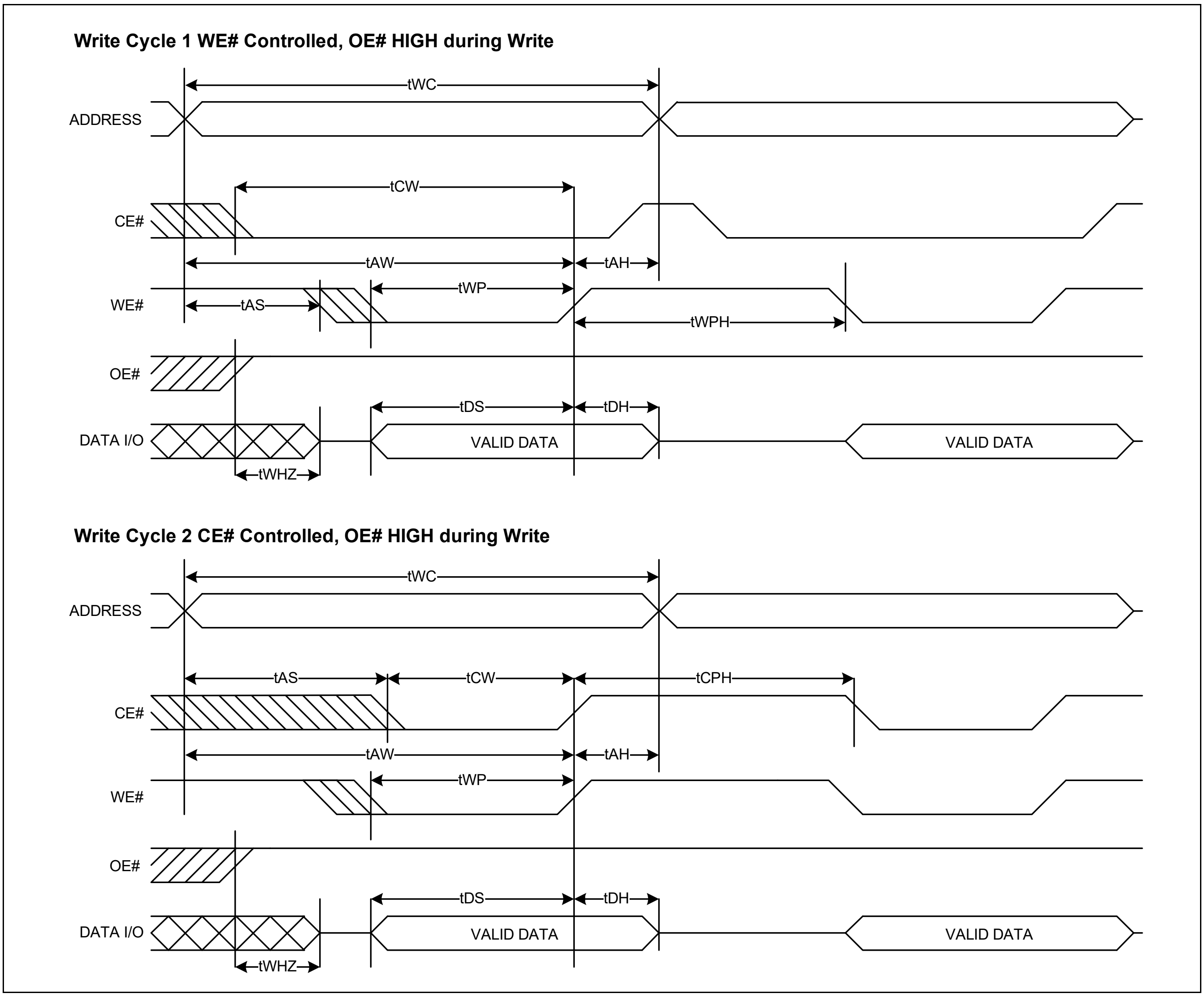


Figure 18 Non-multiplexed Asynchronous SRAM Write timing (WE# and CE# Controlled)

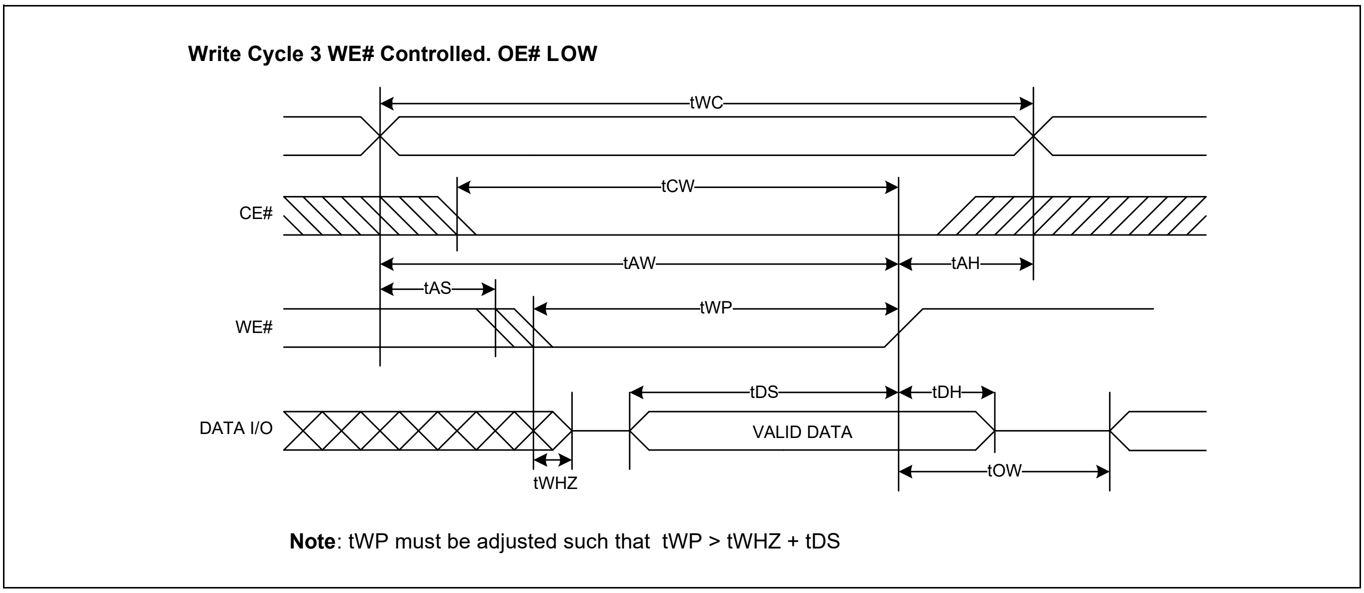


Figure 19 Non-multiplexed Asynchronous SRAM Write timing (WE# Controlled, OE# LOW)

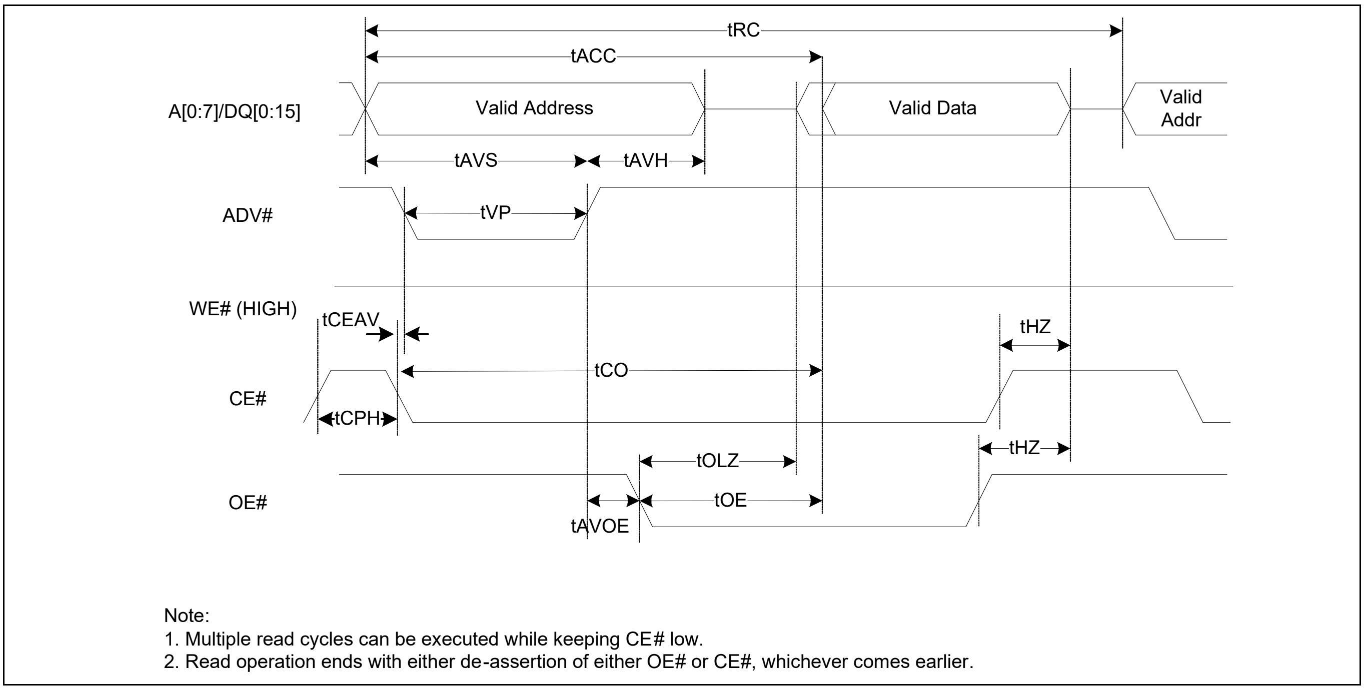
Table 17 **Asynchronous SRAM timing parameters**[13]

Parameter	Description	Min	Max	Units
–	SRAM interface bandwidth	–	61.5	Mbps
tRC	Read cycle time	32.5	–	ns
tAA	Address to data valid	–	30	ns
tAOS	Address to OE# LOW setup time	7	–	ns
tOH	Data output hold from address change	3	–	ns
tOHH	OE# HIGH hold time	7.5	–	ns
tOHC	OE# HIGH to CE# HIGH	2	–	ns
tOE	OE# LOW to data valid	–	25	ns
tOLZ	OE# LOW to Low-Z	0	–	ns
tWC	Write cycle time	30	–	ns
tCW	CE# LOW to write end	30	–	ns
tAW	Address valid to write end	30	–	ns
tAS	Address setup to write start	7	–	ns
tAH	Address hold time from CE# or WE#	2	–	ns
tWP	WE# pulse width	20	–	ns
tWPH	WE# HIGH time	10	–	ns
tCPH	CE# HIGH time	10	–	ns
tDS	Data setup to write end	7	–	ns
tDH	Data hold to write end	2	–	ns
tWHZ	Write to DQ High-Z output	–	22.5	ns
tOEZ	OE# HIGH to DQ High-Z output	–	22.5	ns
tOW	End of write to Low-Z output	0	–	ns

Note

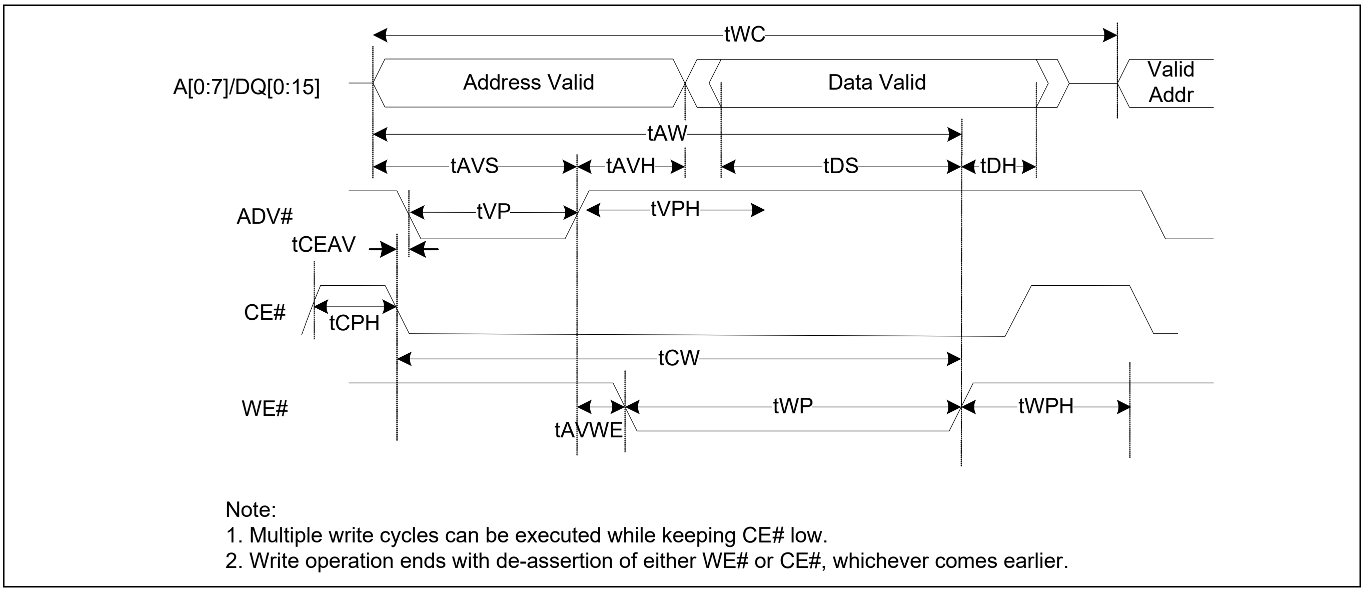
[13] All parameters guaranteed by design and validated through characterization.

19.5.2 ADMux timing for Asynchronous Access



Note:
1. Multiple read cycles can be executed while keeping CE# low.
2. Read operation ends with either de-assertion of either OE# or CE#, whichever comes earlier.

Figure 20 ADMux Asynchronous Random Read



Note:
1. Multiple write cycles can be executed while keeping CE# low.
2. Write operation ends with de-assertion of either WE# or CE#, whichever comes earlier.

Figure 21 ADMux Asynchronous Random Write

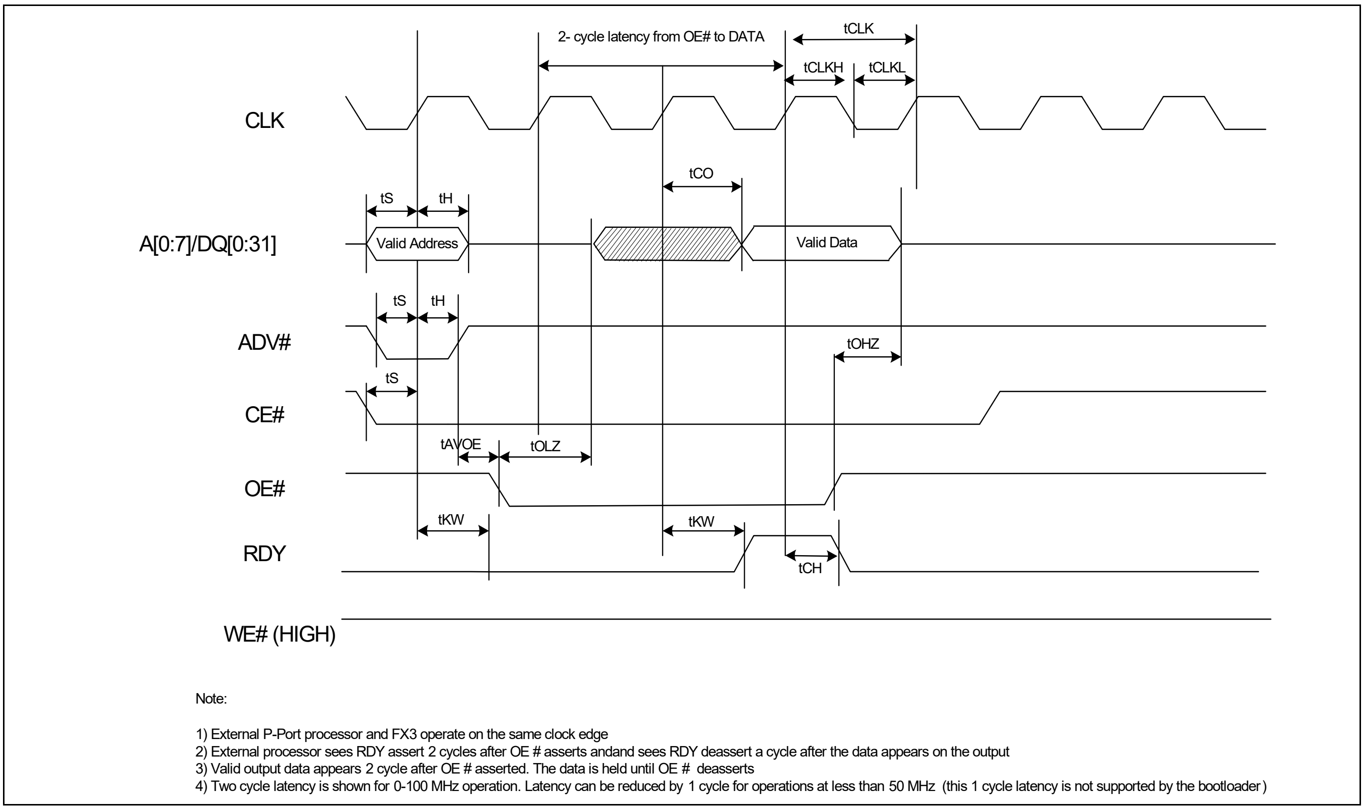
Table 18 **Asynchronous ADMux timing parameters**[14]

Parameter	Description	Min	Max	Units	Notes
ADMux Asynchronous READ Access timing parameters					
tRC	Read cycle time (address valid to address valid)	54.5	–	ns	This parameter is dependent on when the P-port processors deasserts OE#
tACC	Address valid to data valid	–	32	ns	–
tCO	CE# assert to data valid	–	34.5	ns	–
tAVOE	ADV# deassert to OE# assert	2	–	ns	–
tOLZ	OE# assert to data Low-Z	0	–	ns	–
tOE	OE# assert to data valid	–	25	ns	–
tHZ	Read cycle end to data High-Z	–	22.5	ns	–
ADMux Asynchronous WRITE Access timing parameters					
tWC	Write cycle time (Address Valid to Address Valid)	–	52.5	ns	–
tAW	Address valid to write end	30	–	ns	–
tCW	CE# assert to write end	30	–	ns	–
tAVWE	ADV# deassert to WE# assert	2	–	ns	–
tWP	WE# LOW pulse width	20	–	ns	–
tWPH	WE# HIGH pulse width	10	–	ns	–
tDS	Data valid setup to WE# deassert	18	–	ns	–
tDH	Data valid hold from WE# deassert	2	–	ns	–
ADMux Asynchronous Common READ/WRITE Access timing parameters					
tAVS	Address valid setup to ADV# deassert	5	–	ns	–
tAVH	Address valid hold from ADV# deassert	2	–	ns	–
tVP	ADV# LOW pulse width	7.5	–	ns	–
tCPH	CE# HIGH pulse width	10	–	ns	–
tVPH	ADV# HIGH pulse width	15	–	ns	–
tCEAV	CE# assert to ADV# assert	0	–	ns	–

Note

[14] All parameters guaranteed by design and validated through characterization.

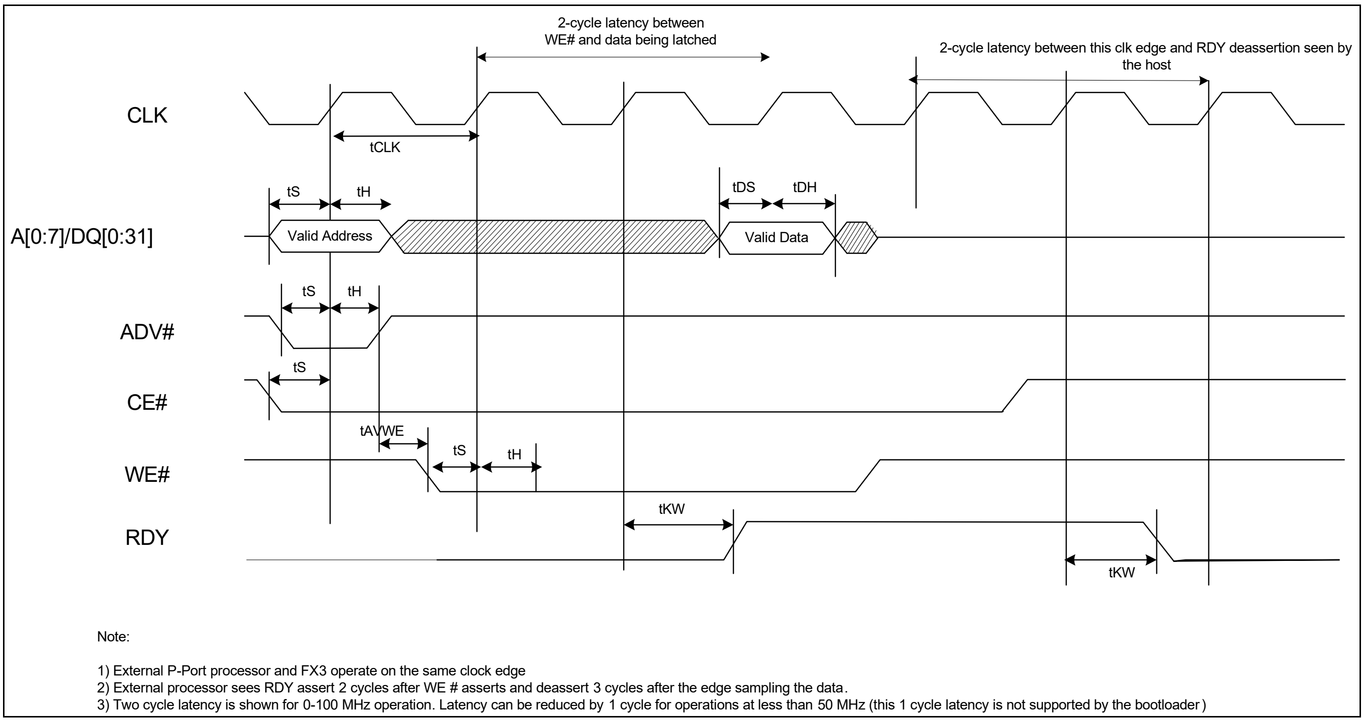
19.5.3 Synchronous ADMux timing



Note:

1) External P-Port processor and FX3 operate on the same clock edge
2) External processor sees RDY assert 2 cycles after OE # asserts andand sees RDY deassert a cycle after the data appears on the output
3) Valid output data appears 2 cycle after OE # asserted. The data is held until OE # deasserts
4) Two cycle latency is shown for 0-100 MHz operation. Latency can be reduced by 1 cycle for operations at less than 50 MHz (this 1 cycle latency is not supported by the bootloader)

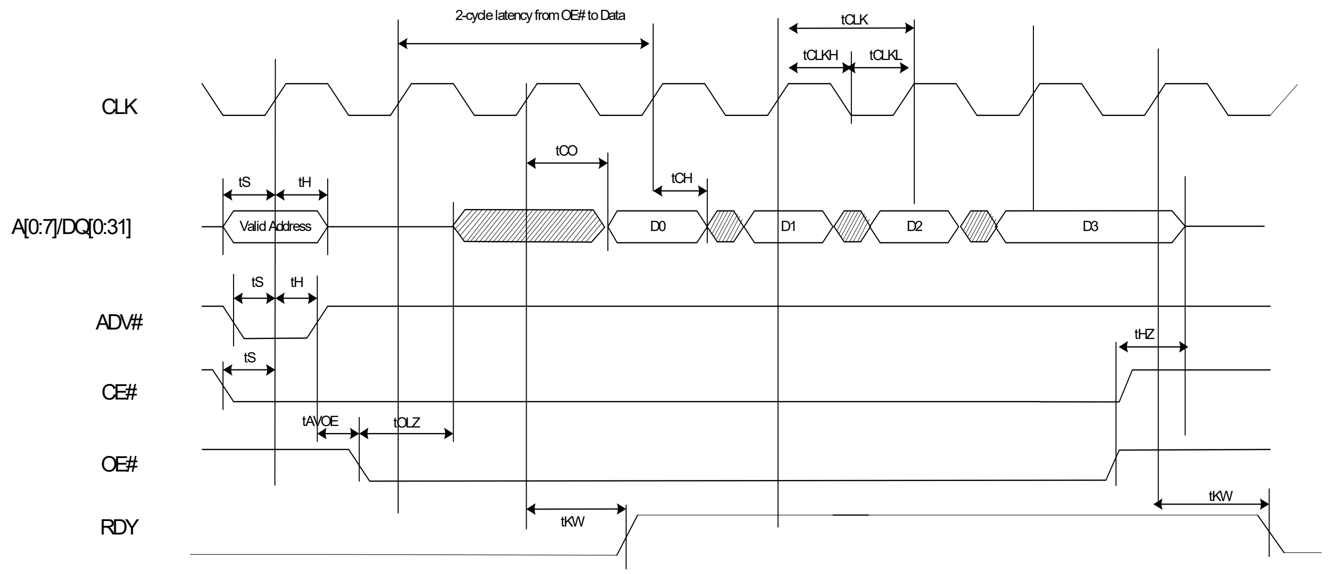
Figure 22 Synchronous ADMux Interface – Read Cycle timing



Note:

1) External P-Port processor and FX3 operate on the same clock edge
2) External processor sees RDY assert 2 cycles after WE # asserts and deassert 3 cycles after the edge sampling the data.
3) Two cycle latency is shown for 0-100 MHz operation. Latency can be reduced by 1 cycle for operations at less than 50 MHz (this 1 cycle latency is not supported by the bootloader)

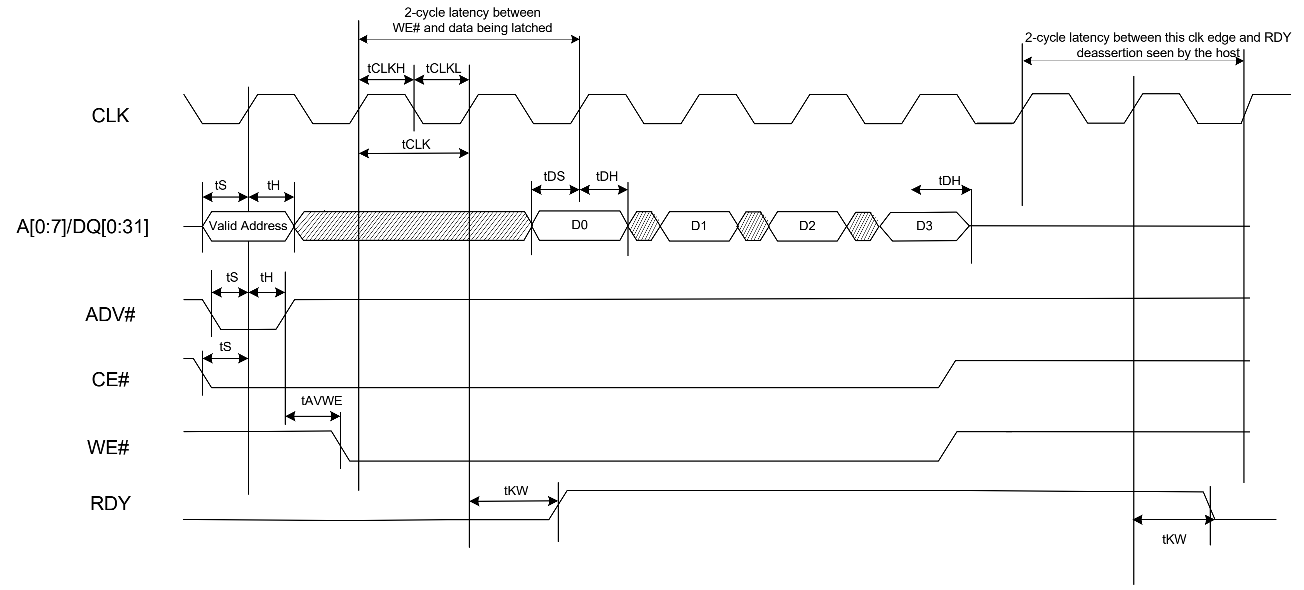
Figure 23 Synchronous ADMux Interface – Write Cycle timing



Note:

1) External P-Port processor and FX3 work operate on the same clock edge
2) External processor sees RDY assert 2 cycles after OE # asserts andand sees RDY deassert a cycle after the last burst data appears on the output
3) Valid output data appears 2 cycle after OE # asserted. The last burst data is held until OE # deasserts
4) Burst size of 4 is shown. Transfer size for the operation must be a multiple of burst size. Burst size is usually power of 2. RDY will not deassert in the middle of the burst.
5) External processor cannot deassert OE in the middle of a burst. If it does so, any bytes remaining in the burst packet could get lost.
6) Two cycle latency is shown for 0-100 MHz operation. Latency can be reduced by 1 cycle for operations at less than 50 MHz (this 1 cycle latency is not supported by the bootloader)

Figure 24 Synchronous ADMux Interface – Burst Read timing



Note:

1) External P-Port processor and FX3 operate on the same clock edge
2) External processor sees RDY assert 2 cycles after WE # asserts and deasserts 3 cycles after the edge sampling the last burst data.
3) Transfer size for the operation must be a multiple of burst size. Burst size is usually power of 2. RDY will not deassert in the middle of the burst. Burst size of 4 is shown
4) External processor cannot deassert WE in the middle of a burst. If it does so, any bytes remaining in the burst packet could get lost.
5)Two cycle latency is shown for 0-100 MHz operation. Latency can be reduced by 1 cycle for operations at less than 50 MHz (this 1 cycle latency is not supported by the bootloader)

Figure 25 Sync ADMux Interface – Burst Write timing

Table 19 **Synchronous ADMux timing parameters**[15]

Parameter	Description	Min	Max	Unit
FREQ	Interface clock frequency	–	100	MHz
tCLK	Clock period	10	–	ns
tCLKH	Clock HIGH time	4	–	ns
tCLKL	Clock LOW time	4	–	ns
tS	CE#/WE#/DQ setup time	2	–	ns
tH	CE#/WE#/DQ hold time	0.5	–	ns
tCH	Clock to data output hold time	0	–	ns
tDS	Data input setup time	2	–	ns
tDH	Clock to data input hold	0.5	–	ns
tAVDOE	ADV# HIGH to OE# LOW	0	–	ns
tAVDWE	ADV# HIGH to WE# LOW	0	–	ns
tHZ	CE# HIGH to Data High-Z	–	8	ns
tOHZ	OE# HIGH to Data High-Z	–	8	ns
tOLZ	OE# LOW to Data Low-Z	0	–	ns
tKW	Clock to RDY valid	–	8	ns

Note

15. All parameters guaranteed by design and validated through characterization.

19.6 Serial Peripherals timing

19.6.1 I^{2}C timing

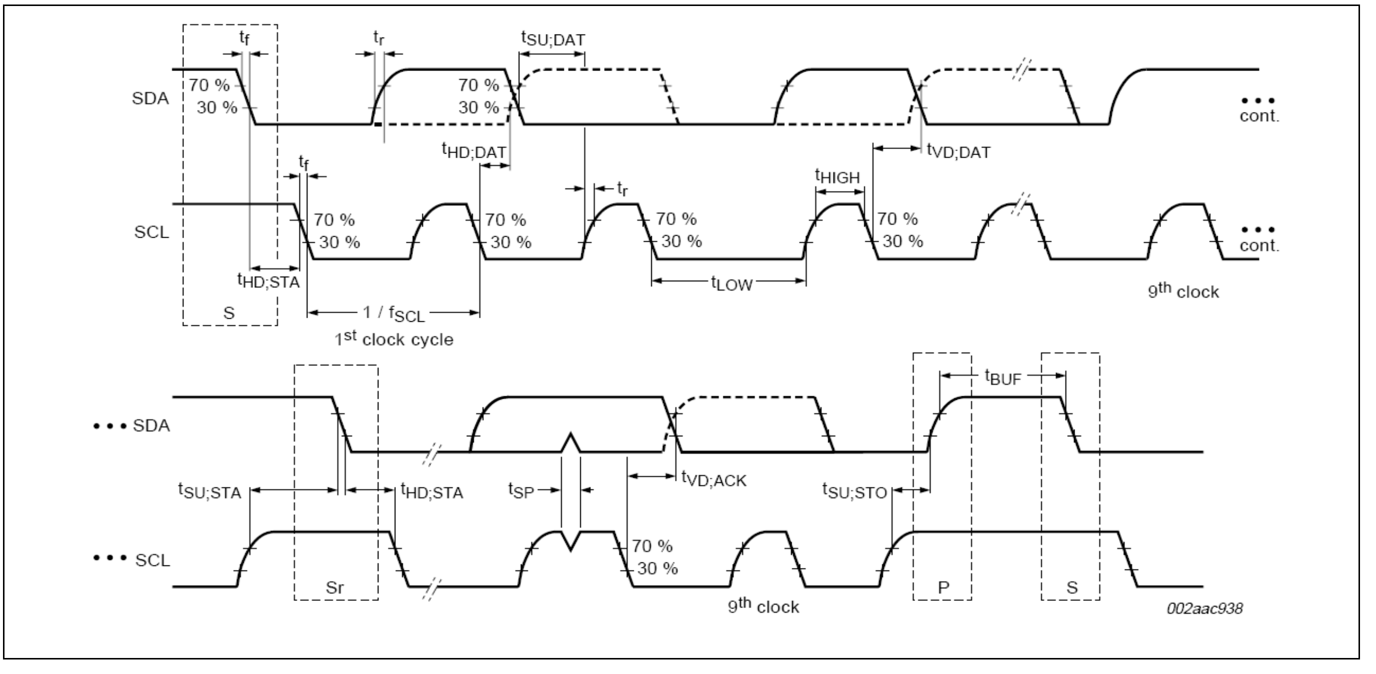


Figure 26 I^{2}C timing definition

Table 20 **I^2C timing parameters**[16]

Parameter	Description	Min	Max	Units
I^2C Standard Mode parameters				
fSCL	SCL clock frequency	0	100	kHz
tHD:STA	Hold time START condition	4	–	µs
tLOW	LOW period of the SCL	4.7	–	µs
tHIGH	HIGH period of the SCL	4	–	µs
tSU:STA	Setup time for a repeated START condition	4.7	–	µs
tHD:DAT	Data hold time	0	–	µs
tSU:DAT	Data setup time	250	–	ns
tr	Rise time of both SDA and SCL signals	–	1000	ns
tf	Fall time of both SDA and SCL signals	–	300	ns
tSU:STO	Setup time for STOP condition	4	–	µs
tBUF	Bus free time between a STOP and START condition	4.7	–	µs
tVD:DAT	Data valid time	–	3.45	µs
tVD:ACK	Data valid ACK	–	3.45	µs
tSP	Pulse width of spikes that must be suppressed by input filter	n/a	n/a	
I^2C Fast Mode parameters				
fSCL	SCL clock frequency	0	400	kHz
tHD:STA	Hold time START condition	0.6	–	µs
tLOW	LOW period of the SCL	1.3	–	µs
tHIGH	HIGH period of the SCL	0.6	–	µs
tSU:STA	Setup time for a repeated START condition	0.6	–	µs
tHD:DAT	Data hold time	0	–	µs
tSU:DAT	Data setup time	100	–	ns
tr	Rise time of both SDA and SCL signals	–	300	ns
tf	Fall time of both SDA and SCL signals	–	300	ns
tSU:STO	Setup time for STOP condition	0.6	–	µs
tBUF	Bus free time between a STOP and START condition	1.3	–	µs
tVD:DAT	Data valid time	–	0.9	µs
tVD:ACK	Data valid ACK	–	0.9	µs
tSP	Pulse width of spikes that must be suppressed by input filter	0	50	ns

Note

16.All parameters guaranteed by design and validated through characterization.

Table 20 **I^2C timing parameters**[16] (continued)

Parameter	Description	Min	Max	Units
I^2C Fast Mode Plus Parameters (Not supported at I2C_VDDQ = 1.2 V)				
fSCL	SCL clock frequency	0	1000	kHz
tHD:STA	Hold time START condition	0.26	–	µs
tLOW	LOW period of the SCL	0.5	–	µs
tHIGH	HIGH period of the SCL	0.26	–	µs
tSU:STA	Setup time for a repeated START condition	0.26	–	µs
tHD:DAT	Data hold time	0	–	µs
tSU:DAT	Data setup time	50	–	ns
tr	Rise time of both SDA and SCL signals	–	120	ns
tf	Fall time of both SDA and SCL signals	–	120	ns
tSU:STO	Setup time for STOP condition	0.26	–	µs
tBUF	Bus-free time between a STOP and START condition	0.5	–	µs
tVD:DAT	Data valid time	–	0.45	µs
tVD:ACK	Data valid ACK	–	0.55	µs
tSP	Pulse width of spikes that must be suppressed by input filter	0	50	ns

19.6.2 I²S timing diagram

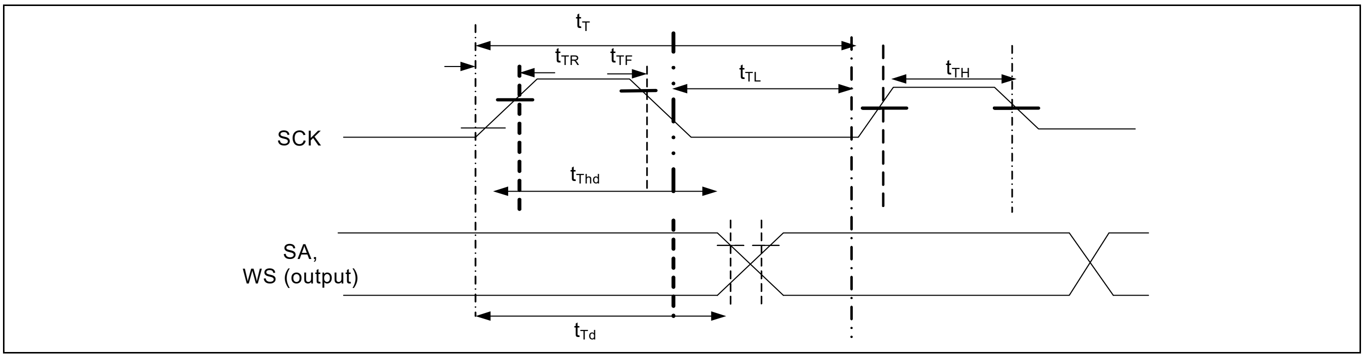


Figure 27 I²S transmit cycle

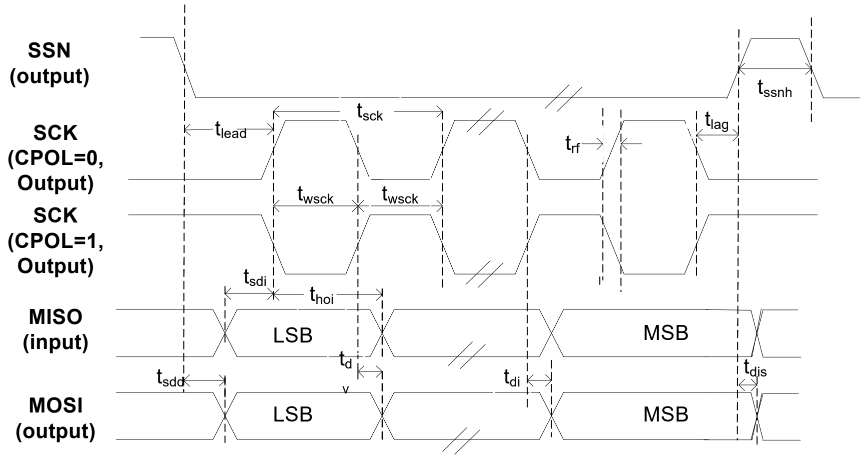
Table 21 I²S timing parameters[17]

Parameter	Description	Min	Max	Units
tT	I²S transmitter clock cycle	Ttr	–	ns
tTL	I²S transmitter cycle LOW period	0.35 × Ttr	–	ns
tTH	I²S transmitter cycle HIGH period	0.35 × Ttr	–	ns
tTR	I²S transmitter rise time	–	0.15 × Ttr	ns
tTF	I²S transmitter fall time	–	0.15 × Ttr	ns
tThd	I²S transmitter data hold time	0	–	ns
tTd	I²S transmitter delay time	–	0.8tT	ns
Note tT is selectable through clock gears. Max Ttr is designed for 96-kHz codec at 32 bits to be 326 ns (3.072 MHz).				

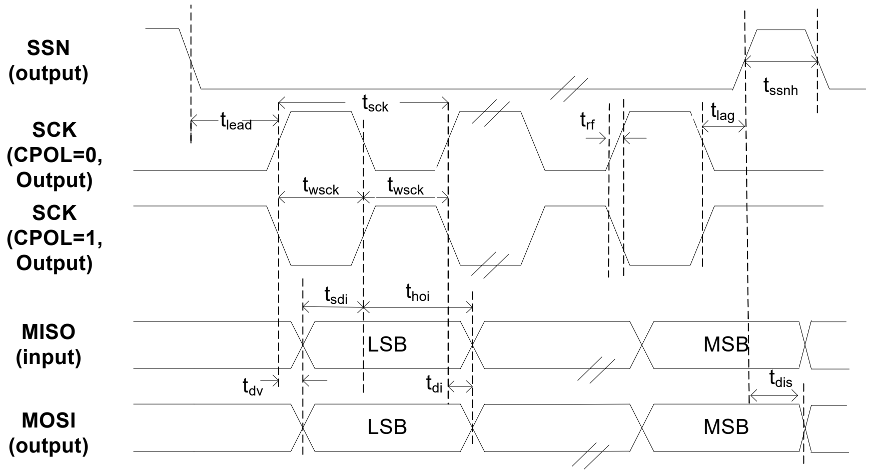
Note

[17] All parameters guaranteed by design and validated through characterization.

19.6.3 SPI timing specification



SPI Master Timing for CPHA = 0



SPI Master Timing for CPHA = 1

Figure 28 SPI timing

Table 22 SPI timing parameters[18]

Parameter	Description	Min	Max	Units
fop	Operating frequency	0	33	MHz
tsck	Cycle time	30	–	ns
twsck	Clock high/low time	13.5	–	ns
tlead	SSN-SCK lead time	1/2 tsck[19] – 5	1.5 tsck[19] + 5	ns
tlag	Enable lag time	0.5	1.5 tsck[19] + 5	ns
trf	Rise/fall time	–	8	ns
tsdd	Output SSN to valid data delay time	–	5	ns
tdv	Output data valid time	–	5	ns
tdi	Output data invalid	0	–	ns
tssnh	Minimum SSN high time	10	–	ns
tsdi	Data setup time input	8	–	ns
thoi	Data hold time input	0	–	ns
tdis	Disable data output on SSN high	0	–	ns

Notes

[18] All parameters guaranteed by design and validated through characterization.

[19] Depends on LAG and LEAD setting in the SPI_CONFIG register.

19.7 Reset sequence

FX3's hard reset sequence requirements are specified in this section.

Table 23 Reset and Standby timing parameters

Parameter	Definition	Conditions	Min (ms)	Max (ms)
tRPW	Minimum RESET# pulse width	Clock input	1	–
		Crystal input	1	–
tRH	Minimum HIGH on RESET#	–	5	–
tRR	Reset recovery time (after which Boot loader begins firmware download)	Clock input	1	–
		Crystal input	5	
tSBY	Time to enter standby/suspend (from the time MAIN_CLOCK_EN/ MAIN_POWER_EN bit is set)	–	–	1
tWU	Time to wakeup from standby	Clock input	1	–
		Crystal input	5	–
tWH	Minimum time before Standby/Suspend source may be reasserted	–	5	–

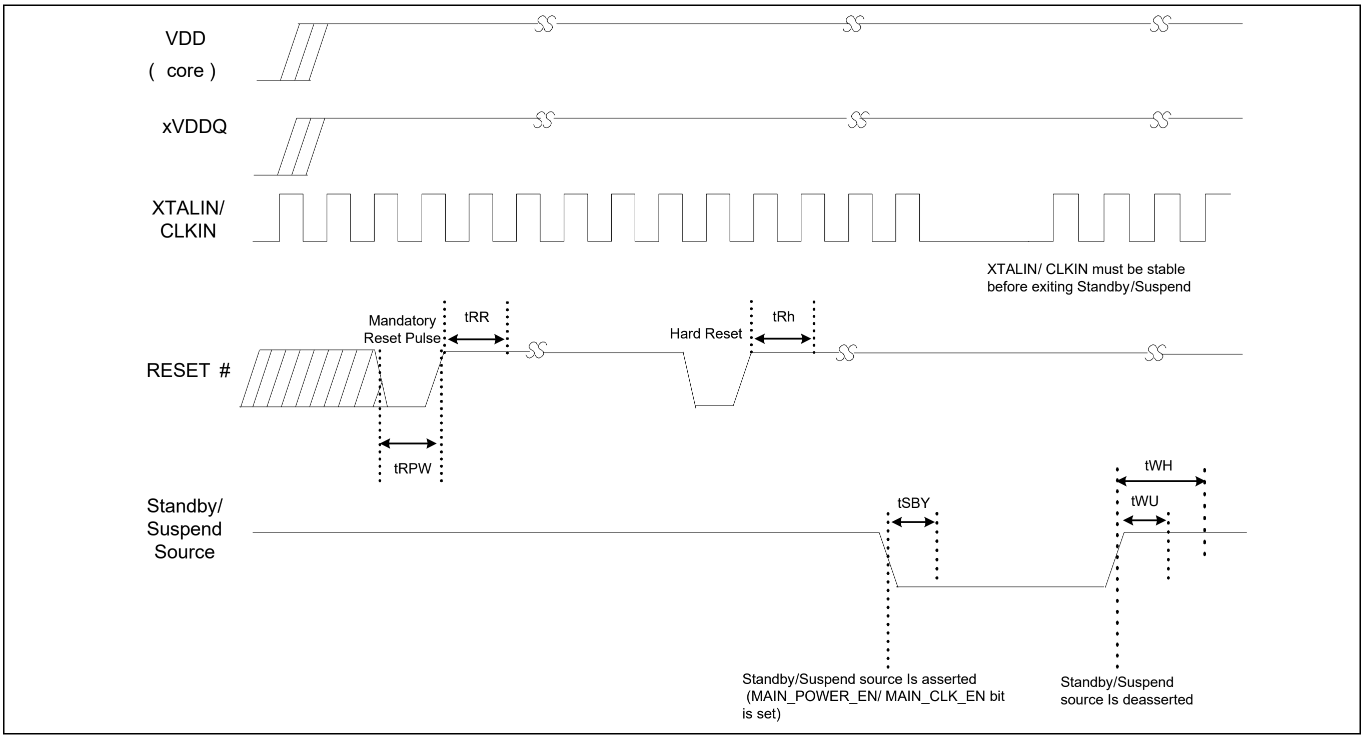
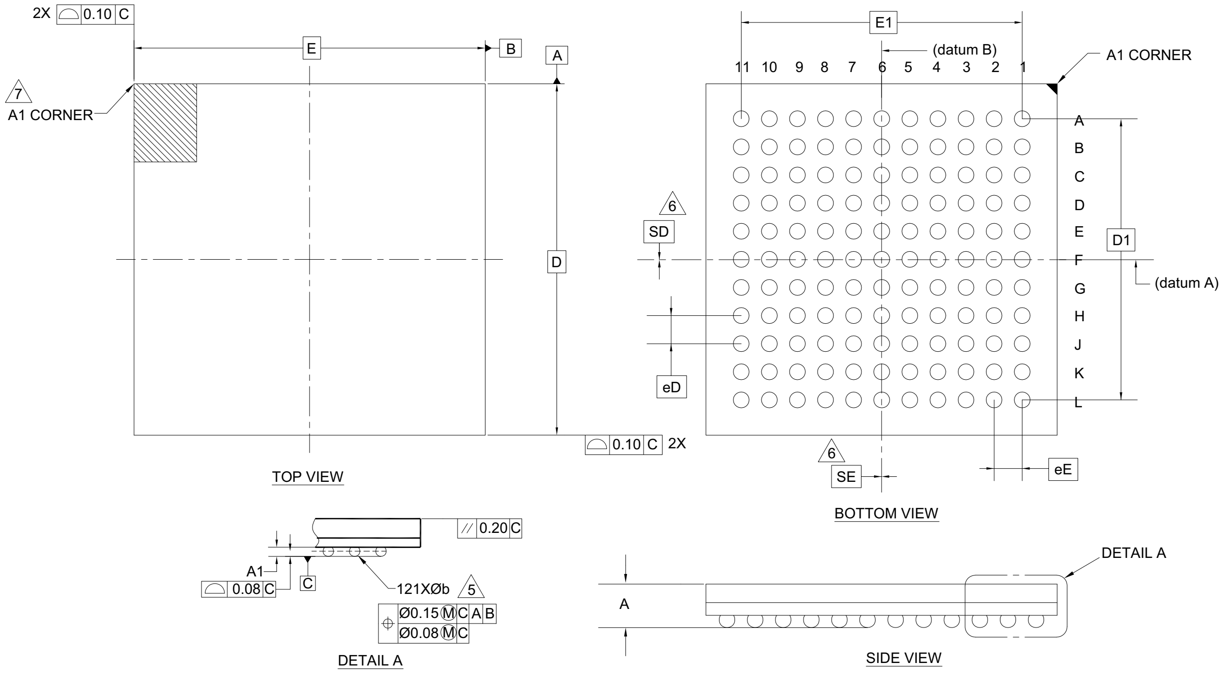


Figure 29 Reset sequence

20 Package diagram



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.20
A1	0.15	-	-
D	10.00 BSC		
E	10.00 BSC		
D1	8.00 BSC		
E1	8.00 BSC		
MD	11		
ME	11		
N	121		
∅ b	0.25	0.30	0.35
eD	0.80 BSC		
eE	0.80 BSC		
SD	0.00		
SE	0.00		

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.

001-54471 *F

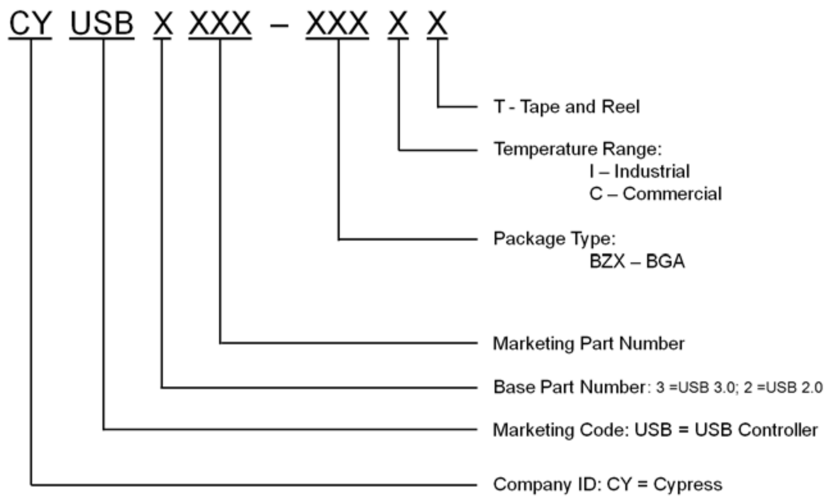
Figure 30 121-ball BGA package diagram

21 Ordering information

Table 24 Ordering information

Ordering code	USB	SRAM (kB)	GPIF II data bus width	Operating temperature	Package type
CYUSB3011-BZXC	USB 3.0	256	16-bit	0°C to +70°C	121-ball BGA
CYUSB3012-BZXC	USB 3.0	256	32-bit	0°C to +70°C	121-ball BGA
CYUSB3013-BZXC	USB 3.0	512	16-bit	0°C to +70°C	121-ball BGA
CYUSB3014-BZXC	USB 3.0	512	32-bit	0°C to +70°C	121-ball BGA
CYUSB3014-BZXI	USB 3.0	512	32-bit	–40°C to +85°C	121-ball BGA
CYUSB2014-BZXC	USB 2.0	512	32-bit	0°C to +70°C	121-ball BGA
CYUSB2014-BZXI	USB 2.0	512	32-bit	–40°C to +85°C	121-ball BGA

21.1 Ordering code definitions



22 Acronyms

Table 25 Acronyms

Acronym	Description
DMA	direct memory access
FIFO	first in, first out
GPIF	general programmable interface
HNP	host negotiation protocol
I^2C	inter-integrated circuit
I^2S	inter IC sound
MISO	master in, slave out
MOSI	master out, slave in
MMC	multimedia card
MSC	mass storage class
MTP	media transfer protocol
OTG	on-the-go
OVP	overvoltage protection
PHY	physical layer
PLL	phase locked loop
PMIC	power management IC
PVT	process voltage temperature
RTOS	real-time operating system
SCL	serial clock line
SCLK	serial clock
SD	secure digital
SD	secure digital
SDA	serial data clock
SDIO	secure digital input / output
SLC	single-level cell
SLCS	Slave Chip Select
SLOE	Slave Output Enable
SLRD	Slave Read
SLWR	Slave Write
SPI	serial peripheral interface
SRP	session request protocol
SSN	SPI slave select (Active low)
UART	universal asynchronous receiver transmitter
UVC	USB Video Class
USB	universal serial bus

23 Document conventions

23.1 Units of measure

Table 26 Units of measure

Symbol	Unit of measure
°C	degree Celsius
µA	microamperes
µs	microseconds
mA	milliamperes
Mbps	Megabits per second
MBps	Megabytes per second
MHz	mega hertz
ms	milliseconds
ns	nanoseconds
Ω	ohms
pF	pico Farad
V	volts

24 Errata

This section describes the errata for Revision D, C and B of the FX3. Details include errata trigger conditions, scope of impact, available workaround, and silicon revision applicability. Contact your local Infineon Sales Representative if you have questions.

Part numbers affected

Part number	Device characteristics
CYUSB301x-xxxx	All variants
CYUSB201x-xxxx	All variants

24.1 Qualification status

Product Status: Production

24.2 Errata summary

The following table defines the errata applicability to available Rev. D EZ-USB FX3 SuperSpeed USB Controller family devices.

Items	Part number	Silicon Revision	Fix status
1. **Turning off VIO1 during Normal, Suspend, and Standby modes causes the FX3 to stop working.**	CYUSB301x-xxxx CYUSB201x-xxxx	Rev. D, C, B	Workaround provided
2. **USB enumeration failure in USB boot mode when FX3 is self-powered.**	CYUSB301x-xxxx CYUSB201x-xxxx	Rev. D, C, B	Workaround provided
3. **Extra ZLP is generated by the COMMIT action in the GPIF II state.**	CYUSB301x-xxxx CYUSB201x-xxxx	Rev. D, C, B	Workaround provided
4. **Invalid PID Sequence in USB 2.0 ISOC data transfer.**	CYUSB301x-xxxx CYUSB201x-xxxx	Rev. D, C, B	Workaround provided
5. **USB data transfer errors are seen when ZLP is followed by data packet within same microframe.**	CYUSB301x-xxxx CYUSB201x-xxxx	Rev. D, C, B	Workaround provided
6. **Bus collision is seen when the I2C block is used as a master in the I2C Multi-master configuration.**	CYUSB301x-xxxx CYUSB201x-xxxx	Rev. D, C, B	Use FX3 in single-master configuration
7. **Low Power U1 Fast-Exit Issue with USB3.0 host controller.**	CYUSB301x-xxxx	Rev. D, C, B	Workaround provided
8. **USB data corruption when operating on hosts with poor link quality.**	CYUSB301x-xxxx	Rev. D, C, B	Workaround provided
9. **Device treats Rx Detect sequence from the USB 3.0 host as a valid U1 exit LFPS burst.**	CYUSB301x-xxxx	Rev. D, C, B	Workaround provided
10. **I2C Data Valid (tVD:DAT) specification violation at 400 kHz with a 40/60 duty cycle.**	CYUSB301x-xxxx CYUSB201x-xxxx	Rev. D, C, B	No workaround needed
11. **FX3 Device does not respond correctly to Port Capability Request from Host after multiple power cycles.**	CYUSB301x-xxxx	Rev. D, C, B	Workaround provided

1. Turning off VIO1 during Normal, Suspend, and Standby modes causes the FX3 to stop working.	
Problem definition	Turning off the VIO1 during Normal, Suspend, and Standby modes will cause the FX3 to stop working.
Parameters affected	NA
Trigger condition(s)	This condition is triggered when the VIO1 is turned off during Normal, Suspend, and Standby modes.
Scope of impact	FX3 stops working.
Workaround	VIO1 must stay on during Normal, Suspend, and Standby modes.
Fix status	No fix. Workaround is required.

2. USB enumeration failure in USB boot mode when FX3 is self-powered.	
Problem definition	When FX3 is self-powered and not connected to the USB host, it enters low-power mode and does not wake up when connected to USB host afterwards. This is because the bootloader does not check the VBUS pin on the connector to detect USB connection. It expects that the USB bus is connected to the host when it is powered on.
Parameters affected	NA
Trigger condition(s)	This condition is triggered when FX3 is self-powered in USB boot mode.
Scope of impact	Device does not enumerate
Workaround	Reset the device after connecting to USB host.
Fix status	No fix. Workaround is required.

3. Extra ZLP is generated by the COMMIT action in the GPIF II state.	
Problem definition	When COMMIT action is used in a GPIF-II state without IN_DATA action then an extra zero length packet (ZLP) is committed along with the data packets.
Parameters affected	NA
Trigger condition(s)	This condition is triggered when COMMIT action is used in a state without IN_DATA action.
Scope of impact	Extra ZLP is generated.
Workaround	Use IN_DATA action along with COMMIT action in the same state.
Fix status	No fix. Workaround is required.

4. Invalid PID Sequence in USB 2.0 ISOC data transfer.	
Problem definition	When the FX3 device is functioning as a high speed USB device with high bandwidth isochronous endpoints, the PID sequence of the ISO data packets is governed solely by the isomult setting. The length of the data packet is not considered while generating the PID sequence during each microframe. For example, even if a short packet is being sent on an endpoint with MULT set to 2; the PID used will be DATA2.
Parameters affected	NA
Trigger condition(s)	This condition is triggered when high bandwidth ISOC transfer endpoints are used.
Scope of impact	ISOC data transfers failure.
Workaround	This problem can be worked around by reconfiguring the endpoint with a lower isomult setting prior to sending short packets, and then switching back to the original value.
Fix status	No fix. Workaround is required.

5. USB data transfer errors are seen when ZLP is followed by data packet within same microframe.	
Problem definition	Some data transfer errors may be seen if a ZLP is followed very quickly (within one microframe or 125 µs) by another data packet on a burst enabled USB IN endpoint operating at super speed.
Parameters affected	NA
Trigger condition(s)	This condition is triggered in SuperSpeed transfer with ZLPs
Scope of impact	Data failure and lower data speed.
Workaround	The solution is to ensure that some time is allowed to elapse between a ZLP and the next data packet on burst enabled USB IN endpoints. If this cannot be ensured at the data source, the CyU3PDmaChannelSetSuspend() API can be used to suspend the corresponding USB DMA socket on seeing the EOP condition. The channel operation can then be resumed as soon as the suspend callback is received.
Fix status	No fix. Workaround is required.

6. Bus collision is seen when the I^2C block is used as a master in the I^2C Multi-master configuration.	
Problem definition	When FX3 is used as a master in the I^2C multi-master configuration, there can be occasional bus collisions.
Parameters affected	NA
Trigger condition(s)	This condition is triggered only when the FX3 I^2C block operates in Multi-master configuration.
Scope of impact	The FX3 I^2C block can transmit data when the I^2C bus is not idle leading to bus collision.
Workaround	Use FX3 as a single master.
Fix status	No fix.

7. Low Power U1 Fast-Exit Issue with USB3.0 host controller.	
Problem definition	When FX3 device transitions from Low power U1 state to U0 state within 5 µs after entering U1 state, the device sometimes fails to transition back to U0 state, resulting in USB Reset.
Parameters affected	NA
Trigger condition(s)	This condition is triggered during low power transition mode.
Scope of impact	Unexpected USB warm reset during data transfer.
Workaround	This problem can be worked around in the FW by disabling LPM (Link Power Management) during data transfer.
Fix status	FW workaround is proven and reliable.

8. USB data corruption when operating on hosts with poor link quality.	
Problem definition	If FX3 is operating on a USB 3.0 link with poor signal quality, the device could send corrupted data on any of the IN endpoints (including the control endpoint).
Parameters affected	NA
Trigger condition(s)	This condition is triggered when the USB3.0 link signal quality is very poor.
Scope of impact	Data corruption in any of the IN endpoints (including the control endpoint).
Workaround	The application firmware should perform an error recovery by stalling the endpoint on receiving CYU3P_USBEPSS_RESET_EVT event, and then stop and restart DMA path when the CLEAR_FEATURE request is received. **Note:** SDK versions 1.3.3 and above internally manages the DMA transfers and performs the endpoint reset when potential error conditions are seen. For more details in application firmware, please refer to **GpiftoUsb** example available with SDK.
Fix status	FW Work-around is proven and reliable.

9. Device treats Rx Detect sequence from the USB 3.0 host as a valid U1 exit LFPS burst.	
Problem definition	The USB 3.0 PHY in the FX3 device uses an electrical idle detector to determine whether LFPS is being received. The duration for which the receiver does not see an electrical idle condition is timed to detect various LFPS bursts. This implementation causes the device to treat an Rx Detect sequence from the USB host as a valid U1 exit LFPS burst.
Parameters affected	NA
Trigger condition(s)	This condition is triggered when the USB host is initiating an Rx Detect sequence while the USB 3.0 Link State Machine on the FX3 is in the U1 state. Since the host will only perform Rx Detect sequence in the RX Detect and U2 states, the error condition is seen only in cases where the USB link on the host has moved into the U2 state while the link on FX3 is in the U1 state.
Scope of impact	FX3 moves into Recovery prematurely leading to a Recovery failure followed by Warm Reset and USB re-enumeration. This sequence can repeat multiple times resulting in data transfer failures.
Workaround	FX3 can be configured to transition from U1 to U2 a few microseconds before the host does so. This will ensure that the link will be in U2 on the device side before the host attempts any Rx Detect sequence; thereby preventing a false detection of U1 exit.
Fix status	Workaround is implemented in FX3 SDK library 1.3.4 and above.

10. I^2C Data Valid (tVD:DAT) specification violation at 400 kHz with a 40/60 duty cycle.	
Problem definition	I^2C Data Valid (tVD:DAT) parameter at 400 kHz with a 40/60 duty cycle is 1.0625 µs, which exceeds the I^2C specification limit of 0.9 µs.
Parameters affected	NA
Trigger condition(s)	This violation occurs only at 400 kHz with a 40/60 duty cycle of the I^2C clock.
Scope of impact	Setup time (t_{SUDAT}) is met with a huge margin for the transmitted data for 400 kHz and so $t_{vd:DAT}$ violation will not cause any data integrity issues.
Workaround	No workaround needed.
Fix status	No fix needed.

11.FX3 Device does not respond correctly to Port Capability Request from Host after multiple power cycles.	
Problem definition	During multiple power cycles, sometimes the FX3 device does not respond correctly to the Port Capability request (Link Packet) from the USB Controller. In view of this, FX3 does not get the subsequent Port Configuration request from the USB controller, resulting in SS.Disabled state. The device fails to recover from this state and finally results in enumeration failure.
Parameters affected	NA
Trigger condition(s)	This condition is triggered when the FX3 provides an incorrect response to the Port Capability request from the host.
Scope of impact	Device fails to enumerate after multiple retries.
Workaround	Since the host does not send the Port Configuration request to the FX3 device, it causes a Port Configuration request timeout interrupt to be triggered in the device. This interrupt is handled in the FX3 SDK 1.3.4 onwards to generate and signal CY_U3P_USB_EVENT_LMP_EXCH_FAIL event to the application. This event should be handled in the user application such that it does a USB Interface Block Restart. Refer the Knowledge Base Article (**KBA225778**) for more details and the firmware workaround example project.
Fix status	Suggested firmware work-around is proven and reliable.

Revision history

Document revision	Date	Description of changes
**	2009-03-06	New data sheet.
*A	2009-09-01	Updated the part# from CYX01XXBB to CYUSB3011-BZXI Changed status from "ADVANCE" to "ADVANCE INFORMATION" In page 1, the second bullet (Flexible Host Interface), add "32-bit, 100 MHz" to first sub bullet. In page 1, changed the second bullet "Flexible Host Interface" to General Programmable Interface". In page 1, the second bullet (Flexible Host Interface), removed "DMA Slave Support" and "MMC Slave support with Pass through Boot" sub bullets. In page 1, third bullet, changed "50 µA with Core Power" to "60 µA with Core Power" In page 1, fifth bullet, added "at 1 MHz" In page 1, seventh bullet, added "up to 4 MHz" to UART In page 1, Applications Section, move "Digital Still Cameras" to second line. In page 1, Applications Section, added "Machine Vision" and Industrial Cameras" Added ™ to GPIF and FX3. In page 1, updated Logic Block Diagram. In page 2, section of "Functional Overview", updated the whole section. In page 2, removed the section of "Product Interface" In page 2, removed the section of "Processor Interface (P-Port)" In page 2, removed the section of "USB Interface (U-Port)" In page 2, removed the section of "Other Interfaces" In page 2, added a section of "GPIF II" In page 2, added a section of "CPU" In page 2, added a section of "JTAG Interface" In page 2, added a section of "Boot Options" In page 2, added a section of "ReNumeration" In page 2, added a section of "Power" In the section of "Package", replaced "West Bridge USB 3.0 Platform" by FX3. In the section of "Package", added 0.8 mm pitch in front of BGA. Added Pin List (**Table 1**)
*B	2009-09-29	Changed title to EZ-USB™ FX3: SuperSpeed USB Controller **Features**: Added the thrid bullet "Fully accessible 32-bit ARM9 core with 512kB of embedded SRAM" Added the thrid line "EZ USB™ Software and DVK for easy code development" **Table 1**: Pin 74, corrected to NC - No Connect.
*C	2009-12-08	Added data sheet to the USB 3.0 EROS spec 001-51884. No technical updates.

Document revision	Date	Description of changes
*D	2010-11-08	Changed status from Advance to Preliminary. Changed part number from CYUSB3011 to CYUSB3014 Added the following sections: **Power**, **Digital I/Os**, **Digital I/Os**, **System-level ESD**, **DC specifications**, **AC timing parameters**, **Reset sequence**, **Package diagram** Added **DC specifications** table Updated feature list Updated Pin List Added support for selectable clock input frequencies. Updated block diagram Updated part number Updated package diagram
*E	2011-03-24	Updated Slave FIFO protocol and added ZLP signaling protocol Changed GPIFII asynchronous tDO parameter Changed Async Slave FIFO tOE parameter Changed Async Slave FIFO tRDO parameter Added tCOE parameter to GPIFII Sync mode timing parameters Renamed GPIFII Sync mode tDO to tCO and tDO_ss0 to tCO_ss0 Modified description of GPIFII Sync tCO (previously tDO) parameter Changed tAH(address hold time) parameter in Async Slave FIFO modes to be with respect to rising edge of SLWR#/SLRD# instead of falling edge. Correspondingly, changed the tAH number. Removed 24 bit data bus support for GPIFII.
*F	2011-04-07	Minor ECN - Release to web. No content changes.
*G	2011-04-20	Minor updates in Features.
*H	2011-04-06	Updated GPIFII Synchronous Timing diagram. Added SPI Boot option. Corrected values of R_USB2 and R_USB3. Corrected TCK and TRST# pull-up/pull-down configuration. Minor updates to block diagrams. Corrected Synchronous Slave FIFO tDH parameter.
*I	2011-07-07	Minor ECN - Correct ECN number in revision *F. No content changes.
*J	2011-12-06	Changed datasheet status from Preliminary to Final. Changed tWRPE parameter to 2 ns Updated tRR and tRPW for crystal input Added clarification regarding IOZ and IIX Updated Sync SLave FIFO Read timing diagram Updated SPI timing diagram Removed tGRANULARITY parameter Updated I2S Timing diagram and tTd parameter Updated 121-ball BGA package diagram. Added clarification regarding VCC in DC Specifications table In Power Modes description, stated that VIO1 cannot be turned off at any time if the GPIFII is used in the application Updated Absolute Maximum Ratings Added requirement for by-pass capacitor on U3RXVDDQ and U3TXVDDQ Updated tPEI parameter in Async Slave FIFO timing table Updated Sync Slave FIFO write and read timing diagrams Updated I2C interface tVD:ACK parameter for 1MHz operation Clarified that CTL[15] is not usable as a GPIO
*K	2012-02-24	Corrected typo in the block diagram.

Document revision	Date	Description of changes
*L	2012-08-16	Changed part number to CYUSB301X. Added 256 KB range for embedded SRAM. Updated Functional Overview, Other Interfaces, and Clocking sections. Added Pin List for CYUSB3011 and CYUSB3013 parts. Updated **Ordering information**: Updated part numbers.
*M	2012-12-20	Updated 121-ball BGA package diagram to current revision.
*N	2013-05-31	Included Commercial Temperature Range related information in all instances across the document. Included 131-ball WLCSP Package related information in all instances across the document. Updated **Pin description**: Updated **Table 7**. Updated **Package diagram**: Added 131-ball WLCSP Package Diagram. Updated **Ordering information**: Updated part numbers.
*O	2014-05-02	Updated **Package diagram**: spec 001-62221 – Changed revision from *B to *C. Updated to new template. Completing Sunset Review.
*P	2014-08-14	Added CYUSB201x MPNs, ball map, and pin list to the datasheet.

Document revision	Date	Description of changes
*Q	2015-02-24	Updated **Features**: Updated description. Updated **Logic block diagram**. Updated **Functional description**: Added "For a complete list of related documentation, click **here**." at the end. Added **More information**. Updated **Functional overview**: Updated **Application examples**: Updated **Figure 1**. Updated **Figure 2**. Updated **USB interface**: Updated description. Removed Figure "USB Interface Signals". Updated **Reset**: Updated **Hard reset**: Updated description. Updated **Pin configurations**: Updated **Figure 6**. Updated **Pin description**: Updated **Table 7**: Updated entire table. Modified CVDDQ power domain description. Removed Table "CYUSB3011 and CYUSB3013 Pin List (GPIF II with 16-bit Data Bus Width)". Removed Table "CYUSB2014 Pin List (GPIF II with 32-bit Data Bus Width)". Updated **DC specifications**: Added ISS parameter and its details. Updated **Slave FIFO interface**: Updated **Synchronous Slave FIFO Read sequence description**: Updated **Figure 11**. Updated **Synchronous Slave FIFO Write sequence description**: Updated **Figure 12**. Updated **Table 15**. Updated **AC timing parameters**: Added **Host Processor Interface (P-Port) timing**. Updated **Acronyms**. Added **Errata**. Replaced West Bridge Benicia with FX3.
*R	2015-03-27	Updated **Slave FIFO interface**: Updated **Synchronous Slave FIFO Read sequence description**: Updated **Figure 11**. Updated **Synchronous Slave FIFO Write sequence description**: Updated **Figure 12**. Updated **Table 15**: Updated minimum value of tSSD parameter. Added tACCD, tFAD parameters and their details.

Document revision	Date	Description of changes
*S	2016-04-07	Updated **Electrical specifications**: Updated **DC specifications**: Updated **Table 8** (Removed I_{SS} parameter and its corresponding details). Updated **Errata**: Updated **Errata summary**: Updated description. Added item “Bus collision is seen when the I^2C block is used as a master in the I^2C Multi-master configuration.” and its corresponding details in the table.
*T	2016-06-29	Updated **AC timing parameters**: Updated **GPIF II timing**: Updated **Table 13**: Changed maximum value of t_{CO} parameter from 8 ns to 7 ns. Updated **Slave FIFO interface**: Updated **Synchronous Slave FIFO Write sequence description**: Updated **Table 15**: Changed maximum value of t_{CO} parameter from 8 ns to 7 ns. Updated to new template.
*U	2017-04-20	Updated Cypress Logo and Copyright.
*V	2018-02-19	Removed 131-ball WLCSP Package related information in all instances across the document. Updated **Package diagram**: spec 001-54471 – Changed revision from *E to *F. Updated to new template.

Document revision	Date	Description of changes
*W	2018-09-25	Updated **Features**: Updated description. Updated **More information**: Updated description. Updated **Functional overview**: Updated description. Updated **USB interface**: Removed "EZ-Dtect". Updated **JTAG interface**: Updated description. Updated **Other interfaces**: Updated **I2S interface**: Updated description. Updated **Boot options**: Updated description. Updated **Power**: Updated description. Updated **Table 6**. Updated **Pin configurations**: Updated **Figure 6**. Updated **Figure 7**. Updated **Pin description**: Updated **Table 7**. Updated **Electrical specifications**: Updated **DC specifications**: Updated **Table 8**. Added **Table 9**. Added **Thermal characteristics**. Updated **AC timing parameters**: Added **GPIF II lines AC characteristics at 100 MHz**. Added **GPIF II PCLK jitter characteristics**. Updated **Errata**: Updated description. Updated **Errata summary**: Updated description. Updated details in "Silicon Revision" column for all items in the table. Added items "Low Power U1 Fast-Exit Issue with USB3.0 host controller.", "USB data corruption when operating on hosts with poor link quality.", "Device treats Rx Detect sequence from the USB 3.0 host as a valid U1 exit LFPS burst.", "I^{2}C Data Valid (tVD:DAT) specification violation at 400 kHz with a 40/60 duty cycle." and their corresponding details in the table.
*X	2018-12-17	Updated **Pin description**: Updated **Table 7**. Updated **Errata**: Updated **Errata summary**: Updated description. Added item "FX3 Device does not respond correctly to Port Capability Request from Host after multiple power cycles." and its corresponding details in the table.

Document revision	Date	Description of changes
*Y	2022-08-11	Updated Document Title to read as “CYUSB301X, CYUSB201X, EZ-USB FX3 SuperSpeed USB Controller”. Added a note on Errata in page 2. Updated **More information**: Updated description. Added hyperlink in required places. Updated **Functional overview**: Updated **Application examples**: Updated **Figure 1**. Updated **Figure 2**. Updated **USB interface**: Updated description. Updated **Boot options**: Updated description. Updated **Errata**: Updated **Errata summary**: Updated details in “[Part Number]” column for Errata items 7, 8, 9, and 11. Migrated to Infineon template.
*Z	2022-09-29	Updated **Features**: Updated description. Updated **More information**: Updated description. Updated hyperlinks. Updated **Functional overview**: Updated description. Updated **USB interface**: Updated description. Updated **Boot options**: Updated description. Updated **Table 2**. Updated **Electrical specifications**: Updated **Absolute maximum ratings**: Updated details corresponding to “Latch-up current”. Updated **Pin description**: Updated **Table 7**.