User Manual

DA14706 PRO Development Kit

UM-B-148

Abstract

This document contains hardware description of the DA14706 PRO development kit, including DA14706 or DA14708 PRO daughterboards, PRO motherboard and the accompanying boards which mounted on the motherboard, namely the LCD module and the power measurement module.

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1 Terms and Definitions

AFE	Analog Front End
BLE	Bluetooth® Low Energy
Dev Kit	Development Kit
PRO-Devkit	Professional Development Kit
PRO-DB	PRO-Daughterboard
PRO-MB	PRO-Motherboard
DB	Daughterboard
MB	Mainboard or Motherboard
OPAMP	Operational Amplifier
OVP	Over Voltage Protection
PCB	Printed Circuit Board
SDK	SW Development Kit
SWD	Serial Wire Debug
HDK	HW Development Kit

2 References

[1] Device specification, DA1470x Datasheet

[2] HW Design, PRO-Motherboard, da1470x-mb_[500-05-x]

[3] HW Design, PRO-daughterboard, da1470x-db-vfbga142_[500-06-x]

[4] HW Design, Current Sense, da1470x-sb-pmm2_[500-29-x]

[5] HW Design, LCD, da1470x-sb-ctspilcd_[500-31-x]

3 Introduction DA14706 PRO Development Kit

3.1 Introduction

The DA14706 PRO Development kit consists of the PRO-Motherboard and PRO-daughterboard.

Special attention for the design of this kit is directed at providing a trouble-free user experience and keeping compatibility with the existing tools from the DA1458x/DA1468x/DA1469x product lines.

When combined with the DA1470x SDK and SmartSnippets tools, the PRO development kit provides an easy to use and complete platform for software/hardware development.

In this document we focus on the DA14706 PRO Development kit which has the following parts:

- PRO-Motherboard (PRO-MB)
  - da1470x-mb, PCBA reference number 500-05-x
- PRO-daughterboard (PRO-DB)
  - **da1470x-db-vfbga142,** PCBA reference number **500-06-x**
- Power Measurement Module 2 (PMM2) add-on
  - **da1470x-sb-pmm2, PCB reference number 500-29-x**
- LCD add-on for TFT 390x390
  - **da1470x-sb-ctspilcd, PCB reference number 500-31-x**

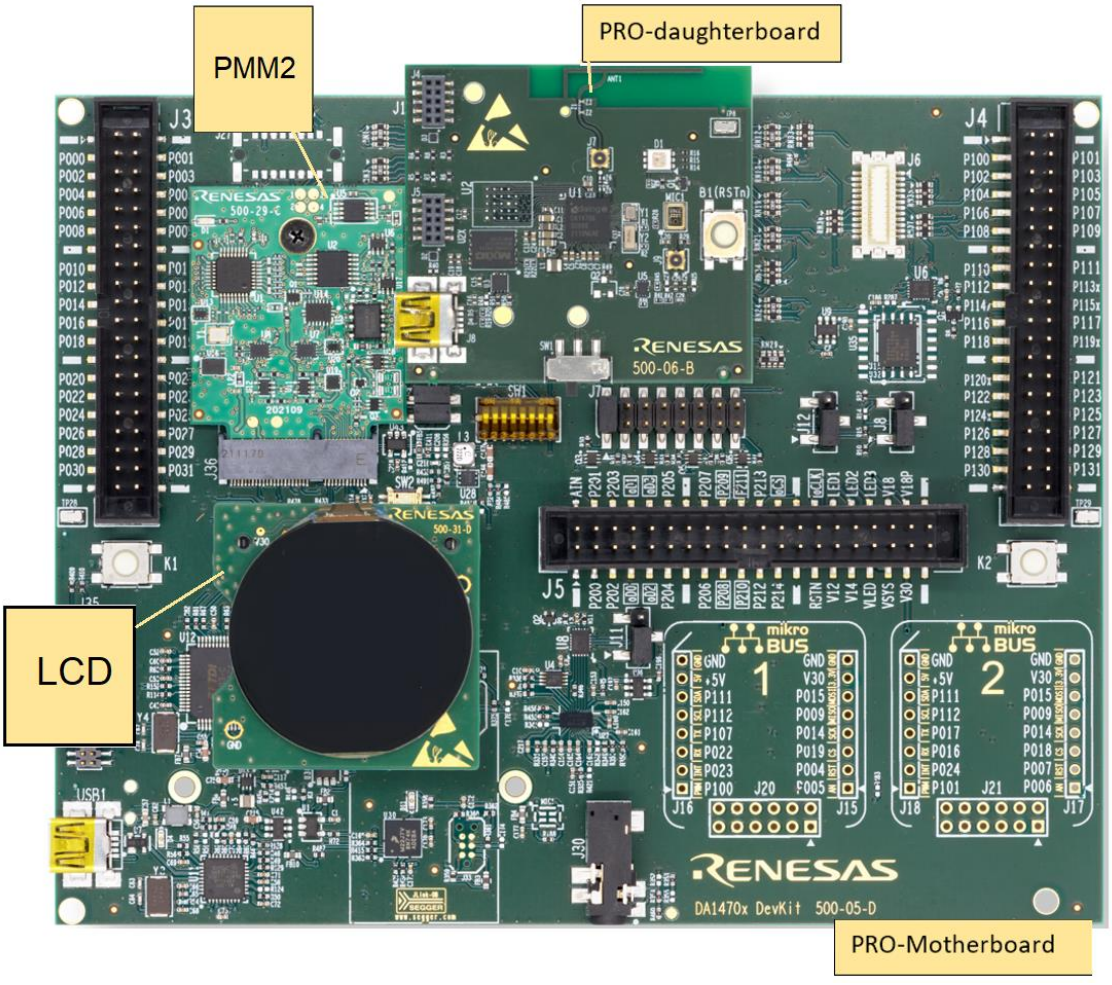


Figure 1: DA14706 PRO Development Kit

3.2 Features

- DA1470x silicon easily replaceable on a daughterboard core module
- Dedicated daughterboard for current measurement (on a M2 socket)
- LCD daughterboard
- On-board basic peripherals for demo and development
- Look and feel like previous PRO-Development kits
- Flexible and robust power options
- SWD debugger on Board and connectivity to PC for M33 and SNC
- Voltage translation section for minimizing leakage
- DIP switches for breaking-up certain signal allowing power measurements and debugging
- Header for SWD debugger for CMAC
- 64 Mbit, QSPI NOR Flash memory for eXecute in Place (XiP)
- 256 Mbit Storage QSPI NOR Flash
- 64 Mbit QSPI RAM
- Break-out header (J6) for connecting an add-on board with eMMC (DA14708) or other peripheral
- Headers for I/O monitoring and expandability1
- Audio codec with jack speaker phone and digital mic capabilities
- Analog Microphone
- RGB LED
- Two general purpose Push Buttons
- Option to support two MikroBUS click boards and other interface boards via the two generic slots could be used as PMOD socket
- Generic SPI expansion header (J27)
- Provisions for automated test

3.3 PRO Development Kit Hardware Block Diagram

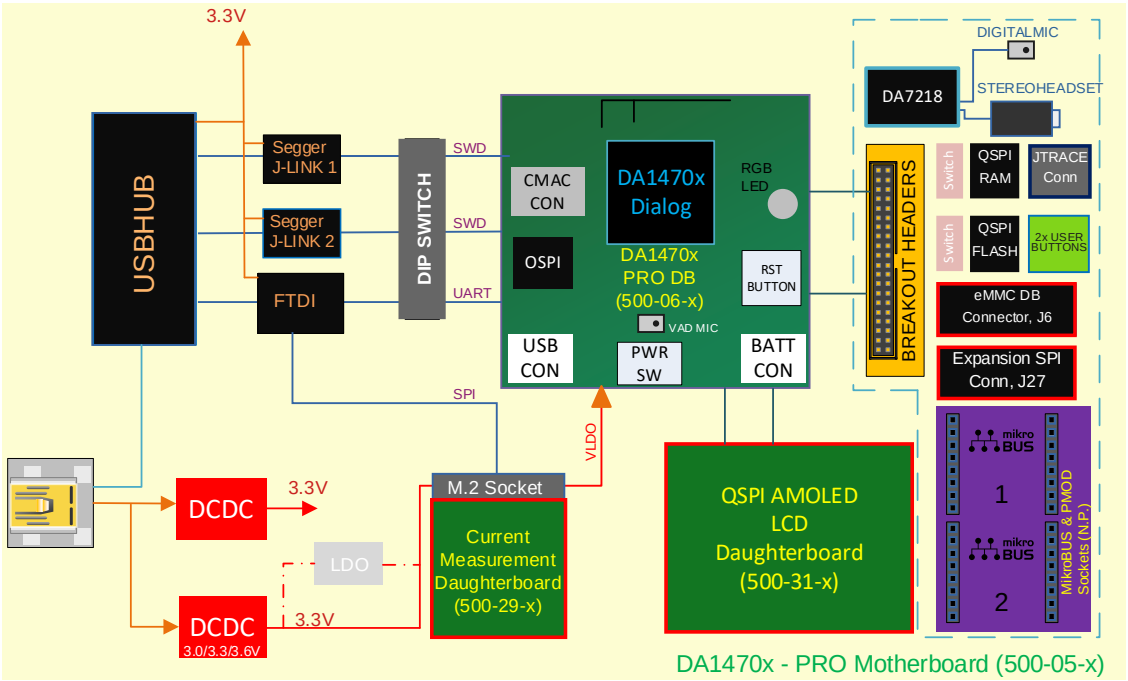


Figure 2: System Block Diagram

4 PRO-Motherboard Main Features

- Single USB connector

Note that USB host must support USB 2.0 high-speed for reliable power measurements

- USB hub with 3 downstream ports
  - Port1: Segger JLink-OB SWD-JTAG debugger for ARM Cortex M33
  - Port2: FT2232H multiprotocol serial interface providing a booting/debugging/HCI UART (2 or 4-pin) and SPI connected to the current measurement daughterboard A/D converter
  - Port3: Segger JLink-OB SWD-JTAG debugger for SNC
- 2 Connectors mating to the DA1470x daughterboard
- Breakout Headers (3 pcs 2x20pin) for monitoring GPIO and power signals, with markings of signal names on the PCB top silkscreen (Figure 3)
- Two user buttons, K1 and K2 connected to GPIOs through header J35
- DIP switch to isolate UART and SWD signals (in case we need to secure the most accurate sleep current measurements)
- Test points on the bottom layer
- Ground points (TP28, TP29) for connecting crocodile clips
- QSPI-RAM with option to disconnect the related GPIOs from the long traces travelling to breakout headers & MikroBUS sockets

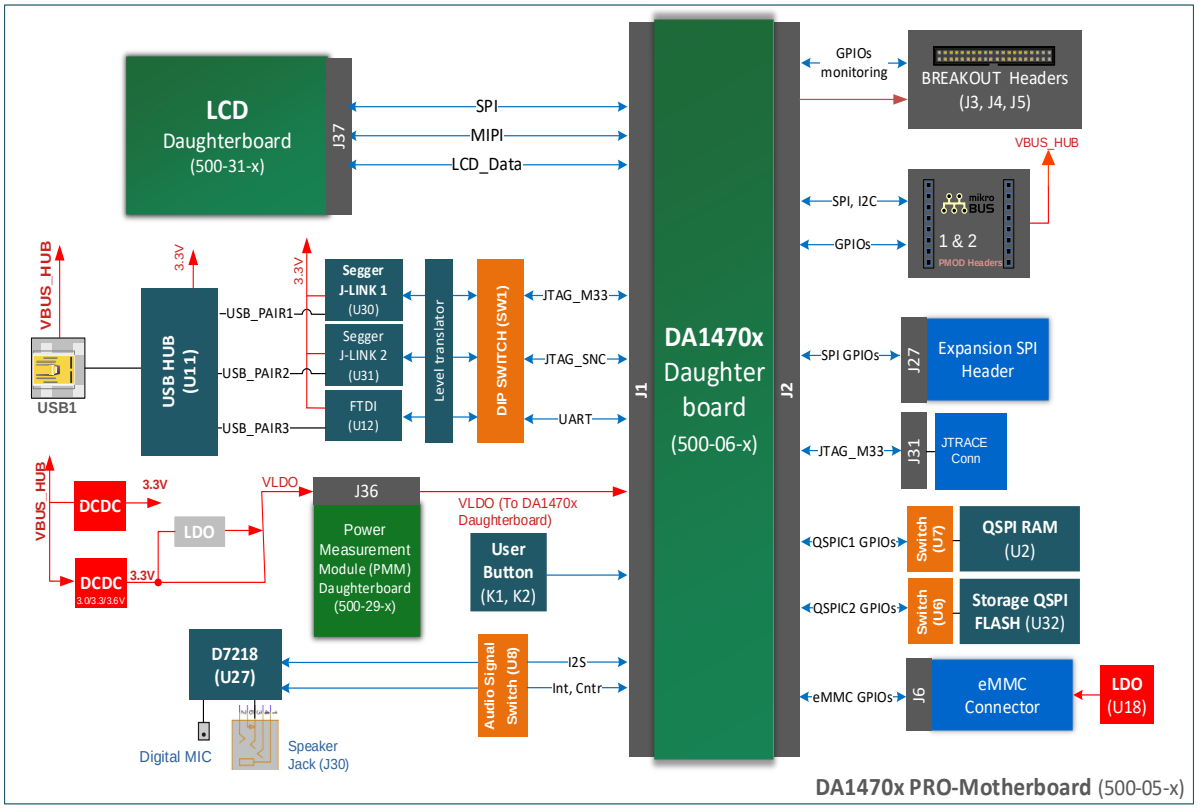


Figure 3: Engineering Level, Voltage and Interface, PRO-Motherboard Block Diagram

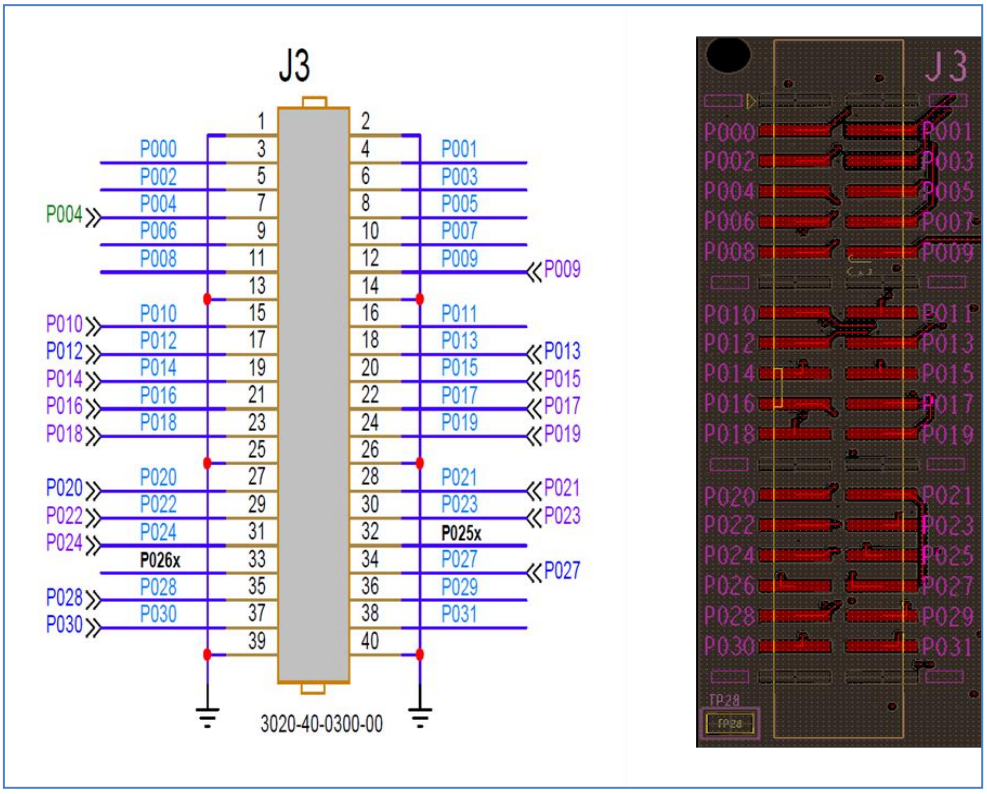


Figure 4: Monitoring Header J3: Schematic (Left) and PCB (Right)

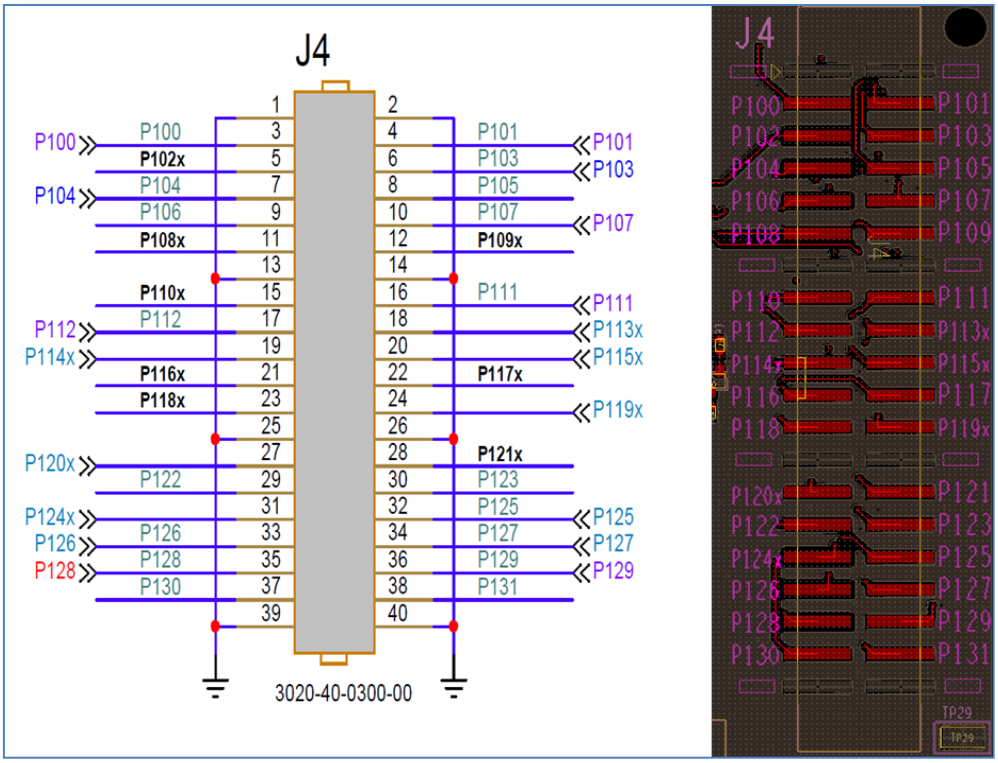


Figure 5: Monitoring Header J4: Schematic (Left) & PCB (Right)

- QSPI flash (with three footprint options)
- Dedicated connector (J6) (see Figure 3) which can accept an eMMC flash daughterboard
- Optional 2x MikroBUS sockets (supporting 3.3 V compatible click boards)

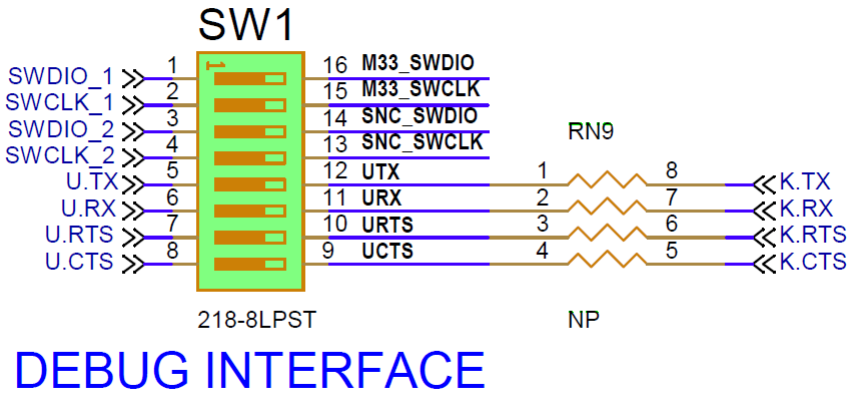


Figure 6: Debug Interface Including DIP Switch SW1

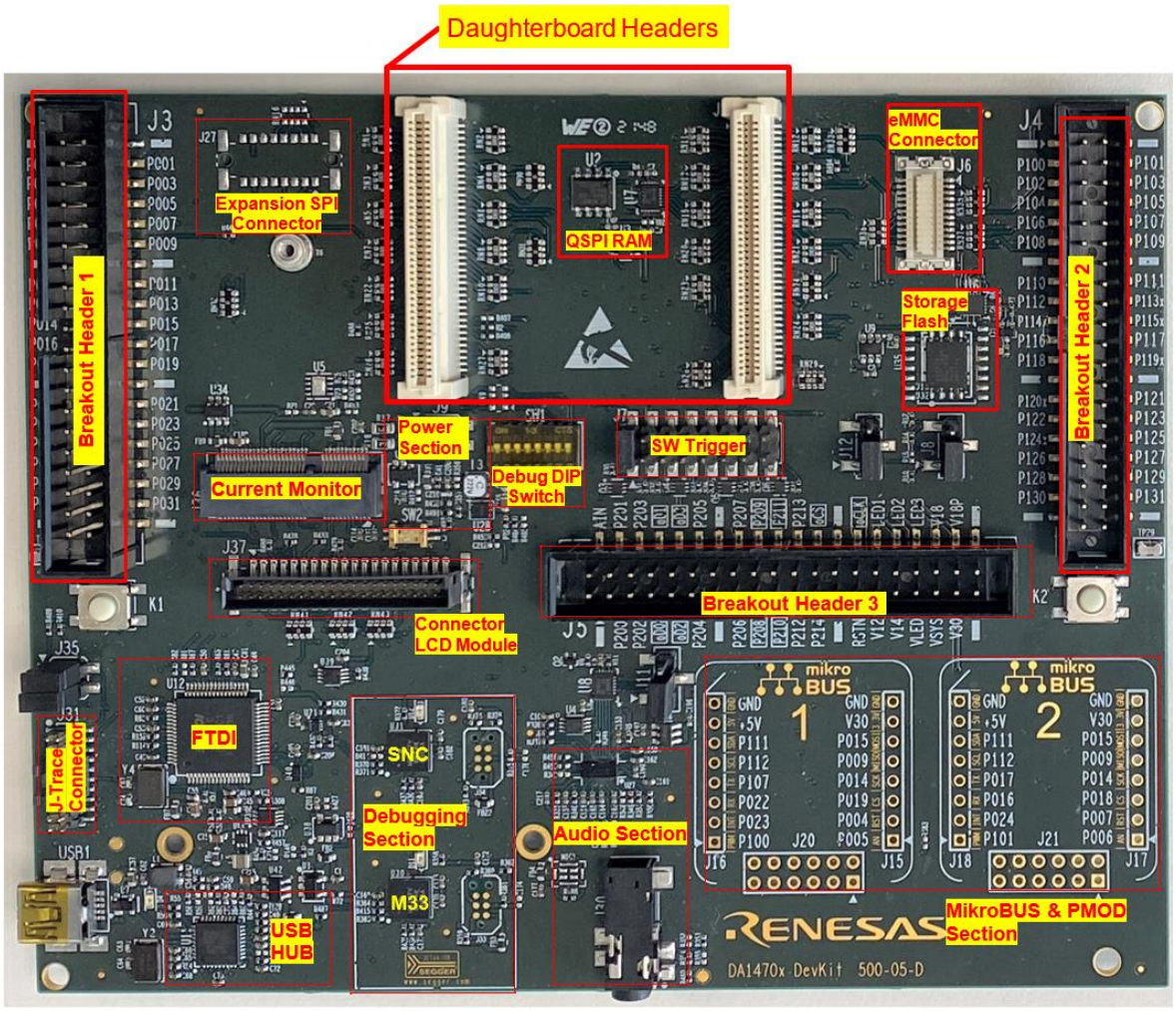


Figure 7: PCB Top of the DA1470x PRO Development Kit Top

4.1 USB Hub

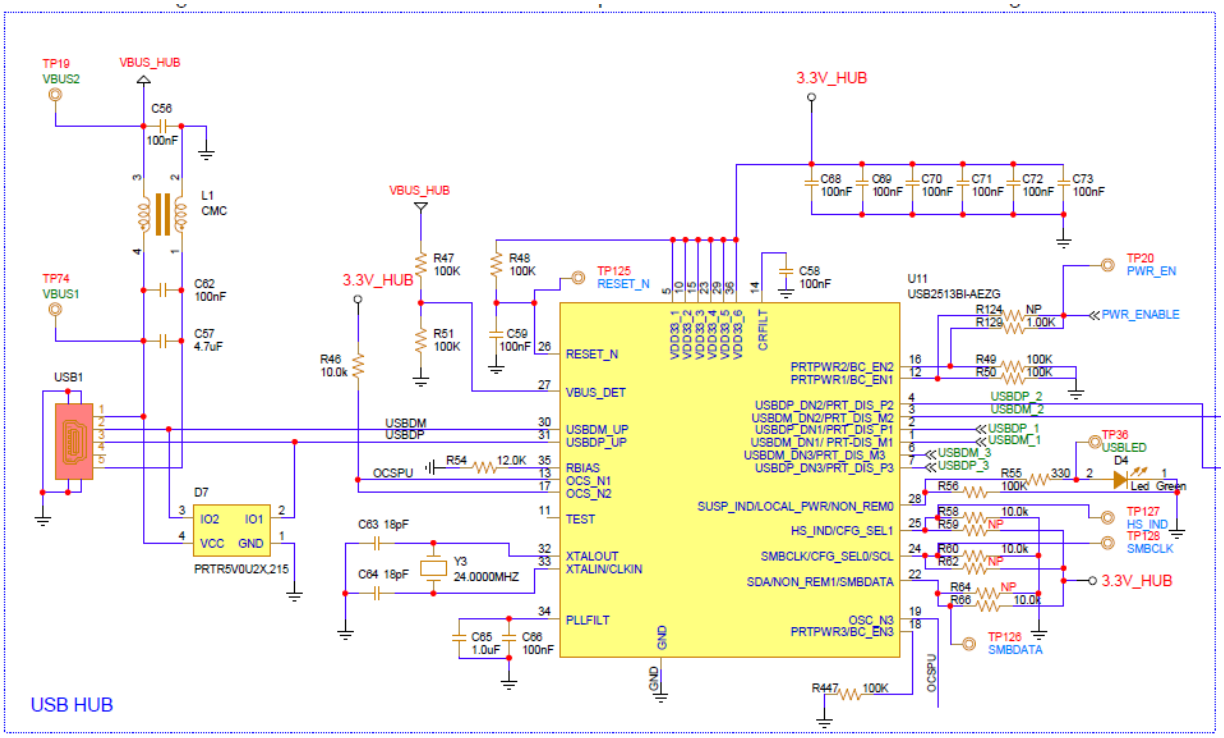


Figure 8: USB hub Circuitry of DA14706 PRO-Motherboard

The USB hub of DA14706 PRO-Motherboard is implemented by U11, USB2513B. This chip is supplied with 3.3 V from a voltage regulator, U13.

The signal PWR_ENABLE is generated from U11 and it is an active high signal. It enables the power components (DCDC converter and power switches) for UART, SWD. The system will power up only after the USB hub has enumerated properly.

Its operation is indicated via the green LED D4 on the motherboard. A 24 MHz crystal (Y3) is required.

4.2 USB to UART

The USB to UART function is implemented by U12, FT2232HL. This chip is supplied with 3.3 V from U13. A 12 MHz crystal (Y4) is required for the chip operation.

Functions served by U12 are as follows:

- Connecting a PC to the UART port of DA1470x SoC
- Connecting a PC to the current sensing circuitry:
  - Software cursor triggering (C_TRIG)

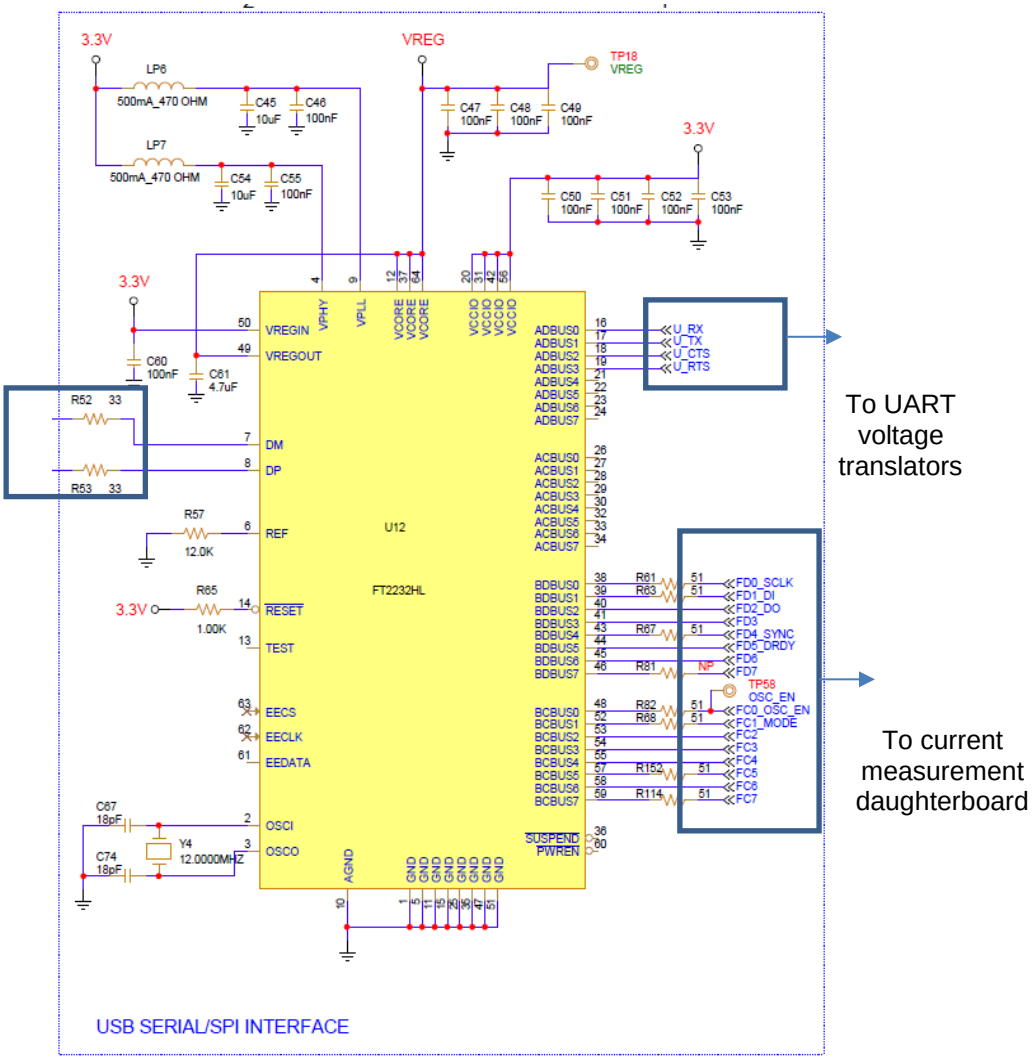


Figure 9: USB to UART (FTDI Module)

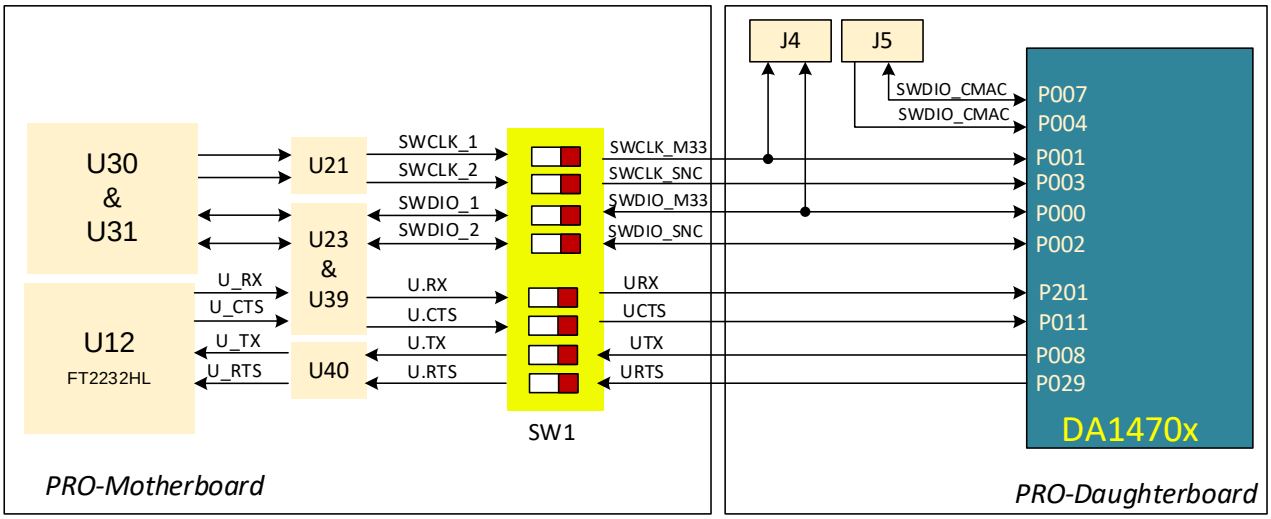


Figure 10: UART and SWD Signals

4.3 USB to Serial Wire Debug Port (SWD)

DA1470x SoC contains three processors, the main processor M33, the SNC, and the CMAC. Each of them can be accessed by a SWD port. M33 and SNC are accessed from the debuggers on board (U30 and U31 respectively) which are located on the PRO-Motherboard. CMAC can be accessed by a connector on PRO-Daughterboard.

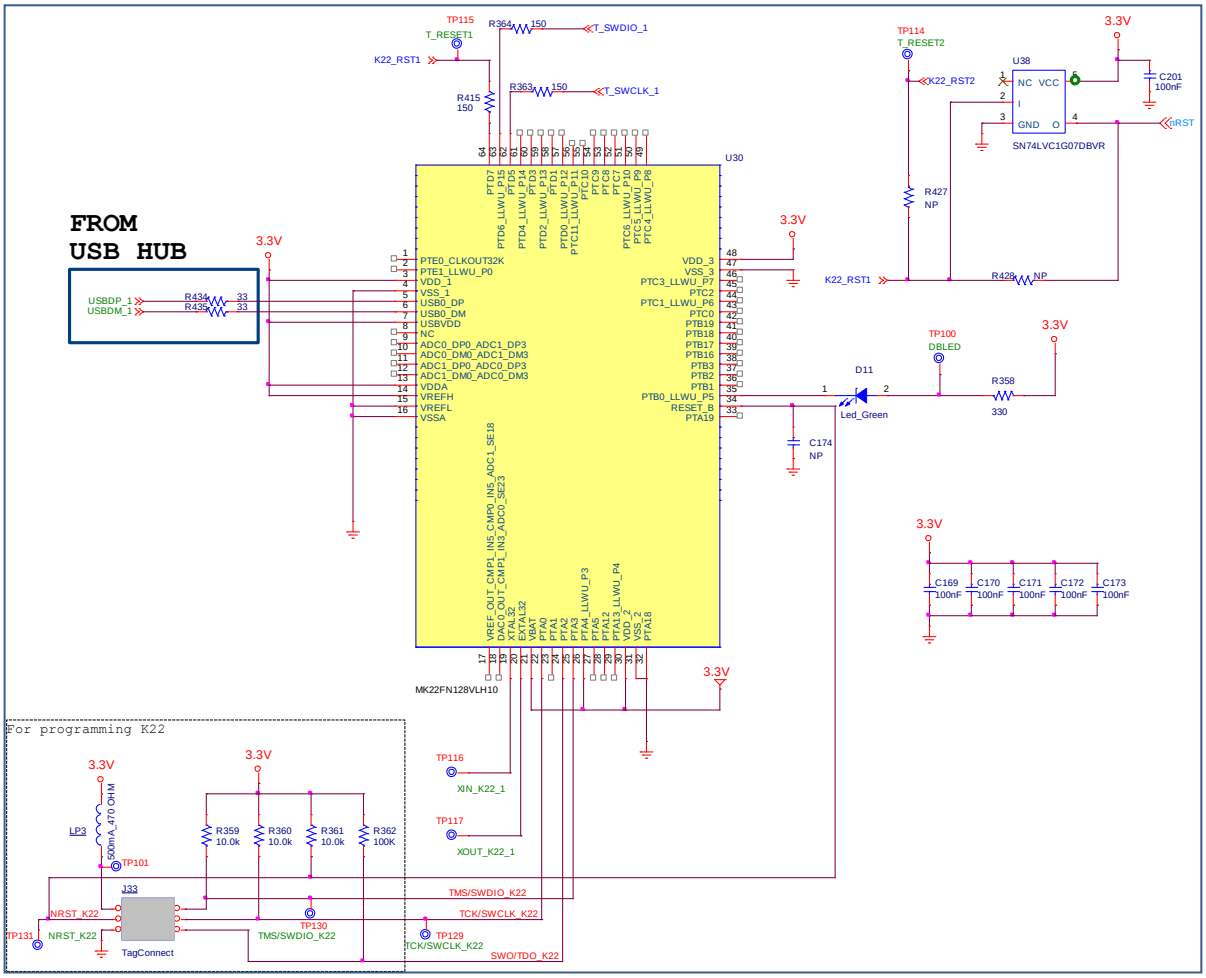


Figure 11: MK22 Debugger Schematic (for M33)

The USB to SWD function is implemented by U30 and U31, MK22FN128VMP10. U30/31 are flashed with the J-Link OB firmware. Their operation is indicated via the green LEDs D11/D12. The chips are supplied with 3.3 V from U13.

Functions served by U30 and U31 include:

- Connecting a PC to the SWD port of DA1470x SoC
- Reset capability of the DA1470x SoC through the nRST signal
- U30 is used for M33
- U31 is used for the SNC

For the M33 processor only, the connector J31 is available to access the Embedded Trace Macrocell (ETM) module via a standard 20-pin high density connector. A J-Link Trace debug probe can be connected to J31 for this purpose.

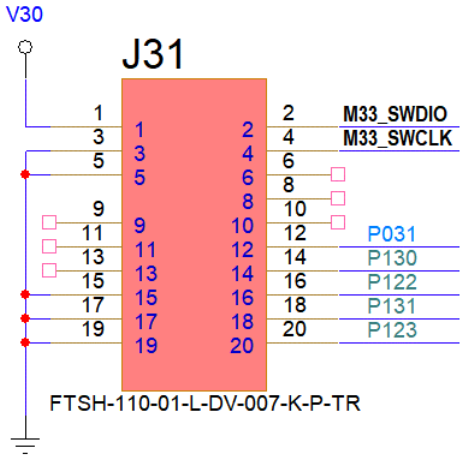


Figure 12: J-Trace Connector for M33

Note that TRACE_DATA_1 and TRACE_DATA_3 are used for buttons K1 and K2.

4.4 Audio Codec

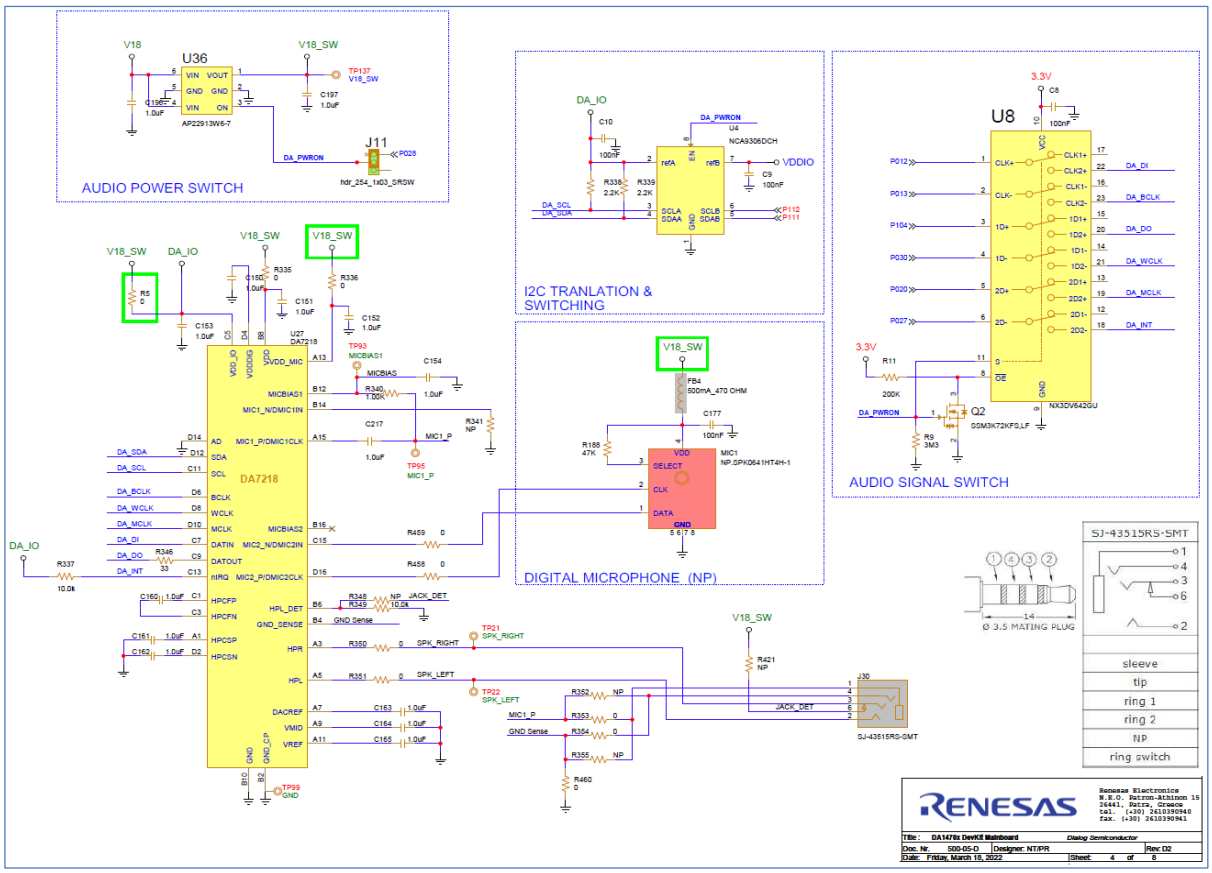


Figure 13: Audio Section Schematic

DA1470x is equipped with the DA7218, a powerful audio codec with a stereo DAC to headphone output and it contains two analog MIC input paths and two PDM channels.

In this development kit there a placeholder for a digital MIC1 that is **not populated** by default as shown in Figure 13. The power domain of the DA7218 is GPIO controlled via two power switches for optimum power consumption.

All digital signals between DA1470x and Audio Codec are controlled and can be disabled by an analog switch (U8), this switch is controlled by DA170x's GPIO P028 connected to DA_PWRON signal alias as shown in Figure 14.

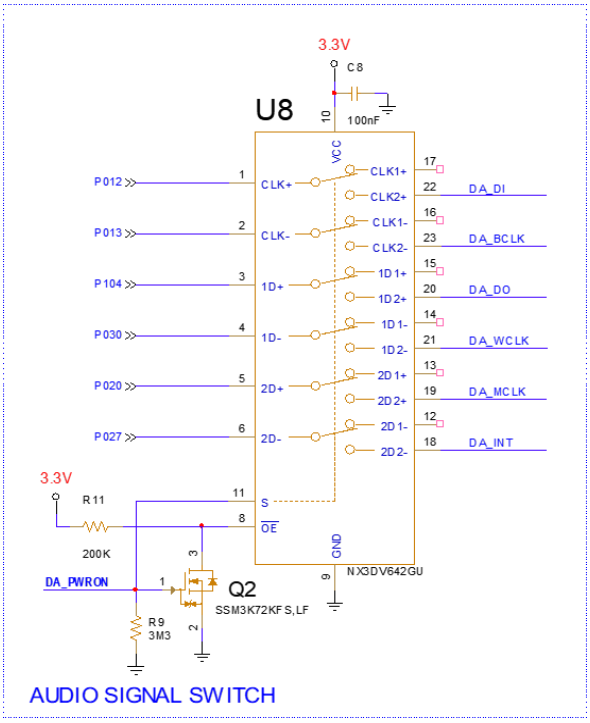


Figure 14: Analog Switch (U8) Used to Isolate the Digital Audio Onterface

NOTE
On DA14706 PRO-Development kit, there is no capability to connect a PDM microphone directly to DA1470x. However, this can be realized by plugging an external PDM microphone break out on break out headers.

4.5 Expansion SPI Connector

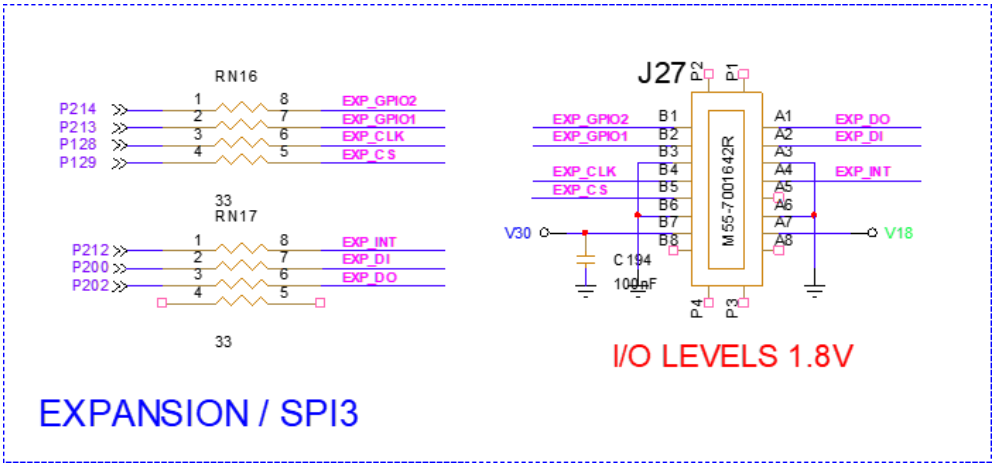


Figure 15: Expansion SPI Connector (J27)

The SPI signals that can be utilized by the J27 connector are either SPI1/SPI2 (up to 24 MHz, Master/Slave) or SPI3 controller (up to 48 MHz, Master only).

4.6 Voltage Level Translation (Debugging)

Voltage translation is required because the DA1470x I/O voltage will vary depending on the battery level and setting for the I/O LDO. So, if the other side (on board interfaces, SWD/UART) is fixed at 3.3 V, there will be leakage through the pins, for example if the DA1470x voltage I/Os are for example at 3.0 V or less.

Table 1: Signals with Level Translation

Pin Name	Signal Name
P00	SWDIO1 (M33)
P01	SWCLK1 (M33)
P02	SWDIO2 (SNC)
P03	SWCLK2 (SNC)
P08	UTX
P201	URX
P011	URTS
P029	UCTS

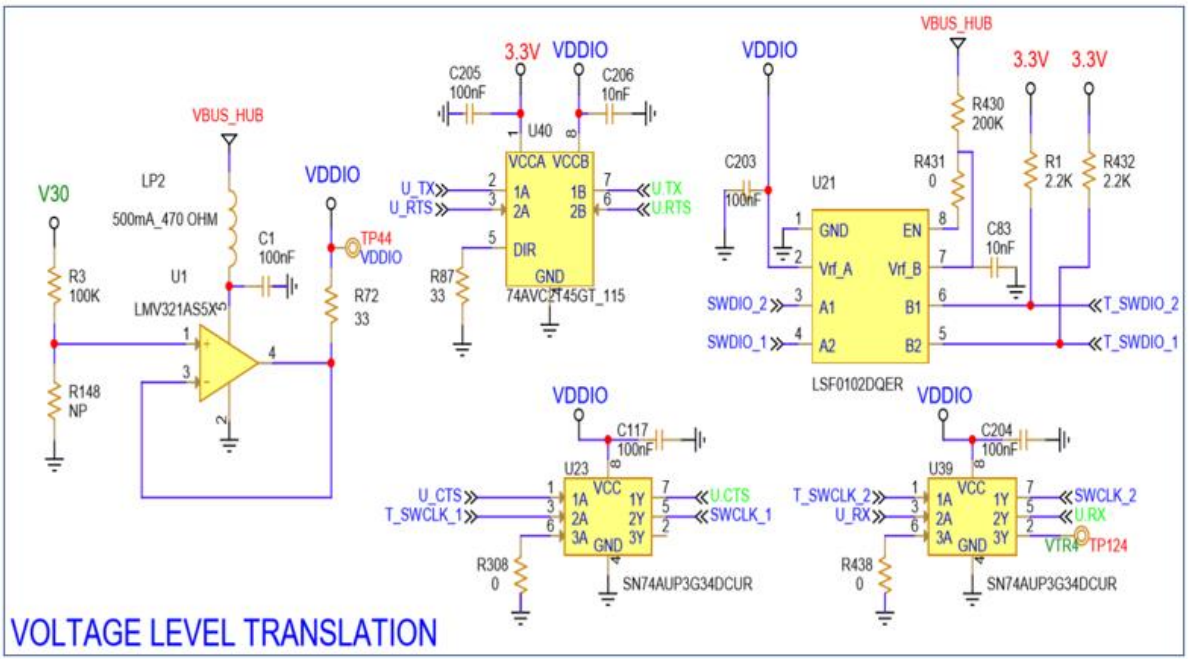


Figure 16: Voltage Level Translation Circuit

- Voltage translation is applied to the UART and SWD signals. The voltage translation is from 3.3 V to VDDIO and vice versa
- In the SWDIO signals the voltage conversion is made from 3.3 V to VDDIO (=V30 by default) VDDIO can be trimmed to lower voltage by populating R148
- VDDIO is generated from U1, where V30 from PRO-daughterboard is used as a reference. Consequently, there is no additional power consumption on the power circuitry of DA14706 PRO-Motherboard due to voltage translation

4.7 Push Buttons

- There are two available push buttons, K1 and K2, on DA14706 PRO-Motherboard
- Push buttons are connected to the DA1470x PRO daughterboard for getting user actions by the Application Software K1 button that is connected to GPIO signal P122 which is shared with J-trace connector signal TRACE_DATA_1
- K2 button is connected to GPIO signal P123 which is shared with J-trace connector signal TRACE_DATA_3
- Jumpers at connector J35 should be mounted

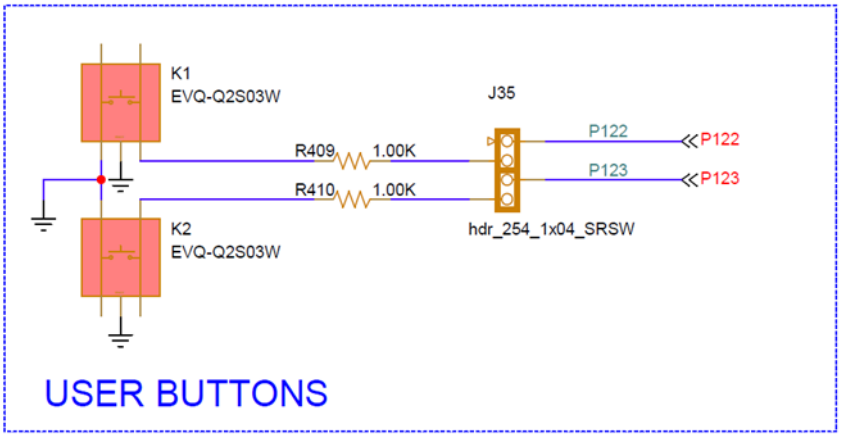


Figure 17: Push Buttons Used in the DA1470x PRO-Motherboard

4.8 GPIO Assignment

Table 2: DA14706 PRO-Development Kit GPIO Pin Assignment

DA1470x GPIO Pin Name	GPIO Assignment	Comments
P0_00	M33_SWDIO	Available on J4 of PRO-Daughterboard
P0_01	M33_SWDCLK	Available on J4 of PRO-Daughterboard
P0_02	SNC_SWDIO	
P0_03	SNC_SWDCLK	
P0_04	MikroBUS-BRSTn(1)	Multiplexed with CMAC_SWDIO, QSPIC_ON
P0_05	MikroBUS-(1)	
P0_06	MikroBUS-A(2)/TRIG_0	Multiplexed with TRIG_0
P0_07	MikroBUS-BRSTn(2)	CMAC_SWDCLK
P0_08	UART Tx (Output)	Available on J4 of PRO-Daughterboard
P0_09	SPI MISO	MikroBUS SPI MISO
P0_10	LCD_TE	LCD_TE signal
P0_11	UART CTSn (input) /NTC supply	Multiplexed GPIO
P0_12	DA_DI	DA7218 data
P0_13	DA_BCLK	DA7218 BCLK

DA1470x GPIO Pin Name	GPIO Assignment	Comments
P0_14	SPI SCK	MikroBUS SPI SCK
P0_15	SPI MOSI	MikroBUS SPI MOSI
P0_16	MikroBUS-RX(2) / LCD_SPI_SD1	Multiplexed GPIO
P0_17	MikroBUS-TX(2) /LCD_SPI_SD3/TRIG_1	Multiplexed GPIO
P0_18	MikroBUS-CS(2) / LCD_CS / TRIG_2	Multiplexed GPIO
P0_19	MikroBUS CS(1) / EXTCOMIN	Multiplexed GPIO
P0_20	DA_MCLK	MCLK of DA7218 codec
P0_21	MIC_PWR1 / TRIG_3	TRIG_3/ Analog MIC supply
P0_22	MikroBUS-RX(1) / LCD_SPI_SD2	Multiplexed GPIO
P0_23	MikroBUS-INT(1) / LCD_RED1	Multiplexed GPIO
P0_24	MikroBUS-INT(2) / LCD_GREEN0	Multiplexed GPIO
P0_25	eMMC_CLK / P025x	eMMC daughterboard, dual usage GPIO described in Section 4.11
P0_26	eMMC_CMD / P026x	eMMC daughterboard, dual usage GPIO described in Section 4.11
P0_27	DA_INT	DA7218 interrupt signal
P0_28	DA_PWRON	Controls the power switches of the DA7218 voltage domains
P0_29	RTSn (output) / NTC_Sence	
P0_30	DA_WCLK/TRIG_4	DA7218 WCLK signal
P0_31	TRACE_CLK / TRIG_5	Multiplexed GPIO
P1_00	MikroBUS-PWM(1) / LCD_GREEN1/ QSPIC2_ON	Multiplexed GPIO
P1_01	MikroBUS-PWM(2) / LCD_BLUE0	Multiplexed GPIO
P1_02	eMMC_D0 / P102x	eMMC module, dual usage GPIO described in Section 4.11
P1_03	TP_INT	Interrupt pin of the LCDs touch controller
P1_04	DA_DO	DA7218 data out
P1_05	PGAp	MIC+
P1_06	PGAm	MIC-
P1_07	MikroBUS-TX(1) / LCD_FRP / LCD_PWR_EN	Multiplexed GPIO
P1_08	eMMC_D3 / P108x	eMMC module, dual usage GPIO described in Section 4.11
P1_09	FL_D0 / eMMC_D2	SPI_FLASH multiplexed with eMMC module, dual usage GPIO described in Section 4.11
P1_10	eMMC_D1	eMMC module, dual usage GPIO described in Section 4.11
P1_11	I3C SDA	I3C data signal
P1_12	I3C SCL	I3C clock signal
P1_13	QSPIC2_D2/P113x	QSPI RAM, dual usage GPIO described in Section 4.9

DA1470x GPIO Pin Name	GPIO Assignment	Comments
P1_14	QSPIC2_D1/P114x	QSPI RAM, dual usage GPIO described in Section 4.9
P1_15	QSPIC2_D0, P115x	QSPI RAM, dual usage GPIO described in Section 4.9
P1_16	eMMC_D6/P116x	eMMC module, dual usage GPIO described in Section 4.11
P1_17	FL_D3/eMMC_D5/P117x	SPI FLASH/eMMC, multi-use GPIO described in Section 4.11
P1_18	FL_D2/eMMC_D4,P118x	SPI FLASH/eMMC, multi-use GPIO described in Section 4.11
P1_19	QSPIC2_CLK,P119x	QSPI RAM, dual usage GPIO described in Section 4.9
P1_20	QSPIC2_D3, P120x	QSPI RAM, dual usage GPIO described in Section 4.9
P1_21	eMMC_RST / P121x	eMMC module reset, dual usage GPIO described in Section 4.11
P1_22	TRACE_DATA[1] / Button 1	
P1_23	TRACE_DATA[3] / Button 2	
P1_24	QSPIC2_CS / P124x	QSPI RAM, dual usage GPIO described in Section 4.9
P1_25	FL_CS	SPI FLASH
P1_26	FL_CLK	SPI FLASH
P1_27	FL_D1	SPI FLASH
P1_28	EXP_CLK	CLK signal on the expansion connector J27
P1_29	EXP_CS	CS signal on the expansion connector J27
P1_30	TRACE_DATA[0] /TRIG_6	Multiplexed GPIO
P1_31	RACE_DATA[2] / TRIG_7	Multiplexed GPIO
P2_00	EXP_DI	DI signal on the expansion connector J27
P2_01	UART RX (input)	Available on J4 of PRO-Daughterboard
P2_02	EXP_D0	D0 signal on the expansion connector J27
P2_03	eMMC_D7/P203x	eMMC module, dual usage GPIO described in Section 4.11
P2_04	OQSPIF_D4	
P2_05	OQSPIF_D5	
P2_06	OQSPIF_D6	
P2_07	OQSPIF_D7	
P2_08	XTAL 32KHZ	
P2_09	XTAL 32KHZ	
P2_10	USBp	

DA1470x GPIO Pin Name	GPIO Assignment	Comments
P2_11	USBn	
P2_12	EXP_INT	INT signal on the expansion connector J27
P2_13	EXP_GPIO1	GPIO1 on the expansion connector J27
P2_14	EXP_GPIO2	GPIO2 on the expansion connector J27

4.9 QSPI-RAM

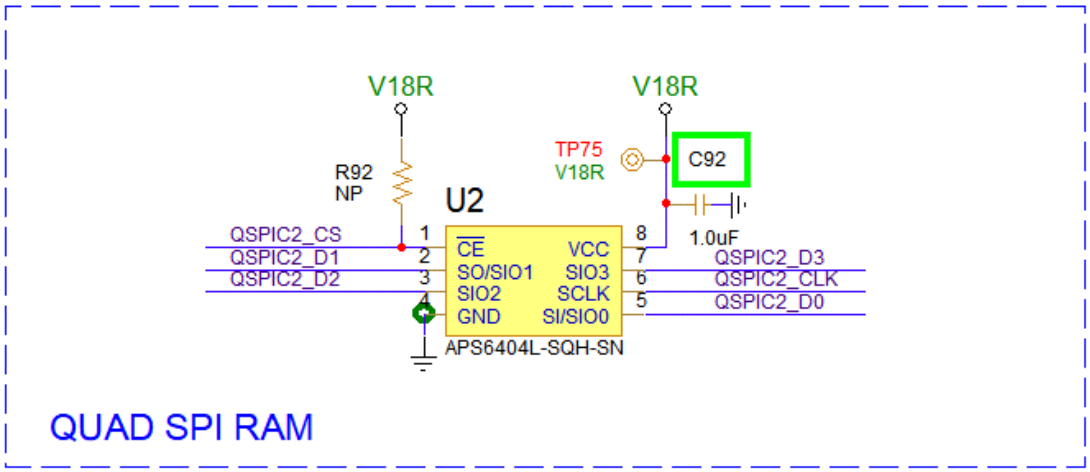


Figure 18: QSPI RAM Schematic

QSPI-RAM may be used in applications where we need bulk data transfers with DMA. The most common case is as LCD frame buffer. On DA14706 PRO-Motherboard, the APS6404L-SQH-SN from APMEMORY is mounted. The memory characteristics are shown below:

- 64 Mbit QSPI RAM memory
- Half Sleep mode with data retention for 30 µA (max) Stand By current
- Operating voltage: 1.65 V to 3.6 V for read, erase and program operations
- SOP-8L (150 mils), package

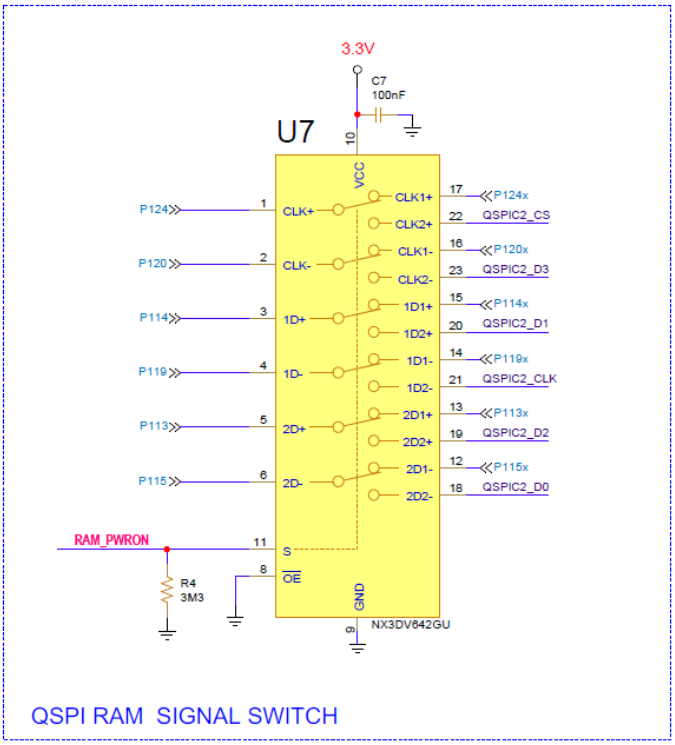


Figure 19: QSPI RAM Analog Switch

The QSPI RAM signals are controlled by an analog switch (see Figure 19), they either connected: to the main SoC DA1470x (when RAM_PWRON is high) or to the monitoring headers (when RAM_PWRON is low).

Default state of RAM_PWRON signal is HIGH.

P113x, P114x, P115x, P119x, P120x, P124x are connected to the monitoring header J4 and they are enabled when signal RAM_PWRON is LOW.

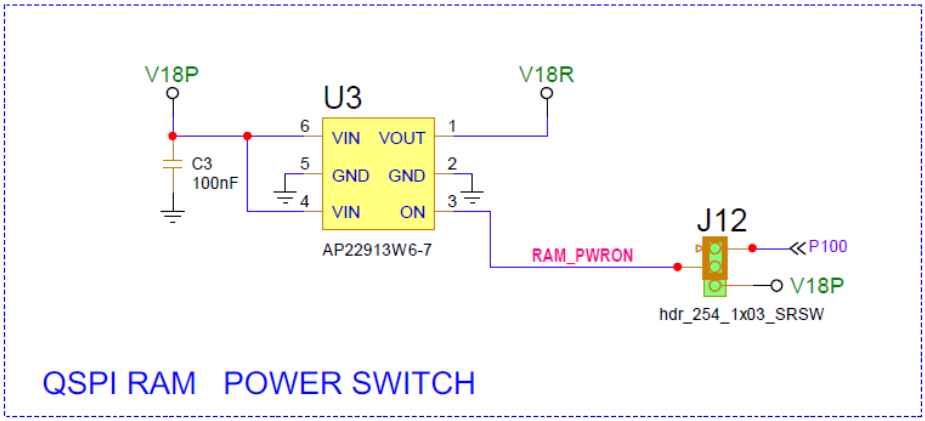


Figure 20: QSPI RAM Power Switch

In the QSPI-RAM both the power (via power switch U3) and the connectivity of the signals are controlled by jumper block J12 and signal RAM_PWRON. This control signal can be driven by GPIO P1_00 (jumper 1-2, default option), set permanently enabled (jumper 2-3).

4.10 QSPI Flash

In this DA14706 PRO-Motherboard, three different footprints are available for the storage flash memory (WSON8, SOIC16 and UDFN8), to support a large selection of memories. The default option is the AT25SL128A-MHE-T at a UDFN8 package.

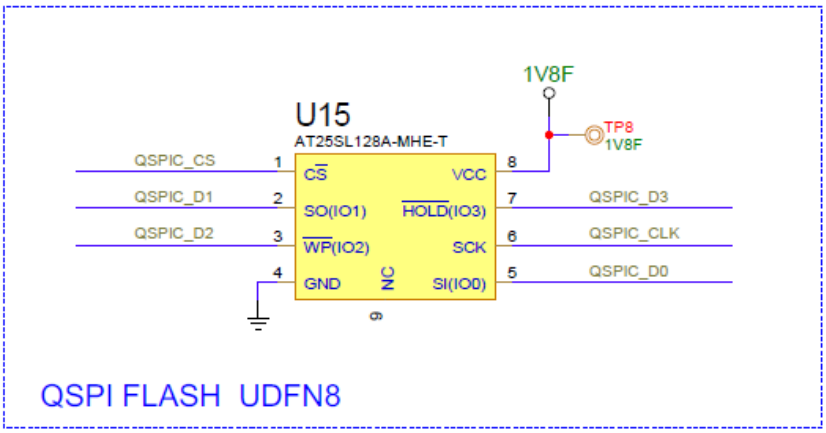


Figure 21: Default QSPI Flash AT25SL128A-MHE-T

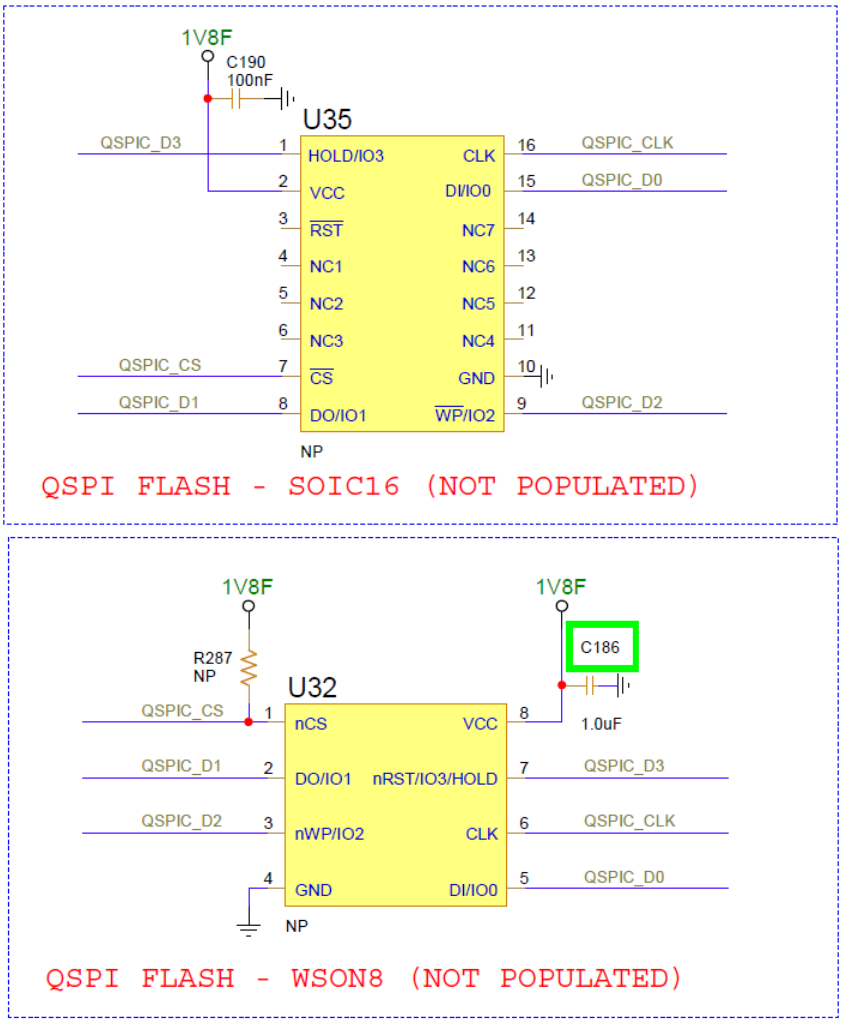


Figure 22: Two QSPI Flash PCB Footprint Options (Not Populated)

The QSPI flash signals are connected to the DA1470x using an analog switch, as shown in Figure 23. The switch serves two purposes:

1. It selects which group of pins (default or marked as “for future use”) will be connected to the QSPI storage flash. This function is controlled by signal BA_DBn which is hardwired on the daughterboard – default is high.
2. Secondly, U6 interrupts the signals to the QSPI memory if the eMMC daughterboard is connected, since the eMMC and QSPI memory controllers on the DA1470x share some pins. Signal eMMC_DBn is grounded on the eMMC daughterboard. When plugged in, the analog switch will disable the output to the QSPI memory via Q1 so only one of the interfaces (QSPI or eMMC) can be selected at a time.

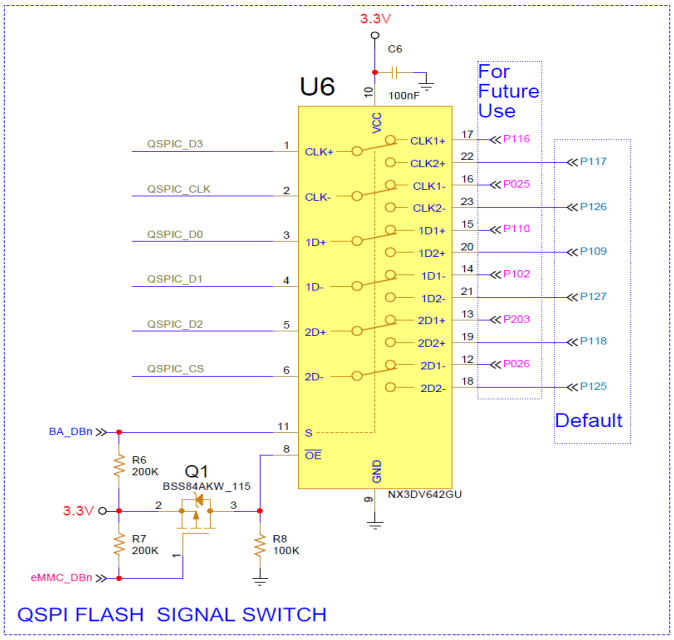


Figure 23: Analog Switch (U6) Used for the QSPI Flash Signals

Table 3: U6 Truth Table

BA_DBn	eMMC_DBn	QSPI Flash	DA1470x	Comments
x	L	switch off		Use with eMMC through connector J6
L	H	QSPIC_D0	P110	Use with QSPI Flash, (U15)
		QSPIC_D1	P102	
		QSPIC_D2	P203	
		QSPIC_D3	P116	
		QSPIC_CS	P026	
		QSPIC_CLK	P025	
H	H	QSPIC_D0	P109	Reserved for Future use
		QSPIC_D1	P127	
		QSPIC_D2	P118	
		QSPIC_D3	P117	
		QSPIC_CS	P125	
		QSPIC_CLK	P126	

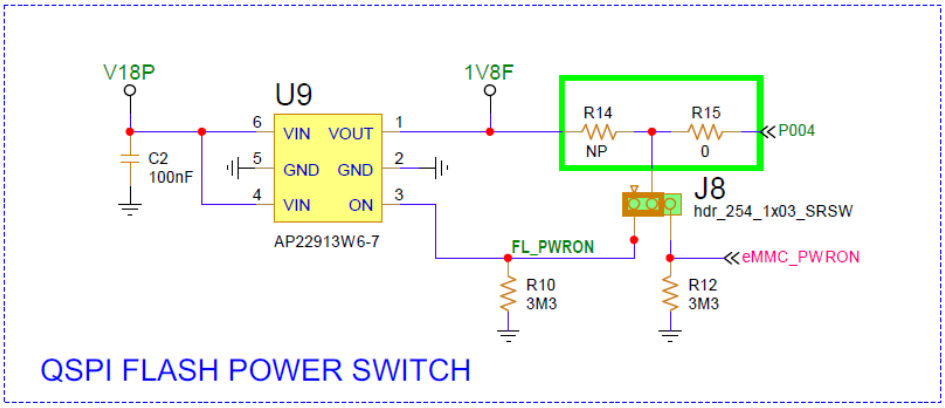


Figure 24: QSPI Flash Power Switch

The QSPI-Flash power switch U9 is controlled by jumper block J8 and signal FL_PWRON. FL_PWRON can be driven by GPIO P0_04 (jumper 1-2, Default option). When jumper is placed on positions 2-3 of J8, then eMMC_PWRON control signal is enabled (see Section 4.11) whereas U9 is disabled. If neither the QSPI flash nor the eMMC daughterboard are needed, then the jumper on J8 can be removed and both of them will not be powered.

4.11 Break-Out Connector (J6)

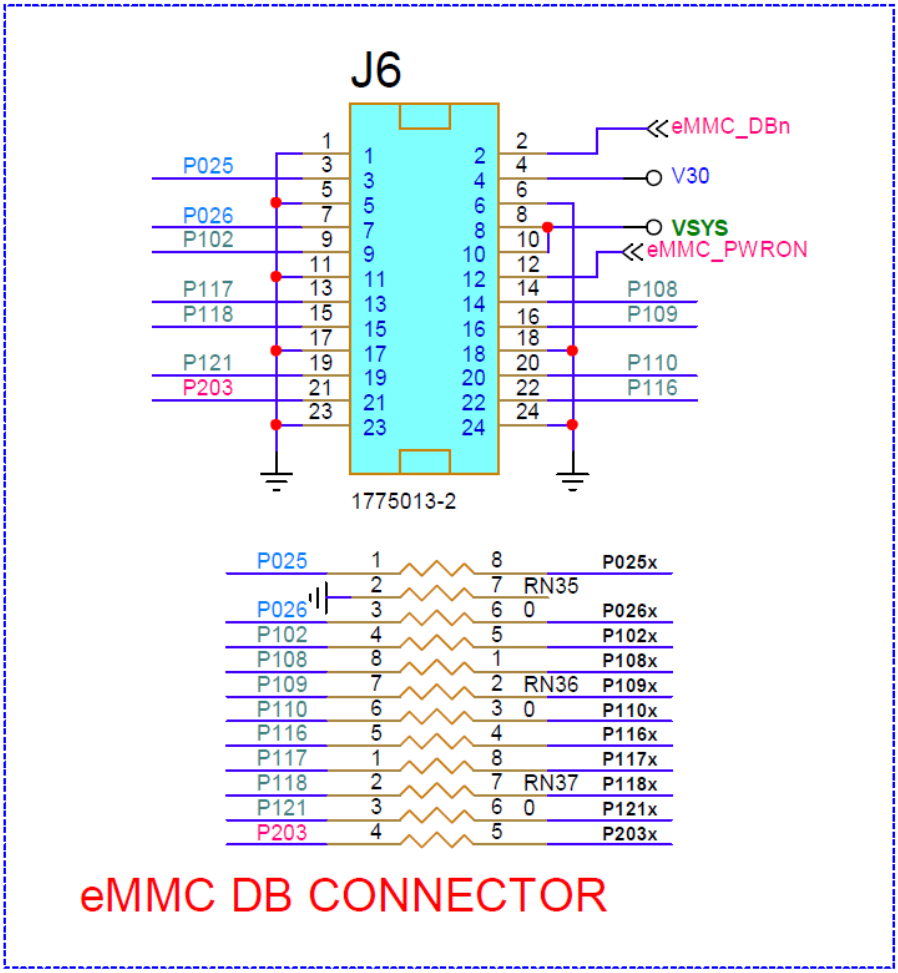


Figure 25: eMMC Connector Schematic

For better flexibility, J6 break-out connector is added on the DA14706 PRO Motherboard. The connector used is the 1775013-2, a 24 positions,0.8 mm, PCB Mount vertical receptacle. Users can design a module using the mate connector.

The GPIOs connected on J6 are multiplexed with eMMC bus, making it possible to test an eMMC memory as well other peripherals.

Also, as a number of the signals are shared with QSPI Flash memory, the analog switch U6 should be turned off using the eMMC_DBn signal as shown in Figure 23.

NOTE
In the absence of the eMMC module GPIOs: P025x, P026x, P102x, P108x, P109x, P110x, P116x, P117x P118x, P121x, P203x can be used as generic GPIOs connected to the monitoring header J4.

4.12 MikroBUS & Generic expansion slot

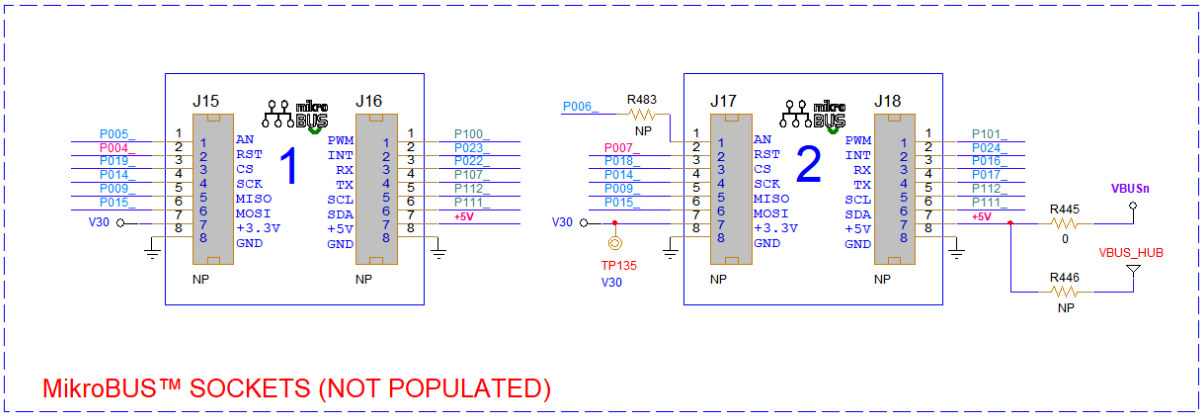


Figure 26: MikroBUS sockets (not populated)

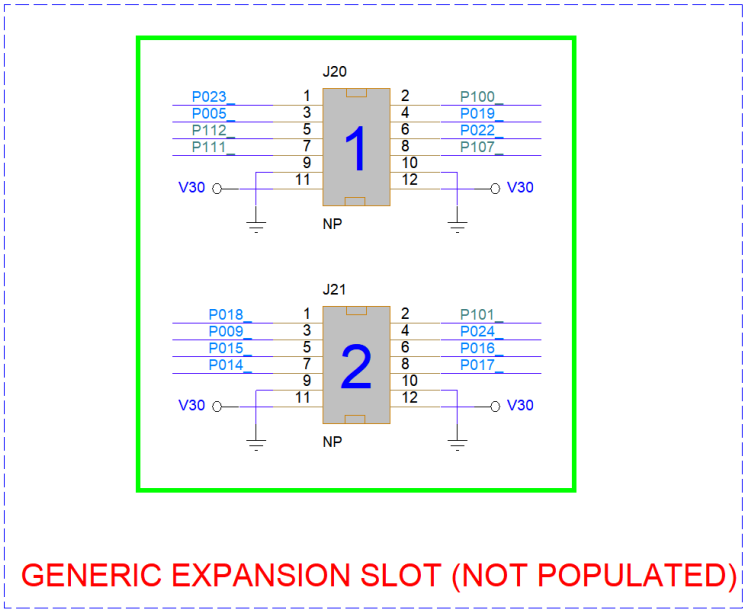


Figure 27: Generic Expansion slots

There is a MikroBUS click board expansion capability that is served via connector slots shown in Figure 26. Two generic connector slots are shown in Figure 27. These can be used as PMOD sockets, but the user should be cautious as these connector slots do not follow the same numbering convention as dictated by the PMOD interface standard.

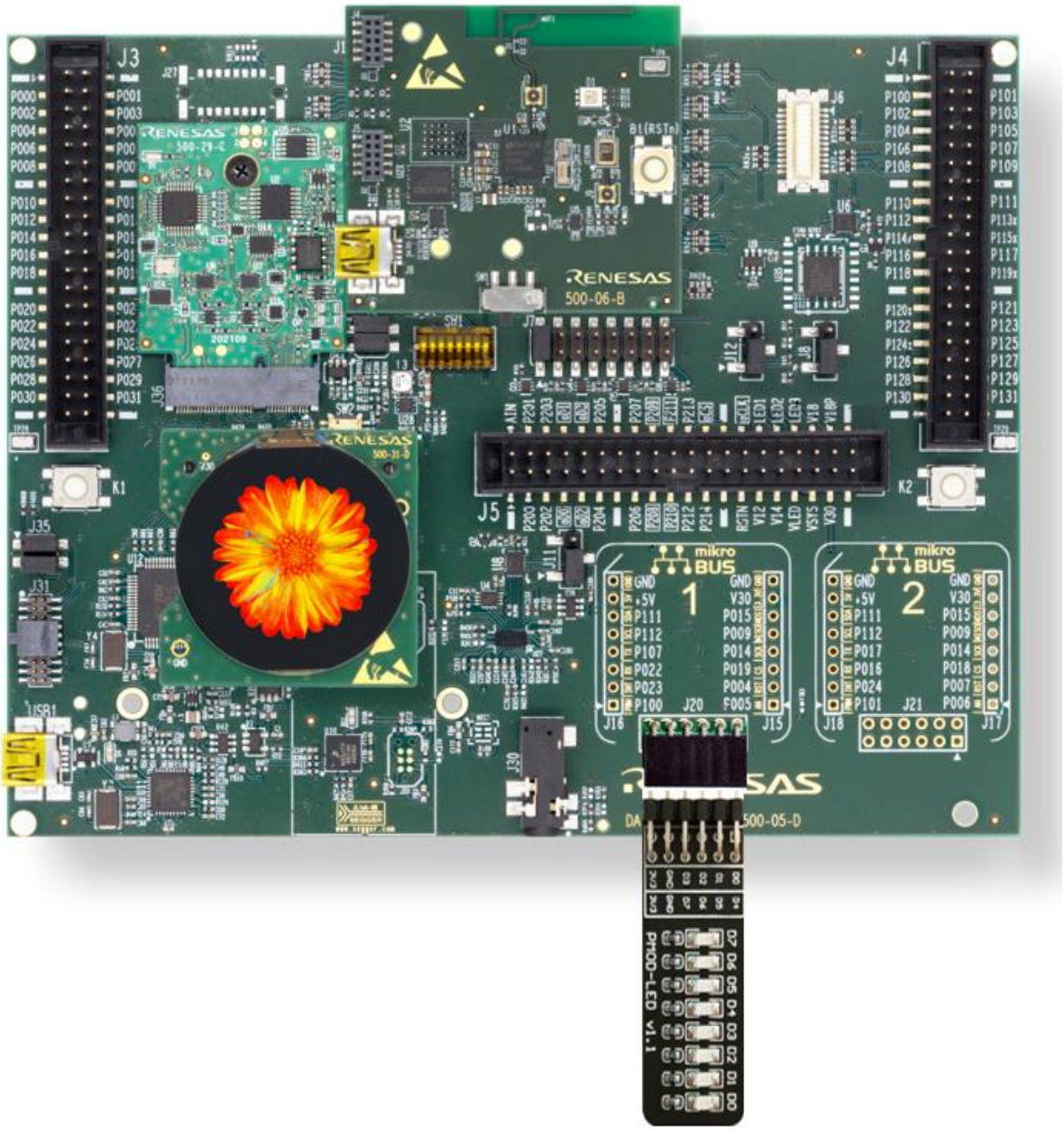


Figure 28: Example of a PMOD Interface Board Connection to DA14706 Development Kit

4.13 DA14706 PRO-Motherboard Power Configuration

The power structure of the PRO-Motherboard (shown in Figure 29) contains two high efficient adjustable 1A DCDC step down converters, the U28 (TPS62250DRVR) and the U13 (AP61100Z6-7). Both are fed from the USB connector 5 V supply (VBUS_HUB). There is one DCDC allocated per supply domain, meaning that there is a dedicated DCDC converter (U28) accompanied with a LDO (U5) for VLDOp voltage generation that passes through the current measurement circuitry and then eventually becoming the VBLDO input supply on the daughterboard section. Note that on PRO-Daughterboard, the VBLDO is connected to the VBAT through switch SW1.

LDO is acting as a backup and suppresses any undesired rippling that may appear at the output of the U28 DCDC converter. U5 not populated by default.

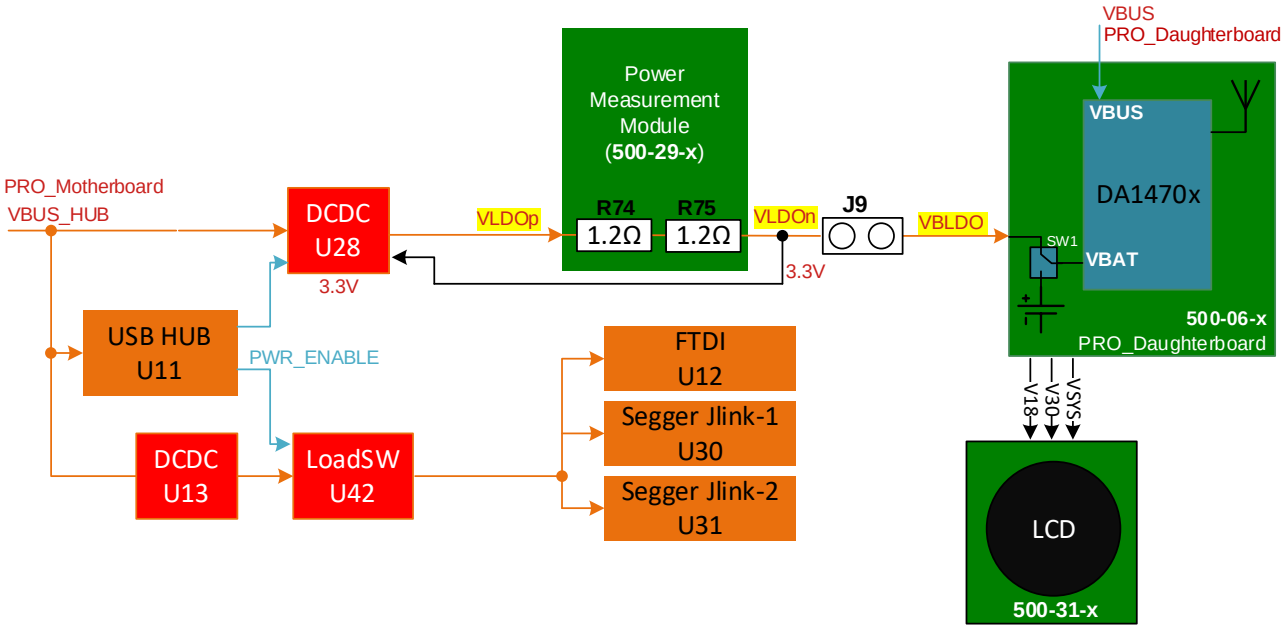


Figure 29: Power Configuration Applied on PRO-Motherboard

The actual schematic of the configuration is shown in Figure 30. The DIP switch SW2 is used to adjust the DCDC's output voltage from 3.0 V to 3.3 V and 3.6 V.

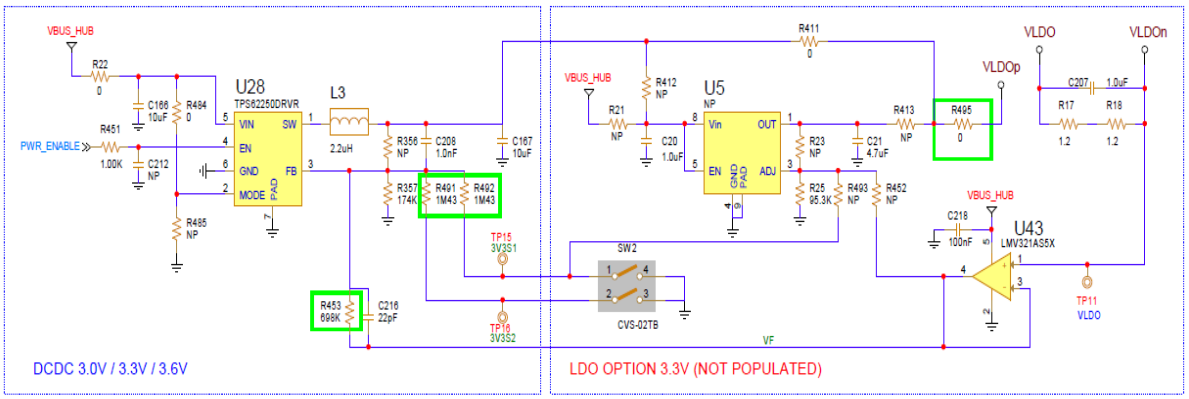


Figure 30: VLDOp Voltage Generation

SW2 switch voltage settings are shown in Figure 31, Figure 32, and Figure 33.

Figure 31: VLDO = 3.0 V

Figure 32: VLDO = 3.3 V Default

Figure 33: VLDO = 3.6 V

Header J9 is added for facilitating the current measurements. Jumper settings of header J9 are presented below in Section 5.2.2.

The remaining support circuits on the PRO-Motherboard are powered by a 2nd DCDC converter that generates the 3.3 V supply. This 3.3 V power rail is used on:

- USB to SWD (FTDI module)
- Onboard debuggers
- Voltage translation circuit
- Current measurement and LCD header

The signal (PWR_ENABLE) that triggers the power switch U42 will go HIGH after the hub has successfully enumerated with a USB host.

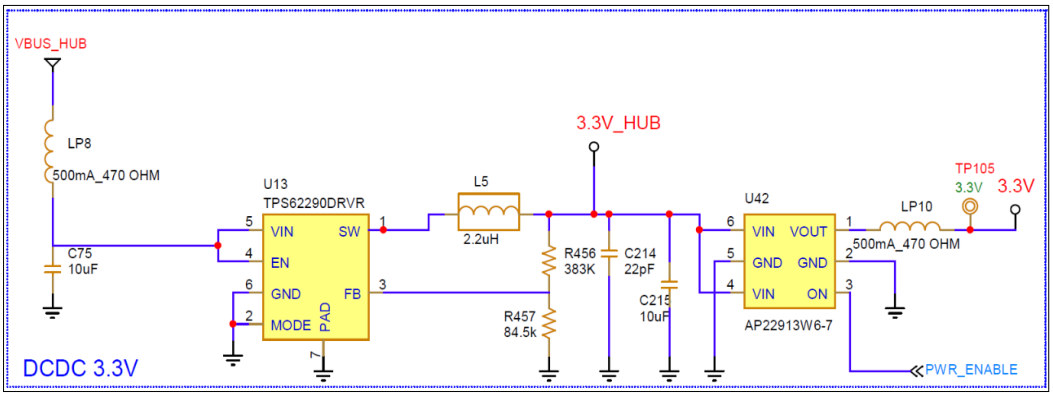


Figure 34: 3.3V LDO for PRO-Motherboard Peripherals

It is important to note on DA14706 PRO Devkit power setup there are two USB ports, one on PRO-Daughterboard and the other on the PRO-Motherboard.

As shown in Figure 29, the USB of PRO-Motherboard supplies all supporting circuits as well as the DCDC converter (U28) which in turn supplies PRO-Daughterboard.

If the USB port of PRO-Daughterboard is used, it is advised to plug the USB cable into the USB port of PRO-Motherboard as well. This will prevent any possible leakages.

5 Power Measurement Circuitry

On DA14706 Development kit has the ability to monitor critical current and voltages of the system. This is implemented with a power measurement circuitry which consists of the power measurement module (PMM2) and the monitoring circuit, which resides on the DA14706 PRO-Motherboard. This feature is intended to provide a good visualization of the system current draw and various voltages. It is relatively accurate, but note that for proper measurements, an external calibrated instrument must be used.

PMM2 features are:

- DA1470x current measurement (1 uA-500 mA at 128 kHz)
- DA1470x system voltage measurement
- USB and battery charging current measurement
- 8x Digital signals (triggers)

On the host side, PMM2 is supported by the Power Profiler tool of Smart Snippets Toolbox. At the time of writing, the software support is limited to current measurement. The more advanced features of PMM2 will be rolled out gradually in subsequent versions of Smart Snippets Toolbox.

The block diagram of PMM2 is shown in Figure 35. The analog frontend and ADC converter are implemented on the M.2 module, whereas the SPI to USB bridge and digital signals reside on the motherboard.

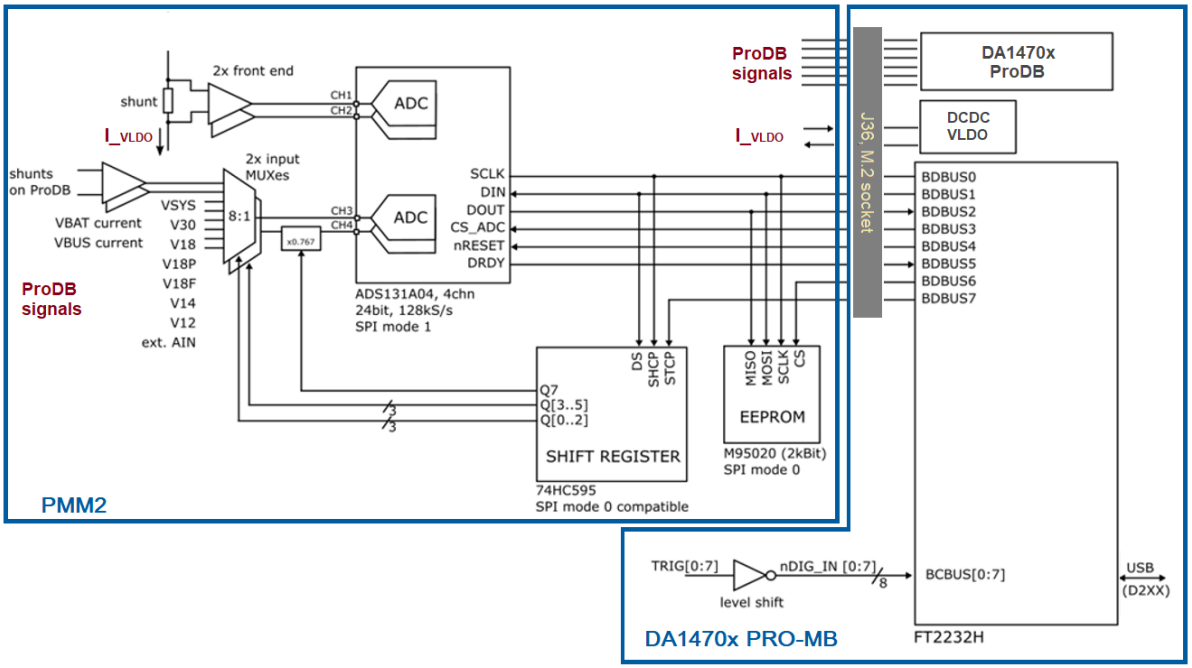


Figure 35: Power Measurement Module (PMM2) Block Diagram

An EEPROM is also provided on the module to store production data and allow autodetection from the host software.

5.1 The Power Measurement Circuitry, the Monitoring Section on PRO-Motherboard

The power measurement module (PMM2) is connected to PRO-Motherboard via J36, M.2 socket. Power to PMM2 is provided from PRO-Motherboard through power switch U34.

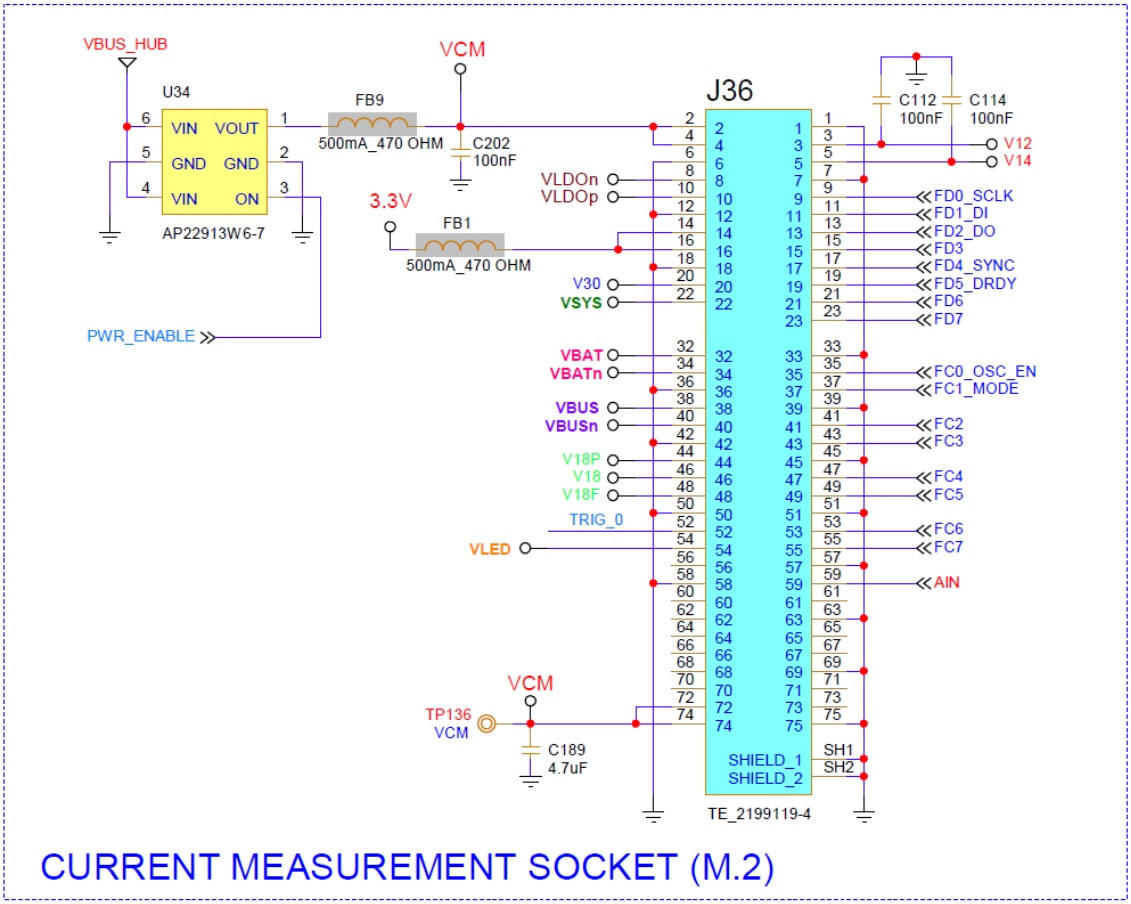


Figure 36: Current Measurement Socket (M2)

Table 4: Monitored Power Sources

Monitored Magnitude	Signal	Comments
V30	V30	Sourced from PRO-Daughterboard
VSYS	VSYS	Sourced from PRO-Daughterboard Main power rail of the Power management unit
1.8 V	V18, V18P, V18F	Sourced from PRO-Daughterboard 1.8 V rails powering peripherals (V18P), external memories (V18) and XiP flash (V18F) of the DA1470x
V14	V14	Sourced from PRO-Daughterboard 1.4 V rail powering the radio, ADC, PLL and oscillators
V12		Sourced from PRO- Daughterboard 1.2 V rail powering the digital core
VLED	VLED	Sourced from PRO- Daughterboard. Boost converter output for supplying white LEDs.
USB charging current	VBUSp, VBUSn	Sourced from PRO- Daughterboard.
VBAT charging current	VBATp, VBATn	The current drawn from battery when it is charged. Battery is connected on J6 header and SW1 must be set accordingly on of PRO- Daughterboard.
VBAT current	VLDOp, VLDOn	The current drawn from DA1470x system. Sourced from PRO-Motherboard. Current enters PMM2 from VLDOp (pin 10) and exits from VLDOn

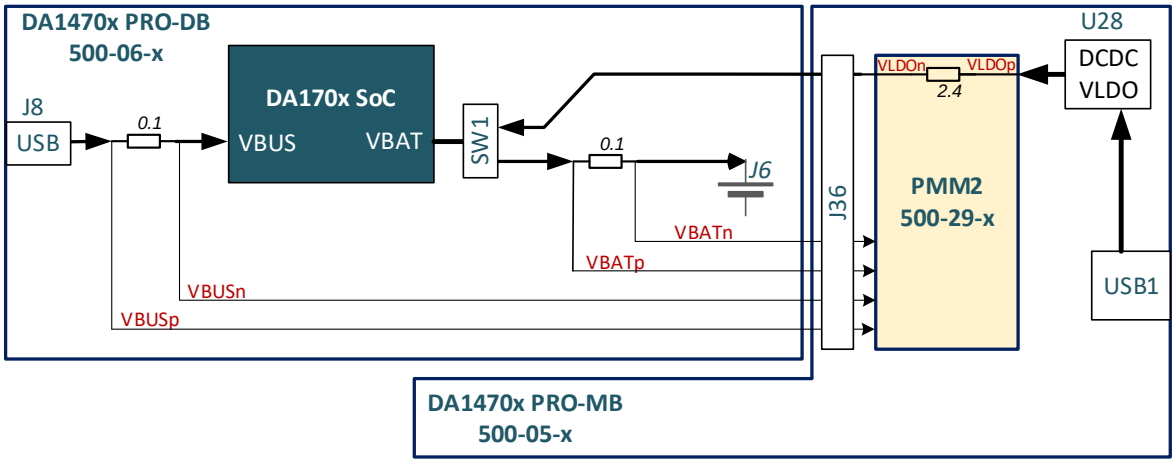


Figure 37: The Hardware Setup for Current Measurements

There are 8 TRIG options defined (TRIG_0 to TRIG_7).

As shown in Figure 38, suitable jumper block (J7) allows the user to select directly C_TRIG (P0_06) and some other preferred options. Any other GPIO can be used as a trigger source by connecting a TRIG pin on J7 with jumper wire to the desired position at breakout headers (J3..J5).

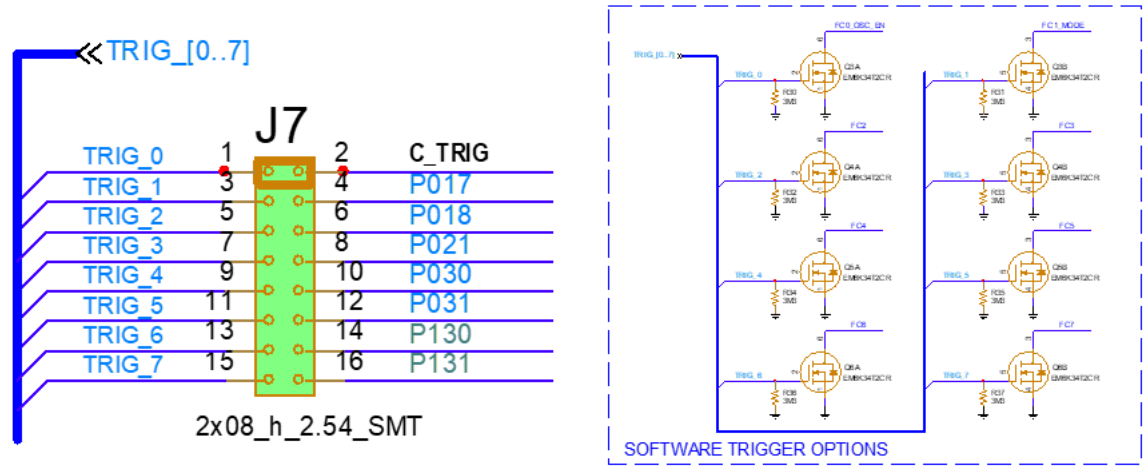


Figure 38: C_TRIG Selection Jumper Block (J7) and Buffer MOSFETS for I/O Levels Compatibility

The dual Mosfets Q3..Q6 buffer the signals to provide compatibility with 1.2 to 3.3 V I/O levels.

5.2 The Power Measurement Module 2 (PMM2), da1470x-sb-pmm2, (500-29-x)

In this DA14706 Development Kit the power measurement module (PMM2) is an external add-on board that is interfaced (connected) on the PRO-Motherboard via connector J36.

This is the da1470x-sb-pmm2, 500-29-D or later.

The current measurement unit has the following features:

- Full scale range 500 mA at 3.3 V
- Measure accurately down to 1 uA
- Dedicated hibernation mode to measure down to 100 nA
- Current sense resistors
  - 2.4 ohm in series to VLDO (located on DA1470x-sb-pmm2, see Figure 29)
  - 0.1 ohm in series with VBAT (located on PRO-Daughterboard)
  - 0.1 ohm in series with VBUS (located on PRO-Daughterboard)
- Analog processing blocks
- Fast quad channel 24-bit ADC with SPI interface
- FTDI chip for transferring data to the PC
- Software trigger circuit
- System voltage measurement
- External analog input 0-5 V

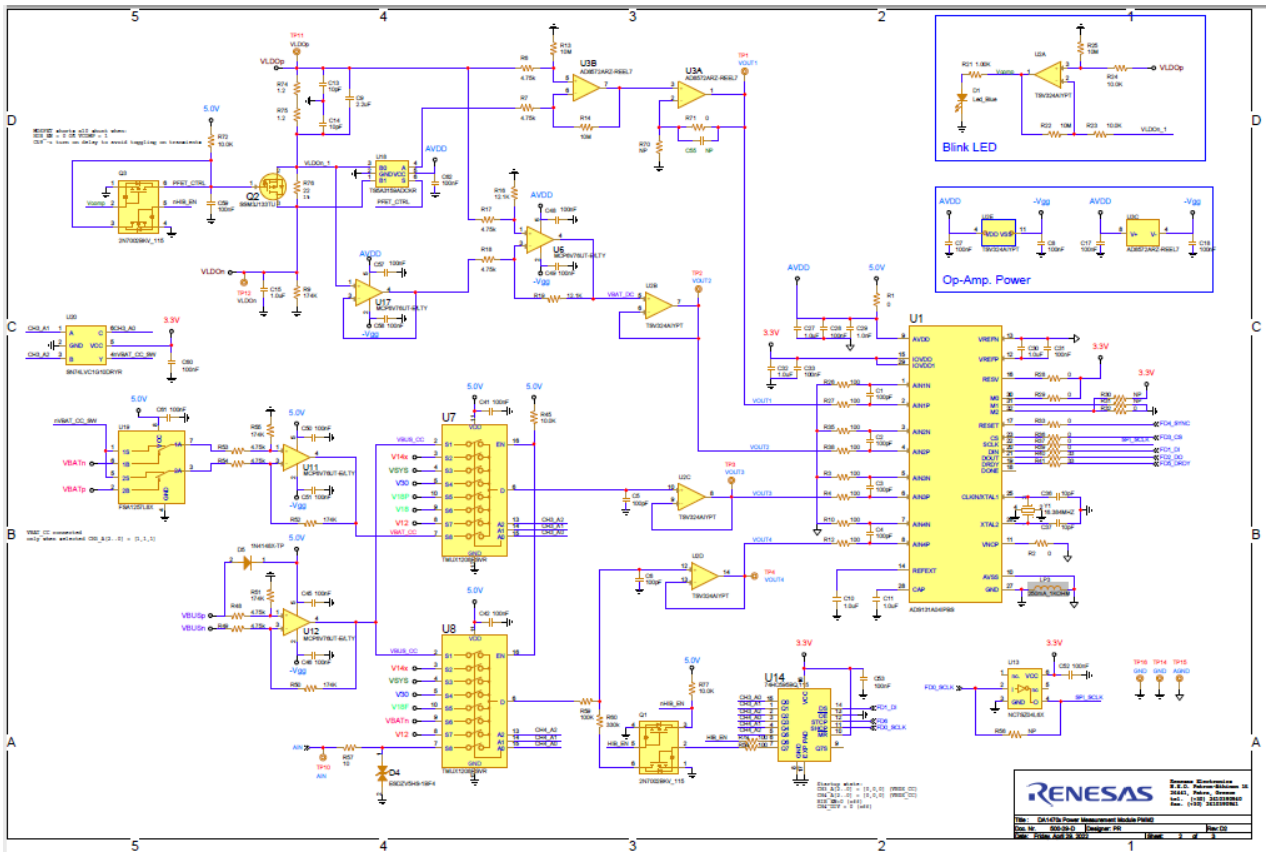


Figure 39: PMM2 Current Measurement Circuit PMM2

The input to the circuit is the voltage across the sense resistors R74 and R75. The voltage across the sense resistors is sampled simultaneously by two differential amplifier stages and is converted by the ADC to a digital value. The low range has a conversion gain of 5053 V/A and covers from 1 uA up to about 790 uA. The high scale has a conversion gain of 6.114 V/A and covers up to about 500 mA depending on the VBAT voltage. Both channels are sampled simultaneously, and the host software selects the correct channel using a threshold of 750 uA. R9 provides a constant offset which helps avoid the nonlinear region of the low scale. A blue LED serves as a visual indicator of the range. It switches on close to 750 uA and allows the user to have a quick indication of the state of the system (on when active, off when sleeping).

Multiplexers U7 and U8 select among the available system voltages and feed channels 3 and 4 of the ADC. A divider formed by R59 and R60 can be selected to allow for 5 V input signal range on VSYS and AIN (the full-scale voltage of the ADC is 4 V). Two analog front ends around U11 and U12 are provided for measuring the VBUS current and the battery charge current. The switch in front of U11 prevents the leakage current of the differential amplifier stage from VBATp/n to be measured as system current.

A shift register and associated logic control the multiplexers and the rest of the functions of the module. An EEPROM memory is used to store production data and allows the host software to autodetect the module. Charge pump U6 generates a slightly negative voltage (-230 mV) to allow the output of the frontend OPAMPs to reach true zero.

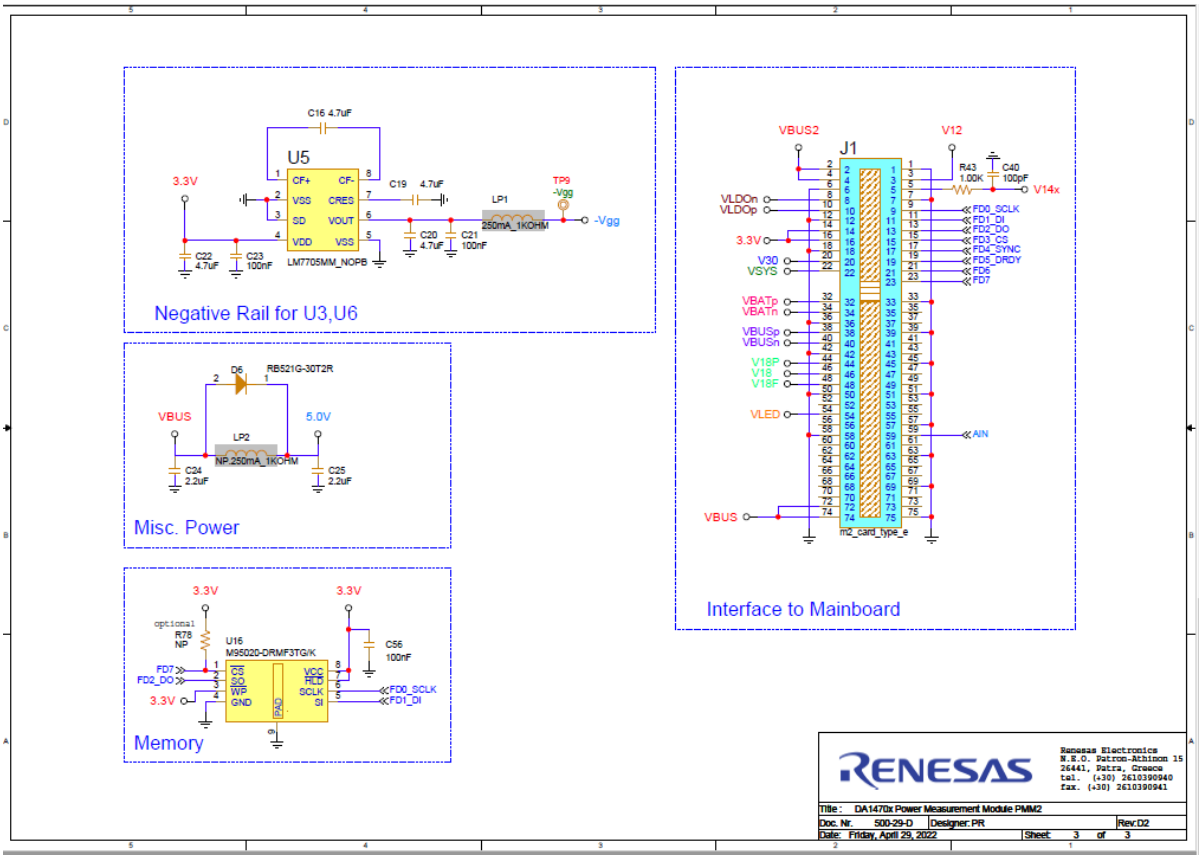


Figure 40: PMM2 on Board Peripherals (Power Supply, Memory and so on)

The circuit can be set in a low current measurement mode from the host (hibernation mode). This is useful to measure the current of the DA1470x in hibernation (shipping) mode, which is in the order of some 100 s of nA. The measurement range of the circuit in this mode is from 100 nA to 60 uA. This is achieved with a significantly larger sense resistor (R76) which is shorted by Q2 in normal operation. In hibernation mode, Q2 switches off and R76 is placed in series with R74 and R75 forming a 24.4 Ω sense resistor. The lower sampling point of the low range is moved to the terminals of this series combination with the help of analog switch U18. The high range connections remain unchanged, and it monitors the current through R74 and R75 only. To avoid excessive voltage drop due to the large sense resistor in case the system wakes up and draws large currents, the LED indicator output will also override the control of Q2 when the measured current exceeds ~600-700 uA. This ensures that the system can wake up normally and its operation is not affected by the hibernation mode.

The offset of the circuit can be calibrated in the Smart Snippets Toolbax software. The procedure necessitates disconnecting the daughterboard either physically or by sliding the daughterboard power selection switch to the right.

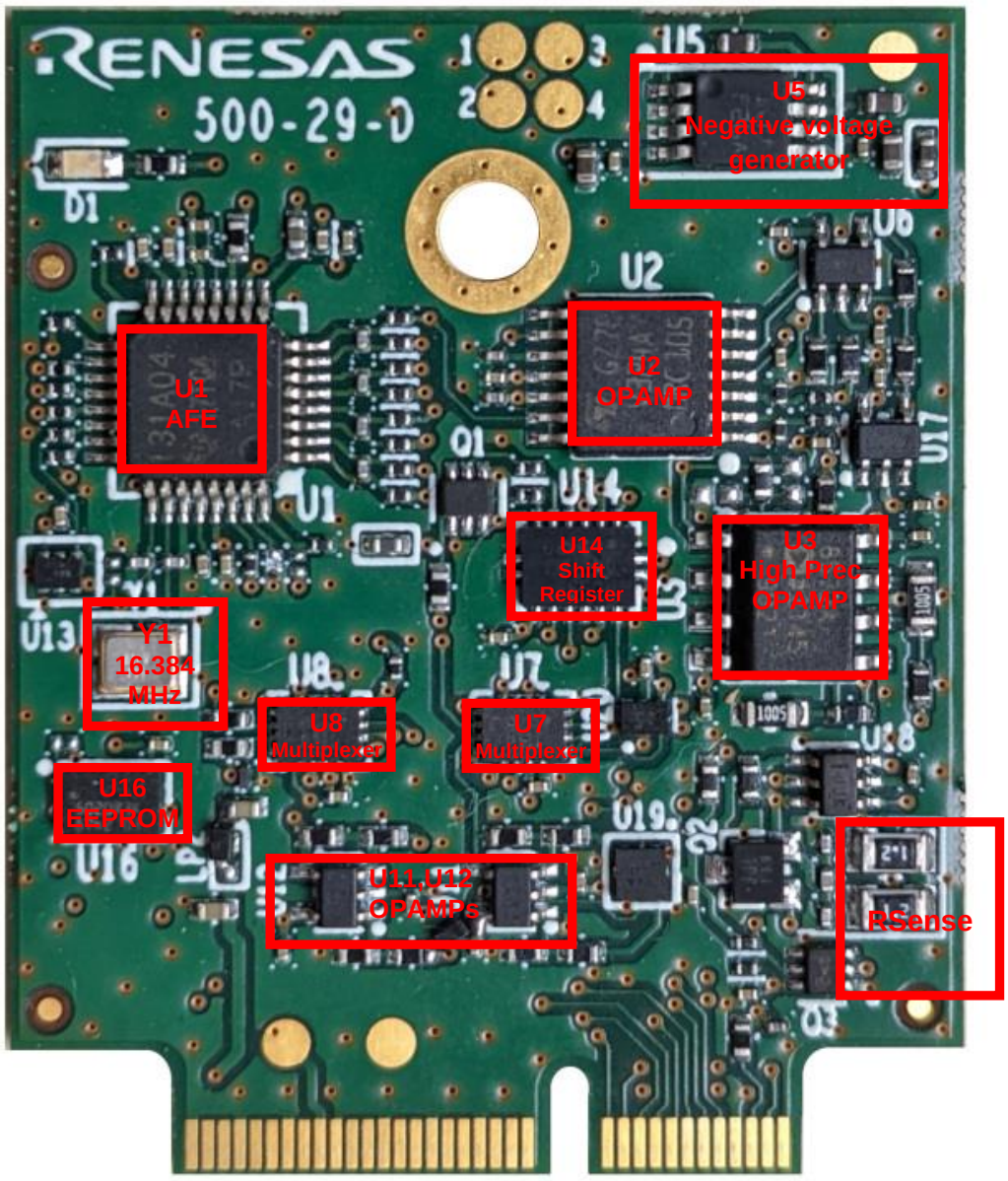


Figure 41: Current Measurement Unit PCBA (TOP)

5.2.1 Accuracy of Current Measurement for DA1470x System (VLDO)

The total measuring range of the current measurement circuit of the power measurement module two is 100 nA to 500 mA for VBLDO= 3.3 V, implemented into two scales. The current measurement range is covered by two operating modes, the default (1 µA to 500 mA) and the hibernation mode (100 nA to 60 µA). Switching from default to hibernation mode is done manually over Smart Snippets Toolbox (a version supporting this mode must be used).

The circuit accuracy is measured by applying a constant current, monitoring the same current with an external instrument and the ADC of the PMM2 module, then comparing the two. In general, the inaccuracy presented in the current measurement circuit is less than 5 % (practically less than 2 %) in most of the current range, (Table 5). Note that the values presented in the Figure 42 are averages of multiple points.

Table 5: Accuracy of the Current Measurement Circuit

Current Range	Mode	Error (%)
100 nA to 1 µA	Hibernation mode	<±10 %
1 µA το 60 uA	Hibernation mode	<±5 %
1 µA to 10 µA	Default mode	<±10 %
10 µA to 500 mA	Default mode	<±2 %

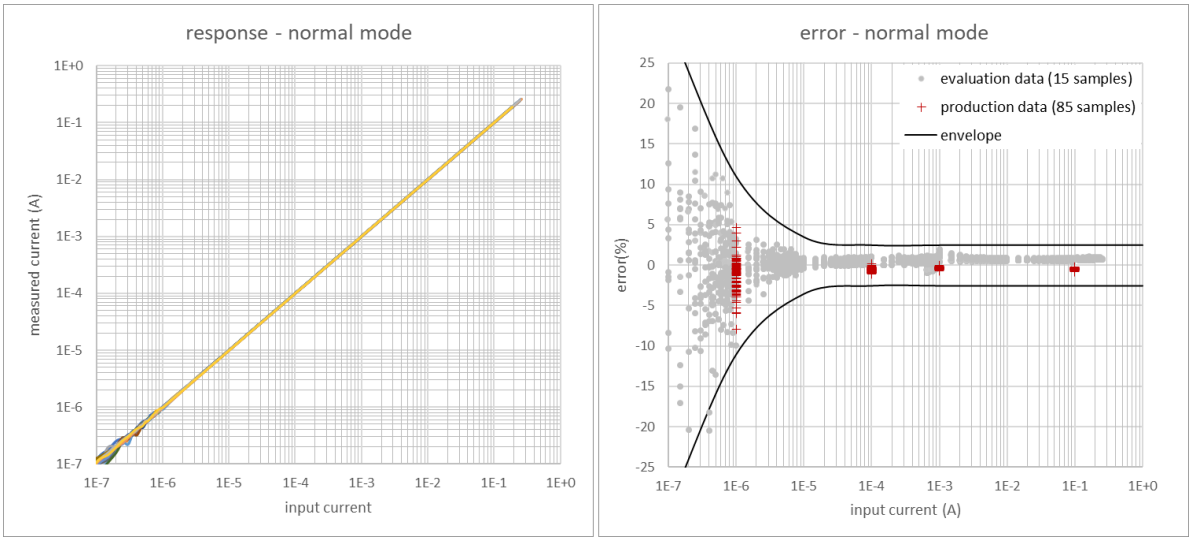


Figure 42: Normal Mode (1 µA to 500 mA at 3.3 V) Data after Offset Calibration

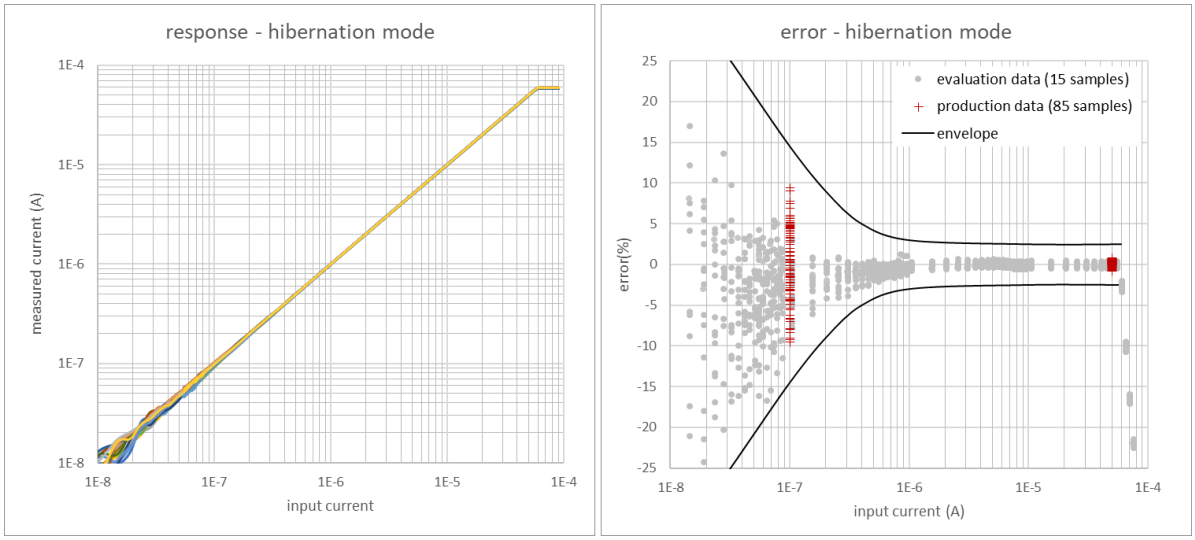


Figure 43: Hibernation Mode (100 nA to 60 uA at 3.3 V) Data after Offset Calibration

5.2.2 Settings of Power Configuration Header J9

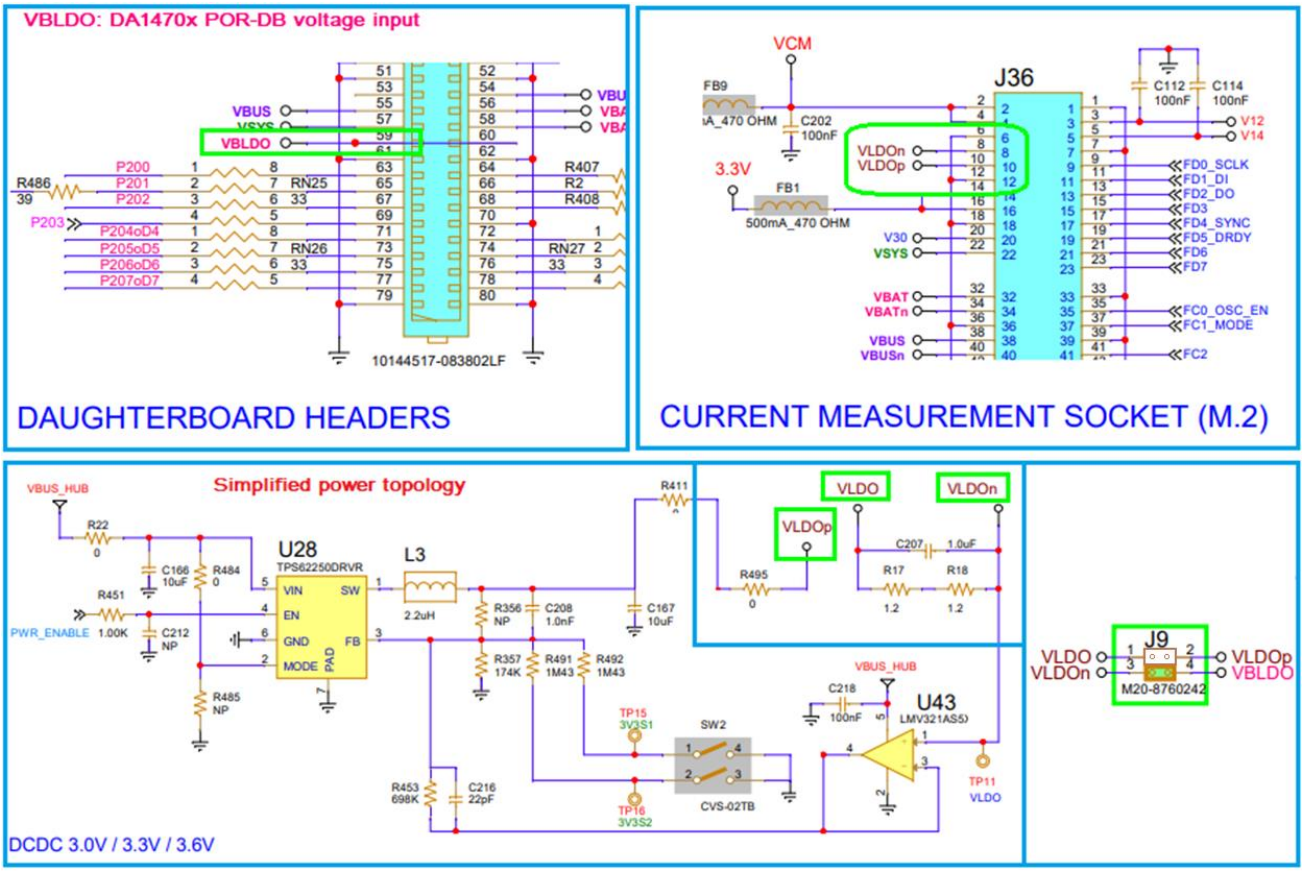
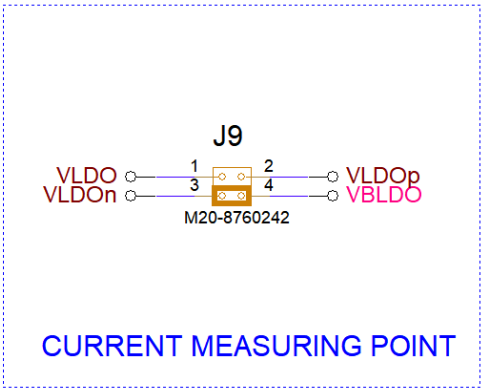


Figure 44: Power Connections

Jumper block J9 allows for different configurations as described in Table 6. Alternatively, an external current measurement instrument can be connected on these jumpers.

Table 6: Jumper Setting of Current Measurement Connector J9

	Settings	Operation
	Mount jumpers on J9:3-4	Use with Power Measurement Module 2 (PMM2,PCB Board, 500-29-D) - Default
	Mount jumpers on J9:2-4	Bypass Power Measurement Module. Use this point to connect external amperometer and measure the current without the burden of the sense resistor in pmm2
	No jumpers mount	PRO- Daughterboard. is not supplied from PRO-Motherboard
	Mount jumpers on: J9:1-2 J9:3-4	When Power Measurement Module is not present

6 LCD Interface and Add-On Board

6.1 LCD Interface on PRO-Motherboard

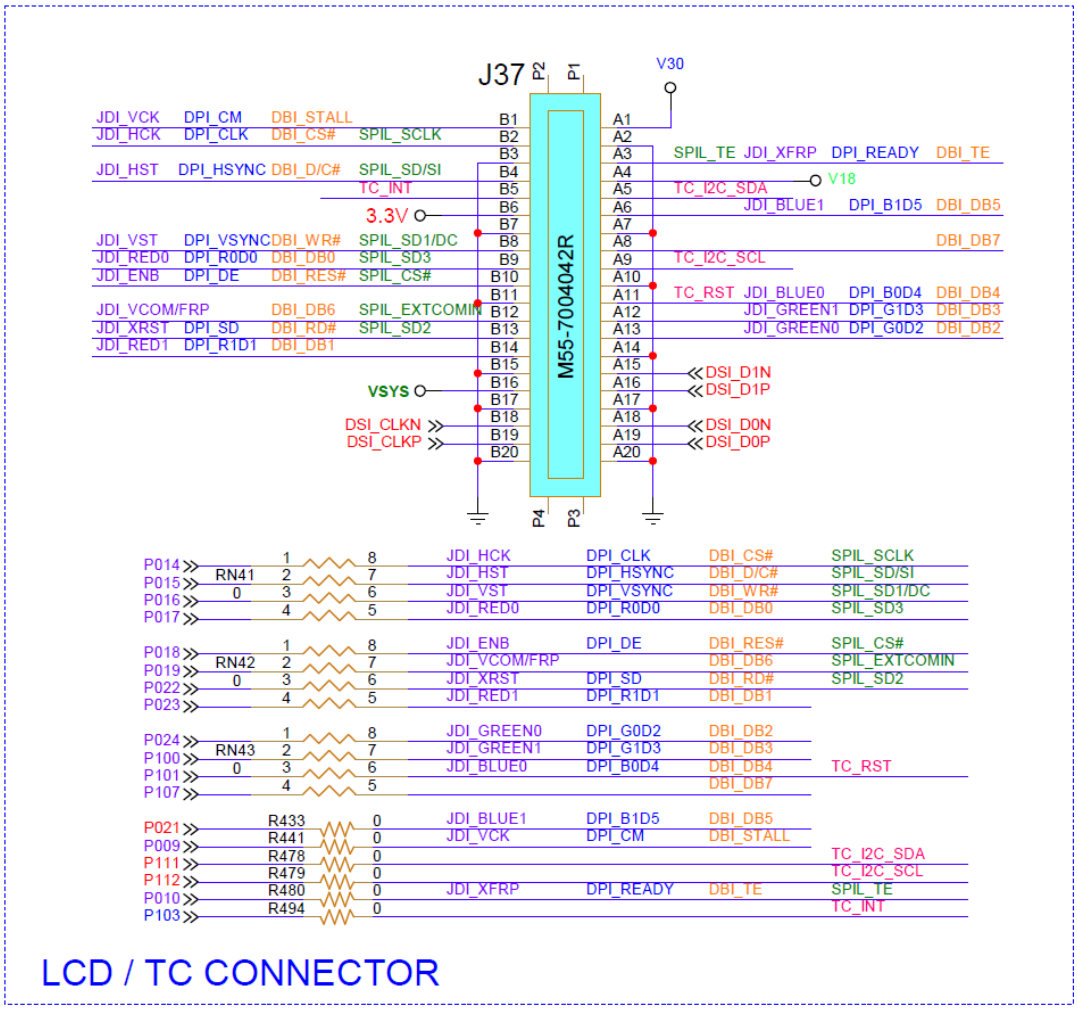


Figure 45: Header Schematic for LCD Daughterboard (Interface Board)

The DA14706 PRO Development kit provides LCD support via a dedicated daughterboard (add-on) mounted on the J37 connector on the PRO-Motherboard side. LCD type:

- AMOLED display: QSPI, High resolution 390x390 display with touch panel

6.2 LCD Amoled Board, da1470x-sb-E120A390QSR (500-31-X)

The E120A390QSR, 390x390 AMOLED with capacitive touch has been selected and applied on the LCD add-on, da1470x-sb-E120A390QSR (500-31-D).

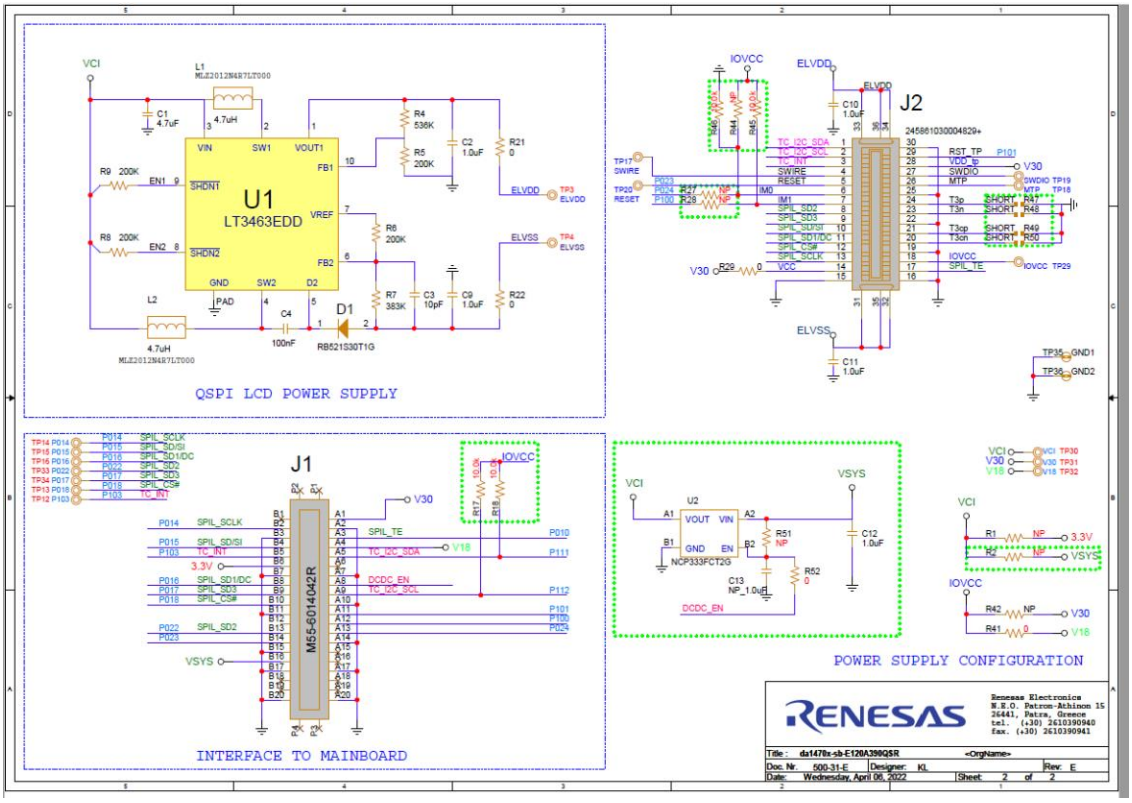


Figure 46: LCD Add-On Daughterboard

U1 is the adjustable DCDC converter LT3463EDDPBF from Analog Devices able to generate positive and negative supplies. Connector J2 provides connectivity with the TFT LCD module while J1 connects this LCD interface (add-on) board with the PRO-Motherboard.

The add-on board is configured for being supplied from VSYS.

E120A390QSR is provided from Panox Displays (https://www.panoxdisplay.com/amoled/1-2-inch-round-oled-390-spi-60hz.html).

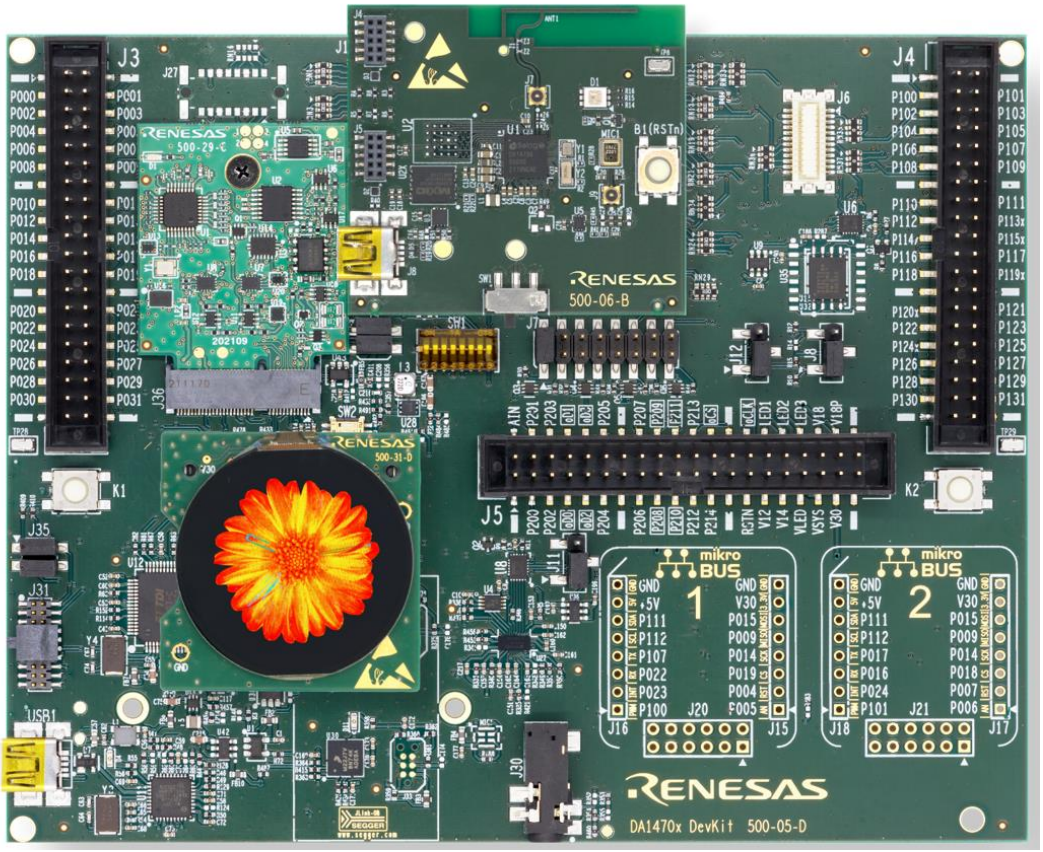


Figure 47: QSPI AMOLED LCD Daughterboard Position on PRO-Development Kit

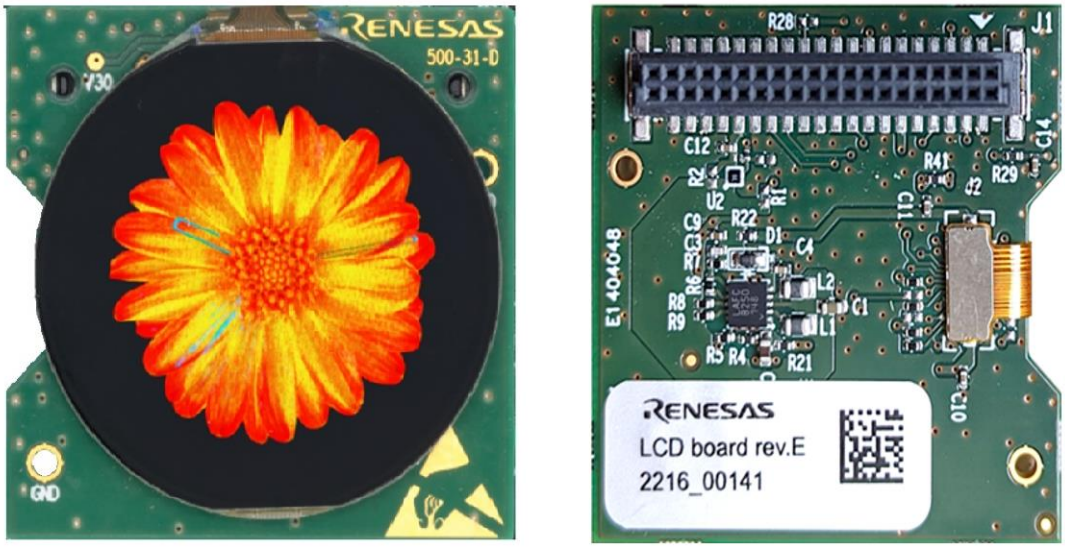


Figure 48: LCD TFT Daughterboard Top (Left) and PCBA Bottom Side (Right)

7 PRO Daughterboard

7.1 Main Features

The system on DA1470x PRO- Daughterboard. consists of the DA1470x SoC, crystals, power and radio sections. The system block diagram and the actual components location are presented in Figure 49.

The SoC variants that will be supported with the DA1470x PRO- Daughterboard are:

- DA14706 (commercial code: DA14706-00000HZ2), package VFBGA142
- DA14708 (commercial code: DA14708-00000HZ2), package VFBGA142

Block diagram blocks description is as follows:

- PRO-Motherboard interface, connectors 2x80pins (J1, J2)
- SWD connector for CMAC/SYS (J4)
- SWD connector for SNC (J5)
- USB mini-B connector
- NOR XiP Flash:
  - Quad-SPI Flash (U2X, default)
  - Octal-SPI Flash (U2, place holder – not populated)
- RGB LED (D1), part number: VLMRGB6112-00-GS08
- Reset push button (B1)
- 3-wire LiPo battery connector (J3, not mounted), part number:147323
- Coin cell holder (BT1 – not mounted)
- Power switch (SW1)
- Analog microphone (MIC1)
- RF coaxial switch (J7)
- External analog MIC coaxial switch (J9)
- Printed antenna

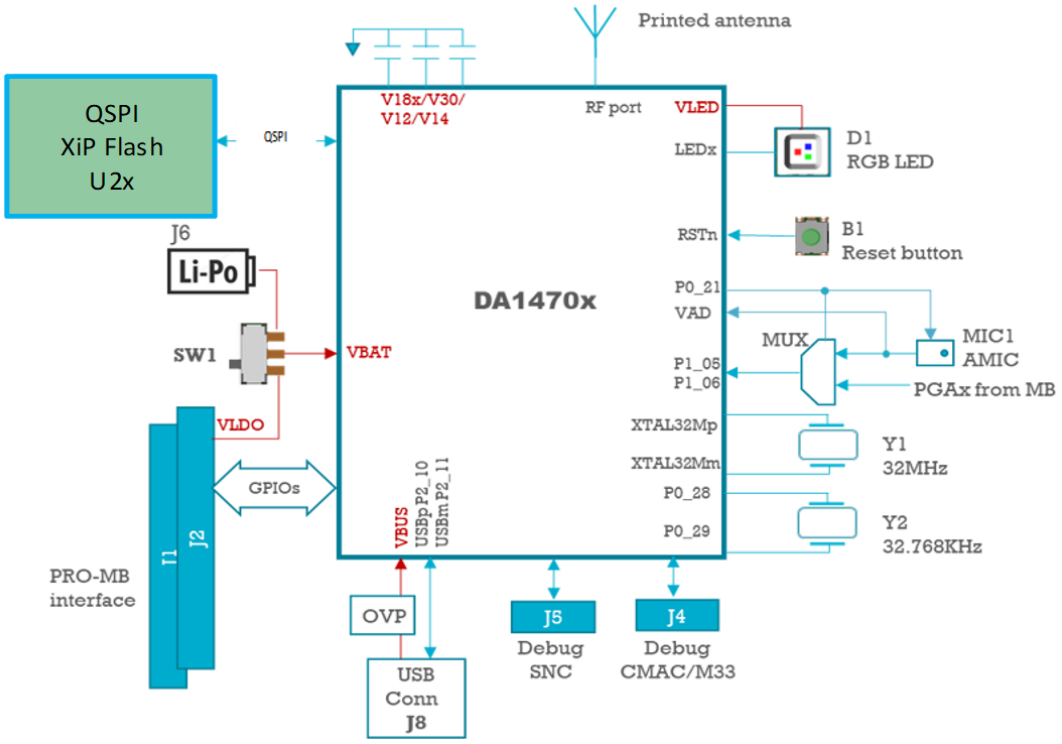


Figure 49: System Block Diagram of DA1470x PRO-Daughterboard

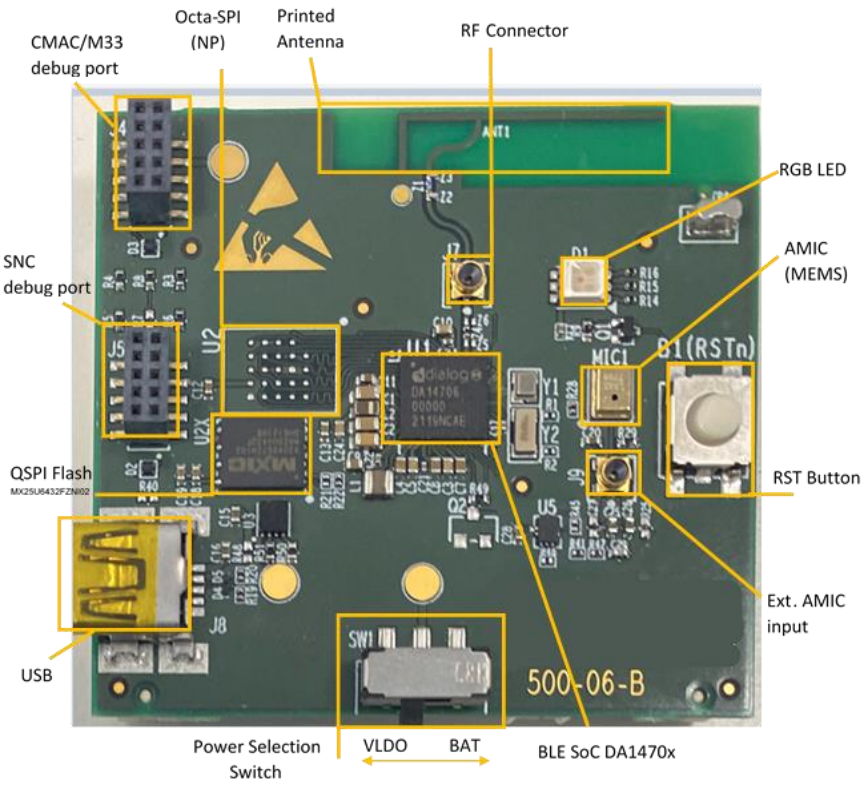


Figure 50: PCB Top of the DA14706 PRO- Daughterboard

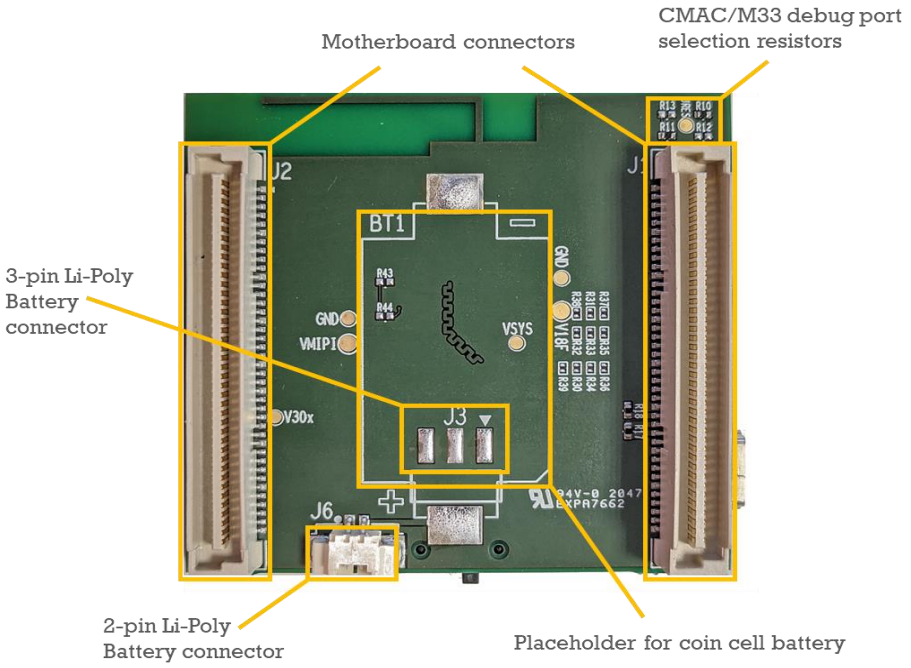


Figure 51: PCB Bottom of the DA1470x PRO- Daughterboard

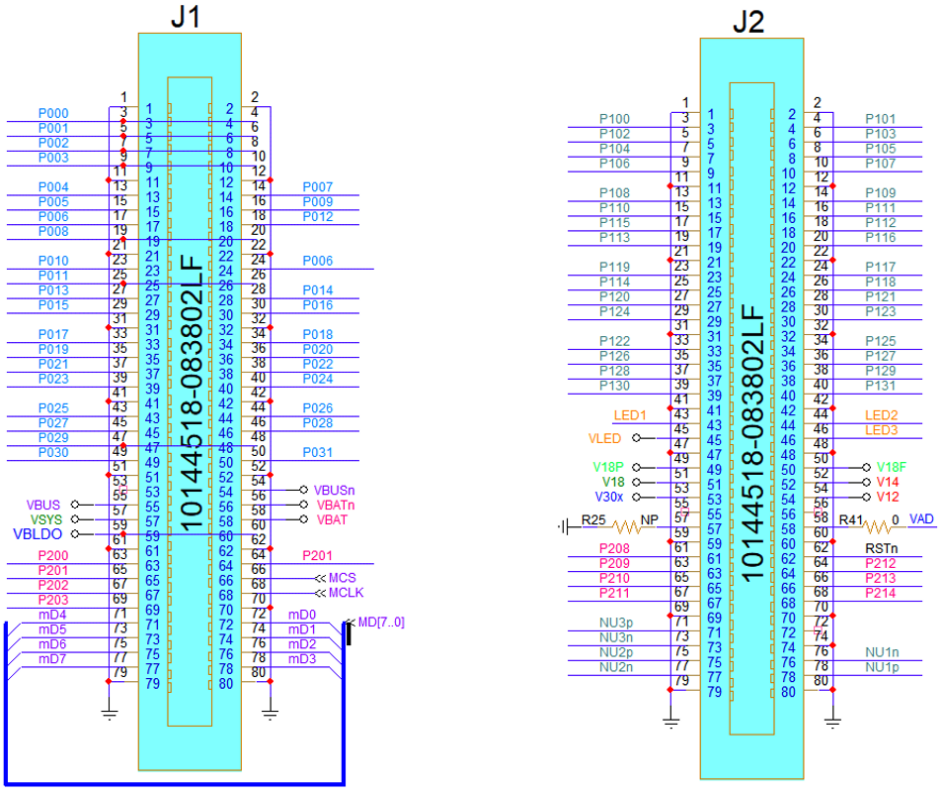


Figure 52: PRO- Daughterboard. Interface Connectors to PRO-Motherboard

7.2 Main Components Description

BLE SoC (U1): DA1470x is a BLE SoC family integrating : the latest Arm® Cortex®-M33 application processor, advanced power management functionality allowing the multi power options approach (LiPo, Coin cell battery),a Graphic Processing Unit (GPU) for advanced graphics processing, a cryptographic security engine, analog and digital peripherals, a dedicated sensor node controller, and

a software configurable protocol engine with a radio that is compliant to the Bluetooth® 5.2 low energy standard.

Table 7 shows the DA1470x SoC family. DA14706 and DA14708 are supported on DA14706 Devkit.

Table 7: DA1470x Product Family Differentiation

Features	DA14701	DA14705	DA14706	DA14708
External PSRAM with data cache	+	x	+	+
JEITA Changer	x	+	+	+
Boost DCDC convertor	x	+	+	+
eMMC	+	x	x	+
Rest of features	+	+	+	+

Table 8 shows a list of the voltage domains either generated (output) by the DA1470x or inserted as inputs.

Table 8: DA1470x SoC Voltage Domains

Voltage Rail	Description	Voltage	Max Current Capability
V_{BAT}	Input: Battery supply rail	4.75 (Max)	
V_{LED}	Output: LED supply voltage	5 V (Max)	150 mA
V_{SYS}	Output: Variable output voltage rail	4.8 V (Typ)	1 A (Max)
V_{30}	Output: 3.0 V power rail	3 V	150 mA (Max)
V_{12}	Output: 1.2 V power rail	1.2 V	150 mA (Max)
V_{14}	Output: 1.4 V power rail	1.4 V	20 mA (Max)
V_{14RF}	INPUT: Radio supply voltage. Connect to V14	1.4 V	
V_{18}	Output: 1.8 V power rail	1.8 V	100 mA (Max)
V_{18F}	Output: 1.8 V power rail	1.8 V	30 mA (Max)
V_{18P}	Output: 1.8 V power rail	1.8 V	100 mA (Max)
V_{BUS}	Input: USB voltage	5 V (Typ)	

32 MHz XTAL (Y1): the main clock of the system is generated from a 32 MHz XTAL which is connected to the internal clock oscillator. The selected crystal for this reference is the XRCGB32M000F1H00R0 of Murata.

Table 9: XTAL32M Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
F_{XTAL}(32M)	Crystal oscillator frequency			32		MHz
ESR(32M)	Equivalent series resistance				60	Ω
C_L(32M)	Load capacitance	No external capacitors are required	5	6	7	pF
Frequency Aging					2	ppm/Year
Δf_{XTAL}(32M)	Crystal frequency tolerance		-10		+10	ppm
Drive Level	Maximum allowable power			150	300	µW
F_{XTAL}(32M)	Crystal oscillator frequency			32		MHz

32.768 kHz XTAL (Y2): a crystal of 32.768 kHz is placed on the pins P2_08 and P2_09 of DA1470x. The selected crystal for this reference is the X CM7V-T1A-32.768kHz-7pF-20PPM-TB-QA from Micro Crystal.

Table 10: XTAL32K Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
f_{CLK_32K}	Clock frequency			32		kHz
f_{XTAL_32K}	Crystal oscillator frequency			32.768		kHz
ESR32K	Equivalent series resistance			50	70	kΩ
C_{L_32K}	Load capacitance			7		pF
C_{0_32K}	Shunt capacitance			1.2		pF
Δf_{XTAL_32K}	Crystal frequency tolerance		-20		+20	ppm
$P_{DRV\_MAX\_32\ K}$	Maximum driver power				1	µW

7.3 Debugging

The DA1470x provides three SWD ports (M33, SNC and CMAC) and a UART port.

On DA14706 PRO-Devkit, by default, SWD ports for M33 and SNC as well as UART port are accessed through the USB connector of PRO-Motherboard. On Daughterboard two debugging connectors are applied (10 Pos, 1.27 mm pitch) one for the CMC/M33 debugging (J4) and one for the SNC debugging (J5). These connectors can provide external access to the corresponded processors.

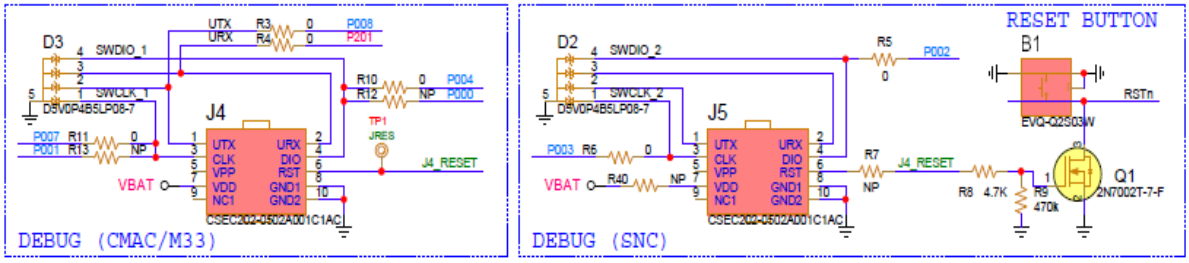


Figure 53: CMAC/M33 and SNC Debugging Connectors Schematic

7.4 Audio

DA1470x SoC provides a Voice Activity Detection (VAD) engine. VAD engine allows DA1470x SoC to stay in sleep mode until enough audible energy has been sensed to trigger an interrupt assertion and consequently wake up the rest of the SoC. On PRO-Daughterboard, an analog microphone (Mic1) is connected to specific pins of DA1470x. SoC through an analog switch (U5).

- **VAD mic (MIC1)**: analog microphone connected on the VAD pin (analog input of the voice activity Detection Engine), MIC1 part number CMM-3729AT-42308-TR of CUI Devices.

An external microphone can be connected on connector/switch J9 if needed. J9 is the MM8130-2600R of Murata. It is an electromechanical connector used for radio signals.

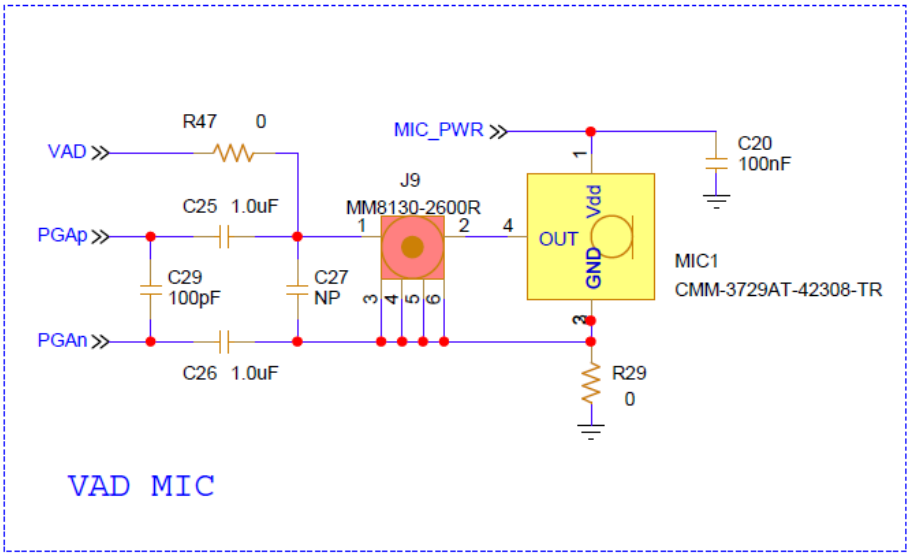


Figure 54: VAD Analog MIC

- **Differential MIC (U5)**: Voice Activity Detection (VAD) mic outputs (PGAp, PGAn) as well as outputs from the digital MIC (P105, P106) placed at the PRO-Motherboard are connected in this differential MIC

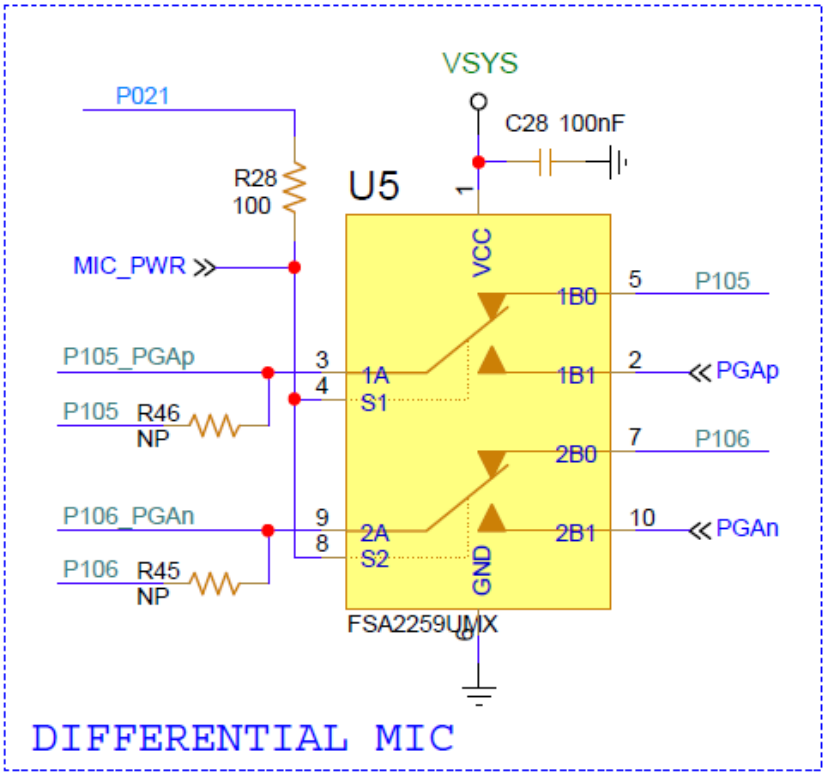


Figure 55: Programmable Gain Amplifier Signal Routing

7.5 RF

A printed F-antenna (ANT1) is used as the radiating element for the DA1470 PRO-DB.

The DA1470x RFIO pin is connected to the printed antenna through a RF strip line and a matching circuit as shown below:

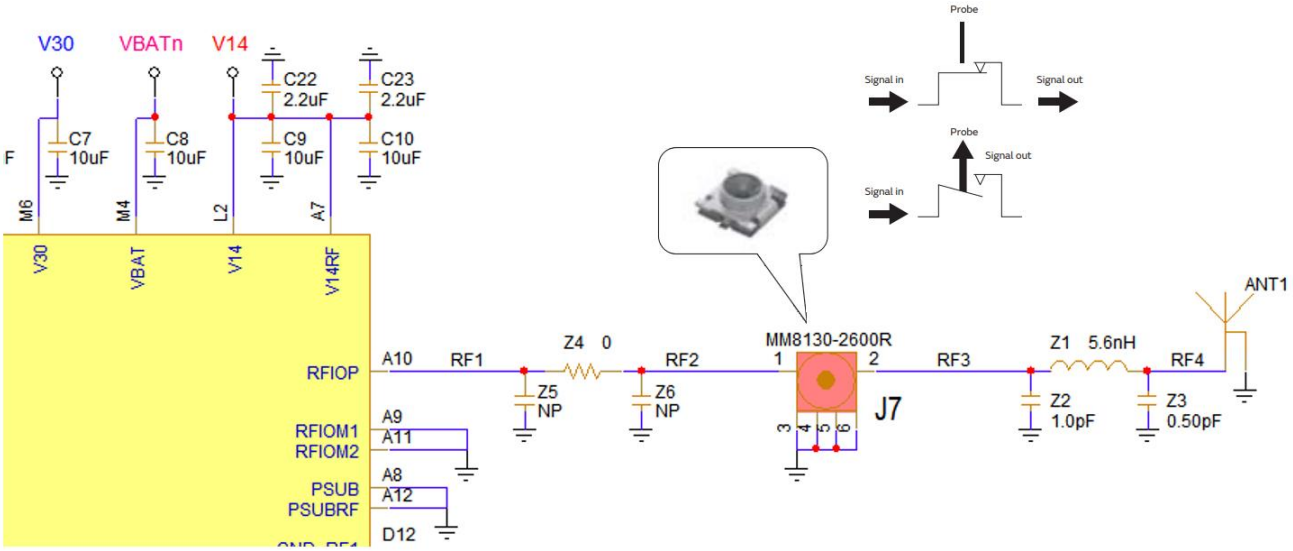


Figure 56: RF Section of PRO-Daughterboard

On PRO-Daughterboard, the printed IFA antenna (ANT1) is enabled.

For conducted measurements J7, MM8130-2600R, microwave coaxial connector with a switch must be used.

The MXHS83QE3000 of Murata (Cable Assembly Coaxial 0.303 m SMA to L Type Probe F-M) must be plugged on J7. The antenna is isolated and the RF signals from/to DA1470x is driven over the coaxial cable.

7.6 Power Section of DA1470x Daughterboard

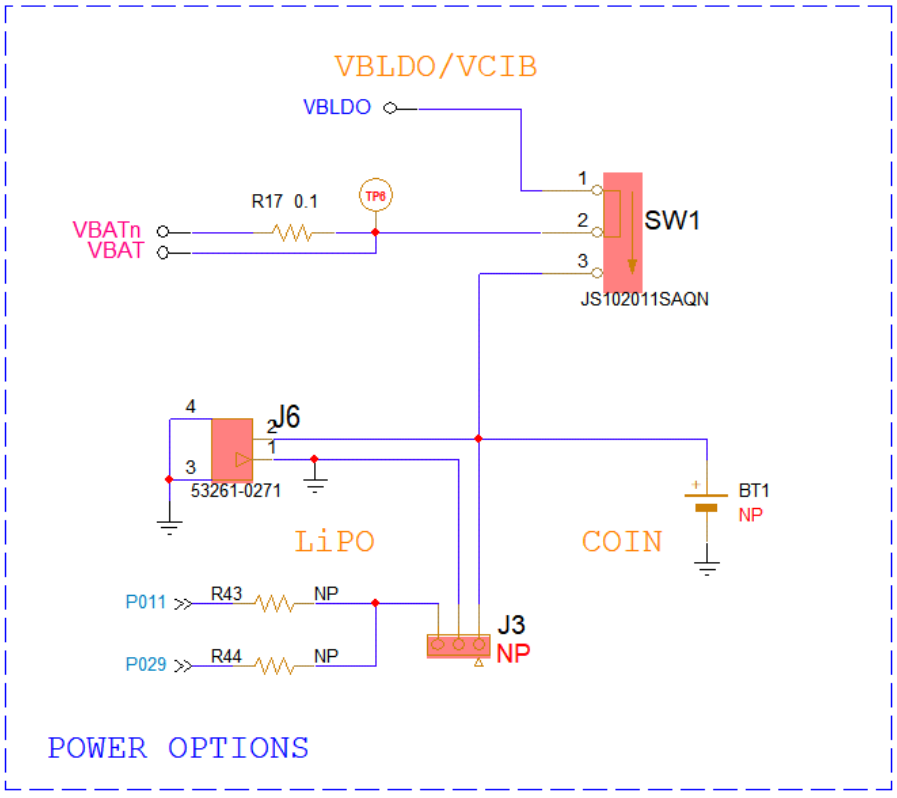


Figure 57: PRO-Daughterboard Power Options

- Battery/Power connectors (shown in Figure 57):
  - 2-pin connector for Li-Ion/LiPo (J6, default), part number: 53261-0271 (mates with 51021-0200)
  - Optional Coin cell holder (unpopulated, CR2032 type)
  - Power selector switch (can be used as on-off switch), (SW1)
  - GPIOs P011 and P029 used for NTC supply and NTC sense respectively

The R17 is acting as a current sense for the current measurement unit in case the PRO daughterboard is battery powered.

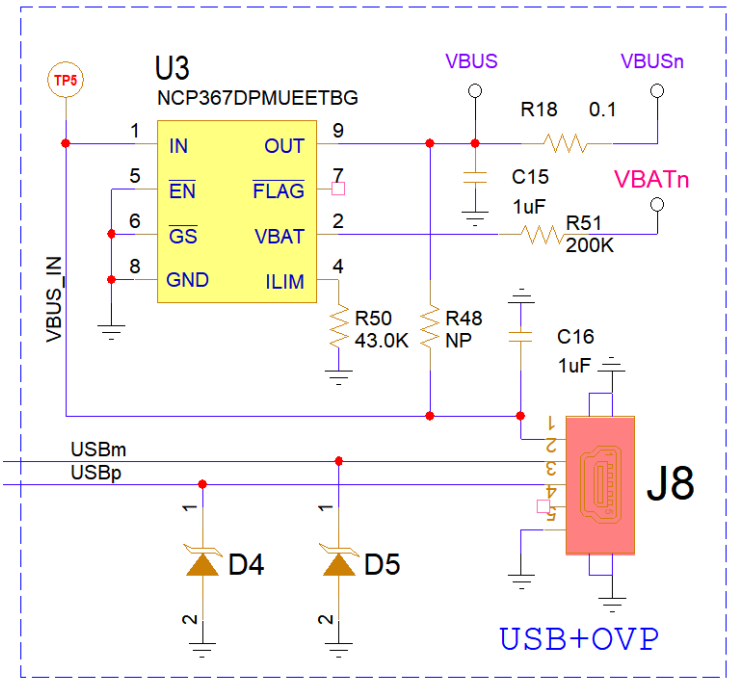


Figure 58: USB OVP Protection (U3) and Rsence (R18)

Figure 58 shows that the OVP protection of the USB is handled by the NCP367DPMUEETBG. This device also provides overvoltage protection for the LiPo battery via the VBAT pin.

R18 is acting as a sensing resistor when the PRO-MB is powered from the USB connector (VBUS).

7.7 QSPI FLASH

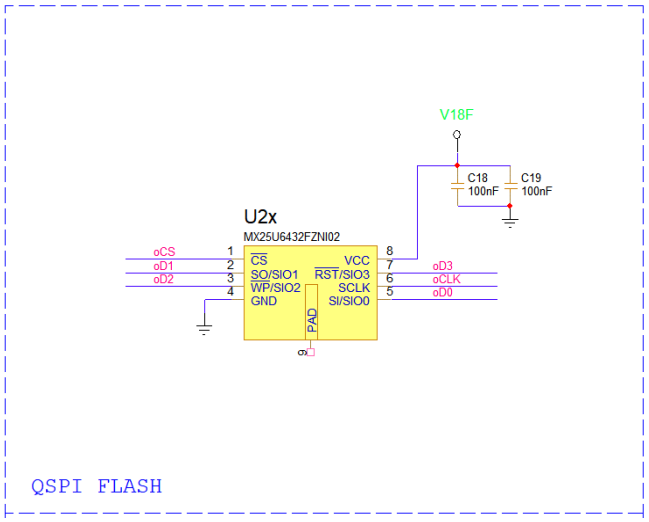


Figure 59: MX25U6432FZNI02 QSPI FLASH Schematic

The 64 Mbit QSPI flash memory used for storage in the PRO- Daughterboard is the MX25U6432FZNI02 from Macronix. During *read* the operating current may reach the 80 mA level, which is beyond the V18F current capability of 30 mA. To ensure that the QSPI flash is properly supplied with sufficient current when operating at 96 MHz V18P and V18F are connected together on PRO-Daughterboard.

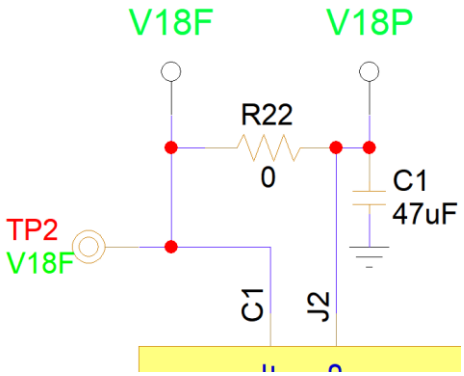


Figure 60: V18P and V18F Are Connected Through R22

The resistor network consisting of resistors R30 to R37 shown in Figure 61 has two purposes:

1. To connect the memory signals on the monitoring headers at the PRO-Motherboard side (shown in Section 4)
2. To disconnect them (for this high-speed signal not to travel long distances and cause reflections and interference).

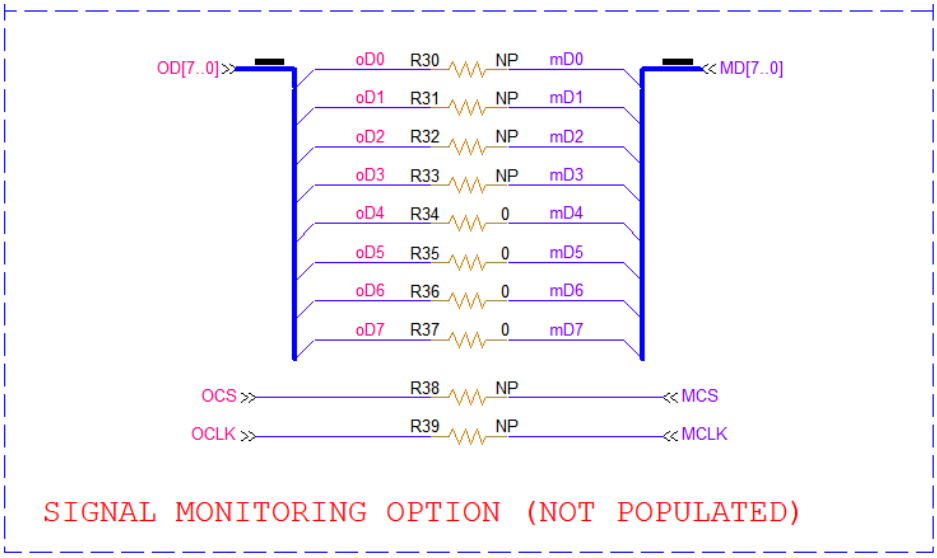


Figure 61: Resistor Network for the Monitoring Signals

Table 11: Flash Memory Signals to the Monitoring Headers at PRO-Motherboard

Flash memory signal	Corresponded GPIO at PRO-MB	Monitoring header at PRO-MB	Direct Connectivity to Monitoring Headers
oD0	oD0	J5 (7)	Resistor R30 should be mounted, PCB marking see Figure 61Figure 62
oD1	oD1	J5 (8)	Resistor R31 should be mounted PCB marking see Figure 61
oD2	oD2	J5 (9)	Resistor R32 should be mounted PCB marking see Figure 61
oD3	oD3	J5 (10)	Resistor R33 should be mounted PCB marking see Figure 61
oD4	P204oD4	J5 (11)	Yes
oD5	P205oD5	J5 (12)	Yes
oD6	P206oD6	J5 (15)	Yes
oD7	P207oD7	J5 (16)	Yes
oCS	oCS	J5 (24)	Resistor R38 should be mounted PCB marking see Figure 61
oCLK	oCLK	J5 (28)	Resistor R39 should be mounted PCB marking see Figure 61

Note that in the PCB layout, the GPIO signals (J5 monitoring header) need a resistor to be populated to connect to the monitoring headers. These are marked with a surrounding frame as shown in Figure 62 (yellow highlight).

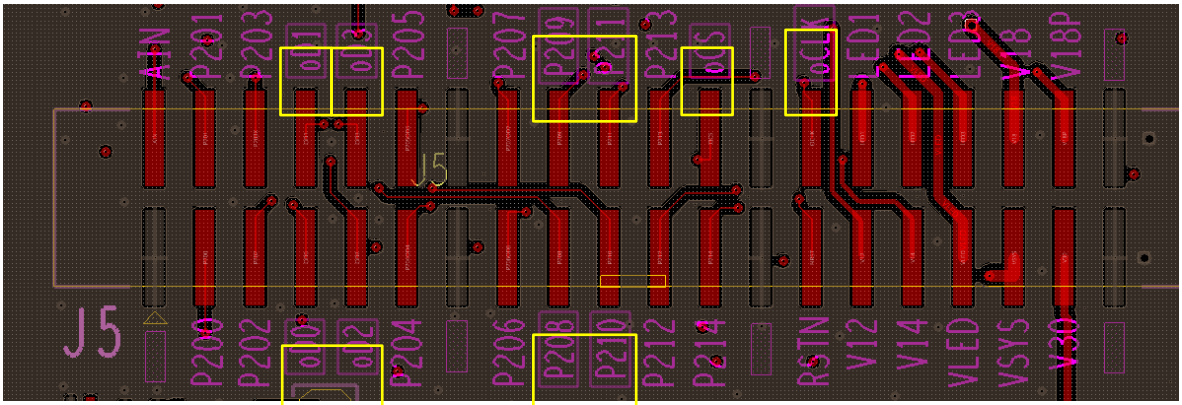


Figure 62: PCB Marking of GPIO Signals not Directly Connected to Monitoring Headers

There is an option for the user to connect a 1Gbit OCTAL NOR flash memory (MX66UM1G45GXD from Macronix) used for storage. This OCTA flash memory is not being populated along with the correlated monitoring resistors (R30-R33) shown in Figure 63.

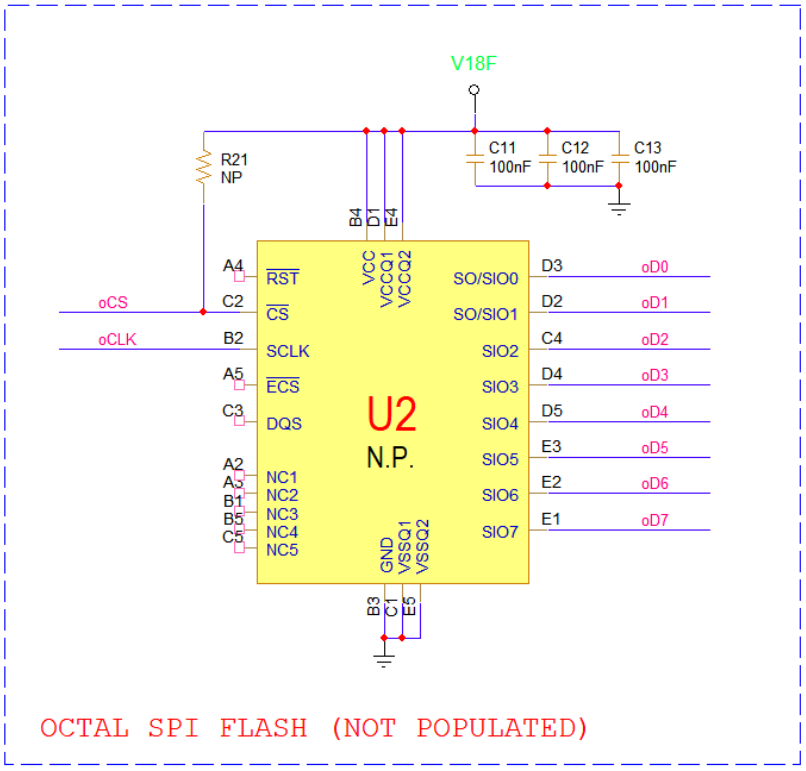


Figure 63: MX66UM1G45GXD OSPI FLASH Schematic

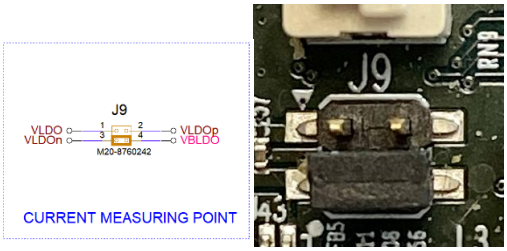
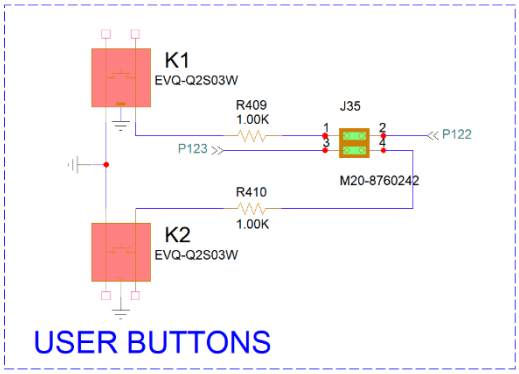
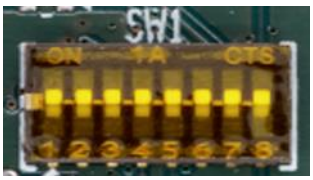
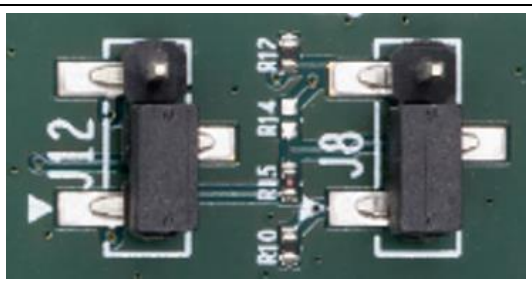
8 Quick Setup

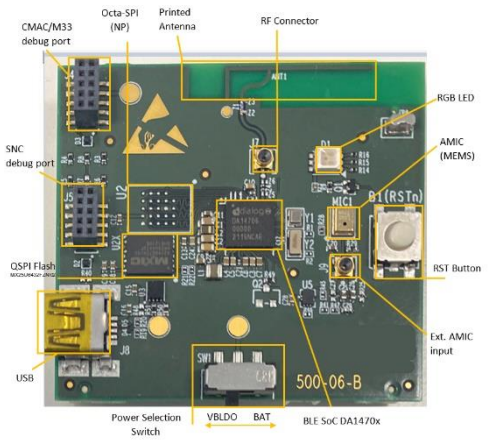
8.1 Hardware Setup

NOTE
Supplying PRO- Daughterboard, only from USB connector, whereas it is plugged on the PRO-MB which is not powered-on should be avoided.

For proper operation, PRO-Motherboard must be always plugged to source (for example PC, laptop and so on) through USB. The reason is that several circuits (for example analog switches, PMM2 module and so on) are supplied from the USB connector of the Pro-MB.

Table 12: DA14706 PRO-Development Kit, Quick Setup

			Description	Comments
PRO-Motherboard	1	Apply jumper on J9.3 and J9.4		Provide power to PRO Motherboard **Important note**: If power measurement module is not connected, see Table 6
	2	Apply jumper on: J35.1 and J35. 2 J35.3 and J35. 4		P122 is used on JTRACE
	3	Ensure DIP Switch correct setting. (Set to ON by default)		SW1 for Debugger
	4	Apply jumpers on power switches: J8.1 and J8.2 J12.1 and J12.2		

PRO-Daughterboard	5	Ensure correct power source and position for SW1		Define power source for PRO-Daughterboard **VBLDO**: 3 V. It is generated on PRO-Motherboard **BAT**: it is supplied from LiPo battery or Coin cell

8.2 Debug Interfaces – SWD/JTAG

There are two onboard debug interfaces with maximum speed of 4 MHz.

The debugger with the lower serial number is assigned to M33. This number is also used as Serial Number for the PRO-Motherboard. A label has been attached on the backside of the PCB.

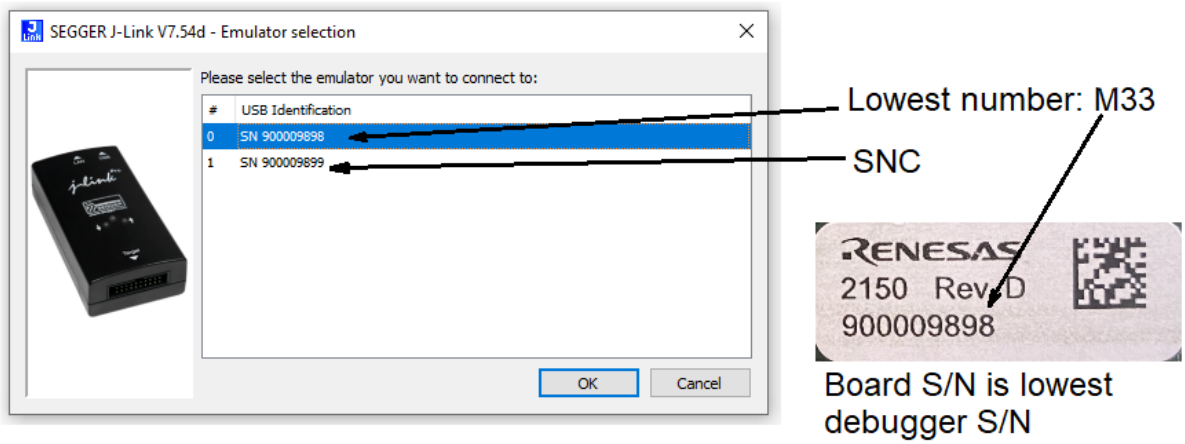


Figure 64: SWD/JTAG Ports to Use

8.3 Debug Interfaces – UART

After connecting the USB port, two virtual COM parts are created on the PC. The COM port with the lowest number is used for UART communication to the DA1470x. The other COM port is used for SPI communication to the Power Management Module.

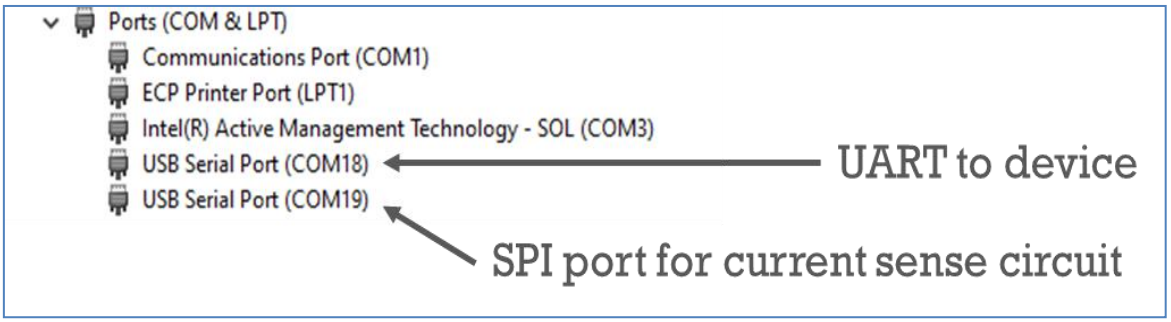


Figure 65: Virtual COM Port Selection

Revision History

Revision	Date	Description
1.2	03-Oct-2022	Modifications + editorial
1.1	30-Jun-2022	Updated Table 6 and Table 12.
1.0	20-Jun- 2022	Initial version.