HIGHLY INTEGRATED POWER MANAGEMENT IC FOR INTEL® ATOM™ Z3000 PROCESSOR

1. General Description

The DA6021 PMIC is a monolithic single chip power management IC for Intel® Atom™ Z3000 processor. It provides all power supplies for tablet PC's and can also be used in multiple embedded applications as well as Netbooks and Nettops. It is designed to support platforms based on Intel's Z3000 Atom processor series, including DDR3 memory and various peripherals.

Integrated power management

Dialog Semiconductor's new DA6021 uses a single supply voltage at a wide range of input voltage and provides low noise supplies to all SoC voltage domains, DDR3 memory and many peripherals.

The DA6021 integrates 6 high performance low dropout (LDO) voltage regulators using Dialog's patented Smart Mirror™ technology for very low quiescent current. It includes 11 internal power switches and the control logic for 9 external switching devices. These include in-rush current control for platform power distribution simplification. Six fully integrated high efficiency DC-DC buck converters provide current to Intel Atom platform's various low voltage domains as well as to the memory and the peripherals. Two buck-boost and one boost converter also supply energy for the platform. All nine regulators are designed to support external component height of 1mm.

Ultra flexible power sequencer

The ultra-flexible power sequencer takes care of the complete platform start-up, state-transitioning and power-down procedure. The DA6021 operates autonomously and reduces the power consumption when entering stand-by or power down mode. The DA6021 is fully programmable and allows adaption to all Intel Atom processor Z3000 and platform sequences. The OTP programmed power sequence is copied into operational registers during power-up. Those registers can be overwritten by EEPROM after initial OTP copy routine or via operational processor.

Auxiliary function

An analogue to digital converter (ADC) with 10-bit resolution combined with a multi-channel input multiplexer allows measurement of the input supply voltage, battery ID, PMIC die temperature as well as 5 battery pack & system temperatures. The number of external components is significantly reduced due to the integration of 16 GPIO's, 3 channel PWM output signal generators, a multi-input detector with a charger control as well as a programmable IRQ controller.

2. Key Features

- Two high efficiency buck converters with integrated SVID interface running IMVP-7 protocol. These two quad phase DC/DC regulators generate the voltages for CPU and graphic cores
- One dual phase buck regulator for memory supply supporting DDR3-L and -LP memory types
- 3 single phase buck regulators supplying 1.0V, 1.05V and 1.8V towards the platform
- 2 buck-boost converters generating 2.85V and 3.3V for the platform even if the input supply is down to 2.7V
- Boost converter providing 5V for the USB components
- 3 LDOs with fixed output voltage
- 2 LDO with programmable output voltage
- 1 push-pull LDO used for DDR3 address line termination
- 11 integrated power rail switching devices
- 9 external power rail switching devices
- Ultra flexible power sequencer programmable via OTP/ EEPROM and register
- I2C communication interface for SoC access
- EEPROM interface for optional OTP over-writing
- 16 general purpose I/Os with alternate functions
- 16 channel 10-bit ADC including conditioning circuits and programmable flexible sequencing for automatic and manual measurements
- System voltage and temperature monitoring, supervising
- Programmable IRQ controller
- 1-wire digital battery interface including 2-wire conversion
- 3 channel PWM signal generation, flexible frequency and duty cycle programmable
- Input power source detection, included with charger control

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3. Revision History

Version	Date	Description
2.A	2012.09.08	First preliminary datasheet
2.B	2012.09.26	Updated ordering information Updated package outline drawing
2.C	2013.05.03	Corrected VSYSU pin types table 4: Pin Description Updated figure 16: Buck VNN Block Diagram Corrected IMAX value in chapter 11.5.2.1 Updated electrical parameters for buck VCC Updated electrical parameters for buck VNN Updated electrical parameters for buck V1P0A Updated electrical parameters for buck V1P05S Updated electrical parameters for buck V1P8A Updated electrical parameters for buck VDDQ Updated electrical parameters for buck boost V2P85S Updated electrical parameters for buck boost V3P3A Updated electrical parameters for boost V5P0S Corrected table 51 naming VDCIN replaced by VDCIN_SENSE VBUS replaced by VBUS_SENSE Updated SVID Status1 registers Included chapter 23 “Debug Ports” Updated ICCMAX alert in Status1 SVID register Included chapter 11.6 “Current Monitor” including typical current sensing errors on the 5 power rails Removed SVID registers 0x07 and 0x0A Added SVID registers 0x14, 0x15, 0x1D, 0x1E, 0x1F, 0x20, 0x2D, 0x2E and 0x2F Updated chapter 10.3 “DA6021 Power Sequences”, included timing diagrams and tables Added efficiency curves for all DC/DC regulators Updated descriptions of internal and external switches Updated PBCONFIG register with new feature of programmable power button debounce time Updated PBSTATUS register with new feature disabling the power button detection for a programmable time Updated register map chapter 24 Updated the content of the following registers: IRQLVL1, MIRQLVL1, VCRIT_CFG, EVENTMAN1, MEVENTMAN1,

Version	Date	Description
		MANCONV1, TSENABLE,TS_CRIT_ENABLE, A0_ST, A1_ST and CRIT_ST,
2.D	2013.05.28	Added information how electrical parameters are validated Included SVID Buffer AC parameters Platform SVID bus timing requirements Included maximum power path routing DC resistance requirement on several rails Added further electrical parameters for Vref Included electrical parameters for VHOST & VBUS output signal Updated ADC channel allocation Updated several register names and dedicated bits Included state transitions tables and conditions Added detailed information on critical events including timings Included current monitor function details Added charger control pin details Several editorial updates
2.E	2013.07.15	Updated MPWRSRCIRQS0 register content Corrected MPWRSRCIRQSX register content Updated reset value of register LOWBATDET0 Corrected reset value of register LOWBATDET1 Updated and corrected the description of the reset source register RESETSCR1 Added register PWRSEQCFG into register map chapter 24 Corrected reset value of register MADCIRQ1 Added S0iX_SVID register in table 34 SVID Supported Registers Corrected number of output caps for VDDQ, V3P3A & V5P0S Corrected table 76 SDIO voltage selection Updated bit naming of SPWRSRC register Renamed MSYS3ALRTx by MSYS2ALRTx in MTHERMIRQ0/1 register Updated reset value of VWARNA_CFG register Corrected description of MBCUIRQ register
2.F	2013.12.13	Changed “new Intel Atom processor” into “Intel Atom processor Z3000” Updated the BOM Updated figure 11: Enter S0iX Sequencing Diagram (VCCAPWROKCFG=0)
2.G	2013.12.17	Added note regarding behaviour V2P85S chapter 11.6.10

Version	Date	Description
3.A	2013.01.27	Version after receiving Intel's PRQ statement Editorial changes in the register descriptions Corrected typo in VHDMI_CTRL register Updated BOM, cost and size optimized

4. Overview

DA6021 features:

- **Power sequencer & System control:** DA6021 includes an ultra-flexible power sequencer programmable via OTP during manufacturing process and modifiable via external EEPROM data. It controls the DA6021 blocks, the power sequences, the programmed ADC sequence, interacts with the SoC and the peripherals
- **Supply Sources**
  - 6 Buck Regulators
  - 2 Buck-Boost Regulators
  - 1 Boost Regulator
  - 6 LDO Regulators
  - 11 internal power rail switches
  - 9 external power rail switches
  - 2 Power mux switches where the supply source can be selected
- **Communication Interfaces**
  - I2C (slave device) mastered from the SoC
  - Handshake/control signals from/towards the SoC and peripherals
  - SVID (slave device) mastered from the SoC, but capable of interrupt from the PMIC
  - I2C (master device) or EEPROM Interface, used to read EEPROM during first power up.
- **Input Source Power Detection**: DA6021 will detect connected power sources and provide such information towards the SoC and/or charger. VBAT, VBUS_SENSE, VDCIN_SENSE and VSYS nodes will be permanently monitored via comparators for insertion, removal events. Furthermore they will be measured via the GPADC in order to take decision on the boot process.
- **System Voltage and Temperature Measurement**: it monitors the DA6021 input voltage at VSYS, the on-die temperature as well as the battery and platform sensor temperatures. It detects over- and under-voltage conditions. If activated, it can issue critical events.
- **GPADC**: The GPADC is primarily for temperature and voltage measurements. It can run predefined sequences or a single programmable one. It supports automatic and manual measurement methods and can also run also in a standby mode at programmable long intervals.
- **Digital Battery Interface:** 1-wire protocol agnostic digital communication between battery and SoC. It introduces a level shifting between the SoC and the main battery
- **OTP & EEPROM Interface:** DA6021 will read its parameters from integrated OTP during power on reset. Optionally those OTP parameter settings can be overwritten by an external EEPROM for back-up solution, debugging or development. Note, The OTP can’t be overwritten and the EEPROM can’t be programmed via the DA6021
- **Platform Back-up Battery Charger:** DA6021 includes an autonomous charger for platform backup batteries such as coin cells or “supercaps”.
- **Display control**:
- **BCU**: Battery controller unit, supervising peripherals based on system voltage
- **PWM**: to accommodate some external functionality, DA6021 can generate up to 3 PWM signals with programmable duty-cycle and frequency.
- **GPIOs**: 16 general purpose I/O with alternate functions.

5. Block Diagram

5.1 Overview Diagram

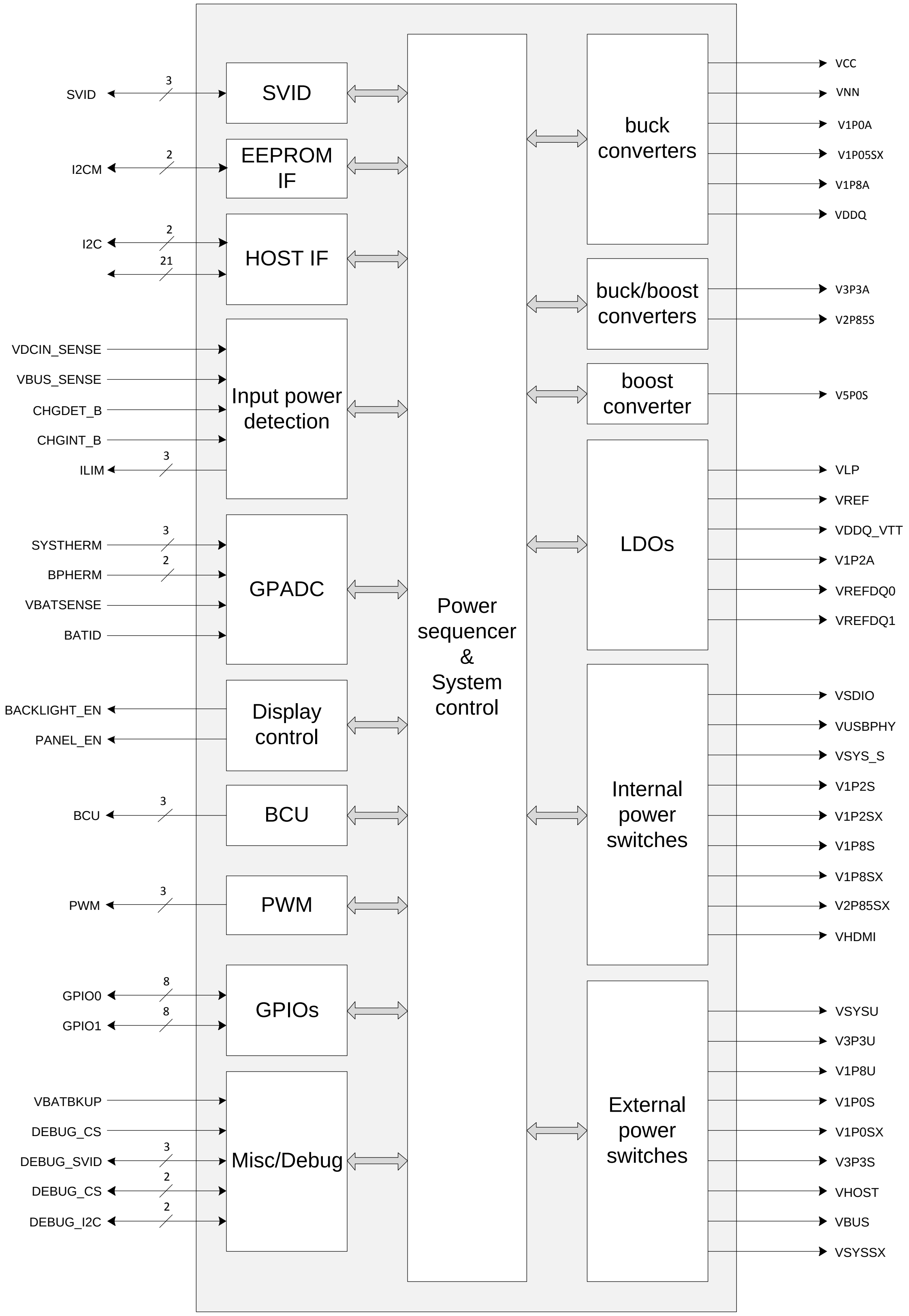


Figure 1: Overview Diagram

5.2 Detailed Block Diagram

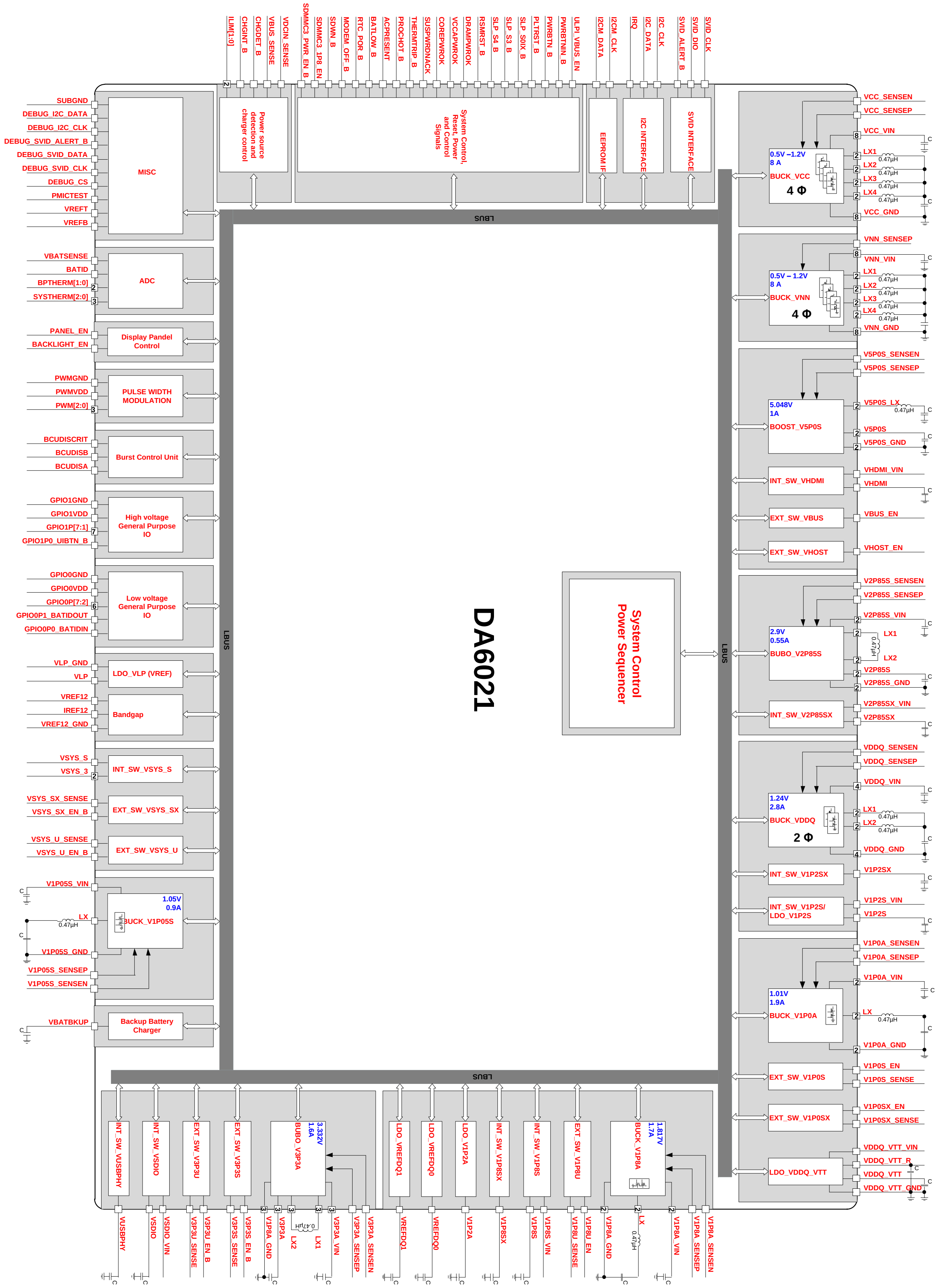


Figure 2: Detailed Block Diagram

6. Operating Conditions

All Voltages are referenced to VSS unless otherwise stated. Currents flowing into DA6021 are deemed positive, currents flowing out are deemed negative.

All parameters are valid over the full operating temperature range and power supply range unless otherwise noted. Please note that the power dissipation must be limited to avoid overheating of DA6021. The maximum power dissipation should not be reached with maximum ambient temperature.

6.1 Absolute Maximum Ratings

Parameter	Conditions	Min	Max	Unit	Val
Storage Temperature	TSTOR	-65	+150	°C	Q
Operating Temperature free-air	TAMB	-30	+85	°C	E
Power Supply Input	VSUP	-0.3	+5.5	V	E/Q
IO Input	(All unless otherwise stated)	-0.3	VSUP+0.3	V	Q
Maximum power dissipation	60°C ambient temperature 55mmx100mmx0.75mm PCB		2.0	W	D,E
Package thermal resistance			TBD	K/W	D,E
ESD CDM (Charge Device Model)	All pins unless otherwise stated.		±500	V	Q
ESD HBM (Human Body Model)	All pins unless otherwise stated.		±2	kV	Q

Table 1: DA6021 Absolute Maximum Ratings

6.2 Recommended Operating Conditions

Parameter	Conditions	Min	Max	Unit	Val
Operating Temperature free-air	TAMB	-30	+85	°C	E,Q
Power Supply Input	VSUP	2.7	4.5	V	E,Q

Table 2: DA6021 Recommended Operating Conditions

The maximum allowed operational die temperature is defined to 125°C. Below you can find the time constraints in relation to the peak power dissipation. The simulation results are based on

- 10 layer board, 70x170x0.8mm^3
- Natural convection, air velocity 0m/s
- Surface-to –surface radiation
- Package initializes at 0.25W with initial temperature of 38°C
- Surrounding ambient temperature in immediate vicinity at 31°C
- Maximum power burst exposure of 100s

Various power burst scenarios at: 0.76, 0.96, 1.20, 2.90, 3.72, 4.52 and 7.0W

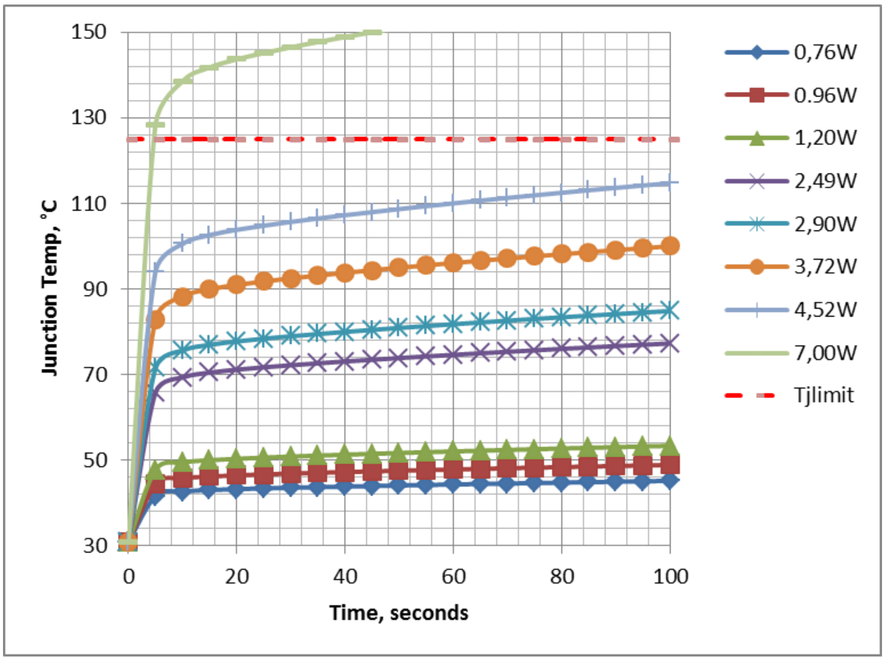


Figure 3: Maximum Allowed Peak Power

VAL status	Description of Abbreviation
D	Parameter is guaranteed by design
E	Parameter is confirmed by silicon evaluation
Q	Parameter is verified by silicon qualification
A	Parameter is screened during final ATE test
A*	Parameter is screened during final ATE test by indirect measurement or with a special test set-up

Table 3: Abbreviations of Validation Status

7. Ordering Information

The order number consists of the part number followed by a suffix indicating a.o. the packing method. For details, please consult the Dialog customer portal on our web site or your local sales representative.

Part Number	Package Name	Package description	Package Outline
DA6021	FCBGA	325 pin, FCBGA 11x6mm, 0.4mm pitch	Figure 76

Current OTP variant: -08 (Intel approved)

8. Pinning Information

The “_B” symbol at the end of a signal name indicates that the active or asserted state occurs when the signal is at a low voltage level (active low). When the “_B” is not present after the signal name the signal is asserted when the signal is at a high voltage level.

	Pin Name	Pins	Power Domain	Description	Type
VCC	VCC_VIN	8	VSYS	VCC buck input supply	IP
	VCC_GND	8	GND	VCC buck ground	IP
	VCC_LX	8	VSYS	Quad phase switching nodes	OP
	VCC_FBP	1	VCC	VCC feedback positive sense	IA
	VCC_FBN	1	VCC	VCC feedback ground sense	IA
VNN	VNN_VIN	8	VSYS	VNN buck input supply	IP
	VNN_GND	8	GND	VNN buck ground	IP
	VNN_LX	8	VSYS	Quad phase switching nodes	OP
	VNN_FBP	1	VNN	VCC feedback positive sense	IA
V1P0A	V1P0A_VIN	2	VSYS	V1P0A buck input supply	IP
	V1P0A_GND	2	GND	V1P0A buck ground	IP
	V1P0A_LX	2	VSYS	V1P0A phase switching nodes	OP
	V1P0A_FBP	1	V1P0A	VCC feedback positive sense	IA
	V1P0A_FBN	1	V1P0A	VCC feedback negative sense	IA
V1P05S	V1P05S_VIN	1	VSYS	V1P05S buck input supply	IP
	V1P05S_GND	1	GND	V1P05S buck ground	IP
	V1P05S_LX	1	VSYS	V1P05S phase switching nodes	OP
	V1P05S_FBP	1	V1P05S	V1P05S feedback sense pos	IA
	V1P05S_FBN	1	V1P05S	V1P05S feedback sense neg	IA
VDDQ	VDDQ_VIN	4	VSYS	VDDQ buck input supply	IP
	VDDQ_GND	4	GND	VDDQ buck ground	IP
	VDDQ_LX	4	VSYS	VDDQ phase switching nodes	OP
	VDDQ_FBP	1	VDDQ	VDDQ feedback positive sense	IA
	VDDQ_FBN	1	VDDQ	VDDQ feedback negative sense	IA
V1P8A	V1P8A_VIN	2	VSYS	V1P8A buck input supply	IP
	V1P8A_GND	2	GND	V1P8A buck ground	IP
	V1P8A_LX	2	VSYS	V1P8A phase switching nodes	OP
	V1P8A_FBP	1	V1P8A	V1P8A feedback positive sense	IA
	V1P8A_FBN	1	V1P8A	V1P8A feedback negative sense	IA
V3P3A	V3P3A_VIN	3	VSYS	V3P3A buck boost input supply	IP
	V3P3A_GND	3	GND	V3P3A buck boost ground	IP

	V3P3A_LX1	3	VSYS	V3P3A LX node 1	IA
	V3P3A_LX2	3	VSYS	V3P3A LX node 2	IA
	V3P3A	3	V3P3A	V3P3A output	OP
	V3P3A_FBP	1	V3P3A	V3P3A feedback positive sense	IA
	V3P3A_FBN	1	V3P3A	V3P3A feedback ground sense	IA
V2P85S	V2P85S_VIN	2	VSYS	V2P85S buck boost input supply	IP
	V2P85S_GND	2	GND	V2P85S buck boost ground	IP
	V2P85S_LX1	2	VSYS	V2P85S LX node 1	IA
	V2P85S_LX2	2	VSYS	V2P85S LX node 2	IA
	V2P85S	2	V2P85S	V2P85S output	OP
	V2P85S_FBP	1	V2P85S	V2P85S feedback positive sense	IA
	V2P85S_FBN	1	V2P85S	V2P85S feedback ground sense	IA
V5P0S	V5P0S_GND	2	GND	V5P0S buck boost ground	IP
	V5P0S_LX	2	VSYS	V5P0S LX node 1	IA
	V5P0S	2	V5P0S	V5P0S output	OP
	V5P0S_FBP	1	V5P0S	V5P0S feedback positive sense	IA
	V5P0S_FBN	1	V5P0S	V5P0S feedback positive sense	IA
VDDQ_VTT	VDDQ_VTT_VIN	1	V1P0A	VDDQ_VTT input voltage	IP
	VDDQ_VTT_GND	1	GND	VDDQ_VTT ground	IP
	VDDQ_VTT	1	VDDQ_VTT	VDDQ_VTT output voltage	OP
	VDDQ_VTT_R	1	VDDQ_VTT	VDDQ_VTT reference voltage	OP
V1P8U	V1P8U_EN_B	1	V1P8A	V1P8U enable signal	OD
	V1P8U_FB	1	V1P8U	V1P8U sense line	IA
V1P8S	V1P8S_VIN	1	V1P8A	V1P8S input voltage	IP
	V1P8S	1	V1P8S	V1P8S output voltage	OP
V1P8SX	V1P8SX	1	V1P8SX	V1P8SX output voltage	OP
V1P2S	V1P2S	1	V1P2S	V1P2S output voltage	OP
V1P2A	V1P2A	1	V1P2A	V1P2A output voltage	OP
V1P2SX	V1P2SX	1	V1P2SX	V1P2SX output voltage	OP
	V1P2SX_IN	1	V1P8A	V1P2SX input voltage	IP
VREFDQ0	VREFDQ0	1	VREFDQ0	VREFDQ0 output voltage	OP
VREFDQ1	VREFDQ1	1	VREFDQ1	VREFDQ1 output voltage	OP
V3P3U	V3P3U_EN	1	V3P3A	V3P3U input voltage	IP
	V3P3U_FB	1	V3P3U	V3P3U output voltage	OP
V3P3S	V3P3S_EN_B	1	V3P3A	V3P3S enable signal	OD
	V3P3S_FB	1	V3P3S	V3P3S sense signal	IA
VSDIO	VSDIO_VIN	1	V3.3A	VSDIO input voltage	OP
	VSDIO	1	VSDIO	VSDIO output voltage	OP
VUSBPHY	VUSBPHY	1	VUSBPHY	VUSBPHY output voltage	OP
VHOST	VHOST_EN	1	VHOST	VHOST enable signal	OD
VBUS	VBUS_EN	1	VBUS	VBUS enable signal	OD
	ULPI_VBUS_EN	1	VSYS	Input signal to enable VBUS	ID
VHDMI	VHDMI_VIN	1	VHDMI	VHDMI input voltage	IP
	VHDMI	1	VHDMI	VHDMI output voltage	OP
V2P85SX	V2P85SX_VIN	1	V2P85S	V2P85SX input voltage	IP

	V2P85SX	1	V2P85SX	V2P85SX output voltage	OP
VSYSU	VSYSU_EN	1	VSYS	VSYSU input voltage	OP
	VSYSU_FB	1	VSYSU	VSYSU output voltage	IP
VSYSS	VSYSS	1	VSYSS	VSYSS output voltage	OP
VSYS_SX	VSYS_SX_EN#	1	VSYS_SX	VSYS_SX enable signal	OD
	VSYS_SX_FB	1	VSYS_SX	VSYS_SX sense signal	IA
V1P0S	V1P0SEN	1	V1P0A	V1P0S enable signal	OD
	V1P0S_FB	1	V1P0A	V1P0S sense signal	IA
V1P0SX	V1P0SXEN	1	V1P0A	V1P0SX enable signal	OD
	V1P0SX_FB	1	V1P0A	V1P0SX sense signal	IA
BG	VREF12	1	VREF12	Bandgap reference voltage	OP
	IREF12	1	IREF12	Bandgap reference current	OP
	VREF12_QUIET	1	VSS_QUIET	quiet ground connection	IP
VLP	VLP	1	VLP	VLP output voltage	OP
	VLP_GND	1	VLP_GND	VLP ground	IP
VSYS1/2	VSYS	2	VSYS	DA6021 input supply voltage	IP
SVID	SVID_CLK	1	V1P0S	Serial VID clock signal	ID
	SVID_DIO	1	V1P0S	Serial VID data in/out	IOD
	SVID_ALERT_B	1	V1P0S	Serial VID to SoC interrupt	OD
Power source detection & charger control	VDCIN_SENSE	1	5V	AC/DC adapter input voltage detection (20V via ext. components)	IP
	ACPRESENT	1	V1P8	Valid AC/DC adapter voltage detection	OD
	VBUSSENSE	1	VUSBPHY	USB input voltage detection (20V via ext. components)	IP
	CHGDET_B	1	VSYS	USB DCP detection from USBPHY (0=USB DCP)	ID
	CHGRINT_B	1		Battery charging status 0=charging in progress 1=charging complete	IA
	ILIM[1:0]	2	VSYS	Charging current limit	OD
System control	I2C_CLK	1	V1P8S	I2C clock signal	ID
	I2C_DATA	1	V1P8S	I2C data IO	IOD
	IRQ	1	V1P8S	Interrupt signal to So	OD
	I2CM_CLK	1	VSYS	I2C clock signal	OD
	I2CM_DATA	1	VSYS	I2C data IO	IOD
	PWRBTNIN_B	1	VSYS	System power button input	ID
	PWRBTN	1	V1P8A	System power button output	OD
	PLTRST_B	1	V1P8A	Platform reset signal	OD
	SLP_S0iX_B	1	V1P8A	Standby S0iXtrigger 0=enter S0iX 1=exit S0iX	ID
	SLP_S3_B	1	V1P8A	Sleep S3 trigger 0=enter S3 1=exit S3	ID
	SLP_S4_B	1	V1P8A	Sleep S4 trigger 0=enter S4 1=exit S4	ID
	RSMRST_B	1	V3P3A	Resume reset to SoC, de-assertion (=1) after V3P3A	OD

	DRAMPWROK	1	VDDQ	Asserted after VDDQ stable	OD
	VCCAPWROK	1	VDDQ	Power good indication to SoC	OD
	COREPWROK	1	V3P3A	Power good indication to SoC	OD
	SUSPWRDNACK	1	V1P8A	power off indication for _A power rails	ID
	BATLOW_B	1	V1P8A	Indicating that battery voltage is not high enough to boot	OD
	THERMTRIP_B	1	V1P8S	Catastrophic thermal event, shut down all power rails	ID
	PROCHOT_B	1	V1P0S	Open drain output to SoC indicating to limit the power	OD
	SDMMC3_1P8_EN	1	V1P8S	1.8/3.3V selection for SD card 0=3.3V 1=1.8V	ID
	SDMMC3_PWR_EN_B	1	V1P8S	SD card power enable 1=off	ID
	MODEM_OFF_B	1	V1P8A	Modem reset signal	OD
	SDWN_B	1	V1P8A	System shut down warning or SIM card removal	OD
	RTCPOR	1	VRTC	Power on reset from system to PMIC	ID
Low voltage GPIOs	GPIO0P0_BATIDIN	1	GPIO0VDD		IOD
	GPIO0P1_BATIDOUT	1	GPIO0VDD		IOD
	GPIO0P[7:2]	6	GPIO0VDD		IOD
	GPIO0VDD	1	V1P8A	Low voltage GPIO supply	IP
	GPIO0GND	1	GND	Low voltage GPIO ground	IP
High voltage GPIOs	GPIO1P0_UIBTN_B	1	GPIO1VDD		IOD
	GPIO1P[7:1]	7	GPIO1VDD		IOD
	GPIO1VDD	1	V3P3A/VSYS	High voltage GPIO supply	IP
	GPIO1GND	1	GND	High voltage GPIO ground	IP
Burst control unit	BCUDISA	1	V1P8A	BCU warning zone A output disable signal	OD
	BCUDISB	1	V1P8A	BCU warning zone B output disable signal	OD
	BCUDISCRIT	1	V1P8A	BCU critical zone output disable signal	OD
PWM	PWM[2:0]	3	PWMVDD	PWM output signals	OD
	PWMVDD	1	V1P8A	PWM supply voltage	IP
	PWMGND	1	GND	PWM ground	IP
Display	BACKLIGHT_EN	1	V3P3A	Backlight enable	OD
	PANEL_EN	1	V3P3A	LCD panel enable	OD
ADC	SYSTHERM[2:0]	3	VLP	System temperature thermistor input	IA
	BPTHERM0	1	VLP	Battery temperature input of pack 0	IA
	BPTHERM1	1	VLP	Battery temperature input of pack 1	IA
	BATID	1	VLP	Battery identification	IA
	VBATSENSE	1	VBAT	battery sense voltage	IA
Test	PMICTEST	1	5V	Test pin	IA

	VBATBKUP	1		Coin Cell backup battery	OP
	VREFB	1	VLP	Battery ID bias voltage	OP
	VREFT	1	VLP	battery thermistor bias voltage	OP
	DEBUG_CS	1	VSYS	Selecting SVID and I2C channel for debugging	I
	DEBUG_SVID_CLK	1	V1P0S	SVID clock from Valleyview 2 debug channel	I
	DEBUG_SVID_DATA	1	V1P0S	SVID data in/out, debug channel	IO
	DEBUG_SVID_ALERT_B	1	V1P0S	SVID interrupt from PMIC debug channel	O
	DEBUG_I2C_CLK	1	V1P8S	I2C clock debug channel	I
	DEBUG_I2C_DATA	1	V1P8A	I2C data debug channel	IO

Table 4: Pin Description

Pin Type	Description	Pin Type	Description
I	Input	D	Digital
O	Output		
P	Power		
A	Analog		

Table 5: Pin Type Definition

9. Operating Conditions

9.1 System Control Signals

9.1.1 VDCIN_SENSE

Input voltage, limited to the maximum input voltage via resistor divider, of the AC/DC adaptor.

9.1.2 ACPRESENT

ACPRESENT is an active high dedicated output signal that indicates the AC/DC adapter or USB DCP/CDP/ACA (CHGDET_B=0) is connected to a valid voltage.

9.1.3 VBUS_SENSE

USB input voltage detection

9.1.4 CHGDET_B

USB DCP detection from USBPHY to DA6021. (0=USB DCP/CDP/ACA)

9.1.5 VSYS1/2

Input power supplies and input voltage supervision

9.1.6 CHGSTAT

Input to DA6021 indicating the battery charger status and fault indicator from charger IC

9.1.7 ILIM[1:0]

Output signals providing information the external connected power sources like AC adaptor, USB DCP/CDP/ACA and USB SDP)

9.1.8 I2C_CLK

I2C clock signal from SoC to DA6021

9.1.9 I2C_DATA

I2C data connection between SoC and DA6021

9.1.10 IRQ

IRQ is an active high dedicated output signal that generates interrupts to the SOC. It is asserted when at least one unmasked interrupt bit is set in the 1st level interrupt register. It is valid when RSMRST_B=1 (de-asserted). The maximum latency from the IRQ detection to the assertion of the IRQ line is 1ms.

9.1.11 I2CM_CLK

I2C clock signal from DA6021 to external I2C EEPROM

9.1.12 I2CM_DATA

I2C data line between DA6021 and external I2C EEPROM

9.1.13 PWRBTNIN_B

System power button input signal, internally connected to VSYS via a 20kΩ resistor and includes a 30ms de-bouncer from proper function avoiding detection during bouncing contacts

9.1.14 PWRBTN_B

DA6021 passes the power button input information via the PWRBTN_B output signal to the SOC. PWRBTN_B is a level shifted copy of PWRBTNIN_B after the 30ms de-bouncer. PWRBTN_B is valid when RSMRST_B=1 (de-asserted).

9.1.15 PLTRST_B

PLTRST_B is an active low dedicated input signal from the SOC that indicates the SOC already comes out of reset upon de-assertion (PLTRST_B=1). Please note that PLTRST_B is not a power state indication signal while SLP_S*_B (i.e. SLP_S0IX_B or SLP_S3_B or SLP_S4_B) signals are. PMIC ignores the PLTRST_B if it is in one of the standby states.

9.1.16 SLP_S0iX_B

SLP_S0IX_B is an active low dedicated input signal from the SOC that indicates SX state entry upon assertion (SLP_S0IX=LOW) and exit upon de-assertion (SLP_S0IX=HIGH). The assertion of the SLP_S0IX_B signal from the SOC launches SOC_SX entry sequence. It is only considered if RSMRST_B=1.

9.1.17 SLP_S3_B

SLP_ S3_B is an active low dedicated input signal from the SOC that indicates S3 state entry upon assertion (SLP_S3_B=LOW) and exit upon de-assertion (SLP_ S3_B=HIGH). The assertion/de-assertion of the SLP_S3_B signal from the SOC launches SOC_S3 state entry/exit sequence. It is valid when RSMRST_B=1 (de-asserted).

9.1.18 SLP_S4_B

SLP_S4_B is an active low dedicated input signal from the SOC that indicates S4 state entry upon assertion (SLP_S4_B=LOW) and exit upon de-assertion (SLP_S4_B=HIGH). The assertion/de-assertion of the SLP_S4_B signal from the SOC launches SOC_S4 state entry/exit sequence. It is valid only when RSMRST_B=1.

9.1.19 RSMRST_B

RSMRST_B is an active low dedicated output signal. RSMRST_B asserts when voltage rail V3P3A is enabled. RSMRST_B shall be actively driven to low in SOC G3 state when SUS rails are turned off. This is down via a pull-down integrated resistor. The nominal voltage of RSMRST_B is 0V when asserted, 3.3V when de-asserted.

9.1.20 DRAMPWROK

DRAMPWROK is an active high dedicated output signal. DRAMPWROK asserts when voltage rail VDDQ is enabled. The nominal voltage of DRAMPWROK is VDDQ when asserted, 0V when de-asserted.

9.1.21 VCCAPWROK

VCCAPWROK is an active high dedicated output signal. VCCAPWROK asserts when all voltage rails that are supposed to be on in SOC_S0 and SOC_SX states are at nominal voltage. The nominal voltage of VCCAPWROK is VDDQ when asserted, 0V when de-asserted. VCCAPWROK will de-assert only if both PLTRST_B and SLP_S0IX_B are asserted (=0) during sleep state entry.

9.1.22 COREPWROK

COREPWROK is an active high dedicated output signal. COREPWROK asserts when all voltage rails that are supposed to be on in SOC_S0 and SOC_SX states, are at nominal voltage. COREPOWROK shall be actively driven to low in SOC G3 state when SUS rails (*_A rails) are turned off. The nominal voltage of COREPWROK is 3.3V when asserted, 0V when de-asserted. COREPWROK will de-assert only if both PLTRST_B and SLP_S0IX_B are asserted (=0) during sleep state entry.

9.1.23 SUSPWRDNOK

SUSPWRDNACK is an active high dedicated input signal from the SOC that indicates the PMIC to turn off the SUS rails (A) rails (V3P3A, V1P8A, V1P0A) in junction with assertion of SLP_S4_B. It is valid when RSMRST_B=1 (de-asserted) and SLP=S4_B=0 (asserted).

9.1.24 BATLOW_B

BATLOW_B is an active low dedicated output signal to the SOC indicating that the battery voltage is not sufficiently high to boot the SoC.

9.1.25 SUSCLK

SUSCLK is the 32.768kHz RTC clock that is supplied from the SoC. It is available to DA6021 about 100ms after RSMRST_B is de-asserted and continue to be available in S0, S0iX, S3 and S4 state. It is not available if the platform will be in G3 mode when the suspend voltage rails are disable.

9.1.26 THERMTRIP_B

THERMTRIP_B is an active low dedicated input signal that notifies the PMIC of a SOC thermal event. It is valid when RSMRST_B=1 and PLTRST_B=1 (de-asserted). Upon sensing the THERMTRIP_B signal has transitioned low, the PMIC shuts down all rails immediately (hard shutdown, not waiting for SLP_S*_B signals from the SOC to execute a Cold Off power down sequence). To avoid spurious detection during power sequencing, the THERMTRIP_B signal is only sampled if PLTRST_B is de-asserted. THERMTRIP has internal pull-up.

9.1.27 PROCHOT_B

PROCHOT_B is an active low dedicated output signal used to notify the SOC of a PMIC, battery or system thermal event. PROCHOT_B will be asserted when the PMIC temperature, battery temperature or system temperature has crossed the alert thresholds define in the thermal monitoring section. It will also assert when battery voltage drops to the threshold set in SVTM. PROCHOT_B is asserted if the PMIC die temperature rises above the internally set alert threshold, for example 110°C, to prevent the PMIC from reaching critical temperature. It is valid when RSMRST_B=1 and PLTRST_B=1 (de-asserted). The SOC will go into a lower power state until the PMIC thermal event is cleared and the pin is de-asserted. PROCHOT_B has internal pull-up.

9.1.28 SDMMC3_1P8_EN

SDMMC3_1P8_EN is a dedicated input signal from the SOC to select 1.8V or 3.3V for SD card.

- SDMMC3_1P8_EN=1 to select 1.8V for SD card.
- SDMMC3_1P8_EN=0 to select 3.3V for SD card.

It is valid when RSMRST_B=1 (de-asserted) and COREPWROK=1 (asserted).

9.1.29 SDMMC3_PWR_EN_B

SDMM3_PWR_EN_B is an active low dedicated output signal to enable SD card power. It is valid when RSMRST_B=1 (de-asserted) and COREPWROK=1 (asserted).

9.1.30 MODEM_OFF_B

9.1.31 SDWN_B

The SDWN_B (Shut-Down Warning) signal is sent by the PMIC to the modem as a warning that a system shutdown event is about to take place.

The SDWN_B signal is asserted (set low) during power down Task Lists. If the PMIC enters a catastrophic shutdown condition which would normally bypass a Cold Off Task List being run, the SDWN_B pin must be asserted a minimum of 900us prior to this catastrophic shutdown commencing. The nominal voltage of SDWN_B is 0V when asserted, 1.8V when de-asserted.

9.1.32 USBRST_B

USBRST_B is an active low dedicated output signal to reset the USB PHY. The minimum pulse is 100µs when asserted. The nominal voltage of USBRST_B is 0V when asserted, 1.8V when de-asserted.

9.1.33 GPIOs

9.1.33.1 Low Voltage GPIOs

GPIO0P1_BATIDIN:

Battery ID input signal from SOC for digital battery communication. Optional function multiplexed with low voltage GPIO0P1

GPIO0P2_BATIDOUT:

Battery ID output to SoC for digital battery communication. Optional function multiplexed with low voltage GPIO0P2

GPIO0P[7:3]:

Low voltage GPIOs with no alternate functions

9.1.33.2 High Voltage GPIOs

GPIO1P0_UIBTN_B:

The UIBTN_B pin is an input from a platform-defined functional interface button, such as the Home button. It includes a 30ms de-bouncer to ensure that spurious transitions aren‘t logged while the switch contacts bounce on initial contact. The output of the de-bouncer enters the edge detect circuits.

GPIO1P[7:1]:

High voltage GPIOs with no alternate functions

9.1.34 Burst Control Unit

9.1.34.1 BCUDISA

Burst controller unit warning zone A. Output signal to disable peripherals (functions)

9.1.34.2 BCUDISB

Burst controller unit warning zone B. output signal to disable peripherals (functions)

9.1.34.3 BCUDISCRIT

Burst controller unit critical zone. Output signal to disable peripherals (functions)

9.1.35 PWM[2:0]

Pulse width modulated output control signals

9.1.36 DISPLAY

9.1.36.1 BACKLIGHT_EN

Output signal to control the display backlight

9.1.36.2 PANEL_EN

Output signal to enable the display

9.1.37 ADC

9.1.37.1 SYSTHERM[2:0]

System temperature thermistor input signal to be multiplexed to DA6021 ADC

9.1.37.2 BPTHERM[1:0]

Battery pack temperature input signal to be multiplexed to DA6021 ADC

9.1.37.3 BATID

Battery identification from the battery for battery presence detection and battery size indication

9.1.37.4 VBATSENSE

Battery voltage sense input

9.2 DA6021 Power States

Following is a brief description of these states:

- **OFF**: No power at all. The platform coin cell has no valid power.
- **COIN**: COIN domain is powered and not under reset. Coin domain refers to a small logic portion inside DA6021, which gets a reset signal and supply from the coin cell or a supercap. These logic registers retain data when DA6021 supply fails or PMIC goes under the POR. These register are sitting on the analog side. The COIN state is not related to any operation in the PMIC and is not coded. It represents just a possible supply scenario.
- **RESET**: The digital core which is not supplied from the COIN is under POR due to the fact that the VSYS input has not crossed yet the POR release threshold.
- **OTP**: Just after POR is released DA6021 goes into OTP state and reads the OTP. In this state all the trimming, calibration, power sequencing, and platform variant data is read and copied into the operational registers. This state is crossed only during first power up or when DA6021 is forced by POR or soft reset to go back into RESET state.
- **EEPROM**: For debugging purpose or as a fallback solution in the field it's possible to overwrite the operational registers via an external EEPROM. This step is always performed from DA6021 after the OTP state and is done once during first power up if the EEPROM contains. It is assumed that the EEPROM is supplied at the time of the access.
- **G3**: This state corresponds to a non-valid system supply VSYS (VSYS < VSYSREF = 3.0V). VSYS is not considered to be good enough for booting.
- **SOC_G3**: This is by definition the "*system power down*" state. Application will be mainly looping between active state and this state. VSYS valid event makes the PMIC going from G3 to SOC_G3 state. Critical events and power button can lead the PMIC to this state. Only in this state it is possible to be sensitive to the external wakeup events.

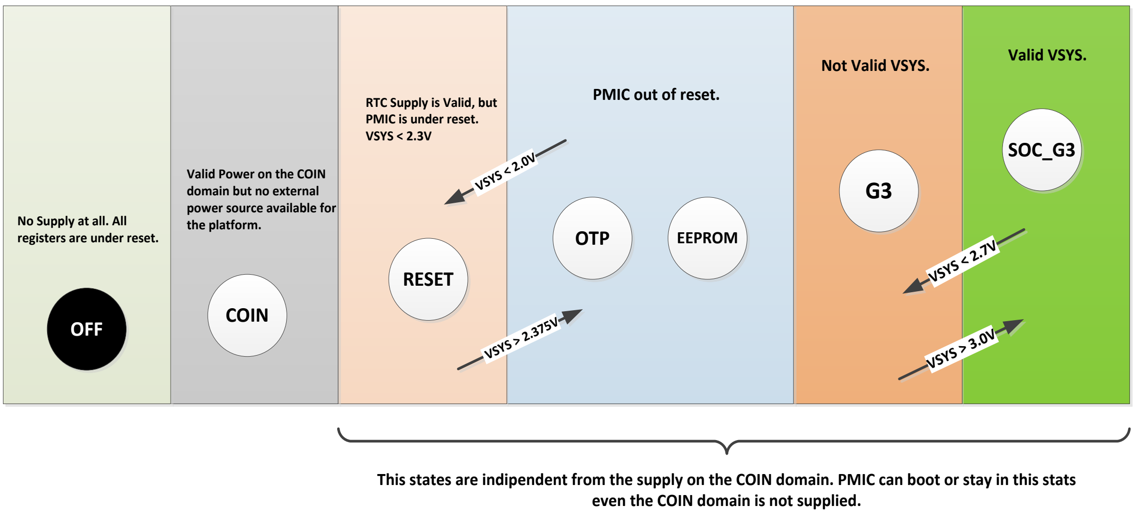


Figure 4: DA6021 Power States

DA6021 will issue an under voltage flag when VSYS will fall below the 2.7V threshold. In this case a shutdown will be executed bringing down all rails in an ordered fashion. The final state will be G3. The following figure shows different thresholds which generate events in DA6021.

When VSYS reaches the 2.0 Volt (point B) the POR will happen and DA6021 will go to reset. All the registers will be initialized with default values. Only registers supplied from RTC will retain their value. POR will be released once the VSYS increases and reaches the 2.375V, point C. In this case the digital core will no longer be in a reset condition and can read the OTP content.

In this case the device again in G3 is waiting for the VSYS to become valid, VSYS > VSYSREF = 3.0. DA6021 will go then to SOC_G3 state waiting for wakeup condition to be met. In order to have valid VSYS de-bouncing of 100ms will be needed. The monitor of the system voltage will be done via ADC once the system is in SOC_S0 state or active state.

VSYS voltage and events generated:

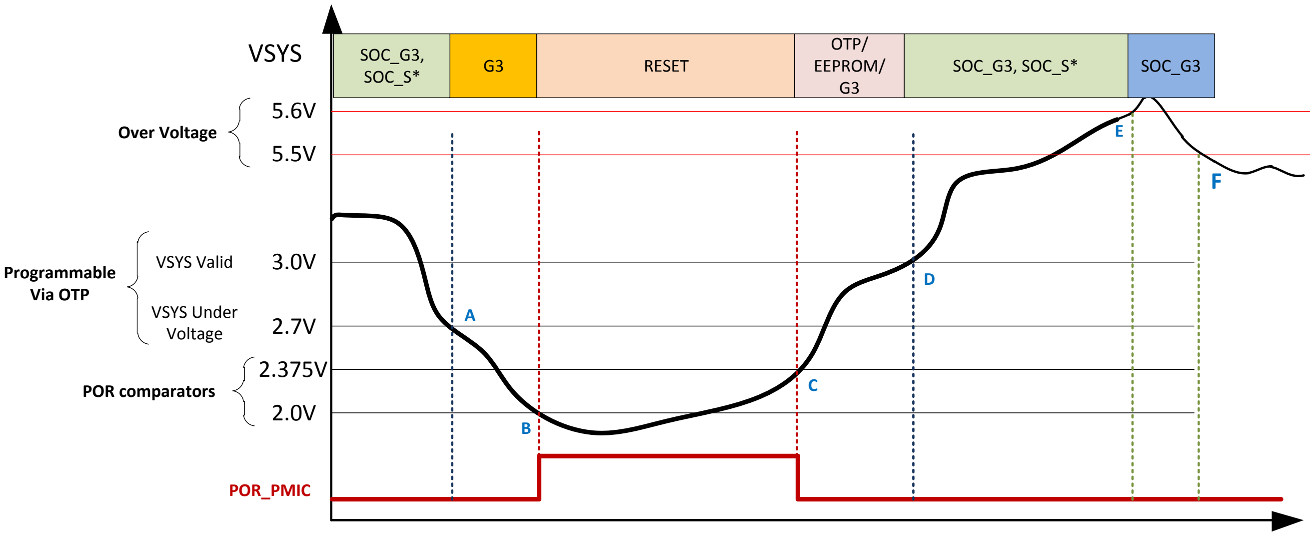


Figure 5: VSYS Areas

Event Trigger	Conditions (all mandatory)	Next state	Note
Main Battery Insertion	VSYS > VMIN	SOC_G3	VLP ramps when VSYS input power becomes sufficient high I2C Register map is reset to default settings
Main Battery becomes valid			
USV or AC/DC Adapter Insertion			

Table 6 : G3 State Transition

Event Trigger	Conditions (all mandatory)	Next state	Note
Input power Source removal and Main Battery Removal/Depletion	VSYS < VMIN VBATBKUP>VMIN	G3	DA6021 loses states, except RTC powered registers Restart with default values except RTC powered registers
	VSYS < VMIN VBATBKUP<VMIN		DA6021 loses states, RTC powered registers loses states Re-start with default values
See event and conditions in Cold Boot Triggers		SOC_S4	DA6021 transitions to SOC_S4 to start cold boot sequence based on SOC handshake

Table 7: SOC_G3 State Transition

9.3 SoC Power States

The following diagram depicts the DA6021 power states, related to the SoC and the platform rails.

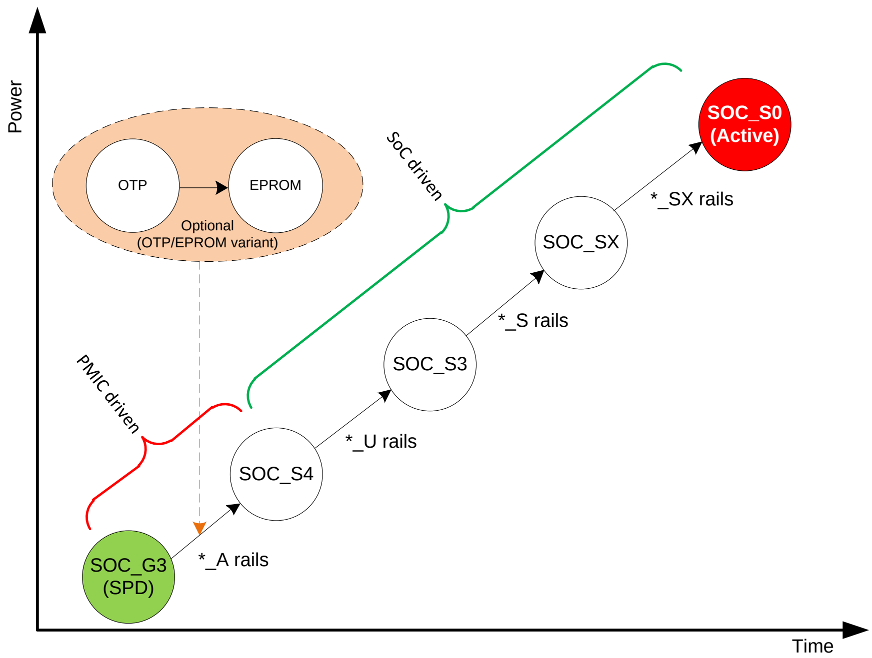


Figure 6: SoC Power States

State description:

- **SOC_S4**: or hibernate. This is the most power saving from all the standby states. Content is saved onto disk. DA6021 runs only with low frequency oscillator. All *_A power rails are active and in low power pulse skipping mode
- **SOC_S3**: or standby: Content is saved in the RAM. It requires more power than SOC_S4, although still considered a low power state. DA6021 has a low power oscillator and in addition all *_U power rails are switched on, running in pulse skipping mode. Temperature monitoring is in-active as power consumption is low and no temperature event is expected. Furthermore the ADC is still disabled, reducing the idle power.
- **SOC_SX**: a power saving active standby mode with very fast recovery time. High frequency oscillator is active as well as all *_S power domains. Temperature supervision is active, but ADC runs on reduced speed.
- **SOC_S0**: This represents the active state for the SoC where most of the rails are on. SoC executes the code and software plus operating system decide on power up/down of the “on-demand” power rails.

Generally the OTP and optionally the external EEPROM are read out only once during first power-up. However, it will be possible via OTP/software to configure the sequencer to go again through the OTP and/or EEPROM between some of the standby states as indicated in the figure above.

9.3.1 SOC_S0 State

In the “SOC S0 State”, DA6021 completed the bring-up of the platform, and released the SOC from reset. In this state, the DA6021 state machines may be modified and controlled by the SOC, through commands issued over the I2C and SVID interfaces.
In this state, the tablet will appear “on” to the user.

The events causing a transition out of the ‘SOC S0’ state are shown in the table below.

Event Trigger	Conditions (all mandatory)	Next state	Note
Input power Source removal and Main Battery Removal/Depletion	VSYS < VMIN VBATBKUP>VMIN	G3	DA6021 loses states, except RTC powered registers Restart with default values except RTC powered registers
	VSYS < VMIN VBATBKUP<VMIN		DA6021 loses states, RTC powered registers loses states Re-start with default values
See event and conditions in Cold off Triggers		SOC_G3	See "Cold Off Triggers"
Power Button Held	Power Button held time < PBCONFIG .FCOT[3:0]	S0iX	DA6021 passes PWRBTN_B information to SoC. SoC toggles SLP_S0iX_B = 0 to enter S0iX
Warm Reset	PLTRST_B=0	SOC_S0	Resets I2C and SVID
SLP_S0iX_B	SLP_S0iX_B=0 Or SLP_S3_B=0 Or SLP_S$_B =0	SOC_S0iX	Enter S0iX state

Table 8:SOC S0 State Transition

9.3.2 SOC S0iX State

The SOC supports three possible standby states: S0IX, S3, and S4. Each of these states represents a different level of SOC standby, with S0IX being the "shallowest" (highest power) and S4 being the "deepest" (lowest power). Each of these three sub-states has its own entry task list, required because of the different states of power rails in each.
The entering and exiting of the SOC S0IX state is controlled by a signal which is delivered to DA6021 by the SOC via a dedicated physical pin SLP_S0IX_B.

- Rails that are on:
  - They are shown in the power sequencing diagrams
  - VRs shall be placed in PFM/power save mode
  - Internal PMIC rails
- Interfaces available:
  - SVID is ON in S0IX
  - I2C is ON in S0IX
- Input source comparators and interrupts active.
- All registers powered, with states retained.
- Thermal monitoring and VR current measurements are disabled by default. If enabled, the measurements are taken at standby frequency.

The events causing a transition out of the 'SOC S0IX' state are shown in the table below.

Event Trigger	Conditions (all mandatory)	Next state	Note
Input power Source removal and Main Battery Removal/Depletion	VSYS < VMIN VBATBKUP>VMIN	G3	DA6021 loses states, except RTC powered registers Restart with default values except RTC powered registers
	VSYS < VMIN VBATBKUP<VMIN		DA6021 loses states, RTC powered registers loses states Re-start with default values
See event and conditions in Cold off Triggers		SOC_G3	See "Cold Off Triggers"
Power Button Held	Power Button held time < PBCONFIG	S0iX	DA6021 passes PWRBTN_B information to SoC. SoC

	.FCOT[3:0]		toggles SLP_S0iX_B = 1 to exit S0iX
SLP_S0iX_B	SLP_S0iX_B=1 SLP_S3_B=1 SLP_S4_B =1	SOC_S0	Exit S0iX state
SLP_S3_B	SLP_S3_B=0 Or SLP_S4_B=0	SOC_S3	Enter S3 state

Table 9: SOC S0iX State Transition

9.3.3 SOC S3 State

The entering and exiting of each the SOC S3 state is controlled by a signal which is delivered to DA6021by the SOC via a dedicated physical pin SLP_S3_B. The exiting of SLP_S3_B is also gated by BATLOW_B.

- Rails that are on:
  - They are shown in the power sequencing diagrams
  - VRs shall be placed in PFM/power save mode
  - Internal PMIC rails
- Interfaces available:
  - SVID is OFF in S3
  - I2C is OFF in S3
- Input source comparators and interrupts active.
- All registers powered, with states retained.
- Thermal monitoring and VR current measurements are disabled by default. If enabled, the measurements are taken at standby frequency.

The events causing a transition out of the ‘SOC S3’ state are shown in the table below.

Event Trigger	Conditions (all mandatory)	Next state	Note
Input power Source removal and Main Battery Removal/Depletion	VSYS < VMIN VBATBKUP>VMIN	G3	DA6021 loses states, except RTC powered registers Restart with default values except RTC powered registers
	VSYS < VMIN VBATBKUP<VMIN		DA6021 loses states, RTC powered registers loses states Re-start with default values
See event and conditions in Cold off Triggers		SOC_G3	See “Cold Off Triggers”
Power Button Held	Power Button held time < PBCONFIG .FCOT[3:0]	S0iX	DA6021 passes PWRBTN_B information to SoC. SoC toggles first SLP_S3_B=1 to exit S3 state followed by SLP_S0iX_B = 1 to exit S0iX
SLP_S3_B	SLP_S3_B=1 SLP_S4_B =1 BATLOW_B=1	SOC_S0iX	Exit S3 state
SLP_S4_B	SLP_S4_B=0	SOC_S4	Enter S4

Table 10: SOC S3 State Transition

9.3.4 SOC S4 State

The entering and exiting of each the SOC S4 state is controlled by a signal which is delivered to the PMIC by the SOC via a dedicated physical pin SLP_S4_B. The exiting of SLP_S4_B is also gated by BATLOW_B.

- Rails that are on:
  - They are shown in the power sequencing diagrams
  - VRs shall be placed in PFM/power save mode
  - Internal PMIC rails
- Interfaces available:
  - SVID is OFF in S4
  - I2C is OFF in S4
- Input source comparators and interrupts active.
- All registers powered, with states retained.
- Thermal monitoring and VR current measurements are disabled by default. If enabled, the measurements are taken at standby frequency.

The events causing a transition out of the ‘SOC S4’ state are shown in the table below.

Event Trigger	Conditions (all mandatory)	Next state	Note
Input power Source removal and Main Battery Removal/Depletion	VSYS < VMIN VBATBKUP>VMIN	G3	DA6021 loses states, except RTC powered registers Restart with default values except RTC powered registers
	VSYS < VMIN VBATBKUP<VMIN		DA6021 loses states, RTC powered registers loses states Re-start with default values
See event and conditions in Cold off Triggers		SOC_G3	See “Cold Off Triggers”
Power Button Held	Power Button held time < PBCONFIG .FCOT[3:0] If exit S4 to SOC_S3, BATLOW_B=1	SOC_S3	DA6021 passes PWRBTN_B information to SoC. SoC toggles first SLP_S4_B=1 to exit S4 state, then SLP_S3_B=1 to exit S3 state followed by SLP_S0iX_B = 1 to exit S0iX
SLP_S3_B	SLP_S4_B =1 BATLOW_B=1	SOC_S3	Exit S4 state
SLP_S4_B	SLP_S4_B=0 SUSPWRDNACK=1 SUSPWRDNACKCFG=1	SOC_G3	SOC can toggle SUSPWRDNACK to 1 when SLP_S4_B=0 to enter SOC_G3 state

Table 11: SOC S4 State Transition

9.3.5 Truth Table of Sleep Signals and DA6021 Final Power States

SUSPWDNACK	SUSPWRDNACKCFG	SLP_S4_B	SLP_S3_B	SLP_S0iX_B	Final Power State	Comment
1	1	0	x	x	SOC_G3	Note 5
0	X	0	X	X	SOC_S4	Note 5
X	0	0	X	X	SOC_S4	Note 5
X	X	1	0	X	SOC_S3	Note 6
X	X	1	1	0	SOC_S0iX	Note 7
X	X	1	1	1	SOC_S0	Note 7

Table 12: Truth Table of Sleep Signals and DA6021 Final Power States

Notes:

1. X don't care
2. RSMRST_B=1 for any sleep signal assertion to be valid
3. The normal (except catastrophic or critical events) power state transition sequence is: SOC G3->SOC S4->SOC S3->SOC S0IX->SOC S0 based on the conditions or in reverse order. Power state transition is from one state to the next state based on sleep signals from the SOC without skipping states. For example, if the PMIC is currently in SOC S0 state, sleep signals SLP_S0IX, SLP_S3_B, SLP_S4_B are all asserted. The PMIC will not jump directly to SOC S4 without first going to SOC S0IX then to SOC S3.
4. 4. To exit from SOC S3 and SOC S4, BATLOW_B=1.
5. 5. Normally SLP_S0IX_B =0, SLP_S3_B=0 when SLP_S4_B=0.
6. 6. Normally SLP_S0IX_B =0 when SLP_S3_B=0. SUSPWRDNACK=1 in this power state.
7. 7. Normally SUSPWRDNACK=1 in this power state.

9.3.6 DA6021 Power State Transitions and Sleep Signals

The table below summarizes how DA6021 transitions from one power state to the next based on sleep signals and SUCPWRDNACK.

SUSPWDNACK	SUSPWRDNACKCFG	SLP_S4_B	SLP_S3_B	SLP_S0iX_B	Present State	Next State
1	1	0	X	X	SOC_S4	SOC_G3
0	X	0	X	X	SOC_S4	SOC_S4
X	0	0	X	X	SOC_S4	SOC_S4
X	X	1	X	X	SOC_S4	SOC_S3
X	X	0	0	X	SOC_S3	SOC_S4
X	X	1	0	X	SOC_S3	SOC_S3
X	X	1	1	X	SOC_S3	SOC_S0iX
X	X	1	1	0	SOC_S0iX	SOC_S0iX
X	X	1	1	1	SOC_S0iX	SOC_S0
X	X	1	0	X	SOC_S0iX	SOC_S3
X	X	X	X	0	SOC_S0	SOC_S0iX

Table 13: DA6021 State Transition and Sleep Signals

9.4 Register File and Address Range

There are 5 register blocks, one for VNN, one for VCC, one for test purpose, one for Intel and another block controlling the power sequence. These blocks can either be accessed via the SVID or I2C interface, via OTP or the external EEPROM, see picture blow.

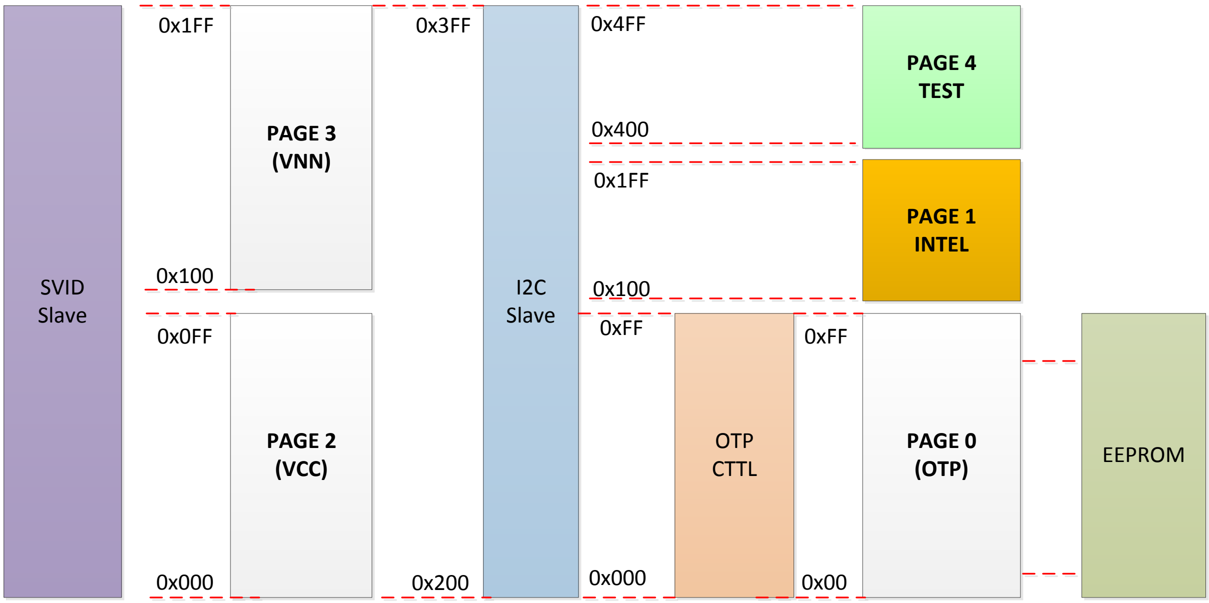


Figure 7: Address Range and Pages

The power sequence is located in the page 0 of the register map and shall not be modified by customer. It is highly recommended not to modify any register in page 0 as this may damage the system. Please contact Dialog Semiconductor if you need changes in the sequencing. Such updates can be made in 2 ways, via new OTP, This would mean producing a new DA6021 variant, or via an external EEPROM.

Page 1 includes all the registers to control the ADC functions, GPIO's, PWM controller, controllable voltage domains and further functions described in the document below.

Page 2 and 3 include the SVID functions for the core and the graphics regulators.

Page 4 is an internal register block for DA6021 internal test functions.

9.4.1 Slave ID versus DA6021 Pages

Each page can be accessed via the I2C interface while using a certain slave ID to address the corresponding I2C slave. The table below shows the relation between slave ID and page to be accessed:

PAGE Accessed	SLAVE_ID	Read Address	Write Address
Page 1	0x6E	0xDD	0xDC
Page 2 – SVID	0x5C	0xB9	0xB8
Page 3 – SVID	0x6C	0xD9	0xD8

Table 14: Slave ID versus DA6021 Storage Page

10. Power Controller State Machine

10.1 Overview

The power controller state machine is the main state machine of DA6021. It is comprises a first phase related to the power up sequence where all the condition for a safe boot are evaluated and the parameter are taken from the OTP/EEPROM, and a second phase related to the SoC power sequence where all the power rails for the SoC and platform are turned on according to certain sequencing rules.

The sequencer is very flexible in terms of components ordering and the intermediate delays between them. Optionally the sequencer can wait for a certain condition, for example a breakpoint, an external programmed trigger or waiting in a system power state like SOC_S4. In case of power-up direction, the components will be enabled. In the power-down direction the components will be disabled.

The sequence configuration is stored in the OTP memory the contents of which are read out during the first power up cycle. The sequencer also controls the clock request of different blocks. Refer to the Introduction section on the power states for an overview on power up states and SoC sequencer states.

10.2 Power State Transitions

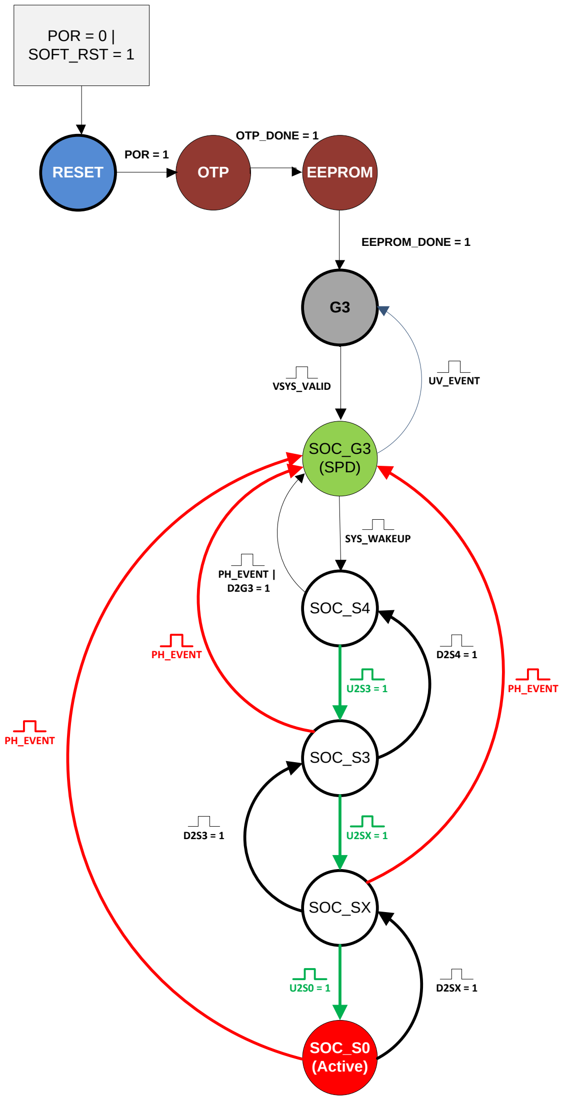


Figure 8: State Transitions

The figure above represents DA6021 power state transitions. There are several events and condition for these transitions to occur. Following is the list of conditions used in the figure.

- ***PH_EVENT***: this is a catastrophic event. At any time the system does an immediate shutdown 90µs after the shutdown warning and goes directly to the SOC_G3 state.
- ***CT_EVENT***: these are all critical events. DA6021 will shut down via power down sequencing which is driven from the PMIC, regardless of the SoC handshake.
- ***U2S****: Indicates a move to the next SOC_S* state. The direction is upwards. The reason can be that one of the SLP_S*_B signals have changed or PWRBTN has been pressed.
- ***D2S****: Indicates a move to the next SOC_S* state. The direction I downwards. Reason can be a change on one of the SLP_S*_B signals.
- ***D2G3***: Can be asserted if DA6021 is sensitive to SUSPWRDNACK input and SUSPWRDNACK = 1.
- ***SYS_WAKEUP***: represents a valid wakeup event from system power down. This event is generated from the sysco block.
- ***UV_EVENT***: represents an under voltage event in DA6021. Under voltage event belongs to the critical event but the final state will be G3, instead of SOC_G3.
- ***VSYS_VALID***: this means that VSYS has crossed the 3.0V and can proceed to SOC_G3 and wait for boot condition

Refer to the table below for U2 and D2 specific conditions.

Condition			ST	NX_ST	Events					
SLP_S4_B	SLP_S3_B	SLP_SX_B			U2S3	U2SX	U2S0	D2SX	D2S3	D2S4
0	X	X	SOC_S4	SOC_S4	0	0	0	0	0	0
1	X	X	SOC_S4	SOC_S3	1	0	0	0	0	0
0	X	X	SOC_S3	SOC_S4	0	0	0	0	0	1
1	0	X	SOC_S3	SOC_S3	0	0	0	0	0	0
1	1	X	SOC_S3	SOC_SX	0	1	0	0	0	0
1	1	0	SOC_SX	SOC_SX	0	0	0	0	0	0
1	1	1	SOC_SX	SOC_S0	0	0	1	0	0	0
X	0	X	SOC_SX	SOC_S3	0	0	0	0	1	0
0	X	X	SOC_SX	SOC_S3	0	0	0	0	1	0
X	X	0	SOC_S0	SOC_SX	0	0	0	1	0	0
1	1	1	SOC_S0	SOC_S0	0	0	0	0	0	0
X	0	X	SOC_S0	SOC_SX	0	0	0	1	0	0
0	X	X	SOC_S0	SOC_SX	0	0	0	1	0	0

Table 15:U2 & D2 Event Generation Table

A soft reset can be generated in application and via configuration in SOC_SX and SOC_S0 states. In other modes it can be generated even in other states where the I2C slave is available.

10.2.1 Sequencing

Each PMIC component (such as a DC/DC converter, LDO, internal or external power switch …) can be placed with high flexibility into the power sequence, whereas enabling and disabling such a component during power-up and power-down can be programmed independently.

The sequencing is defined by Intel processor specification, implemented and evaluated accordingly. Customers requesting power sequencing other than specified, please contact Dialog Semiconductor.

10.3 DA6021 Power Sequences

There are 10 power state transitions to be performed in DA6021. These are:

- **Cold Boot**: A cold boot sequence begins at the “SOC G3” state, and terminates at the “SOC S0” state. Once all of the rails are on, the COREPWROK signal will assert and the PLTRST_B will de-assert. This will effectively turn on the SOC in order for it to begin executing code and controlling the system.
- **Warm Reset**: A Warm Reset resets the SOC as well as the I2C and SVID interfaces (reset corresponding state machine, ignore any on-going transaction on the bus) in the PMIC. In addition the VCC, VNN will change the output voltage to the VBOOT settings. PMIC configuration registers are not reset to default. During a Warm Reset, only the PLTRST_B pin to the SOC is toggled. All rails remain in regulation. Warm reset can only be issued while the SoC stays in SOC_S0 state.
- **Enter SOC S0iX**: The S0IX state is entered when the SOC is in a shallow sleep state. This state is entered when the SOC asserts the SLP_S0IX_B (LOW) pin to the PMIC. VDDQ_VTT and SX rails are turned off. The VCC rail is turned off by SVID commands (not by SLP_S0IX_B signal). The rest of the VRs remain on but enter into power save mode.
- **Exit SOCS0iX**: The S0IX state is exited when the SOC de-asserts the SLP_S0IX_B pin (HIGH). VDDQ_VTT and SX rails are turned on. The VCC rail will be turned on by SVID commands (not by SLP_S0IX). The rest of the rails will come out of power save mode. Exiting the SOC_SX state will be performed within maximum 200µs.
- **Enter SOC_S3**: The S3 state is entered when the SOC asserts the SLP_S3_B pin (LOW). VRs that remain on enter into power save mode.
- **Exit SOC_S3**: The S3 state is exited when the SOC de-asserts the SLP_S3_B pin (HIGH). Voltage rails will be turned on and come out of power save mode. Exiting SOC_S3 state will be performed within 2ms maximum.
- **Enter SOC_S4**: The S4 state is entered when the SOC asserts the SLP_S4_B pin (LOW). VRs that remain on enter into power save mode.
- **Exit SOC_S4**: The S4 state is exited when the SOC de-asserts the SLP_S4_B pin (HIGH). Voltage rails will be turned on and come out of power save mode.
- **Cold OFF**: PMIC will go into SOC_G3 and stay until a wakeup event is not bringing it back to active state.
- **Modem Reset**: A Modem Reset task is initiated by setting the MODEMRSTSEQ bit in the MODEMCTRL register. (The MODEMOFF bit in the same register directly controls the status of the MODEM_OFF_B output pin, but does not launch this task). The Modem Reset task toggles the SDWN and MODEM_OFF_B pins, implementing appropriate (modem-specific) delay timings.

Several of these state transitions are triggered by hardware events, such as a power button event, or power source insertion. The transitions are gated by SOC signals such as, SLP_S0IX, SLP_S3_B, SLP_S4_B and SUSPWRDNACK.

The behaviours associated with each of these state transitions are stored in the PMIC’s power sequencing state machine.

The sections below describe the trigger sources of each transition and the default sequencing behaviour.

The voltage rails are classified in the following categories which will be referred to in such a way to simplify the power state transition (power sequencing) diagrams:

- **SUS rails** (A rails): V1P0A, V1P8A, V1P2A and V3P3A. They together with VUSBPHY remain on in “SOC S4” state. They are turned off in “SOC G3” state.
- **U rails**: V1P8U, together with VDDQ, VREFDQ0/1 remains on in “SOC S3” state. They are turned off in “SOC S4” state.

- **S rails**: V5P0S, VNN, V1P05S, V1P0S, V1P8S, V1P2S, V3P3S and V2P85S. They remain on in "SOC S0IX" state. They are turned off in "SOC S3" state.
- **SX rails**: VDDQ_VTT, V1P0SX and V1P2SX. They are on in "SOC S0" state. They are turned off in "SOC S0IX" state.
- **Default On rails**: VRs that are powered on during COLD BOOT by the power sequencing state machine.
- **Defaults Off rails**: VRs that are not powered on during COLD BOOT by the power sequencing state machine. They are managed by the SOC. Their on/off status depends on a platform device or other conditions.

10.3.1 Cold Boot

A cold boot sequence is followed whenever DA6021 is fully turning on the system from a powered-down state. As such, a cold boot sequence begins at the "SOC G3" state, and terminates at the "SOC S0" state. Once all of the rails are on, the COREPWROK signal will assert and the PLTRST_B will de-assert. This will effectively turn on the SOC in order for it to begin executing code and controlling the system.

During this state transition, one or more of the sleep signals (SLP_S*_B) could be asserted at some point of time. The VRs, LDOs, internal and external switches are turned on in the requested power sequence order into normal operational.

Furthermore, the rails are turned on one at a time in a ramp-rate controlled manner (voltage slew rate limited) in order to avoid battery inrush current situations that could cause shut down events.

All the triggers listed in the table below will cause DA6021 bringing up the SUS rails. After that, signals from the SOC (SLP_S4_B, SLP_S3_B) are needed for DA6021 completing the cold boot sequence. Battery insertion is used as an illustration of Cold Boot power sequence due to one of triggers.

Event	Conditions (all mandatory)
USB VBUS Inserted (SVBUSDET)	• USBWAKEEN is set • VSYS valid (after VBUS debounce satisfied) • VBUS valid (after VBUS debounce satisfied) • VBAT valid (SBATDET=1 and BATLOW_B=1)
AC/DC Adapter Inserted (SVDCINDET)	• ADPWAKEEN is set • VSYS valid (after adapter debounce satisfied) • VDCIN valid (after adapter debounce satisfied) • VBAT valid (SBATDET=1 and BATLOW_B=1 if BATRMPDEN set, or BATLOW_B=1 if BATRMPDEN cleared).
Main Battery Inserted (SBATDET:0→1)	• BATWAKEEN is set • VSYS valid (after battery detection debounce) • VBAT valid (after battery detection debounce, BATLOW_B=1)

Event	Conditions (all mandatory)
Main Battery becomes Valid with Input Power Source (VBAT rising, VBAT > LOWBAT)	• ADPWAKEEN or USBWAKEEN is set • VSYS valid. • Battery already present (SBATDET=1, not an insertion event) • AC/DC Adapter (SVDCINDET=1 when DCBOOT=0) or USB already inserted (SVBUSDET =1) – BATLOW_B was initially “0” when external power was plugged then becomes “1” after battery has been charged up, prevents case where battery voltage may float up due to cell “relaxing” during SOC G3.
Power Button Pressed	• VSYS valid • VBAT valid (SBATDET=1 and BATLOW_B=1 if BATRMPDEN set, or BATLOW_B=1 if BATRMPDEN cleared)

Table 16: Cold Boot Triggers

Following table provides further clarification for a cold boot trigger

Event	Cold Boot Conditions (all conditions mandatory)				
	Power Source Insertion	Power Button Press	Wake-up Enable Bit	VSYS	VBAT
USB VBUS Inserted	SVBUSDET : 0→1	Not applicable	USBWAKE EN=1	≥ VSYSREF	SBATDET = 1 and BATLOW_B = 1
AC/DC Adapter Inserted	SVDCINDE T: 0→1	Not applicable	ADPWAKE EN=1	≥ VSYSREF	SBATDET = 1 and BATLOW_B = 1 if BATRMPDEN = 1
					BATLOW_B=1 if BATRMPDEN = 0
Main Battery Inserted	SBATDET: 0→1	Not applicable	BATWAKE EN= 1	≥ VSYSREF	BATLOW_B = 1
Main Battery becomes Valid with Input Power Source (VBAT rising, VBAT > LOWBAT)	SVBUSDET =1	Not applicable	USBWAKE E=1	≥ VSYSREF	BATLOW_B: 0→1
	SVDCINDE T=1 and DCBOOT= 0	Not applicable	ADPWAKE EN=1	≥ VSYSREF	BATLOW_B: 0→1
Power Button Pressed	Not applicable	PBLVL = 0	Not applicable	≥ VSYSREF	SBATDET = 1 and BATLOW_B = 1 if BATRMPDEN = 1
					BATLOW_B = 1 if BATRMPDEN = 0 (when battery is removed but AC/DC adapter is present)

Table 17: Truth Table of Cold Boot Triggers

All the conditions in the table above shall be met for Cold Boot (wakeup) to occur. For example, wakeup with AC/DC adapter insertion but without a battery can only occur when all these conditions are met: SVDCINDET=1 (AC/DC adapter insertion), ADPWAKEEN=1, BATLOW_B=1 (which means DCBOOT=1), BATRMPDEN=0. Without a battery, USB power source insertion cannot cause the system to boot.

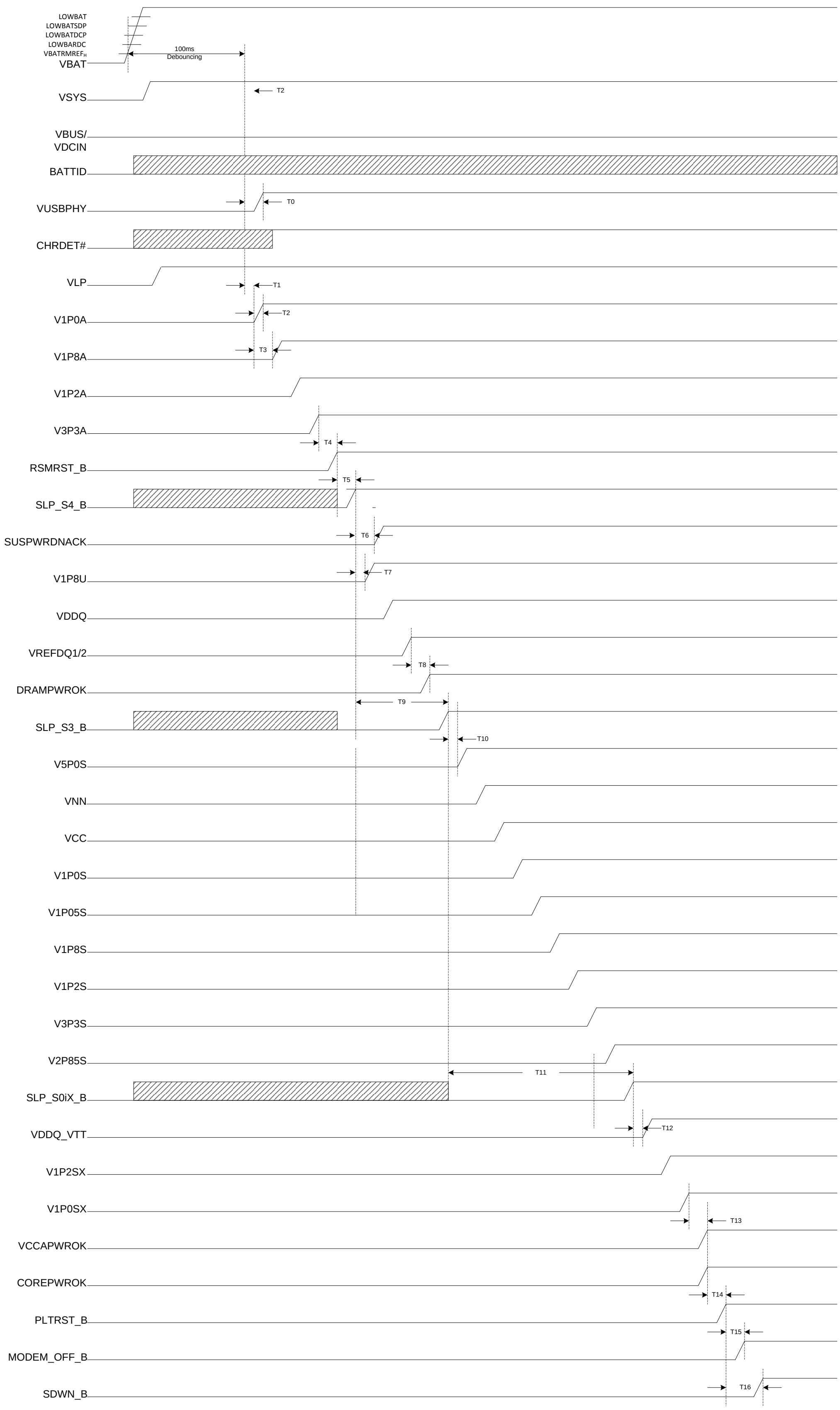


Figure 9: Cold Boot Power Sequencing Diagram, Valid Battery Insertion

Parameter	Description	Min [ms]	Typ [ms]	Max [ms]	Measured [ms]
T0	VUSBPHY Turn on Delay + Ramp-Up Time	0,08		2,00	
T1	not measureable				----
T2_VUSBPHY	Ramp-Up time from 10% to 90% voltage	0,08	1,00	2,00	0,112
T2_V1P0A	Ramp-Up time from 10% to 90% voltage	0,08	1,00	2,00	0,357
T3_V1P0A-V1P8A	Rail to Subsequent Rail Turn-On Delay	0,50	1,00	2,05	0,767
T2_V1P8A	Ramp-Up time from 10% to 90% voltage	0,08	1,00	2,00	0,672
T3_V1P8A-V1P2A	Rail to Subsequent Rail Turn-On Delay	0,50	1,00	2,05	0,869
T2_V1P2A	Ramp-Up time from 10% to 90% voltage	0,08	1,00	2,00	0,051
T3_V1P2A-V3P3A	Rail to Subsequent Rail Turn-On Delay	0,50	1,00	2,05	0,687
T2_V3P3A	Ramp-Up time from 10% to 90% voltage	0,08	1,00	2,00	0,295
T4	V3P3A valid to RSMRST_B deassertion	0,000	0,024	0,032	0,009
T5	RSMRST_B deassertion to SLP_S4_B deassertion	0,02			SOC related
T6	SLP_S4_B deassertion to SUSPWRDNACK goes HIGH	0,00			SOC related
T3_V3P3A-V1P8U	Rail to Subsequent Rail Turn-On Delay	0,50	1,00	2,05	0,703
T7	SLP_S4_B deassertion to V1P8U turn-on delay	0,000	0,024	0,032	0,049
T2_V1P8U	Ramp-Up time from 10% to 90% voltage	0,08	1,00	2,00	0,102
T3_V1P8U-VDDQ	Rail to Subsequent Rail Turn-On Delay	0,10	1,00	2,05	0,474
T2_VDDQ	Ramp-Up time from 10% to 90% voltage	0,08	1,00	2,00	0,473
T3_VDDQ-VREFDQ0	Rail to Subsequent Rail Turn-On Delay	0,50	1,00	2,05	0,707
T2_VREFDQ0	Ramp-Up time from 10% to 90% voltage	0,08	1,00	2,00	0,014
T3_VREFDQ0-VREFDQ1	Rail to Subsequent Rail Turn-On Delay	0,00			0,013
T2_VREFDQ1	Ramp-Up time from 10% to 90% voltage	0,08	1,00	2,00	0,015
T8	VREFDQ1 to DRAMPWROK assertion	0,000	0,024	0,032	0,018
T9	SLP_S4_B deassertion to SLP_S3_B deassertion	0,02			SOC related
T3_VREFDQ1-V5P0S	Rail to Subsequent Rail Turn-On Delay	0,50	1,00	2,05	0,566
T10	SLP_S3_B de-assertion to first S rail turn-on delay	0,000	3,000	6,166	0,015
T2_V5P0S	Ramp-Up time from 10% to 90% voltage	0,08	1,00	2,00	0,010
T3_V5P0S-VNN	Rail to Subsequent Rail Turn-On Delay	0,20	1,00	2,05	0,259
T2_VNN	Ramp-Up time from 10% to 90% voltage	0,08	1,00	2,00	0,084
T3_VNN-VCC	Rail to Subsequent Rail Turn-On Delay	0,20	1,00	2,05	0,257
T2_VCC	Ramp-Up time from 10% to 90% voltage	0,08	1,00	2,00	0,082
T3_VCC-V1P0S	Rail to Subsequent Rail Turn-On Delay	0,20	1,00	2,05	0,238
T2_V1P0S	Ramp-Up time from 10% to 90% voltage	0,08	1,00	2,00	0,062
T3_V1P0S-V1P05S	Rail to Subsequent Rail Turn-On Delay	0,10	1,00	2,05	0,109

T2_V1P05S	Ramp-Up time from 10% to 90% voltage	0,08	1,00	2,00	0,051
T3_V1P05S-V1P8S	Rail to Subsequent Rail Turn-On Delay	0,10	1,00	2,05	0,237
T2_V1P8S	Ramp-Up time from 10% to 90% voltage	0,08	1,00	2,00	0,092
T3_V1P8S-V1P2S	Rail to Subsequent Rail Turn-On Delay	0,10	1,00	2,05	0,155
T2_V1P2S	Ramp-Up time from 10% to 90% voltage	0,08	1,00	2,00	0,006
T3_V1P2S-V3P3S	Rail to Subsequent Rail Turn-On Delay	0,10	1,00	2,05	0,173
T2_V3P3S	Ramp-Up time from 10% to 90% voltage	0,08	1,00	2,00	0,290
T3_V3P3S-V2P285S	Rail to Subsequent Rail Turn-On Delay	0,10	1,00	2,05	0,108
T2_V2P85S	Ramp-Up time from 10% to 90% voltage	0,08	1,00	2,00	0,260
T11	SLP_S3_B deassertion to SLP_S0IX_B deassertion	0,03			SOC related
T3_V2P85S-VDDQ_VTT	Rail to Subsequent Rail Turn-On Delay	0,10	1,00	2,05	0,260
T12	SLP_S0IX_B deassertion to first SX rail turn-on delay	0,000	8,000	16,434	0,048
T2_VDDQ_VTT	Ramp-Up time from 10% to 90% voltage	0,08	1,00	2,00	0,006
T3_VDDQ_VTT-V1P2SX	Rail to Subsequent Rail Turn-On Delay	0,50	1,00	2,05	0,053
T2_V1P2SX	Ramp-Up time from 10% to 90% voltage	0,08	1,00	2,00	0,0001
T3_V1P2SX-V1P0SX	Rail to Subsequent Rail Turn-On Delay	0,10	1,00	2,05	0,017
T2_V1P0SX	Ramp-Up time from 10% to 90% voltage	0,08	1,00	2,00	0,061
T13	Core rails valid to VCCAPWEROK and COREPWROK assertion		100		100,1
T14	COREPWROK assertion to PLTRST_B deassertion	0,06			SOC related
T15	MODEM_OFF_B deassertion Delay from PLTRST_B deassertion	0,01	0,02	0,04	0,035
T16	SDWN_B deassertion Delay from PLTRST_B deassertion	0,04	0,06	0,075	0,068

Table 18: Cold Boot Timings

As the regulators power-up times are load dependent, worst case times of 2ms are programmed. This will guarantee that the rails have reached the target voltage. Optimization reducing the start-up time can be done when power rail load conditions are clear or on the final product.

The delay time for “Core rails valid to VCCAPWEROK and COREPWROK assertion” is programmable by the following register. The configuration bit for VCCAPWROK and SUSPWRDNOK are also included in the PWRSEQCFG register (page 0), as defined below.

Register Name		PWRSEQCFG		Address	0xDC Page 0	Read	
				Reset Value	0x0E		
MSB							LSB
R	R	R	R/W	R/W	R/W	R/W	R/W
Reserved			USBS DPCFG	VCCA PWROKCFG	SUSPWRD NACKCFG	DTPWROK	

DTPWROK	 00 01 **10** 11	Delay time for Core rails valid to VCCAPWROK and COREPWROK assertion 1ms 10ms 100ms 120ms
SUSPWRDNACKCFG	 0 **1**	When SLP_S4_B = 0, this bit decides if the power sequencer should go to SOC_G3 state if the SUSPWRDNACK is asserted. go to SOC G3 if SUSPWRDNACK = 1. not go to SOC G3 regardless of SUSPWRDNACK status.
VCCAPWROKCFG	 0 **1**	Option to de-assert VCCAPWROK when PMIC enters SOC S0IX state. VCCAPWROK gets de-asserted (=0) when entering SOC S0IX. VCCAPWROK remains asserted (=1) when entering SOC S0IX.
USBDPCFG	 **0** 1	Option to set ILIM[1:0] for USB SDP current limit. USB SDP, set ILIM[1:0] to 01 for 100mA current limit. USB SDP, set ILIM[1:0] to 11 for 500mA current limit.

10.3.2 Warm Reset Sequence

During a warm reset the SoC will toggle the PLTRST_B pin for a certain amount of time. This sequence can only happen while in SOC_S0 state. DA6021 captures this event in order to disable/idle the I2C interface and SVID interface. All voltage rails remain in regulation, except VCC and VNN, as those will be re-programmed to VBOOT voltage.

10.3.3 Enter SOC S0iX Mode

The S0iX state is entered when the SOC is in a shallow sleep state. This state is entered when the SOC asserts the SLP_S0IX_B (LOW) pin to the PMIC. VDDQ_VTT and SX rails are turned off. The VCC rail is either turned off by SVID commands (not by SLP_S0IX_B signal) or set to a voltage set in SVID address 0x39. The VNN rail is set to a voltage set in SVID address 0x39.The rest of the VRs remain on but enters into power save mode.

VCCAPWROKCFG bit in register PWRSEQCFG provides the option to de-assert VCCAPWROK in S0IX state.

VCCAPWROKCFG =1, PMIC does not deassert VCCAPWROK when entering S0IX state,

VCCAPWROKCFG =0, PMIC deasserts VCCAPWROK after SLP_S0IX_B is asserted and before VRs start to turn off when entering S0IX state.

The rail sequencing is shown in the figure below.

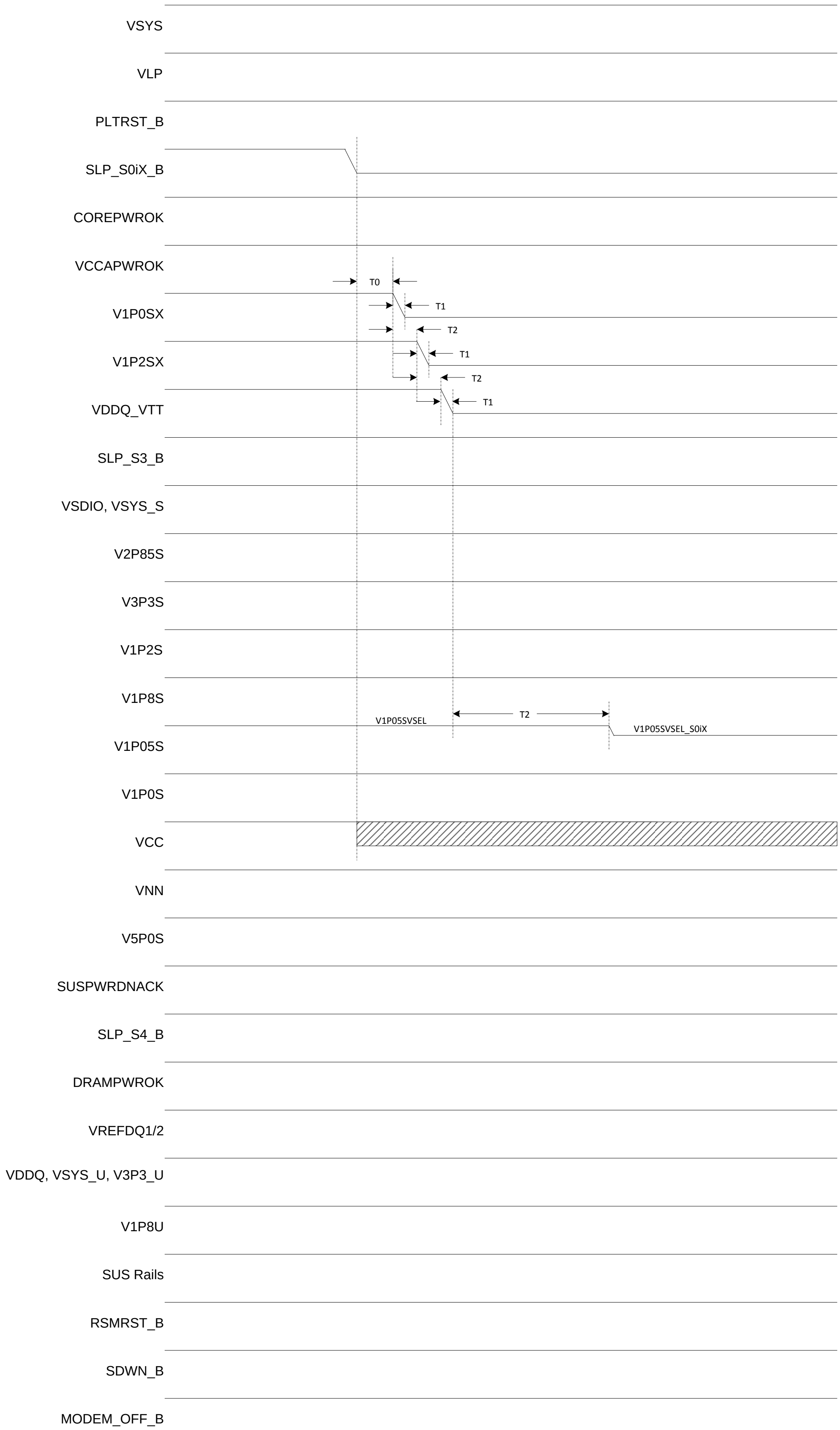


Figure 10: Enter S0iX Sequencing Diagram (VCCAPWROKCFG=1)

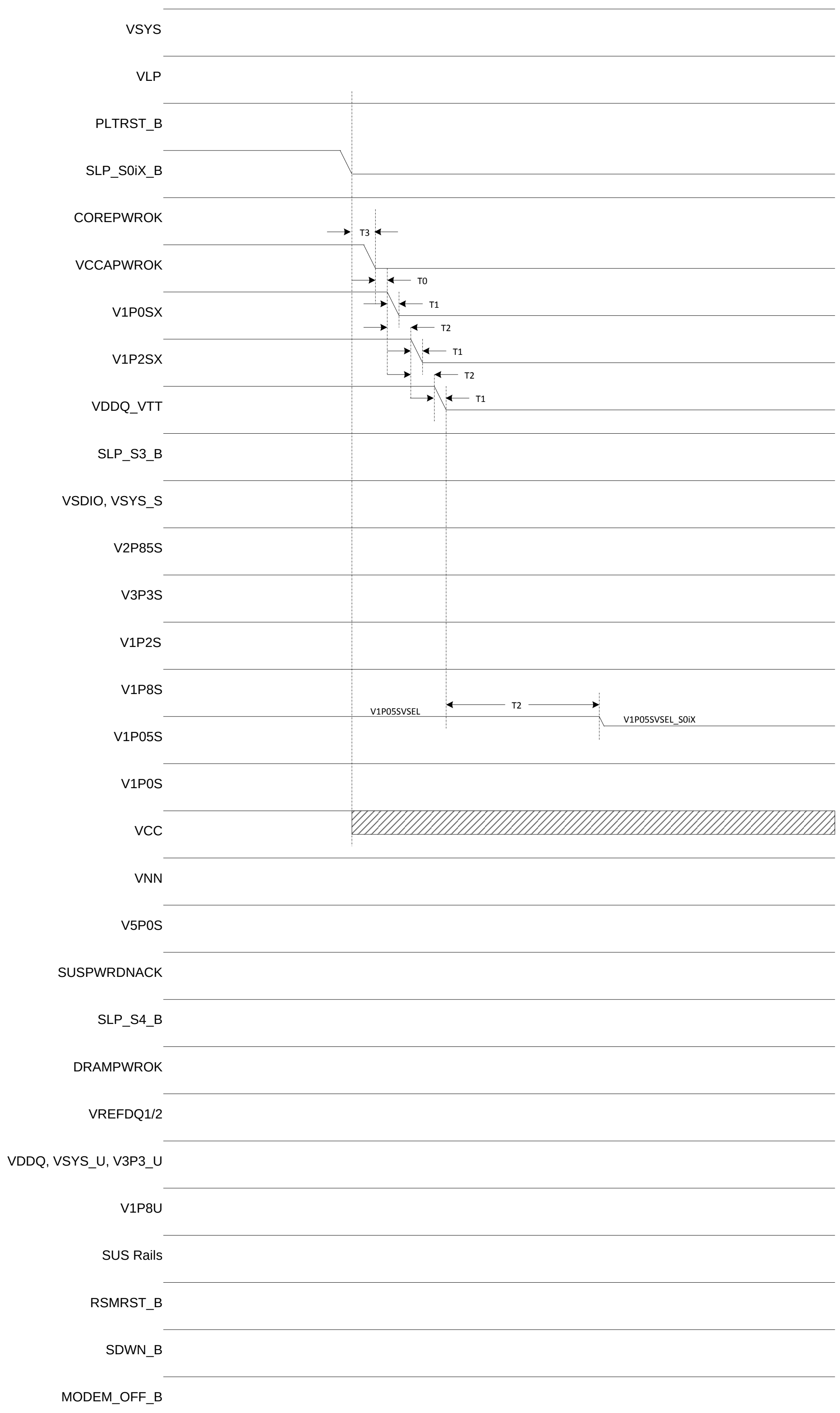


Figure 11: Enter S0iX Sequencing Diagram (VCCAPWROKCFG=0)

Parameter	Description	Min [ms]	Typ [ms]	Max [ms]	Measured [ms]
T3	SLP_S0IX_B assertion to VCCAPWROK deassertion	0,000	0,008	0,016	0,001
T0_V1P2SX	SLP_S0IX_B assertion to first SX rail starts to turn off	0,000	0,008	0,016	0,048
T1_V1P2SX	Ramp-down time from 90% to 10%	0,1	1,00	2,00	0,608
T2_V1P0SX-V1P2SX	Rail to Subsequent Rail Turn-Off Delay	0,5	1,00	3,00	0,975
T1_V1P0SX	Ramp-down time from 90% to 10%	0,1	1,00	2,00	0,01
T2_V1P2SX-VDDQ_VTT	Rail to Subsequent Rail Turn-Off Delay	0,5	1,00	3,00	1,053
T1_VDDQ_VTT	Ramp-down time from 90% to 10%	0,1	1,00	2,00	0,619
T2_VDDQ_VTT-V1P05S	Rail to Subsequent Rail Turn-Off Delay	0,5	1,00	3,00	0,615
T1_V1P05S	V1P05S S0 to S0IX Level transition	0,5	1,00	2,00	0,032

Table 19: Enter S0iX timing

10.3.4 Exit SOC S0iX Mode

The S0IX state is exited when the SOC de-asserts the SLP_S0IX_B pin (HIGH). VDDQ_VTT and SX rails are turned on. The VCC rail will be turned on by SVID commands (not by SLP_S0IX). The rest of the rails will come out of power save mode.

The rail sequencing is shown in the figure below:

Figure 12: Exit S0iX Sequencing Diagram (VCCAPWROKCFG=1)

Figure 13: Exit S0iX Sequencing Diagram (VCCAPWROKCFG=0)

Parameter	Description	Min [ms]	Typ [ms]	Max [ms]	Measured [ms]
T0	SLP_S0IX_B deassertion to first SX rail turn-on delay	0,000	0,008	0,016	0,006
T1_V1P05S	Ramp-Up time from 10% to 90%	0,04	0,08	0,16	0,033
T2_V1P05S-VDDQ_VTT	Rail to Subsequent Rail Turn-On Delay	0,00	0,05	0,10	0,028
T1_VDDQ_VTT	Ramp-Up time from 10% to 90%	0,04	0,08	0,16	0,007
T2_VDDQ_VTT-V1P2SX	Rail to Subsequent Rail Turn-On Delay	0,00	0,05	0,10	0,053
T1_V1P2SX	Ramp-Up time from 10% to 90%	0,04	0,08	0,16	0,0001
T2_V1P2SX-V1P0SX	Rail to Subsequent Rail Turn-On Delay	0,00	0,05	0,10	0,017
T1_V1P0SX	Ramp-Up time from 10% to 90%	0,04	0,08	0,16	0,062
T3	Total S0IX exit latency: from SLP_S0IX_B de-assertion to all VRs up			0,200	0,169
T4	Time from All VRs are valid to VCCAPWEROK assertion	0,000	0,008	0,016	0,013

Table 20: Exit S0iX timing

10.3.5 Enter SOC S3 Mode

The S3 state is entered when the SOC asserts the SLP_S3_B pin (LOW). VRs that remain on enter into power saving mode.

The rail sequencing is shown in the figure below.

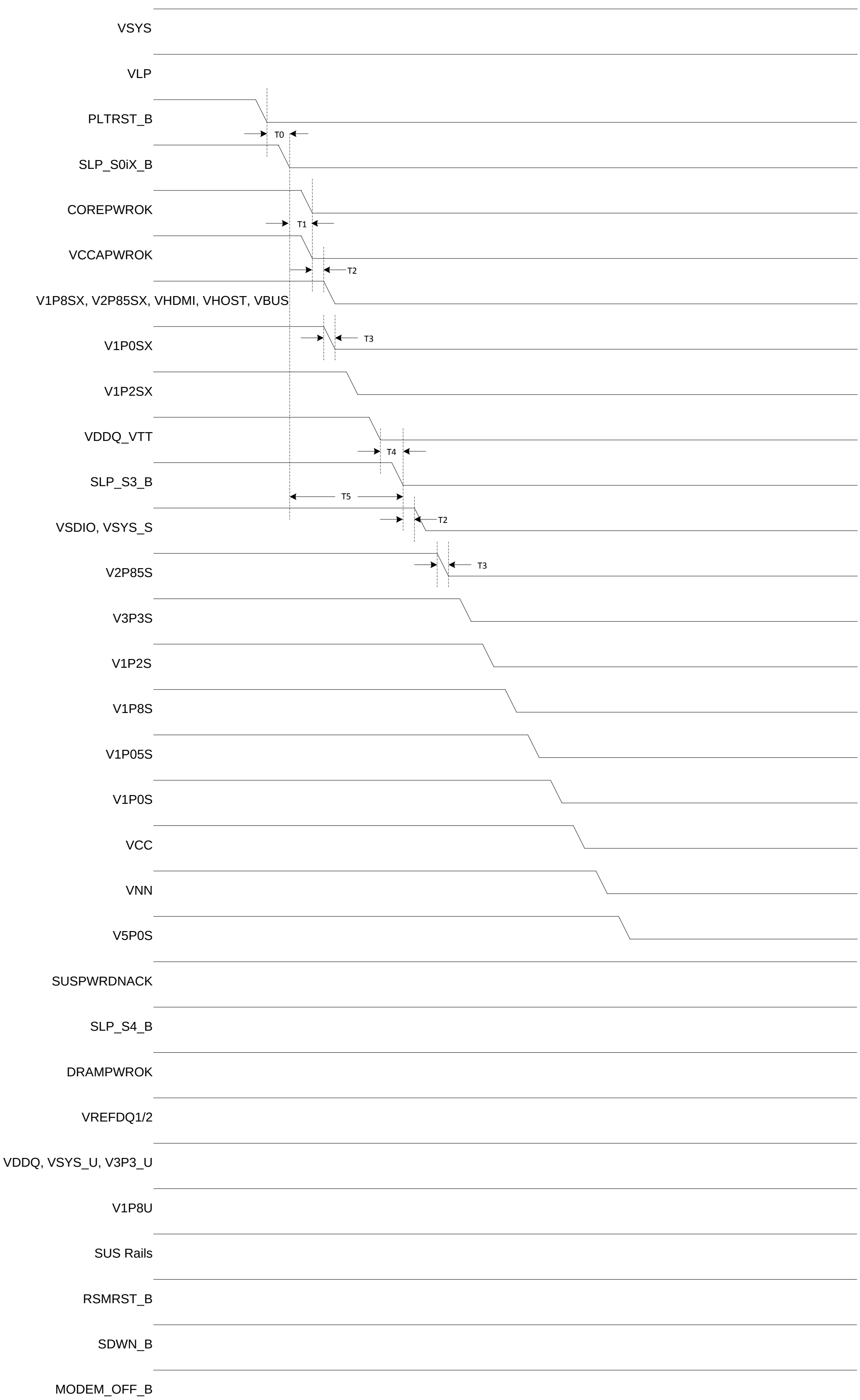


Figure 14: Enter S3 Sequencing Diagram

10.3.6 Exit SOC S3 Mode

The S3 state is exited when the SOC de-asserts the SLP_S3_B pin (HIGH). Voltage rails will be turned on and come out of power saving mode.

The rail sequencing is shown in the figure below.

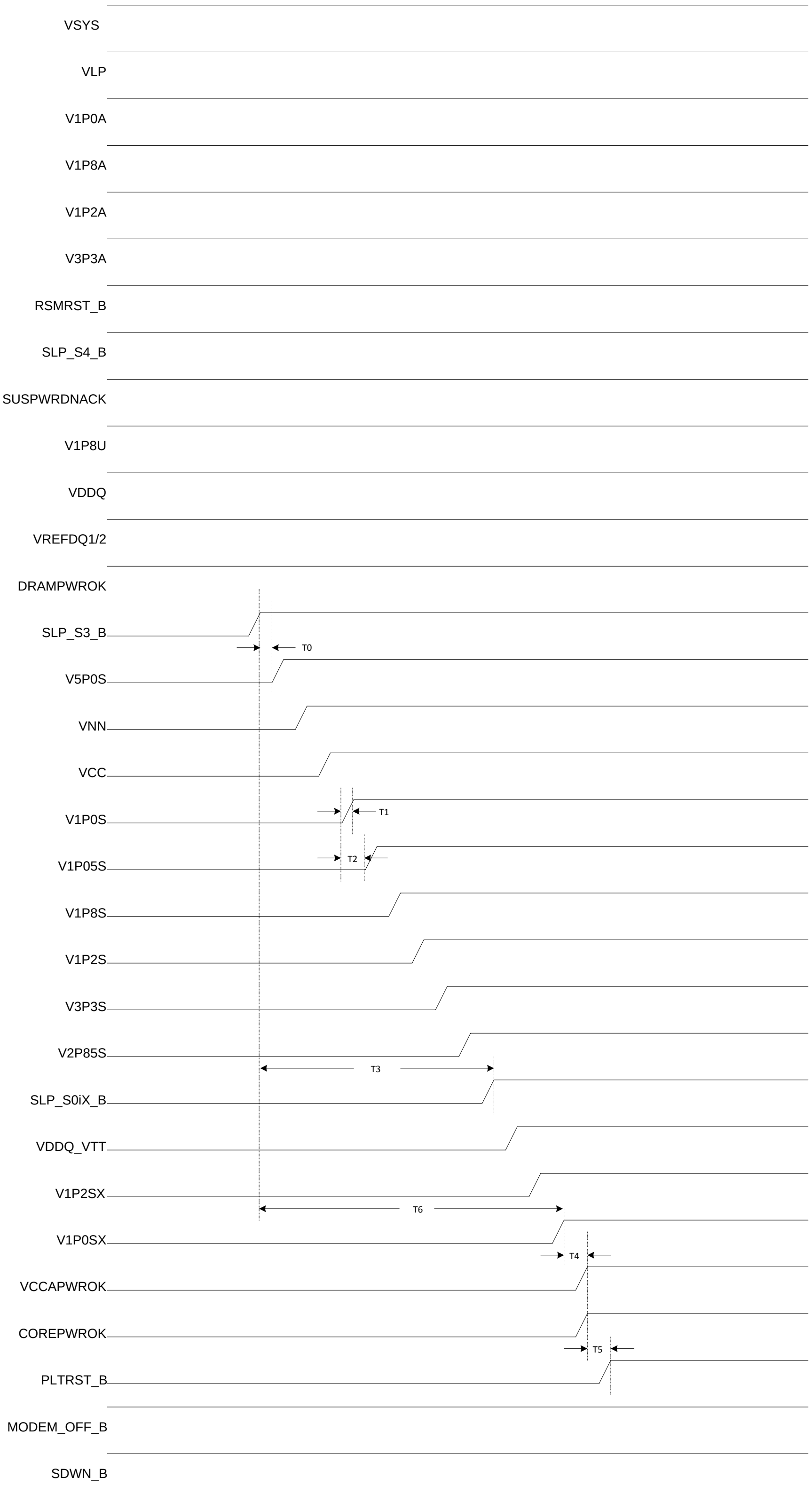


Figure 15: Exit S3 Sequencing Diagram

10.3.7 Enter SOC S4 Mode

The S4 state is entered when the SOC asserts the SLP_S4_B pin (LOW). VRs that remain on enter into power saving mode.

The rail sequencing is shown in the figure below.

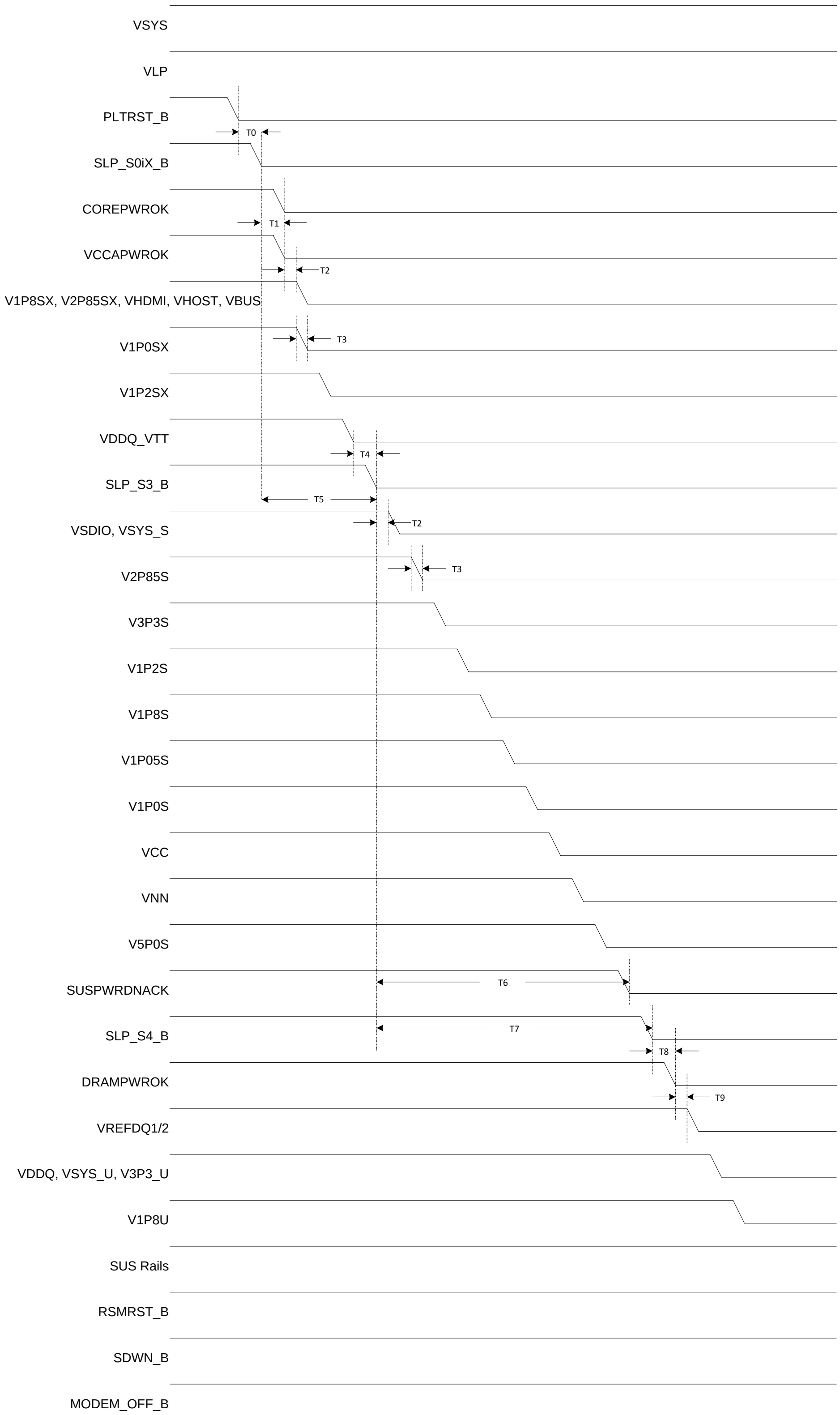


Figure 16: Enter S4 Sequencing Diagram

10.3.8 Exit SOC S4 Mode

The S4 state is exited when the SOC de-asserts the SLP_S4_B pin (HIGH). Voltage rails will be turned on and come out of power saving mode.

The rail sequencing is shown in the figure below.

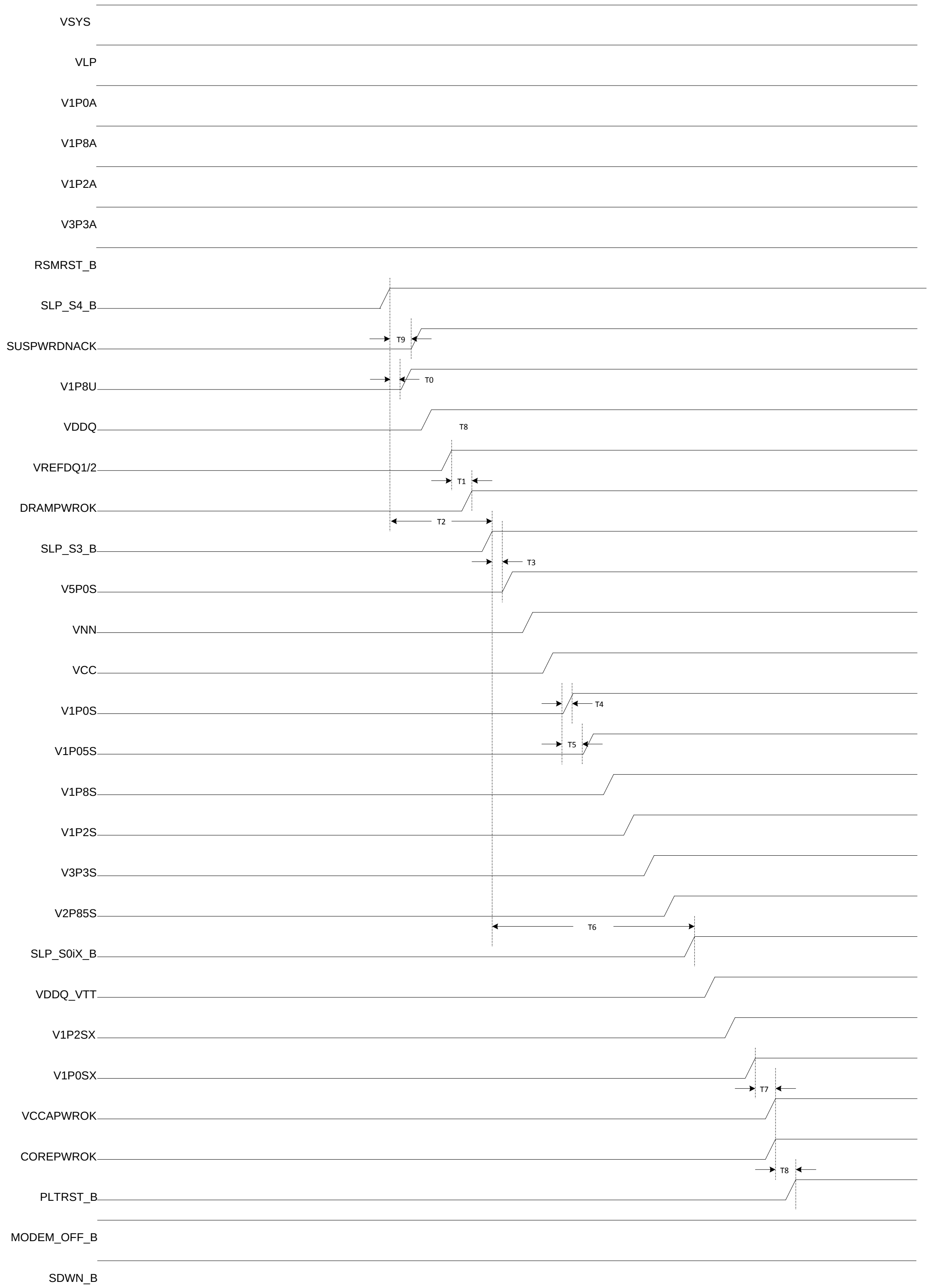


Figure 17: Exit S4 Sequencing Diagram

10.3.9 Cold Off

A Cold Off, either through a SOC request or a system event, requests DA6021 in the 'Mechanical Off' (SOC G3, G3 for battery removal with no external power source) state. The system remains in this state until it receives a wake-up event, or until platform power sources are removed.

Event	Conditions (all mandatory)	Notes
SOC Initiated Shut Down	• SUSPWRDNACKCFG = 1 • SUSPWRDNACK = 1 • SLP_S4_B = 0 • RSMRST_B = 1	• DA6021 powers down in sequenced order controlled by SLP_S*_B and SUSPWRDNACK = 1 from SOC
Power Button Held	• Power button pressed for a defined length in FCOT[3:0] or longer (i.e. PBHT Timer ≥ FCOT[3:0])	• After debounce time, power button are held for at least the length defined in FCOT[3:0] (the default is 4 seconds), assert SDWN_B immediately. After 90us, DA6021 powers down in sequenced order, without waiting for SLP_S*_B from SOC
PMIC Critical Events	• See events defined in "PMIC Catastrophic and Critical Events"	• Assert SDWN_B immediately. After 90us, DA6021 powers down in sequenced order, without waiting for SLP_S*_B from SOC
PMIC Catastrophic Events Except VSYSOVP	• See events defined in "PMIC Catastrophic and Critical Events"	• Assert SDWN_B immediately. After 90us, DA6021 powers down, without waiting for SLP_S*_B from SOC
VSYSOVP	• See events defined in "PMIC Catastrophic and Critical Events"	• Assert SDWN_B together with powering down immediately without waiting for SLP_S*_B from SOC

Table 21: Cold Off Triggers

Cold Off sequencing and timings are detailed in the figures and tables below.

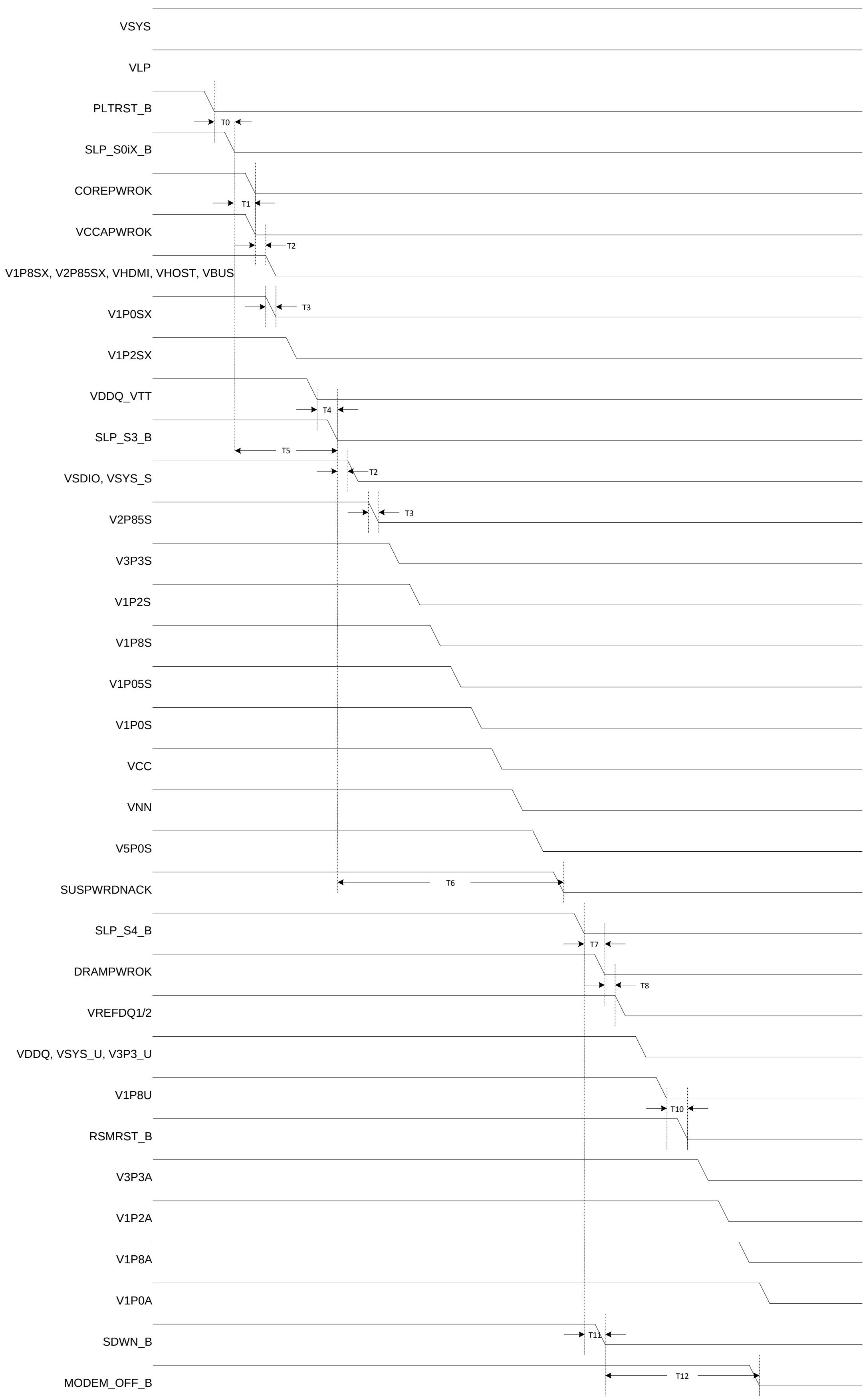


Figure 18: Cold Off Power Sequencing Diagram (SUSPWRDNACKCFG=1)

For SOC initiated Cold Off, there is a configuration bit in the RTC domain supplied registers called SUSPWRDNACKCFG. This bit decides whether DA6021 enters SOC G3 state or stops at SOC S4 state:

- When RSMRST_B=1, SLP_S4_B=0 and SUSPWRDNACKCFG=1, DA6021 enters SOC G3 state if SUSPWRDNACK=1
- When RSMRST_B=1, SLP_S4_B=0 and SUSPWRDNACKCFG=0, DA6021 stops at SOC S4 state, no matter SUSPWRDNACK=1 or 0. The Power Sequence diagram will be the same as that of “Enter SOC S4 Sequence Default Behavior Diagram” except that SUSPWRDNACK could be set (=1) or cleared (=0) when SLP_S4_B is asserted (=0).

Parameter	Description	Min [ms]	Typ [ms]	Max [ms]	Measured [ms]
T0	PLTRST_B assertion to SLP_S0IX_B assertion	0,031			SOC related
T1	SLP_S0IX_B assertion to VCCAPWROKCFG deassertion	0,000	0,008	0,016	0,002
T2_V1P2SX	VCCAPWROK deassertion to first VR starts to turn off	0,000	0,008	0,016	0,051
T3_V1P0SX	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	0,624
T4_V1P0SX-V1P2SX	Rail to Subsequent Rail Turn-Off Delay	0,5	1,00	3,00	0,995
T3_V1P2SX	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	0,010
T4_V1P2SX-VDDQ_VTT	Rail to Subsequent Rail Turn-Off Delay	0,5	1,00	3,00	1,037
T3_VDDQ_VTT	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	0,617
T2_VBUS	VCCAPWROK deassertion to OnDemand VR starts to turn off	0,5	1,00	3,00	1,794
T3_VBUS	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	2,660
T2_V1P8SX	VCCAPWROK deassertion to OnDemand VR starts to turn off	0,5	1,00	3,00	2,378
T3_V1P8SX	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	0,059
T2_V2P85SX	VCCAPWROK deassertion to OnDemand VR starts to turn off	0,5	1,00	3,00	2,120
T3_V2P85SX	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	0,028
T2_VHDMI	VCCAPWROK deassertion to OnDemand VR starts to turn off	0,5	1,00	3,00	2,366
T3_VHDMI	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	1,563
T2_VHOST	VCCAPWROK deassertion to OnDemand VR starts to turn off	0,5	1,00	3,00	2,719
T3_VHOST	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	0,402
T5	SLP_S0IX_B assertion to SLP_S3_B assertion	0			SOC related
T4_VDDQ_VTT-V2P85S	Rail to Subsequent Rail Turn-Off Delay	0,5	1,00	3,00	0,661
T2_V2P85S	SLP_S3_B assertion to VR starts to turn off	0,000	0,008	0,016	0,037
T3_V2P85S	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	0,687
T4_V2P85S-V3P3S	Rail to Subsequent Rail Turn-Off Delay	0,5	1,00	3,00	0,621
T3_V3P3S	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	3,363
T4_V3P3S-V1P2S	Rail to Subsequent Rail Turn-Off Delay	0,5	1,00	3,00	0,891

T3_V1P2S	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	0,074
T4_V1P2S-V1P8S	Rail to Subsequent Rail Turn-Off Delay	0,5	1,00	3,00	0,660
T3_V1P8S	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	0,037
T4_V1P8S-V1P05S	Rail to Subsequent Rail Turn-Off Delay	0,5	1,00	3,00	0,878
T3_V1P05S	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	0,426
T4_V1P05S-V1P0S	Rail to Subsequent Rail Turn-Off Delay	0,5	1,00	3,00	0,533
T3_V1P0S	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	0,574
T4_V1P0S-VCC	Rail to Subsequent Rail Turn-Off Delay	0,5	1,00	3,00	0,997
T3_VCC	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	0,196
T4_VCC-VNN	Rail to Subsequent Rail Turn-Off Delay	0,5	1,00	3,00	0,512
T3_VNN	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	0,203
T4_VNN-V5P0S	Rail to Subsequent Rail Turn-Off Delay	0,5	1,00	3,00	0,548
T3_V5P0S	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	4,557
T2_VSYS_S	VCCAPWROK deassertion to OnDemand VR starts to turn off	0,5	1,00	3,00	2,327
T3_VSYS_S	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	0,003
T2_VSDIO	SLP_S3_B deassertion to OnDemand VR starts to turn off	0,5	1,00	3,00	1,284
T3_VSDIO	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	0,025
T6	SLP_S3_B assertion to SLP_S4_B assertion	0			SOC related
T7	SLP_S4_B assertion to DRAMPWROK deassertion	0,000	0,024	26,02	0,015
T4_V5P0S-VREFDQ0	Rail to Subsequent Rail Turn-Off Delay	0,5	1,00	3,00	0,601
T8	DRAMPWROK deassertion to VREFDQ0 starts to turn off	0,000	0,024	0,032	0,005
T3_VREFDQ0	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	0,063
T4_VREFDQ0-VREFDQ1	Rail to Subsequent Rail Turn-Off Delay	0,5	1,00	3,00	0,513
T3_VREFDQ1	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	0,062
T4_VREFDQ1-VDDQ	Rail to Subsequent Rail Turn-Off Delay	0,5	1,00	3,00	0,535
T3_VDDQ	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	0,999
T4_VDDQ-VSYS_U	Rail to Subsequent Rail Turn-Off Delay	0,5	1,00	3,00	1,027
T3_VSYS_U	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	0,085
T4_VSYS_U-V3P3U	Rail to Subsequent Rail Turn-Off Delay	0,5	1,00	3,00	1,079
T3_V3P3U	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	1,024
T4_V3P3_U-V1P8U	Rail to Subsequent Rail Turn-Off Delay	0,5	1,00	3,00	0,970
T3_V1P8U	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	0,329
T9	V1P8U voltage < 10% to RSMRST_B assertion	0,000	0,024	0,032	0,098
T10	RSMRST_B assertion to V3P3A starts to turn off	0,000	0,024	0,032	0,036
T3_V3P3A	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	0,951

T4_V3P3A-V1P2A	Rail to Subsequent Rail Turn-Off Delay	0,5	1,00	3,00	0,992
T3_V1P2A	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	0,075
T4_V1P2A-V1P8A	Rail to Subsequent Rail Turn-Off Delay	0,5	1,00	3,00	1,086
T3_V1P8A	Ramp-down Time from 90% to 10%	0,5	1,00	2,00	0,730
T4_V1P8A-V1P0A	Rail to Subsequent Rail Turn-Off Delay	0,5	1,00	3,00	0,979
T3_V1P0A	Rail to Subsequent Rail Turn-On Delay	0,50	1,00	2,05	0,538
T11	SLP_S4_B assertion to SDWN_B assertion	0,000	0,024	0,032	0,003
T12	SDWN_B assertion to MODEM_OFF_B assertion	0,40		0,80	0,608

Table 22: Cold Off Sequencing Timing

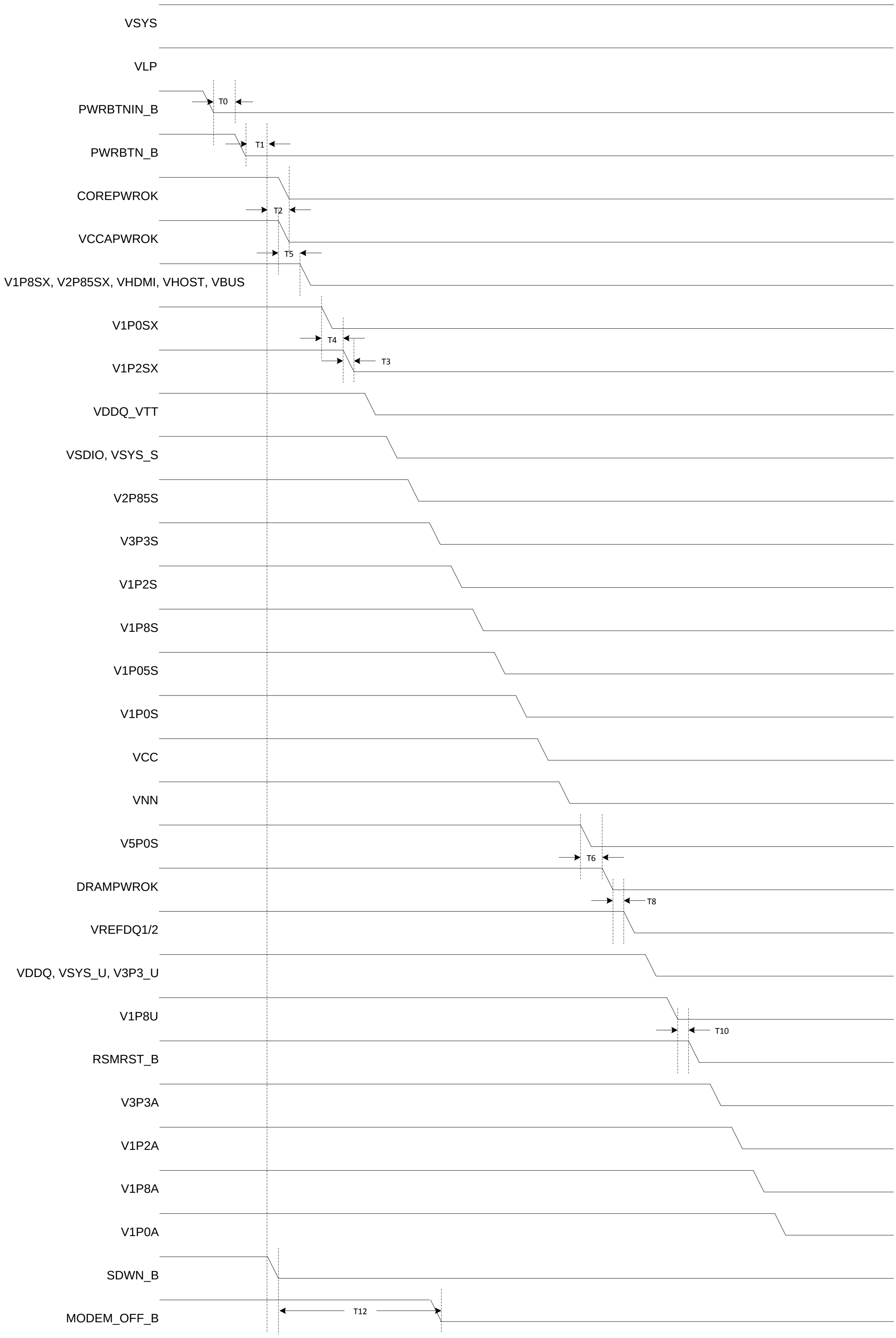


Figure 19: Power Button forced Cold Off

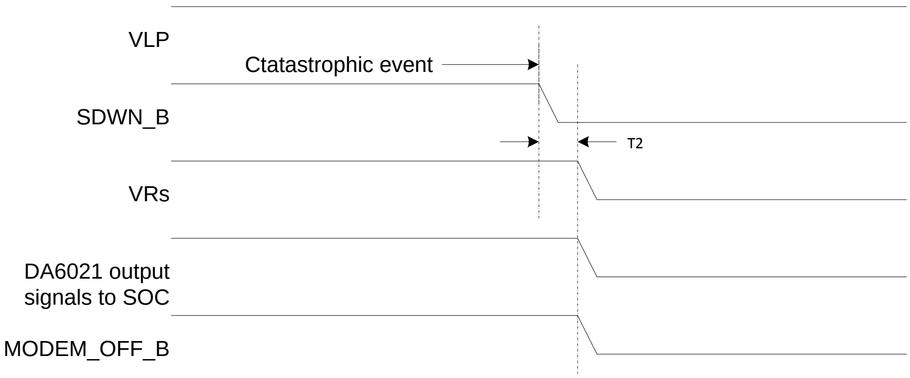


Figure 20: Catastrophic Event (except VSYSOVP) Shutdown Sequence

Parameter	Description	Min	Typ [µs]	Max	VAL
T2	SDWN_B assertion to shutdown all VRs and DA6021 output signals	-10%	90	+10%	D,E

Table 23: Catastrophic Event (except VSYSOVP) Shutdown Sequence

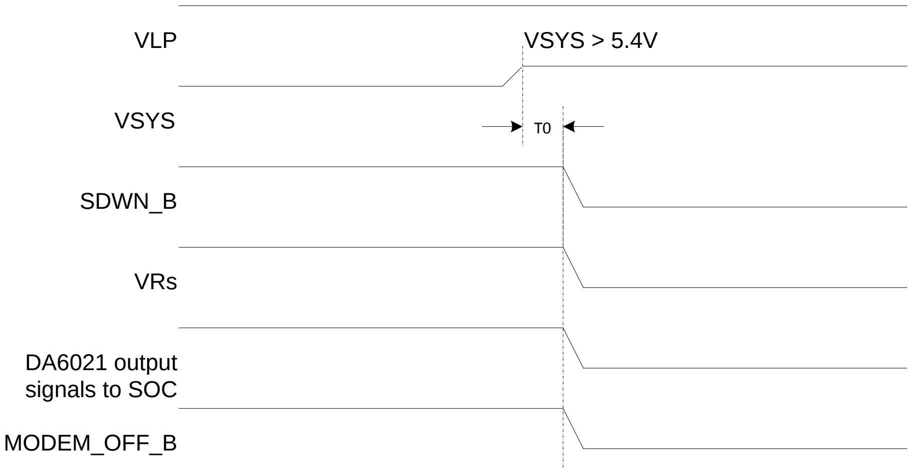


Figure 21: VSYSOVP Shutdown Sequence

Parameter	Description	Min [µs]	Typ [µs]	Max [µs]	VAL
T0	VSYSOVP debounce time	90	100	110	D,E

Table 24: VSYSOVP Shutdown Timing

10.3.10 Modem Reset Sequence

The sequence is initiated by the SoC while setting the MODEMRSTSEQ bit. During a modem reset sequence DA6021 will toggle the SDWN_B and MODEM_OFF_B pins. For detail refer to the following diagram.

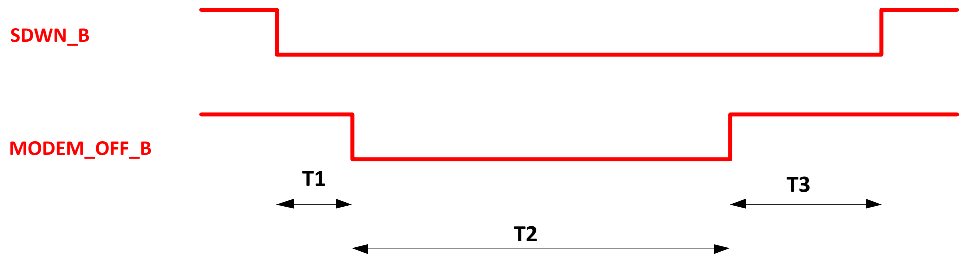


Figure 22: Modem Reset Sequencing Diagram

Intervals	T1	T2	T3
Time	400us-800us	14ms (min)	5ms (min)

Table 25: Modem Reset Timing Intervals

Register Name		**MODEMCTRL**		Address	**0x29 Page 1**	Read/Write	
					0x01		
MSB							LSB
R	R	R	R	R	R	R/W	R/W
reserved						MODEM_ RSTSEQ	MODEM_ OFF_ST
MODEM_OFF_ST		0 **1**	Actual status of the MODEM_OFF_B bit				
MODEM_RSTSEQ		**0** 1					

10.4 PMIC Resets

The following table summarizes the reset sources for DA6021

Reset Source	Reset trigger	Reset Type/Sequence
SoC Request	PLTRST_B	Warm Reset
External Button	PWRBTN_B held longer than time defined in FCOT[3:9]	Forced Cold Off, shutdown all voltage regulators and return to SOC_G3 state (not waiting for any SLP_S*_B signals from SOC
Catastrophic and Critical Event	THERMTRIP_B	Shutdown all voltage regulators, return to SOC_G3 state (not waiting for any SLP_S*_B signals from SOC)
	PMICTEMP	
	System Temperature	
	Battery Temperature	
	VSYSUVP	
	VSYSOVP	
	Main Battery Removal (BATRM, if BATRMDEN set)	
	BCU VCRIT (if enabled)	
Wake Event from Cold off	Battery Insertion	Cold boot
	USB Charger insertion	
	AC/DC Adapter insertion	
	PWRBTN_B pressed	

Table 26 : PMIC Reset Sources

10.5 Wake Events

There are several events that can wake the system from SOC_G3 or G3 state. These are:

- Battery Insertion
- USB Charger Insertion
- AC/DC Adapter Insertion
- Power Button

All of these events can cause a System Boot if it is in SOC_G3, but booting is depending on the battery voltage. The first 3 wake events, battery insertion, USB or AC/DC adapter insertion can cause a boot depending on the SRCWAKECFG register as defined below:

Register Name		**SRCWAKECFG**		Address	**0xDB Page 1**	Read/Write	
					0x00		
MSB							LSB
R	R	R	R	R	R/W	R/W	R/W
reserved					ADWAKEEN	USBWAKEEN	BATWAKEEN
BATWAKEEN		**0** 1	No wake up if battery insertion is detected Wake up if battery insertion detected and further boot criteria met				
USBWAKEEN		**0** 1	No wake up if USB charger insertion is detected Wake up if USB charger insertion detected and further boot criteria met				
ADWAKEEN		**0** 1	No wake up if ACDC adapter insertion is detected Wake up if ACDC adapter insertion detected and further boot criteria met				

11. Platform Power Domains

11.1 Power Domains Summary

The power supply part of DA6021 consists of various power supplies modules:

Power Supply Module	DA6021 Supplied Pins	Supplied Voltage	Supplied Current	Notes
BUCK_CORE	VCC	0.5 – 1.2V ±2% accuracy (DC & ripple) Default: 1.0V ±1.5%	8000mA	Quad phase buck converter, including IMVP-7 SVID interface with a voltage granularity of 10mV
BUCK_GRAPHIC	VNN	0.5 – 1.2V ±2% accuracy (DC & ripple) Default: 1.0V ±1.5%	8000mA	Quad phase buck converter, optional triple phase buck (OTP), including IMVP-7 SVID interface with a voltage granularity of 10mV
BUCK_V1P0	V1P0A	1.00V ±2% accuracy (DC & ripple)	1900mA	Single phase buck converter Nominal voltage 1.01V
BUCK_V1P05S	V1P05S	1.05V ±2% accuracy (DC & ripple)	475mA	Single phase buck converter Nominal output voltage 1.05V
BUCK_1P8	V1P8A	1.8V ±2% accuracy (DC & ripple)	1627mA	Single phase buck converter Nominal voltage 1.817V
BUCK_VDDQ	VDDQ	1.5/1.35/1.25V ±2% accuracy (DC & ripple)	2800mA	Dual phase buck converter Nominal voltage 1.24V
BUBO_V3P3	V3P3A	3.3V ±2% accuracy (DC & ripple)	1569mA	Buck boost converter Nominal voltage 3.332V
BUBO_V2P85	V2P85S	2.9V ±4% accuracy (DC & ripple & transient over/under)	550mA	Buck boost converter Nominal voltage 2.9V
BOOST_V5P0	V5P0S	5.0V ±4% accuracy (DC & ripple & transient over/under))	1000mA	Boost converter Nominal voltage 5.048V
LDO_VDDQ_VTT	VDDQ_VTT	½ VDDQ ±2% accuracy (DC)	325mA	Push-pull LDO for DDR3 address line termination.
LDO_V1P2A	V1P2A	1.2V ±2% accuracy (DC)	30mA	LDO supplied by BUCK_V1P8A, low quiescent current
LDO_VREFDQ0	VREFDQ0	±3% accuracy (DC & ripple)	10mA	LDO supplied by BUCK_V1P8A
LDO_VREFDQ1	VREFDQ1	±3% accuracy (DC & ripple)	10mA	LDO supplied by BUCK_V1P8A
LDO_VLP	VLP	2.5V ±1.5% accuracy (DC)	10mA	LDO supplying the internal DA6021 electronic

SD/LDO_V1P2S	V1P2S	VDDQ/V1P8	34mA	Function between switching device (SD) and LDO can be selected via device order code. SD can be used with DDR3 LP memory for all other types of memories the LDO solution is proposed
SD_V1P2SX	V1P2SX	VDDQ/V1P8	155mA	Switching device to generate V1P2SX. In case of DDR3 L memory this voltage will be 1.35V
SD_VUSBPHY	VUSBPHY	VSYS/V3P3_A	40mA	Switching device supplying the USBPHY with 3.3V. If V3P3A is switched off VUSBPHY is supplied by VSYS
SD_VSDIO	VSDIO	V1P8A/V3P3A	400mA/200mA	Switching device supplying the SDIO interface. Output voltage is controlled by digital input signals from SoC
SD_V1P8S	V1P8S	V1P8A	144mA	DA6021 internal switching device supplied by V1P8A
SD_V1P8SX	V1P8SX	V1P8A	240mA	DA6021 internal switching device supplied by V1P8A
SD_V2P85SX	V2P85SX	V2P85S	250mA	DA6021 internal switching device supplied by V2P85S
SD_VHDMI	VHDMI	V5P0S	55mA	DA6021 internal switching device supplied by V5P0S
SD_VSYS_S	VSYS_S	VSYS	10mA	DA6021 internal switching device supplied by VSYS
EFS_VSYSU	VSYSU	VSYS	2750mA	External p-channel FET switched power domain supplied by VSYS
EFS_VSYS_SX	VSYS_SX	VSYS	2500mA	External p-channel FET switched power domain supplied by VSYS
EFS_V3P3U	V3P3U	V3P3A	700mA	External p-channel FET switched power domain supplied by V3P3A
EFS_V3P3S	V3P3S	V3P3A	584mA	External p-channel FET switched power domain supplied by V3P3A
EFS_V1P8U	V1P8U	V1P8A	355mA	External p-channel FET switched power domain supplied by V1P8A
EFS_V1P0S	V1P0S	V1P0A	410mA	External n-channel FET switched power domain supplied by V1P0A
EFS_V1P0SX	V1P0SX	V1P0A	916mA	External n-channel FET switched power domain supplied by V1P0A
EFS_VHOST	VHOST	V5P0S	900mA	External switched power domain supplied by V5P0S
EFS_VBUS	VBUS	V5P0S	900mA	External switched power domain supplied by V5P0S

Table 27: Power Domains

11.2 Voltage Rail ON/OFF On Various Power States

Supply Module	Voltage domain	S0	S0ix	S3	S4/5	G3
VLV2	VCC	On	Off	Off	Off	Off
VLV2	VNN	On	On	Off	Off	Off
VLV2	V1P0A	On	On	On	On	Off
VLV2	V1P05S	On	On	Off	Off	Off
VLV2	V1P8A	On	On	On	On	Off
VLV2/DDR3	VDDQ	On	On	On	Off	Off
VLV2, Peripherals	V3P3A	On	On	On	On	Off
Peripherals	V2P85S	On	On	Off	Off	Off
Peripherals	V5P0S	On	On	Off	Off	Off
DDR3	VDDQ_VTT	On	On	Off	Off	Off
VLV2	V1P2A	On	On	On	On	Off
	VREFDQ0	On	On	On	Off	Off
	VREFDQ1	On	On	On	Off	Off
DA6021	VLP	On	On	On	On	Off
	V1P2S	On	On	Off	Off	Off
	V1P2SX	On	Off	Off	Off	Off
Peripherals	VUSBPHY	On	On	On	On	Off
Peripherals	VSDIO	On/Off *)	On/Off *)	Off	Off	Off
VLV2	V1P8S	On	On	Off	Off	Off
	V1P8SX	On/Off *)	Off/Off *)	Off	Off	Off
Peripherals	VHDMI	On/Off *)	On/Off *)	Off	Off	Off
	VSYS_S	On/Off *)	On/Off *)	Off	Off	Off
Peripherals	VSYSU	On/Off *)	On/Off *)	On/Off *)	Off	Off
Peripherals	VSYS_SX	On/Off *)	On/Off *)	Off	Off	Off
Peripherals	V2P85SX	On/Off *)	On/Off *)	Off	Off	Off
Peripherals	V3P3U	On/Off *)	On/Off *)	On/Off *)	Off	Off
VLV2	V3P3S	On	On	Off	Off	Off
Peripherals	V1P8U	On	On	On	Off	Off
VLV2	V1P0S	On	On	Off	Off	Off
VLV2	V1P0SX	On	Off	Off	Off	Off
Peripherals	VHOST	On/Off *)	On/Off *)	Off	Off	Off
Peripherals	VBUS	On/Off *)	On/Off *)	Off	Off	Off

Table 28: Status Power Domains

*) on-demand register controlled

11.3 PMIC Current Consumption in Various States

Ta = 25°C, VSYS = 3.7V, no load

Power State	min	Typ. [mA]	Max
SOC_S0		2.089	
SOC_S0iX		1.793	
SOC_S3		1.022	
SOC_S4		0.789	
SOC_G3		0.069	
G3		0.056	

Table 29: PMIC Current Consumption

11.4 Voltage Rail Control Mechanism

Proper power-up/down sequencing is mandatory preventing damages. Optimizing the platform power consumption, unneccessary components as well as its related power rails shall be switched off. There are several methods controlling the power rails.

- VCC & VNN are controlled via the SVID interface
- State transitions, SOC provides SLP_S0iX_B, SLP_S3_B and SLP_S4_B signals to DA6021 controlling the related power rails
- Sequencer controlling
- Dedicated register control

11.5 SVID Interface

SOC communicates with the DA6021 via the SVID interface. SVID's commands composed of 9 bits – 4 MSBs determine the address and 5 LSBs are the command bits. DA6021 supports 2 SVID voltage regulators – VCC & VNN. The address for each of the voltage regulator is indicated in the table below:

Address	Target	Description
0x00	VCC	All commands will be routed to the VCC SVID registers and DA6021 will respond with the VCC status information
0x01	VNN	All commands will be routed to the VNN SVID registers and DA6021 will respond with the VNN status information

Table 30: VCC & VNN Addresses

11.5.1 SVID DC Electrical Parameters

The following table outlines the SVID DC electrical parameters. Note that low voltage operation is essential to avoid level converters to/from the processor. DA6021 SVID buffer should take V1P0S_FB as a reference voltage for improved signal integrity at the receiver.

Symbol	Parameter	Min	Typ	Max	Units	Notes	Val
V1P0S	SVID IO voltage	0.95	1.00	1.05	V		-
VIL	Input low voltage			0.45* V1P0S	V	1	A
VIH	Input high voltage	0.65* V1P0S			V	1	A
VHYS	Hysteresis voltage	0.05			V		E,D
VOH	Output high voltage		V1P0S		V	1	-
RON	Buffer on resistance (data line & alert# line)	10		20	Ω	2	D
IL	Leakage current	-100		100	uA	3	A
CPAD	Pad capacitance			4.0	pF	4	D
VPIN	Pin capacitance			5.0	pF		D

Table 31: SVID DC Electrical Characteristics

NOTES:

1. V1P0S refers to instantaneous voltage at V1P0S_FB location.
2. Measured at 0.31 * V1P0S.
3. VIN between 0V and V1P0S.
4. CPAD includes die capacitance only. No package parasitic included.

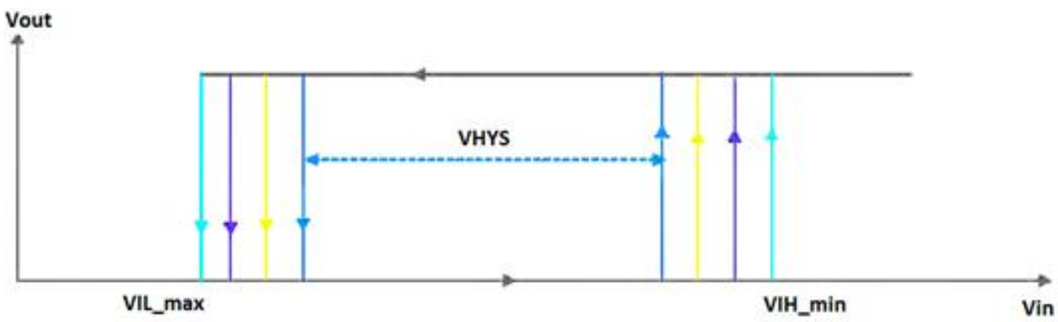


Figure 23: Definition of VHYS

Symbol	Parameter	Min	Typ	Max	Units	Notes	Val
Vmax	VDS max open drain buffer to accommodate bus ringing	-1.00		3.30	V		-
SR Fall Data/Alert		1.20		3.50	V/ns	Load: Rpu=64.9Ω	A
SR Rise Data/Alert		1.20		3.50	V/ns	Load: Rpu=64.9Ω	A

Table 32: SVID buffer AC Electrical Parameters

Slew Rate (SR) is measured between 0.7*V1P0S and 0.3*V1P0S. SR is measured at the output of the buffer; Rpu is connected to V1P0S as a load with no additional capacitance on the board. The slew rate is defined with VR buffer capacitance only.

11.5.2 VCLK Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units	Notes	Val
	VCLK frequency	13.3	25	26.25	MHz	1,4	A
Thigh	VCLK high time	-10%		+10%	% of 0.5 Tperiod	2,4	D
Tlow	VCLK low time	-10%		+10%	% of 0.5 Tperiod	2,4	D
Trise	VCLK rise time @VR Pad	0.25		3.0	ns	3	A
Tfall	VCLK fall time @VR Pad	0.25		3.0	ns	3	A
	Duty cycle	45		55	%	1,4	E,D

Table 33: VCLK AC Timing Parameters

NOTES:

1. Period and duty cycle are measured with respect to 0.5 * V1P0S.
2. High time is measured with respect to 0.7 * V1P0S. Low time is measured with respect to 0.3 * V1P0S.
3. Rise time is measured from 0.3*V1P0S – 0.7*V1P0S. Fall time is measured 0.7*V1P0S - 0.3*V1P0S.
4. Tperiod, Thigh, Tlow and Duty Cycle variation as a result of internal CPU Clock logic only. Additional variation may be introduced as a result of the Clock MB topology (like different Rpu values or MB impedance).

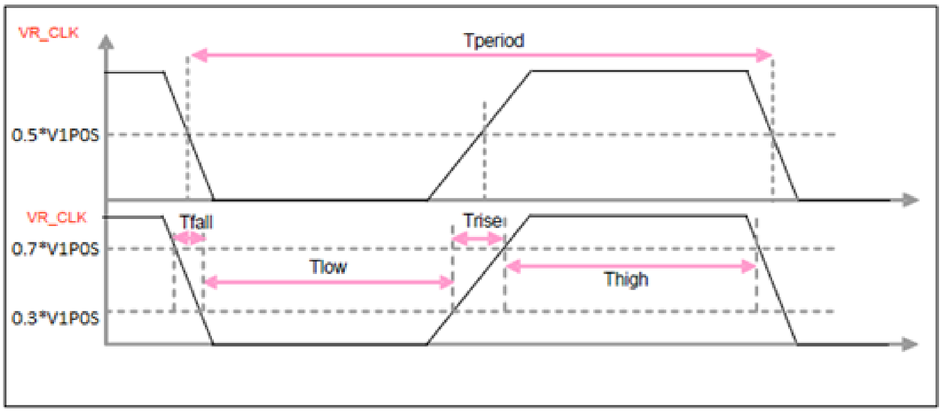


Figure 24: Measurement Points for VCLK

The SVID interface will have access only to the SVID registers. In case of dynamical content like the status registers the latching mechanism ensures not falling in meta-stability.

11.5.3 Data Sampling and Timing

Following SVID Bus platform timings have to be fulfilled

- Tco_max_VR clock to data delay = 12ns
- Tco_min_VR clock to data delay = 4ns
- Tsu_VR VDIO setup time at DA6021 = 7ns
- Thld_VR VDIO hold time at DA6021 = 14ns
- Tfly_min 0.3ns
- Tfly_max 1.5ns

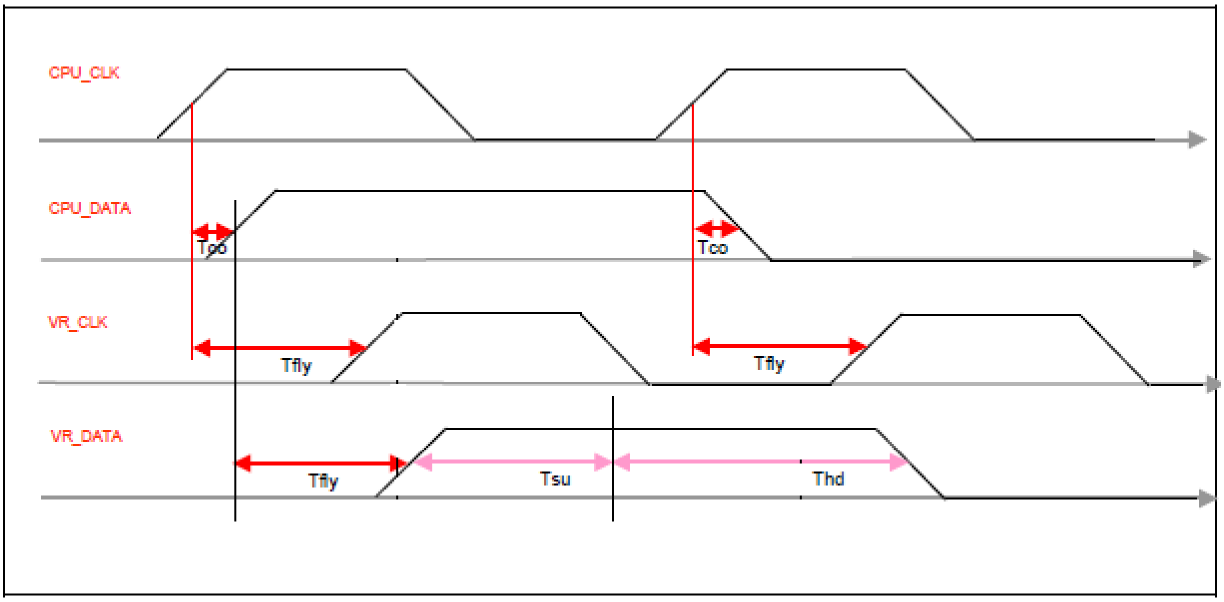


Figure 25: SoC Driving Timing Definition

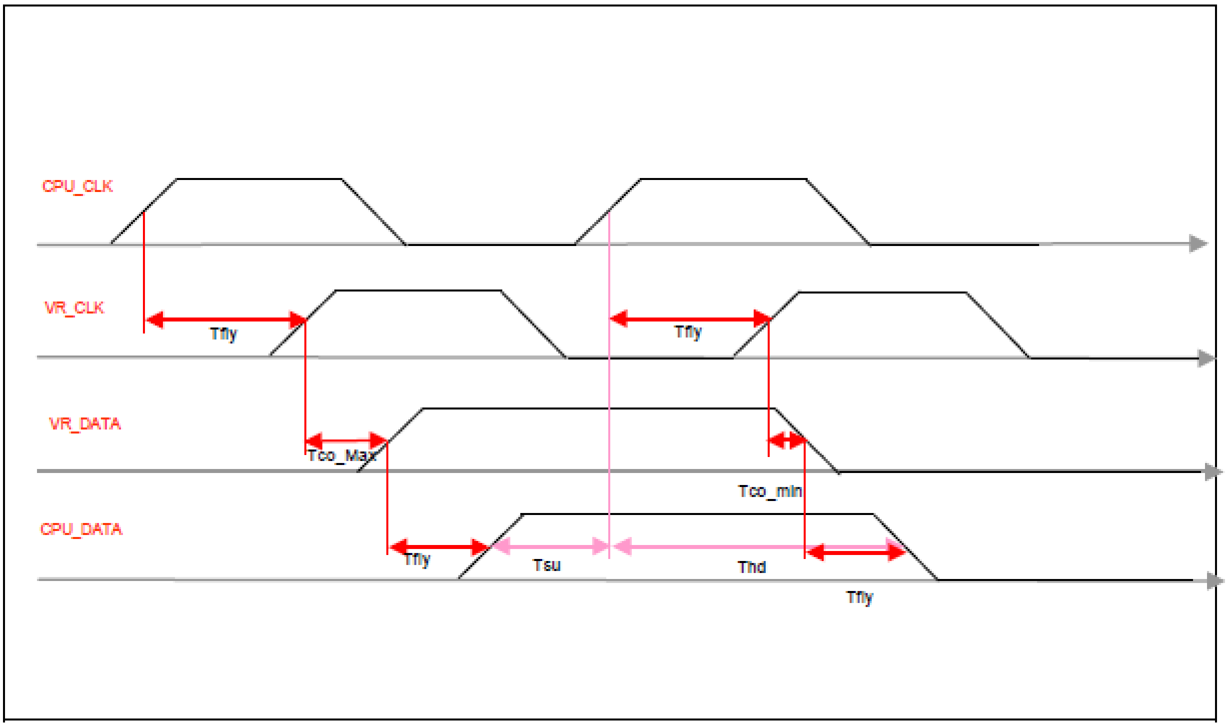


Figure 26: DA6021 Driving Timing Definition

11.5.4 SVID Command Set

VCC & VNN implement a subset of the full VR12/IMVP7 SVID protocol

#	Command	Master payload content	Slave payload content	Description
01h	SetVID-fast (Individual address & all call address)	VID code	NA	Applicable for VCC & VNN. Set the new VID target, VR Jumps to new VID target with controlled (up or down) slew rate programmed by the VR. When VR receives VID moving up command it will exit all low power states to the normal state to ensure the fastest slew to the new voltage. VR sets VR_settled bit and issues alert when VR has reached new VID target.
02h	SetVID-slow (Individual address & all call address)	VID code	NA	Applicable for VCC & VNN. Set the VID target, VR Jumps to new VID target with controlled slew rate (up or down) programmed by the VR. When VR receives VID moving up command it will exit all low power states to the normal state. VR sets VR_settled and issues alert when VR has reached new VID target.
03h	SetVID-decay (Individual address & all call address)	VID code	NA	Applicable for VCC & VNN. Sets the VID target, VR jumps to new VID target, but does not control the slew rate, the output voltage decays at a rate proportional to the load current. SetVID_decay is only used in VID down direction and implies VR goes to PS2 state. VR sets VR_settled but Alert line is not asserted for SetVID-decay
04h	SetPS	Byte indicating power status of voltage rail	NA	Only applicable for VCC. SoC sets the power state of the VR according to core P-state and C-state so that VCC VR controller can be configured to improve efficiency, especially at light load
05h	SetRegADR (Individual address only. NAK all call address)	Address of the index in the data table	NA	Sets the address pointer in the data register table. Typically the next command SetRegDAT is the payload that gets loaded into this address. However for multiple writes to the same address, only one SetRegADR is needed.
06h.	SetRegDAT (Individual address only. NAK all call address)	New data register contents	NA	Writes the contents to the data register that was previously identified by the address pointer with SetRegADR
07h	GetReg (Individual address only. NAK all call address)	Define which register	Specified register contents	Slave returns the contents of the specified register as the payload; The majority of the VR monitoring data is accessed through the GetReg command.

Table 34: SVID Supported Commands

11.5.5 SVID Register Set

#	Register	Description	Access	Note
0x00	Vendor ID	The vendor ID is defined by Intel . DA6021 returns the assigned vendor ID	Read only	
0x01	Product ID	Identifies the DA6021 with its specific number	Read only	
0x02	Product revision	This byte is slpit into the new release code (NRC[3:0]) in the high nibble and the minor revision code (MRC[3:0]) in the low nibble of this byte.	Read only	
0x06	Capability	current monitoring is supported	Read only	
0x10	Status_1	Data register read after the alert_B signal is asserted. Conveying the status of the VR.	Read only	
0x14	VCC/VNN Output Current, Imon (H)	Running 1 ms averaging (analog or digital), approximately 1 ms register update. 10 bits ADC, store MSB & 2nd MSB of the ADC output onto D[1..0] on this register	Read only	VCC in VCC registers VNN in VNN registers
0x15	VCC/VNN Output Current, Imon (L)	Running 1 ms averaging (analog or digital), approximately 1 ms register update. 10 bits ADC, store the 1st 8 LSB of the ADC output onto this register.	Read only	VCC in VCC registers VNN in VNN registers
0x1D	V1P0A/VDDQ Output Current, Imon (H)	Running 1 ms averaging (analog or digital), approximately 1ms register update, 10 bits ADC, store MSB & 2nd MSB of the ADC output onto D[1..0] on this register.	Read only	V1P0A in VCC regs VDDQ in VNN regs
0x1E	V1P0A/VDDQ Output Current, Imon (L)	Running 1 ms averaging (analog or digital), approximately 1ms register update, 10 bits ADC, store the 1st 8 LSB of the ADC output onto this register.	Read only	V1P0A in VCC regs VDDQ in VNN regs
0x1F	V1P05S Output Current, Imon (H)	Running 1 ms averaging (analog or digital), approximately 1ms register update, 10 bits ADC, store MSB & 2nd MSB of the ADC output onto D[1..0] on this register.	Read only	V1P05S in VCC regs
0x20	V1P05S Output Current, Imon (L)	Running 1 ms averaging (analog or digital), approximately 1ms register update, 10 bits ADC, store the 1st 8 LSB of the ADC output onto this register.	Read only	V1P05S in VCC regs
0x26	Vboot	Data register containing Vboot voltage. VR12 VID format, 0x97 = 1.0V	Read only	0x97 equals to 1.0V
0x2A	Slew	Slew rate control register		
0x2D	VCC/VNN Imon accuracy	Data register containing the Imon error in percentage. Binary Coded Decimal format in %, IE 10% = 0x0A. This data is used with the Imon register (0x14 & 0x15).	Read only	
0x2E	V1P0A/VDDQ Imon accuracy	Data register containing the Imon error in percentage. Binary Coded Decimal format in %, IE 10% = 0x0A. This data is used with the Imon register (0x1D & 0x1E)	Read only	
0x2F	V1P05S Imon accuracy	Data register containing the Imon error in percentage. Binary Coded Decimal format in %, IE 10% = 0x0A. This data is used with the Imon register (0x1F & 0x20)	Read only	
0x30	Vout max	This register is programmable by the master and sets the maximum VID the VR will support. If a higher VID code is received, the VR should respond with “Reject, not	Read/write	0xD3

#	Register	Description	Access	Note
		supported" acknowledge. VR12 VID data format. Must be programmed by MASTER during boot up sequence if a value other than default is desired. Offset (33h) does not effect Vout_max. IE VID+offset can be > Vout_max.		
0x31	VID setting	Data register containing currently programmed VID voltage. VID data format. Default is 00h, zero volts out, VR off.	Read/write	
0x32	PWR state	Register containing the current programmed power state. Default is 00h, normal power mode	Read/write	
0x33	Offset	Sets offset in VID steps added to the VID setting for voltage margining. Bit 7 is sign bit, 0=positive margin, 1= negative margin. Remaining 7 BITS are _B VID steps for the margin 2s complement. 00h= no margin. 01h=+1 VID step, 02h=+2 VID steps FFh=-1 VID step…	Read/write	
0x39	S0iX_SVID setting	Data register containing the VID voltage that is used to DECAY to when the SLP_S0IX_B is asserted and PLTRST_B de-asserted; The voltage ramps back to 31h using fast ramp set in VSLEW(2Ah) at de-assertion of SLP_S0IX_B	Read/write	

Table 35: SVID Supported Registers

Register Name		VENDOR_ID		Address	0x00 Page 2/3	Read	
					0x00		
MSB							LSB
R	R	R	R	R	R	R	R
VendorID[7:0]							
VendorID[7:0]		**0x2B**	identifies Dialog Semiconductor				

Register Name		PRODUCT_ID		Address	0x01 Page 2/3	Read	
					0x00		
MSB							LSB
R	R	R	R	R	R	R	R
ProductID[7:0]							
ProductID[7:0]		**0**	Identifies the product				

Register Name		**PRODUCT_REV**		Address	**0x02 Page 2/3**	Read	
					0x00		
MSB							LSB
R	R	R	R	R	R	R	R
ProductRev[7:0]							
ProductRev[7:0]		**0**	Identifies the VR stepping				

Register Name		**CAPABILITY**		Address	**0x06 Page 2/3**	Read	
				Reset Value	0x01		
MSB							LSB
R	R	R	R	R	R	R	R
Capability[7:0]							
Capability[7:0]		0 **1**	Current monitoring not supported Current monitoring supported				

ICCmax alert is issued from DA6021 to the SOC via the ALERT_B line of the SVID interface if the output current of VCC or VNN is considered to exceed the Imax threshold.When VCC and VNN are active,DA6021 measures and averages the output current and compares it with the alert threshold which is programmed to approximately 10% above Imax. This ensures proper operating and avoids invalid alerts due to process tolerances.

Register Name		**STATUS1**		Address	**0x10 Page 2/3**	Read	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R	R
Reserved					ICCmax Alert	Thermal Alert	VR settled
VR settled		**0** 1	VR is ramping VR is at target voltage				
Thermal Alert		**0** 1	Temperature ok Over-temperature detected				
ICCmax Alert		**0** 1	Normal current range, ICC < Imax (1ms averaging) Over-current detected, Imax ≤ ICC ≤ 1.3*Imax (1ms averaging)				

Register Name		**VBOOT**		Address	**0x26 Page 2/3**	Read	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R	R
VBOOT[7:0]							
VBOOT[7:0]		0..255	Defines the boot voltage VID, initial 0x97 = 1.0V				

Register Name	**SLEW**			Address	**0x2A Page 2/3**	Read/Write	
				Reset Value	0x10		
MSB							LSB
R	R	R/W	R/W	R	R	R	R/W
Reserved		SetVID_Fast		Reserved			SetVID_ Slow
SetVID_Slow		**0** 1	2.5mV/µs 5mV/µs				
SetVID_Fast		00 **01** 10 11	10mV/µs 20mV/µs 40mV/µs reserved				

Register Name	**Vout_Max**			Address	**0x30 Page 2/3**	Read/Write	
				Reset Value	0xD3		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SVID Max[7:0]							
SVID Max[7:0]		**0**..255	Defines the maximum allowed VID voltage. VID values above this threshold won't be accepted and a message "rejected, not supported" will be sent out				

Register Name	**VID_Setting**			Address	**0x31 Page 2/3**	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
VID setting[7:0]							
VID setting[7:0]		**0**..255	Defines the output voltage according to the VID coding				

Register Name	**PWR_State**			Address	**0x32 Page 2/3**	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
VID setting[7:0]							
PWR state[7:0]		**0**..3	0x00 normal mode 0x01 light load 0x02 very light load 0x03 ultra light mode 0x04 .. 0xFF not supported, error message is sent out				

Register Name	Offset		Address	0x33 Page 2/3	Read/Write		
			Reset Value	0x00			
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Offset[7:0]							
Offset[7:0]	**0**..0xFF	0xFE -2 VID steps 0xFF -1 VID step 0x00 no margin 0x01 +1 step 0x02 +2 steps … Sets offset in VID steps added to the VID setting for voltage margining. Values in 2s complement					

11.5.6 VID DAC Table

VID 7	VID 6	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	Voltage	Accuracy
0	0	0	0	0	0	0	x	OFF	NA
0	0	0	0	0	0	1	x	0.26V	
0	0	0	0	0	1	0	x	0.27V	
...									
0	0	1	0	1	1	1	x	0.48V	N/A
0	0	1	1	0	0	0	X	0.49V	N/A
0	0	1	1	0	0	1	X	0.50V	+/- 8mV
0	0	1	1	0	1	0	X	0.51V	+/- 8mV
...									
0	1	0	0	1	1	0	x	0.63V	+/- 8mV
0	1	0	0	1	1	1	X	0.64V	+/- 8mV
0	1	0	1	0	0	0	X	0.65V	+/- 5mV
0	1	0	1	0	0	1	X	0.66V	+/- 5mV
...									
1	0	0	1	0	0	1		0.98V	+/- 5mV
1	0	0	1	0	1	0	X	0.99V	+/- 5mV
1	0	0	1	0	1	1	X	1.00V	+/- 0.5% VID
1	0	0	1	1	0	0	X	1.01V	+/- 0.5% VID
...									
1	0	1	1	1	1	0	X	1.19V	+/- 0.5% VID
1	0	1	1	1	1	1	X	1.20V	+/- 0.5% VID
1	1	0	0	0	0	0	X	1.21V	N/A
1	1	X	X	X	X	X	X	>1.21V	N/A

Table 36: VID Values

11.5.7 Low Power State Control Signals

SLP_S0iX_B is asserted low when SoC goes into S0iX state. When S0iX_B signal is held low, VNN, V1P0_A, V1P8_A and VDDQ are entering a low power state. V1P0SX,V1P05S, V1P2SX, V1P8SX, VHDMI, VBUS, VDDQ_VTT and V2P85SX are switched off.

11.6 Power Supplies

11.6.1 DC/DC Buck Regulator VCC

The BUCK_CORE converter is a high efficiency synchronous quad phase step down regulator operating at a high frequency (3 MHz) supplying a voltage (VCC) of 0.5 … 1.2V at maximum 8000mA. This buck regulator has the ability to dynamically change its output voltage setting to per SoCs frequency-power requirements. The output voltage is controlled using the SVID interface.

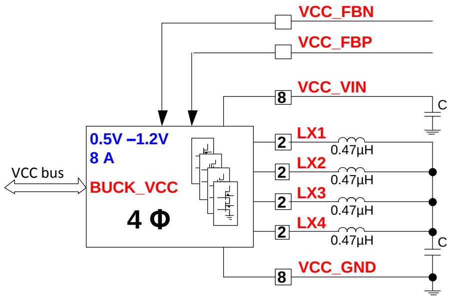


Figure 27: VCC Block Diagram

11.6.1.1 VCC Current

The SoC has the ability to increase the core frequency during burst mode (achieving exceptional performance) when the system environment is conducive. As long as the thermal and power budget allows, the current of the VCC voltage rail can be more than twice the normal mode value.

Imax = 8000mA

11.6.1.2 Power States

PS0 – active state:

DA6021 VCC voltage rail can handle up to 8A peak current for a duration of several seconds before it reaches the maximum operational temperature of DA6021. The regulator automatically switches between synchronous PWM and asynchronous PFM mode depending on the load.

At usage workloads, VCC current is typically in the range of 200mA to 1500mA

PS1:

N/A

PS2 – C6 at S0idle

When the SoC enters the C6 state it sends a SetVID_decay to C6 VID voltage command. DA6021 sets the output voltage to the C6 level, without discharging the output capacitors. In PS2 mode VCC regulator turns off all unnecessary functional blocks for minimal power dissipation. Exiting PS2 mode can either be achieved after receiving a SetPS to PS0 or SetVID_slow/fast to a value equal or higher VID voltage rail. The power state transition delay time is ≤ 5µs

In this power saving mode the VCC buck supports up to 200mA without catastrophic failure.

PS3 – C6 at S0ix

The SoC sends a SVID command SetVID_decay with 0V to enter the PS3 mode. DA6021 switches off all unnecessary functional blocks minimizing the quiescent current. When detecting an exit from S0ix state, the SoC sends SetVID_fast/slow and DA6021 recovers VCC to the operating voltage level.

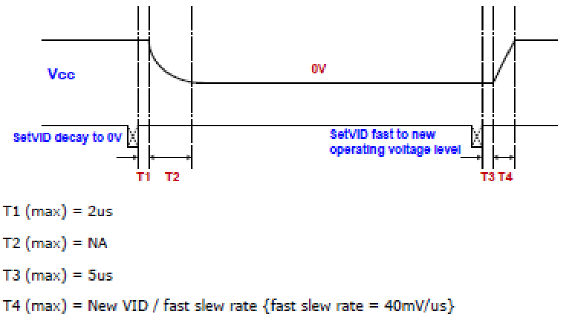


Figure 28: VCC Timings

11.6.1.3 Electrical Characteristics VCC

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Val
VCC_IN	Input Voltage		2.7		4.5	V	-
Cin	at VCC_IN			4 x 4.7		µF	-
Cout				6 x 47		µF	-
ESR of output capacitor				6 @ 47µF		mΩ	-
ESL of output capacitor				1.6 @ 3MHz		nH	-
L_BUCK	inductor value		-20%	4x0.47	+20%	µH	-
L_R	inductor DC resistance				48	mΩ	-
VCC	Output Voltage	IOUT= Imax	0.50		1.2	V	A
VCC	Output Accuracy		See chapter 0				A
F_BUCK	Frequency of operation	Tablet		3		MHz	A
Transient load current profile		1000-8000mA 25-7000mA		200 200		ns ns	-
Transient droop[1]		1000-8000mA 25-7000mA			40	mV	E
Transient overshoot[2]		8000-1000mA 7000-25mA			40	mV	E
Ton	Turn on time				2	ms	E
Toff	Turn off time	Vout down to 0.5V			20	µs	D
Rpd	Discharge impedance	0.5V down to 0V			20	Ω	A
IQ_ON	Quiescent Current in On Mode	No load			200	µA	E
Normal Mode – Synchronous rectification (PWM)							
Maximum Output	Current (Imax)		8000			mA	D
ILIMIT	Current limitation	Cycle by cycle	1.3*Imax			mA	A*
Boot up voltage for V_{CC} V_{BOOT}				1.1		V	D,E
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout		Typical BOM environment		See Figure 29			D,E, A*[3]

[1] Including DC accuracy, ripple and load regulation
[2] Including DC accuracy, ripple and load regulation
[3] RDSON measurement on ATE

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	Val
Sleep Mode – Pulse skipping (PSK)						
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout			See Figure 29			D,E, A*

Table 37: Electrical Parameters for BUCK_VCC

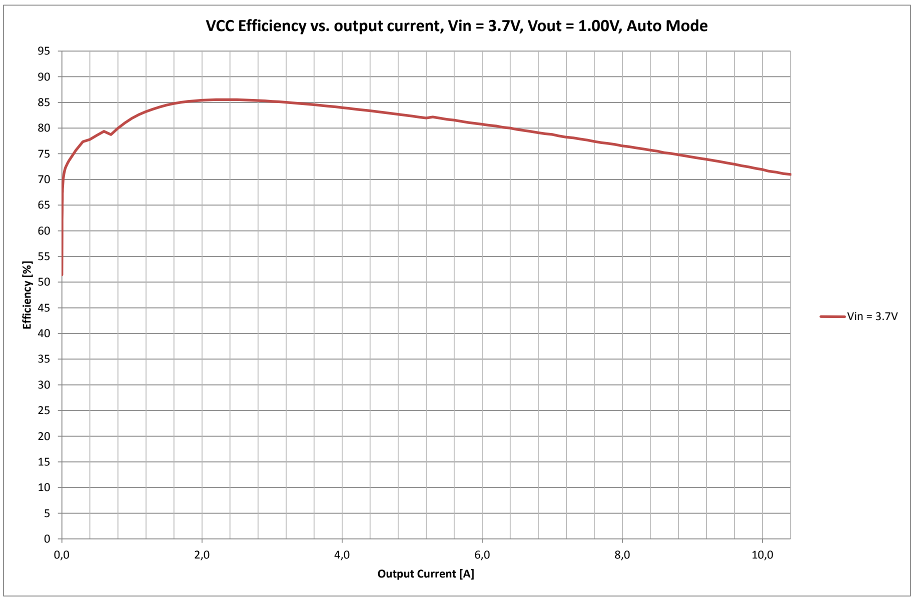


Figure 29: VCC Efficiency

11.6.2 DC/DC Buck Regulator VNN

The BUCK_VNN converter is a high efficiency synchronous step down regulator operating at a high frequency (3 MHz) supplying a voltage (VNN) of 0.5 … 1.2V at maximum 8000mA. This buck regulator has the ability to dynamically change its output voltage setting to per SoC's frequency-power requirements. The output voltage is controlled using the SVID interface.

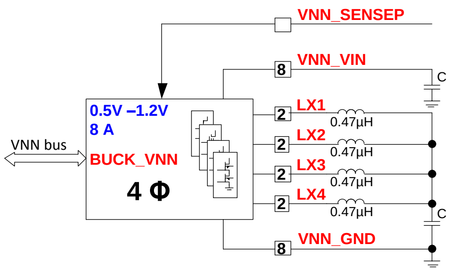


Figure 30: Buck VNN Block Diagram

11.6.2.1 VNN Current

The SoC has the ability to increase the core frequency during burst mode (achieving exceptional performance) when the system environment is conducive. As long as the thermal and power budget allows, the current of the VCC voltage rail can be more than twice the normal mode value.

IMAX = 8000mA

11.6.2.2 Power States

Active state:

DA6021 VNN voltage rail can handle up to 8A peak current for duration of several seconds until it would reach the maximum operational temperature of DA6021. The regulator automatically switches between synchronous PWM and asynchronous PFM mode depending on the load.

At usage workloads, VNN current is typically in the range of 50mA to 500mA

S0ix:

When The SoC enters the S0ix state, SLP_S0ix is held low. DA6021 turns the VNN buck regulator into low power mode and disables all un-necessary blocks, reducing the power requirements. PMIC exits this power saving mode within 5µs after SoC asserts the SLP_S0ix signal to high.

Typical current requirements for S0ix mode are 7mA .. 20mA. However this power saving mode supports up to 200mA maximum current without catastrophic failures.

11.6.2.3 Electrical Characteristics VNN

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Val
VNN_IN	Input Voltage		2.7		4.5	V	-
Cin	at VNN_IN			4 x 4.7		µF	-
Cout			6 x 22			µF	-
ESR of output capacitor				6 @ 22µF		mΩ	-
ESL of output capacitor				1.6 @ 3MHz		nH	-
L_BUCK	inductor value		-20%	4x0.47µ	+20%	µH	-
L_DCR	inductor DC resistance				48	mΩ	-
VNN	Output Voltage	IOUT= Imax	0.50		1.2	V	A
VNN	Output Accuracy			See chapter 0			A
F_BUCK	Frequency of operation			3		MHz	A
Transient load current profile		2900-5600mA		200		ns	-

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Val
		50-2750mA		200		ns	
Transient droop[4]		2900-5600mA 50-2750mA			40	mV	E
Transient overshoot[5]		5600-2900mA 2750-50mA			40	mV	E
Ton	Turn on time				2	ms	E
Toff	Turn off time	Vout .. 0.5V			20	µs	D
Rpd	Discharge impedance	0.5V ..0V			20	Ω	A
IQ_ON	Quiescent Current in ON Mode				200	µA	A
Normal Mode – Synchronous rectification (PWM)							
Maximum Output Current (Imax)			8000			mA	D
ILIMIT	Current limitation	Cycle by cycle	1.3*Imax			mA	A*
Boot up voltage for V_{NN} V_{BOOT}				1.1		V	D,E
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 31			D,E, A*[6]
Sleep Mode – Pulse skipping (PSK)							
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 31			D,E, A*

Table 38: Electrical Parameters for BUCK_VNN

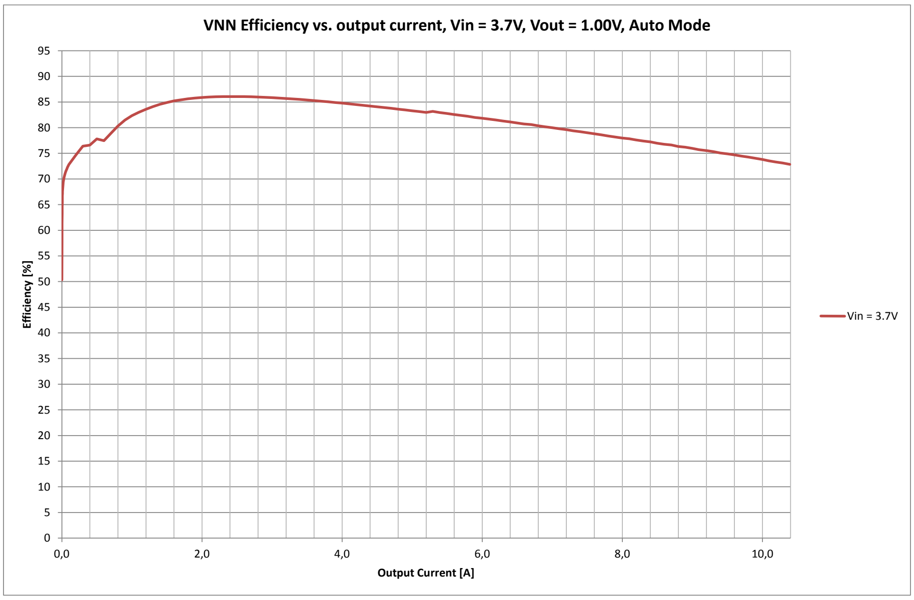


Figure 31: VNN Efficiency

[4] Including DC accuracy, ripple and load regulation
[5] Including DC accuracy, ripple and load regulation
[6] RDSON measurement on ATE

11.6.3 DC/DC Buck Regulator V1P0A

The high efficiency buck regulator supplies the USB sus, clock, CFIO and the V1P0S power rails of the SoC. This power rail is also capable of supplying the pass device of the push pull source for the DDR3 address line termination.

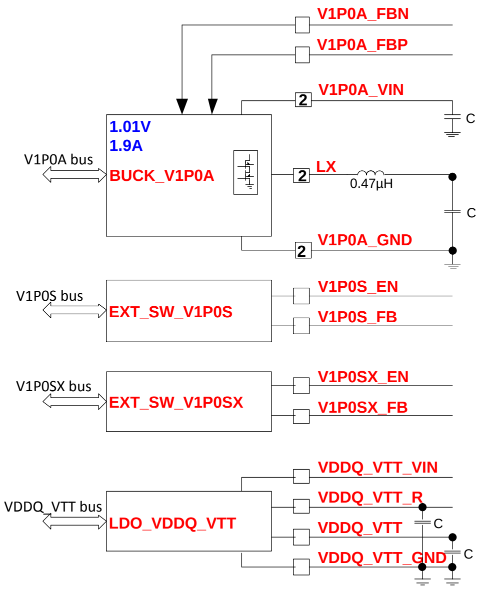


Figure 32: V1P0A Power Rail Block Diagram

To allow for voltage drops on the PCB it is possible to program the output voltage to either 1.01V or 1.05V, see register below.

The maximum output current of the 1P0A buck regulator is 1900mA

11.6.3.1 Power States

Active State:

DA6021 V1P0A voltage rail can handle up to 1.9A. Even though the average current is in the range of 50mA to 350mA. Optimized efficiency is achieved from 50mA to 500mA. Automatically switching from PWM to PFM mode achieves the best power efficiency.

S0ix State:

When the SoC enters the S0ix state, SLP_S0ix is held low. DA6021 turns the V1P0A buck regulator into low power mode and disables all un-necessary blocks, reducing the power requirements. DA6021 exits this power saving mode within 5µs after SoC asserts the SLP_S0ix signal to high.

Typical current requirements for S0ix mode are 5mA .. 30mA, this power saving mode supports up to 200mA maximum current without catastrophic failures.

S3 & S4 State:

In S3 or S4 state the average current of V1P0A is expected to be ~2.6mA and the buck converter is in low power mode.

11.6.3.2 Electrical Characteristics V1P0A

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Val
V1P0A_VIN	Input Voltage		2.7		4.5	V	-
Cin	at V1P0A_IN			2 x 4.7		µF	-
Cout	≥ 80µF			4 x 22 or 2 x 47		µF	-
ESR of output capacitor				6 @ 22/47µF		mΩ	-
ESL of output capacitor				1.6 @ 3MHz		nH	-
L_BUCK	inductor value		-20%	0.47	+20%	µH	-
L_DCR	inductor resistance				48	mΩ	-
V1P0A	Output Voltage	IOUT= Imax		1.01±2%		V	A
F_BUCK	Frequency of operation			3		MHz	A
Transient load current profile		5-250mA	200			ns	-
Transient droop[7]		75-1820mA 5-250mA			40	mV	E
Transient overshoot[8]		1820-75mA 250-5mA			40	mV	E
Ton	Turn on time				2	ms	E
Rpd	Discharge impedance	Vout ..0V			20	Ω	A
IQ_ON	Quiescent Current in On Mode				50	µA	E
Normal Mode – Synchronous rectification (PWM)							
Maximum Output Current (Imax)			1900			mA	D
ILIMIT	Current limitation		1.3*Imax			mA	A*
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 33			D,E, A*[9]
Sleep Mode – Pulse skipping (PSK)							
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 33			D,E, A*

Table 39: Electrical Parameter for BUCK_V1P0A

[7] Including DC accuracy, ripple and load regulation
[8] Including DC accuracy, ripple and load regulation
[9] RDSON measurement on ATE

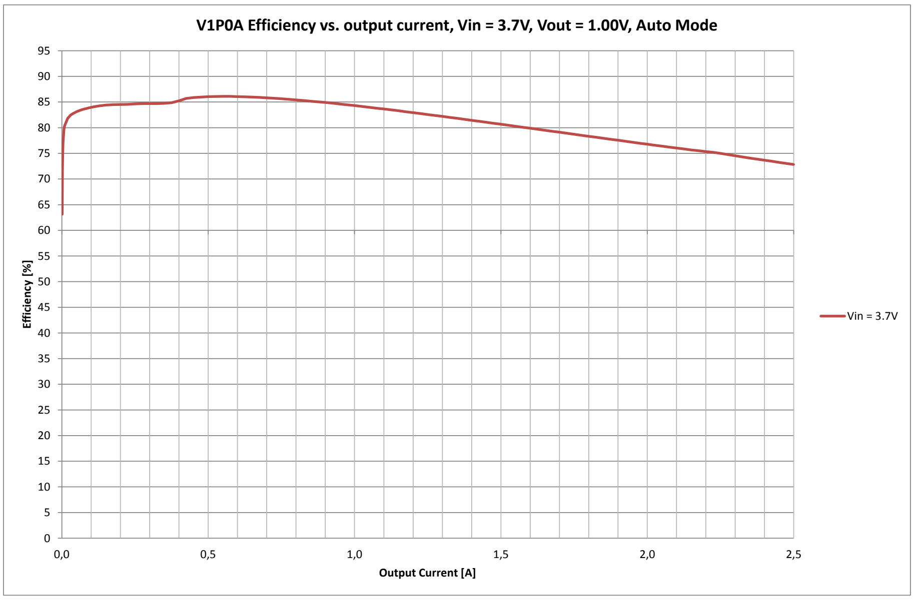


Figure 33: V1P0A Efficiency

11.6.3.3 V1P0A Registers

Register Name		V1P0A_CTRL		Address	0x55 Page 1	Read/Write	
				Reset Value	0x60		
MSB							LSB
R/W	R/W	R/W	R	R	R/W	R/W	R/W
V1P0A_VSEL			reserved		NoS0iX	V1P0A_SEL	V1P0A_EN
V1P0A_EN		**0** 1	V1P0A off V1P0A on				
V1P0A_SEL		**0** 1	V1P0A controlled by SUSPWRDNACK according to sequencing V1P0A controlled by V1P0A_CTRL.V1P0A_EN Regardless of V1P0A_EN and V1P0A_SEL, V1P0A is disabled when SUSPWRDNNACK is de-asserted means high				
NoS0iX		**0** 1	V1P0A active state or S0iX state is determined by SLP_S0iX_B V1P0A only operate at active state, no S0iX, regardless of SLP_S0iX_B				
V1P0A_VSEL		000 001 010 **011** 100 101 110 111	0.900V 0.950V 1.000V **1.010V** 1.020V 1.030V 1.050V 1.100V				

V1P0A_CTRL. V1P0A_SEL	V1P0A_CTRL. V1P0A_EN	SUSPWRDNACK	V1P0A
1	0	0	Off
1	1	0	On
x	x	1	Off

Table 40: V1P0A Truth Table

11.6.3.4 V1P0A Subsystem

V1P0S:

This voltage rail powers the SoC graphic, display & DDR3 I/O, MIPI, clock and further functions. The current requirement of this voltage rail is 410mA and requests an external switch providing this power rail to the SoC. DA6021 provides a control signal named V1P0S_EN supplied by V5P0S.When this signal is asserted (high), the slew rate is controlled in order to limit the inrush current drawn via the external N-channel FET. The V1P0S_EN signal is derived from SLP_S3_B signal sent out by the SoC.

Register Name		V1P0S_CTRL		Address	0x56 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R/W	R/W
reserved						V1P0S_SEL	V1P0S_EN
V1P0S_EN		**0** 1	V1P0S off V1P0S on				
V1P0S_SEL		**0** 1	V1P0S controlled by SLP_S3_B according to sequencing V1P0S controlled by V1P0S_CTRL.V1P0S_EN bit Regardless of V1P0S_EN and V1P0S_SEL, V1P0S_EN is low when SLP_S3_B is asserted, means low				

V1P0S_CTRL. V1P0S_SEL	V1P0S_CTRL. V1P0S_EN	SLP_S3_B	V1P0S_EN
1	0	1	Low
1	1	1	High
x	x	0	Low

Table 41: V1P0S_EN Truth Table

V1P0S external N-channel power switch parameters:

Rdson (Vgs=4V)	10-49mohm
Input capacitance, Ciss	700-2640pF
Output capacitance, Coss	150-530pF
Reverse transfer capacitance, Crss	85-465pF

V1P0SX:

This voltage rail powers the SoC display & DDR3 I/O, PCIe and further functions. The current requirement of this voltage rail is 916mA and requests an external switch providing this power rail to the SoC. DA6021 provides a control signal named V1P0SX_EN supplied by V5P0S.When this signal is asserted (high), the slew rate is controlled in order to limit the inrush current drawn via the external N-channel FET. This signal is derived from SLP_S0iX_B signal sent out by the SoC.

Register Name	V1P0SX_CTRL			Address	0x57 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R/W	R/W
Reserved						V1P0SX_SEL	V1P0SX_EN
V1P0SX_EN		**0** 1	V1P0SX off V1P0SX on				
V1P0SX_SEL		**0** 1	V1P0SX controlled by SLP_S0iX_B according to sequencing V1P0SX controlled by V1P0SX_CTRL.V1P0SX_EN bit Regardless of V1P0SX_EN and V1P0SX_SEL, V1P0SX_EN is high when SLP_S3_B is asserted, means low				

V1P0SX_CTRL. V1P0SX_SEL	V1P0SX_CTRL. V1P0SX_EN	SLP_S3_B	V1P0SX_EN
1	0	1	High
1	1	1	Low
x	x	0	High

Table 42: V1P0SX_EN Truth Table

V1P0SX external N-channel power switch parameters:

Rdson (Vgs=4V)	10-22mohm
Input capacitance, Ciss	750-2640pF
Output capacitance, Coss	150-530pF
Reverse transfer capacitance, Crss	85-465pF

VDDQ_VTT:

The VDDQ_VTT power rail is a push-pull LDO capable to source and sink maximum 325mA. VDDQ_VTT is ½ of VDDQ and its pass device is sourced by V1P0_A in order to reduce the overall power dissipation in the system.

Register Name	VDDQ_VTT_CTRL			Address	0x58 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R/W	R/W
Reserved						VDDQ_VTT_SEL	VDDQ_VTT_EN
VDDQ_VTT_EN		**0** 1	VDDQ_VTT off VDDQ_VTT on				
VDDQ_VTT_SEL		**0** 1	VDDQ_VTT controlled by SLP_S0iX_B according to sequencing VDDQ_VTT controlled by VDDQ_VTT_CTRL.VDDQ_VTT_EN bit Regardless of VDDQ_VTT_EN and VDDQ_VTT_SEL, VDDQ_VTT is disabled when SLP_S3_B is asserted, means low				

VDDQ_VTT_CTRL.		SLP_S3_B	VDDQ_VTT
VDDQ_VTT_SEL	VDDQ_VTT_EN		
1	0	1	Off
1	1	1	On
x	x	0	Off

Table 43: VDDQ_VTT Truth Table

VDDQ_VTT electrical specification:

Symbol	Parameter	Min	Typ	Max	Unit	Notes/Condition	Val
Input requirement							
Vin (DDR3 LP)	Main input voltage VDDQ_VTT_VIN		1.01		V	Supplied by V1P0A	-
Vin (DDR3 L)	Main input voltage VDDQ_VTT_VIN		1.35		V	Supplied by VDDQ	-
Cin	VDDQ_VTT_IN		100		nF		-
Output requirement							
Vnom	Nominal output voltage		VDDQ/2		V	VDDQ used to generate VDDQ_VTT_VREF	-
Vtol	Output voltage tolerance	-2		+2	%	Of input supply voltage	A
Cout	Output capacity		10		µF		-
Iout-DC	Output load current	±325			mA		D,E
Transient load current	0-240mA	200	200		ns		E
IQSC	Quiescent current VDDQ_VTT_VIN			200	µA	Iout-DC = 0mA	A
PSRR	Power supply rejection ratio	40	60		dB	Noise = 1 Vpp, 1-10kHz, ½ Iout-DC	D,E
Vnoise	Output Noise		60	100	µVRMS	BW = 10-100kHz, ½ Iout	D,E

Table 44: Electrical Parameter for VDDQ_VTT

11.6.4 DC/DC Buck Regulator V1P05S

The high efficiency buck regulator supplies the L2 SRAM of the SoC.

The maximum output current of the 1P05S buck regulator is 474mA

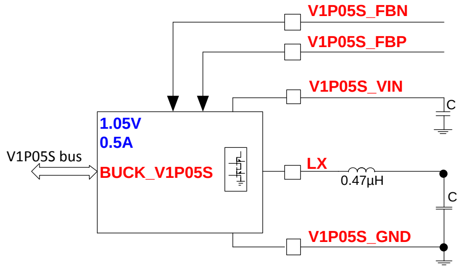


Figure 34: Buck V1P05S Block Diagram

11.6.4.1 Power States

Active state:

DA6021 V1P05S voltage rail can handle up to 474mA max current. Its usual average current workload is at 1mA to 50mA, but thermally able to handle 474mA in peaks. Optimized efficiency is achieved from 1mA to 50mA. Automatically switching from PWM to PFM mode achieves the best power efficiency.

S0ix State:

When the SoC enters the S0ix state, SLP_S0ix is held low. DA6021 turns the V1P0S buck regulator off except V1P05S.V1P05S_EN bit is set. DA6021 exits S0iX state while asserting SLP_S0iX_B to high and enabling V1P05S buck regulator and ramps the voltage to 1.05V±5% within 60µs.

11.6.4.2 Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Val
V1P05S_VIN	Input Voltage		2.7		4.5	V	-
Cin	at V1P05S_IN			4.7		µF	-
Cout				2 x 22		µF	-
ESR of output capacitor				6 @ 22µF		mΩ	-
ESL of output capacitor				1.6 @ 3MHz		nH	-
L_BUCK	inductor value		-20%	0.47	+20%	µH	-
L_DCR	inductor resistance				48	mΩ	-
V1P05S	Output Voltage	IOUT= Imax		1.05±2%		V	A
F_BUCK	Frequency of operation			3		MHz	A
Transient load current profile		0-740mA		200		ns	-
Transient droop[10]		0-740mA			53	mV	E
Transient overshoot[11]		740-0mA			53	mV	E
Ton	Turn on time				2	ms	E
Rpd	Discharge impedance	Vout .. 0V			20	Ω	A
IQ_ON	Quiescent Current in On Mode				50	µA	E
Normal Mode – Synchronous rectification (PWM)							
Maximum Output Current (Imax)		Cycle by cycle	475			mA	D
ILIMIT	Current limitation		900			mA	A*
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 35			D,E, A*[12]
Sleep Mode – Pulse skipping (PSK)							
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 35			D,E, A*

Table 45: Electrical Parameter for BUCK_V1P05S

[10] Including DC accuracy, ripple and load regulation
[11] Including DC accuracy, ripple and load regulation
[12] RDSON measurement on ATE

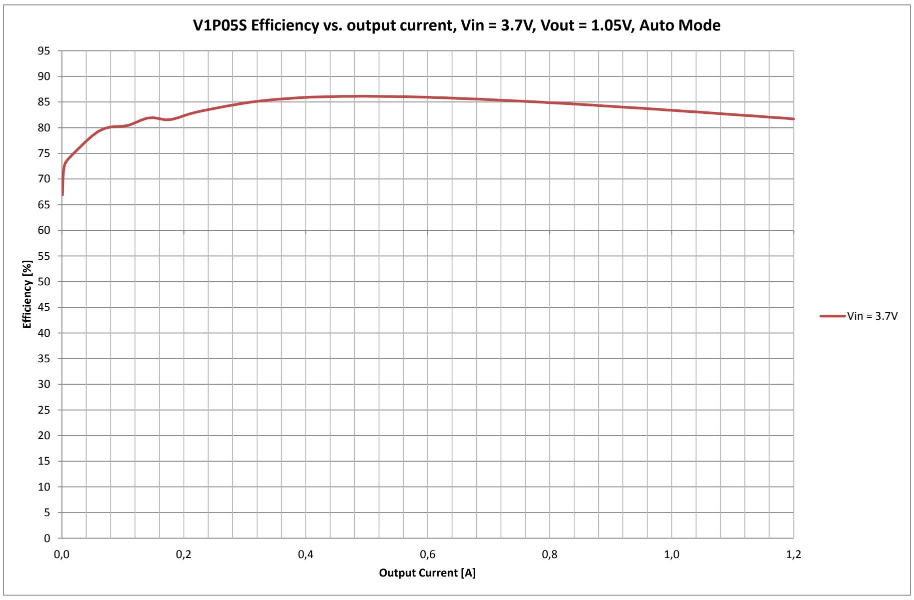


Figure 35: V1P05S Efficiency

11.6.4.3 V1P05S registers

Register Name		V1P05S_CTRL		Address	0x59 Page 1	Read/Write	
				Reset Value	0xA8		
MSB							LSB
R/W	R/W	R/W	R	R	R	R/W	R/W
V1P05S_VSEL			V1P05SVSEL_S0iX		NoS0iX	V1P05S_SEL	V1P05S_EN

V1P05S_EN	**0** 1	V1P05S off V1P05S on
V1P05S_SEL	**0** 1	V1P05S controlled by SLP_S0iX_B according to sequencing V1P05S controlled by V1P05S_CTRL.V1P05S_EN Regardless of V1P05S_EN and V1P05S_SEL, V1P05S is disabled when SLP_S3_B is asserted, means low
NoS0iX	**0** 1	V1P05S active determined by SLP_S0iX_B V1P05S active, regardless of SLP_S0iX_B
V1P05SVSEL_S0iX	 00 **01** 10 11	Output voltage in S0iX mode 0.60V **0.65V** 0.70V Nominal voltage (1.05V)
V1P05S_VSEL	000 001 010 011 100 **101** 110 111	0.945V 0.998V 1.020V 1.030V 1.040V **1.050V** 1.103V 1.115V

V1P05S_CTRL.		SLP_S3_B	V1P05S
V1P05S_SEL	V1P05S_EN		
1	0	1	Off
1	1	1	On
x	X	0	Off

Table 46: V1P05S Truth Table

11.6.5 DC/DC Buck Regulator V1P8_A

The high efficiency buck regulator supplies 1.8V I/Os, USB, V1P8U, V1P8S and V1P8SX.The maximum output current of the 1P8A buck regulator is 1627mA

11.6.5.1 Power States

Active State:

DA6021 V1P8A voltage rail can handle up to 1627mA max current. The usual average current workload is at 8mA to 260mA, but thermally able to handle 1627mA in peaks. Optimized efficiency is achieved from 8mA to 260mA. Automatically switching from PWM to PFM mode achieves the best power efficiency.

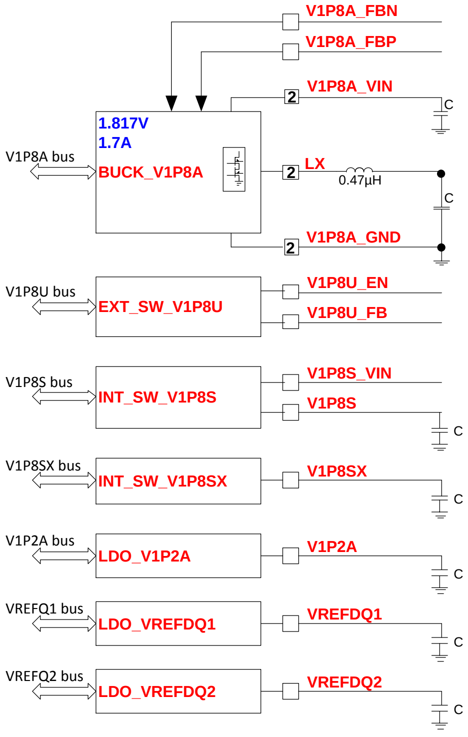


Figure 36: Buck V1P8A Power Rail Block Diagram

S0ix State:

When the SoC enters the S0ix state, SLP_S0ix is held low. DA6021 turns the V1P8A buck regulator into low power mode and disables all un-necessary blocks, reducing the power requirements. DA6021 exits this power saving mode within 5µs after SoC asserts the SLP_S0ix signal to high.

S3 & S4 States:

In S3 & S4 mode the average current of V1P8A is expected to be 4mA & 25µA.

11.6.5.2 Electrical Characteristics V1P8A

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	ATE test
V1P8A_VIN	Input Voltage		2.7		4.5	V	-
Cin	at V1P8A_IN			4.7		µF	-
Cout				2 x 22		µF	-
ESR of output capacitor				6 @ 22µF		mΩ	-
ESL of output capacitor				1.6 @ 3MHz		nH	-
L_BUCK	inductor value		-20%	0.47	+20%	µH	-
L_DCR	inductor resistance				48	mΩ	-
V1P0A	Output Voltage	IOUT= Imax		1.817±2%		V	A
F_BUCK	Frequency of operation			3		MHz	A
Transient load profile		0-861mA			250	ns	-
Transient droop[13]		0-861mA			73	mV	E
Transient overshoot[14]		861-0mA			73	mV	E
Ton	Turn on time				2	ms	E
Rpd	Discharge impedance	Vout .. 0V			20	Ω	A
IQ_ON	Quiescent Current in On Mode				50	µA	E
Normal Mode – Synchronous rectification (PWM)							
Maximum Output Current (Imax)			1627			mA	D
ILIMIT	Current limitation	Cycle by cycle	1.3*Imax			mA	A*
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 37			D,E, A*[15]
Sleep Mode – Pulse skipping (PSK)							
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 37			D,E, A*

Table 47: Electrical Parameter for BUCK_V1P8A

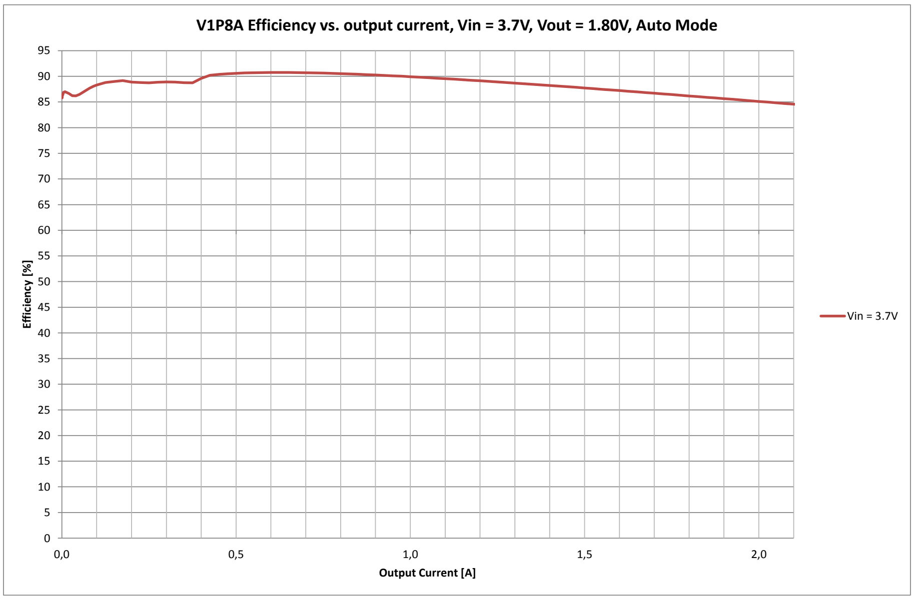


Figure 37: V1P8A Efficiency

[13] Including DC accuracy, ripple and load regulation
[14] Including DC accuracy, ripple and load regulation
[15] RDSON measurement on ATE

11.6.5.3 V1P8A Registers

Register Name		V1P8A_CTRL		Address	0x5A Page 1	Read/Write	
				Reset Value	0x60		
MSB							LSB
R/W	R/W	R/W	R	R	R/W	R/W	R/W
V1P8A_VSEL			reserved		NoS0iX	V1P8A_SEL	V1P8A_EN

V1P8A_EN	**0** 1	V1P8A off V1P8A on
V1P8A_SEL	**0** 1	V1P8A controlled by SUSPWRDNACK according to sequencing V1P8A controlled by V1P8A_CTRL.V1P8A_EN bit Regardless of V1P8_EN and V1P8A_SEL, V1P8A is disabled when SUSPWRDNACK is de-asserted, means high
NoS0iX	**0** 1	V1P8A active determined by SLP_S0iX_B V1P8A active regardless of SLP_S0iX_B
V1P8A_VSEL	000 001 010 **011** 100 101 110 111	1.620V 1.710V 1.800V **1.817V nominal voltage** 1.836V 1.854V 1.890V 1.980V

V1P8A_CTRL. V1P8A_SEL	V1P8A_CTRL. V1P8A_EN	SUSPWRDNACK	V1P8A
1	0	0	Off
1	1	0	On
x	x	1	Off

Table 48: V1P8A Truth Table

11.6.5.4 V1P8A Subsystems

V1P8U:

This power rail is primarily to supply LPDDR2 or LPDDR3 RAMs. DA6021 provides a control signal V1P8U_EN_B supplied by VSYS and derived from SLP_S4_B sent out by the SoC. When V1P8U_EN_B is asserted low, the signal slew rate is controlled to limit the inrush current when the external P-channel FET is turned on. The current of this power rail is maximum 355mA

Register Name		V1P8U_CTRL		Address	0x5B Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R/W	R/W
Reserved						V1P8U_SEL	V1P8U_EN

V1P8U_EN	**0** 1	V1P8U off V1P8U on
V1P8U_SEL	**0** 1	V1P8U controlled by SLP_S4_B according to sequencing V1P8U controlled by V1P8U_CTRL.V1P8U_EN bit Regardless of V1P8U_EN and V1P8U_SEL, V1P8U_EN_B is high when SLP_S4_B is asserted, means low

V1P8U_CTRL. V1P8U_SEL	V1P8U_CTRL. V1P8U_EN	SLP_S4_B	V1P8U_EN_B
1	0	1	High
1	1	1	Low
x	x	0	High

Table 49: V1P8U_EN_B Truth Table

V1P8U external P-channel power switch parameters:

Rdson (Vgs=1.8V)	50-97mohm
Input capacitance, Ciss	750-2315pF
Output capacitance, Coss	150-530pF
Reverse transfer capacitance, Crss	100-465pF

V1P8S:

The maximum current of this power rail is defined to 145mA, sourcing the SoC, USB PHY, UICC SIM … DA6021 controls this power rail while deriving the information from SoC SLP_S3_B signal and switching the rail internally. The typical RDSon value of this internal switch is 170mΩ

Description	Value [max, mΩ]	Val
Input power path board resistance	10	-
Output power path board resistance	20	-
Input, output rails wirebond & internal FET RDS-ON	242	A,D,E

Table 50: V1P8S Power Switch Specification

Register Name	V1P8S_CTRL			Address	0x5C Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R/W	R/W
Reserved						V1P8S_SEL	V1P8S_EN
V1P8S_EN	**0** 1	V1P8S off V1P8S on					
V1P8S_SEL	**0** 1	V1P8S controlled by SLP_S3_B according to sequencing V1P8S controlled by V1P8S_CTRL.V1P8S_EN bit Regardless of V1P8S_EN and V1P8S_SEL, V1P8S is disabled when SLP_S3_B is asserted, means low					

V1P8S_CTRL. V1P8S_SEL	V1P8S_CTRL. V1P8S_EN	SLP_S3_B	V1P8S
1	0	1	Off
1	1	1	On
x	x	0	Off

Table 51: V1P8S Truth Table

V1P8SX:

This power rail is used to source platform devices such as eMMC, camera, audio codecs … The maximum allowed output current is defined to 240mA. DA6021 controls this power rail while deriving the information from SoC SLP_S0ix_B signal and switching the rail internally. The typical R_{DSon} of this internal switch is 100mΩ.

Description	Value [max, mΩ]	Val
Input power path board resistance	10	-
Output power path board resistance	20	-
Input, output rails wirebond & internal FET RDS-ON	147	A,D,E

Table 52: V1P8S Power Switch Specification

Register Name	V1P8SX_CTRL		Address	0x5D Page 1	Read/Write		
			Reset Value	0x02			
MSB							LSB
R	R	R	R	R	R	R/W	R/W
Reserved						V1P8SX_SEL	V1P8SX_EN
V1P8SX_EN	**0** 1	V1P8SX off V1P8SX on					
V1P8SX_SEL	0 **1**	V1P8SX controlled by SLP_S0iX_B according to sequencing V1P8SX controlled by V1P8SX_CTRL.V1P8SX_EN bit Regardless of V1P8SX_EN and V1P8SX_SEL, V1P8SX is disabled when SLP_S3_B is asserted, means low					

V1PSX_CTRL.		SLP_S3_B	V1P8SX
V1P8SX_SEL	V1P8SX_EN		
1	0	1	Off
1	1	1	On
X	X	0	Off

Table 53: V1P8SX Truth Table

V1P2A:

V1P2A is a LDO that is sourced by V1P8A and generates a voltage of 1.2V to supply USB HSIC

Symbol	Parameter	Min	Typ	Max	Unit	Notes/Condition	Val
Input requirement							
Vin	Main input voltage		1.80		V	Supplied by V1P8A	-
Output requirement							
Vnom	Nominal output voltage		1.2		V		A
Vtol	Output voltage tolerance	-2%		+2%			A
Cout	Output capacity		1		µF		-
Iout-DC	Output load current		1	30	mA		A
IQSC	Quiescent current (operational)		10		µA	Iout-DC = 0mA	D,E
IQSC	Quiescent current (sleep)		2		µA	Iout-DC = 0mA	D,E

PSRR	Power supply rejection ratio	50			dB	Noise = 0.1Vpp, 1-10kHz, ½ Iout-DC	D,E
Vnoise	Output noise	50		100	µVRMS	10-100kHz, ½ Iout-DC	D,E

Table 54: Electrical Parameter for V1P2A

VREFDQ0:

Register Name		VREFDQ0_CTRL		Address	0x5E Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R/W	R/W	R/W	R/W	R/W
VREFDQVSEL					reserved	VREFDQ_SEL	VREFDQ_EN

VREFDQ_EN	**0** 1	VREFDQ0 enable VREFDQ0 disable
VREFDQ_SEL	**0** 1	VREFDQ0 controlled by SLP_S4_B according sequencing VREFDQ0 controlled by VREFDQ.VREFDQ_EN bit Regardless of VREFDQ_EN and VREFDQ_SEL, VREFDQ0 is disable when SLP_S4_B is asserted, means low
VREFDQVSEL[4:0]	**00000** 00001 00010 00011 … 11100 11101 11110 11111	0.600V 0.620V 0.640V 0.660V … 1.160V 1.180V 1.200V 1.220V

VREFDQ1:

Register Name		VREFDQ1_VSEL		Address	0xC6 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R/W	R/W	R/W	R/W	R/W
VREFDQVSEL					reserved	VREFDQ_SEL	VREFDQ_EN

VREFDQ_EN	**0** 1	VREFDQ1 enable VREFDQ1 disable
VREFDQ_SEL	**0** 1	VREFDQ1 controlled by SLP_S4_B according sequencing VREFDQ1 controlled by VREFDQ.VREFDQ_EN bit Regardless of VREFDQ_EN and VREFDQ_SEL, VREFDQ1 is disable when SLP_S4_B is asserted, means low
VREFDQVSEL[4:0]	**00000** 00001 00010 00011 … 11100 11101 11110 11111	0.600V 0.620V 0.640V 0.660V … 1.160V 1.180V 1.200V 1.220V

VREFDQ0/1 Electrical Specification:

Symbol	Parameter	Min	Typ	Max	Unit	Notes/Condition	Val
Input requirement							
Vin	Main input voltage		1.80		V	Supplied by V1P8A	-
Output requirement							
Vnom	Nominal output voltage		0.6..1.2		V	Via VREFDQ0/1_VSEL register	A
Vtol	Output voltage tolerance	-5%		+5%			A
Cout	Output capacity		1		µF		-
Iout-DC	Output load current		1	10	mA		A
IQSC	Quiescent current (operational)		10		µA	Iout-DC = 0mA	D,E
IQSC	Quiescent current (sleep)		2		µA	Iout-DC = 0mA	D,E
PSRR	Power supply rejection ratio	50			dB	Noise = 0.1Vpp, 1-10kHz, ½ Iout-DC	D.E
Vnoise	Output noise	50		100	µVRMS	10-100kHz, ½ Iout-DC	D,E

Table 55: Electrical Parameter for VREFDQ1/2

11.6.6 DC/DC Buck Regulator VDDQ

The high efficiency buck regulator supplies any type (1.5V/1.35V/1.25V) of DDR3 memory. The maximum output current of VDDQ buck regulator is 2800mA

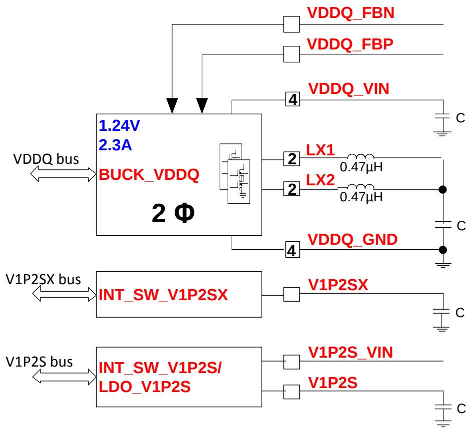


Figure 38: VDDQ Power Domain Block Diagram

11.6.6.1 Power States

Active State:

DA6021 VDDQ voltage rail can handle up to 2800mA max current. The usual average current is at 50mA to 500mA, but thermally able to handle 2800mA in peaks.. Optimized efficiency is achieved from 50mA to 500mA. Automatically switching from PWM to PFM mode achieves the best power efficiency.

S0ix State:

When the SoC enters the S0ix state, SLP_S0ix is held low. DA6021 turns the VDDQ buck regulator into low power mode and disables all un-necessary blocks, reducing the power requirements. DA6021 exits this power saving mode within 5µs after the SoC asserts the SLP_S0ix signal to high.

DA6021 is capable to support up to 200mA in this state.

S3 State:

In S3 state the average current of VDDQ is expected to be ~30mA which the regulator provides in power saving mode.

11.6.6.2 Electrical Characteristics VDDQ

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Val
VDDQ_VIN	Input Voltage		2.7		4.5	V	-
Cin	at VDDQ_IN			2 x 4.7		µF	-
Cout				3 x 47 or 6 x 22		µF	-
ESR of output capacitor				6 @ 22/47µF		mΩ	-
ESL of output capacitor				1.6 @ 3MHz		nH	-
L_BUCK	inductor value		-20%	2 x 0.47	+20%	µH	-
L_DCR	inductor resistance				48	mΩ	-
V1P0A	Output Voltage	IOUT= Imax		1.24/1.35±2%		V	A
F_BUCK	Frequency of operation			3		MHz	A
Transient load profile		35-2085mA			200	ns	-
Transient droop[16]		35-2085mA			50	mV	E
Transient overshoot[17]		2085-35mA			50	mV	E
Ton	Turn on time				2	ms	E
Rpd	Discharge impedance	VDDQ .. 0V			20	Ω	A
IQ_ON	Quiescent Current in On Mode				100	µA	E
Normal Mode – Synchronous rectification (PWM)							
Maximum Output Current (Imax)			2800			mA	D
ILIMIT	Current limitation	Cycle by cycle	1.3*Imax			mA	A*
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 39			D,E ,A*[18]
Sleep Mode – Pulse skipping (PSK)							
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 39			D,E ,A*

Table 56: Electrical Parameter for BUCK_VDDQ

[16] Including DC accuracy, ripple and load regulation
[17] Including DC accuracy, ripple and load regulation
[18] RDSON measurement on ATE

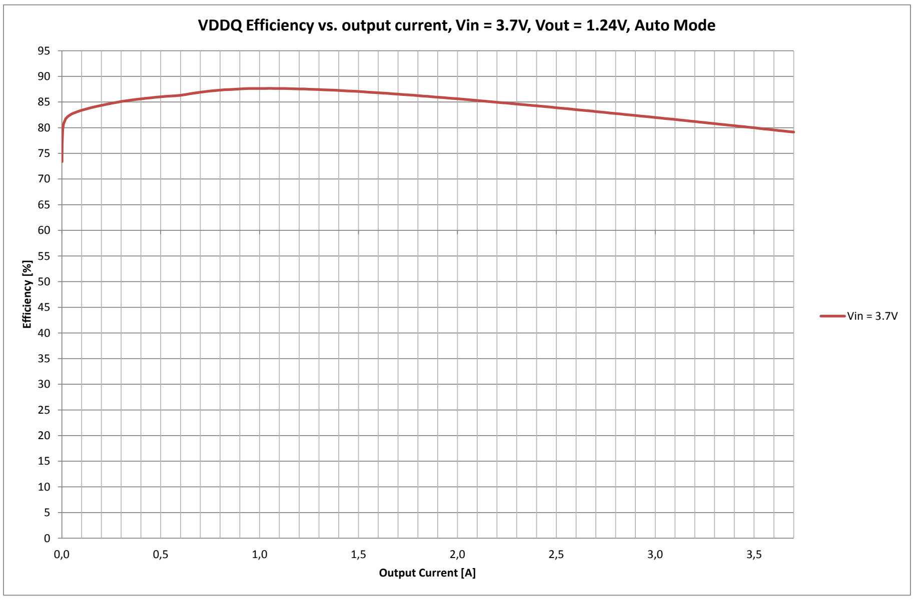


Figure 39: VDDQ Efficiency

11.6.6.3 VDDQ Registers

Register Name		VDDQ_CTRL		Address	**0x5F Page 1**	Read/Write	
				Reset Value	0x60		
MSB							LSB
R/W	R/W	R/W	R	R	RW	R/W	R/W
VDDQ_VSEL			reserved		NoS0iX	VDDQ _SEL	VDDQ _EN
VDDQ_EN		**0** 1	VDDQ off VDDQ on				
VDDQ_SEL		**0** 1	VDDQ controlled by SLP_S4_B according to sequencing VDDQ controlled by VDDQ_CTRL.VDDQ_EN bit Regardless of VDDQ_EN and VDDQ_SEL, VDDQ is disable when SLP_S4_B is asserted, means low				
NoS0iX		**0** 1	VDDQ active determined by SLP_S0iX_B VDDQ active, regardless of SLP_S0iX_B				
VDDQ_VSEL		000 001 010 **011** 100 101 110 111	1.080V 1.140V 1.200V **1.240V nominal voltage DDR3LP** 1.350V DDR3L 1.390V 1.418V 1.500V DDR3				

VDDQ_CTRL. VDDQ_SEL	VDDQ_CTRL. VDDQ_EN	SLP_S4_B	VDDQ
1	0	1	Off
1	1	1	On
x	x	0	Off

Table 57: VDDQ Truth Table

11.6.6.4 VDDQ Subsystems

V1P2S:

This voltage rail is used to supply mainly the MIP interface. In case of 1.24V DDR3 memory the input voltage of this power domain is VDDQ and it acts as a power switch. For all other types of DDR3 memories the input voltage is V1P8A and V1P2S is generated via a small LDO.

Description	Value [max, mΩ]	Val
Input power path board resistance	20	-
Output power path board resistance	20	-
Input, output rails wirebond & internal FET RDS-ON	620	A,D,E

Table 58: V1P2S Power Switch Specification

Electrical Parameters in case of a LDO function

Symbol	Parameter	Min	Typ	Max	Unit	Notes/Condition	Val
Input requirement							
Vin	Main input voltage		1.80		V	Supplied by V1P8A	-
Cin	V1P2S_IN		100		nF		-
Output requirement							
Vnom	Nominal output voltage		1.2		V		A
Vtol	Output voltage tolerance	-2%		+2%			A
Cout	Output capacity		2.2		µF		-
Iout-DC	Output load current		1	50	mA		A
IQSC	Quiescent current (operational)		10		µA	Iout-DC = 0mA	D,E
IQSC	Quiescent current (sleep)		2		µA	Iout-DC = 0mA	D,E
PSRR	Power supply rejection ratio	50			dB	Noise = 0.1Vpp, 1-10kHz, ½ Iout-DC	D,E
Vnoise	Output noise	50		100	µVRMS	10-100kHz, ½ Iout-DC	D,E

Table 59: Electrical Parameter for V1P2S LDO

Register Name	V1P2S_CTRL			Address	0x60 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R/W	R/W
Reserved						V1P2S _SEL	V1P2S _EN
V1P2S_EN		**0** 1	V1P2S off V1P2S on				
V1P2S_SEL		**0** 1	V1P2S controlled by SLP_S3_B according to sequencing V1P2S controlled by V1P2S_CTRL.V1P2S_EN bit Regardless of V1P2S_EN and V1P2S_SEL, V1P2S is disable when SLP_S3_B is asserted, means low				

V1P2S_CTRL.		SLP_S3_B	V1P2S
V1P2S_SEL	V1P2S_EN		
1	0	1	Off
1	1	1	On
x	x	0	Off

Table 60: V1P2S Truth Table

V1P2SX:

This voltage rail is used to supply the SoC SFR via an internal switch from VDDQ.

Description	Value [max, mΩ]	Val
Input power path board resistance	20	-
Output power path board resistance	20	-
Input, output rails wirebond & internal FET RDS-ON	160	A,D,E

Table 61: V1P2SX Power Switch Specification

Register Name	V1P2SX_CTRL			Address	0x61 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R/W	R/W
Reserved						V1P2SX _SEL	V1P2SX _EN
V1P2SX_EN		**0** 1	V1P2SX off V1P2SX on				
V1P2SX_SEL		**0** 1	V1P2SX controlled by SLP_S0iX_B according to sequencing V1P2SX controlled by V1P2SX_CTRL.V1P2SX_EN bit Regardless of V1P2SX_EN and V1P2SX_SEL, V1P2SX is disable when SLP_S3_B is asserted, means low				

The maximum current is defined to 155mA, switched internally and controlled via the SoC SLP_S0iX_B signal.

V1P2SX_CTRL. V1P2SX_SEL	V1P2SX_CTRL. V1P2SX_EN	SLP_S3_B	V1P2SX
1	0	1	Off
1	1	1	On
x	x	0	Off

Table 62: V1P2SX Truth Table

11.6.7 Power Rail VSYSU

VSYSU is the voltage rail that sources power of VSYS through an external power switch. This power domain is used to source communication and the modem. The external power switch is generated via a P-channel FET.

DA6021 provides an enable signal VSYSU_EN_B supplied by VSYS, driving the gate of the external FET. DA6021 provides also a feedback input signal VSYSU_FB to control the slew rate and limit the inrush current

Register Name		VSYSU_CTRL		Address		0x62 Page 1	Read/Write
				Reset Value		0x02	
MSB							LSB
R	R	R	R	R	R	R/W	R/W
Reserved						VSYSU _SEL	VSYSU _EN
VSYSU_EN		**0** 1	VSYSU off VSYSU on				
VSYSU_SEL		0 **1**	VSYSU controlled by SLP_S4_B according to sequencing VSYSU controlled by VSYSU_CTRL.VSYSU_EN bit Regardless of VSYSU_EN and VSYSU_SEL, VSYSU_EN_B is high when SLP_S4_B is asserted, means low				

VSYSU_CTRL. VSYSU_SEL	VSYSU_CTRL. VSYSU_EN	SLP_S4_B	VSYSU_EN_B
1	0	1	High
1	1	1	Low
x	x	0	High

Table 63: VSYSU_EN_B Truth Table

VSYSU external P-channel power switch parameters:

Rdson (Vgs=3.7V)	15-35mohm
Input capacitance, Ciss	750-2315pF
Output capacitance, Coss	265-900pF
Reverse transfer capacitance, Crss	240-800pF

11.6.8 Power Rail VSYS_SX

VSYSU is the voltage rail that sources power of VSYS through an external power switch. This power domain is used to source the vibra. The external power switch is generated via a P-channel FET.

DA6021 provides an enable signal VSYSSX_EN_B, supplied by VSYS, driving the gate of the external FET. DA6021 provides also a feedback input signal VSYSSX_FB to control the slew rate and limit the inrush current

Register Name	VSYSSX_CTRL			Address	0x63 Page 1	Read/Write	
				Reset Value	0x02		
MSB							LSB
R	R	R	R	R	R	R/W	R/W
Reserved						VSYSSX _SEL	VSYSSX _EN
VSYSSX_EN		**0** 1	VSYSSX_EN_B set to high VSYSSX_EN_B set to low				
VSYSSX_SEL		0 **1**	VSYSSX_EN_B controlled by SLP_S0iX_B according to sequencing VSYSSX_EN_B controlled by VSYSSX_CTRL.VSYSSX_EN bit Regardless of VSYSSX_EN and VSYSSX_SEL, VSYSSX_EN_B is high when SLP_S3_B is asserted, means low				

VSYSSX_CTRL. VSYSSX_SEL	VSYSSX_CTRL. VSYSSX_EN	SLP_S3_B	VSYSSX_EN_B
1	0	1	High
1	1	1	Low
x	x	0	High

Table 64: VSYSSX_EN_B Truth Table

VSYS_SX external P-channel power switch parameters:

Rdson (Vgs=3.7V)	15-35mohm
Input capacitance, Ciss	750-2315pF
Output capacitance, Coss	265-900pF
Reverse transfer capacitance, Crss	240-800pF

11.6.9 Power Rail VSYS_S

VSYS_S is a voltage rail that is supplied by VSYS through an internal DA6021 power switch with a R_{DSon} of 900mΩ.

Description	Value [max, mΩ]	Val
Input, output rails wirebond & internal FET RDS-ON	1000	A,D,E

Table 65: VSYS_S Power Switch Specification

VSYS_S power switch is enabled when SLP_S3_B is high, unless VSYS_S_CTRL.VSYS_S_SEL bit is set to high.

Register Name		**VSYS_S_CTRL**		Address	**0x64 Page 1**	Read/Write	
				Reset Value	0x02		
MSB							LSB
R	R	R	R	R	R	R	R
reserved						VSYS_S_SEL	VSYS_S_EN
VSYS_S_EN		**0** 1	VSYS_S off VSYS_S on				
VSYS_S_SEL		0 **1**	VSYS_S controlled by SLP_S3_B according to sequencing VSYS_S controlled by VSYS_S_CTRL.VSYS_S_EN bit Regardless of VSYS_S_EN and VSYS_S_SEL, VSYS_S is disable when SLP_S3_B is asserted, means low				

VSYS_S_CTRL. VSYS_S_SEL	VSYS_S_CTRL. VSYS_S_EN	SLP_S3_B	VSYS_S
1	0	1	Off
1	1	1	On
x	x	0	Off

Table 66: VSYS_S Truth Table

11.6.10 Buck Boost Regulator V2P85S

DA6021 integrates a buck/boost converter supplying 2.85V into the system for touch screen, eMMC, sensors and V2P85SX loads. The maximum output current of V2P85S buck/boost regulator is 550mA

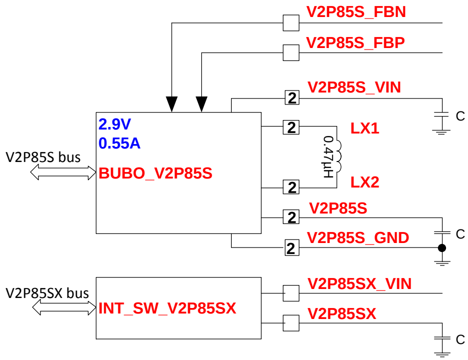


Figure 40: Buck Boost V2P85S Power Domain Block Diagram

11.6.10.1 Electrical Characteristics V2P85S

Buck/boost regulator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Val
V2P85S_VIN	Input Voltage		2.7		4.5	V	-
Cin	at V2P85S_IN			4.7		µF	-
Cout				2 x 22		µF	-
ESR of output capacitor				6 @ 22µF		mΩ	-
ESL of output capacitor				1.6 @ 3MHz		nH	-
L_BUCK	inductor value		-20%	0.47	+20%	µH	
L_DCR	inductor resistance				48	mΩ	-
V2P85S	Output Voltage	IOUT= Imax		2.9±2%		V	A
F_BUCK/BOOST operation	Frequency of			3		MHz	A
Transient load profile		0-550mA		250		ns	-
Transient droop[19]		0-550mA			116	mV	E
Transient overshoot[20]		550-0mA			116	mV	E
Ton	Turn on time				2	ms	E
Rpd	discharge impedance	V2P85S .. 0V			20	Ω	A
IQ_OFF Off Mode	Quiescent Current in				50	µA	E
Normal Mode – Synchronous rectification (PWM)							
Maximum Output Current (Imax)			550			mA	D
ILIMIT	Current limitation	Cycle by cycle	850			mA	A*
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 41			D,E, A*[21]
Sleep Mode – Pulse skipping (PSK)							
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 41			D,E, A*

Table 67: Electrical Parameter for BUCKBOOST_V2P85S

[19] Including DC accuracy, ripple and load regulation
[20] Including DC accuracy, ripple and load regulation
[21] RDSON meansurement on ATE

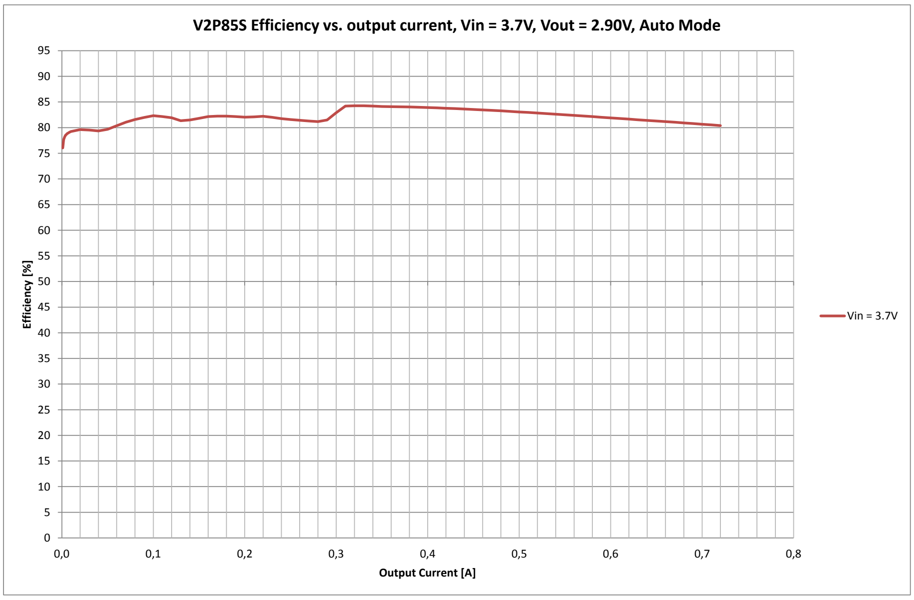


Figure 41: V2P85S Efficiency

11.6.10.2 V2P85 Registers

Register Name		**V2P85S_CTRL**		Address	**0x65 Page 1**	Read/Write	
				Reset Value	0x60		
MSB							LSB
R/W	R/W	R/W	R	R	R	R/W	R/W
V2P85S_VSEL			reserved			V2P85S_SEL	V2P85S_EN
V2P85S_EN		**0** 1	V2P85S off V2P85S on				
V2P85S_SEL		**0** 1	V2P85S controlled by SLP_S3_B according to sequencing V2P85S controlled by V2P85S_CTRL.V2P85S_EN bit Regardless of V2P85S_EN and V2P85S_SEL, V2P85S is disable when SLP_S3_B is asserted, means low				
V2P85S_VSEL		000 001 010 **011** 100 101 110 111	2.565V 2.700V 2.850V **2.900V nominal voltage** 2.950V 3.000V 3.135V 3.300V				

Note: If V2P85S is disabled when system in S0-mode, after exiting S0iX-mode, the regulator will be enabled automatically

V2P85S_CTRL.		SLP_S3_B	V2P85S
V2P85S_SEL	V2P85S_EN		
1	0	1	Off
1	1	1	On
x	x	0	Off

Table 68: V2P85S Truth Table

11.6.10.3 V2P85S Subsystems

V2P85SX:

This voltage rail supplies mainly cameras. The control of this power rail is derived from the SoC SLP_S0ix_B signal. The maximum current is 250mA. The internal switch has a R_{DSon} of 460mΩ.

Description	Value [max, mΩ]	Val
Input power path board resistance	0	-
Output power path board resistance	40	-
Input, output rails wirebond & internal FET RDS-ON	180	A,D,E

Table 69: V2P85SX Power Switch Specification

Register Name		V2P85SX_CTRL		Address		0x66 Page 1	Read/Write
				Reset Value		0x02	
MSB							LSB
R	R	R	R	R	R	R/W	R/W
Reserved						V2P85SX_SEL	V2P85SX_EN
V2P85SX_EN		**0** 1	V2P85SX off V2P85SX on				
V2P85SX_SEL		0 **1**	V2P85SX controlled by SLP_S0iX_B according to sequencing V2P85SX controlled by 2P85SX_CTRL.V2P85SX_EN bit Regardless of V2P85SX_EN and V2P85SX_SEL, V2P85SX is high when SLP_S3_B is asserted, means low				

V2P85SX_CTRL. V2P85SX_SEL	V2P85SX_CTRL. V2P85SX_EN	SLP_S3_B	V2P85SX
1	0	1	Off
1	1	1	On
x	x	0	Off

Table 70: V2P85SX Truth Table

11.6.11 Buck Boost Regulator V3P3A

DA6021 integrates a buck/boost converter supplying 3.3V into the system towards the SoC, V3P3U, V3P3S, VUSBPHY and VSDIO. The output voltage is set to 3.333V. The maximum output current of V3P3A buck regulator is 1600mA

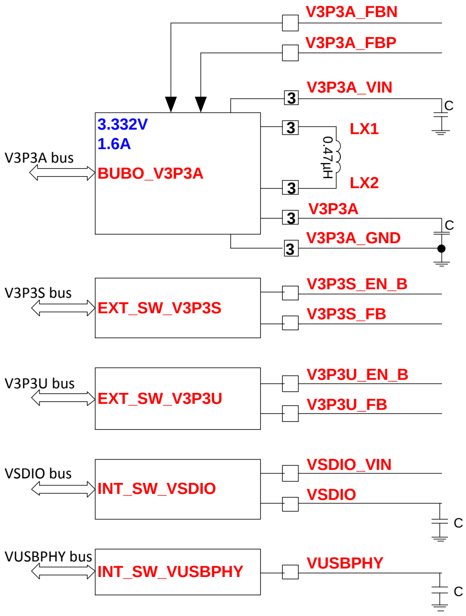


Figure 42:V3P3A Power Domain Block Diagram

11.6.11.1 Electrical Characteristics V3P3A

Buck/boost regulator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Val
V3P3A_VIN	Input Voltage		2.7		4.5	V	-
Cin	at V3P3A_IN			4.7		µF	-
Cout				3x47 or 6x22		µF	-
ESR of output capacitor				6 @ 22µF		mΩ	-
ESL of output capacitor				1.6 @ 3MHz		nH	-
L_BUCK	inductor value		-20% or	0.47 2x1	+20%	µH	-
L_DCR	inductor resistance				48	mΩ	-
V3P3A	Output Voltage	IOUT= Imax		3.333±2%		V	A
F_BUCK/BOOST	Frequency of operation			3		MHz	A
Transient load profile		150-1519mA		250		ns	
Transient droop[22]		150-1519mA			133	mV	
Transient overshoot[23]		1519-150mA			133	mV	
Ton	Turn on time				2	ms	
IQ_OON Mode	Quiescent Current in On				50	µA	
Rpd	Discharge impedance				20	Ω	A
Normal Mode – Synchronous rectification (PWM)							
Maximum Output Current (Imax)			1570			mA	D,E
ILIMIT	Current limitation	Cycle by cycle	1.3*Imax			mA	A*

[22] Including DC accuracy, ripple and load regulation
[23] Including DC accuracy, ripple and load regulation

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	Val
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout			See Figure 43			D,E, A*
Sleep Mode – Pulse skipping (PSK)						
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout			See Figure 43			D,E, A*

Table 71: Electrical Parameter for BUCKBOOST_V3P3A

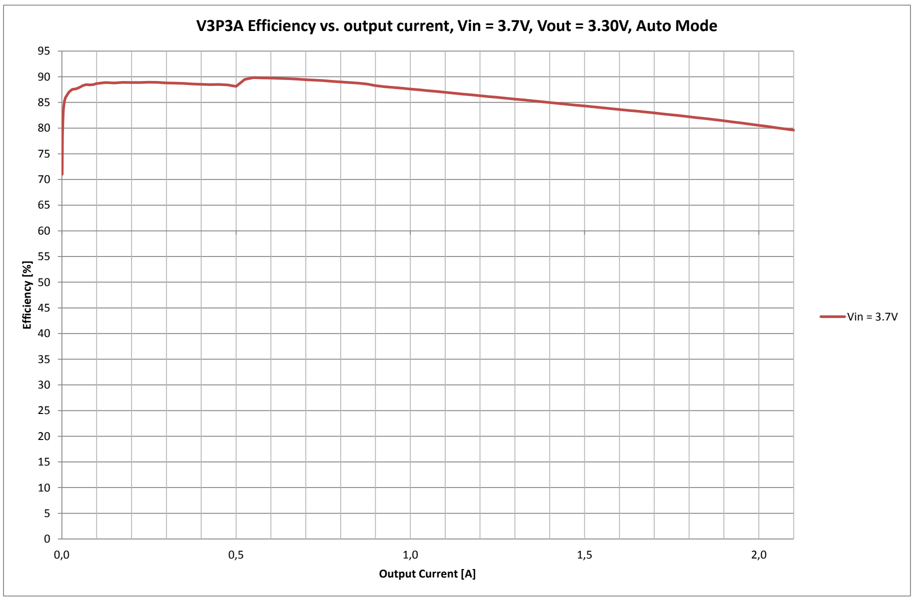


Figure 43:V3P3A Efficiency

11.6.11.2 V3P3A Registers

<table>
<tr><td>Register Name</td><td colspan="2">V3P3A_CTRL</td><td colspan="2">Address</td><td colspan="2">0x67
Page 1</td><td>Read/Write</td></tr>
<tr><td colspan="4"></td><td>Reset Value</td><td colspan="2">0x60</td><td></td></tr>
<tr><td>MSB</td><td colspan="6"></td><td>LSB</td></tr>
<tr><td>R/W</td><td>R/W</td><td>R/W</td><td>R</td><td>R</td><td>R</td><td>R/W</td><td>R/W</td></tr>
<tr><td colspan="3">V3P3A_VSEL</td><td colspan="3">reserved</td><td>V3P3A_SEL</td><td>V3P3A_EN</td></tr>
<tr><td colspan="2">V3P3A_EN</td><td>0
1</td><td colspan="5">V3P3A off
V3P3A on</td></tr>
<tr><td colspan="2">V3P3A_SEL</td><td>0
1</td><td colspan="5">V3P3A controlled by SUSPWRDNACK according to sequencing
V3P3A controlled by V3P3A_CTRL.V3P3A_EN bit
Regardless of V3P3A_EN and V3P3A_SEL, V3P3A is disable when SUSPWRDNACK is de-asserted, means high</td></tr>
</table>

V3P3A_VSEL	000 001 010 **011** 100 101 110 111	2.970V 3.135V 3.300V **3.333V nominal voltage** 3.340V reserved 3.465V 3.630V

V3P3A_CTRL. V3P3A_SEL	V3P3A_EN	SUSPWRDNACK	V3P3A
1	0	0	Off
1	1	0	On
x	x	1	Off

Table 72: V3P3A Truth Table

11.6.11.3 V3P3A Subsystems

V3P3U:

V3P3U is the voltage rail which is sourced by V3P3A and switched by an external P-channel FET. This voltage rail is foreseen to supply mainly WIFI and BT. DA6021 provides a control signal V3P3_U_EN supplied by V3P3A and derived from SoC's SLP_S4_B signal. The maximum current for this power rail is 700mA

Register Name	V3P3U_CTRL			Address	0x68 Page 1	Read/Write	
				Reset Value	0x02		
MSB							LSB
R	R	R	R	R	R	R/W	R/W
Reserved						V3P3U_SEL	V3P3U_EN
V3P3U_EN	**0** 1	V3P3U off V3P3U on					
V3P3U_SEL	0 **1**	V3P3U controlled by SLP_S4_B according to sequencing V3P3U controlled by V3P3U_CTRL.V3P3U_EN bit Regardless of V3P3U_EN and V3P3U_SEL, V3P3U_EN_B is high when SLP_S4_B is asserted, means low					

V3P3U_CTRL. V3P3U_SEL	V3P3U_EN	SLP_S4_B	V3P3U_EN_B
1	0	1	High
1	1	1	Low
x	x	0	High

Table 73: V3P3U_EN_B Truth Table

V3P3U external P-channel power switch parameters:

Rdson (Vgs=3.3V)	35-62.5mohm
Input capacitance, Ciss	750-2000pF
Output capacitance, Coss	150-530pF
Reverse transfer capacitance, Crss	100-360pF

V3P3S:

V3P3S is the voltage rail which is sourced by V3P3A and switched by an external P-channel FET. The power domain is used to power the display, MIPI LVDS bridge, SSD drive and audio codecs. The control signal V3P3S_EN_B is supplied by V3P3A and when asserted low, the signal slew rate is controlled to limit the in-rush current when the external P-channel FET turns on.

Register Name		**V3P3S_CTRL**		Address	**0x69 Page 1**	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R/W	R/W
Reserved						V3P3S _SEL	V3P3S _EN
V3P3S_EN		**0** 1	V3P3S_EN_B set to high V3P3S_EN_B set to low				
V3P3S_SEL		**0** 1	V3P3S_EN_B controlled by SLP_S3_B according to sequencing V3P3S_EN_B controlled by V3P3S_CTRL.V3P3S_EN bit Regardless of V3P3S_EN and V3P3S_SEL, V3P3S_EN_B is high when SLP_S3_B is asserted, means low				

V3P3S_CTRL. V3P3S_SEL	V3P3S_CTRL. V3P3S_EN	SLP_S3_B	V3P3S_EN_B
1	0	1	High
1	1	1	Low
x	X	0	High

Table 74: V3P3S_EN_B Truth Table

V3P3S external P-channel power switch parameters:

Rdson (Vgs=3.3V)	35-62.5mohm
Input capacitance, Ciss	750-2000pF
Output capacitance, Coss	150-530pF
Reverse transfer capacitance, Crss	100-360pF

VUSBPHY:

VUSBPHY is composed of V3P3A or VSYS via an internal power rail switch. It sources power from V3P3A whenever the V3P3A buck boost converter is enabled. When V3P3A is switched off VUSBPHY is sourced by VSYS.

Description	Value [max, mΩ]	Val
V3P3A input power path board resistance	10	-
VSYS input power path board resistance	10	-
Output power path board resistance	20	-
Input, output rails wirebond & internal FET RDS-ON	305	A,D,E

Table 75: VUSBPHY Power Switch Specification

VSDIO:

This power rail supplies energy towards the SDIO/MMC subsystem. The power rail is either supplied by 1.8V via V1P8_A buck converter or by V3P3_A. In case of a 3.3V supply, the internal switch has a R_{DSon} of 200mΩ, in case of 1.8V the R_{DSon} is 80mΩ. The maximum current is defined to 200mA.

Description	Value [max, mΩ]	Val
V3P3A input power path board resistance	10	-
V1P8A input power path board resistance	10	-
Output power path board resistance	20	-
Input, output rails wirebond & internal FET RDS-ON	108	A,D,E

Table 76: VSDIO Power Switch Specification

The table below shows how the VSDIO voltage is selected:

SDMMC3_PWR_EN_B	SDMMC3_1P8_EN	VSDIO
0	0	3.3V
0	1	1.8V
1	0	0V
1	1	0V

Table 77: VSDIO Output Voltage Selection

11.6.12 Boost Regulator V5P0S

DA6021 integrates a boost converter supplying 5V into the platform towards HDMI, USB3, VBUS & USB2/3 OTG. The maximum output current of V5P0_S boost converter is 955mA

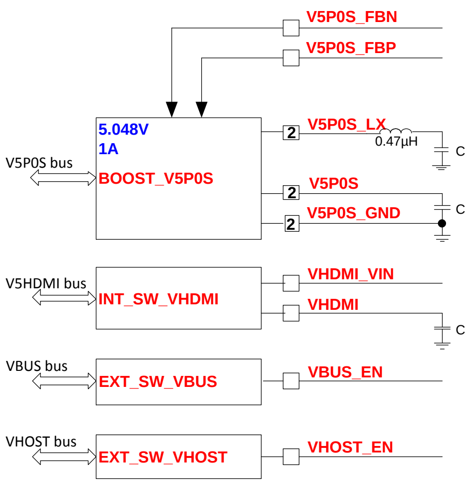


Figure 44:V5P0S Power Domain Block Diagram

11.6.12.1 Electrical Characteristics V5P0S

Boost regulator

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Val
V5P0S_VIN	Input Voltage		2.7		4.5	V	-
Cin	at V5P0S_IN			2 x 10		µF	-
Cout				4 x 22		µF	-
ESR of output capacitor				6 @ 22µF		mΩ	-

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Val
ESL of output capacitor				1.6 @ 3MHz		nH	-
L_BOOST	inductor value		-20%	0.47	+20%	µH	-
L_DCR	inductor resistance				48	mΩ	-
V5P0S	Output Voltage	IOUT= Imax		5.0±2%		V	A
F_BOOST	Frequency of operation			3		MHz	A
Transient load profile		0-955mA			250	ns	-
Transient droop[24]		0-955mA			202	mV	E
Transient overshoot[25]		955-0mA			202	mV	E
Ton	Turn on time				2	ms	E
IQ_OFF Off	Quiescent Current in Mode				50	µA	E
Normal Mode – Synchronous rectification (PWM)							
Maximum Output Current (Imax)			1000			mA	D
ILIMIT	Current limitation	Cycle by cycle	1.3*Imax			mA	A*
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 45			D,E, A*[26]
Sleep Mode – Pulse skipping (PSK)							
Efficiency at VSYS = 3.7V & Tamb=60°C with proposed external components and PCB layout				See Figure 45			D,E, A*

Table 78: Electrical Parameter for BOOST_V5P0S

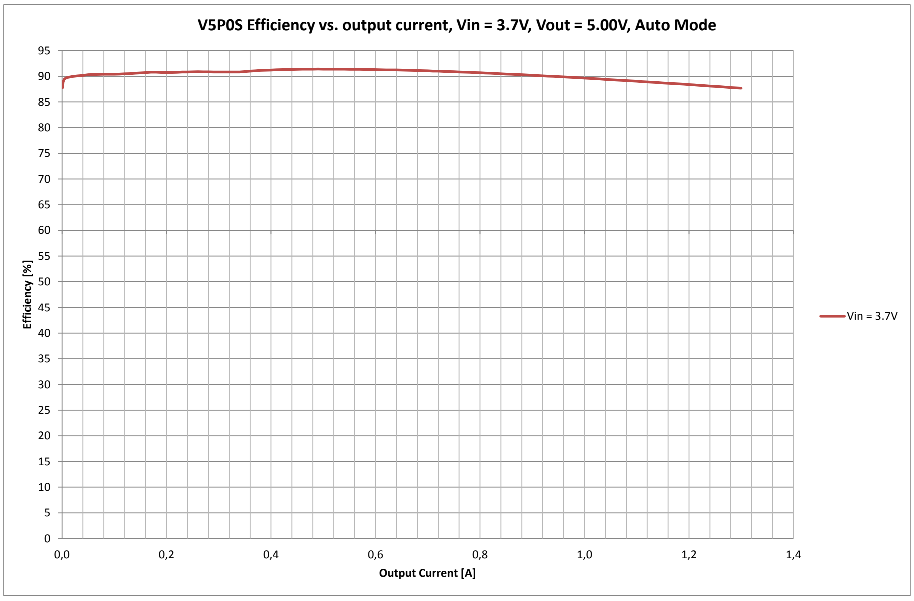


Figure 45:V5P0S Efficiency

[24] Including DC accuracy, ripple and load regulation
[25] Including DC accuracy, ripple and load regulation
[26] RDSON measurement on ATE

11.6.12.2 V5P0S Registers

Register Name			V5P0S_CTRL	Address		0x6A Page 1	Read/Write
				Reset Value		0x60	
MSB							LSB
R/W	R/W	R/W	R	R	R	R/W	R/W
V5P0S_VSEL			reserved			V5P0S_SEL	V5P0S_EN

V5P0S_EN	**0** 1	V5P0S off V5P0S on
V5P0S_SEL	**0** 1	V5P0S controlled by SLP_S3_B according to sequencing V5P0S controlled by V5P0S_CTRL.V5P0S_EN bit Regardless of V5P0S_EN and V5P0S_SEL, V5P0 is disable when SLP_S3_B is asserted, means low
V5P0S_VSEL	000 001 010 **011** 100 101 110 111	4.500V 4.750V 5.000V **5.050V nominal voltage** 5.100V reserved 5.250V 5.500V

V5P0S_CTRL. V5P0S_SEL	V5P0S_CTRL. V5P0S_EN	SLP_S3_B	V5P0S
1	0	1	Off
1	1	1	On
x	x	0	Off

Table 79: V5P0S Truth Table

11.6.12.3 V5P0S Subsystems

VHOST:

This voltage rail is used for the 5V VBUS providing energy to the USB2/3 host, switched by an external power switch.

Register Name			VHOST_CTRL	Address		0x6B Page 1	Read/Write
				Reset Value		0x02	
MSB							LSB
R	R	R	R	R	R	R/W	R/W
Reserved						VHOST_SEL	VHOST_EN

VHOST_EN	**0** 1	VHOST_EN set to high VHOST_EN set to low
VHOST_SEL	0 **1**	VHOST_EN controlled by SLP_S0iX_B according to sequencing VHOST_EN controlled by VHOST_CTRL.VHOST_EN bit Regardless of VHOST_EN and VHOST_SEL, VHOST_EN is low when SLP_S3_B is asserted, means low

The maximum current of this power domain is defined to 900mA

VHOST_CTRL.		SLP_S3_B	VHOST_EN
VHOST_SEL	VHOST_EN		
1	0	1	Low
1	1	1	High
x	x	0	Low

Table 80: VHOST_EN Truth Table

Parameter	Value	Val
V_IL	>0.66V	
V_IH	<1.1V	
I_EN	>0.5µA	

Table 81: VHOST External Power Switch Driver Capability

VBUS:

VBUS is the power rail supplying the VBUS of USB2/3 OTG through an external power switch.

Register Name		VBUS_CTRL		Address	0x6C Page 1	Read/Write	
				Reset Value	0x02		
MSB							LSB
R	R	R	R	R	R	R/W	R/W
Reserved						VBUS _SEL	VBUS _EN
VBUS_EN		**0** 1	VBUS_EN set to high VBUS_EN set to low				
VBUS_SEL		0 **1**	VBUS_EN controlled by ULPI_VBUS_EN VBUS_EN controlled by VBUS_CTRL.VBUS_EN bit Regardless of VBUS_EN and VBUS_SEL, VBUS_EN is low when SLP_S3_B is asserted, means low				

The maximum current of this power domain is defined to 900mA

VBUS_CTRL.		ULPI_VBUS_EN	VBUS_EN
VBUS_SEL	VBUS_EN		
0	X	Low	Low
0	x	high	High
1	0	X	Low
1	1	X	high

Table 82: VBUS_EN Truth Table

Parameter	Value	Val
V_IL	>0.66V	
V_IH	<1.1V	
I_EN	>0.5µA	

Table 83: VBUS External Switch Driver Capability

VHDMI:

VHDMI is the 5V power supply to HDMI connector sourced by V5P0S through an internal switch. The R_{DSon} of the internal switch it 900mΩ

Description	Value [max, mΩ]	Val
Input power path board resistance	20	-
Output power path board resistance	200	-
Input, output rails wirebond & internal FET RDS-ON	1200	A,D,E

Table 84: VHDMI Power Switch Specification

Register Name	VHDMI_CTRL		Address	0x6D Page 1	Read/Write		
			Reset Value	0x02			
MSB							LSB
R	R	R	R	R	R	R/W	R/W
Reserved						VHDMI _SEL	VHDMI _EN
VHDMI_EN	**0** 1	VHDMI_EN off VHDMI_EN on					
VHDMI_SEL	0 **1**	VHDMI_EN controlled by SLP_S0iX_B according sequencing VHDMI_EN controlled by VHDMI_CTRL.VHDMI_EN bit Regardless of VHDMI_EN and VHDMI_SEL, VHDMI is disable when SLP_S3_B is asserted, means low					

The maximum current of this power domain is defined to 55mA

VHDMI_CTRL. VHDMI_SEL	VHDMI_CTRL. VHDMI_EN	SLP_S3_B	VHDMI
1	0	1	Off
1	1	1	On
x	x	0	Off

Table 85: VHDMI Truth Table

11.6.13 VLP Low Power Regulator

The LDO_LP will be used for running the internal sequencer. It is supplied by the system supply voltage VSYS. This allows a power up prior the system power domains. This LDO acts as the supply for the bias, reference, OTP and DA6021 registers.

Electrical Characteristics (Ta = -40 to +85 ºC) VSUP = 2.7 to 4.5V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	Val
VSYS1 VSYS2	Input Voltage		2.7		4.5	V	-
VLP	Output Voltage	IOUT= Imax	2.45	2.5	2.55	V	A
Accuracy		Room temperature			0.6	%	A
Cstab	Stabilization capacitor	Tolerance of ± 35%	2.2			µF	-
Cdec	Decoupling capacitor	Tolerance of ±	220			nF	-

		35%					
Cesr	ESR of capacitor	F > 1MHz		0.1		Ω	
IMAX Current	Maximum Output		10			mA	D,E
IQ_ON ON	Quiescent current in MODE				10	µA	D
PSRR	Power Supply Rejection Ratio	Noise = 0.1VPP, 1-10kHz, ½ Iout	50		60	dB	D,E
Vnoise	Output Noise	BW = 10-100kHz, ½ Iout	60		100	µV	D,E
Ton	Turn on time from POR		5	10		ms	D,E

Table 86: Electrical Parameter for LDO_LP

11.7 Current Monitor

Following switching regulators include an output current measurement feature: VCC, VNN, V1P0A, V1P05S and VDDQ. The output current is measured internally and averaged across 1ms. The average current is digitalized by using 10 bits ADC (refer to ADC section) and stored into 2 x 8 bits registers for each mentioned voltage rail as specified. The average current is updated to the respective registers once every 1ms. VCC & VNN output current are stored in SVID registers 0x14(IoutH) and 0x15(IoutL) with their respective voltage rail address. V1P0A output current is stored in 0x1D(IoutH) and 0x1E(IoutL) registers at SVID voltage rail address of 00h. VDDQ output current is stored in 0x1D(IoutH) and 0x1E(IoutL) registers at SVID voltage rail address of 01h. V1P05S output current is stored in 0x1F(IoutH) & 0x20h(IoutL) registers at SVID voltage rail address of 00h.

Current measurement tolerance target for each voltage rails above is as below:

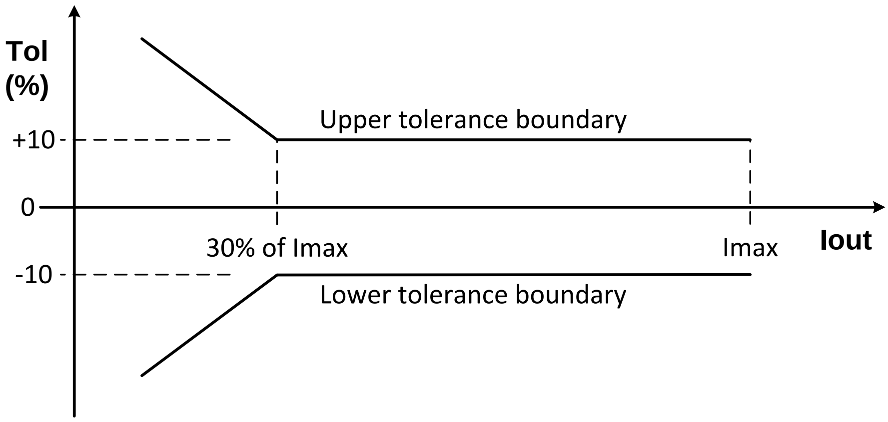


Figure 46: Current Measurement Tolerance Boundary

Voltage Rail	Resolution	Tolerance	Val
VCC	20mA/LSB	±5%	A*
VNN	20mA/LSB	±5%	A*
V1P0A	5mA/LSB	±5%	A*
V1P05S	2.5mA/LSB	±5%	A*
VDDQ	5mA/LSB	±5%	A*

Table 87: Current Measurement Resolution

11.7.1 VCC/VNN Current vs ADC data

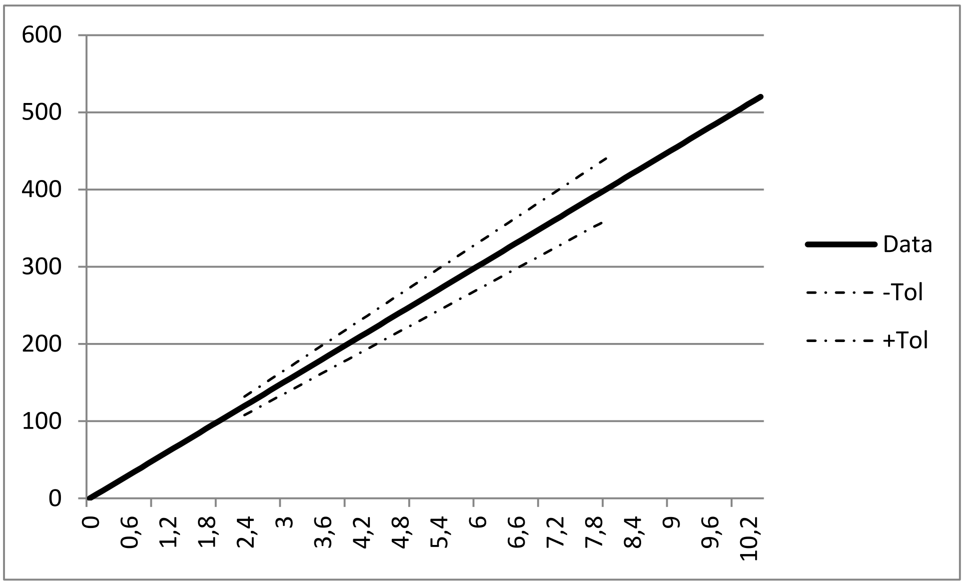


Figure 47: VCC/VNN ADC Current Coding

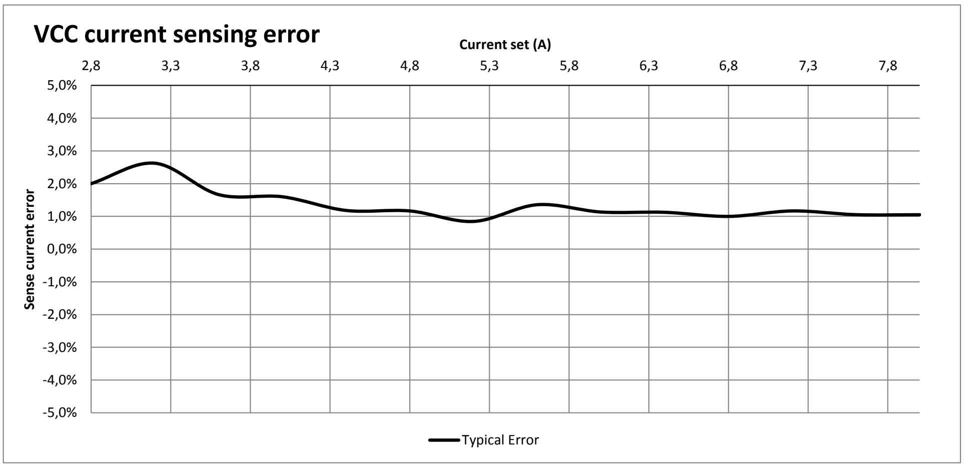


Figure 48: Typical VCC Current Sensing Error

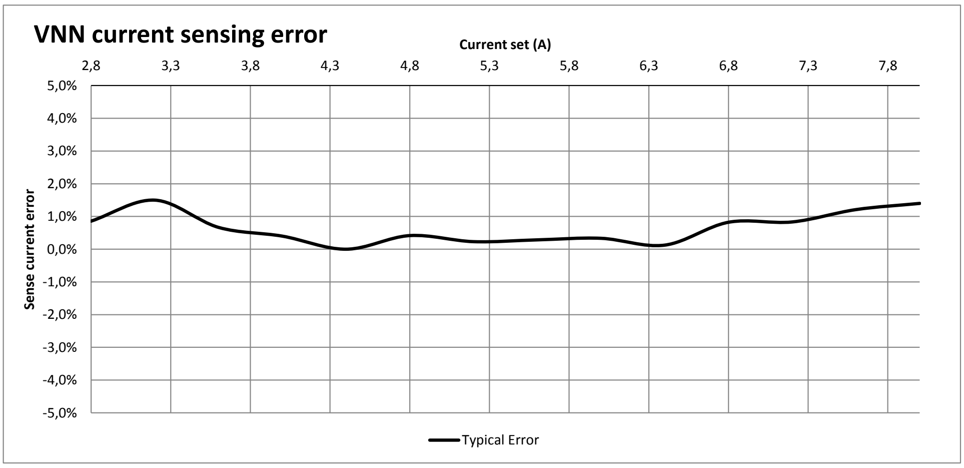


Figure 49: Typical VNN Current Sensing Error

11.7.2 V1P0A Current vs ADC data

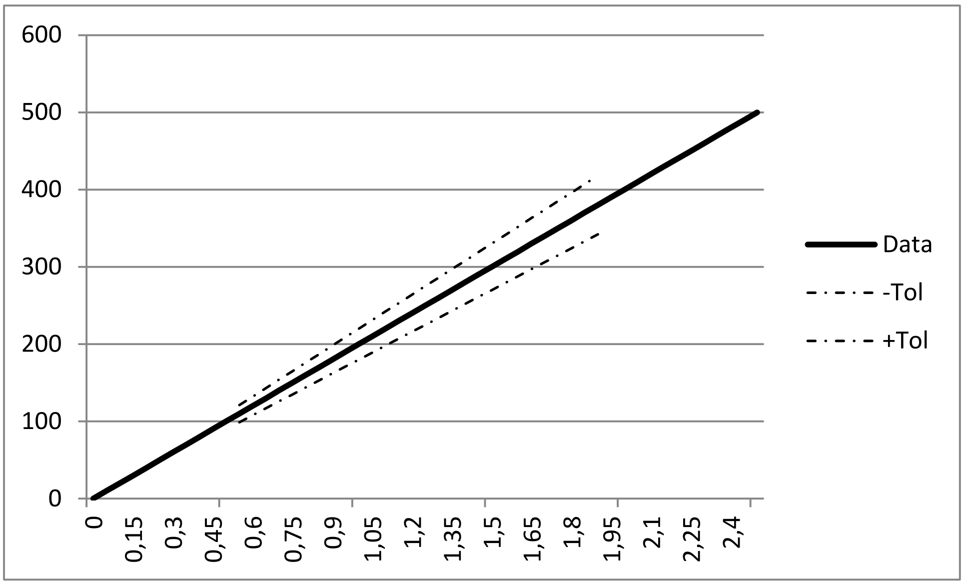


Figure 50: V1P0A ADC Current Coding

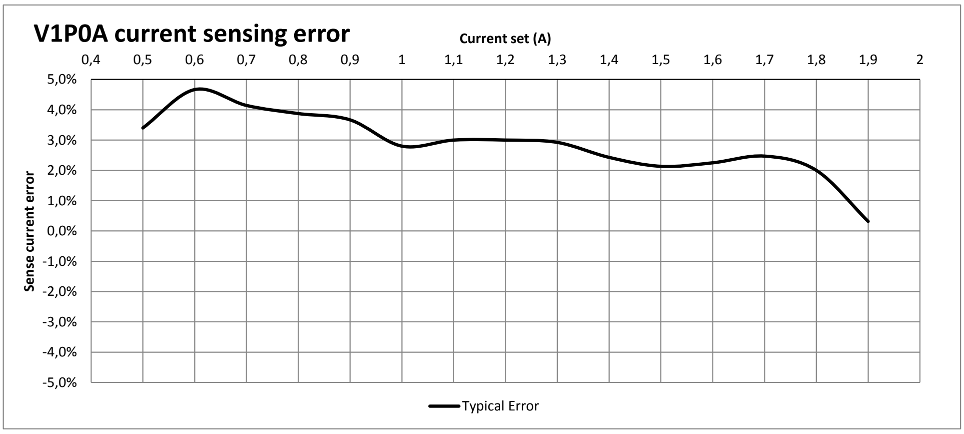


Figure 51: Typical V1P0A Current Sensing Error

11.7.3 V1P5S Current vs ADC data

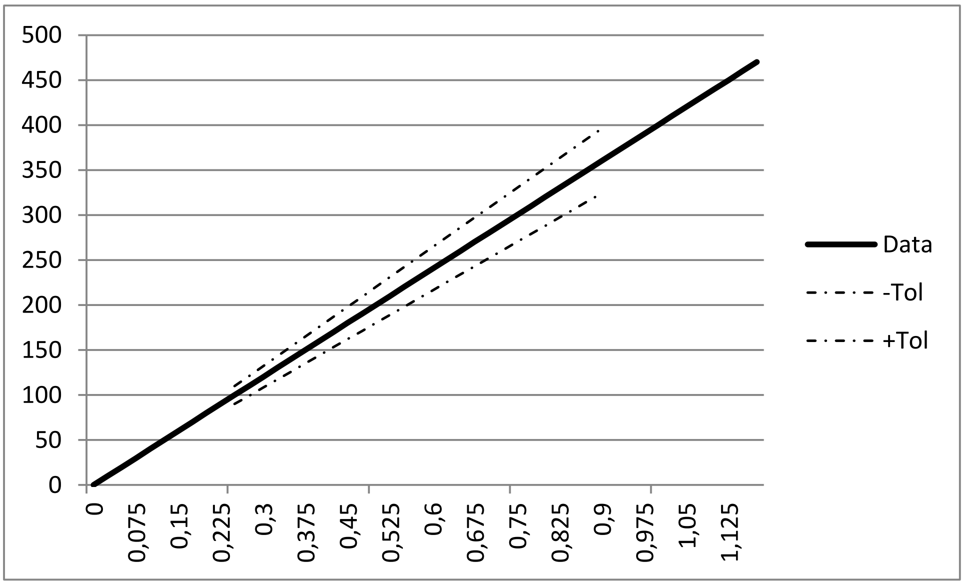


Figure 52: V1P05S ADC Current Coding

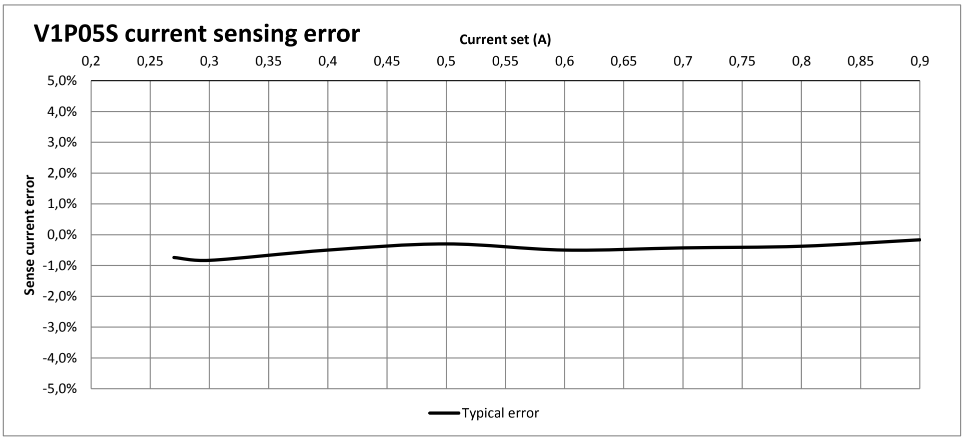


Figure 53: Typical V1P05S Current Sensing Error

11.7.4 VDDQ Current vs ADC data

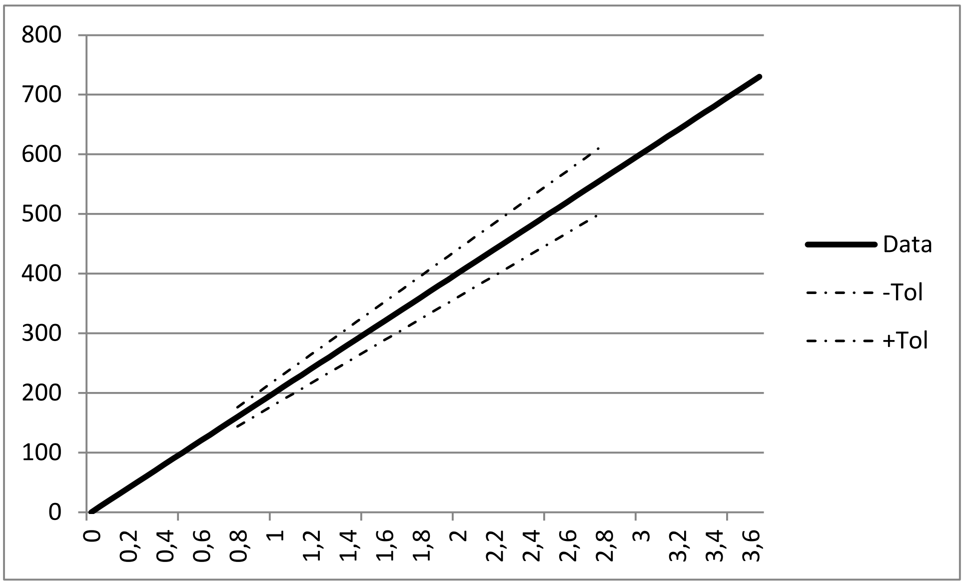


Figure 54: VDDQ ADC Current Coding

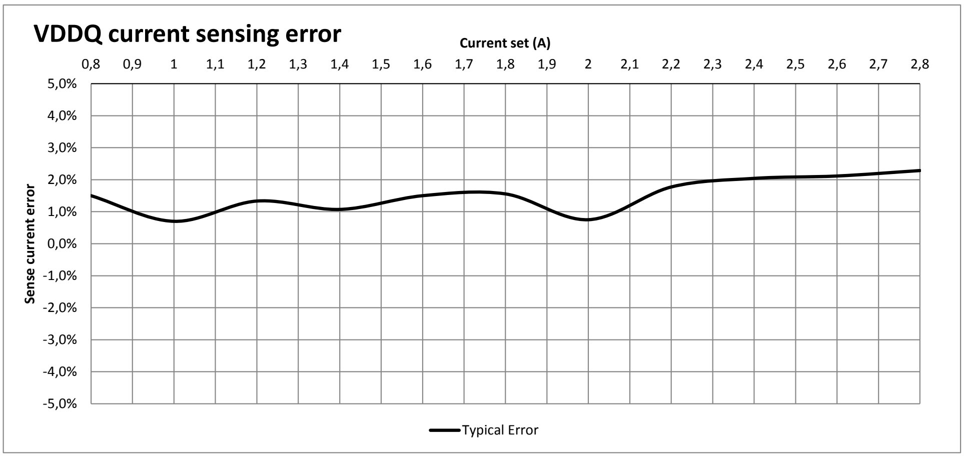


Figure 55: Typical VDDQ Current Sensing Error

12. I2C Interface

12.1 Overview

DA6021 is a slave-only device that is mastered by the SoC. It resides off the SoC's I2C. The slave device implemented on DA6021 side is an asynchronous implementation and will support the high speed mode (3.4MHz). Some of the main features for the I2C slave are:

- DA6021 is accessed using a 7-bit addressing scheme.
- I2C slave is not allowed to stretch the clock, and must be capable of being multi-mastered in a debug environment.
- The interface draws as minimum power when not actively reading/writing registers.
- The slave adapts to the incoming frequency without any communication as the protocol for fast mode and high speed mode is the same.
- 2 Slave Address are supported. Each address is targeting a 256 register page inside DA6021.
- Sequential offset accesses within a single transaction (burst reads and writes) are not required.
- Interface implementation is asynchronous.

12.2 Slave Addresses

DA6021 supports the standard I2C read and write functions. The configuration register space is divided into two 256-byte partitions. DA6021 supports five 7-bit device addresses to access each of the 256 byte partitions. Note that in 8-bit format, these addresses correspond to 0xBC and 0xDC for writes, and 0xBD and 0xDD for reads.

In order to avoid conflict with the assigned addresses the slave addresses will be programmable via OTP.

	Slave address	Read address	Write address
Device 1	0x5E	0xBC	0xBD
Device 2	0x6E	0xDC	0xDD

Table 88: I2C Slave Addresses

The slave addresses need to be locked in order to avoid that software can overwrite them and disable the communication.

12.3 Protocol

Reads from PMIC registers follow the "combined protocol" as described in the I2C specification, in which the first byte written is the register offset to be read, and the first byte read (after a repeat START condition) is the data from that register offset. See the figures below for details. The following diagrams capture the different high-speed and fast-speed transaction format/protocol

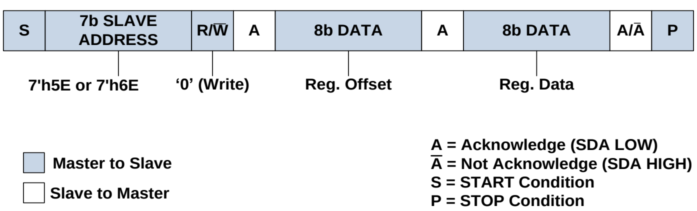


Figure 56: I2C Fast Speed Write

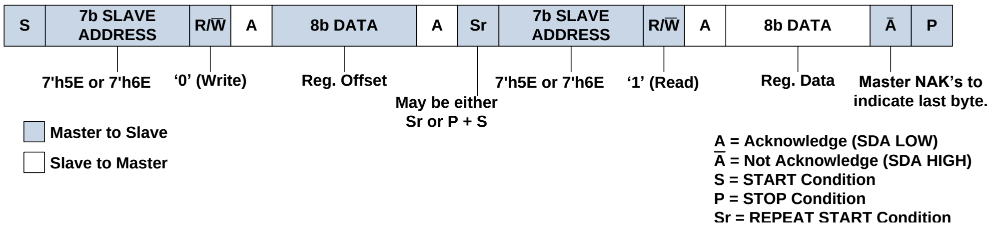


Figure 57: I2C Fast Speed Read

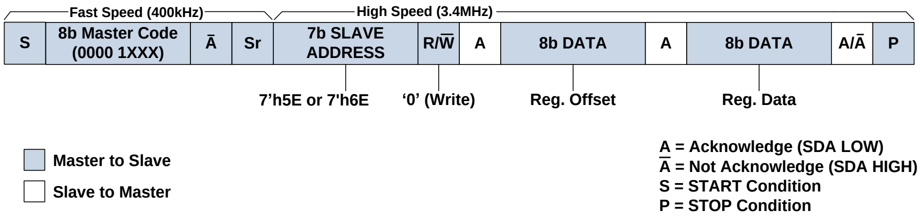


Figure 58: High Speed Write

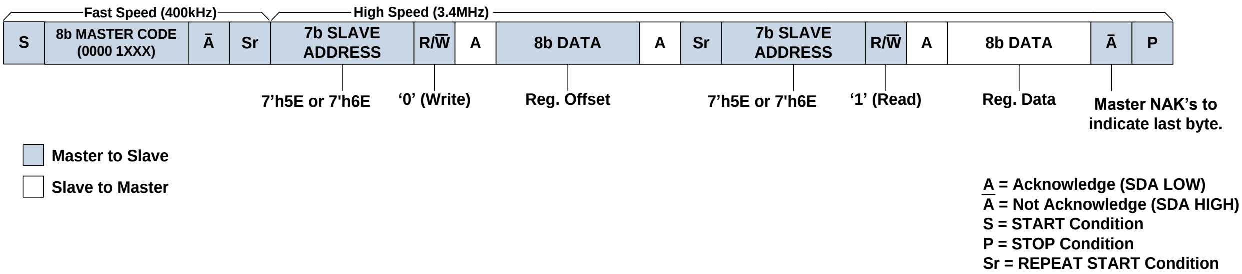


Figure 59: High Speed Read

12.4 Electrical Requirements

Parameter	Min	Nom	Max	Units	Notes	Val
Voltage (VDD)	1.71	1.8	1.89	V	At pin	-
Vil			0.3*VDD	V		A
Vih	0.7*VDD			V		A
Vhys	0.1			V		D,E
Vol			0.2*VDD	V		A
Cpin	2		5	pF		D,E
Tfall_hs	10		40	ns	3.33 Mb/s Operation	E
Tfall_fs	20		300	Ns	400 Kb/s Operation	E
Tr/Tf	30		70	%	Measurement Points	E

Table 89: I2C Signal Electrical Specification

13. External EEPROM Controller

13.1 Overview

During the initial power-on sequence the content of the OTP is copied into the sequencer execution registers. As the OTP registers can be programmed only during manufacturing & testing process, the EEPROM controller function provides the possibility in overwriting the sequencer execution registers in the field and/or as backup.

During initial power-on the EEPROM access will always be interrogated. EEPROM reading and register copying depend on a valid signature inside the EEPROM. Therefore the EEPROM has to be supplied from a dedicated external power rail or directly from the main battery. If no valid signature is read, DA6021 operates with the register setting based on the OTP registers.

13.2 Electrical Characteristics

Parameter	Min	Nom	Max	Units	Notes	Val
Voltage	1.71	1.8	1.89	V	At pin	-
Vil			0.3*VDD1	V		A
Vih	0.7*VDD1			V		A
Vhys	0.1			V		D,E
Vol			0.2*VDD1	V		A
Cpin	2		5	pF		D
fmax			125	kHz		D,E
Trise_fs	20		300	Ns	Pull-up resistor is integrated in DA6021	D,E
Tfall_fs	20		300	ns	Full Speed Operation	D,E
Tr/Tf	30		70	%	Measurement Points	D,E

Table 90: EEPROM Signal Electrical Specifications

13.3 Functions

- The internal CLKGEN provides a 125kHz clock signal to the EEPROM I2C master clock output.
- An EEPROM read is internally initiated by DA6021 power sequence state machine.
- EEPROM initial address EEPROM_SIGN_ADDR, defined by Register Bit written by OTP is read first to see if EEPROM is connected and data at initial address is correct. If one of these two conditions is not fulfilled, EEPROM data will not be copied to register.
- In case EEPROM is connected and data at initial address SIGN_ADDR is correct, EEPROM content from SIGN_ADDR + 1 to end address STOP_ADDR will be copied to register starting at address defined by register SIGN_ADDR = SIGN_ADDR + 1.
- There is a status register in DA6021 implemented indicating the status of EEPROM connection, the signature matching and data copying.

14. Power Source Detection

14.1 Overview

There are three input supply sources that can be detected by DA6021: VBAT, VDCIN_SENSE and VBUS_SENSE referring respectively to the battery, AC adapter and USB connector. For all power sources dedicated comparators are used for the power detection. All detectors include de-bounce logic with a nominal time period of 100ms which can be disabled by software.

14.2 VBAT Power Source Detection

14.2.1 Battery Voltage Monitor & Removal / Insertion Detection

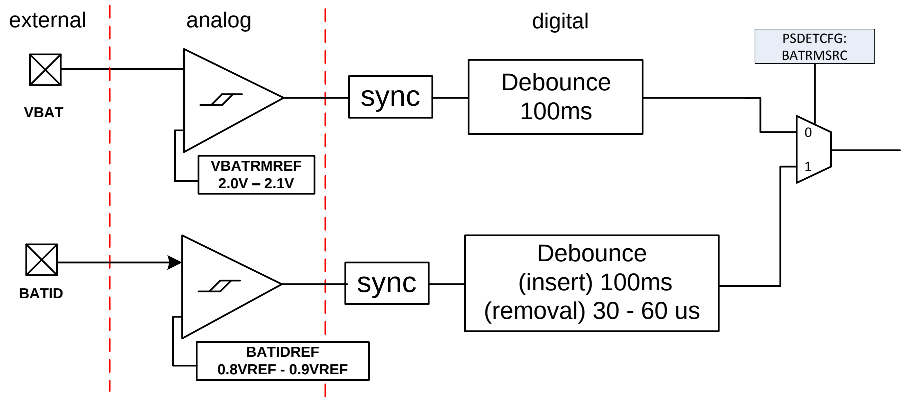


Figure 60: VBAT Input Detection

It is advantageous to use a battery pack with integrated BSI resistance (pull-down in the battery pack indicating the ID or size) as it offers an advanced warning on battery removal events. Such an implementation is necessary to meet the SDWN_B signal timing requirement of some modem SIM cards.

During normal operation (battery pack present/inserted), the BSI resistance in the battery pack pulls the analog voltage at the BATID pin to an intermediate voltage, between VREF (ADC bias voltage from the VREFB pin) and GND. When the BSI terminal of the battery pack no longer makes contact (as on removal), BATID is immediately pulled high to VREF by the measurement resistance on the platform, R_{MBI} (30KΩ to 200KΩ).

While using the BATID comparator sensing the battery insertion / removal, there are separate de-bounce times for insertion and removal. This provides sufficient power-up time for USB PHY related components on insertion, on the other hand it allows a quick detection time of battery removal for SIM card early warning (via SDWN_B).

Note that BAITD comparator is giving a low output if the battery is removed.

When BATRMSRC=1 (using BATID comparator), the thresholds in the table below define the present/absent voltage trip points. Note that when using the BATID comparator to sense battery insertion / removal, there are separate debounce times for insertion and removal. This is to allow for sufficient power-up sequencing of USB PHY related components on insertion, and also allow for quick detection of battery removal for SIM card early warning (via SDWN_B).

Parameter	Description	Min	Typ	Max	Unit	Val
V'BATIDREFH	BATID Rising threshold (L->H, indicating battery removal)	Typ-0.025	0.9*Vref	Typ+0.025	V	A
V'BATIDREFL	BATID Falling threshold (H->L, indicating battery insertion)	Typ-0.025	0.8*Vref	Typ+0.025	V	A
tDEBOUNCE insert	BATID Presence Comparator Debouncing Time (Insertion)	90	100	110	ms	A
tDEBOUNCE remove	BATID Presence Comparator Debouncing Time (Removal)	30		62	µs	A

Table 91: BATID Comparator Threshold

The second method detecting a battery removal is while monitoring the battery voltage itself via a battery voltage comparator. The table below specifies the thresholds of the battery removal comparator.

Parameter	Description	Min	Typ	Max	Unit	Val
V'BATRMREFH	VBAT Rising Threshold (L->H, indicating battery insertion)	2.075	2.1	2.125	V	A
V'BATRMREFL	VBAT Falling Threshold (H->L, indicating battery removal)	1.975	2.0	2.025	V	A
tDEBOUNCE	Battey Voltage Comparator Debouncing Time (Insertion and removal)	90	100	110	ms	A

Table 92: VBAT Removal Comparator Threshold

14.2.2 Battery Pack Interface

The BATID pin supports three possible functions: digital battery communication, analog measurement of an ID resistance, and/or analog battery presence detection.

This digital communication is intended to be left generic, with simple pass through level shifters to/from the host on 2 discrete pins, one to the SOC and one from the SOC. The intent is to be protocol agnostic to provide support for many standards. The figure below illustrates the multiple uses of BATID.

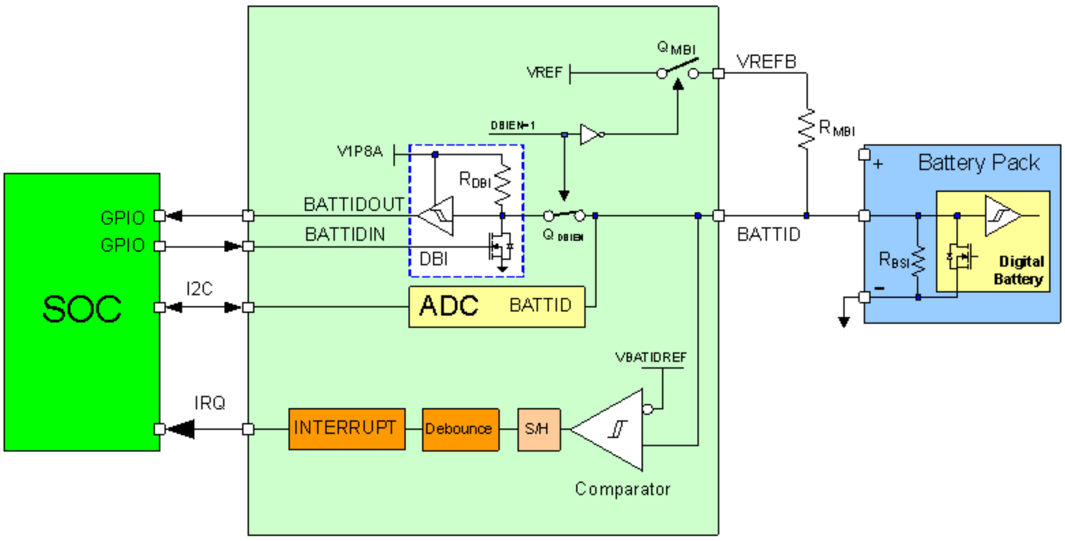


Figure 61: Battery Single Wire Block Diagram for Analog sensing, Digital communication

Parameter	Min	Nom	Max	Units	Notes	Val
Frequency	3.268		250	kHz	Digital communication	D, E
Voltage	1.71	1.8	1.89	V		-
Vil			0.35	V		A
Vih	0.9			V		A
Vhys	0.05			V		D,E

Vol			0.1	V	1mA source current	A
Cload			380	pF		D,E
Trise			500	ns	0V to Vih(min)	D,E
Tfall			500	ns	Vpu to Vil(max)	D,E

Table 93: BATID Electrical Specification

14.2.3 Battery Presence Detection

Normally the BSI resistor will pull the voltage on the BATID line to a level that is lower than a set trip point. If the battery is removed, the BATID node will be pulled high by the R_{MBI} platform resistor which is typically in the range of 30KΩ to 200KΩ. When this occurs, DA6021 detects that the battery is being removed (if configured). The integrated 100ms de-bounce logic ensures there are no false removal alerts.

Depending on the DA6021 setting either a complete Cold Off sequence will be performed or an interrupt to the SOC will be sent.

If the DBIEN bit be set, allowing digital battery communication mode to be entered on the BATID pin, the battery presence logic is switched off to avoid battery removal detection. Prior to Digital Battery Communication, DA6021 retains the last known BATID line voltage value in order to ensure that no false battery removal events are reported.

14.2.4 BSI Sensing

DA6021 is able to detect the presence of the R_{BSI} resistor as shown. The R_{BSI} is a 1% resistor and can range anywhere from 0 to 130kΩ. DA6021 is able to differentiate between different ID resistances (assuming standard 1% values over the aforementioned range).

14.2.5 Digital Battery Communications

DA6021 includes level shifting hardware that will take the single BATID line and convert it to two unidirectional 1.8V I/O signals, BATIDIN and BATIDOUT. The SOC will communicate with the battery digital interface via DA6021 which is transparent and shifts the signals from the battery voltage domain to the 1.8V SOC domain. GPIO0P1 and GPIO0P2 pins are used for this function.

Software, based on the value of the BSI resistance discovered, may choose to enable digital battery communication.

Whenever digital communication is enabled (DBIEN bit in the BATDETCTRL register), DA6021 disables the analog BATID presence sensing logic, and not falsely report removal events.

Parameter	Min	Nom	Max	Units	Notes	Val
Voltage (VDD)	1.71	1.8	1.89	V	At pin	-
Vil			0.3*VDD	V		A
Vih	0.7*VDD			V		A
Vhys	0.1			V		D,E
Vol			0.2*VDD	V		A
Voh	VDD-0.45			V		
Trise	20		300	ns		D,E
Tfall	20		300	ns		D,E
Tr/Tf	30		70	%	Measurement Points	

Table 94: Digital Battery Interface Specification

14.2.6 System Voltage Monitor

For the system voltage comparator is meaningful to be acknowledged once the VSYS is considered valid. This can be done via simple comparator and fixed thresholds. For lower threshold the behavior must be seen together with the POR.

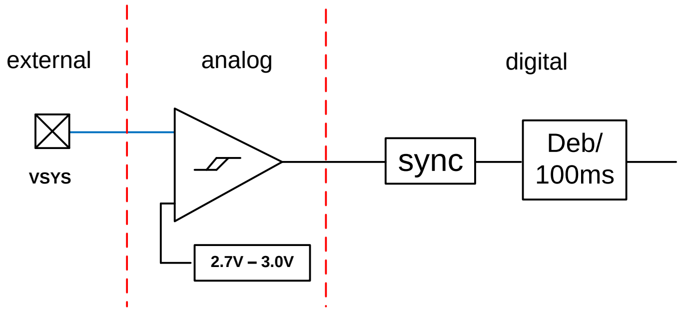


Figure 62: VSYS Valid Input Power Detection

Parameter	Description	Min	Typ	Max	Unit	Val
VSYSREFH	VSYS Rising Threshold (VSYS: L->H)	2.975	3.0	3.035	V	A
VSYSREFL	VSYS Falling Threshold (VSYS: H->L)	2.675	2.70	2.725	V	A
tDEBOUNCE	VSYS comparator debouncing time	90	100	110	ms	A

Table 95: VSYSREF Definition

14.3 VBUS Power Source Detection

Following is the diagram of the VBUS voltage detection.

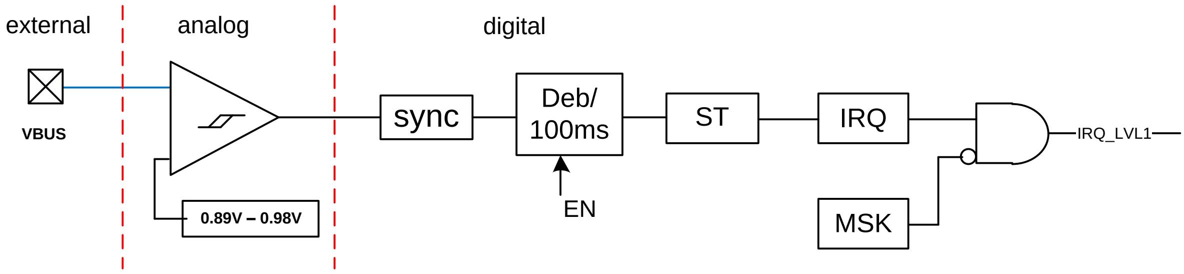


Figure 63: USB Detection

VBUS Rising (Connection Event)
When the VBUS level at the comparator becomes higher than reference voltage (including rising edge hysteresis), VBUS is considered valid. If the VBUSDBEN bit is set in the VBUSDETCTRL register, VBUS must be sensed as valid for the full 100ms de-bounce time before the SVBUSDET bit in the SPWRSRCIRQ register is set, indicating charger connection. If VBUSDBEN is cleared, SVBUSDET is set immediately upon VBUS becoming valid.

VBUS Falling (Disconnection Event)
When the VBUS level at the comparator becomes lower than reference voltage (including falling edge hysteresis), VBUS is considered invalid. If the VBUSDBEN bit is set in the VBUSDETCTRL register, VBUS must be sensed as invalid for the full 100ms de-bounce time before the SVBUSDET bit in the SPWRSRCIRQ register is cleared, indicating charger disconnection. If VBUSDBEN is cleared, SVBUSDET is cleared immediately upon VBUS becoming invalid.

On any change in the SVBUSDET bit in the SPWRSRCIRQ register (set or clear), the corresponding interrupt flag, VBUSDET, is set in the PWRSRCIRQ 2^{nd}-level interrupt register. This automatically sets the PWRSRC interrupt flag in the IRQLVL1 interrupt register, and alerts the SOC. The SOC is expected to query the SVBUSDET bit in SPWRSRCIRQ to determine if the event was a connection or disconnection.

Analog electrical parameters:

Parameter	Symbol	Condition	Min	Typ	Max	unit	Val
Static parameters							
Rising Threshold			895	940	990	mV	A
Falling Threshold			810	860	900	mV	A
Hysteresis			65	80	90	mV	D,E
Dynamic parameters							
Rising Delay			1	10	20	us	D,E
Falling Delay			1	10	20	us	D,E

Table 96: VBUS Detection, Analog Electrical Parameters

14.4 VDCIN Power Source Detection Comparators

The VDCIN_SENSE detection will be done in a similar fashion as for the VBUS.

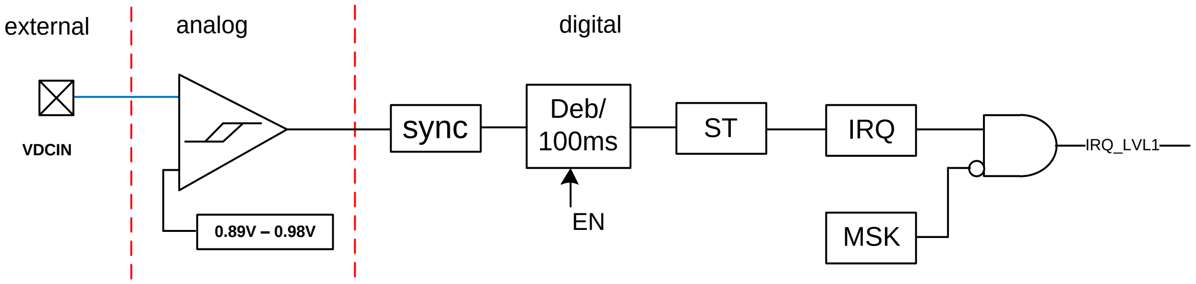


Figure 64: DCIN Detection

The same sequence of operation as in the case of the VBUS will be followed to decide on the booting. After detecting the DCIN an IRQ on removal / Insertion event will be generated.

VDCIN Rising (Connection Event)
When the VDCIN level at the comparator becomes higher than the reference voltage (including rising edge hysteresis), VDCIN is considered valid. If the VDCINDBEN bit is set in the VDCINDETCTRL register, VDCIN must be sensed as valid for the full 100ms de-bounce time before the SDCINDET bit in the SPWRSRCIRQ register is set, indicating adapter connection. If VDCINDBEN is cleared, SDCINDET is set immediately upon VDCIN becoming valid.

VDCIN Falling (Disconnection Event)
When the VDCIN level at the comparator becomes lower than the reference voltage (including falling edge hysteresis), VDCIN is considered invalid. If the VDCINDBEN bit is set in the VDCINDETCTRL register, VDCIN must be sensed as invalid for the full 100ms de-bounce time before the SDCINDET bit in the SPWRSRCIRQ register is cleared, indicating charger disconnection. If VDCINDBEN is cleared, SDCINDET is cleared immediately upon VDCIN becoming invalid.

On any change in the SDCINDET bit in the SPWRSRCIRQ register (set or clear), the corresponding interrupt flag, DCINDET, is set in the PWRSRCIRQ 2nd-level interrupt register. This automatically sets the PWRSRC interrupt flag in the IRQLVL1 interrupt register, and alerts the SOC. The SOC is expected to query the SDCINDET bit in SPWRSRCIRQ to determine if the event was a connection or disconnection.

Analog electrical parameters:

Parameter	Symbol	Min	Typ	Max	unit	Val
VDCIN Rising Threshold (VDCIN: L->H)	VDCINREFH	895	940	990	mV	A
VDCIN Falling Threshold (VDCIN H->L)	VDCINREFL	810	860	900	mV	A
debouncing		90	100	110	ms	A

Table 97: VDCIN Detection, Analog Electrical Parameters

14.5 BATLOW Definition

Once detection is done, according to the supply configuration, the ADC will be triggered to measure the VBAT voltage. The result register will be compared with one of the four possible threshold levels defined to generate the BATLOW signal. This is needed in order to decide if we can boot or not. Below a figure with the levels and the explanation for the different LOWBAT levels

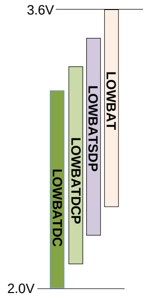


Figure 65: Valid Battery Thresholds

- **LOWBAT**: No supply source detected apart from the main battery.
- **LOWBATSDP**: VBUS_SENSE detected and USB is of the SDP type.
- **LOWBATDCP**: VBUS_SENSE detected and USB is of the DCP, CDP or ACA type.
- **LOWBATDC**: VDCIN_SENSE is detected so an AC adapter is connected.

After every battery measurement the result will be compared with the corresponding thresholds. If the system is running on AC/DC plug or USB supply the VBAT input voltage is measured frequently with the ADC. If the level drops below an appropriate threshold the PMIC will assert the BATLOW pin, the processor will then take action. All thresholds are preprogrammed in OTP and can be overwritten by software.

14.6 Power Source Detection Events

The events generated from the Power Source Detection Logic and driven into the event interface are:

- Battery Insertion Event.
- Battery Removal Event.
- USB Insertion Event.
- USB Removal Event.
- DCIN Insertion Event.
- DCIN Removal Event.
- VSYS Valid Event

All power source detection events will generate an Interrupt towards the SoC

- Battery wake-up
- AC/DC wake-up
- USB wake-up

14.7 Wake-Up Logic

In order to make decision about the wakeup, SYSCO takes status information regarding power supply source and the power button and event generated from these. Following table shows the wakeup decision.

Events	Condition to be Fulfilled	Comments
Battery Insertion	• BATWAKEEN = 1 • BATLOW_B = 1	Regardless of other power supplies status.
AC Adapter Insertion	• ADPWAKEEN = 1 • BATLOW_B = 1 • DCBOOT = 0	Dependency on battery status
	• ADPWAKEEN = 1 • BATLOW_B = 1 • DCBOOT = 1	No dependency on battery status
USB Insertion	• USBWAKEEN = 1 • BATLOW_B = 1 • Battery Present.	Wakeup is not allowed if we are running only on USB.
Battery Becomes Valid	• BATLOW_B = 1 • ADPWAKEEN = 1	Battery present. AC/DC insertion event (DCBOOT = 0). The wakeup is only delayed till battery is charged enough (VBAT > BATLOW)..
	• BATLOW_B = 1 • USBWAKEEN = 1	Battery present. USB insertion event. The wakeup is only delayed till battery is charged enough.
Power Button	• BATLOW_B = 1	System running on battery
	• PWRBTNWAKE.USBWAKE = 01 • PWRBTNWAKE.USBWAKE = 10	Battery present and charging from USB. Battery not charged enough. 01 = DCP charging wakeup 11 = SDP (500mA) charging wakeup With 100mA USB source there is not boot possible.
	• PWRBTNWAKE.ACDCWAKE = 1 • DCBOOT = 0	Battery present and charging from AC/DC. Battery still not charged enough.
	• DCBOOT = 1 • BSTRMDETRN = 0	Wakeup immediately

Table 98: System Wake-Up Condition

It is assumed that DA6021 is in SOC_G3 and VSYS is valid. Such wake-up event will be generated even if the system is in SOC_S4, SOC_S3 and SOC_SX. Wake-up is completely under the control of the processor.

A power button event is forwarded to the SOC via the DA6021 PWRBTN_B output pin and SOC will take the action. In case of an event other than the power button an interrupt towards the SoC will be generated.

Following the wake-up signal generation in SOC_G3:

1. Power Source Detection Logic detects an event (power button or power source insertion)
2. ADC is triggered to measure VBAT
3. ADC will provide the measurement result is available
4. Power Source detection Logic compares the measurement result with the programmed LOWBAT value, according to the available source
5. Issue a wake-up event notifying the wake-up source

This will be done only if in SOC_G3 and there is no need to measure the VBUS and DCIN. In case of USB insertion and the battery measurement gives as result battery low Power Source Detection Logic will trigger the ADC every 4 second. As this is not critical time an error of 100ms is tolerated.

14.8 DA6021 Catastrophic and Critical Events

There are 9 “catastrophic and critical events” which may force an immediate Cold Off, i.e. force an immediate hardware-controlled VR shutdown, or simply alert the SOC. Four of these events – BCU VCRIT, BATRM, System TEMP and battery TEMP – may have configurable action, programmed via the I2C register map. These events are split into two categories: “Catastrophic” and “Critical”

Catastrophic events are:

- THERMTRIP_B - The SOC asserts THERMTRIP_B in response to an SOC over-temperature condition. DA6021 asserts SDWN_B immediately. After 90us, shuts down all VRs.
- PMICTEMP – DA6021 detects a critical over-temperature condition on its internal die sensor and asserts SDWN_B immediately. After 90us, shuts down all VRs.
- System TEMP – DA6021 detects a critical over-temperature condition on an external system thermistor. If programmed DA6021 asserts SDWN_B immediately. After 90us, shuts down all VRs.
- Battery TEMP – DA6021 detects a critical over-temperature condition on an external battery thermistor. If programmed DA6021 asserts SDWN_B immediately. After 90us, shuts down all VRs.
- VSYSUVP – DA6021 detects VSYS “undervoltage” (VSYS ≤ 2.7V) by VSYS under voltage hard-coded comparator for more than 100µs.DA6021 asserts SDWN_B immediately. After 90us, shuts down all VRs.
- VSYSOVP – DA6021 detects VSYS “overvoltage” (VSYS ≥ 5.4V min) by VSYS over voltage hard-coded comparator for more than 100µs.DA6021 asserts SDWN_B together with shutting down all VRs immediately.
- VBATRM – DA6021 detects that a battery was removed from the system by VBAT comparator when the bit BATRMSRC in the PSDETCTRL register is cleared (=0). If BATRMPDEN is set (=1), DA6021 asserts SDWN_B immediately. After 90us, shut down all VRs. If BATRMPDEN is cleared, DA6021 operates without detecting a valid battery is present ONLY if an AC/DC adapter (SDCINDET_B=1), therefore no Cold Off in this case. Instead, an interrupt is sent to the SOC (assuming unmasked, via the normal behavior of the SBATDET bit). However, even if BATRMPDEN is cleared, a Cold Off will still be executed if no AC/DC adapter is detected (SDCINDET_B=0).

Critical events are:

- IDBATRM – DA6021 detects that a battery was removed from the system by BATID presence comparator when the bit BATRMSRC in the PSDETCTRL register is set (=1). All VRs are shut down in sequenced order but without waiting for SLP_S*_B from SOC. If BATRMPDEN is cleared, the PMIC may operate without detecting a valid battery is present ONLY if an AC/DC adapter (SDCINDET_B=1), therefore no Cold Off in this case. Instead, an interrupt is sent to the SOC (assuming unmasked, via the normal behavior of the SBATDET bit). However, even if BATRMPDEN is cleared, a Cold Off will still be executed if no AC/DC adapter is detected (SDCINDET_B=0)
- BCU VCRIT – The BCU detects that the VSYS voltage node has entered the “VCRIT” operating zone. If the VCRITCFG register in the BCU configuration space is set to enable shutdown action, All VRs are shut down in sequenced order but without waiting for SLP_S*_B from SOC. If VCRITCFG is not set to enable shutdown action, only an interrupt is sent to the SOC (via the normal method).

14.9 Power Source Registers

Register Name		**PWRSRCIRQ**		Address	**0x03 Page 1**	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R/W	R/W	R/W
reserved					BATDET	DCDET	VBUSDET
VBUSDET		**0** 1	No change Change in connection status				
DCDET		**0** 1	No change Change in connection status				
BATDET		**0** 1	No change Change in connection status				

Register Name		**MPWRSRCIRQS0**		Address	**0x0F Page 1**	Read/Write	
				Reset Value	0x07		
MSB							LSB
R	R	R	R	R	R/W	R/W	R/W
Reserved					MBATDET _S0	MDCDET _S0	MVBUS DET_S0
MVBUSDET_S0		0 **1**	VBUS detection not masked, S0 mode only VBUS detection masked, S0 mode only				
MDCDET_S0		0 **1**	AC/DC adapter detection not masked, S0 mode only AC/DC adapter detection masked, S0 mode only				
MBATDET_S0		0 **1**	Battery detection not masked, S0 mode only Battery detection masked, S0 mode only				

Register Name	MPWRSRCIRQSX		Address	0x10 Page 1	Read/Write		
			Reset Value	0x07			
MSB							LSB
R	R	R	R	R	R/W	R/W	R/W
reserved					MBATDET	MDCDET	MVBUSDET
MVBUSDET		0 **1**	VBUS detection not masked, sleep modes only VBUS detection masked, sleep modes only				
MDCDET		0 **1**	AC/DC adapter detection not masked, sleep modes only AC/DC adapter detection masked, sleep modes only				
MBATDET		0 **1**	Battery detection not masked, sleep modes only Battery detection masked, sleep modes only				

Register Name	SPWRSRC		Address	0x1E Page 1	Read/Write		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R/W	R/W	R/W
reserved					SBATDET	SDCDET	SVBUSDET
SVBUSDET		**0** 1	VBUS detection status disconnected Connected				
SDCDET		**0** 1	AC/DC detection status disconnected Connected				
SBATDET		**0** 1	Battery detection status disconnected Connected				

Register Name	PSDETCFG		Address	0x25 Page 1	Read/Write		
			Reset Value	0x07			
MSB							LSB
R	R	R	R/W	R/W	R/W	R/W	R/W
reserved		DBIEN	BATRMSRC	BATRMDEN	BATDBEN	VDCINDBEN	VBUSDBEN
VBUSDBEN		0 **1**	VBUS de-bounce window disable VBUS de-bounce window enable				
VDCDBEN		0 **1**	VDCIN_SENSE de-bounce window disable VDCIN_SENSE de-bounce window enable				
BATDBEN		0 **1**	Battery detection de-bounce window disable Battery detection de-bounce window enable				
BATRMDEN		 **0** 1	Battery removal power down enable Disable, take no action upon battery removal. If CHGDET=0 send DCP, if CHGDET=1 then perform a Cold off Enable, perform a cold off				
BATRMSRC		**0** 1	VBAT comparator BATID presence comparator				
DBIEN		**0** 1	Digital battery interface communication disable Digital battery interface communication enable				

Register Name	LOWBATDET0		Address	0x23 Page 1	Read/Write		
			Reset Value	0xCB			
MSB							LSB
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DCBOOT	LOWBATDC			LOWBAT			

LOWBAT[3:0]	0000	2.2V
	0001	2.4V
	0010	2.6V
	0011	2.7V
	0100	2.8V
	0101	2.9V
	0110	3.0V
	0111	3.1V
	1000	3.2v
	1001	3.3V
	1010	3.4V
	1011	**3.5V**
	1100	3.6V
	1101	3.7V
	1110	3.8V
	1111	3.9V
LOWBATDC[2:0]	000	2.2V
	001	2.4V
	010	2.6V
	011	2.8V
	100	**3.0V**
	101	3.2V
	110	3.4V
	111	3.6V
DCBOOT	0	System boot depending on battery setting by LOWBAT[3:0] when AD/DC adapter is plugged in
	1	System boot enable with AD/DC adaptor alone, no battery required

Register Name	LOWBATDET1		Address	0x24 Page 1	Read/Write		
			Reset Value	0x8A			
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
LOWBATDCP				LOWBATSDP			

LOWBATSDP[3:0]	0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 **1010** 1011 1100 1101 1110 1111	2.2V 2.4V 2.6V 2.7V 2.8V 2.9V 3.0V 3.1V 3.2V 3.3V **3.4V** 3.5V 3.6V 3.7V 3.8V 3.9V
LOWBATDCP[3:0]	0000 0001 0010 0011 0100 0101 0110 0111 **1000** 1001 1010 1011 1100 1101 1110 1111	2.2V 2.4V 2.6V 2.7V 2.8V 2.9V 3.0V 3.1V **3.2V** 3.3V 3.4V 3.5V 3.6V 3.7V 3.8V 3.9V

Register Name		SRCWAKECFG		Address	0xDB Page 0	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R/W	R/W	R/W
reserved	reserved				ADP WAKEEN	USB WAKEEN	BAT WAKEEN

BATWAKEEN	**0** 1	System won’t wake up when battery insertion is detected System wakes up when battery insertion is detected and boot conditions are met
USBWAKEEN	**0** 1	System won’t wake up when USB charger insertion is detected System wakes up when USB charger insertion is detected and boot conditions met
ADPWAKEEN	**0** 1	System won’t wake up when AC/DC adapter insertion is detected System wakes up when AC/DC adapter insertion is detected and boot conditions are met

Register Name	RESETSRC0			Address	0x20 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R	R
reserved	RVBATRM	RVSYSOVP	RVSYSUVP	RBATTEMP	RSYSTEMP	RPMICTEMP	RTHERMTRIP

RTHERMTRIP	**0** 1	 Previous immediate shutdown due to SOC THERMTRIP_B
RPMICTEMP	**0** 1	 Previous immediate shutdown due to PMIC over temperature
RSYSTEMP	**0** 1	 Previous immediate shutdown due to system over temperature
RBATTEMP	**0** 1	 Previous immediate shutdown due to battery over temperature
RVSYSUVP	**0** 1	 Previous immediate shutdown due to VSYS under voltage
RVSYSOVP	**0** 1	 Previous immediate shutdown due to VSYS over voltage
RVBATRM	**0** 1	 Previous immediate shutdown due to battery removal

Register Name	RESETSRC1			Address	0x21 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R	R
reserved					RFCO	RIDBATRM	RVCRIT

RVCRIT	**0** 1	Default Previous shutdown was due to violation of the VCRIT threshold as programmed in the BCU configuration
RIDBATRM	**0** 1	 Previous shutdown was due to battery removal event detected by BATID comparator
RFCO	**0** 1	 Previous shutdown was due to user holding down the power button

Register Name	WAKESRC			Address	0x22 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R	R
reserved				WAKEADP	WAKEUSB	WAKEBAT	WAKEBTN

WAKEBTN	**0** 1	 Wake-up triggered by power button
WAKEBAT	**0** 1	 Wake-up triggered by battery insertion
WABEUSB	**0** 1	 Wake-up triggered by USB charger insertion
WAKEADP	**0** 1	 Wake-up triggered by AC/DC adapter insertion

15. Analog–to–Digital Converter

A general purpose analog-to-digital converter (GPADC) provides measurements of various voltages, currents and temperatures within the device. There is one 10-bit ADC which is time-division multiplexed to perform the measurements of the various parameters. The GPADC contains the 10-bit ADC, the analog input channel multiplexer and some additional analog functions.

The digital ADC block automates the measurement process by overlaying a sequencer function. It performs some automatic measurements at predefined sequence points, if enabled. Besides that, the host can initiate manual measurements at certain points in the sequence. The ADC replaces some on-chip comparator used for internal purpose so in addition to the automatic measures initiated by the host, internal measure sequences are processed, too.

The automatic measurements can raise interrupts if the measurement is outside of configurable thresholds.

The digital block controls the analog-to-digital (AD) conversion process. This allows testing the conversion logic via scan tests.

When powering down the device the digital ADC block may stop the measurements and disable the GPADC in order to reduce the power consumption. This feature is controlled by the Power Supply Sequencer (PSS) and some registers.

15.1 Electrical Characteristics

PARAMETER	SYMBOL	TEST CONDITIONS	Min	Typ	Max	UNIT	Val
ADC Resolution				10		bit	D,E
Absolute Accuracy			12		15	mV	A
Integral Non-Linearity	INL			+/- 2		LSB	A
Differential Non-Linearity	DNL			+/- 0.8		LSB	A
ADC Supply Voltage				2.5		V	-
ADC Reference Voltage	VADC_REF	VDD_CORE		2.5		V	-
ADC Operating Current		during conversion		100		µA	D
Power Down Current					1	µA	D
ADC Clock				1		MHz	D
Auto-Zero Time				3		us	D
Total Sampling Time		including the Auto-Zero time		10		us	D
Conversion Time				11		us	D
Total ADC Conversion Time				21		us	D
Maximum Source Impedance	R_S	RS is the impedance of the external source sampled by the ADC			120	kΩ	D
Internal Mux Resistance	R_{INT}			5		kΩ	D
Internal Sampling Capacitor	C_S			10		pF	D
Total Input Capacitance	C_{INT}	parasitic and pad capacitance included		11		pF	D
Acquisition Time		~7τ = 7 x (RS + RINT) x CINT			10	us	D
VSYS Voltage Range / channel A0 /		ADC=[(VSYS-2.5) x 0.5] x 1023	2.5		5.5	V	A

		gain = 0.8					
ADC_IN1÷3 Voltage Range / channels A1, A2, A3 /		ADC=[VIN / 2.5] x 1023 gain = 1.0	0		2.5	V	A
Internal Temp. Sensor Voltage / channel A4 /		ADC=[1 – 1.2 x VTJ] x 1023 gain = 3.0	0		0.833	V	A
VBBAT Voltage Range / channel A5 /		ADC=[1 - 0.2 x VBBAT] x 1023 gain = 0.5	0		5	V	A
Inter Channel Isolation		80dB for channel A3 (ADC_IN6)		60		dB	D
Regulator OV/UV monitoring Channel A8 ÷ A10		Gain =0.5	0		5.5	V	

Table 99: ADC Electrical Charakteristics

15.2 Analog Overview

The AD conversion is of successive approximation type using sample and hold. It has a resolution of 10 bits and a conversion cycle of 21 clock cycles including an auto-zero phase (23 cycles consumed back-to-back). The GPADC is supplied from the same supply, VDDCORE, as the digital block. If unused, the GPADC can be disabled to reduce its power consumption by a factor around 100.

The GPADC has an analog input multiplexer with in total 16 input channels.

CH	Description	Signal name	Measurement range	Cond.	Comment	ADC value	Gain
0	Battery Voltage, VBAT (Pin: IBATSENSE)	VREG	0.0V.. 5.0V	YES		0.5* Vin/VLP*1023	0.5
1	Battery ID (Pin: BATID)	ADCIN1	0.0V .. VLP	NO	VREFB needs to be switched on 1ms prior to ADC measurement. VREFB needs to stay on when battery removal has to be detected by the VBATID Comparator.	Vin/VREFB*1023	1
2	DA6021 Die Temperature (no pin)	vbe_ADC/ adc_temp	0.0V .. VLP/3	YES		3* Vin/VLP *1023	3
3	Battery Pack Temp 0 (Pin: BPTHERM0)	ADCIN2	0.0V .. VLP	NO	VREFT needs to be switched on 1ms prior to ADC measurement.	Vin/VREFT *1023	1
4	Battery Pack Temp 1 (Pin: BPTHERM1)	ADCIN3	0.0V .. VLP	NO		Vin/VREFT*1023	1
5	System Temp 0 (Pin: SYSTHERM0)	ADCIN4	0.0V .. VLP	NO		Vin/VREFT*1023	1
6	System Temp 1 (Pin:	ADCIN5	0.0V .. VLP	NO		Vin/VREFT*1023	1

	SYSTHERM1)						
7	System Temp 2 (Pin: SYSTHERM2)	ADCIN6	0.0V .. VLP	NO		Vin/VREFT*1023	1
8	VSYS (Pin: VSYS)	VSYS	2.5V .. 5.5V	YES		0.8*(VSYS - VLP)/VLP*1023	0.8
9	Averaging output current	ADCIN7	0.0V .. VLP	YES	There is a pre-selection on which rail the current measurement will be averaged	2*Vin/VREF*1023	2

Table 100: ADC Channel Overview

The ADC is used for temperature, current and voltage measurements. It is managed by the DA6021 ADC state machine. The state machine performs ADC operations are, like regular readings of temperatures, current and voltage, programmed in registers and may be modified by the SOC after boot and initialization. The ADC state machine is an independent hardware engine which prevents the management of lengthy ADC transactions from blocking time-critical power sequencing tasks.
The GPADC will be used to perform the following tasks:

1. Repeated (on-going) battery temperature acquisition (initiated via timer defined in THRMMONCTL)
2. Repeated (on-going) system temperature acquisition (initiated via timer defined in THRMMONCTL)
3. Repeated (on-going) PMIC die temperature acquisition (initiated via timer defined in THRMMONCTL)
4. Repeated (on-going) VR current acquisition (initiated via timer define VRIMONCTL)
5. SOC-requested acquisition of any GPADC channels (initiated via MANCONV0-1)
6. Thermal Alerts - triggering thermal interrupts when either battery temperatures, system temperatures or PMIC temperature exceed the alert thresholds which are set in corresponding registers, asserts PROCHOT_ B to SOC when enabled
7. Critical Temperature Shutdown – if enabled, triggering system shutdown when either battery temperatures, system temperatures or PMIC temperature exceed the critical temperature thresholds which are set in corresponding registers

15.2.1 ADC Measurement Support

The analog ADC domain includes 2 voltage reference switches VREFB and VREFT. The reference switches for the reference sources are enabled according vrefb/t_en signals.

There is another measurement function which allows comparing the input voltage against a fixed reference voltage. Although this feature is implemented within the analog part of the ADC, it is completely independent from all the scheduler based ADC functions. Because the comparison result may be put out via a pad, the PADS block manages this function instead of the digital ADC block.

15.2.2 Preamplifier

A preamplifier is used for channels with an input range exceeding the ADC input range. The preamplifier is an inverting amplifier so the ADC conversion values for these channels are bitwise inverted before use. For channel 3-7 it includes low pass filtering to reduce impact on platform noise.

Ch	Input	Data Format
0	VBAT	
1	BATID	
2	TPMIC	inverted
3	TBAT0	Inverted
4	TBAT1	Inverted
5	TSYS0	Inverted
6	TSYS1	Inverted
7	TSYS2	Inverted
8	IVCC	
9	IVNN	
10	IV1P0A	
11	IV1P05S	
12	IVDDQ	
13	VSYS	

Table 101: ADC Channel Data Format

15.3 ADC Sequencer

The operation of all ADC functionality is controlled by an independent standalone ultra-flexible ADC sequencer. The sequence has 16 slots and each slot a duration of min t_{slot} = ~64 µs. Each slot contains two steps. First a single automatic measure initiated by the SOC and configured by register settings is performed, second a single (if min t_{slot} = ~64 µs) or multiple (min t_{slot} > 64 µs) internal measure for on-chip functions and decisions might be performed. Whenever there is no automatic or internal measurement, manual measure initiated by the SOC can be performed. If no measurement is performed, the ADC is turning off to reduce power consumption.

The sequencing is configured in such a way that it fulfills the Intel ADC specification and performs automatically measurement at the appropriate time (platform state defendant)

15.3.1 Manual Measurements

An automatic measurement can be assigned to a specific slot while a manual measurement can't. Manual measurements will be performed at free slots or whenever there is space in the internal measure frame. Free slots are unassigned slots, slot with down sampling while not measuring and masked or disabled slots in standby mode. To initiate a manual measurement two separate registers MANCONV0 and MANCONV1 exists, one bit for each ADC Channel. One or more channels can be selected in one register write.

Register Name		MANCONV0		Address	0x72 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SYS THERM2	SYS THERM1	SYS THERM0	BP THERM1	BP THERM0	PMIC TEMP	BATID	VBAT
VBAT		**0** 1	 Initiates manual conversion of VBAT, clears after conversion				
BATID		**0** 1	 Initiates manual conversion of BATID, clears after conversion				
PMICTEMP		**0** 1	 Initiates manual conversion of PMICTEMP, clears after conversion				
BPTHERM0		**0** 1	 Initiates manual conversion of BPTHERM0, clears after conversion				
BPTHERM1		**0** 1	 Initiates manual conversion of BPTHERM1, clears after conversion				

SYSTHERM0	**0** 1	 Initiates manual conversion of SYSTHERM0, clears after conversion
SYSTHERM1	**0** 1	 Initiates manual conversion of SYSTHERM1, clears after conversion
SYSTHERM2	**0** 1	 Initiates manual conversion of SYSTHERM2, clears after conversion

Register Name		**MANCONV1**		Address	**0x73 Page 1**	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R/W	R/W	R/W	R/W	R/W	R/W
reserved		VSYS	IVDDQ	IV1P05S	IV1P0A	IVNN	IVCC

IVCC	**0** 1	 Initiates manual conversion of VCC current, clears after conversion
IVNN	**0** 1	 Initiates manual conversion of VNN current, clears after conversion
IV1P0A	**0** 1	 Initiates manual conversion of V1P0A current, clears after conversion
IV1P05S	**0** 1	 Initiates manual conversion of V1P05S current, clears after conversion
IVDDQ	**0** 1	 Initiates manual conversion of VDDQ current, clears after conversion
VSYS	**0** 1	 Initiates manual conversion of VSYS, clears after conversion

As soon as at least one of the manual register is set, the sequencer starts to measure the first manual channel at the next MAN_TRIGGER from the main state machine. At the end of this first conversion, it puts the result in to the result register related to the channel measured. The next channel selected in the MANCONV register is measured at the next trigger.

Manual measurements include setting an event bit and raising a nIRQ interrupt after end of conversion.

Register Name		**ADCIRQ0**		Address	**0x08 Page 1**	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SYS THERM2	SYS THERM1	SYS THERM0	BP THERM1	BP THERM0	PMIC TEMP	BATID	VBAT

VBAT	**0** 1	 Conversion request for VBAT complete, clear by writing “1”
BATID	**0** 1	 Conversion request for BATID complete, clear by writing “1”
PMICTEMP	**0** 1	 Conversion request for PMICTEMP complete, clear by writing “1”
BPTHERM0	**0** 1	 Conversion request for BPTHERM0 complete, clear by writing “1”
BPTHERM1	**0** 1	 Conversion request for BPTHERM1 complete, clear by writing “1”

SYSTHERM0	**0** 1	 Conversion request for SYSTHERM0 complete, clear by writing “1”
SYSTHERM1	**0** 1	 Conversion request for SYSTHERM1 complete, clear by writing “1”
SYSTHERM2	**0** 1	 Conversion request for SYSTHERM2 complete, clear by writing “1”

Register Name		ADCIRQ1		Address	0x09 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R/W	R/W	R/W	R/W	R/W	R/W
reserved		VSYS	IVDDQ	IV1P05S	IV1P0A	IVNN	IVCC

IVCC	**0** 1	 Conversion request for IVCC complete, clear by writing “1”
IVNN	**0** 1	 Conversion request for IVNN complete, clear by writing “1”
IV1P0A	**0** 1	 Conversion request for IV1P0A complete, clear by writing “1”
IV1P05S	**0** 1	 Conversion request for V1P05S complete, clear by writing “1”
IVDDQ	**0** 1	 Conversion request for VDDQ complete, clear by writing “1”
VSYS	**0** 1	 Conversion request for VSYS complete, clear by writing “1”

Register Name		MADCIRQ0		Address	0x15 Page 1	Read/Write	
				Reset Value	0xFF		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
SYS THERM2	SYS THERM1	SYS THERM0	BP THERM1	BP THERM0	PMIC TEMP	BATID	VBAT

VBAT	0 **1**	 mask channel 0 event
BATID	0 **1**	 mask channel 1 event
PMICTEMP	0 **1**	 mask channel 2 event
BPTHERM0	0 **1**	 mask channel 3 event
BPTHERM1	0 **1**	 mask channel 4 event
SYSTHERM0	0 **1**	 mask channel 5 event
SYSTHERM1	0 **1**	 mask channel 6 event
SYSTHERM2	0 **1**	 mask channel 7 event

Register Name		MADCIRQ1		Address	0x16 Page 1	Read/Write	
				Reset Value	0x3F		
MSB							LSB
R	R	R/W	R/W	R/W	R/W	R/W	R/W
reserved		VSYS	IVDDQ	IV1P05S	IV1P0A	IVNN	IVCC
IVCC		0 **1**	mask channel 8 event				
IVNN		0 **1**	mask channel 9 event				
IV1P0A		0 **1**	mask channel 10 event				
IV1P05S		0 **1**	mask channel 11 event				
IVDDQ		0 **1**	mask channel 12 event				
VSYS		0 **1**	mask channel 13 event				

15.3.2 Reference Source

The reference voltage or current sources for the thermal measurements needs to be enabled at least 1ms before a measurement is performed at the resistive channels. The settling time is handled by the sequencer module.

On manual measure requests the references will be turned on when a measurement of such a channel is requested. The measurement request of such channel will be delayed by 1-2ms by the state machine. The remaining channels will be measured. If the channel counter for the manual measurements has reached this channel before the settling time of 1-2ms, the next channels will be measured first. In this case the channel counter will start again from channel 0 after finishing with channel 8.

The similar approach is used on internal measure request. The request for channels with a reference will be delayed by 1-2ms.

Automatic measurements use a different approach. There the channels with a reference will delayed by an entire cycle. So when they are due to be measured, the reference will be turned on and the measurement will be done on the next appearance of that slot. In case the channel is measured on each cycle, the reference keeps on all the time.

15.3.3 Event and Status Generation

Some channels contain event and status information in automatic measure mode when a predefined result threshold is exceeded. The status information is stored in read only registers. In case a measurement exceeds a certain threshold, the status flag is set. If the measurement is in normal range again, the status flag is cleared. The status information on auto measures is handled in the SVTM module.

Along with a change of a status an event is generated and flagged to SOC via an interrupt port. The event register is usually generated on both edges of a status change if not otherwise stated. The event register of automatic measures is handled by SVTM. The ADC generates interrupts on manual measure only. These interrupt flags are send to the event interface and are 1MHz pules only. The handling of the event pulses is done in the IRQ module.

The SOC needs to write a ‘1’ to the event register to serve and clear the event. This clears the interrupt line, too if there is not another interrupt request pending.

As with all event registers in the DA6021 device, a Mask bit to disable the event and interrupt generation exists.

15.3.4 Result register

Each channel has an individual 10 bit result register. Each result of an automatic, internal or manual measurement will simply be stored into the according result register after end of conversion no matter where the measurement is initiated from. So always the newest value is represented in the result register. All result registers are split to two register addresses with 2 bit MSB and 8 bit LSB.

In case a LBUS read access appears on one of the 2 result register addresses of a channel, MSBs and LSBs of result register of that channel will be locked for internal accesses from the ADC. So no result will be written to these registers in this case. The sequencer will not be interrupted. All other ADC results of that channel will be lost if a register is locked and a result is due to be stored. Since the result of a manual measurement cannot be stored in case the result register of this channel is locked, no interrupt will be generated and the manual request register will not be cleared. This channel will be measured until the result register can be accessed.

If another LBUS read access is detected on this or another register, the result register will be unlocked again. All locks will be cleared when entering SOC_G3.

15.3.5 CH0: Battery Pack Voltage

The Battery Pack Voltage measurement requires the preamplifier to be turned on with a gain of 0.5.

Battery Pack Voltages is internally measured every 4s in all active and standby states S4-S0.

15.3.6 CH1: Battery ID resistance

The Battery ID resistance measurement requires the Voltage Reference VREFB to be turned on at least 1ms before a measurement is initiated. Instead of the Voltage Reference a Current Source ISRCB can be used. This is selected by bit CALIB.ISRC_ENA

15.3.7 CH2: Die Temperature

The DA6021 die temperature thermistor has an alert event register EPMICALRT that flag an interrupt when the according temperature threshold PMICALRT is exceeded. In case temperature exceeds one of the thresholds, the status register SPMICALRT and the event register EPMICALRT are set and an Interrupt is generated to the SOC. A hysteresis is implemented for this event, so the status is cleared and another event is generated when the temperature falls below the PMICALRT + PMICHYS threshold.

Note, high temperature means low ADC result values.

15.3.8 CH3-4: Battery Pack Temperature

A critical event is implemented with an upper and a lower threshold defined in THRMBATCRIT registers. In case temperature exceeds one of the thresholds, the charger is turned off, the status register SBATCTRITALRT and the event register EBATCTRITALRT are set and an Interrupt is generated to the SOC. The status register is cleared when the over-temperature condition is not given any longer. Since there is no hysteresis register for this measurement threshold, three consecutive measurements need to be in the normal range to clear the over/under temp status.

Charging is only allowed between the HOT and COLD thresholds.

Each of the battery temperature thermistors BAT0 and BAT1 has its own alert event register EBATxALRT that flag an interrupt when the according temperature threshold BATxALRT-missing in Intel requirement spec is exceeded. In case temperature exceeds one of the thresholds, the status register SBATxALRT and the event register EBATxALRT are set and an Interrupt is generated to the SOC. A hysteresis is implemented for this event, so the status is cleared and another event is generated when the temperature falls below the BATxALRT + BATxHYS threshold.

Note, high temperature means low ADC result values.

15.3.9 CH5-7: System Temperature Thermistor

Each of the system temperature thermistors SYS0, SYS1 and SYS2 has its own alert event register ESYSxALRT that flag an interrupt when the according temperature threshold SYSxALRT is exceeded. In case temperature exceeds one of the thresholds, the status register SSYSxALRT and the event register ESYSxALRT are set and an Interrupt is generated to the SOC. A hysteresis is implemented for this event, so the status is cleared and another event is generated when the temperature falls below the SYSxALRT + SYSxHYS threshold.

Note, high temperature means low ADC result values.

15.3.10 CH8-12: VR Current Measurement

DA6021 is capable to monitor the output current of the VCC, VNN, V1P0A, V1P05S and VDDQ buck regulator. The results are stored in the corresponding result registers.

Usually the current of the buck regulators is monitored when the system is in S0 state. The current is averaged and measured per default every 1ms. The control register described below provides flexibility for user enable/disable and program the average time constant.

Register Name		**VRIMONCTL**		Address		**0x71 Page 1**	Read
				Reset Value		0x03	
MSB							LSB
R	R	R	R	R	R	R	R
reserved			VRIFRQS		VRIFRQA		VRIEN
VRIEN		0 **1**		 Enable ADC based current monitor timer			
VRIFRQA		 00 **01** 10 11		Specifies the time constant at which the current measurements are initiated while system is in S0 mode 0.5ms 1ms 2ms 4ms			
VRIFRQS		 **00** 01 10 11		Specifies the time constant at which system temperature measurements are initiated while system is in S0iX mode Disable 1ms 4ms 8ms			

15.3.11 CH8: VSYS Voltage Measurements

The System Voltage measure requires the preamplifier to be turned on with a gain of 0.8

System Voltages is internally measured every 128us in active states S0.

15.4 ADC Registers

Register Name	SYS0_THRM_RSLTH		Address	0x74 Page 1	Read		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R	R	R
Reserved						SYS0TEMP	
SYS0TEMP[9:8]	**0**..3	Upper bits of system0 thermistor temperature result					

Register Name	SYS0_THRM_RSLTL		Address	0x75 Page 1	Read		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R	R	R
SYS0TEMP							
SYS0TEMP[7:0]	**0**..255	Lower bits of system0 thermistor temperature result					

Register Name	SYS1_THRM_RSLTH		Address	0x76 Page 1	Read		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R	R/W	R/W
Reserved						SYS1TEMP	
SYS1TEMP[9:8]	**0**..3	Upper bits of temperature alert threshold for SYS1TEMP					

Register Name	SYS1_THRM_RSLTL		Address	0x77 Page 1	Read		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R	R	R
SYS1TEMP							
SYS1TEMP[7:0]	**0**..255	Lower bits of temperature alert threshold for SYS1TEMP					

Register Name	SYS2_THRM_RSLTH		Address	0x78 Page 1	Read		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R	R	R
Reserved						SYS2TEMP	
SYS2TEMP[9:8]	**0**..3	Upper bits of temperature alert threshold for SYS2TEMP					

Register Name	SYS2_THRM_RSLTL		Address	0x79 Page 1	Read		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R	R	R
SYS2TEMP							
SYS2TEMP[7:0]	**0**..255	Lower bits of temperature alert threshold for SYS2TEMP					

Register Name	BAT0_THRM_RSLTH		Address	0x7A Page 1	Read		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R	R	R
Reserved						BAT0TEMP	
BAT0TEMP[9:8]	**0**..3	Upper bits of temperature alert threshold for BAT0TEMP					

Register Name	BAT0_THRM_RSLTL		Address	0x7B Page 1	Read		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R	R	R
BAT0TEMP							
BAT0TEMP[7:0]	**0**..255	Lower bits of temperature alert threshold for BAT0TEMP					

Register Name	BAT1_THRM_RSLTH		Address	0x7C Page 1	Read		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R	R	R
Reserved						BAT1TEMP	
BAT1TEMP[9:8]	**0**..3	Upper bits of temperature alert threshold for BAT1TEMP					

Register Name	BAT1_THRM_RSLTL		Address	0x7D Page 1	Read		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R	R	R
BAT1TEMP							
BAT1TEMP[7:0]	**0**..255	Lower bits of temperature alert threshold for BAT1TEMP					

Register Name	PMIC_THRM_RSLTH		Address	0x7E Page 1	Read		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R	R	R
Reserved						PMICTEMP	
PMICTEMP[9:8]	**0**..3	Upper bits of temperature alert threshold for PMICTEMP					

Register Name	PMIC_THRM_RSLTL		Address	0x7F Page 1	Read		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R	R	R
PMICTEMP							
PMICTEMP[7:0]	**0**..255	Lower bits of temperature alert threshold for PMICTEMP					

Register Name	VBATRSLTH		Address	0x80 Page 1	Read		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R	R	R
Reserved						VBAT	
VBAT[9:8]	**0**..3	Upper bits of the battery voltage					

Register Name	VBATRSLTL		Address	0x81 Page 1	Read		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R	R	R
VBAT							
VBAT[7:0]	**0**..255	Lower bits of the battery voltage					

Register Name	BATIDRSLTH		Address	0x82 Page 1	Read		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R	R	R
Reserved						BATID	
BATID[9:8]	**0**..3	Upper bits of the battery ID voltage measurement					

Register Name	BATIDRSLTL		Address	0x83 Page 1	Read		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R	R	R
BATID							
BATID[7:0]	**0**..255	Lower bits of the battery ID voltage measurement					

Register Name	IVCCRSLTH		Address	0x84 Page 1	Read		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R	R	R
Reserved						IVCC	
IVCC[9:8]	**0**..3	Upper bits of VCC current measurement					

Register Name	IVCCRSLTL		Address	0x85 Page 1	Read		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R	R	R
IVCC							
IVCC[7:0]	**0**..255	Lower bits of VCC current measurement					

Register Name	IVNNRSLTH		Address	0x86 Page 1	Read		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R	R	R
Reserved						IVNN	
IVNN[9:8]		**0**..3	Upper bits of VNN current measurement				

Register Name	IVNNRSLTL		Address	0x87 Page 1	Read		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R	R	R
IVNN							
IVNN[7:0]		**0**..255	Lower bits of VNN current measurement				

Register Name	IV1P0ARSLTH		Address	0x88 Page 1	Read		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R	R	R
Reserved						IV1P0A	
IV1P0A[9:8]		**0**..3	Upper bits of V1P0A current measurement				

Register Name	IV1P0ARSLTL		Address	0x89 Page 1	Read		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R	R	R
IV1P0A							
IV1P0A[7:0]		**0**..255	Lower bits of V1P0A current measurement				

Register Name	IV1P05SRSLTH		Address	0x8A Page 1	Read		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R	R	R
Reserved						IV1P05S	
IV1P05S[9:8]		**0**..3	Upper bits of V1P05S current measurement				

Register Name	IV1P05SRSLTL		Address	0x8B Page 1	Read		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R	R	R
IV1P0A							
IV1P05S[7:0]		**0**..255	Lower bits of V1P05S current measurement				

Register Name	IVDDQRSLTH		Address	0x8C Page 1	Read		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R	R	R
Reserved						IVDDQ	
IVDDQ[9:8]	**0**..3	Upper bits of VDDQ current measurement					

Register Name	IVDDQRSLTL		Address	0x8D Page 1	Read		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R	R	R
IVDDQ							
IVDDQ[7:0]	**0**..255	Lower bits of VDDQ current measurement					

16. System Voltage & Temperature Monitoring

16.1 Overview

The system voltage and temperature monitoring allows high power, high temperature events as well as the system voltage monitoring. These functions allow several system conditions to be monitored by DA6021, taking autonomous action and informing the SoC on system voltage and temperature events.

The SVTM will monitor the following:

- **System voltage input VSYS**: in SOC_S0 via the ADC channel 8
- **DA6021 onDie temperature**: this is done via comparator in real time and via ADC channel 2
- **Battery temperature**: 2 ADC channels (channel 3 & 4)
- **Platform temperature**: 3 ADC channels (channel 5, 6 & 7)
- **Under Voltage**: A comparator flags such a condition.
- **Over Voltage**: A comparator will flag such a condition

In reaction to either threshold crosses or a flag coming from several comparators the SVTM will drive several pins on DA6021 for use by the processor and to other platform components. According to the condition it can generate warnings, and or interrupts and can generate a shutdown event.

Register Name		TS_ENABLE		Address	0x90 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R/W	R/W	R/W	R/W	R/W	R/W
reserved		PMICEN	BAT1EN	BAT0EN	SYS2EN	SYS1EN	SYS0EN
SYS0EN		**0** 1	Platform sensor 0 disable Enable				
SYS1EN		**0** 1	Platform sensor 1 disable Enable				
SYS2EN		**0** 1	Platform sensor 2 disable Enable				
BAT0EN		**0** 1	Battery sensor 0 disable Enable				
BAT1EN		**0** 1	Battery sensor 1 disable Enable				
PMICEN		**0** 1	PMIC sensor 0 disable Enable				

Register Name		TS_CRIT_ENABLE		Address	0x91 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R/W	R/W	R/W	R/W	R/W	R/W
reserved		PMICEN	BAT1EN	BAT0EN	SYS2EN	SYS1EN	SYS0EN
SYS0EN		**0** 1	Platform sensor 0 disable Enable				
SYS1EN		**0** 1	Platform sensor 1 disable Enable				
SYS2EN		**0** 1	Platform sensor 2 disable Enable				

BAT0EN	**0** 1	Battery sensor 0 disable Enable
BAT1EN	**0** 1	Battery sensor 1 disable Enable
PMICEN	**0** 1	PMIC sensor 0 disable Enable

Register Name		TS_A0_STATUS		Address	0x92 Page 1	Read	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R	R
reserved		PMIC_ A0_ST	BAT1_ A0_ST	BAT0_ A0_ST	SYS2_ A0_ST	SYS1_ A0_ST	SYS0_ A0_ST
SYS0_A0_ST		**0** 1	 Alert0 thermal status passed platform thermistor 0				
SYS1_A0_ST		**0** 1	 Alert0 thermal status passed platform thermistor 1				
SYS2_A0_ST		**0** 1	 Alert0 thermal status passed platform thermistor 1				
BAT0_A0_ST		**0** 1	 Alert0 thermal status passed battery thermistor0				
BAT1_A0_ST		**0** 1	 Alert0 thermal status passed battery thermistor1				
PMIC_A0_ST		**0** 1	 Alert0 thermal status passed PMIC thermistor				

Register Name		TS_A1_STATUS		Address	0x93 Page 1	Read	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R	R
reserved		PMIC_ A1_ST	BAT1_ A1_ST	BAT0_ A1_ST	SYS2_ A1_ST	SYS1_ A1_ST	SYS0_ A1_ST
SYS0_A1_ST		**0** 1	 Alert1 thermal status passed platform thermistor 0				
SYS1_A1_ST		**0** 1	 Alert1 thermal status passed platform thermistor 1				
SYS2_A1_ST		**0** 1	 Alert1 thermal status passed platform thermistor 1				
BAT0_A1_ST		**0** 1	 Alert1 thermal status passed battery thermistor0				
BAT1_A1_ST		**0** 1	 Alert1 thermal status passed battery thermistor1				
PMIC_A1_ST		**0** 1	 Alert1 thermal status passed PMIC thermistor				

Register Name	TS_CRIT_ST			Address	0xBD Page 1	Read	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R	R
reserved		PMICST	BAT1ST	BAT0ST	SYS2ST	SYS1ST	SYS0ST
SYS0ST		**0** 1	 Critical thermal status passed platform thermistor 0				
SYS1ST		**0** 1	 Critical thermal status passed platform thermistor 1				
SYS2ST		**0** 1	 Critical thermal status passed platform thermistor 2				
BAT0ST		**0** 1	 Critical thermal status passed battery thermistor 0				
BAT1ST		**0** 1	 Critical thermal status passed battery thermistor 1				
PMICST		**0** 1	 Critical thermal status passed PMIC thermistor				

Register Name	THERMIRQ0			Address	0x04 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PMIC ALRT1	SYS2 ALRT1	SYS1 ALRT1	SYS0 ALRT1	PMIC ALRT0	SYS2 ALRT0	SYS1 ALRT0	SYS0 ALERT0
SYS0ALRT0		**0** 1	Set by thermal state machine when system thermistor 0 thermal alert 0 occurs				
SYS1ALRT0		**0** 1	Set by thermal state machine when system thermistor 1 thermal alert 0 occurs				
SYS3ALRT0		**0** 1	Set by thermal state machine when system thermistor 2 thermal alert 0 occurs				
PMICALRT0		**0** 1	Set by thermal state machine when PMIC thermal alert 0 occurs				
SYS0ALRT1		**0** 1	Set by thermal state machine when system thermistor 0 thermal alert 1 occurs				
SYS1ALRT1		**0** 1	Set by thermal state machine when system thermistor 1 thermal alert 1 occurs				
SYS3ALRT1		**0** 1	Set by thermal state machine when system thermistor 2 thermal alert 1 occurs				
PMICALRT1		**0** 1	Set by thermal state machine when PMIC thermal alert 1 occurs				

Register Name	THERMIRQ1			Address	0x05 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
reserved				PMIC CRIT	SYS2 CRIT	SYS1 CRIT	SYS0 CRIT
SYS0CRIT		**0** 1	Set by thermal state machine when system thermistor 0 thermal critical event occurs				

SYS1CRIT	**0** 1	Set by thermal state machine when system thermistor 1 thermal critical event occurs
SYS3CRIT	**0** 1	Set by thermal state machine when system thermistor 2 thermal critical event occurs
PMICCRIT	**0** 1	Set by thermal state machine when PMIC thermal critical event occurs

Register Name		**THERMIRQ2**		Address	**0x06 Page 1**	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
reserved		BAT1 CRIT	BAT0 CRIT	BAT1 ALRT1	BAT0 ALRT1	BAT1 ALRT0	BAT0 ALERT0

BAT0ALRT0	**0** 1	Set by thermal state machine when battery thermistor 0 thermal alert 0 occurs
BAT1ALRT0	**0** 1	Set by thermal state machine when battery thermistor 1 thermal alert 0 occurs
BAT0ALRT1	**0** 1	Set by thermal state machine when battery thermistor 0 thermal alert 1 occurs
BAT1ALRT1	**0** 1	Set by thermal state machine when battery thermistor 1 thermal alert 1 occurs
BAT0CRIT	**0** 1	Set by thermal state machine when a battery critical temperature event occurs. This bit indicates that BATTEMP0) has crossed the value specified in the TCRIT.
BAT1CRIT	**0** 1	Set by thermal state machine when a battery critical temperature event occurs. This bit indicates that BATTEMP1) has crossed the value specified in the TCRIT.

Register Name		**MTHERMIRQ0**		Address	**0x11 Page 1**	Read/Write	
				Reset Value	0xFF		
MSB							LSB
R	R	R/W	R/W	R/W	R/W	R/W	R/W
MPMIC ALRT1	MSYS2 ALRT1	MSYS1 ALRT1	MSYS0 ALRT1	MPMIC ALRT0	MSYS2 ALRT0	MSYS1 ALRT0	MSYS0 ALERT0

MSYS0ALRT0	0 **1**	No mask Interrupt masked
MSYS1ALRT0	0 **1**	No mask Interrupt masked
MSYS2ALRT0	0 **1**	No mask Interrupt masked
MPMICALRT0	0 **1**	No mask Interrupt masked
MSYS0ALRT1	0 **1**	No mask Interrupt masked
MSYS1ALRT1	0 **1**	No mask Interrupt masked
MSYS2ALRT1	0 **1**	No mask Interrupt masked
MPMICALRT1	0 **1**	No mask Interrupt masked

Register Name	MTHERMIRQ1		Address	0x12 Page 1	Read/Write		
			Reset Value	0x0F			
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
reserved				MPMIC CRIT	MSYS2 CRIT	MSYS1 CRIT	MSYS0 CRIT
MSYS0CRIT	0 **1**	No mask Interrupt masked					
MSYS1CRIT	0 **1**	No mask Interrupt masked					
MSYS2CRIT	0 **1**	No mask Interrupt masked					
MPMICCRIT	0 **1**	No mask Interrupt masked					

Register Name	MTHERMIRQ2		Address	0x13 Page 1	Read/Write		
			Reset Value	0x3F			
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
reserved		MBAT1 CRIT	MBAT0 CRIT	MBAT1 ALRT1	MBAT0 ALRT1	MBAT1 ALRT0	MBAT0 ALERT0
BAT0ALRT0	0 **1**	No mask Interrupt masked					
BAT1ALRT0	0 **1**	No mask Interrupt masked					
BAT0ALRT1	0 **1**	No mask Interrupt masked					
BAT1ALRT1	0 **1**	No mask Interrupt masked					
BAT0CRIT	0 **1**	No mask Interrupt masked					
BAT1CRIT	0 **1**	No mask Interrupt masked					

16.2 SVTM Block Diagram

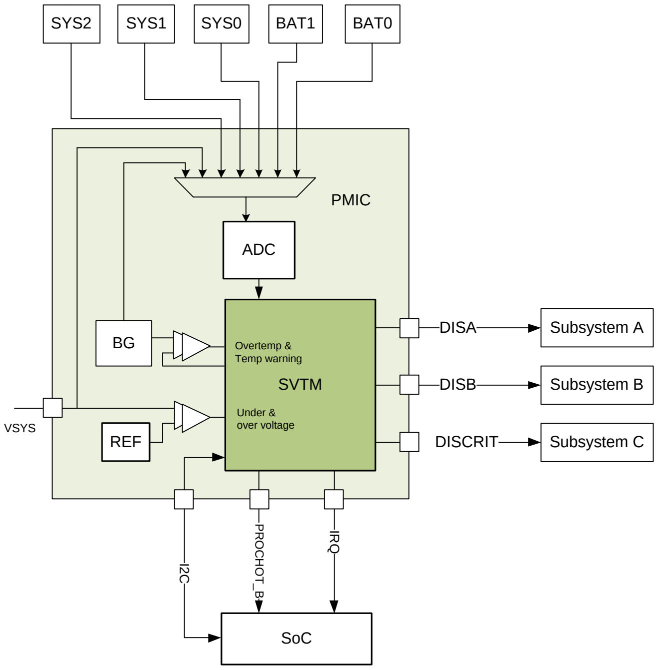


Figure 66: SVTM Block Diagram

Each specific implementation will connect the SVTM output as they deem appropriate except the PROCHOT_B and IRQ which must be connected to the SoC.

16.3 Functional Description

The SVTM will react on voltage comparators placed on the VSYS node and comparators related to the bandgap module (this is related to temperature thresholds). In addition it will react to the measurements results from the ADC according to the programmed values.

16.3.1 VSYS Input Trip Points for ADC Measurement

There are three configurable independent VSYS trip points:

- **VWARNA**: Warning zone A trip point. Will assert the DISA signal and interrupts the SoC when the level crosses below and above the trip point for longer than the programmed value.
- **VWARNB**: Warning zone B trip point. Will assert the DISB signal and interrupts the SoC when the level crosses below and above the trip point for longer than the programmed value.
- **VCRIT**: Warning zone CRITICAL trip point. Will assert the DISCRIT signal and interrupts the SoC when the level crosses below and above the trip point for longer than the programmed value.

All the settings can be programmed via the configuration registers. It is assumed that these thresholds are programmed as VWARNA > VWARNB > VCRIT.

VSYS monitoring will only be executed while being in SoC_S0 state.

Register Name		VWARNA_CFG		Address	0xB4 page 1	Read/Write	
				Reset Value	0x04		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
VWARNA_DEB[3:0]				VWARNA_EN	VWARNA[2:0]		

VWARNA[2:0]	000 001 010 011 **100** 101 110 111	3.3V 3.2V 3.1V 3.0V 2.9V 2.8V 2.7V 2.6V
VWARNA_EN	**0** 1	VWARNA logic disable VWARNA logic enable
VWARNA_DEB[3:0]	**0000** 0001 0010 0011 0100 0101 0110 0111 1000 … 1111	2 fast clock cycles 3 fast clock cycles 4 fast clock cycles 5 fast clock cycles 6 fast clock cycles 7 fast clock cycles 10 fast clock cycles 20 fast clock cycles 30 fast clock cycles … 100 fast clock cycles

Register Name		VWARNB_CFG		Address	0xB5 page 1	Read/Write	
				Reset Value	0x04		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
VWARNB_DEB[3:0]				VWARNB_EN	VWARNB[2:0]		

VWARNB[2:0]	000 001 010 011 **100** 101 110 111	3.3V 3.2V 3.1V 3.0V 2.9V 2.8V 2.7V 2.6V
VWARNB_EN	**0** 1	VWARNB logic disable VWARNB logic enable
VWARNB_DEB[3:0]	**0000** 0001 0010 0011 0100 0101 0110 0111 1000 … 1111	2 fast clock cycles 3 fast clock cycles 4 fast clock cycles 5 fast clock cycles 6 fast clock cycles 7 fast clock cycles 10 fast clock cycles 20 fast clock cycles 30 fast clock cycles … 100 fast clock cycles

Register Name	VCRIT_CFG	Address	0xB6 page 1	Read/Write			
		Reset Value	0x06				
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
VCRIT_DEB[2:0]			VCRITSDWNEN	VCRIT_EN	VCRIT[2:0]		

VCRIT[2:0]	000 001 010 011 100 101 **110** 111	3.3V 3.2V 3.1V 3.0V 2.9V 2.8V 2.7V 2.6V
VCRIT_EN	**0** 1	VCRIT logic disable VCRIT logic enable
VCRITSDWNEN	 **0** 1	DA6021 shuts down when VSYS is below threshold in VCRIT[2:0] Disable enable
VCRIT_DEB[2:0]	**000** 001 010 011 100 101 110 111	2 fast clock cycles 3 fast clock cycles 4 fast clock cycles 5 fast clock cycles 6 fast clock cycles 7 fast clock cycles 10 fast clock cycles 20 fast clock cycles

16.3.2 VSYS Related Output Control

The DA6021 outputs DISA, DISB, DISCRIT are directly derived from the current platform status and the register settings.

The PROCCHOT_B signal is derived from a several input criterias as DA6021 on-die, battery and system temperature as well as battery voltage drop. In order to make decision, the corresponding result registers on the ADC side will be accessible (in static way) for reading from the SVTM.

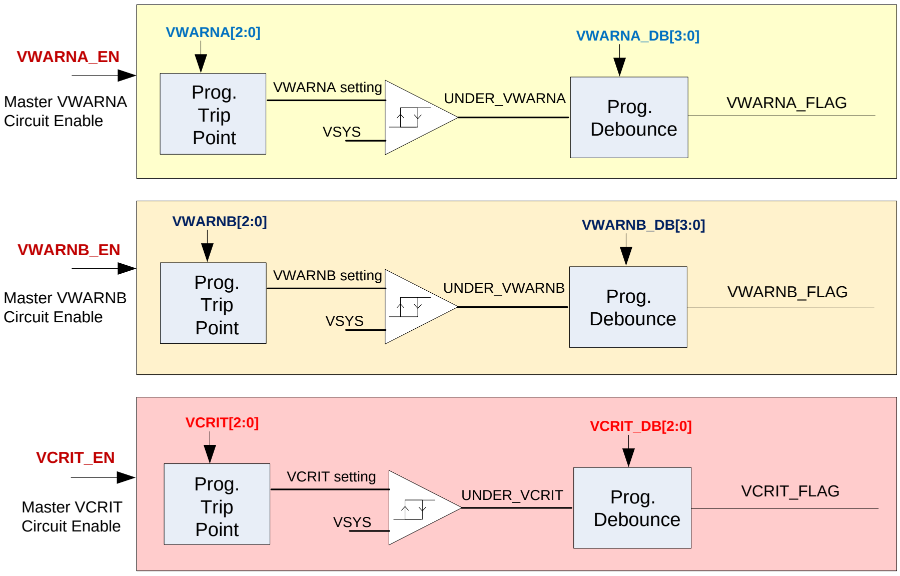


Figure 67: BCU Warning Flag Generation

There is a possibility to disable and change the polarity of a certain output via BEH register setting. In addition it is possible to have a sticky output so under certain conditions an output is asserted, the output value is maintained even when the condition is not valid.. The sticky function is selected with the ST bit and is cleared with the CL bit. The CL bit must be a self-clearing bit.

Register Name		**BCUIRQ**		Address	**0x07 Page 1**	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R/W	R/W	R/W
reserved					VCRIT	VWARNB	VWARNB
VWARNB		**0** 1	No interrupt pending Interrupt pending				
VWARNA		**0** 1	No interrupt pending Interrupt pending				
VCRIT		**0** 1	No interrupt pending Interrupt pending				

Register Name		**MBCUIRQ**		Address	**0x14 Page 1**	Read/Write	
				Reset Value	0x07		
MSB							LSB
R	R	R	R	R	R/W	R/W	R/W
reserved					MVCRIT	MVWARNB	MVWARNB
MVWARNB		0 **1**	Interrupt not masked Interrupt masked				
MVWARNA		0 **1**	Interrupt not masked Interrupt masked				
MVCRIT		0 **1**	Interrupt not masked Interrupt masked				

Register Name		DISA_BEH		Address	0xB7 Page1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R/W	R/W	R/W
reserved					DISA_ STICKY	DISA_POL	DISA_EN
DISA_EN		0 1	BCU DISA signal disable BCU DISA function signal enable				
DISA_POL		0 1	BCU DISA pin active low BCU DISA pin active high				
DISA_STICKY		0 1	0 = signal assertion not sticky 1= signal assertion is sticky				

Register Name		DISB_BEH		Address	0xB8 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R/W	R/W	R/W
reserved					DISB_ STICKY	DISB_POL	DISB_EN
DISB_EN		0 1	BCU DISB signal disable BCU DISB function signal enable				
DISB_POL		0 1	BCU DISB pin active low BCU DISB pin active high				
DISB_STICKY		0 1	0 = signal assertion not sticky 1= signal assertion is sticky				

Register Name		DISCRIT_BEH		Address	0xB9 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R/W	R/W	R/W
reserved					DISCRIT_ STICKY	DISCRIT _POL	DISCRIT _EN
DISCRIT_EN		0 1	BCU DISCRIT signal disable BCU DISCRIT function signal enable				
DISCRIT_POL		0 1	BCU DISCRIT pin active low BCU DISCRIT pin active high				
DISCRIT_STICKY		0 1	0 = signal assertion not sticky 1= signal assertion is sticky				

Register Name	BCU_TRIP_ST			Address	0xBB Page 1	Read	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R	R
reserved					SVSCRIT	SVWARNA	SVWARNB
SVWARNB		**0** 1	VSYS above VWARNB trip point VSYS below VWARNB trip point				
SVWARNA		**0** 1	VSYS above VWARNA trip point VSYS below VWARNA trip point				
SVCRIT		**0** 1	VSYS above VCRIT trip point VSYS below VCRIT trip point				

Register Name	BCUOUT_ST			Address	0xBC Page 1	Read	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R	R
reserved				SDISA	SDISB	SDISCRIT	SPROTHOT_B
SPROTHOT_B		**0** 1	PROTHOT_B not asserted PROTHOT_B asserted				
DISCRIT		**0** 1	DISCRIT not asserted DISCRIT asserted				
SDISB		**0** 1	DISB not asserted DISB asserted				
SDISA		**0** 1	DISA not asserted DISA asserted				

16.3.2.1 VSYS Waveform Example

Below is an explanation of the BCU VSYS trip points and how the voltage may behave under a given situation. A table describes a select subset of the numbered events to describe expected BCU behavior.

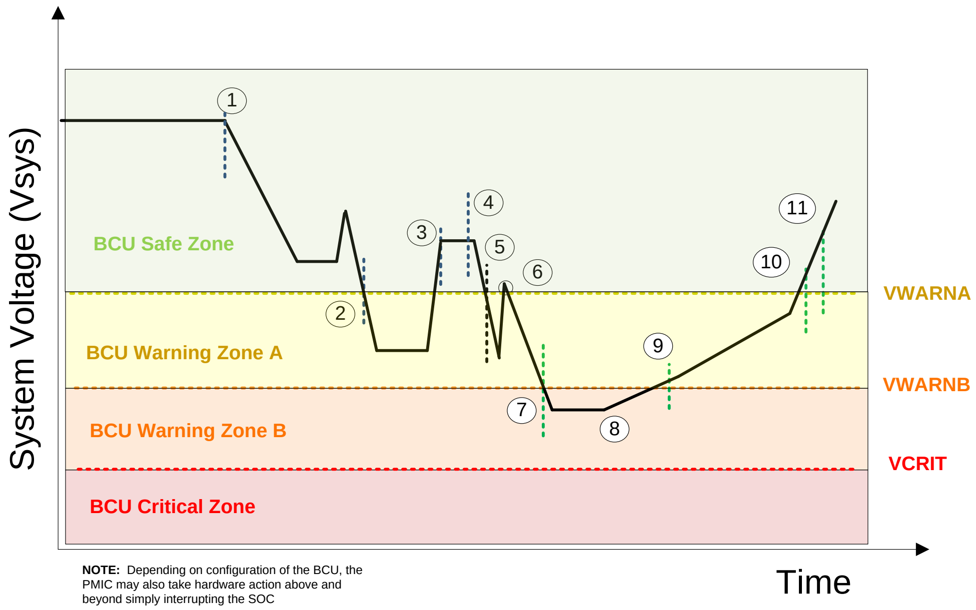


Figure 68: VSYS Trip Points Flag Logic

#	System Event	BCU Response		SOC Response
		Interrupts	Hardware Actions	
1	Large system burst event begins, dropping VSYS	N/A	N/A	N/A
2	VSYS goes below VWARNA BCU threshold and into Warning Zone A	After the de-bounce period for VWARNA, the BCU interrupts SOC with BCUIRQ and VWARNAIRQ bits...	Assert BCUDISA and/or PROCHOT_B (if enabled as such)	Gets interrupt and knows what hardware actions (if any) have been done. Clears BCUIRQ and VWARNA interrupt bits.
3	VSYS goes back above VWARNA threshold due to BCU response	After the de-bounce period for VWARNA, the BCU interrupts SOC with BCUIRQ and VWARNAIRQ bits...	De-assert BCUDISA and/or PROCHOT_B (if not sticky)	Gets interrupt and knows system is out of warning Zone A. If pin assertion is sticky, will clear BCUDISA and/or PROCHOT_B assertion.
4	A further large system burst event begins, dropping VSYS	N/A	N/A	N/A
7	VSYS goes below VWARNB BCU threshold and into Warning Zone B	After the de-bounce period for VWARNB, the BCU interrupts SOC with BCUIRQ and VWARNBIRQ bits...	Asserts BCUDISB and/or PROCHOT_B (if enabled as such)	Gets interrupt and knows what hardware actions (if any) have been done. Clears BCUIRQ and VWARNB interrupt bits.

9	VSYS goes back above VWARNB threshold due to BCU response. Still in Warning Zone A.	After the de-bounce period for VWARNB, the BCU interrupts SOC with BCUIRQ and VWARNBIRQ bits...	De-assert BCUDISB and/or PROCHOT_B (if not sticky). VWARNA and/or PROCHOT_B may stay asserted since still in Warning Zone A.	Gets interrupt and knows system is out of warning Zone A. If pin assertion is sticky, will clear BCUDISB and/or PROCHOT_B assertion.

Table 102: VSYS Event Table

16.3.3 Under- & Over- Voltage Condition

Two comparator inputs monitor whether VSYS is between 2 predefined thresholds under-voltage (2.7V) and the over-voltage (5.5V±100mV).

Both comparators will have built-in hysteresis and in both cases the system will perform an immediate shutdown without processor control. This protects the system from damage due to over-voltage or in the under-voltage condition ensures the system does not become unstable because on the DA6021 has insufficient power.. Refer to the introduction section for an overview of the catastrophic events.

In the case of the over-voltage flag the system will go to the SOC_G3 state and wait there until the overvoltage input flag is removed. Then the system is able to wake up again.

In the case of the under-voltage condition the VSYS is too low being considered valid and the analog circuitry cannot work properly. DA6021 will initiate a system shut down regardless of the SoC state and will end up in G3 state. It will stay here until the VSYS becomes valid again (VSY is valid, from input source detection logic). If the voltage on VSYS drops again, it will reach the POR level and DA6021 will go into the RESET state (under POR) There will be no IRQ sent to DA6021 due to over or under-voltage condition. Both under- and over-voltage conditions are de-bounced with a 100µs filter.

16.3.4 Permanent Temperature Monitoring

The bandgap on DA6021 also implements an over temperature detection. Two temperature ranges are supervised:

- A pre-alarm is issued at about 110°C.
- An over-temperature system-shutdown is issued at about 140°C.

If a pre-alarm is detected for a time frame > 100µs (de-bounce time), the PROCHOT_B output gets asserted. If the pre-alarm is de-asserted for at least 500µs (de-bounce time) PROCHOT_B gets de-asserted. This guarantees a 500us minimum assertion time of PROCHOT_B.

If asserting PROCHOT_B (the external processor should start throttling which in turn should lead to a decrease of the temperature due to less power consumption) does not lower the temperature and the temperature reaches the 140°C limit for at least 100us circa (de-bounce time), DA6021 performers an immediate shutdown (it goes into SOC_G3 state).

Register Name	PROCHOT_BEH		Address	0xBA Page 1		Read/Write	
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R/W	R/W	R/W
reserved					PROCHOT_B_ST	PROCHOT_B_VWA_EN	PROCHOT_B_VWB_EN
PROCHOT_B_VWB_EN	**0** 1	BCU will not enable PROCHOT_B based on VWARNB Assert PROCHOT_B at VWARNB					
PROCHOT_B_VWA_EN	**0** 1	BCU will not enable PROCHOT_B based on VWARNB Assert PROCHOT_B at VWARNB					
PROCHOT_B_ST	**0** 1	0 = low status indication 1= high status indication					

16.3.5 Temperature Monitoring via ADC

DA6021 has the capability to monitor six miscellaneous temperatures and stores the measurement results in the corresponding registers

- SYSTHERM0: System temperature 0
- SYSTHERM1: System temperature 1
- SYSTHERM2: System temperature 2
- PMICTEMP: DA6021 on-die temperature
- BPTHERM0: Primary battery temperature
- BPTHERM1: Secondary battery temperature

The external temperatures are sensed using external precision NTC thermistors. PMICTEMP, the internal die temperature, is sensed using an internal silicon temperature thermometer circuit. All six temperatures are sampled by the 10-bit GPADC (ADC). Voltages across the thermistors are converted by the ADC channels. That means a higher temperature at a thermistor will give a lower voltage at the input of ADC channel thus produces a smaller digital code at the ADC result registers. The SVTM will read always the measurement result for the system, platform and PMIC temperature and will react according to some programmable thresholds.

The THRMMONCTL0-1 registers are the master control for the timer-based thermal monitoring state machine. They are defined in the table below.

Register Name	THRMMONCTL0		Address	0x8E Page 1		Read/Write	
			Reset Value	0x15			
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
reserved	SYSFRQS	BATFRQS	SYSFRQA		BATFRQA		THRMEN
THRMEN	0 **1**	DA6021 shuts down if die temperature exceeds critical limit Enables ADC based automatic thermal monitoring timer for system, battery and DA6021 die					
BATFRQA[1:0]	 00 01 **10** 11	Specifies the frequency at which battery temperature measurements are initiated while system is in S0 mode Disable 1s 4s 32s					

SYSFRQA[1:0]	 00 01 **10** 11	Specifies the frequency at which system temperature measurements are initiated while system is in S0 mode Disable 1s 4s 32s
BATFRQS	 **0** 1	Specifies the frequency at which battery temperature measurements are initiated while system is in S0iX mode disable 32s
SYSFRQS	 **0** 1	Specifies the frequency at which system temperature measurements are initiated while system is in S0iX mode disable 32s

Register Name		**THRMMONCTL1**		Address	**0x8F Page 1**	Read/Write	
				Reset Value	0x02		
MSB							LSB
R	R	R	R	R	R/W	R/W	R/W
reserved					PMICFRQS	PMICFRA	

PMICFRQA[1:0]	 00 01 **10** 11	Specifies the frequency at which PMIC die temperature measurements are initiated while system is in S0 mode Disable 1s 4s 32s
PMICFRQS	 **0** 1	Specifies the frequency at which PMIC die temperature measurements are initiated while system is in S0iX mode disable 32s

The thermal monitoring is active only in state SOC_SX and SOC_S0.

Temperature monitoring of each thermistor may be enabled or disabled (register TS_ENABLE) depending on whether the thermistor and its bias circuit is populated on the platform. This enables the thermal monitoring state machine to know if any alert or interrupt associated with the thermistor should be generated. If in register TS_ENABLE the corresponding enable bit is set, the thermistor is connected to the PMIC and the PMIC can poll the sensor.

There are three pre-defined and programmable threshold for each of the measurements

- ALERT0
- ALERT1
- TCRIT

Each ALERT has a 4-bit hysteresis and 4 STATUS bits (A0_ST, A1_ST, CRIT_ST) and for all the ALERT0 a policy register (A0P_EN) is defined in order to allow actions upon crossing thresholds.

Register Name	SYS0_THRMALRT0H			Address	0x94 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
A0PEN	A0EN	ALERT0_HYST				ALERT0MSB	
ALERT0MSB[1:0]		**00**..11	Alert0 threshold MSBs				
ALERT0_HYST[0:3]		**0000** 0001 … 1110 1111	SYSTEMP0 must be above ALERT0 + ALERT0_HYS to clear a thermal event				
A0EN		**0** 1	Disable Enable				
A0PEN		**0** 1	Policy action disable Policy action enable				

Register Name	SYS0_THRMALRT0L			Address	0x95 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ALERT0LSB							
ALERT0LSB [7:0]		**0**..255					

Register Name	SYS0_THRMALRT1H			Address	0x96 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
reserved	A1EN	ALERT1_HYST				ALERT1MSB	
ALERT1MSB[1:0]		**00**..11	Alert1 threshold MSBs				
ALERT1_HYST[0:3]		**0000** 0001 … 1110 1111	SYSTEMP0 must be above ALERT1 + ALERT1_HYS to clear a thermal event				
A1EN		**0** 1	Disable Enable				

Register Name	SYS0_THRMALRT1L			Address	0x97 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ALERT1LSB							
ALERT1LSB [7:0]		**0**..255					

Register Name	SYS0THERMCRIT			Address	0x98 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
TCRIT							
TCRIT [8:1]		**0**..255	Note that TCRIT[9] and TCRIT[0] are always 0				

Register Name		SYS1THERMAL0		Address	0x99 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
A0PEN	A0EN	ALERT0_HYST				ALERT0MSB	
ALERT0MSB[1:0]		**00**..11	Alert0 threshold MSBs				
ALERT0_HYST[0:3]		**0000** 0001 … 1110 1111	SYSTEMP0 must be above ALERT0 + ALERT0_HYS to clear a thermal event				
A0EN		**0** 1	Disable Enable				
A0PEN		**0** 1	Policy action disable Policy action enable				

Register Name		SYS1THERMAL1		Address	0x9A Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ALERT0LSB							
ALERT0LSB [7:0]		**0**..255					

Register Name		SYS1THERMAL2		Address	0x9B Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
reserved	A1EN	ALERT1_HYST				ALERT1MSB	
ALERT1MSB[1:0]		**00**..11	Alert1 threshold MSBs				
ALERT1_HYST[0:3]		**0000** 0001 … 1110 1111	SYSTEMP0 must be above ALERT1 + ALERT1_HYS to clear a thermal event				
A1EN		**0** 1	Disable Enable				

Register Name		SYS1THERMAL3		Address	0x9C Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ALERT1LSB							
ALERT1LSB [7:0]		**0**..255					

Register Name		SYS1THERMCRIT		Address	0x9D Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
TCRIT							
TCRIT [8:1]		**0**..255	Note that TCRIT[9] and TCRIT[0] are always 0				

Register Name		SYS2THERMAL0		Address	0x9E Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
A0PEN	A0EN	ALERT0_HYST				ALERT0MSB	
ALERT0MSB[1:0]		**00**..11	Alert0 threshold MSBs				
ALERT0_HYST[0:3]		**0000** 0001 … 1110 1111	SYSTEMP0 must be above ALERT0 + ALERT0_HYS to clear a thermal event				
A0EN		**0** 1	Disable Enable				
A0PEN		**0** 1	Policy action disable Policy action enable				

Register Name		SYS2THERMAL1		Address	0x9F Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ALERT0LSB							
ALERT0LSB [7:0]		**0**..255					

Register Name		SYS2THERMAL2		Address	0xA0 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
reserved	A1EN	ALERT1_HYST				ALERT1MSB	
ALERT1MSB[1:0]		**00**..11	Alert1 threshold MSBs				

ALERT1_HYST[0:3]	**0000** 0001 … 1110 1111	SYSTEMP0 must be above ALERT1 + ALERT1_HYS to clear a thermal event
A1EN	**0** 1	Disable Enable

Register Name		**SYS2THERMAL3**		Address	**0xA1** **Page 1**	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ALERT1LSB							
ALERT1LSB [7:0]		**0**..255					

Register Name		**SYS2THERMCRIT**		Address	**0xA2** **Page 1**	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
TCRIT							
TCRIT [8:1]		**0**..255	Note that TCRIT[9] and TCRIT[0] are always 0				

Register Name		**BAT0THERMAL0**		Address	**0xA3** **Page 1**	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
A0PEN	A0EN	ALERT0_HYST				ALERT0MSB	
ALERT0MSB[1:0]		**00**..11	Alert0 threshold MSBs				
ALERT0_HYST[0:3]		**0000** 0001 … 1110 1111	SYSTEMP0 must be above ALERT0 + ALERT0_HYS to clear a thermal event				
A0EN		**0** 1	Disable Enable				
A0PEN		**0** 1	Policy action disable Policy action enable				

Register Name		**BAT0THERMAL1**		Address	**0xA4** **Page 1**	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ALERT0LSB							
ALERT0LSB [7:0]		**0**..255					

Register Name	BAT0THERMAL2		Address	0xA5 Page 1	Read/Write		
			Reset Value	0x00			
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
reserved	A1EN	ALERT1_HYST				ALERT1MSB	
ALERT1MSB[1:0]	**00**..11	Alert1 threshold MSBs					
ALERT1_HYST[0:3]	**0000** 0001 … 1110 1111	SYSTEMP0 must be above ALERT1 + ALERT1_HYS to clear a thermal event					
A1EN	**0** 1	Disable Enable					

Register Name	BAT0THERMAL3		Address	0xA6 Page 1	Read/Write		
			Reset Value	0x00			
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ALERT1LSB							
ALERT1LSB [7:0]	**0**..255						

Register Name	BAT0THERMCRITH		Address	0xA7 Page 1	Read/Write		
			Reset Value	0x00			
MSB							LSB
R	R	R	R	R	R	R/W	R/W
TCRIT[8:1]							
TCRIT [8:1]	**0**.255	Value of the critical HIGH temperature threshold, bit8 .. bit1 for temperature measurement channel BPTHERM0					

Register Name	BAT0THERMCRITL		Address	0xA8 Page 1	Read/Write		
			Reset Value	0x00			
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
TCRIT[9:2]							
TCRIT [9:2]	**0**..255	Value of the critical LOW temperature threshold, bit9 .. bit2 fot the temperature measurement channel BPTHERM0					

Register Name	BAT1THERMAL0		Address	0xA9 Page 1	Read/Write		
			Reset Value	0x00			
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
A0PEN	A0EN	ALERT0_HYST				ALERT0MSB	
ALERT0MSB[1:0]	**00**..11	Alert0 threshold MSBs					

ALERT0_HYST[0:3]	**0000** 0001 … 1110 1111	SYSTEMP0 must be above ALERT0 + ALERT0_HYS to clear a thermal event
A0EN	**0** 1	Disable Enable
A0PEN	**0** 1	Policy action disable Policy action enable

Register Name		**BAT1THERMAL1**		Address	**0xAA Page 1**	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ALERT0LSB							
ALERT0LSB [7:0]		**0**.255					

Register Name		**BAT1THERMAL2**		Address	**0xAB Page 1**	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
reserved	A1EN	ALERT1_HYST				ALERT1MSB	
ALERT1MSB[1:0]		**00**..11	Alert1 threshold MSBs				
ALERT1_HYST[0:3]		**0000** 0001 … 1110 1111	SYSTEMP0 must be above ALERT1 + ALERT1_HYS to clear a thermal event				
A1EN		**0** 1	Disable Enable				

Register Name		**BAT1THERMAL3**		Address	**0xAC Page 1**	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ALERT1LSB							
ALERT1LSB [7:0]		**0**..255					

Register Name		**BAT1THERMCRITH**		Address	**0xAD Page 1**	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R/W	R/W
reserved						TCRIT[9:8]	
TCRIT [9:8]		**0**..3	MSBs				

Register Name		BAT1THERCRITL		Address	0xAE Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
TCRIT[7:0]							
TCRIT [7:0]		**0**..255					

Register Name		BAT1THERCRITL		Address	0xAF Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
A0PEN	A0EN	ALERT0_HYST				ALERT0MSB	
ALERT0MSB[1:0]		**00**..11	Alert0 threshold MSBs				
ALERT0_HYST[0:3]		**0000** 0001 … 1110 1111	SYSTEMP0 must be above ALERT0 + ALERT0_HYS to clear a thermal event				
A0EN		**0** 1	Disable Enable				
A0PEN		**0** 1	Policy action disable Policy action enable				

Register Name		PMICTHERMAL1		Address	0xB0 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ALERT0LSB							
ALERT0LSB [7:0]		**0**.255					

Register Name		PMICTHERMAL2		Address	0xB1 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
reserved	A1EN	ALERT1_HYST				ALERT1MSB	
ALERT1MSB[1:0]		**00**..11	Alert1 threshold MSBs				
ALERT1_HYST[0:3]		**0000** 0001 … 1110 1111	SYSTEMP0 must be above ALERT1 + ALERT1_HYS to clear a thermal event				
A1EN		**0** 1	Disable Enable				

Register Name	PMICTHERMAL3			Address	0xB2 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ALERT1LSB							
ALERT1LSB [7:0]		**0**..255					

Register Name	PMICTHERMCRIT			Address	0xB3 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
TCRIT							
TCRIT [8:1]		**0**..255	Note that TCRIT[9] and TCRIT[0] are always 0				

When in register TS_ENABLE the corresponding thermistor bit as well as the corresponding A0PEN bit asserted, any crossover of ALERT0 will assert PROCHOT_B. Any cross down below ALERT0_HYST must remove the related warning and de-assert PROCHOT_B if there are no other warnings.

A0_ST and A1_ST are always set if:

- temp > ALERTX or
- temp < (ALERTX – ALERTX_HYST) with X=0 or 1.

Setting A0_ST or A1_ST will generate an interrupt for the processor

Alert warnings concurrently assert the PROCHOT_B. The processor must investigate this and act to optimize power consumption to control the temperature until the sensed voltage is at the correct level. Assertion should hold until all the warnings are cleared.

16.4 Critical Thermal Events

Unlike alerts, which are pre-emptive warnings, —critical thermal events occur when the system or battery pack(s) or DA6021 die temperature exceed design thresholds, immediate action must be taken to resolve this thermal issue.

16.4.1 System Temperature

The system temperature exceeds the critical thermal limit set for the SYSTEMP0-2, and critical temperature shut down is enabled (CRITEN=1), the following actions are taken:

- If enabled, DA6021 forces the immediate shutdown of all VR rails currently in regulation, returning DA6021 to the SOC G3 state without depending on the assertion of SLP_S*_B signals from the SOC.
- DA6021 sets the RSYSTEMP bit in the RESETSRC0 register to indicate the reason for shutdown.
- DA6021 sets SYS*CRIT in THRMIRQ1 to interrupt the SOC. However, the SOC may not have time to respond before the system is shut down.

The system temperature exceeds the critical thermal limit set for the SYSTEMP0-2, and critical temperature shut down is not enabled (CRIT_EN=0), the following actions are taken:

- DA6021 sets SYS*CRIT in THRMIRQ1 to interrupt the SOC.
- In response to the IRQ, the SOC should check CRIT_ST in SYS*_THRM_RSH to see if the system critical over/under temperature condition still exists
- When the battery critical over/under temperature event resolves (system thermistor voltages are back within defined voltage ranges), the SOC clears the SYS*CRIT interrupt.

16.4.2 Battery Critical Temperature

While the temperature threshold registers define the boundaries between different operating temperature alert levels, the absolute ends of the battery operating temperature are monitored/enforced by two voltage comparators (one per battery thermistor), comparing these voltages against programmable thresholds which, for a particular thermistor curve, specify the minimum and maximum battery temperatures.

These ―critical temperature‖ comparators monitor the same thermistor voltages as the ADC channels for the primary and/or secondary battery. These values (TCRIT_HIGH and TCRIT_LOW) have default values defined.

If the voltage on one or both battery temperature pins falls outside of the TCRIT_HIGH and TCRIT_LOW thresholds, and critical temperature shut down is enabled (CRIT_EN=1), the following actions are taken:

- DA6021 forces the immediate shutdown of all VR rails currently in regulation, returning DA6021 to the SOC G3 state without depending on the assertion of SLP_S*_B signals from the SOC.
- DA6021 sets the RBATTEMP bit in the RESETSRC0 register to indicate the reason for shutdown.
- DA6021 sets BATCRIT in THRMIRQ2 to interrupt the SOC. However, the SOC may not have time to respond before the system is shut down.

If the voltage on one or both battery temperature pins falls outside of the TCRIT_HIGH and TCRIT_LOW thresholds, and critical temperature shut down is not enabled (CRIT_EN=0), the following actions are taken:

- DA6021 sets BAT*CRIT in THRMIRQ to interrupt the SOC.
- In response to the IRQ, the SOC should check CRIT_ST in BAT*_THRM_RSH to see if the battery critical over/under temperature condition still exists
- When the battery critical over/under temperature event resolves (battery thermistor voltages are back within defined voltage ranges), the SOC clears the BAT*CRIT interrupt.

This protection feature is disabled if the battery is detected to be not present (SBATDET). In order to avoid spurious tripping of this condition upon battery removal, a 200ms de-bounce is required. If, in that 200ms window, the battery presence detection logic determines the battery was removed, the thermal event de-bounce counter ends and no action is taken.

16.4.3 DA6021 die Temperature

DA6021 die temperature monitor exceeds the hard-coded critical thermal limit for the device:

- A hardware comparator circuit forces the immediate shutdown of all VR rails currently in regulation, returning DA6021 to the SOC G3 state without depending on the assertion of SLP_S*_B signals from the SOC.
- DA6021 sets the RPMICTEMP bit in the RESETSRC0 register to indicate the reason for shutdown.

However the ADC will also monitor the DA6021 temperature and have similar critical temperature handling procedure to that outlined above for the system and battery critical temperature events.

16.4.4 Thermal Monitoring Event Table

Following is a table which summarizes the behavior of DA6021 in relation to thermal monitoring.

TS_EN	A1_EN	A0_EN	A0P_EN	ALERT1_SET	ALERT0_SET	irqALRT1	irqALRT0	PROCHOT_B
0	x	x	x	x	x	0	0	1
1	0	0	x	0	0	0	0	1
1	0	1	0	0	0	0	0	1
1	0	1	0	0	1	0	1	1
1	0	1	1	0	0	0	0	1
1	0	1	1	0	1	0	1	0 (Asserted)
1	1	0	x	0	0	0	0	1
1	1	0	x	1	0	1	0	1
1	1	1	0	0	0	0	0	1
1	1	1	0	0	1	0	1	1
1	1	1	0	1	0	1	0	1
1	1	1	0	1	1	1	1	1
1	1	1	1	0	0	0	0	1
1	1	1	1	0	1	0	1	0 (Asserted)
1	1	1	1	1	0	1	0	1
1	1	1	1	1	1	1	1	0 (Asserted)

Table 103: Thermal Monitoring Events

Note that PROCHOT_B only gets asserted when temperature crossed over (rose above) the ALERT0 temperature threshold and A0EN=1 and A0PEN=1. It gets de-asserted when temperature crossed down (fell below) the ALERT0 temperature threshold.

16.5 Backup Battery Management

Configuration and status registers of DA6021, and timekeeping logic (powered by a platform voltage rail VRTC) in the SOC are backed-up by a super capacitor or coin cell battery in case of SOC power loss (e.g., main battery changed). The VRTC is supplied usually through a diode by either V3P3A or VBATBKUP with V3P3A taking priority whenever it is available. If a SOC power loss is of an extended duration, the back-up supply will fall below the minimum operational voltage, VMIN, and the content of the registers will be lost and reset to default value.

16.5.1 Backup Battery Charger

The Backup Battery Charger is used to charge coin cell Li-Ion batteries or "Super-capacitors". Due to the chemistry and/or relatively high internal resistance of these batteries it is necessary to charge in two stages: a constant current stage; and a constant voltage stage. In essence this means that the charger acts as a current-limited voltage source. The target voltage and maximum charge current are configurable via separate 2-bit register settings.

In addition to battery charging the circuit must protect against discharging of the backup battery in cases when the system supply drops below the backup battery voltage. For this reason an always-on protection circuit is utilized which shuts off the reverse current path as required.

To facilitate low power system modes wherein no oscillator is running, the Backup Battery Charger is capable of autonomously self-regulating its state such as to stop charging when the battery is full and to start once again when the battery is sufficiently emptied.

Register Name		**BBCHR_CFG**		Address	**0x2A Page 1**	Read/Write	
				Reset Value	0x1F		
MSB							LSB
R	R	R	R/W	R/W	R/W	R/W	R/W
reserved	CHG_DONE_ST	CHG_ST	CHGI		CHGV		CHGEN

Field	Value	Description
CHGEN	0 **1**	Disable charging of back-up battery Enable charging of back-up battery
CHGV	 00 01 10 **11**	Back-up supply charging 2.5V 2.8V 3.0V 3.3V
CHGI	 00 01 10 **11**	Current limit of back-up charger 10µA 50µA 100µA 500µA
CHG_ST	**0** 1	Not charging Charging ongoing
CHG_DONE_ST	**0** 1	Not fully charged Back-up charging completed

16.5.2 Power Consumption

The DA6021 logic supplied by the RTC domain will consume <5µA.

17. General Purpose IOs

17.1 Overview

DA6021 provides 16 GPIO pins for general purpose IOs under the control of the SoC. The majority of these GPIO pins have a default configuration as CMOS inputs with weak (50 KOhm) pull downs enabled. The GPIO buffers support operation as open-drain or push pull outputs. They are split into 2 groups, each with a different fixed supply:

- GPIO0P0 – GPIO0P7 support a level of 1.8V
- GPIO1P0 – GPIO1P7 support 3.3V

Following are the supported feature from the digital GPIO IP:

- CMOS or Open Drain output and input configuration
- 2k-ohm or 50k-ohm pull-up or pull-down resistance
- Read back of output PAD values
- Output Level select by register
- Digital glitch filter of 62µs
- Digital filter (de-bouncer, typically 32ms) with programmable bypass
- Interrupt and interrupt mask functionality.
- Polarity selection (default active high)
- Analog/Digital Input
- Alternate input/output functionality.

Note: for the implementation of the GPIO core functionality is useful to know that the register file will not be part of the IP, same is for the logic which controls the mapping of the alternate functions.

17.2 Analog Block, Control & Data Signals

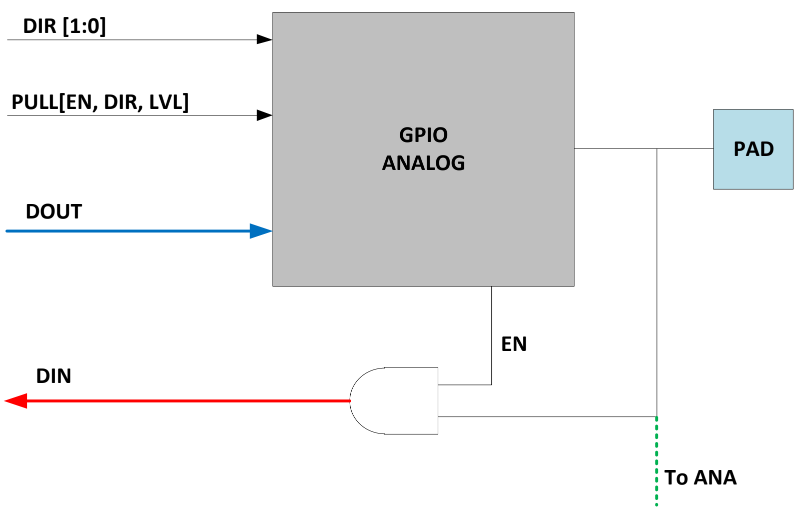


Figure 69 : GPIO Block Diagram

As is shown from the above picture (analog block as black box) there are 5 signals which controls the analog behavior of the GPIO pin. Note that EN is generated from the analog pad block itself.

The following tables show the coding for configuring the GPIO pads.

DIR		GPIO Configuration
0	0	Input Analog
0	1	Input Digital
1	0	Output Open-Drain
1	1	Output CMOS

Table 104: GPIO Direction Configuration

PULL_EN	PULL_DIR	PULL_LVL	GPIO Configuration
0	X	X	No pull-up / pull-down
1	0	0	2-KOhm pull-down
	0	1	50-KOhm pull-down
	1	0	2-KOhm pull-up
	1	1	50-KOhm pull-up

Table 105: GPIO Pull-up/Pull-down Configuration

17.3 GPIO Digital Features

17.3.1 De-Bouncing

When a GPIO is used as a digital input, a 32ms de-bounce circuit can be assigned to the input path. The input signal should be stable for the de-bounce time before the de-bounce circuit flags the output. If GPIOx_DEB is set, de-bouncing is enabled. All pads share the same de-bounce time setting. High and low pulses that are shorter than 32ms +/- 4ms are filtered out. To reduce power consumption, a 3 bit counter running with the 4ms tick is used to generate the de-bounce functionality.

17.3.2 Status Register

The GPIO status is synchronized, de-bounced and can be read back from the GPIOx_CTLI[0] read-only register.

17.3.3 Interrupt Functionality

In addition to the status information, the SOC can configure a GPIO to flag an edge sensitive interrupt on a state change of the GPIO PAD cell. Interrupts can be generated on rising and/or falling edges of GPIO inputs.

DA6021 provides includes an internal interrupt interface collecting all events from various modules to generate the interrupt signal to the SOC. The interrupt options are defined in GPIOx_IRQCFG register.

17.4 Analogue Mode

In case the GPIOx_DIR register is set to 0x0, the PAD is used as analogue PAD and is disconnected from the digital. In this case the input (analogue input) will be feeding some analogue circuitry.

17.5 Alternative Functions

GPIOs also enable the use of alternative functions In order to use these GPIO need to be configured first. This consists of setting the GPIPO as input or output and then, selecting the mapping functionality to select which particular GPIO a certain alternate function should be related.

17.6 Defining an Output Value

A DOUT bit for each GPIO has been defined so it is possible to define the output level of each GPIO. See the register file description for more information regarding the output.

17.7 Supported Alternate Functions

17.7.1 GPIO0P0 – BATIDIN

GPIO0P0 can be configured as a digital battery interface input driven by SOC

17.7.2 GPIO0P1 – BATIDOUT

GPIO0P1 can be used as a digital battery interface output driving the SOC

17.7.3 GPIO0P2 – GPIO0P7-PCSMCNT

GPIO0P7 to GPIO0P2 outputs the PCSM state pointer to allow access of the power on sequence via pins in real-time.

17.7.4 GPIO1P0 – UIBTN_B

GPIO1P0 can be used as HW UI button as an additional interface button.

17.7.5 GPIO1P1 – CLK32OUT

GPIO1P1 can be configured to output a 32k clock derived from the internal oscillator.

17.7.6 GPIO1P2 – TRIG1

GPIO1P2 can be used as a power on control input forcing the PCSM to keep its current state. This gives the SOC the capability to insert additional wait states to the power on sequence. The sequencer can be programmed to wait at a certain point or an external trigger (TRIG1).

17.7.7 GPIO1P3 – TRIG2

GPIO1P3 can be used as power on control input forcing the PCSM to keep its current state. Main purpose is to give the SOC the capability to insert additional wait states to the power on sequence. The sequencer can be programmed to wait at a certain point for an external trigger (TRIG2).

17.7.8 GPIO1P4 – WAKE1

GPIO1P4 can be used as an additional wakeup input forcing the PCSM to switch to S0 state

17.7.9 GPIO1P5 – WAKE2

GPIO1P5 can be used as an additional wakeup input forcing the PCSM to switch to S0 state.

17.8 Electrical Characteristics

Parameter	Min	Nom	Max	Units	Notes	Val
Voltage (VDD)	1.71	1.8	1.89	V	At pin	-
Vil			0.35*VDD	V		A
Vih	0.65*VDD			V		A
Vhys	0.1			V		D,E
Vol			0.45	V	Imax 8mA	A
Voh	VDD-0.45			V	Imax 4mA	A
Trise	10		45	ns		D,E
Tfall	10		45	ns		D,E
Tr/Tf	10		90	%	Measurement Points	D,E
Cload			150	pF		-
Rpu/Rpd50	-30%	50	30%	kΩ	Programmable	A
Rpu2/Rpd2	-30%	2	30%	kΩ	Programmable	A

Table 106: GPIO 1.8V Electrical Specification

Parameter	Min	Nom	Max	Units	Notes	Val
Voltage (VDD)	3.135	3.3	3.465	V	At pin	-
Vil			0.35*VDD	V		A
Vih	0.65*VDD			V		A
Vhys	0.1			V		D,E
Vol			0.45	V	Imax 8mA	A
Voh	VDD-0.45			V	Imax 4mA	A
Trise	18		75	ns		D,E
Tfall	18		75	ns		D,E
Tr/Tf	10		90	%	Measurement Points	D,E
Cload			150	pF		-
Rpu/Rpd50	-30%	50	30%	kΩ	Programmable	A
Rpu2/Rpd2	-30%	2	30%	kΩ	Programmable	A

Table 107: GPIO 3.3V Electrical Specification

17.9 GPIO Registers

Register Name	GPIO0P0..7CTL0	Address	0x2B..0x32 Page 1	Read/Write			
		Reset Value	0x14				
MSB							LSB
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
reserved	ALT	DIR	DRV	PULL_EN	PULL_LVL	PULL_DIR	DOUT

DOUT	**0** 1	Low output High output (CMOS or high-Z OD)
PULL_DIR	**0** 1	Pull down Pull up
PULL_LVL	0 **1**	2kΩ 50kΩ

PULL_EN	**0** 1	No pull-up or pull-down Pull-up/-down enable
DRV	0 **1**	CMOS Open Drain
DIR	**0** 1	Input Output
ALT	**0** 1	Normal GPIO port GPIO used with alternative function

Register Name	**GPIO0P0..7CTLI**	Address	**0x33..0x3A Page 1**	Read/Write
		Reset Value	0x00	

MSB							LSB
R	R	R	R/W	R/W	R/W	R/W	R
reserved			POL	DEB	IRQCFG		DIN

DIN	**0** 1	Input status low Input status high
IRQCFG	 **00** 01 10 11	Interrupt detection on Disable Negative edge Positive edge Both edges
DEB	 **0** 1	30ms de-bounce filter Off On
POL	 **0** 1	Input polarity: Not inverted inverted

Register Name	**GPIO1P0..7CTL0**	Address	**0x3B..0x42 Page 1**	Read/Write
		Reset Value	0x14	

MSB							LSB
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
reserved	ALT	DIR	DRV	PULL_EN	PULL_LVL	PULL_DIR	DOUT

DOUT	**0** 1	Low output High output (CMOS or high-Z OD)
PULL_DIR	**0** 1	Pull down Pull up
PULL_LVL	0 **1**	2kΩ 50kΩ
PULL_EN	**0** 1	No pull-up or pull-down Pull-up/-down enable
DRV	0 **1**	CMOS Open Drain
DIR	**0** 1	Input Output
ALT	**0** 1	Normal GPIO port GPIO used with alternative function

Register Name	**GPIO1P0..7CTLI**		Address	**0x43..0x4A Page 1**	Read/Write		
			Reset Value	0x00			
MSB							LSB
R	R	R	R/W	R/W	R/W	R/W	R
reserved			POL	DEB	IRQCFG		DIN
DIN	**0** 1	Input status low Input status high					
IRQCFG	 **00** 01 10 11	Interrupt detection on Disable Negative edge Positive edge Both edges					
DEB	 **0** 1	30ms de-bounce filter Off On					
POL	 **0** 1	Input polarity: Not inverted inverted					

Register Name	**GPIOIRQ0**		Address	**0x0B Page 1**	Read/Write		
			Reset Value	0x00			
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
GPIO0P7_ IRQ	GPIO0P6_ IRQ	GPIO0P5_ IRQ	GPIO0P4_ IRQ	GPIO0P3_ IRQ	GPIO0P2_ IRQ	GPIO0P1_ IRQ	GPIO0P0_ IRQ
GPIO0P0_IRQ	**0** 1	No pending Interrupt Interrupt pending					
GPIO0P1_IRQ	**0** 1	No pending Interrupt Interrupt pending					
GPIO0P2_IRQ	**0** 1	No pending Interrupt Interrupt pending					
GPIO0P3_IRQ	**0** 1	No pending Interrupt Interrupt pending					
GPIO0P4_IRQ	**0** 1	No pending Interrupt Interrupt pending					
GPIO0P5_IRQ	**0** 1	No pending Interrupt Interrupt pending					
GPIO0P6_IRQ	**0** 1	No pending Interrupt Interrupt pending					
GPIO0P7_IRQ	**0** 1	No pending Interrupt Interrupt pending					

Register Name		GPIOIRQ1		Address	0x0C Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
GPIO1P7_IRQ	GPIO1P6_IRQ	GPIO1P5_IRQ	GPIO1P4_IRQ	GPIO1P3_IRQ	GPIO1P2_IRQ	GPIO1P1_IRQ	GPIO1P0_IRQ

GPIO1P0_IRQ	**0** 1	No pending Interrupt Interrupt pending
GPIO1P1_IRQ	**0** 1	No pending Interrupt Interrupt pending
GPIO1P2_IRQ	**0** 1	No pending Interrupt Interrupt pending
GPIO1P3_IRQ	**0** 1	No pending Interrupt Interrupt pending
GPIO1P4_IRQ	**0** 1	No pending Interrupt Interrupt pending
GPIO1P5_IRQ	**0** 1	No pending Interrupt Interrupt pending
GPIO1P6_IRQ	**0** 1	No pending Interrupt Interrupt pending
GPIO1P7_IRQ	**0** 1	No pending Interrupt Interrupt pending

Register Name		MGPIO0IRQS0		Address	0x19 Page 1	Read/Write	
				Reset Value	0xFF		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
MGPIO 0P7_IRQ	MGPIO 0P6_IRQ	MGPIO 0P5_IRQ	MGPIO 0P4_IRQ	MGPIO 0P3_IRQ	MGPIO 0P2_IRQ	MGPIO 0P1_IRQ	MGPIO 0P0_IRQ

MGPIO0P0_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO0P1_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO0P2_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO0P3_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO0P4_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO0P5_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO0P6_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO0P7_IRQ	0 **1**	IRQ unmasked IRQ masked

Register Name	MGPIO1IRQS0		Address	0x1A Page 1	Read/Write		
			Reset Value	0xFF			
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
MGPIO 1P7_IRQ	MGPIO 1P6_IRQ	MGPIO 1P5_IRQ	MGPIO 1P4_IRQ	MGPIO 1P3_IRQ	MGPIO 1P2_IRQ	MGPIO 1P1_IRQ	MGPIO 1P_IRQ

MGPIO1P0_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO1P1_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO1P2_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO1P3_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO1P4_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO1P5_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO1P6_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO1P7_IRQ	0 **1**	IRQ unmasked IRQ masked

Register Name	MGPIO0IRQSX		Address	0x1B Page 1	Read/Write		
			Reset Value	0xFF			
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
MGPIO 0P7_IRQ	MGPIO 0P6_IRQ	MGPIO 0P5_IRQ	MGPIO 0P4_IRQ	MGPIO 0P3_IRQ	MGPIO 0P2_IRQ	MGPIO 0P1_IRQ	MGPIO 0P0_IRQ

MGPIO0P0_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO0P1_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO0P2_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO0P3_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO0P4_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO0P5_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO0P6_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO0P7_IRQ	0 **1**	IRQ unmasked IRQ masked

Register Name		MGPIO1IRQSX		Address	0x1C Page 1	Read/Write	
				Reset Value	0xFF		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
MGPIO 1P7_IRQ	MGPIO 1P6_IRQ	MGPIO 1P5_IRQ	MGPIO 1P4_IRQ	MGPIO 1P3_IRQ	MGPIO 1P2_IRQ	MGPIO 1P1_IRQ	MGPIO 1P0_IRQ

MGPIO1P0_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO1P1_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO1P2_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO1P3_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO1P4_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO1P5_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO1P6_IRQ	0 **1**	IRQ unmasked IRQ masked
MGPIO1P7_IRQ	0 **1**	IRQ unmasked IRQ masked

18. External Battery Charger Control

18.1 Overview

In order to determine the appropriate input current limit for the charger during certain scenarios, the CHGDET_B pin is asserted or de-asserted by the USB PHY on the platform depending on output current capability of the USB charger detected.

ILIM0 and ILIM1 pins of DA6021 will output signals to the charger to set the charger input current limit. The external charger is capable of interrupt which will be forwarded to the SoC via DA6021. This interrupt will come from the CHGRINT_B pin. During charging the battery temperature will be monitored.

18.2 Charger Current Limit

The external charger input current limits are set according to the table below

CHRDET_B	ILIM1	ILIM0	Power source	Input current limit
1	0	0	USB DCP	More than 100mA, usually 1.5A
1	0	1	USB SDP	100mA
1	1	1	USB SDP	500mA
x	1	0	AC/DC adapter	Customer specific, limited by max charger output current

Table 108: External Charger Current Limits

The AC/DC adapter usually takes priority over the USB charger as input power to the external battery charger. However, DA6021 detects the AC/DC adapter by monitoring VDCIN_SENSE. DA6021 changes ILIM0 and ILIM1 level immediately VDCIN_SENSE fall below the internal voltage reference threshold to inform the external charger to lower its current limit at the removal of AC/DC adapter.

18.3 External Charger Control Signals

DA6021 has the following I/O pins to interface with a discrete charger and USB PHY.

Name	Dir	Voltage	Signal Description
CHGRINT_B	I	VSYS	Battery charging status and fault interrupt from charger IC, active low. Internal 10kOhm pull-up to VSYS. 0=interrupt, asserted with a minimum pulse width of 200µs
ILIM[1:0]	O	VSYS	External charger input current limits
CHGDET_B	I	VUSBPHY	USB DCP detection. Asserted by USBPHY when it detected a charger that can source more than 100mA Internal 100kOhm pull-up to VSYS 1=SDP detected 0=DCP or CDP/ACA

Table 109: Charger Control Pins

The external battery charger interrupt is routed through DA6021 via CHGRINT_B pin. It alerts the SOC of an interrupt by the CHGRIRQ register in which bit D0 is set at the falling edge of CHGRINT_B if not masked. The interrupt mask registers allow external battery charger interrupt to be masked. There are two sets of interrupt mask registers to offer the flexibility to selectively mask the interrupt in S0 state (MCHGRIRQS0) or in sleep (S0IX, S3, S4) states (MPCHGRIRQSX)

18.4 Battery Charger Registers

There are no configuration registers foreseen for the battery charger

Register Name		**CHRG_IRQ**		Address	**0x0A Page 1**	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R	R/W
Reserved							CHRG_ IRQ
CHRG_IRQ		**0** 1	Charger IRQ not asserted Charger IRQ asserted				

Register Name		**MCHRG_IRQ_S0**		Address	**0x17 Page 1**	Read/Write	
				Reset Value	0x01		
MSB							LSB
R	R	R	R	R	R	R	R/W
Reserved							MCHRG_ IRQ_S0
CHRG_IRQ		0 **1**	Charger IRQ unmasked Charger IRQ masked				

Register Name		**MCHRG_IRQ**		Address	**0x18 Page 1**	Read/Write	
				Reset Value	0x01		
MSB							LSB
R	R	R	R	R	R	R	R/W
Reserved							MCHRG_ IRQ
CHRG_IRQ		0 **1**	Charger IRQ unmasked Charger IRQ masked				

19. Interrupt Controller

19.1 Overview

The interrupt control unit maintains the state of the First Level IRQ tree and is responsible for asserting and de-asserting the DA6021's IRQ to the application SoC. It contains status bits for interrupts from all the second-level sub-blocks. If unmasked, the second-level interrupts will propagate to the appropriate first-level interrupt bit, as assigned below. If the first-level interrupt is unmasked, it will propagate to the IRQ pin, which will remain high as long as unmasked interrupts have not been cleared.

19.2 First Level Interrupt

DA6021 interrupt signal IRQ signal is connected to a GPIO of the SoC indicating DA6021 unmasked events to be investigated by the SOC while reading the IRQ status registers via I2C.

The DA6021 interrupt scheme contains two levels. The first-level interrupt register contains 6 IRQ bits, and indicates which PMIC sub-block triggered the interrupt. One bit is dedicated to each of the interrupt-causing DA6021 sub-blocks. For all units, the second-level interrupt registers indicate the specific interrupt triggers for each sub-block. A masking system is provided to enable or disable specific interrupt handlers.

If any bits are set in the first-level IRQ mask, the assertion of an interrupt from the masked sub-block(s) will not cause an assertion of the IRQ signal, nor will it set the first-level IRQ bit. By limiting the first-level IRQ bits set to only those that are unmasked; this disambiguates the dispatching of interrupts.

First-Level IRQ bits may not be directly cleared; they are cleared by clearing all unmasked second-level IRQ bits, and then are implicitly cleared.

When all unmasked first-level IRQ bits are implicitly cleared (all unmasked second-level interrupts directly cleared), the IRQ pin is de-asserted.

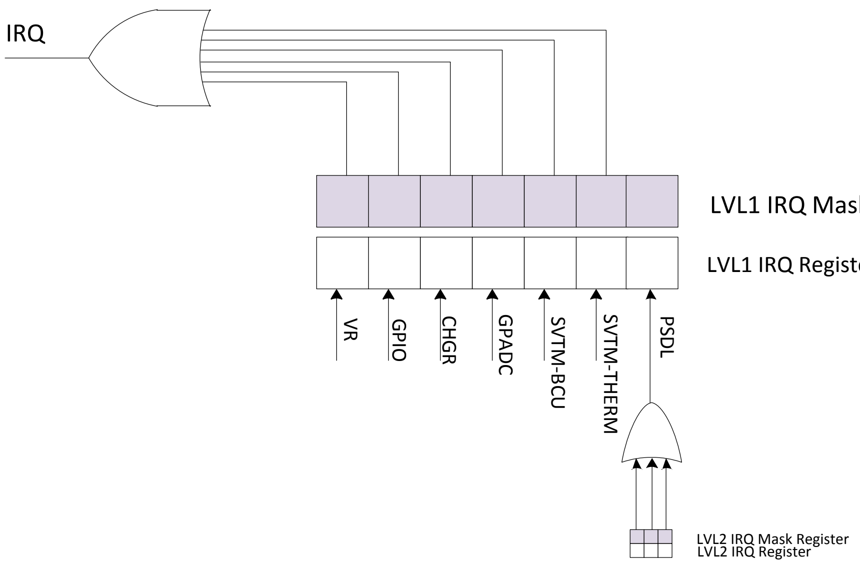


Figure 70: 1st Level Interrupts

19.3 Second Level Interrupt

While First-Level Interrupt bits inform the interrupt handler of which sub-block interrupted, second-level interrupt registers/bits provide the interrupt handler with the specific nature of the block's interrupt event.

If any bits are set in a second-level interrupt mask, then the appropriate second level interrupt bit is prevented from asserting the first level interrupt bit for the corresponding sub-block, nor will the bit become set. (Only unmasked 2nd level interrupt bits may be set).

Interrupt bits are write-1-to-clear. This includes all second-level interrupt register locations. The IRQ signal will not be de-asserted until all unmasked interrupt bits are cleared. For detailed description of Second level interrupts refer to the dedicated blocks in this document.

The table below summarizes the second level interrupts.

Interrupt Name	Register	Source	First-Level Interrupt	Related Status Bit	DESCRIPTION
VBUSDET	PWRSRCIRQ	Input Power source Detection	PWRSRC	SVBUSDET	Indicates that a valid VBUS voltage is detected or removed. Software can test the current cable connection status by checking the SVBUSDET bit in SPWRSRC.
DCINDET	PWRSRCIRQ	Input Power source Detection	PWRSRC	SDCINDET	Triggered when a AC/DC adapter has been detected or removed. The status of the DC cable connection can be verified by reading the SDCINDET bit in SPWRSRC.
BATDET	PWRSRCIRQ	Input Power source Detection	PWRSRC	SBATDET	Interrupt is triggered when a battery is connected or disconnected. The status of the battery connection can be verified by reading the SBATDET bit in SPWRSRC.
SYS0ALRT0	THRMIRQ0	Thermal Control Unit	THRM		Set by the thermal state machine when a system thermistor 0 temperature thermal alert0 occurs
SYS1ALRT0	THRMIRQ0	Thermal Control Unit	THRM		Set by the thermal state machine when a system thermistor 1 temperature alert0 occurs
SYS2ALRT0	THRMIRQ0	Thermal Control Unit	THRM		Set by the thermal state machine when a system thermistor 2 temperature alert0 occurs
PMICALRT0	THRMIRQ0	Thermal Control Unit	THRM		Set by the thermal state machine when a PMIC die temperature alert0 occurs
SYS0ALRT1	THRMIRQ0	Thermal Control Unit	THRM		Set by the thermal state machine when a system thermistor 0 temperature alert1 occurs
SYS1ALRT1	THRMIRQ0	Thermal Control Unit	THRM		Set by the thermal state machine when a system thermistor 1 temperature alert1 occurs
SYS2ALRT1	THRMIRQ0	Thermal Control Unit	THRM		Set by the thermal state machine when a system thermistor 2 temperature alert1 occurs
PMICALRT1	THRMIRQ0	Thermal Control Unit	THRM		Set by the thermal state machine when a PMIC die temperature alert1 occurs
SYS0CRIT	THRMIRQ1	Thermal Control Unit	THRM		Set by the thermal state machine when a system thermistor 0 critical temperature event occurs
SYS1CRIT	THRMIRQ1	Thermal Control Unit	THRM		Set by the thermal state machine when a system thermistor 1 critical temperature event occurs
SYS2CRIT	THRMIRQ1	Thermal Control Unit	THRM		Set by the thermal state machine when a system thermistor 2 critical temperature event occurs
PMICCRIT	THRMIRQ1	Thermal Control	THRM		Set by the thermal state machine when a PMIC die critical temperature event

Interrupt Name	Register	Source	First-Level Interrupt	Related Status Bit	DESCRIPTION
		Unit			occurs
BAT0ALRT0	THRMIRQ2	Thermal Control Unit	THRM		Set by the thermal state machine when a battery thermistor 0 temperature alert0 occurs
BAT1ALRT0	THRMIRQ2	Thermal Control Unit	THRM		Set by the thermal state machine when a battery thermistor 1 temperature alert0 occurs
BAT0ALRT1	THRMIRQ2	Thermal Control Unit	THRM		Set by the thermal state machine when a battery thermistor 0 temperature alert1 occurs
BAT1ALRT1	THRMIRQ2	Thermal Control Unit	THRM		Set by the thermal state machine when a battery thermistor 1 temperature alert1 occurs
BAT0CRIT	THRMIRQ2	Thermal Control Unit	THRM		Set by thermal state machine when a battery thermistor 0 critical temperature event occurs.
BAT1CRIT	THRMIRQ2	Thermal Control Unit	THRM		Set by thermal state machine when a battery thermistor 1 critical temperature event occurs.
VWARNBIRQ	BCUIRQ	BCU	BCU		Triggers whenever the VSYS voltage crosses the VWARNB threshold, rising or falling.
VWARNAIRQ	BCUIRQ	BCU	BCU		Triggers whenever the VSYS voltage crosses the VWARNA threshold, rising or falling.
VCRITIRQ	BCUIRQ	BCU	BCU		Triggers whenever the VSYS voltage crosses the VCRIT threshold, rising or falling.
VBAT	ADCIRQ0	ADC	ADC		Bit is set after completion of VBAT manual conversion if not masked
BATID	ADCIRQ0	ADC	ADC		Bit is set after completion of BATID manual conversion if not masked
PMICTEMP	ADCIRQ0	ADC	ADC		Bit is set after completion of PMIC die temperature manual conversion if not masked
BPTHERM0	ADCIRQ0	ADC	ADC		Bit is set after completion of BPTHERM0 manual conversion if not masked
BPTHERM1	ADCIRQ0	ADC	ADC		Bit is set after completion of BPTHERM0 manual conversion if not masked
SYSTHERM0	ADCIRQ0	ADC	ADC		Bit is set after completion of SYSTHERM0 manual conversion if not masked
SYSTHERM1	ADCIRQ0	ADC	ADC		Bit is set after completion of SYSTHERM1 manual conversion if not masked
SYSTHERM2	ADCIRQ0	ADC	ADC		Bit is set after completion of SYSTHERM2 manual conversion if not masked
CHRG	CHGRIRQ	Charger Control Unit	CHGR		Triggered when an interrupt input from the external discrete charger is generated.
GPIOxPx	GPIOIRQ	GPIO	GPIO	DINxPx	Each GPIO pin can be configured as input with programmable interrupt edge

Interrupt Name	Register	Source	First-Level Interrupt	Related Status Bit	DESCRIPTION
					for rise, fall or both. See GPIOxPxCTLI registers for INTCNTxPx setting. Triggered when the conditions set with GPIOxPxCTLI registers have been met. The status of the GPIO input can be verified by reading the DINxPx bit from the GPIOxPxCTLI register.
VHDMIOCP	VHDMIIRQ	VHDMI	VHDMIOCP		Bit is set when VHDMI over current condition occurs if not masked

Table 110: Second Level Interrupts

19.4 Critical Race Condition (set vs. clear)

An IRQ register can only be cleared by the SoC. This can lead to a potential for critical race if a certain block try to assert the interrupt and at the same time the clearing command comes from the SoC. In this case it is given priority to the block skipping the clearing. In this case the SoC will try to clear it again. Due to block running with lower frequency (lowest 31,25 KHz) some of the IRQ can be in the SET mode for a time window of circa 30us. This means that the IRQ, in the corner case when clear is concurrent, it cannot be cleared within that time window.

19.5 Interrupt Controller Registers

Register Name		IRQLVL1		Address	0x02 Page 1	Read	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R	R
reserved	HDMI	GPIO	CHRG	ADC	BCU	THRM	PSDL

PSDL	**0** 1	PSDL IRQ not asserted PSDL IRQ asserted
THRM	**0** 1	THRM IRQ not asserted THRM IRQ asserted
BCU	**0** 1	BCU IRQ not asserted BCU IRQ asserted
ADC	**0** 1	ADC IRQ not asserted ADC IRQ asserted
CHRG	**0** 1	CHRG IRQ not asserted CHRG IRQ asserted
GPIO	**0** 1	GPIO IRQ not asserted GPIO IRQ asserted
HDMI	**0** 1	HDMI IRQ not asserted HDMI IRQ asserted

Register Name		MIRQLVL1		Address	0x0E Page 1	Read/Write	
				Reset Value	0x7F		
MSB							LSB
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
reserved	MHDMI	MGPIO	MCHRG	MADC	MBCU	MTHRM	MPSDL

MPSDL	0 **1**	PSDL IRQ unmasked PSDL IRQ masked
MTHRM	0 **1**	THRM IRQ unmasked THRM IRQ masked
MBCU	0 **1**	BCU IRQ unmasked BCU IRQ masked
MADC	0 **1**	ADC IRQ unmasked ADC IRQ masked
MCHRG	0 **1**	CHRG IRQ unmasked CHRG IRQ masked
MGPIO	0 **1**	GPIO IRQ unmasked GPIO IRQ masked
MHDMI	0 **1**	HDMI IRQ unmasked HDMI IRQ masked

20. Power Button & Utility Button

20.1 Overview

The system has two buttons that can be used together to trigger the system to power “on” or “off” in different ways.

The main power button (PWRBTNIN_B) is an active-low input with an internal pull-up resistor to VSYS.

The second button is the Utility button or user interface button (UI button, UIBTN_B). This button is typically used as a home button and also includes the pull-up resistor to VSYS.

Both buttons are de-bounced with a 30ms filter and supervised by a timer unit measuring the pulse length.

20.2 Power/Utility Button Block Diagram

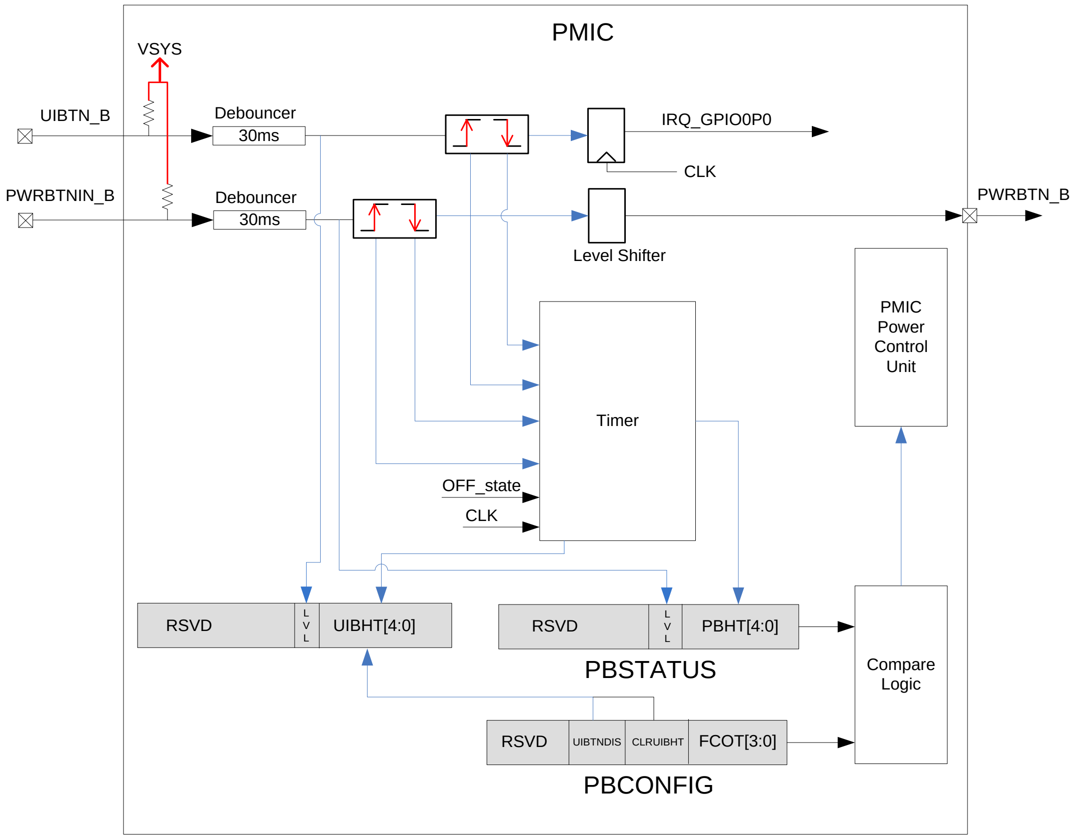


Figure 71 : Power/Utility Button Detection Logic

20.3 PWRBTNIN_B Electrical Parameters

The table below provides the PWRBTNIN_B pad thresholds:

	L->H Vth, high	H->L Vth, low	Vhyst	Val
	[mV]	[mV]	[mV]	
Min	672.5	577.5	95	A
Typ	927.5	732.5	195	A
Max	1158.5	860.5	298	A

20.4 Power Button

The DA6021 PWRBTNIN_B input pin has an internal pull-up resistor (20kΩ ± 10%) to VSYS and includes a 30ms de-bouncing filter of 30ms, ensuring that spurious transitions are not logged. The de-bounced signal is forwarded to the timer logic, measuring the pulse length and comparing it with pre-programmed timing registers. DA6021 passes such power button information level-shifted to the SOC via the PWRBTN_B output pin. Such PWRBTN_B signal is only valid when RSMRST=1.

If the system is in SOC_G3 state and the power button is pressed more than 100ms, the DA6021 switches on all suspend (*_A) rails, de-asserts RSMRST_B after the power button is released and passes the power button information towards the SoC.

If the system is active or down to SOC_S4, pressing the power button will cause DA6021 to pass the level shifted PWRBTNIN_B signal after 100ms de-bouncing to the SoC, which takes the appropriate actions.

20.5 Power Button Cold Boot Flow Diagram

The chart below shows how the boot signal is generated from the power button.

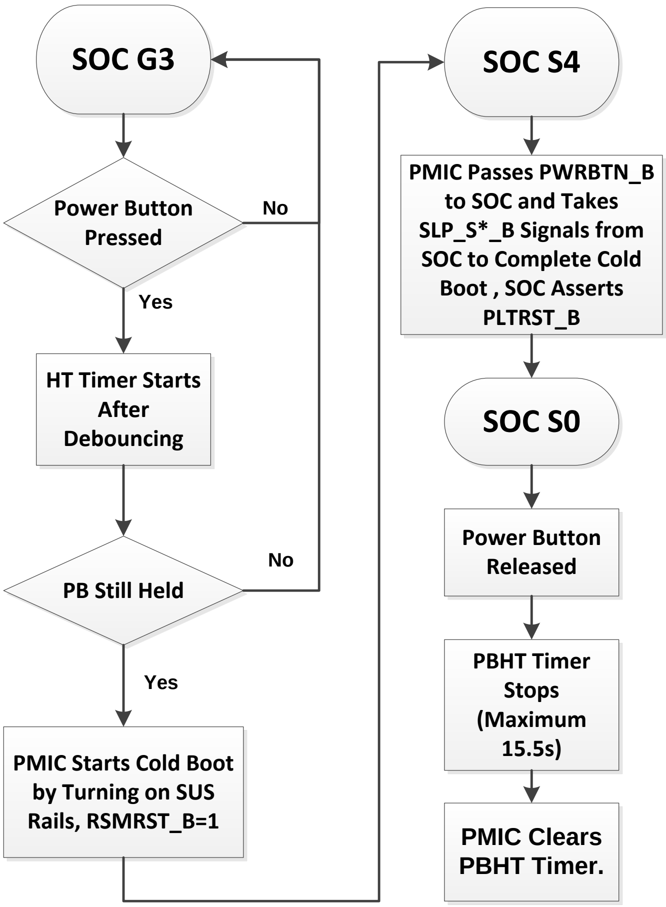


Figure 72: Power Button Boot Flow Diagram

20.6 Force a Cold Off Sequence

DA6021 triggers a "Cold Off" sequence when the power button is hold for more than in register PBCONFIG specified time (default is 4sec). In the event of such a "Cold Off" sequence, DA6021 sets the RFCO (Reset due to Forced Cold Off) in register RESETSRCCRIT and clears the timer PBHT bits in the power button status register PBSTATUS. The PMIC shuts down the system by turning off all its voltage rails in sequence without waiting for instructions (e.g. SLP_S*_B signals) from the SOC.

20.7 Force Cold Off Flow Diagram

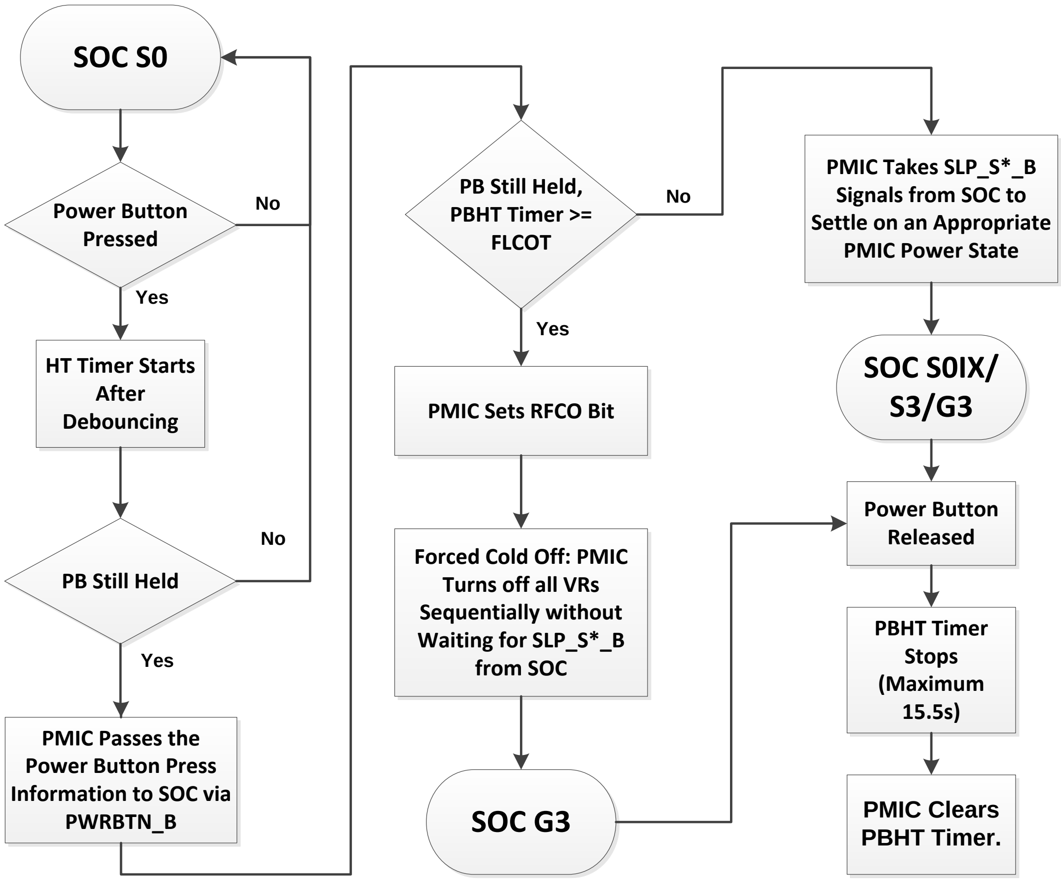


Figure 73: Power Button Cold Off Flow Diagram

20.8 UIBTN_B

The UIBTN_B pin is an input from a platform-defined functional interface button, such as the Home button. The GPIO1P0 pin can be programmed with its alternate function for the UI button. It is internally connected to VSYS via a pull-up resistor (20KOhm±10%). It includes a 30ms de-bouncer to ensure that spurious transitions aren't logged while the switch contacts bounce on initial contact. The output of the de-bouncer enters the edge detect circuits.

Both edges can trigger a utility button interrupt, which is the GPIOP1P0 bit in the second-level GPIO0IRQ Register. It is cleared when a 1 is written to this location. The output of the de-bouncer can be read from the UIBLVL bit of the UIBSTATUS register to determine the current state of the button.

The output of the de-bouncer also goes to the timer logic block that measures the length of time that the button has been held down, and this value can be read from the Hold Time field (UIBHT[4:0]) in the UIBSTATUS register.

20.9 Power Button Registers

Register Name		PBCONFIG		Address	0x26 Page 1	Read/Write	
					0x63		
MSB							LSB
R	R	R/W	R/W	R/W	R/W	R/W	R/W
PBDBCNT		UIBTNDISABLE	CLRUIBHT	FCOT[3:0]			

Field	Value	Description
FCOT[3:0]	 0000 0001 0010 **0011** … 1111	Time that PWR and UI buttons have to be held down together before a system power down is triggered Disable 3.0s 3.5s 4s … 10s
CLRUIBHT	**0** 1	No action performed Reset the UIBTN HT timer logic
UIBTNDISABLE	0 **1**	UIBTN not disabled UIBTN disabled
PBDBCNT	 00 **01** 10 11	Power button input pin debounce time 10ms 30ms 60ms 100ms

Register Name		PBSTATUS		Address	0x27 Page 1	Read	
					0x20		
MSB							LSB
R	R	R	R	R	R	R	R
PBDT		PBLVL	PBHT[3:0]				

Field	Value	Description
PBHT[3:0]	 **00000** 00001 00010 … 11111	Time that PWR button has been held down 0s 0.5s 1s … 15.5s
PBLVL	0 **1**	PWR button pressed PWR button released
PBDT	 00 01 10 11	Power button disable timer, clears when expired not disabled (0s) 30s disabled 60s disabled 120s disabled

Register Name		UBSTATUS		Address	0x28 Page 1	Read	
					0x20		
MSB							LSB
R	R	R	R	R	R	R	R
reserved		UBLVL	UBHT[3:0]				
PBHT[3:0]		 **00000** 00001 00010 … 11111	Time that UI button has been held down 0s 0.5s 1s … 15.5s				
UBLVL		0 **1**	UI button pressed UI button released				

21. Pulse Width Modulation Generation

21.1 Overview

The PWM block is used to generate up to three PWM signals on three dedicated output pins. Mainly they are used to drive display backlight circuits. All the PWM outputs can be enabled on demand. In addition the functionality is gates with power sequencer state as for this the high frequency oscillator is needed in order to provide the 6 MHz clock needed to generate the signal.

21.2 Functional Description

Each of the PWM outputs is able to generate output frequencies from ~23.44 KHz down to ~183Hz in 128 steps.

- f= (6MHz/256) / (FREQ+1)

The duty cycle can be selected between 1/256 to 256/256 (always high).

21.3 PWM Output Signals

There are 3 PWM output signals (PWM[2:0]) on DA6021

Name	I/O	Voltage Level	Pin Mode	Pin Level	Internal pu/pd
PWM[2:0]	O	1.8V	CMOS	Low	no

Table 111: PWM Output Signals

21.4 PWM Registers

Register Name		**PWM1CFG1**		Address	**0x4B Page 1**	Read/Write	
				Reset Value	0x00		
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ENA	FREQ						

FREQ[6:0]	 **0** 1 .. 126 127	f0 = 6MHz/256 f=f0 f=f0/2 … f=f0/127 f=f0/128
ENA	**0** 1	PWM1 disable PWM1 enable

Register Name	PWM2CFG1		Address	0x4C Page 1	Read/Write		
			Reset Value	0x00			
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ENA	FREQ						
FREQ[6:0]		 **0** 1 .. 126 127	f0 = 6MHz/256 f=f0 f=f0/2 … f=f0/127 f=f0/128				
ENA		**0** 1	PWM1 disable PWM1 enable				

Register Name	PWM3CFG1		Address	0x4D Page 1	Read/Write		
			Reset Value	0x00			
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
ENA	FREQ						
FREQ[6:0]		 **0** 1 .. 126 127	f0 = 6MHz/256 f=f0 f=f0/2 … f=f0/127 f=f0/128				
ENA		**0** 1	PWM1 disable PWM1 enable				

Register Name	PWM1CFG0		Address	0x4E Page 1	Read/Write		
			Reset Value	0x00			
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DUTY							
DUTY[7:0]		**0** 1 .. 254 255	High for 1/256 PWM period High for 2/256 PWM period … High for 255/256 PWM period Always high				

Register Name	PWM2CFG0		Address	0x4F Page 1	Read/Write		
			Reset Value	0x00			
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DUTY							
DUTY[7:0]	**0** 1 .. 254 255	High for 1/256 PWM period High for 2/256 PWM period … High for 255/256 PWM period Always high					

Register Name	PWM3CFG0		Address	0x50 Page 1	Read/Write		
			Reset Value	0x00			
MSB							LSB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
DUTY							
DUTY[7:0]	**0** 1 .. 254 255	High for 1/256 PWM period High for 2/256 PWM period … High for 255/256 PWM period Always high					

22. Panel Control

22.1 Overview

The DA6021 provides two pins for display panel control, BACKLIGHT_EN to enable the display backlight circuit and PANEL_EN to enable the display panel electronics. The buffers driving these pins are slew-rate controlled push-pull output buffers similar to the GPIOs, each capable of high-voltage (3.3V) operation.

22.2 Functional Description

This registers are directly driving the BACKLIGHT_EN and PANEL_EN pins of DA6021. SoC has complete control on this.

Register Name	BACKLIGHT_EN			Address	0x51 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R	R/W
Reserved							BACKLIGHT_EN
BACKLIGHT_EN		**0** 1	Backlight off Backlight on				

Register Name	PANEL_EN			Address	0x52 Page 1	Read/Write	
				Reset Value	0x00		
MSB							LSB
R	R	R	R	R	R	R	R/W
reserved							PANEL_EN
PANEL_EN		**0** 1	Panel off Panel on				

23. Debug Ports

There are 2 debug ports foreseen, one for the SVID and another one for the I2C interface

23.1 SVID Debug port

The intent is to disable PMIC SVID buffers connected to the SOC/CPU when in debug mode and redirect communication to an external bus master using a secondary set of pins. This will enable external control of the PMIC interface without SOC/CPU bus contention. In addition, the debug channel enables a point to point bus topology with the external bus master, thereby providing clean signal integrity. The DEBUG_CS signal is used to disable SOC SVID transmission during debug. This will ensure the SOC does not hang awaiting PMIC SVID responses.

A diagram, truth table, and brief write up are provided below.

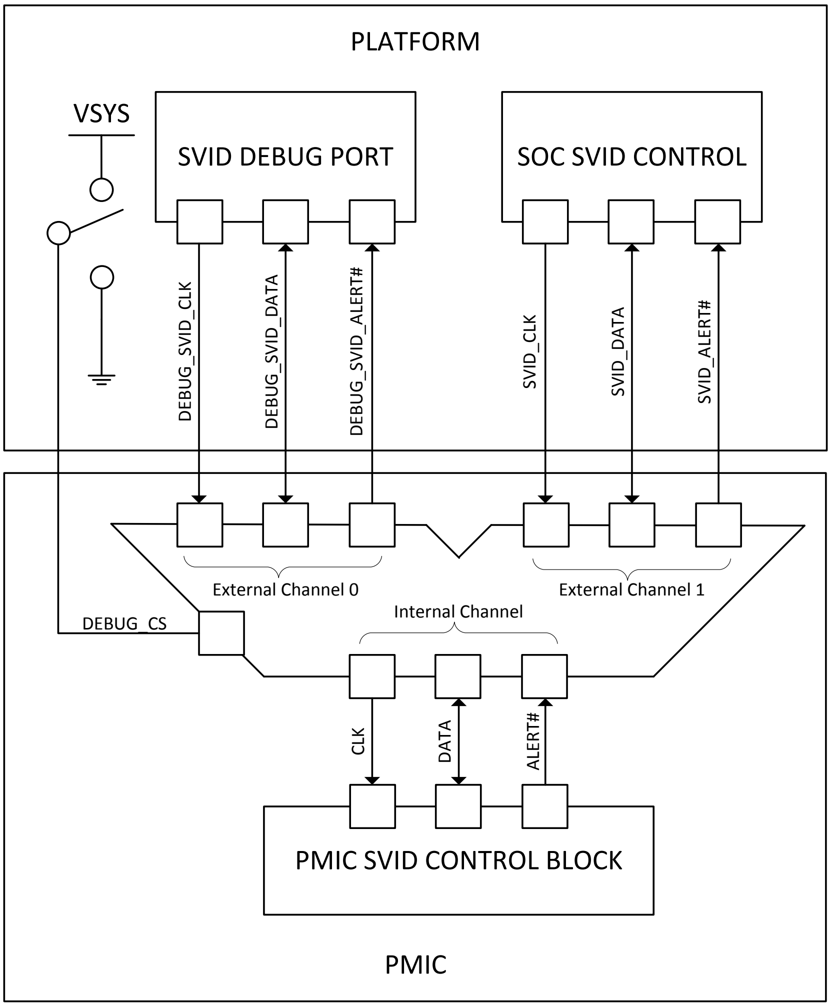


Figure 74: SVID Debug Port Bus Diagram

	External Channel 0 (Debug)			External Channel 1 (SOC)		
DEBUG_CS	DEBUG_SVID_CLK	DEBUG_SVID_DATA	DEBUG_SVID_ALERT#	SVID_CLK	SVID_DATA	SVID_ALERT#
"H" (VSYS)	CLK	DATA	ALERT#	Disabled	Disabled	Disabled
"L" (0V)	Disabled	Disabled	Disabled	CLK	DATA	ALERT#

Table 112: SVID Debug Port Truth Table

To enable external bus master control of the PMIC SVID interface for debug purposes, DA6021 includes an internal bus switch controlled by a SVID channel select pin (DEBUG_CS) as shown in the figure above. When DEBUG_CS is high (tied to VSYS), DA6021 directs the internal channel to external channel 0 and disables the I/O of external channel 1. When DEBUG_CS is low (tied to ground), DA6021 enables communication between External Channel 1 and the internal channel, with External Channel 0 I/O disabled. Both channels are compliant to the VR12/IMVP7 SVID timing and signaling protocols.

23.2 I2C Debug port

This addresses I2C in a way similar to the SVID. The intent is to disable DA6021 I2C buffers connected to the SOC when in debug mode and redirect communication to an external bus master using a secondary set of pins. This will enable external control of the DA6021 interface without SOC/CPU bus contention. In addition, the debug channel enables a point to point bus topology with the external bus master, thereby providing clean signal integrity.

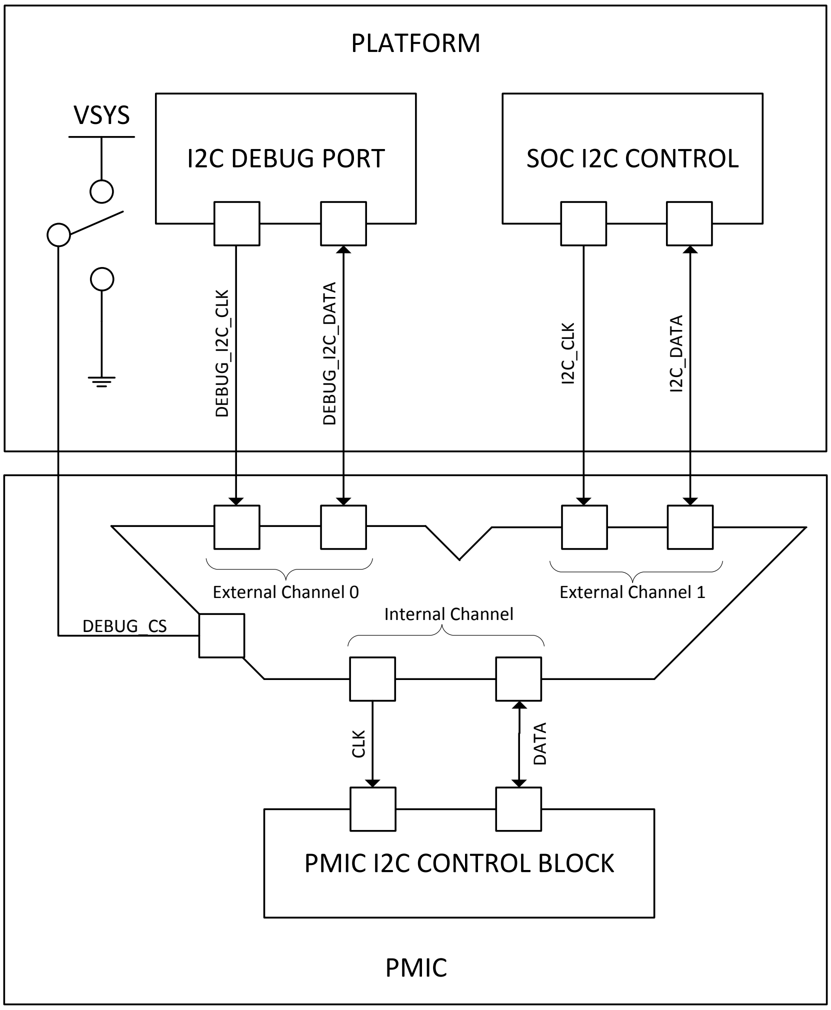


Figure 75: I2C Debug Port Bus Diagram

A diagram, truth table, and brief write up are provided below.

	External Channel 0 (Debug)		External Channel 1 (SOC)	
DEBUG_CS	DEBUG_I2C_CLK	DEBUG_I2C_DATA	I2C_CLK	I2C_DATA
“H” (VSYS)	CLK	DATA	Disabled	Disabled
“L” (0V)	Disabled	Disabled	CLK	DATA

Table 113: I2C Debug Port Truth Table

To enable external bus master control of DA6021 I2C interface for debug purposes, DA6021 includes an internal bus switch controlled by an I2C channel select pin (DEBUG_CS) as shown in the figure above. When DEBUG_CS is tied to VSYS, DA6021 directs the internal channel to external channel 0 and disables the I/O of external channel 1. When DEBUG_CS is tied to ground, DA6021 enables communication between External Channel 1 and the internal channel, with External Channel 0 I/O disabled. The debug port supports clock frequencies in the range 400kHz - 3.4Mhz.

24. Register Map

Page 0									
Register name	**Reg addr**	**MSB**							**LSB**
Internal	0x0..0xDA								
SRCWAKECFG	0xDB						ADPWAKEEN	USBWAKEEN	BATWAKEEN
PWRSEQCFG	0xDC				USBSDPCFG	VCCAPWROKCFG	SUSPWRDNACKCFG	DTPWROK	
Internal registers	0xE2..0xFF								
Page 1									
Register name	**Reg addr**	**MSB**							**LSB**
VendorID	0x00	VendorID							
ProductID	0x01	ProductID							
IRQLVL1	0x02		HDMI	GPIO	CHRG	ADC	BCU	THRM	PSDL
PWRSRCIRQ	0x03						BATDET	DCDET	VBUSDET
THERMIRQ0	0x04	PMICALRT1	SYS2ALRT1	SYS1ALRT1	SYS0ALRT1	PMICALRT0	SYS2ALRT0	SYS1ALRT0	SYS0ALRT0
THERMIRQ1	0x05					PMICCRIT	SYS2CRIT	SYS1CRIT	SYS0CRIT
THERMIRQ2	0x06			BAT1CRIT	BAT0CRIT	BAT1ALRT1	BAT0ALRT1	BAT1ALRT0	BAT0ALRT0
BCUIRQ	0x07						VCRIT	VWARNB	VWARNB
ADCIRQ0	0x08	SYSTHERM2	SYSTHERM1	SYSTHERM0	BPTHERM1	BPTHERM0	PMICTEMP	BATID	VBAT
ADCIRQ1	0x09			VSYS	IVDDQ	IV1P05S	IV1P0A	IVNN	IVCC
CHRG_IRQ	0x0A								CHRG_IRG
GPIO0IRQ	0x0B	GPIO0P7_IRQ	GPIO0P6_IRQ	GPIO0P5_IRQ	GPIO0P4_IRQ	GPIO0P3_IRQ	GPIO0P2_IRQ	GPIO0P1_IRQ	GPIO0P0_IRQ
GPIO1IRQ	0x0C	GPIO1P7_IRQ	GPIO1P6_IRQ	GPIO1P5_IRQ	GPIO1P4_IRQ	GPIO1P3_IRQ	GPIO1P2_IRQ	GPIO1P1_IRQ	GPIO1P0_IRQ
VHDMI_IRQ	0x0D								VHDMI_IRQ
MIRQLVL1	0x0E		MHDMI	GPIO	CHRG	ADC	BCU	THRM	PSDL
MPWRSRCIRQS0	0x0F						MBATDET_S0	MDCDET_S0	MVBUSDET_S0
MPWRSRCIRQSX	0x10						MBATDET	MDCDET	MVBUSDET
MTHERMIRQ0	0x11	MPMICALRT1	MSYS2ALRT1	MSYS1ALRT1	MSYS0ALRT1	MPMICALRT0	MSYS2ALRT0	MSYS1ALRT0	MSYS0ALRT0
MTHERMIRQ1	0x12					MPMICCRIT	MSYS2CRIT	MSYS1CRIT	MSYS0CRIT
MTHERMIRQ2	0x13			MBAT1CRIT	MBAT0CRIT	MBAT1ALRT1	MBAT0ALRT1	MBAT1ALRT0	MBAT0ALRT0
MBCUIRQ	0x14						MVCRIT	MVWARNB	MVWARNB
MADCIRQ0	0x15	SYSTHERM2	SYSTHERM1	SYSTHERM0	BPTHERM1	BPTHERM0	PMICTEMP	BATID	VBAT
MADCIRQ1	0x16			VSYS	IVDDQ	IV1P05S	IV1P0A	IVNN	IVCC
MCHRG_IRQ_S0	0x17								MCHRG_IRG
MCHRG_IRQ	0x18								MCHRG_IRG
MGPIO0IRQS0	0x19	MGPIO0P7_IRQ	MGPIO0P6_IRQ	MGPIO0P5_IRQ	MGPIO0P4_IRQ	MGPIO0P3_IRQ	MGPIO0P2_IRQ	MGPIO0P1_IRQ	MGPIO0P0_IRQ
MGPIO1IRQS0	0x1A	MGPIO1P7_IRQ	MGPIO1P6_IRQ	MGPIO1P5_IRQ	MGPIO1P4_IRQ	MGPIO1P3_IRQ	MGPIO1P2_IRQ	MGPIO1P1_IRQ	MGPIO1P0_RQ
MGPIO0IRQSX	0x1B	MGPIO1P7_IRQ	MGPIO1P6_IRQ	MGPIO1P5_IRQ	MGPIO1P4_IRQ	MGPIO1P3_IRQ	MGPIO1P2_IRQ	MGPIO1P1_IRQ	MGPIO1P0_RQ
MGPIO1IRQSX	0x1C	MGPIO1P7_IRQ	MGPIO1P6_IRQ	MGPIO1P5_IRQ	MGPIO1P4_IRQ	MGPIO1P3_IRQ	MGPIO1P2_IRQ	MGPIO1P1_IRQ	MGPIO1P0_RQ
MVHDMI_IRQ	0x1D								MVHDMI_IRQ
SPWRSRC	0x1E						SBATDET	SDCDET	SVBUSDET
REGLOCK0	0x1F					LOWBATDET	THERMAL	VCRIT_CFG	VREG
RESETSRC0	0x20		RVBATRM	RVSYSOVP	RVSYSUVP	RBATTEMP	RSYSTEMP	RPMICTEMP	RTHERMTRIP
RESTSRC1	0x21						RFCO	RIDBATRM	RVCRIT
WAKESRC	0x22					WAKEADP	WAKEUSB	WAKEBAT	WAKEBTN
LOWBATDET0	0x23	DCBOOT	LOWBATDC			LOWBAT			
LOWBATDET1	0x24	LOWBATDCP				LOWBATSDP			
PSDETCFG	0x25			DBIEN	BATRMSRC	BATRMDEN	BATDBEN	VDCINDBEN	VBUSDBEN
PBCONFIG	0x26	PBDBCNT		UIBTNDISABLE	CLRUIBHT	FCOT			
PBSTATUS	0x27	PBDT		PBLVL	PBHT				
UBSTATUS	0x28			UBLVL	UBHT				

Register name	Reg addr	MSB							LSB
MODEMCTRL	0x29							MODEM_ RSTSEQ	MODEM_ OFF_ST
BBCHR_CFG	0x2A		CHRG_DON E_ST	CHR_ST	CHGI		CHGV		CHEN
GPIO0P0..7_CTLO	0x2B. .0x32		ALT	DIR	DRV	PULL_EN	PULL_LVL	PULL_DIR	DOUT
GPIO0P0..7_CTLI	0x33.. 0x3A				POL	DEB	IRQCFG		DIN
GPIO1P0..7_CTL0	0x3B. .0x42		ALT	DIR	DRV	PULL_EN	PULL_LVL	PULL_DIR	DOU
GPIO1P0..7_CTLI	0x43.. 0x4A				POL	DEB	IRQCFG		DIN
PWM1CFG1	0x4B	ENA	FREQ						
PWM2CFG1	0x4C	ENA	FREQ						
PWM3CFG1	0x4D	ENA	FREQ						
PWM1CFG0	0x4E	Duty							
PWM2CFG0	0x4F	Duty							
PWM3CFG0	0x50	Duty							
BACKLIGHT_EN	0x51								BACKLIGHT_EN
PANEL_EN	0x52								PANEL_EN
Reserved	0x53.. 0x54								
V1P0A_CTRL	0x55	V1P0A_VSEL					NoS0iX	V1P0A_SEL	V1P0A_EN
V1P0S_CTRL	0x56							V1P0S_SEL	V1P0S_EN
V1P0SX_CTRL	0x57							V1P0SX_SEL	V1P0SX_EN
VDDQ_VTT_CTRL	0x58							VDDQ_VTT _SEL	VDDQ_VTT _EN
V1P05S_CTRL	0x59	V1P05S_VSEL			V1P05SVSEL_S0iX		NoS0iX	V1P05S_SEL	V1P05S_EN
V1P8A_CTRL	0x5A	V1P8A_VSEL					NoS0iX	V1P8A_SEL	V1P8A_EN
V1P8U_CTRL	0x5B							V1P8U_SEL	V1P8U_EN
V1P8S_CTRL	0x5C							V1P8S_SEL	V1P8S_EN
V1P8SX_CTRL	0x5D							V1P8SX_SEL	V1P8SX_EN
VREFDQ0_CTRL	0x5E	VREFDQVSEL						VREFDQ_SEL	VREFDQ_EN
VDDQ_CTRL	0x5F	VDDQ_VSEL					NoS0iX	VDDQ_SEL	VDDQ_EN
V1P2S_CTRL	0x60							V1P2S_SEL	V1P2S_EN
V1P2SX_CTRL	0x61							V1P2SX_SEL	V1P2SX_EN
VSYSU_CTRL	0x62							VSYSU_SEL	VSYSU_EN
VSYSSX_CTRL	0x63							VSYSSX_SEL	VSYSSX_EN
VSYSS_CTRL	0x64							VSYSS_SEL	VSYSS_EN
V2P85S_CTRL	0x65	V2P85S_VSEL						V2P85S_SEL	V2P85S_EN
V2P85SX_CTRL	0x66							V2P85SX_SEL	V2P85SX_EN
V3P3A_CTRL	0x67	V3P3A_VSEL						V3P3A_SEL	V3P3A_EN
V3P3U_CTRL	0x68							V3P3U_SEL	V3P3U_EN
V3P3S_CTRL	0x69							V3P3S_SEL	V3P3S_EN
V5P0S_CTRL	0x6A	V5P0S_VSEL						V5P0S_SEL	V5P0S_EN
VHOST_CTRL	0x6B							VHOST_SEL	VHOST_EN
VBUS_CTRL	0x6C							VBUS_SEL	VBUS_EN
VHDMI_CTRL	0x6D							VHDMI_SEL	VHDMI_EN
Reserved	0x6E.. 0x71								
MANCONV0	0x72	SYSTHERM2	SYSTHERM1	SYSTHERM0	BPTHERM1	BPTHERM0	PMICTEMP	BATID	VBAT
MANCONV1	0x73			VSYS	IVDDQ	IV1P05S	IV1P0A	IVNN	IVCC
SYS0_THRM_RSLH	0x74							SYSTEMP0	
SYS0_THRM_RSLTL	0x75	SYSTEMP0							
…	…	…							
THRMRSLT5H	0x7E							SYSTEMP5	
THRMRSLT5L	0x7F	SYSTEMP5							
VBATRSLTH	0x80							VBAT	
VBATRSLTL	0x81	VBAT							
BATIDRSLTH	0x82							BATID	
BATIDRSLTL	0x83	BATID							
IVCCRSLTH	0x84							IVCC	
IVCCRSLTL	0x85	IVCC							
IVNNRSLTH	0x86							IVNN	
IVNNRSLTL	0x87	IVNN							
IV1P0ARSLTH	0x88							IV1P0A	
IV1P0ARSLTL	0x89	IV1P0A							
IV1P05SRSLTH	0x8A							IV1P05S	
IV1P05SRSLTL	0x8B	IV1P05S							
IVDDQRSLTH	0x8C							IVDDQ	
IVDDQRSLTL	0x8D	IVDDQ							
THRMMONCTL0	0x8E		SYSFRQS	BATFRQS	SYSFRQA		BATFRQA		THRMEN
THRMMONCTL1	0c8F						PMICFRQS	PMICFRQA	
TS_ENABLE	0x90			PMICEN	BAT1EN	BAT0EN	SYS2EN	SYS1EN	SYS0EN

Register name	Reg addr	MSB							LSB
TS_CRIT_ENABLE	0x91			PMICEN	BAT1EN	BAT0EN	SYS2EN	SYS1EN	SYS0EN
TS_A0_STATUS	0x92			PMIC_A0_ST	BAT1_A0_ST	BAT0_A0_ST	SYS2_A0_ST	SYS1_A0_ST	SYS0_A0_ST
TS_A1_STATUS	0x93			PMIC_A0_ST	BAT1_A0_ST	BAT0_A0_ST	SYS2_A0_ST	SYS1_A0_ST	SYS0_A0_ST
SYS0_THRMALRT0H	0x94	A0PEN	A0EN	ALERT0_HYST				ALERT0MSB	
SYS0_THRMALRT0L	0x95	ALERT0LSB							
SYS0_THRMALRT1H	0x96		A1EN	ALERT1_HYST				ALERT1MSB	
SYS0_THRMALRT1L	0x97	ALERT1LSB							
SYS0THERMCRIT	0x98	TCRIT							
SYS1THERMAL0	0x99	A0PEN	A0EN	ALERT0_HYST				ALERT0MSB	
SYS1THERMAL1	0x9A	ALERT0LSB							
SYS1THERMAL2	0x9B		A1EN	ALERT1_HYST				ALERT1MSB	
SYS1THERMAL3	0x9C	ALERT1LSB							
SYS1THERMCRIT	0x9D	TCRIT							
SYS2THERMAL0	0x9E	A0PEN	A0EN	ALERT0_HYST				ALERT0MSB	
SYS2THERMAL1	0x9F	ALERT0LSB							
SYS2THERMAL2	0xA0		A1EN	ALERT1_HYST				ALERT1MSB	
SYS2THERMAL3	0xA1	ALERT1LSB							
SYS2THERMCRIT	0xA2	TCRIT							
BAT0THERMAL0	0xA3	A0PEN	A0EN	ALERT0_HYST				ALERT0MSB	
BAT0THERMAL1	0xA4	ALERT0LSB							
BAT0THERMAL2	0xA5		A1EN	ALERT1_HYST				ALERT1MSB	
BAT0THERMAL3	0xA6	ALERT1LSB							
BAT0THERMCRITH	0xA7	TCRIT[8:1]							
BAT0THERMCRITL	0xA8	TCRIT[9:2]							
BAT1THERMAL0	0xA9	A0PEN	A0EN	ALERT0_HYST				ALERT0MSB	
BAT1THERMAL1	0xAA	ALERT0LSB							
BAT1THERMAL2	0xAB		A1EN	ALERT1_HYST				ALERT1MSB	
BAT1THERMAL3	0xAC	ALERT1LSB							
BAT1THERMCRITH	0xAD							TCRIT	
BAT1THERMCRITL	0xAE	TCRIT							
PMICTHERMAL0	0xAF	A0PEN	A0EN	ALERT0_HYST				ALERT0MSB	
PMICTHERMAL1	0xB0	ALERT0LSB							
PMICTHERMAL2	0xB1		A1EN	ALERT1_HYST				ALERT1MSB	
PMICTHERMAL3	0xB2	ALERT1LSB							
PMICTHERMCRIT	0xB3	TCRIT							
VWARNA_CFG	0xB4	VWARNA_DEB				VWARNA_EN	VWARNA		
VWARNB_CFG	0xB5	VWARNB_DEB				VWARNB_EN	VWARNB		
VCRIT_CFG	0xB6		VCRIT_DEB	VCRITSDWNEN		VCRIT_EN	VCRIT		
DISA_BEH	0xB7						DISA_STICKY	DISA_POL	DISA_EN
DISB_BEH	0xB8						DISB_STICKY	DISB_POL	DISB_EN
DISCRIT_BEH	0xB9						DISCRIT_STICKY	DISCRIT_POL	DISCRIT_EN
PROCHOT_BEH	0xBA						PROCHOT_BST	PROCHOT_B_VWB_EN	PROCHOT_B_VWB_EN
BCUTRIP_ST	0xBB						SVCRIT	SVWARNA	SVWARNB
BCUOUT_ST	0xBC					SDISA	SDISB	SCRIT	SPROCHOT_B
TS_CRIT_ST	0xBD			PMICST	BAT1ST	BAT0ST	SYS2ST	SYS1ST	SYS0ST
reserved	0xBE..0xC5								
VREFDQ1_CTRL	0xC6	VREFDQVSEL						VREFDQ_SEL	VREFDQ_EN
reserved	0xC7..0xFF								

Table 114: DA6021 Register Map

25. Package Information

25.1 DA6021 Package Details

25.1.1 Pin Description, Pin Out

Below is the pin description list of DA6021. In the type column the following abbreviations have been used

- PS, VSS — Power Supply
- DI, DO, DIO — Digital Input, Output, Input/Output
- AI, AO, AIO — Analog Input, Output, Input/Output
- OD — Open-Drain Output

25.1.2 Ball Order

Ball	Name	Type	Description
A1	VSYS41	PS	system power supply
A2	VSYS43	PS	system power supply
A3	VNN_IN2A	PS	VNN buck regulator supply voltage
A4	VNN_IN2B	PS	VNN buck regulator supply voltage
A5	VNN_IN3A	PS	VNN buck regulator supply voltage
A6	VNN_IN3B	PS	VNN buck regulator supply voltage
A7	VNN_IN4A	PS	VNN buck regulator supply voltage
A8	VNN_IN4B	PS	VNN buck regulator supply voltage
A9	VSYS_4	PS	System power supply
A10	V1P8A_INA	PS	V1P8A buck regulator supply voltage
A11	V1P8A_INB	PS	V1P8A buck regulator supply voltage
A12	VDDQ_IN1A	PS	VDDQ buck regulator supply voltage
A13	VDDQ_IN1B	PS	VDDQ buck regulator supply voltage
A14	VDDQ_IN2A	PS	VDDQ buck regulator supply voltage
A15	VDDQ_IN2B	PS	VDDQ buck regulator supply voltage
A16	V2P85S_INA	PS	V2P85S buck boost supply voltage
A17	V2P85S_INB	PS	V2P85S buck boost supply voltage
A18	V2P85S_A	AO	V2P85S output voltage
A19	V2P85S_B	AO	V2P85S output voltage
A20	VCCAPWROK	DO	VCCAPWROK output signal
A21	V1P2SX_IN	AI	V1P2SX input supply
A22	V2P85SX_IN	PS	V2P85SX input supply
A23	V1P2S	AO	V1P2S output voltage
A24	VSYS33	PS	system power supply
A25	VSYS32	PS	system power supply
B1	VSYS42	PS	system power supply
B2	VNN_LX2A	AO	VNN buck LX node phase 2
B3	VNN_LX2B	AO	VNN buck LX node phase 2

B4	VNN_LX3A	AO	VNN buck LX node phase 3
B5	VNN_LX3B	AO	VNN buck LX node phase 3
B6	VNN_LX4A	AO	VNN buck LX node phase 4
B7	VNN_LX4B	AO	VNN buck LX node phase 4
B8	DGND1	VSS	Ground
B9	V1P8S_IN	AI	V1P8S input supply
B10	V1P8A_LXA	AO	V1P8A buck LX node
B11	V1P8A_LXB	AO	V1P8A buck LX node
B12	VDDQ_LX1A	AO	VDDQ buck LX node phase 1
B13	VDDQ_LX1B	AO	VDDQ buck LX node phase 1
B14	VDDQ_LX2A	AO	VDDQ buck LX node phase 2
B15	VDDQ_LX2B	AO	VDDQ buck LX node phase 2
B16	V2P85S_LX1A	AO	buck boost V2P85S LX node 1
B17	V2P85S_LX1B	AO	buck boost V2P85S LX node 1
B18	V2P85S_LX2A	AO	buck boost V2P85S LX node 2
B19	V2P85S_LX2B	AO	buck boost V2P85S LX node 2
B20	DGND11	VSS	Ground
B21	V1P2SX	AO	V1P2SX output voltage
B22	V2P85SX	AO	V2P85SX output voltage
B23	DGND12	VSS	Ground
B24	DGND13	VSS	Ground
B25	VSYS31	PS	system power supply
C1	VNN_IN1B	PS	VNN buck regulator supply voltage
C2	VNN_LX1B	AO	VNN buck LX node phase 1
C3	VNN_GND1A	VSS	Ground
C4	VNN_GND2A	VSS	Ground
C5	VNN_GND3A	VSS	Ground
C6	VNN_GND4A	VSS	Ground
C7	DGND3	VSS	Ground
C8	DGND4	VSS	Ground
C9	V1P8S	AO	V1P8S output voltage
C10	V1P8A_GNDA	VSS	Ground
C11	V1P8A_GNDB	VSS	Ground
C12	VDDQ_GND1A	VSS	Ground
C13	VDDQ_GND1B	VSS	Ground
C14	VDDQ_GND2A	VSS	Ground
C15	VDDQ_GND2B	VSS	Ground
C16	V2P85S_GNDA	VSS	Ground
C17	V2P85S_GNDB	VSS	Ground
C18	IRQ	DO	interrupt output signal
C19	PWM1	AO	PWM1 output signal
C20	PWM0	AO	PWM0 output signal
C21	PWM2	AO	PWM2 output signal
C22	PWM_GND	VSS	Ground

C23	V3P3A_GNDA	VSS	Ground
C24	V3P3A_LX1A	AO	buck boost V3P3A LX node 1
C25	V3P3A_INC	PS	V3P3A buck boost supply voltage
D1	VNN_IN1A	PS	VNN buck regulator supply voltage
D2	VNN_LX1A	AO	VNN buck LX node phase 1
D3	VNN_GND1B	PS	Ground
D4	VNN_GND2B	PS	Ground
D5	VNN_GND3B	PS	Ground
D6	VNN_GND4B	PS	Ground
D7	GPIO0_VDD	VSS	Ground
D8	V1P2A	AO	V1P2A output voltage
D9	V1P8SX	AO	V1P8SX output voltage
D10	V1P8U_FB	AI	V1P8U sense line
D11	V1P8U_EN_B	AO	V1P8U external FET control
D12	V1P8A_FBP	AI	buck V1P8A sense line positive
D13	V1P8A_FBN	AI	buck V1P8A sense line negative
D14	VDDQ_FBP	AI	buck VDDQ sense line positive
D15	VDDQ_FBN	AI	buck VDDQ sense line negative
D16	V2P85S_FBN	AI	buck boost V2P85S sense line positive
D17	V2P85S_FBP	AI	buck boost V2P85S sense line negative
D18	CHGDET_B	DI	USB charger detection input signal
D19	VHOST_EN	DO	VHOST enable signal
D20	VBUS_EN	DO	VBUS enable output signal
D21	PWM_VDD	AI	PWM input supply
D22	V3P3A_FBN	AI	buck boost V3P3A sense line negative
D23	V3P3A_GNDB	VSS	Ground
D24	V3P3A_LX1B	AO	buck boost V3P3A LX node 1
D25	V3P3A_INB	PS	V3P3A buck boost supply voltage
E1	DGND14	VSS	Ground
E2	DGND15	VSS	Ground
E3	GPIO0_GND	VSS	Ground
E4	VNN_FBP	AI	buck VNN sense line positive
E5	GPIO0P4	ADIO	low voltage GPIO 4
E6	GPIO0P3	ADIO	low voltage GPIO 3
E7	GPIO0P2	ADIO	low voltage GPIO 2
E8	GPIO0P1_BATIDOUT	ADIO	low voltage GPIO 1
E9	GPIO0P0_BATIDIN	ADIO	low voltage GPIO 0
E10	SUSPWRDNACK	DI	SUSPWRDNACK input signal
E11	SLP_S4_B	DI	SLP_S4_B input signal
E12	SLP_S0IX_B	DI	SLP_S0iX_B input signal
E13	SLP_S3_B	DI	SLP_S3_B input signal
E14	SDMMC3_PWR_EN_B	DI	SDMMC-card power enable
E15	SDMMC3_1P8_EN	DI	SDMMC-card power select
E16	PWRBTN_B	DO	Power button signal towards SoC

E17	PLTRST_B	DI	platform reset signal
E18	DRAMPWROK	DO	DRAMPWROK output signal
E19	MODEM_OFF_B	DO	Modem off output signal
E20	CHGRINT_B		Interrupt input signal of external charger
E21	THERMTRIP_B		THERMTRIP_B output signal
E22	V3P3A_FBP	AI	buck boost V3P3A sense line positive
E23	V3P3A_GNDC	VSS	Ground
E24	V3P3A_LX1C	AO	buck boost V3P3A LX node 1
E25	V3P3A_INA	PS	V3P3A buck boost supply voltage
F1	SVID_DIO	DIO	SVID data signal
F2	I2C_DATA	DIO	I2C data signal
F3	DEBUG_SVID_DIO	DIO	debug SVID data signal
F4	GPIO0P7	ADIO	low voltage GPIO 7
F5	GPIO0P5	ADIO	low voltage GPIO 5
F6	DGND18	VSS	Ground
F7	DGND19	VSS	Ground
F8	DGND20	VSS	Ground
F9	DGND21	VSS	Ground
F10	DGND22	VSS	Ground
F11	DGND23	VSS	Ground
F12	DGND24	VSS	Ground
F13	DGND25	VSS	Ground
F14	DGND26	VSS	Ground
F15	DGND27	VSS	Ground
F16	DGND28	VSS	Ground
F17	DGND29	VSS	Ground
F18	DGND30	VSS	Ground
F19	DGND31	VSS	Ground
F20	DGND32	VSS	Ground
F21	DGND33	VSS	Ground
F22	V3P3S_FB	AI	V3P3S sense signal
F23	DGND8	VSS	Ground
F24	V3P3A_LX2A	AO	buck boost V3P3A LX node 2
F25	V3P3A_C	AO	buck boost V3P3A output voltage
G1	SVID_CLK	DI	SVID clock signal
G2	I2C_CLK	DI	I2C clock signal
G3	DEBUG_SVID_CLK	DI	debug SVID clock signal
G4	DEBUG_SVID_ALERT_B	DO	debug SVID alert signal
G5	GPIO0P6	ADIO	low voltage GPIO 6
G6	DGND35	VSS	Ground
G7	DGND36	VSS	Ground
G8	DGND37	VSS	Ground
G9	DGND38	VSS	Ground
G10	DGND39	VSS	Ground

G11	DGND40	VSS	Ground
G12	DGND41	VSS	Ground
G13	DGND42	VSS	Ground
G14	DGND43	VSS	Ground
G15	DGND44	VSS	Ground
G16	DGND45	VSS	Ground
G17	DGND46	VSS	Ground
G18	DGND47	VSS	Ground
G19	DGND48	VSS	Ground
G20	DGND49	VSS	Ground
G21	VREFDQ1	AO	VREFDQ1 output voltage
G22	V3P3S_EN_B	AO	V3P3S external FET control signal
G23	DGND9	VSS	Ground
G24	V3P3A_LX2B	AO	buck boost V3P3A LX node 2
G25	V3P3A_B	AO	buck boost V3P3A output voltage
H1	SVID_ALERT_B	DO	SVID alert signal
H2	DEBUG_CS	DI	debug interface selection signal
H3	DEBUG_I2C_CLK	DI	debug I2C clock signal
H4	DEBUG_I2C_DATA	DIO	debug I2C data signal
H5	GPIO1P6	ADIO	high voltage GPIO 6
H6	DGND51	VSS	Ground
H7	DGND52	VSS	Ground
H8	DGND53	VSS	Ground
H9	DGND54	VSS	Ground
H10	DGND55	VSS	Ground
H11	DGND56	VSS	Ground
H12	DGND57	VSS	Ground
H13	DGND58	VSS	Ground
H14	DGND59	VSS	Ground
H15	DGND60	VSS	Ground
H16	DGND61	VSS	Ground
H17	DGND62	VSS	Ground
H18	DGND63	VSS	Ground
H19	DGND64	VSS	Ground
H20	DGND65	VSS	Ground
H21	VREFDQ0	AO	VREFDQ0 output voltage
H22	V3P3U_FB	AI	
H23	DGND10	VSS	Ground
H24	V3P3A_LX2C	AO	buck boost V3P3A LX node 2
H25	V3P3A_A	AO	buck boost V3P3A output voltage
J1	DGND16	VSS	Ground
J2	DGND17	VSS	Ground
J3	VCC_GND1A	VSS	Ground
J4	GPIO1P7	ADIO	high voltage GPIO 7

J5	GPIO1P5	ADIO	high voltage GPIO 5
J6	GPIO1P4	ADIO	high voltage GPIO 4
J7	GPIO1P3	ADIO	high voltage GPIO 3
J8	GPIO1P2	ADIO	high voltage GPIO 2
J9	GPIO1P1	ADIO	high voltage GPIO 1
J10	GPIO1P0_UIBTN_B	ADIO	high voltage GPIO 0
J11	PROCHOT_B	DO	DA6021 high temperature indication
J12	VREFT	AO	Reference thermistor output voltage
J13	VREFB	AO	Reference voltage battery ID measurement
J14	PWRBTNIN_B	AI	power detection input signal
J15	VDCIN_SENSE	AI	DC input voltage detection
J16	ILIM1	DO	charger current control signal 1
J17	ILIM0	DO	charger current control signal 0
J18	ULPI_VBUS_EN	DI	Input signal controlling VBUS_EN signal
J19	RTC_POR		RTC power on reset indication
J20	RSMRST_B	DO	Resume reset output signal
J21	COREPWROK	DO	COREPWROK output signal
J22	V3P3U_EN_B	AO	V3P3U external FET control signal
J23	V1P8A	AO	V1P8A output supply
J24	BACKLIGHT_EN	DO	backlight enable signal
J25	VSDIO_VIN	AI	VSDIO input power
K1	VCC_IN1A	PS	VCC buck regulator supply voltage
K2	VCC_LX1A	AO	VCC buck LX node phase 1
K3	VCC_GND1B	VSS	Ground
K4	VCC_FBN	AI	VCC buck sense line negative
K5	VCC_FBP	AI	VCC buck sense line positive
K6	GPIO1_GND	VSS	Ground
K7	GPIO1_VDD	ADIO	high voltage GPIO input supply
K8	V1P05S_FBN	AI	V1P05S buck sense line negative
K9	V1P05S_FBP	AI	V1P05S buck sense line positive
K10	VDDQ_VTT_R	AO	VDDQ_VTT reference output voltage
K11	VLP	AO	low power regulator output voltage
K12	SYSTHERM0	AI	system thermistor 0 input
K13	VBUS_SENSE	AI	VBUS_SENSE input voltage detection
K14	SYSTHERM2	AI	system thermistor 2 input
K15	BPTHERM0	AI	battery pack 0 thermistor input
K16	BPTHERM1	AI	battery pack 1 thermistor input
K17	V5P0S_FBN	AI	V5P0S buck boost sense line negative
K18	V5P0S_FBP	AI	V5P0S buck boost sense line positive
K19	V1P0A_FBN	AI	V1P0A buck sense line negative
K20	V1P0A_FBP	AI	V1P0A buck sense line positive
K21	BATLOW_B	DO	Low battery detection output signal
K22	ACPRESENT	AI	Indication of availability of external supply
K23	PANEL_EN	DO	LCD panel enable signal

K24	VUSBPHY	AO	VUSBPHY output voltage
K25	VSDIO	AO	VSDIO output voltage
L1	VCC_IN1B	PS	VCC buck regulator supply voltage
L2	VCC_LX1B	AO	VCC buck LX node phase 1
L3	VCC_GND2A	VSS	Ground
L4	VCC_GND2B	VSS	Ground
L5	VCC_GND3A	VSS	Ground
L6	VCC_GND3B	VSS	Ground
L7	VCC_GND4A	VSS	Ground
L8	VCC_GND4B	VSS	Ground
L9	V1P05S_GND	VSS	Ground
L10	VDDQ_VTT_GND	VSS	Ground
L11	VLP_GND	VSS	Ground
L12	SYSTHERM1	AI	system thermistor 1 input
L13	V1P0SX_FB	AI	V1P0SX sense line
L14	VBAT_SENSE	AI	battery voltage sense input signal
L15	VREF0P9	AO	0.9V reference output voltage
L16	VHDMI	AO	VHDMI output voltage
L17	V5P0S_GNDA	VSS	Ground
L18	V5P0S_GNDB	VSS	Ground
L19	V1P0A_GNDA	VSS	Ground
L20	V1P0A_GNDB	VSS	Ground
L21	BATID	DIO	battery ID port
L22	VSYSU_FB	AI	VSYSU sense line
L23	VSYS_SX_FB	AI	VSYS_SX sense line
L24	VSYSU_EN_B	AO	VSYSU external FET control line
L25	VSYS_SX_EN_B	AO	VSYS_SX external FET control line
M1	VSYS11	PS	system power supply
M2	VSYS13	PS	system power supply
M3	VCC_LX2A	AO	VCC buck LX node phase 2
M4	VCC_LX2B	AO	VCC buck LX node phase 2
M5	VCC_LX3A	AO	VCC buck LX node phase 3
M6	VCC_LX3B	AO	VCC buck LX node phase 3
M7	VCC_LX4A	AO	VCC buck LX node phase 4
M8	VCC_LX4B	AO	VCC buck LX node phase 4
M9	V1P05S_LX	AO	buck V1P05S LX node
M10	VSYS_3	PS	system power supply
M11	VDDQ_VTT	AO	VDDQ_VTT output voltage
M12	VSYS_2	PS	system power supply
M13	V1P0S_FB	AI	V1P0S sense line
M14	V1P0SX_EN	AO	V1P0SX external FET control line
M15	VREF12_GND	VSS	Ground
M16	PMICTEST	DI	test signal
M17	V5P0S_LXA	AO	V5P0S buck boost LX node 1

M18	V5P0S_LXB	AO	V5P0S buck boost LX node 1
M19	V1P0A_LXA	AO	V5P0S buck boost LX node 2
M20	V1P0A_LXB	AO	V5P0S buck boost LX node 2
M21	SDWN_B	DO	Shut down warning output signal
M22	BCUDISA	DO	system voltage in warning zone A
M23	I2CM_SCL	DO	EEPROM clock signal
M24	VBATBKUP		coin cell battery supply
M25	VSYS23	PS	system power supply
N1	VSYS12	PS	system power supply
N2	VSYS14	PS	system power supply
N3	VCC_IN2A	PS	VCC buck regulator supply voltage
N4	VCC_IN2B	PS	VCC buck regulator supply voltage
N5	VCC_IN3A	PS	VCC buck regulator supply voltage
N6	VCC_IN3B	PS	VCC buck regulator supply voltage
N7	VCC_IN4A	PS	VCC buck regulator supply voltage
N8	VCC_IN4B	PS	VCC buck regulator supply voltage
N9	V1P05S_IN	PS	buck V1P05S input supply
N10	VSYS_S	PS	system power supply
N11	VDDQ_VTT_IN	AI	VDDQ_VTT input supply
N12	VSYS_1	PS	system power supply
N13	V1P0S_EN	AO	V1P0S external FET control signal
N14	IREF12		bandgap current reference output
N15	VREF12	AO	bandgap voltage reference output
N16	VHDMI_IN	AI	VHDMI supply voltage
N17	V5P0S_A	AO	V5P0S buck boost output voltage
N18	V5P0S_B	AO	V5P0S buck boost output voltage
N19	V1P0A_INA	PS	buck V1P0A input supply
N20	V1P0A_INB	PS	buck V1P0A input supply
N21	BCUDISB	DO	system voltage in warning zone B
N22	BCUDISCRIT	DO	system voltage in critical range
N23	I2CM_SDA	DI	EEPROM data signal
N24	VSYS21	PS	system power supply
N25	VSYS22	PS	system power supply

Table 115: DA6021 Ball Order

25.2 DA6021 325 Pin FCBGA Package

Map of ball allocations as seen from above the package.

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	VSYS41	VSYS43	VNN_IN2A	VNN_IN2B	VNN_IN3A	VNN_IN3B	VNN_IN4A	VNN_IN4B	VSYS_4	V1P8A_INA	V1P8A_INB	VDDQ_IN1A	VDDQ_IN1B
B	VSYS42	VNN_LX2A	VNN_LX2B	VNN_LX3A	VNN_LX3B	VNN_LX4A	VNN_LX4B	DGND1	V1P8S_IN	V1P8A_LXA	V1P8A_LXB	VDDQ_LX1A	VDDQ_LX1B
C	VNN_IN1B	VNN_LX1B	VNN_GND1A	VNN_GND2A	VNN_GND3A	VNN_GND4A	DGND3	DGND4	V1P8S	V1P8A_GNDA	V1P8A_GNDB	VDDQ_GND1A	VDDQ_GND1B
D	VNN_IN1A	VNN_LX1A	VNN_GND1B	VNN_GND2B	VNN_GND3B	VNN_GND4B	GPIO0_VDD	V1P2A	V1P8SX	V1P8U_FB	V1P8U_EN_B	V1P8A_FBP	V1P8A_FBN
E	DGND14	DGND15	GPIO0_GND	VNN_FBP	GPIO0P4	GPIO0P3	GPIO0P2	GPIO0P1_BATIDOUT	GPIO0P0_BATIDIN	SUSPWRDNACK	SLP_S4_B	SLP_S0IX_B	SLP_S3_B
F	SVID_DIO	I2C_DATA	DEBUG_SVID_DIO	GPIO0P7	GPIO0P5	DGND18	DGND19	DGND20	DGND21	DGND22	DGND23	DGND24	DGND25
G	SVID_CLK	I2C_CLK	DEBUG_SVID_CLK	DEBUG_SVID_ALERT_B	GPIO0P6	DGND35	DGND36	DGND37	DGND38	DGND39	DGND40	DGND41	DGND42
H	SVID_ALERT_B	DEBUG_CS	DEBUG_I2C_CLK	DEBUG_I2C_DATA	GPIO1P6	DGND51	DGND52	DGND53	DGND54	DGND55	DGND56	DGND57	DGND58
J	DGND16	DGND17	VCC_GND1A	GPIO1P7	GPIO1P5	GPIO1P4	GPIO1P3	GPIO1P2	GPIO1P1	GPIO1P0_UIBTN_B	PROCHOT_B	VREFT	VREFB
K	VCC_IN1A	VCC_LX1A	VCC_GND1B	VCC_FBN	VCC_FBP	GPIO1_GND	GPIO1_VDD	V1P05S_FBN	V1P05S_FBP	VDDQ_VTT_R	VLP	SYSTHERM0	VBUS_SENSE
L	VCC_IN1B	VCC_LX1B	VCC_GND2A	VCC_GND2B	VCC_GND3A	VCC_GND3B	VCC_GND4A	VCC_GND4B	V1P05S_GND	VDDQ_VTT_GND	VLP_GND	SYSTHERM1	V1P0SX_FB
M	VSYS11	VSYS13	VCC_LX2A	VCC_LX2B	VCC_LX3A	VCC_LX3B	VCC_LX4A	VCC_LX4B	V1P05S_LX	VSYS_3	VDDQ_VTT	VSYS_2	V1P0S_FB
N	VSYS12	VSYS14	VCC_IN2A	VCC_IN2B	VCC_IN3A	VCC_IN3B	VCC_IN4A	VCC_IN4B	V1P05S_IN	VSYS_S	VDDQ_VTT_IN	VSYS_1	V1P0S_EN

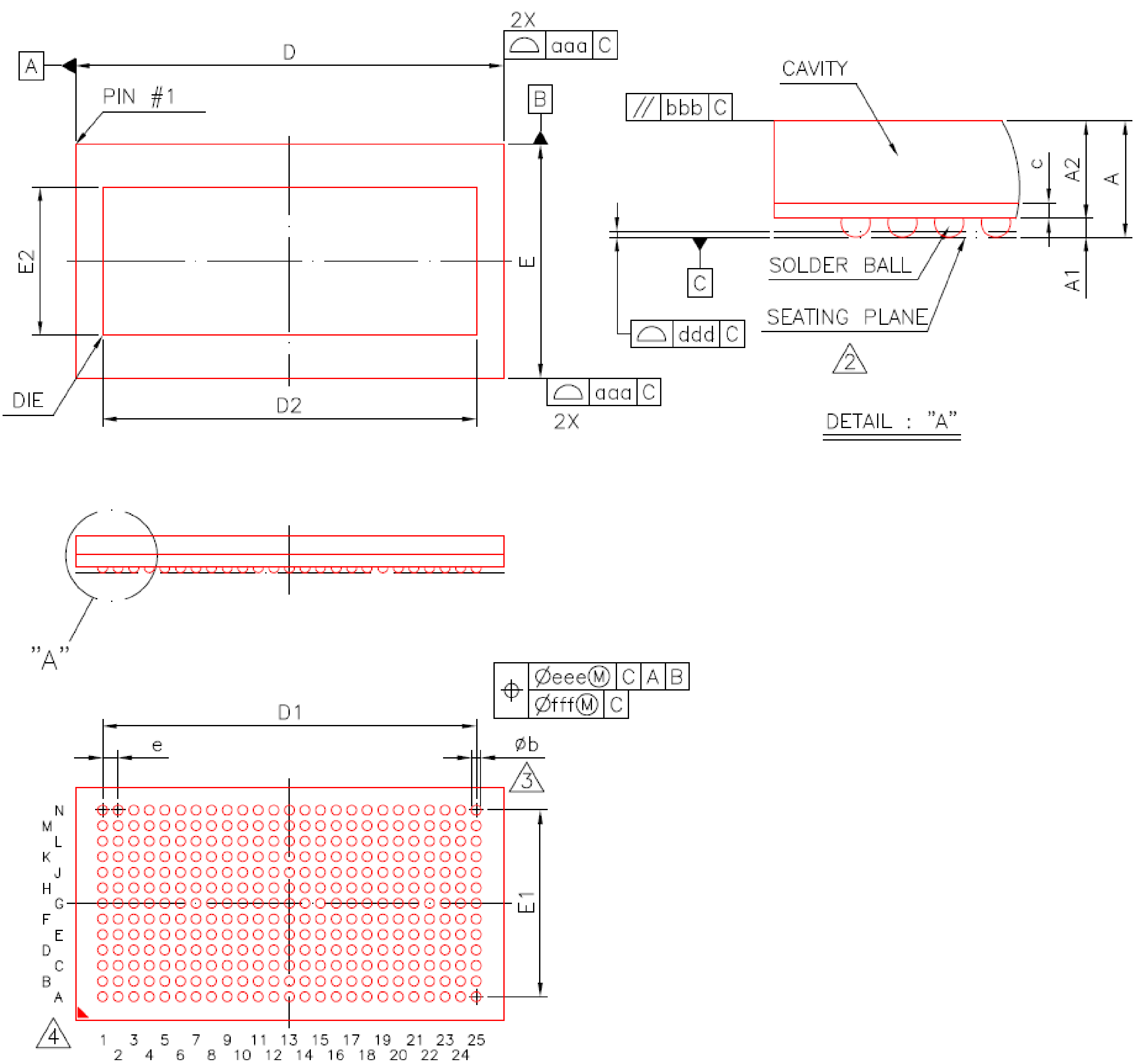
	14	15	16	17	18	19	20	21	22	23	24	25
A	VDDQ_IN2A	VDDQ_IN2B	V2P85S_INA	V2P85S_INB	V2P85S_A	V2P85S_B	VCCAPWROK	V1P2SX_IN	V2P85SX_IN	V1P2S	VSYS33	VSYS32
B	VDDQ_LX2A	VDDQ_LX2B	V2P85S_LX1A	V2P85S_LX1B	V2P85S_LX2A	V2P85S_LX2B	DGND11	V1P2SX	V2P85SX	DGND12	DGND13	VSYS31
C	VDDQ_GND2A	VDDQ_GND2B	V2P85S_GNDA	V2P85S_GNDB	IRQ	PWM1	PWM0	PWM2	PWM_GND	V3P3A_GNDA	V3P3A_LX1A	V3P3A_INC
D	VDDQ_FBP	VDDQ_FBN	V2P85S_FBN	V2P85S_FBP	CHGDET_B	VHOST_EN	VBUS_EN	PWM_VDD	V3P3A_FBN	V3P3A_GNDB	V3P3A_LX1B	V3P3A_INB
E	SDMMC3_PWR_EN_B	SDMMC3_1P8_EN	PWRBTN_B	PLTRST_B	DRAMPWROK	MODEM_OFF_B	CHGRINT_B	THERMTRIP_B	V3P3A_FBP	V3P3A_GNDC	V3P3A_LX1C	V3P3A_INA
F	DGND26	DGND27	DGND28	DGND29	DGND30	DGND31	DGND32	DGND33	V3P3S_FB	DGND8	V3P3A_LX2A	V3P3A_C
G	DGND43	DGND44	DGND45	DGND46	DGND47	DGND48	DGND49	VREFDQ1	V3P3S_EN_B	DGND9	V3P3A_LX2B	V3P3A_B
H	DGND59	DGND60	DGND61	DGND62	DGND63	DGND64	DGND65	VREFDQ0	V3P3U_FB	DGND10	V3P3A_LX2C	V3P3A_A
J	PWRBTNIN_B	VDCIN_SENSE	ILIM1	ILIM0	ULPI_VBUS_EN	RTC_POR	RSMRST_B	COREPWROK	V3P3U_EN_B	V1P8A	BACKLIGHT_EN	VSDIO_VIN
K	SYSTHERM2	BPTHERM0	BPTHERM1	V5P0S_FBN	V5P0S_FBP	V1P0A_FBN	V1P0A_FBP	BATLOW_B	ACPRESENT	PANEL_EN	VUSBPHY	VSDIO
L	VBAT_SENSE	VREF0P9	VHDMI	V5P0S_GNDA	V5P0S_GNDB	V1P0A_GNDA	V1P0A_GNDB	BATID	VSYS_U_FB	VSYS_SX_FB	VSYS_U_EN_B	VSYS_SX_EN_B
M	V1P0SX_EN	VREF12_GND	PMICTEST	V5P0S_LXA	V5P0S_LXB	V1P0A_LXA	V1P0A_LXB	SDWN_B	BCUDISA	I2CM_CLK	VBATBKUP	VSYS23
N	IREF12	VREF12	VHDMI_IN	V5P0S_A	V5P0S_B	V1P0A_INA	V1P0A_INB	BCUDISB	BCUDISCRIT	I2CM_DATA	VSYS21	VSYS22

25.3 Component Marking

Every component will be marked according to the following:

- Product code – DA6021, as referred to in the relevant purchase order.
- Dialog logo.
- Date of manufacture, in a four digit code of the form WWYY (e.g. 3504) or other codes as agreed upon.
- An identification index on the case to identify pin one.

25.4 Package Outline



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	0.99	1.09	0.035	0.039	0.043
A1	0.11	0.16	0.21	0.004	0.006	0.008
A2	0.78	0.83	0.88	0.031	0.033	0.035
c	0.27	0.30	0.33	0.011	0.012	0.013
D	10.93	11.00	11.07	0.430	0.433	0.436
E	5.93	6.00	6.07	0.233	0.236	0.239
D1	---	9.60	---	---	0.378	---
E1	---	4.80	---	---	0.189	---
D2	---	9.60	---	---	0.378	---
E2	---	3.82	---	---	0.150	---
e	---	0.40	---	---	0.016	---
b	0.20	0.25	0.30	0.008	0.010	0.012
aaa	0.07			0.003		
bbb	0.10			0.004		
ddd	0.08			0.003		
eee	0.10			0.004		
fff	0.05			0.002		
MD/ME	25/13			25/13		

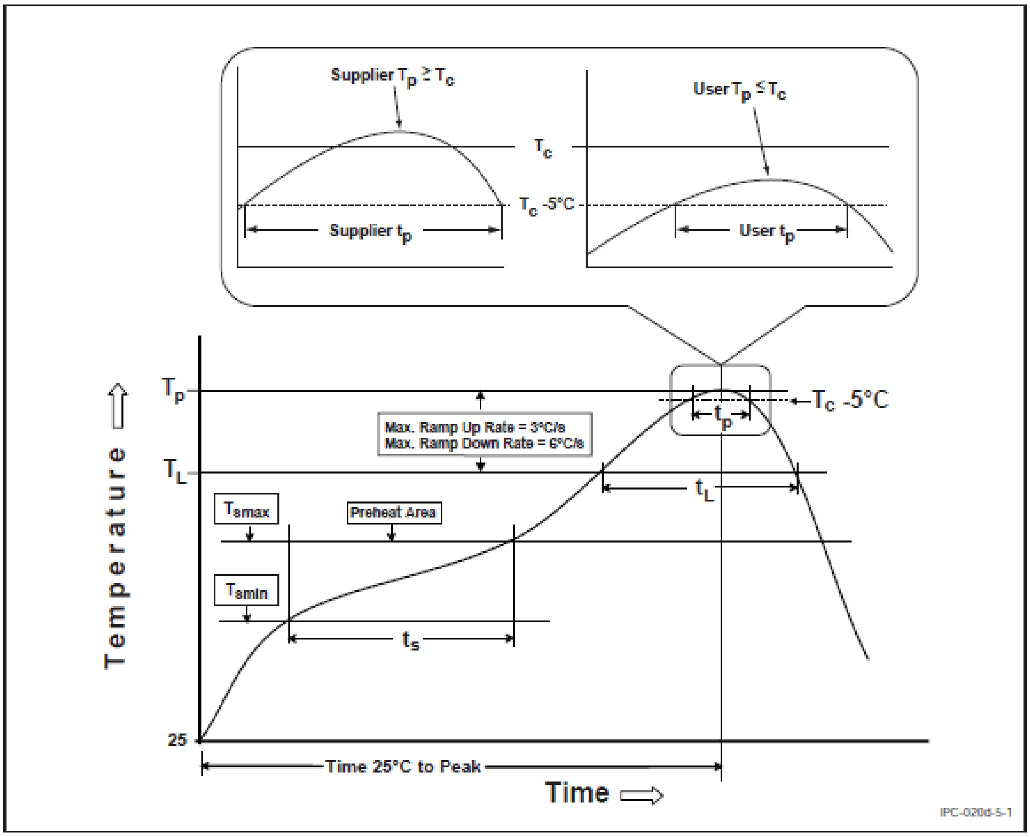
Figure 76: Package Outline Drawing and Dimensions

25.5 Soldering Profile

A PCBA reflow profile depends on the thermal mass of the entire populated board. The actual temperature used in the reflow oven is a function of:

- Solder paste types
- Board density
- Component location
- Component mass
- Board finish

Referring to IPC/JEDEC J-STD-20D.a the figure and table below show the recommended reflow profile condition for 3Sn/37Pb and lead free solder.



Profile Feature	Pb-Free Assembly
Preheat/Soak Temperature Min (T_{smin}) Temperature Max (T_{smax}) Time (t_s) from (T_{smin} to T_{smax})	150 °C 200 °C 60-120 seconds
Ramp-up rate (T_L to T_p)	3 °C/second max.
Liquidous temperature (T_L) Time (t_L) maintained above T_L	217 °C 60-150 seconds
Peak package body temperature (T_p)	For users T_p must not exceed the Classification temp in Table 4-2. For suppliers T_p must equal or exceed the Classification temp in Table 4-2.
Time (t_p)* within 5 °C of the specified classification temperature (T_c), see Figure 5-1.	30* seconds
Ramp-down rate (T_p to T_L)	6 °C/second max.
Time 25 °C to peak temperature	8 minutes max.

Table 116: Soldering Profile

Appendix A: BOM

Voltage rail	#	Value	Tol	Min Voltage	Rmax	Package	Comment
VCC	4	4.7µF	±20%	10V		0603	Supply voltage filter capacitors
	6	47µF	±20%	2.5V		0805	Output stabilization capacitors
	4	0.47µH	±30%		38mΩ	1008	e.g. Taiyo Yuden MAMK2520TR47M
VNN	4	4.7µF	±20%	10V		0603	Supply voltage filter capacitors
	3	47µF	±20%	2.5V		0805	Output stabilization capacitors
	4	0.47µH	±30%		38mΩ	1008	e.g. MAMK2520TR47M
V1P0A	1	4.7µF	±20%	10V		0603	Supply voltage filter capacitors
	2	47µF	±20%	2.5V		0805	Output stabilization capacitors
	1	0.47µH	±30%		38mΩ	1008	e.g. MAMK2520TR47M
V1P05S	1	4.7µF	±20%	10V		0603	Supply voltage filter capacitor
	1	47µF	±20%	2.5V		0805	Output stabilization capacitors
	1	0.47µH	±30%		38mΩ	1008	e.g. MAMK2520TR47M
V1P8A	1	4.7µF	±20%	10V		0603	Supply voltage filter capacitor
	1	47µF	±20%	2.5V		0805	Output stabilization capacitors
	1	0.47µH	±30%		38mΩ	1008	e.g. MAMK2520TR47M
VDDQ	2	4.7µF	±20%	10V		0603	Supply voltage filter capacitors
	2	47µF	±20%	2.5V		0805	Output stabilization capacitors
	2	0.47µH	±30%		38mΩ	1008	e.g. MAMK2520TR47M
V3P3A	1	4.7µF	±20%	10V		0603	Supply voltage filter capacitors
	3	47µF	±20%	6.3V		0805	Output stabilization capacitors
	2	1µH	±30%		38mΩ	1008	e.g. MAMK2520T1R0M or 1x 0.47µH with some efficiency performance degradation
V2P85S	1	4.7µF	±20%	10V		0603	Supply voltage filter capacitor
	1	47µF	±20%	6.3V		0805	Output stabilization capacitor
	1	0.47µH	±30%		38mΩ	1008	e.g. MAMK2520TR47M
V5P0S	2	10µF	±20%	16V		0603	Supply voltage filter capacitors
	2	47µF	±20%	6.3V		0805	Output stabilization capacitors
	1	0.47µH	±30%		38mΩ	1008	e.g. MAMK2520TR47M
VDDQ_VTT_IN	1	100nF	±10%	6.3V		0201	Supply voltage filter capacitor
VDDQ_VTT	1	10µF	±20%	4V		0603	Output stabilization capacitor
VDDQ_VTT_R	1	1µF	±20%	6.3V		0201	Output stabilization capacitor
V1P2S	1	1µF	±20%	6.3V		0201	Output stabilization capacitor
V1P2A	1	1µF	±20%	6.3V		0201	Output stabilization capacitor
VREFDQ0	1	1µF	±20%	6.3V		0201	Output stabilization capacitor
VREFDQ1	1	1µF	±20%	6.3V		0201	Output stabilization capacitor
VLP	1	2.2µF	±10%	6.3V		0201	Output stabilization capacitor
VREF0P9	1	2.2µF	±10%	6.3V		0201	Output stabilization capacitor
VREF12	1	2.2µF	±10%	6.3V		0201	Output stabilization capacitor
IREF12	1	200kΩ	±1%			01005	
VSYS_1	1	100nF	±10%	10V		0201	Supply voltage filter capacitor
VSYS_2	1	100nF	±10%	10V		0201	Supply voltage filter capacitor
VSYS_3	1	100nF	±10%	10V		0201	Supply voltage filter capacitor
VSYS_8_9_10	1	100nF	±10%	10V		0201	Supply voltage filter capacitor
VSYS_11_12_13	1	100nF	±10%	10V		0201	Supply voltage filter capacitor
PWM_VDD	1	1µF	±20%	6.3V		0201	Supply voltage filter capacitor
V1P8A	1	1µF	±20%	6.3V		0201	Output stabilization capacitor
GPIO0_VDD	1	100nF	±10%	10V		0201	Supply voltage filter capacitor
GPIO1_VDD	1	100nF	±10%	10V		0201	Supply voltage filter capacitor

Voltage rail	#	Value	Tol	Min Voltage	Rmax	Package	Comment
V1P8S_IN	1	100nF	±10%	10V		0201	Supply voltage filter capacitor
VHDMI_IN	1	100nF	±10%	10V		0201	Supply voltage filter capacitor
VSDIO_IN	1	100nF	±10%	10V		0201	Supply voltage filter capacitor
V1P05S_FB	1	1µ	±20%	6.3V		0201	
VSDIO	1	100nF	±10%	10V		0201	Output stabilization capacitor
VUSBPHY	1	100nF	±10%	10V		0201	Output stabilization capacitor
V1P2SX	1	100nF	±10%	10V		0201	Output stabilization capacitor
V1P8S	1	100nF	±10%	10V		0201	Output stabilization capacitor
V1P8SX	1	100nF	±10%	10V		0201	Output stabilization capacitor
V2P85SSX	1	100nF	±10%	10V		0201	Output stabilization capacitor
VHDMI	1	100nF	±10%	10V		0201	Output stabilization capacitor
VUSBPHY	1	100nF	±10%	10V		0201	Output stabilization capacitor
VBATBKUP	1	10µF	±20%	6.3V		0201	Output stabilization capacitor
PWRBTNIN_B	0	100nF	±10%	10V		0201	Optional
SYSTHERM0	0	10nF	±20%	10V		0201	optional
SYSTHERM1	0	10nF	±20%	10V		0201	optional
SYSTHERM2	0	10nF	±20%	10V		0201	optional
BPTHERM0	0	10nF	±20%	10V		0201	optional
BPTHERM0	0	10nF	±20%	10V		0201	optional
BATID	0	330pF	±5%	25V		0201	optional
VBUS_SENSE	1	10nF	±20%	25V		0201	Optional
VBAT_SENSE	0	10nF	±20%	10V		0201	optional
VDCIN_SENSE	1	10nF	±20%	10V		0201	optional

Table 117: DA6021 BOM Proposal

Status Definitions

Version	Data Sheet Status	Product Status	Definition
1.<n>	Target	Development	This data sheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This data sheet contains the specifications and preliminary characterisation data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This data sheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via Customer Product Notifications.
4.<n>	Obsolete	Archived	This data sheet contains the specifications for discontinued products. The information is provided for reference only.

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