

DA7210/11 USER MANUAL



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User manual for the set-up and operation of the DA7210/11 evaluation board and control software

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1 Introduction

The DA7210/11 evaluation board has been produced to allow measurement, evaluation and programming of the DA7210/11 ultra-low power audio codec evaluation board and control software. The evaluation PCB is supplied together with a DVD ROM containing documentation and driver files.

The driver software uses a simple graphical user interface (GUI), allowing the DA7210/11 device to be controlled via a USB port of a PC. An additional GUI is available to control the highly configurable filter paths within the DA7210/11; including general purpose, five-band equaliser and high pass filters

The board has a number of jumper links to allow configuration of the board and to provide measurement test points.

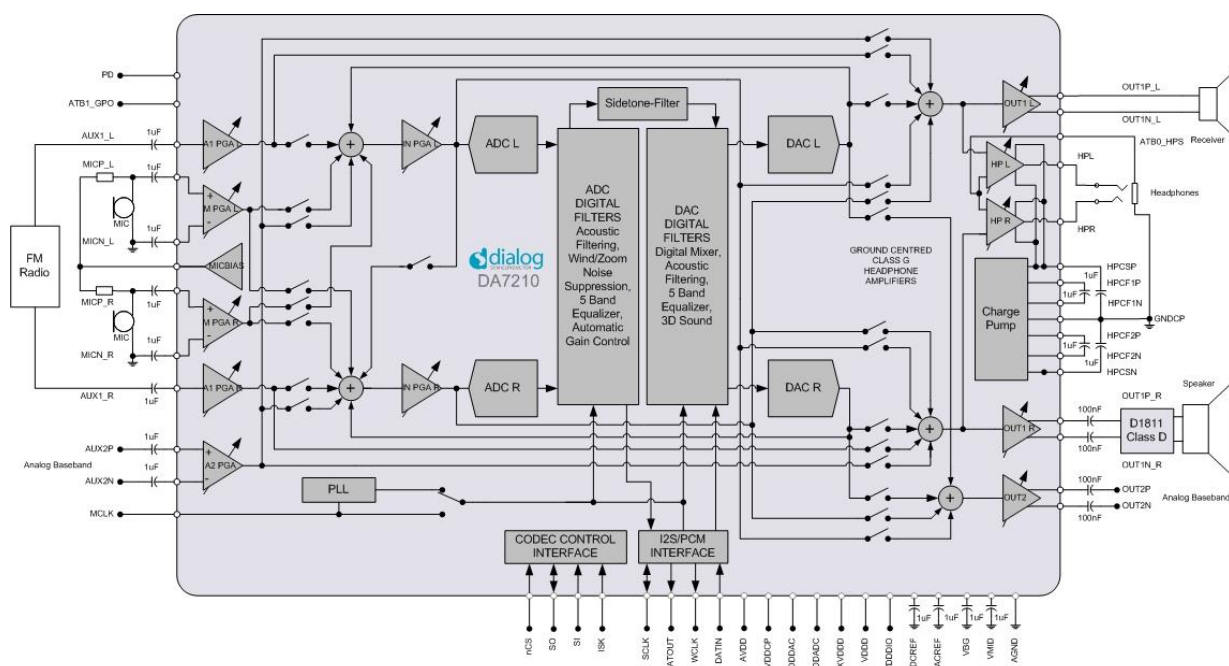


Figure 1 DA7210/11 Block Diagram

The accompanying software requires a PC operating Windows 2000/XP with a USB1.1 or USB2 interface. The software will run under Vista if the default installation location is changed to 'C:\Dialog Semiconductor\'

The DA7210/11 device plus the USB Interface consume approximately 5mA in the standby state. The evaluation board and software are not guaranteed to operate in a USB hub. See the section on Power Supplies below.

The control software permits configuration of the device using either pre-prepared templates or individual write and read operations to all control registers

2 Hardware

There are three options available when using the DA7210/11 evaluation mainboard, Figure 2:

1. A miniboard containing the DA7210 in a CSP 49-pin package connected to evaluation board 44-179-93-02-C via jumpers J28, J30, J36 and J38, Figure 3. This board can also be used standalone or in conjunction with a customer development system.

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2. A miniboard containing the DA7211-00 in a 36-pin CSP package connected to evaluation board 44-179-93-02-B via jumpers J28, J30, J36 and J38, Figure 4. This board can also be used standalone or in conjunction with a customer development system.
3. A miniboard containing the DA7211-01 in a 36-pin CSP package connected to evaluation board 44-179-93-02-E via jumpers J28, J30, J36 and J38,. This board can also be used standalone or in conjunction with a customer development system.

A USB-I2C bridge is used for communication with the device, and there are number of external active components to reduce the requirement for external equipment.

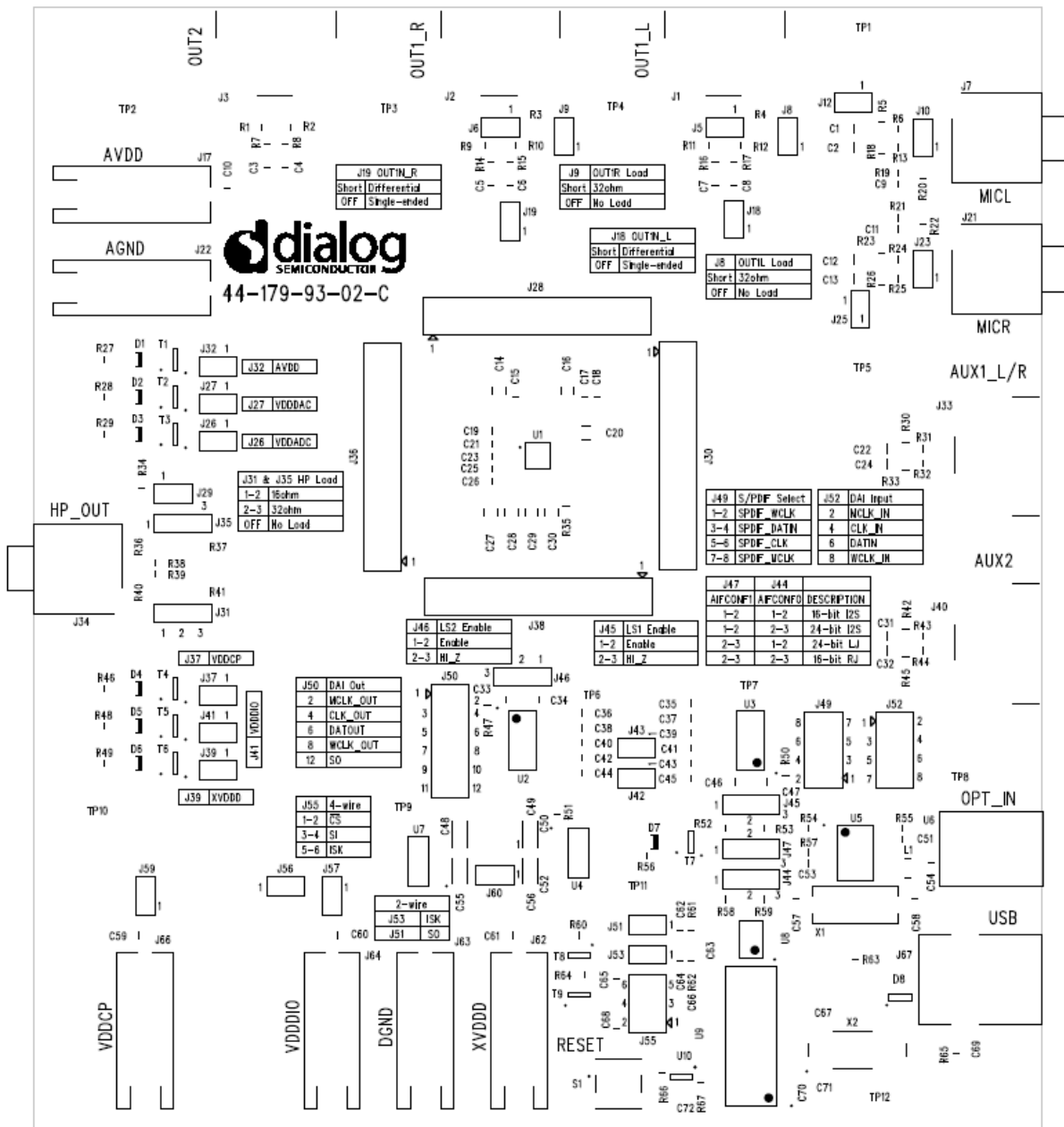


Figure 2 Evaluation Board 44-179-93-02-C Mainboard

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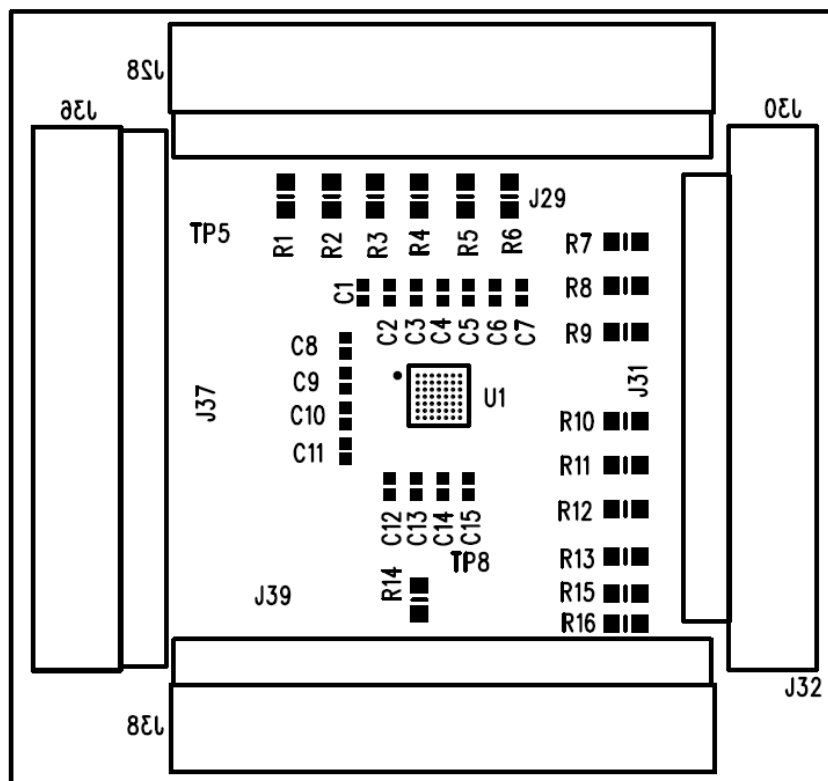


Figure 3 DA7210 44-179-93-04-C Miniboard

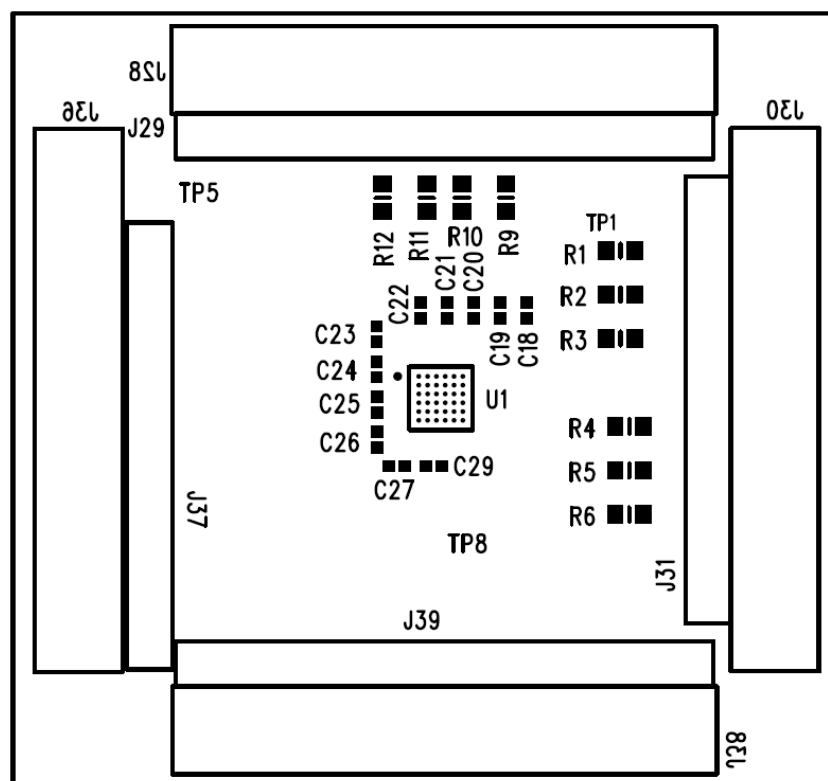


Figure 4 DA7211-00 44-179-93-04-B Miniboard

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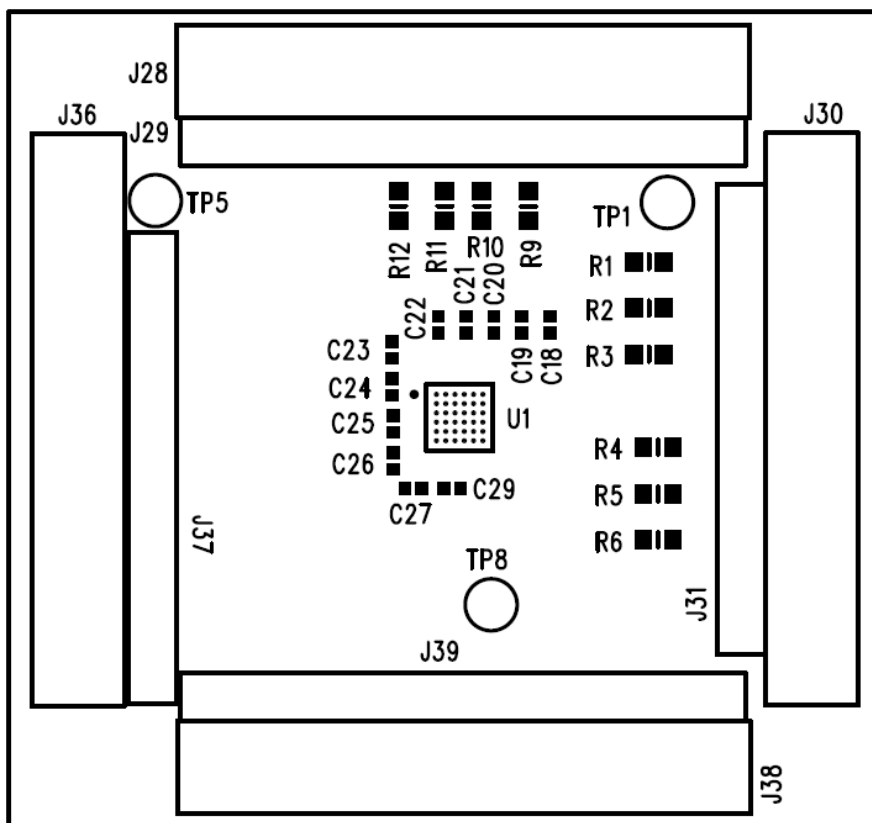


Figure 5 DA7211-01 44-179-93-04-E Miniboard

The passive components needed for noise decoupling or charge pump operation have been placed as close as possible to the DUT pins to ensure optimum operational performance.

Gerber data for the board is available on request.

2.1 Power Supplies

The board is intended to be supplied by power supplies in the range $+1.8V_{dc}$ to $+2.5V_{dc}$ (nominal). The power supplies are connected via 4mm sockets: AVDD, VDDCP, VDDDAC, VDDADC, VDDDIO, DGND and AGND. LEDs D1 to D6 will illuminate when the power supplies are correctly connected.

Some devices on the board will be powered from the $+5V_{dc}$ or $+3.3V_{dc}$ supply produced by the USB interface module.

For demonstration purposes the $+5V_{dc}$ USB supply can be connected to regulator, U9, to produce $+1.8V_{dc}$ capable of supplying all of the DUT the power supply pins. This configuration allows complete DUT operation using just USB and TOSLINK connections only, but maximum headphone power output will be limited when using $+1.8V$ VDDDCP power supply.

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2.2 Jumpers and Link Positions

| Header | Link Position | Function | Notes | |
|--------|---------------|--|-----------------------------------|---------------------|
| J5 | | OUT1_L speaker connection | External connection | |
| J6 | | OUT1_R speaker connection | External connection | |
| J8 | On | OUT1_L 32Ω load selected | | |
| | Off | OUT1_L no load | | |
| J9 | On | OUT1_R 32Ω load selected | | |
| | Off | OUT1_R no load | | |
| J10 | | MIC_L differential connection | | External connection |
| J12 | On | MICN_L single-ended input | | |
| | Off | MICN_L differential input | | |
| J18 | On | OUT1N_L differential output | | |
| | Off | OUT1N_L single-ended output | | |
| J19 | On | OUT1N_R differential output | | |
| | Off | OUT1N_R single-ended output | | |
| J23 | | MIC_R differential connection | External connection | |
| J25 | On | MIC_R single-ended input | | |
| | Off | MIC_R differential input | | |
| J26 | Short link | Short VDDADC current measurement point | N/A for DA7211 | |
| | DMM link | VDDADC current measurement point | | |
| J27 | Short link | Short VDDDAC current measurement point | N/A for DA7211 | |
| | DMM link | VDDDAC current measurement point | | |
| J29 | On | Headphone sense ground connected | Should be disconnected for DA7211 | |
| | Off | Headphone sense ground disconnected | | |
| J31 | 1-2 | HPL 16Ω load selected | | |
| | 2-3 | HPL 32Ω load selected | | |
| J32 | Short link | Short AVDD current measurement point | | |

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| | | | |
|-----------|------------|--|---|
| | DMM link | AVDD current measurement point | |
| J35 | 1-2 | HPR 16Ω load selected | |
| | 2-3 | HPR 32Ω load selected | |
| J37 | Short link | Short VDDCP current measurement point | |
| | DMM link | VDDCP current measurement point | |
| J39 | Short link | Short XVDDD current measurement point | N/A for DA7211 |
| | DMM link | XVDDD current measurement point | |
| J41 | Short link | Short VDDDIO current measurement point | N/A for DA7211 |
| | DMM | VDDDIO current measurement point | |
| J42 | On | WCLK slave mode | |
| | Off | WCLK master mode | |
| J43 | On | CLK slave mode | |
| | Off | CLK master mode | |
| J44 / J47 | 1-2 / 1-2 | 16-bit I2S mode | J44 and J47 must both be set for correct S/PDIF receiver DAI format and word length |
| | 1-2 / 2-3 | 24-bit I2S mode | |
| | 2-3 / 1-2 | 24-bit left justified mode | |
| | 2-3 / 2-3 | 16-bit right justified mode | |
| J45 | 1-2 | DAI input level shift enable | |
| | 2-3 | DAI input level shift high impedance | |
| J46 | 1-2 | DAI output level shift enable | |
| | 2-3 | DAI output level shift high impedance | |
| J48 | On | S/PDIF receiver +5V supply enabled | |
| | Off | S/PDIF receiver +5V supply disabled | |
| J49 | 1-2 | SPDIF word clock | Short links only if no sources are connected to J52 |
| | 3-4 | SPDIF bit clock | |
| | 5-6 | SPDIF data | |
| | 7-8 | SPDIF master clock | |

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| | | | |
|-----|-------|--|---|
| J50 | 1-2 | MCLK output | External connections |
| | 3-4 | CLK output | |
| | 5-6 | DATOUT output | |
| | 7-8 | WCLK output | |
| | 11-12 | SO output | |
| J51 | On | Control interface 2-wire ISK selected | Short only if J55 links are removed |
| | Off | Control interface 2-wire ISK de-selected | |
| J52 | 1-2 | DAI MCLK input | Short only if J49 links are removed |
| | 3-4 | DAI CLK input | |
| | 5-6 | DAI DATIN input | |
| | 7-8 | DAI WCLK input | |
| J53 | On | Control interface 2-wire SO selected | Short only if J55 links removed |
| | Off | Control interface 2-wire SO de-selected | |
| J55 | 1-2 | Control interface 4-wire nCS selected | Short only if J51 and J53 links removed |
| | 3-4 | Control interface 4-wire SI de-selected | |
| | 5-6 | Control interface 4-wire ISK selected | |
| J56 | On | XVDDD connected to VDDCP | |
| | Off | XVDDD disconnected from VDDCP | |
| J57 | On | XVDDD connected to VDDDIO | |
| | Off | XVDDD disconnected from VDDDIO | |
| J59 | On | VDDCP connected to AVDD | |
| | Off | VDDCP disconnected from AVDD | |
| J60 | On | REG_+1.8V supply connected | |
| | Off | REG_+1.8V disconnected | |

Table 1 Jumpers and Link Positions

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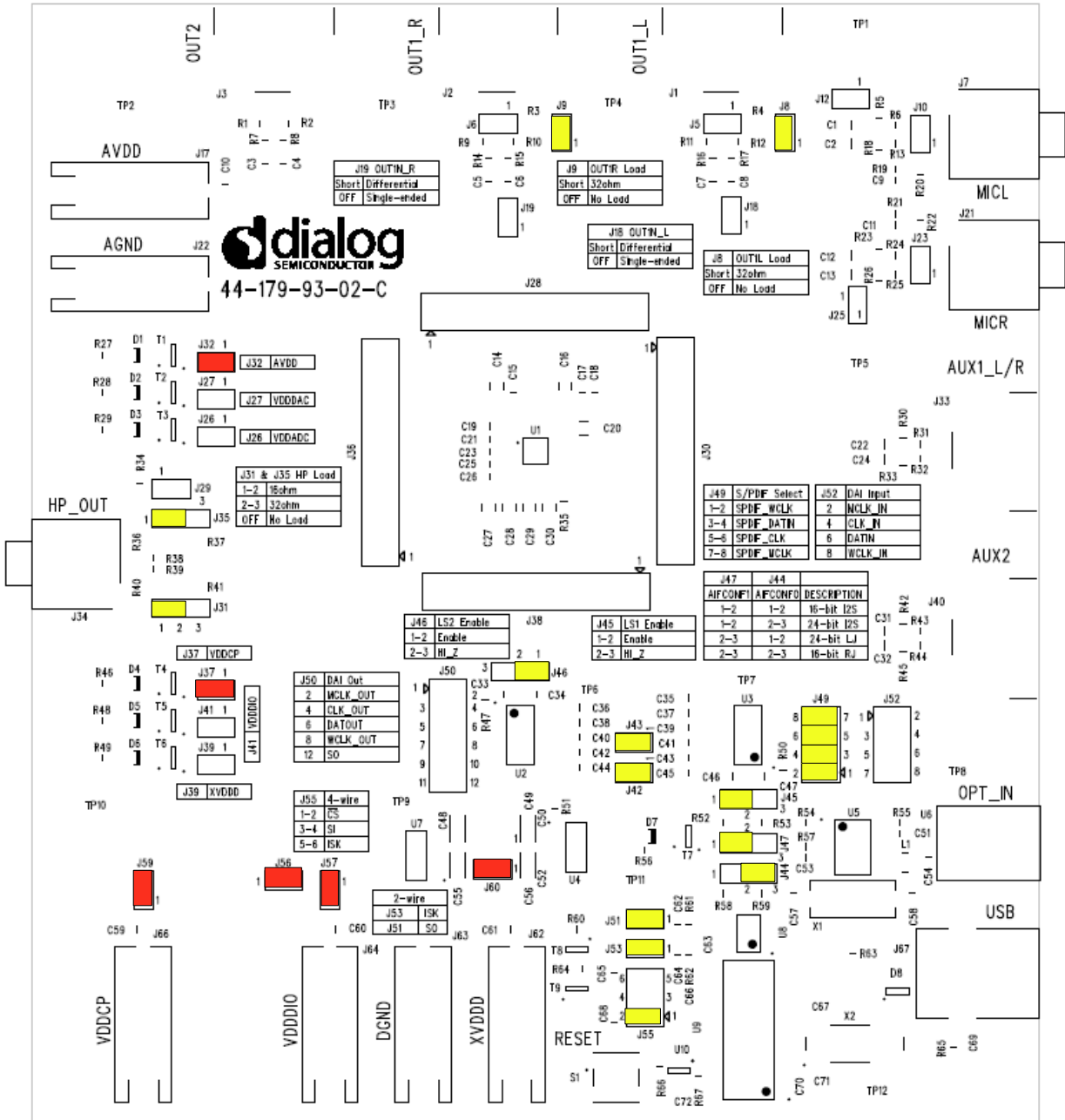


Figure 7 DA7211-00 Default Link Locations

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Figure 9 shows the locations of the jumper links when using the DA7210 with external power supplies to AVDD J66, VDDCP J17, XVDDD J62 and VDDDIO J64. The digital audio interface jumpers are set to receive a TOSLINK input and should be removed to accept other external I2S clocks at J52.

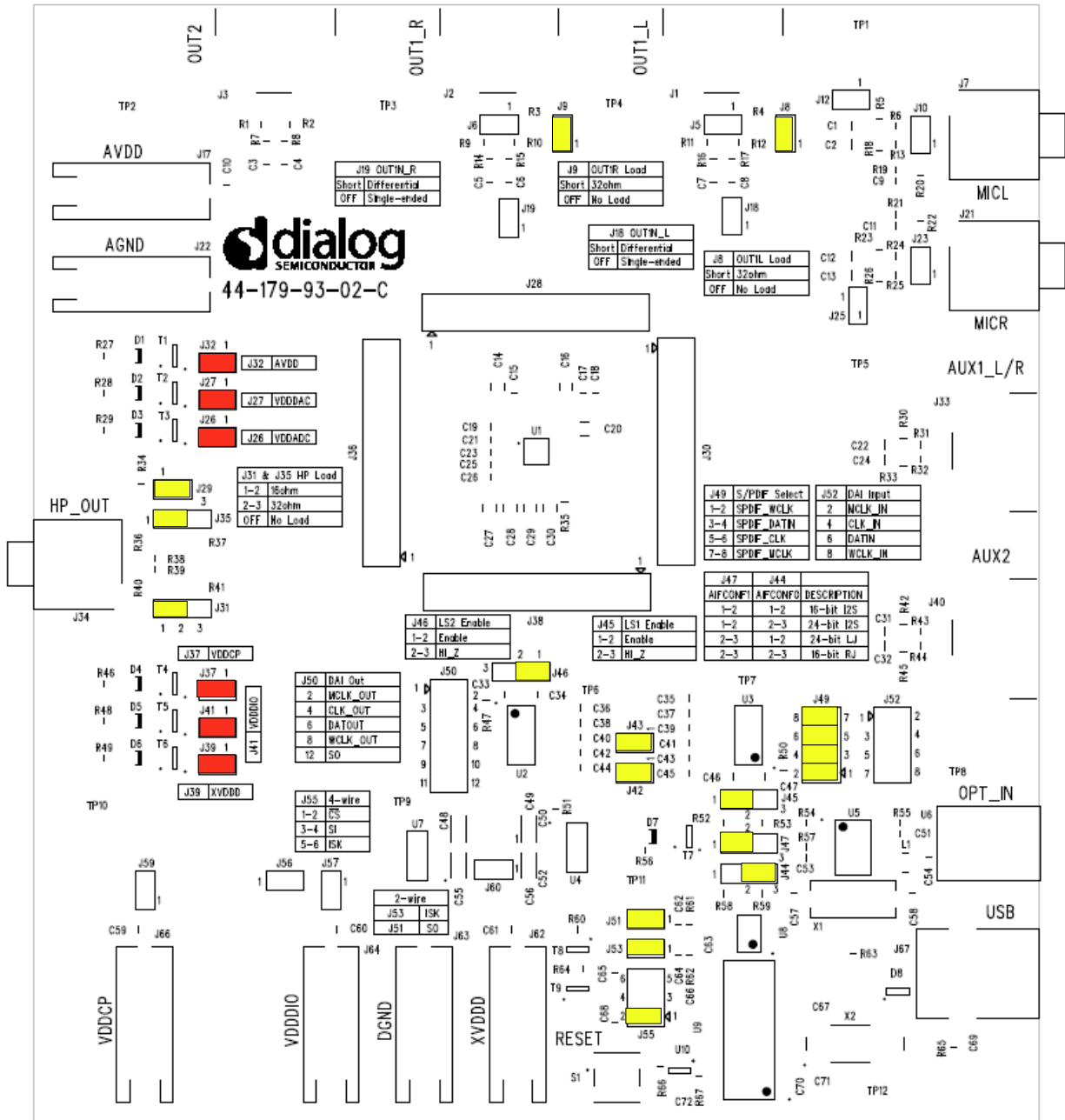


Figure 9 External Power Supply Jumper Configuration

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3 Evaluation Board Features

3.1 USB Interface

The USB Interface is used here for the following purposes:

- As a source of I2C and SPI control signals.
- To provide a discrete signal to the power down pin *PD* (DA7210 only).
- To provide level shifting voltages.
- To allow standalone operation of the evaluation board using the +5V_{dc} USB power supply only.

The USB control signal device is powered by the USB bus cable via a fixed +3.3V_{dc} regulator.

The USB interface control signals can be isolated from rest of the evaluation board by removing J51, J53 and J55 described in Table 1. Removing these jumpers will allow external signal access to the DA7210 control interface. The USB interface can also be used to supply the power supplies to the DUT on the evaluation board.

The USB Interface implements multi-mastering on its I2C interface, permitting concurrent operation with any other multi-mastering controller. This allows the software to control a DA7210/11 device which is already part of the users system, and under control of the system processor.

4 Control Software

4.1 Installation

Insert the DVD-ROM containing the software into the controlling PC. If the installation does not start automatically, run the program 'setup.exe' from the DVD-ROM containing the software. An automated script will install the program to your PC. By default, the directory 'C:\ProgramFiles\Dialog Semiconductor\Audio\DA7210 Rev x.x' will be used.

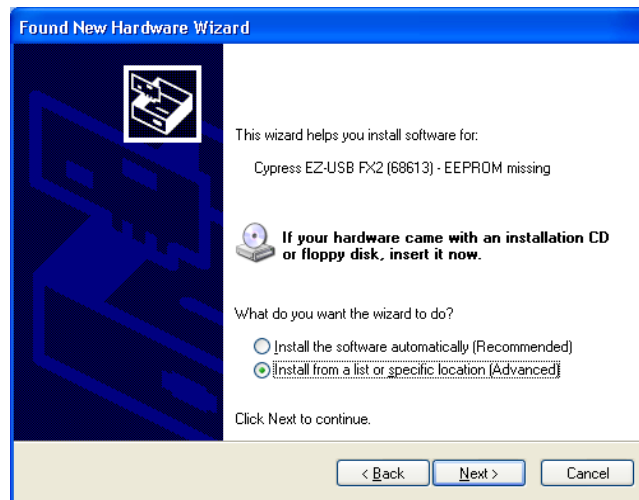
As Windows Vista imposes limitations on the 'C:\Program Files' directory, change this default to 'C:\Dialog Semiconductor\Audio\DA7210 Rev x.x' when prompted.

Plug in the USB cable, and Windows will detect the USB device. It will prompt for the drivers, which should be automatically located on the root directory of the DVD-ROM. The setup file is 'dlgezusb.inf' and the following description explains how to install the driver.

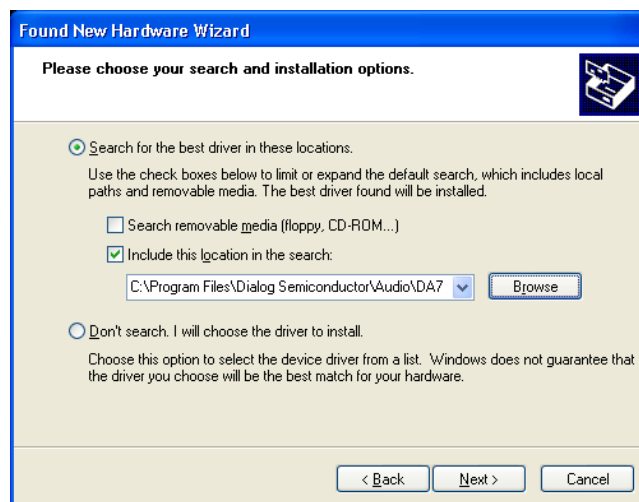


Select No, not this time and press Next >

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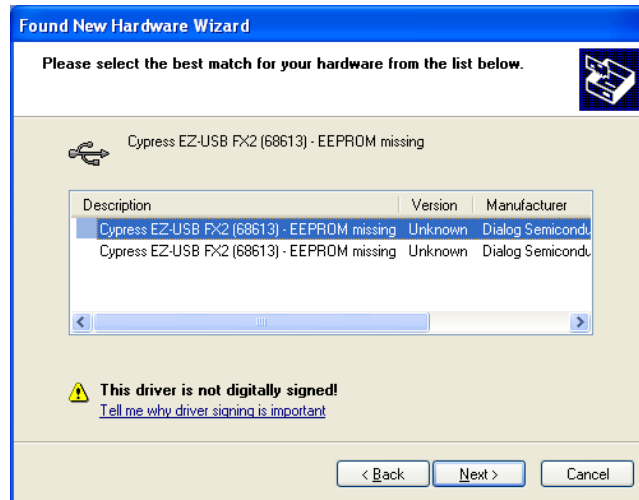
Select Install from a list or specific location (Advanced) and press Next >



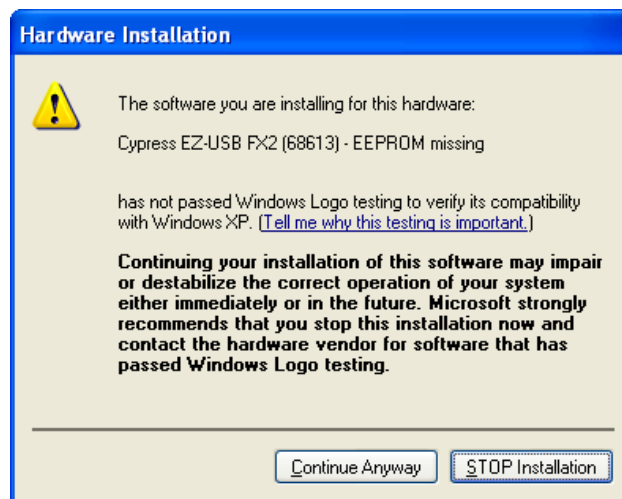
Select Browse and locate the folder

C:\Program Files\Dialog Semiconductor\Audio\DA7210_11 Rev x.x

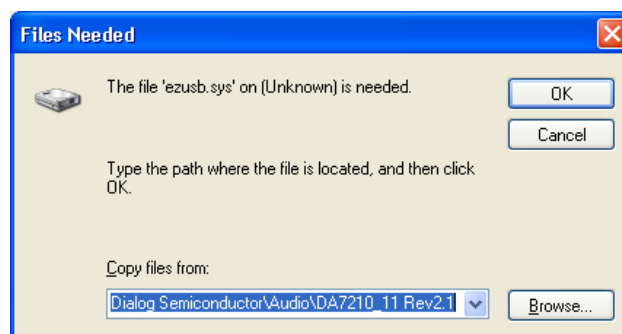
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Select *dlgezusb.inf* and press *Next >*

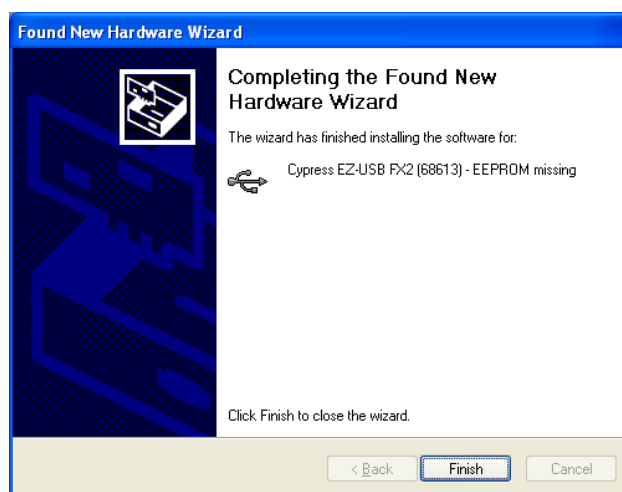


Press Continue Anyway



Select Browse and locate C:\Program Files\Dialog Semiconductor\Audio\DA7210_11 Rev x.x then press OK

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Select Finish

If you are using Windows XP, you may get a message saying that a USB2 device is attached to a USB1.1 port. This can safely be ignored.

To uninstall the software please use the Windows 'Add/Remove Programs' function that can be found under 'Start->Settings->Control Panel'.

4.2 Set-up Files

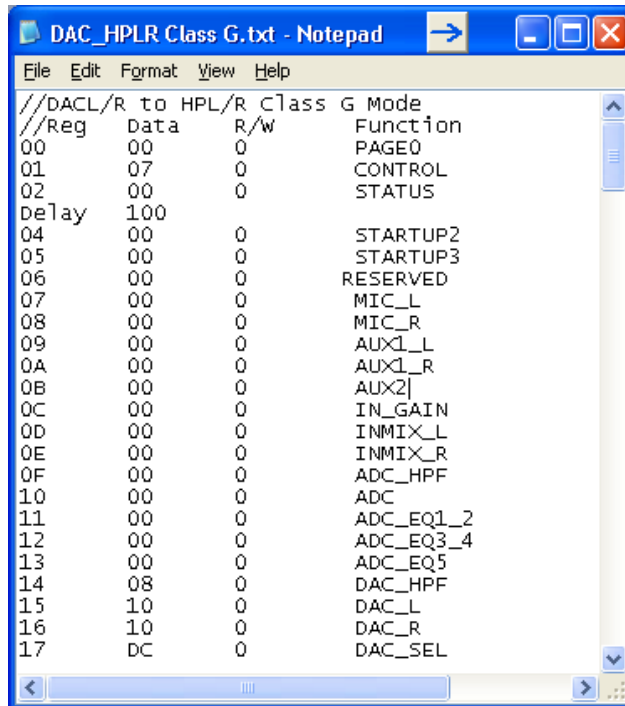
4.2.1 Text File

The DUT registers can be written to by submitting a text file containing the register values; Figure 10 shows an example file. Only the data in the first three columns is required: register, data, R/W; other comments, such as those shown in the example, will be ignored. Lines of text that do not follow register write entries should be preceded by // in order that the line is ignored when reading the text file.

The text file can be created by saving the first three columns of the template spreadsheet file above as a text file or can be created from scratch; it is only necessary for the text file to contain the registers required for set up all others can be omitted.

To add a delay in the file the register value is entered as *Delay* followed by the delay time required in milliseconds. The example in Figure 10 shows a 100ms delay added as the third entry.

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```
File Edit Format View Help
//DACL/R to HPL/R Class G Mode
//Reg Data R/w Function
00 00 0 PAGE0
01 07 0 CONTROL
02 00 0 STATUS
Delay 100
04 00 0 STARTUP2
05 00 0 STARTUP3
06 00 0 RESERVED
07 00 0 MIC_L
08 00 0 MIC_R
09 00 0 AUX1_L
0A 00 0 AUX1_R
0B 00 0 AUX2
0C 00 0 IN_GAIN
0D 00 0 INMIX_L
0E 00 0 INMIX_R
0F 00 0 ADC_HPF
10 00 0 ADC
11 00 0 ADC_EQ1_2
12 00 0 ADC_EQ3_4
13 00 0 ADC_EQ5
14 08 0 DAC_HPF
15 10 0 DAC_L
16 10 0 DAC_R
17 DC 0 DAC_SEL
```

Figure 10 Text Set-up File

A selection of text files can be found on the DVD containing the register control software setup files.

4.2.2 Spreadsheet File

The register settings can be prepared using a spreadsheet file template provided, Figure 11, and saved as a tab delimited text file like Figure 10. The only bits that can be altered on the spreadsheet are the individual register bits in columns G to N and the R/W bit in column O. If any of these bits are set to 1 the bit will be highlighted in green on the register map. If the bit default setting is 1 and the bit value is changed to 0 then the register map bit will be highlighted in grey. This highlighting allows easy visual reference to the register changes from the default settings.

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| Register | Data | HW | Function | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | R | S | T | U | V | X | Y | Default |
|----------|------|----|---------------|----|----|----|----|----|----|----|----|---|---|---|---|---|---|---|---------|
| 01 | 00 | 0 | PAGE0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 02 | 00 | 1 | CONTROL | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 03 | 00 | 0 | STATUS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 04 | 00 | 0 | MIC_L | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 05 | 00 | 0 | MIC_R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 06 | 00 | 0 | AUX1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 07 | 00 | 0 | AUX2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 08 | 00 | 0 | IN_L | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 09 | 00 | 0 | IN_R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 10 | 00 | 0 | INMIX_L | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 11 | 00 | 0 | INMIX_R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 12 | 0A | 00 | ALC_MAKR | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 13 | 0B | 00 | ALC_MN1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 14 | 0C | 00 | ALC_NDIS | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 15 | 0D | 00 | ALC_ATT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 16 | 0E | 00 | ALC_REL | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 17 | 0F | 00 | ALC_DEL | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 18 | 10 | 00 | ALC_CNT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 19 | 11 | 08 | ADC_HPF | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1000 |
| 20 | 12 | 00 | ADC | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 21 | 13 | 00 | ADC_EG1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 22 | 14 | 00 | ADC_EG2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 23 | 15 | 00 | ADC_EG3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 24 | 16 | 54 | ADC_EG4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 100000 |
| 25 | 17 | 08 | DAC_HPF | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1000 |
| 26 | 18 | 88 | DAC | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 27 | 19 | 00 | DAC_EG1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 28 | 1A | 00 | DAC_EG2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 29 | 1B | 00 | DAC_EG3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 30 | 1C | 00 | DAC_SOFT_MUTE | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 31 | 1D | 00 | OUTMIX_L | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 32 | 1E | 80 | OUTMIX_R | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 33 | 1F | 65 | OUT1_L | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 34 | 20 | 65 | OUT1_R | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 35 | 21 | 00 | OUT2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 36 | 22 | 00 | HP_L_VOL | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 37 | 23 | 00 | HP_R_VOL | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 38 | 24 | 00 | HP_CONT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 39 | 25 | 00 | ZEROX | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 40 | 26 | 78 | DAI_SRC_SEL | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 41 | 27 | 08 | DAI_CONF1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 42 | 28 | 00 | DAI_CONF2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 43 | 29 | 80 | DAI_CONF3 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 44 | 2A | 00 | PLL_DMT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 45 | 2B | 00 | PLL_Div2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 46 | 2C | 40 | PLL_Div3 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 10000 |
| 47 | 2D | 6E | PLL | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 10000 |
| 48 | 2E | 00 | GPIA_A0L | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 49 | 2F | 00 | GPIA_A0H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 50 | 30 | 00 | GPIB_A0L | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 51 | 31 | 00 | GPIB_A0H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 52 | 32 | 00 | GPI_C_A0L | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 53 | 33 | 00 | GPI_C_A0H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 54 | 34 | 00 | GPI_D_A0L | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 55 | 35 | 00 | GPI_D_A0H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 56 | 36 | 00 | GPI2_A0L | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 57 | 37 | 00 | GPI2_A0H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 58 | 38 | 00 | GPI2B_A0L | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 59 | 39 | 00 | GPI2B_A0H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 60 | 3A | 00 | GPI2C_A0L | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 61 | 3B | 00 | GPI2C_A0H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 62 | 3C | 00 | GPI2D_A0L | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Figure 11 Spreadsheet Set-up File

DA7210/11 USER MANUAL

4.3 Control Panels

Run the DA7210/11 program by clicking the shortcut on the appropriate item in the Start menu. The best setting for the PC display size is 1024x768 pixels or above. Font size on the PC display should be Normal (95dpi). It is important to note that a display size other than the recommended setting may affect the way in which the panels appear.

4.3.1 Front Panel

The front panel allows selection of a number of methods for programming the registers of the DUT.

- Submit a text file template, which allows register sequencing and time delays to be added.
- Select register map page 0 for individual register read/write access.
- Select register map page 1 for individual register write access.
- Select general purpose filters register map for individual register write access.
- Open a panel to access the volume control registers for real time volume control.
- Direct read/write access to a single register.

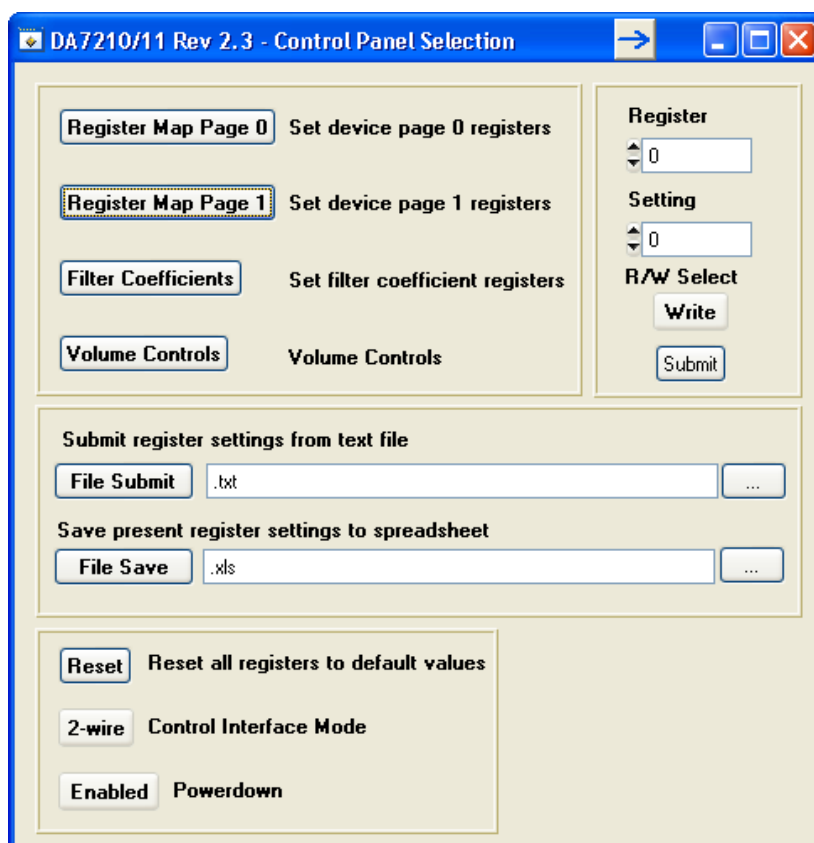


Figure 12 Front Panel

Any file path required can be opened using the ‘...’ button to the right of the corresponding text box, but it must then be submitted or saved using the submit button to the left of the corresponding text box.

DA7210/11 USER MANUAL

It is possible to save the present register settings by selecting a spreadsheet file by locating the filename path using the 'Save present register setting to spreadsheet' box. This function will not read back the device registers, but will only output the values shown on Page 0 and Page 1 of the GUI.

The front panel also contains a reset button, a device power down button and 2-wire/4-wire control selection.

4.3.2 Register Map Page 0

The page 0 register map panel allows read/write access to single bits or to the hex value of a single register; both can be submitted individually.

| Register | R/W | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | Hex | Submit | FUNCTION | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | DEFAULT | |
|----------|-----|----|----|----|----|----|----|----|----|-----|----------|-------------|--------------|------------------|--------------------|------------|-----------------|------------------|--------------------|-----------------|---------|-------|
| 0x00 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | PAGE0 | REG_PAGE | | | | | | | | 0 | |
| 0x01 | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 | - | CONTROL | WRITE_MODE | | ATB1_LEV | ATB1_SEL | NOISE_SUP | BIAS_EN | VDDIO_RANGE | REG_EN | 10000 | |
| 0x02 | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | STATUS | | | | | MUTING | SOFTMUTED | I2S_LOCK | PLL_LOCK | 0 | |
| 0x03 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | STARTUP1 | SC_CLK_DIS | | SC_OVERRIDE | | | | | SC_MST_EN | 0 | |
| 0x04 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | STARTUP2 | | | | | | | STARTUP2[6:0] | | 0 | |
| 0x05 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | STARTUPS | | | | | | | STARTUPS[6:0] | | 0 | |
| 0x06 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | RESERVED | | | | | | | RESERVED | | 0 | |
| 0x07 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | MIC_L | MIC_L_EN | MICBIAS_EN | MICBIAS_SEL[1:0] | MIC_L_MUTE | | MIC_L_VOL[2:0] | | | 0 | |
| 0x08 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | MIC_R | MIC_R_EN | | | MIC_R_MUTE | | MIC_R_VOL[2:0] | | | 0 | |
| 0x09 | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 | - | AUX1_L | AUX1_L_EN | | | | AUX1_L_VOL[6:0] | | | | 10000 | |
| 0x0A | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 | - | AUX1_R | AUX1_R_EN | | | | AUX1_R_VOL[6:0] | | | | 10000 | |
| 0x0B | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | AUX2 | | | | AUX2_EN | AUX2_MUTE | AUX2_VOL[1:0] | | | 0 | |
| 0x0C | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | IN_GAIN | | INPGA_R_VOL[3:0] | | | | INPGA_L_VOL[3:0] | | | 0 | |
| 0x0D | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | INMIX_L | IN_L_EN | | | | | IN_L_SEL[4:0] | | | 0 | |
| 0x0E | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | INMIX_R | IN_R_EN | | | | | IN_R_SEL[6:0] | | | 0 | |
| 0x0F | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 8 | - | ADC_HPF | ADC_VOICE_EN | | ADC_VOICE_F0[2:0] | | ADC_HPF_EN | | ADC_HPF_F0[1:0] | | | 1000 |
| 0x10 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | ADC | ADC_R_EN | ADC_R_MUTE | | | ADC_L_EN | ADC_L_MUTE | | ALC_EN | 0 | |
| 0x11 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | ADC_EQ1_2 | | ADC_EQ2_VOL[8:0] | | | | ADC_EQ1_VOL[8:0] | | | 0 | |
| 0x12 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | ADC_EQ3_4 | | ADC_EQ4_VOL[8:0] | | | | ADC_EQ3_VOL[8:0] | | | 0 | |
| 0x13 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | ADC_EQ5 | ADC_EQ_EN | | ADC_EQ_GAIN[1:0] | | | ADC_EQ5_VOL[8:0] | | | 0 | |
| 0x14 | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 8 | - | DAC_HPF | DAC_VOICE_EN | | DAC_VOICE_F0[2:0] | | DAC_HPF_EN | DAC_MUTE | | DAC_HPF_F0[1:0] | 1000 | |
| 0x15 | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 | - | DAC_L | DAC_L_INV | | | | DAC_L_GAIN[6:0] | | | | 10000 | |
| 0x16 | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 | - | DAC_R | DAC_R_INV | | | | DAC_R_GAIN[6:0] | | | | 10000 | |
| 0x17 | W | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 54 | - | DAC_SEL | DAC_R_EN | | DAC_R_SRC[2:0] | | DAC_L_EN | | DAC_L_SRC[2:0] | | 1010100 | |
| 0x18 | W | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 40 | - | SOFT_MUTE | SOFT_MUTE | RAMP_EN | | | | MUTE_RATE[2:0] | | | 1000000 | |
| 0x19 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | DAC_EQ1_2 | | DAC_EQ2_VOL[8:0] | | | | DAC_EQ1_VOL[8:0] | | | 0 | |
| 0x1A | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | DAC_EQ3_4 | | DAC_EQ4_VOL[8:0] | | | | DAC_EQ3_VOL[8:0] | | | 0 | |
| 0x1B | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | DAC_EQ5 | DAC_EQ_EN | | | | | DAC_EQ5_VOL[8:0] | | | 0 | |
| 0x1C | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | OUTMIX_L | OUT_L_EN | OUT_L_INV | | | | OUT_L_SEL[4:0] | | | 0 | |
| 0x1D | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | OUTMIX_R | OUT_R_EN | OUT_R_INV | | | | OUT_R_SEL[4:0] | | | 0 | |
| 0x1E | W | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 35 | - | OUT1_L | OUT1_L_EN | OUT1_L_SE | | | | OUT1_L_VOL[6:0] | | | 110101 | |
| 0x1F | W | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 35 | - | OUT1_R | OUT1_R_EN | OUT1_R_SE | | | | OUT1_R_VOL[6:0] | | | 110101 | |
| 0x20 | W | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3 | - | OUT2 | OUT2_EN | | OUT2_SEL[8:0] | | | | OUT2_VOL[2:0] | | | 11 | |
| 0x21 | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 10 | - | HP_L_VOL | | HP_L_INV | | | | | HP_L_VOL[6:0] | | | 10000 | |
| 0x22 | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 10 | - | HP_R_VOL | | HP_R_INV | | | | | HP_R_VOL[6:0] | | | 10000 | |
| 0x23 | W | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 | - | HP_CFG | HP_R_EN | HP_MODE | STEREO_TRACK | HP_HIGHZ_R | HP_L_EN | HP_SENSE_EN | HP_2CAP_MODE | HP_HIGHZ_L | | 10 | |
| 0x24 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | ZEROX | HPZX_R_EN | HPZX_L_EN | OUTZX_S_EN | OUTZX_L_EN | INZX_R_EN | INZX_L_EN | A1ZX_R_EN | A1ZX_L_EN | | 0 | |
| 0x25 | W | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 75 | - | DAI_SRC_SEL | DAI_IN_R_MIX | | DAI_OUT_R_SRC[2:0] | | DAI_IN_L_MIX | | DAI_OUT_L_SRC[2:0] | | 1110110 | |
| 0x26 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | DAI_CFG1 | DAI_MODE | | DAI_TDM_MONO | | DAI_FRAME[1:0] | | DAI_WORD[1:0] | | 0 | |
| 0x27 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | DAI_CFG2 | | | DAI_TDM_OFFS[7:0] | | | | | | 0 | |
| 0x28 | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 8 | - | DAI_CFG3 | DAI_EN | | | DAI_OE | DAI_TDM | | DAI_FORMAT[1:0] | | | 1000 | |
| 0x29 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | PLL_DIV1 | | | | | | PLL_DIV_H[19:12] | | | 0 | |
| 0x2A | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | PLL_DIV2 | | | | | | PLL_DIV_M[11:4] | | | 0 | |
| 0x2B | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 | - | PLL_DIV3 | | PLL_BYP | MCLK_RANGE[1:0] | | | | PLL_DIV_L[6:0] | | | 10000 |
| 0x2C | W | 0 | 0 | 0 | 1 | 0 | 1 | 0 | A | - | PLL | PLL_EN | MCLK_SRM_EN | MCLK_DET_EN | MCLK_SHAPE_EN | | | | F0[8:0] | | | 1010 |

Figure 13 Register Map Page 0

To select readback of an individual register click on the R/W bit of the required register and select R. To read the value press the submit button of the same row.

DA7210/11 USER MANUAL

| Register Map Page 0 | | | | | | | | | | | | | |
|---------------------|-----|----|----|----|----|----|----|----|----|-----|--------|----------|---------|
| Register | R/W | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | Hex | Submit | FUNCTION | |
| 0x00 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | PAGE0 | REG_P0 |
| 0x01 | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 | - | CONTROL | WRITE_M |
| 0x02 | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | STATUS | |
| 0x03 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | STARTUP1 | SC_CLK |
| 0x04 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | STARTUP2 | |
| 0x05 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | STARTUP3 | |
| 0x06 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | RESERVED | |
| 0x07 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | MIC_L | MIC_L |
| 0x08 | R | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | MIC_R | MIC_R |
| 0x09 | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 | - | AUX1_L | AUX1_L |
| 0x0A | W | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10 | - | AUX1_R | AUX1_R |
| 0x0B | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | AUX2 | |
| 0x0C | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | IN_GAIN | |
| 0x0D | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | INMIX_L | IN_L |
| 0x0E | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | INMIX_R | IN_R |

Figure 14 Selecting Individual Register Readback

A pop up window will then appear displaying the readback value of the register, Figure 15.

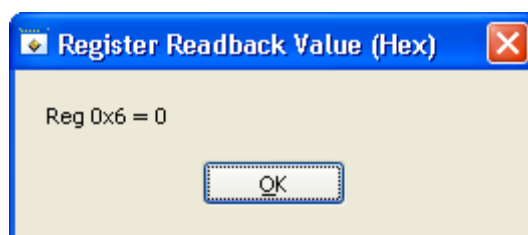


Figure 15 Readback Pop-up Window

To select readback of all Page 0 register simultaneously press the read all button at the base of the R/W column. This will write the register readback values to a spreadsheet file at the following location: *C:\Program Files\Dialog Semiconductor\Audio\DA7210_11 Rev x.x \Page0_Readback_Values.xls*

| Register Map Page 0 | | | | | | | | | | | | | |
|---------------------|-----|----|----|----|----|----|----|----|----|-----|--------|----------|--|
| Register | R/W | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | Hex | Submit | FUNCTION | |
| 0x21 | W | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 35 | - | HP_L | |
| 0x22 | W | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 35 | - | HP_R | |
| 0x23 | W | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | AE | - | HP | |
| 0x24 | W | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | C0 | - | ZER | |
| 0x25 | W | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 76 | - | DAI_SF | |
| 0x26 | W | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 6 | - | DAI | |
| 0x27 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | DAI | |
| 0x28 | W | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 80 | - | DAI | |
| 0x29 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | PLL | |
| 0x2A | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | PLL | |
| 0x2B | W | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 50 | - | PLL | |
| 0x2C | W | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | B | - | P | |

Read All Submit All Reset

Figure 16 Readback All Registers

4.3.3 Register Map Page 1

The page 1 register map panel allows access to single bits or to the hex value of a single register; both can be submitted individually. Readback from Page 1 registers is limited, but individual register readback can be selected in the same way as Page 1 where available.

DA7210/11 USER MANUAL

| Address | W | R | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | FUNCTION | DEFAULT |
|---------|---|---|---|---|---|---|---|---|----|----|--------------------|----------|
| 0x80 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PAGE1 | 0 |
| 0x81 | R | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11 | CHIP_ID | 12001 |
| 0x82 | R | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 2C | INTERFACE | 101100 |
| 0x83 | W | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 40 | ALC_MAX | 1030000 |
| 0x84 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ALC_MIN | 0 |
| 0x85 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ALC_NOIS | 0 |
| 0x86 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ALC_ATT | 0 |
| 0x87 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ALC_REL | 0 |
| 0x88 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ALC_DEL | 0 |
| 0x8A | W | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 8B | A_HD_UNLOCK | 10001011 |
| 0x8B | W | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 84 | A_TST_UNLOCK | 10110100 |
| 0x90 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A_PLL1 | 0 |
| 0x95 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A_ADC0 | 0 |
| 0x96 | W | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 7 | A_DAC0 | 111 |
| 0xA7 | W | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 7E | 0 | A_CP_MODE | 11111110 |
| 0xB7 | W | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | A_B3A ² | 0 |

Figure 17 Register Map Page 1

4.3.4 GP Filters Register Map

The general purpose filters register map panel allows access to the hex value of a single register; all registers are submitted after changes. All registers may also be reset using the *Reset Filters* button.

Filter Coefficients

| | | | | | | | | | | | | | | | |
|----|----------|----|----------|----|----------|----|----------|----|----------|----|----------|----|----------|----|----------|
| 2E | GP1A_A0L | 38 | GP1D_A0L | 42 | GP2A_A1L | 4C | GP2D_A1L | 56 | GP1C_A2L | 60 | GP1B_B1L | 6A | GP2C_B1L | 74 | GP2B_B2L |
| 2F | GP1A_A0H | 39 | GP1D_A0H | 43 | GP2A_A1H | 4D | GP2D_A1H | 57 | GP1C_A2H | 61 | GP1B_B1H | 6B | GP2C_B1H | 75 | GP2B_B2H |
| 30 | GP1B_A0L | 3A | GP2C_A0L | 44 | GP2B_A1L | 4E | GP1A_A2L | 58 | GP1D_A2L | 62 | GP2A_B1L | 6C | GP2D_B1L | 76 | GP1C_B2L |
| 31 | GP1B_A0H | 3B | GP2C_A0H | 45 | GP2B_A1H | 4F | GP1A_A2H | 59 | GP1D_A2H | 63 | GP2A_B1H | 6D | GP2D_B1H | 77 | GP1C_B2H |
| 32 | GP2A_A0L | 3C | GP2D_A0L | 46 | GP1C_A1L | 50 | GP1B_A2L | 5A | GP2C_A2L | 64 | GP2B_B1L | 6E | GP1A_B2L | 78 | GP1D_B2L |
| 33 | GP2A_A0H | 3D | GP2D_A0H | 47 | GP1C_A1H | 51 | GP1B_A2H | 5B | GP2C_A2H | 65 | GP2B_B1H | 6F | GP1A_B2H | 79 | GP1D_B2H |
| 34 | GP2B_A0L | 3E | GP1A_A1L | 48 | GP1D_A1L | 52 | GP2A_A2L | 5C | GP2D_A2L | 66 | GP1C_B1L | 70 | GP1B_B2L | 7A | GP2C_B2L |
| 35 | GP2B_A0H | 3F | GP1A_A1H | 49 | GP1D_A1H | 53 | GP2A_A2H | 5D | GP2D_A2H | 67 | GP1C_B1H | 71 | GP1B_B2H | 7B | GP2C_B2H |
| 36 | GP1C_A0L | 40 | GP1B_A1L | 4A | GP2C_A1L | 54 | GP2B_A2L | 5E | GP1A_B1L | 68 | GP1D_B1L | 72 | GP2A_B2L | 7C | GP2D_B2L |
| 37 | GP1C_A0H | 41 | GP1B_A1H | 4B | GP2C_A1H | 55 | GP2B_A2H | 5F | GP1A_B1H | 69 | GP1D_B1H | 73 | GP2A_B2H | 7D | GP2D_B2H |

FILTER COEFFICIENT REGISTERS

0x2D 0x37 0x41 0x4B 0x55 0x5F 0x69 0x73

0x2E 0x38 0x42 0x4C 0x56 0x60 0x6A 0x74

0x2F 0x39 0x43 0x4D 0x57 0x61 0x6B 0x75

0x30 0x3A 0x44 0x4E 0x58 0x62 0x6C 0x76

0x31 0x3B 0x45 0x4F 0x59 0x63 0x6D 0x77

0x32 0x3C 0x46 0x50 0x5A 0x64 0x6E 0x78

0x33 0x3D 0x47 0x51 0x5B 0x65 0x6F 0x79

0x34 0x3E 0x48 0x52 0x5C 0x66 0x70 0x7A

0x35 0x3F 0x49 0x53 0x5D 0x67 0x71 0x7B

0x36 0x40 0x4A 0x54 0x5E 0x68 0x72 0x7C

Submit Filters Reset Filters GP1AB/2AB - 0x7D GP1CD/2CD - 0x7E GP Enable - 0x7F

Figure 18 Filter Coefficients Set-up Panel

An alternative 'RT Filters' GUI is available that allows easy submission of any of the DAC or ADC filters paths present within the DA7210/11. This is contained on the installation DVD within the distribution kit.

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4.3.5 Volume Control Panel

The *Volume Control* panel allows real time changes to any of the analogue input or output PGAs within the DUT. Muting is also possible where this function exists.

Gain controls are available to the following PGAs:

- AUX_L and AUX_R
- MIC_L and MIC_R
- A2 PGA
- Left and Right Input PGAs
- OUT1_L and OUT1_R
- HPL and HPR
- OUT2

It is possible to change the headphone and OUT1 gain control registers as stereo pairs by simultaneously selecting the *HPL follow HPR* and *OUT1L follow OUT1R* buttons.

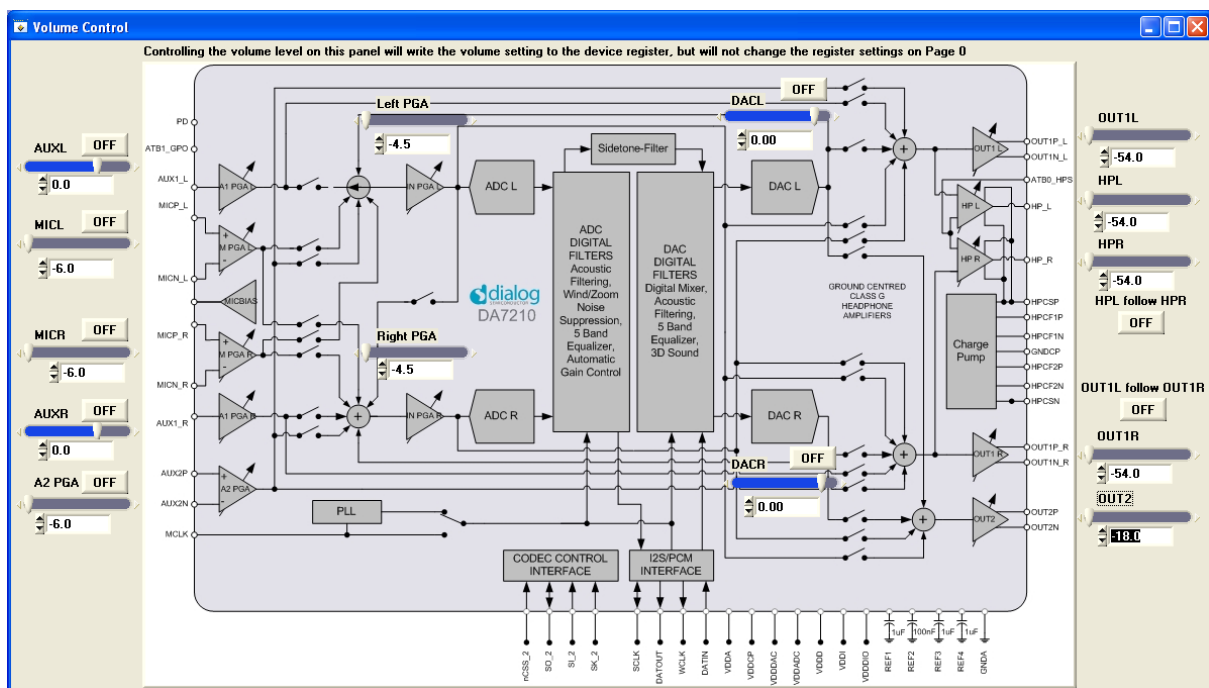


Figure 19 Volume Control Panel

DA7210/11 USER MANUAL

5 RT Filters GUI

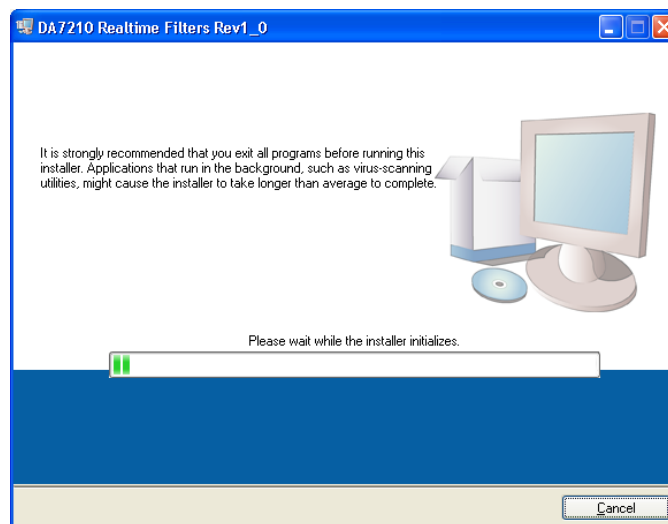
The RT filters GUI allows easy control of all the filter options within the DA7210/11 device through USB control. This includes general purpose filters, five-band equalisers and voice filters for ADC and DAC.

The *Filter Setup* page makes it possible to design the required filter response for all of the general purpose filter bi-quad IIR paths available in the DA7210/11.

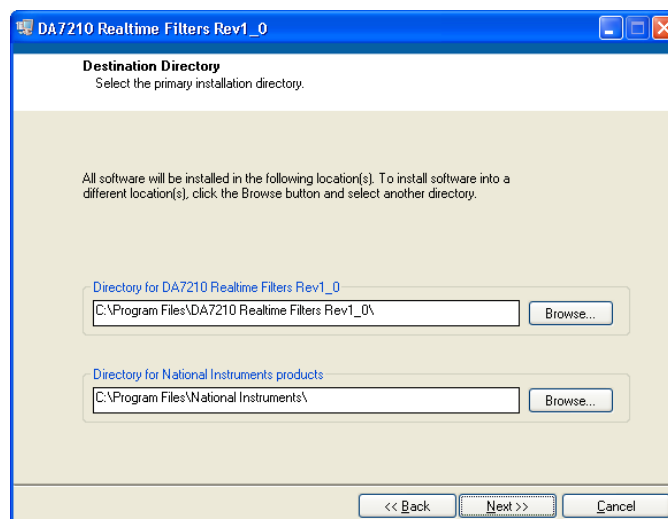
5.1 Software Installation

The set-up file for the RT Filters control software can be found on the accompanying DVD in the folder *DA7210 RT Filters Rev x.x*

Double click *setup.exe* file and the install will begin.

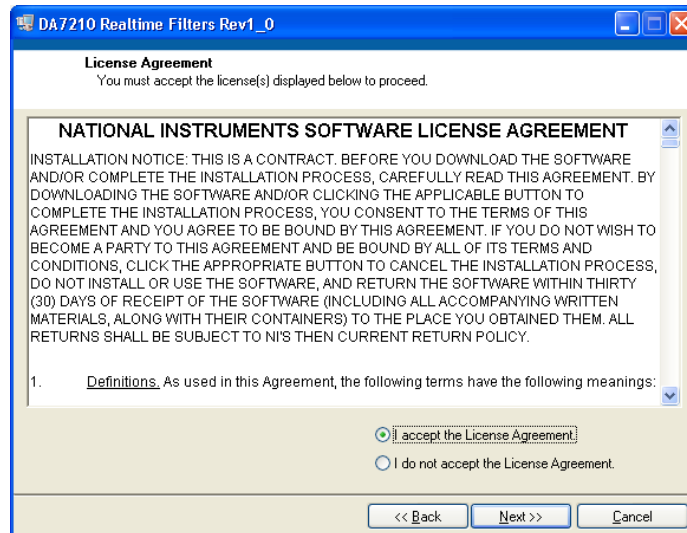


Do not change the installation directory or necessary license files will not be accessible.

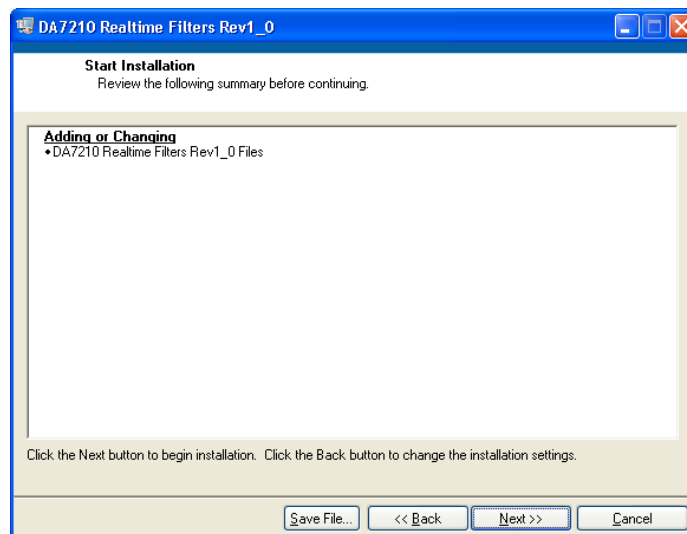


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Select I accept the License Agreement and press Next>>

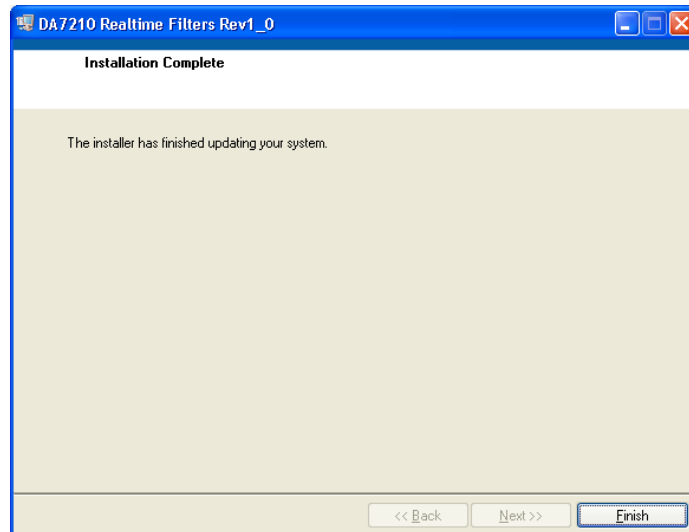


Press Next>>



Allow the application to install. If Labview run-time files have not been installed on the target computer previously, the installation may take a few minutes.

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When installation is complete press *Finish*

5.2 Control Panels

5.2.1 Running the Interface and USB Initialisation

The *RT Filters Rev x.x* GUI can be used in conjunction with the *DA7210_11 Register Control Software Rev x.x* to set up the DA7210/11 device registers. In order to allow both interfaces to access the DA7210/11 simultaneously it is necessary to initialise the *RT Filters* GUI first before opening the *DA7210_11 Register Control Software*.

The flowchart in Figure 20 details the start-up procedure when using the DA7210 Register Control GUI and RT Filter GUI in conjunction with each other.

On starting-up the *RT Filters* application the interface will be running. Once the coefficients are calculated the interface will stop and the registers writes will be submitted to the DA7210/11. To start the interface running again, press the white arrow situated below the *Operate* drop down menu on the top row; this will turn to black and the interface is running again ready for new selections.

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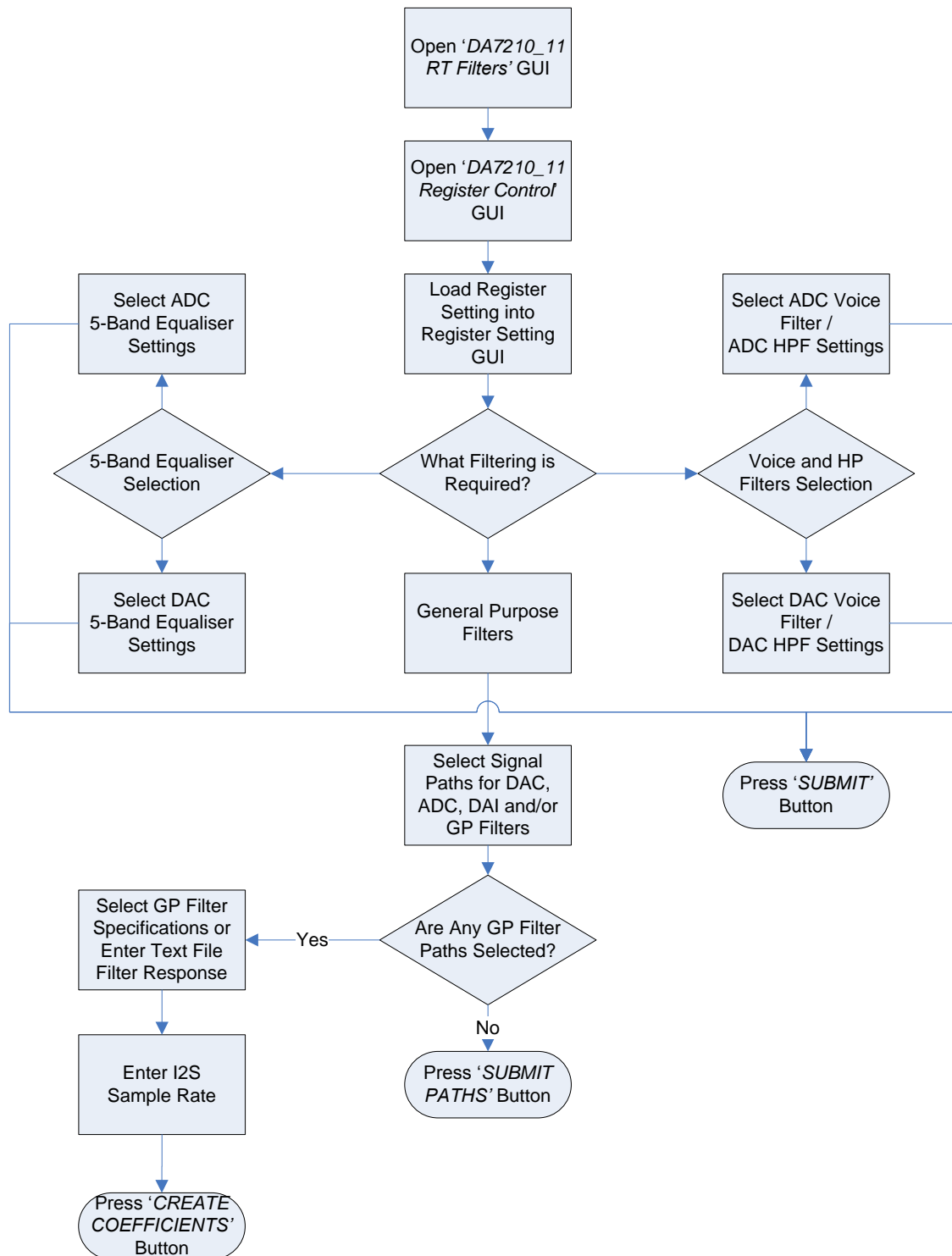


Figure 20 RT Filter Setup Flowchart

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5.3 Filter Setup Panel

The *Filter Setup* panel makes it possible to design desired filter responses through any of the general purpose filter banks, using the filter specification selections.

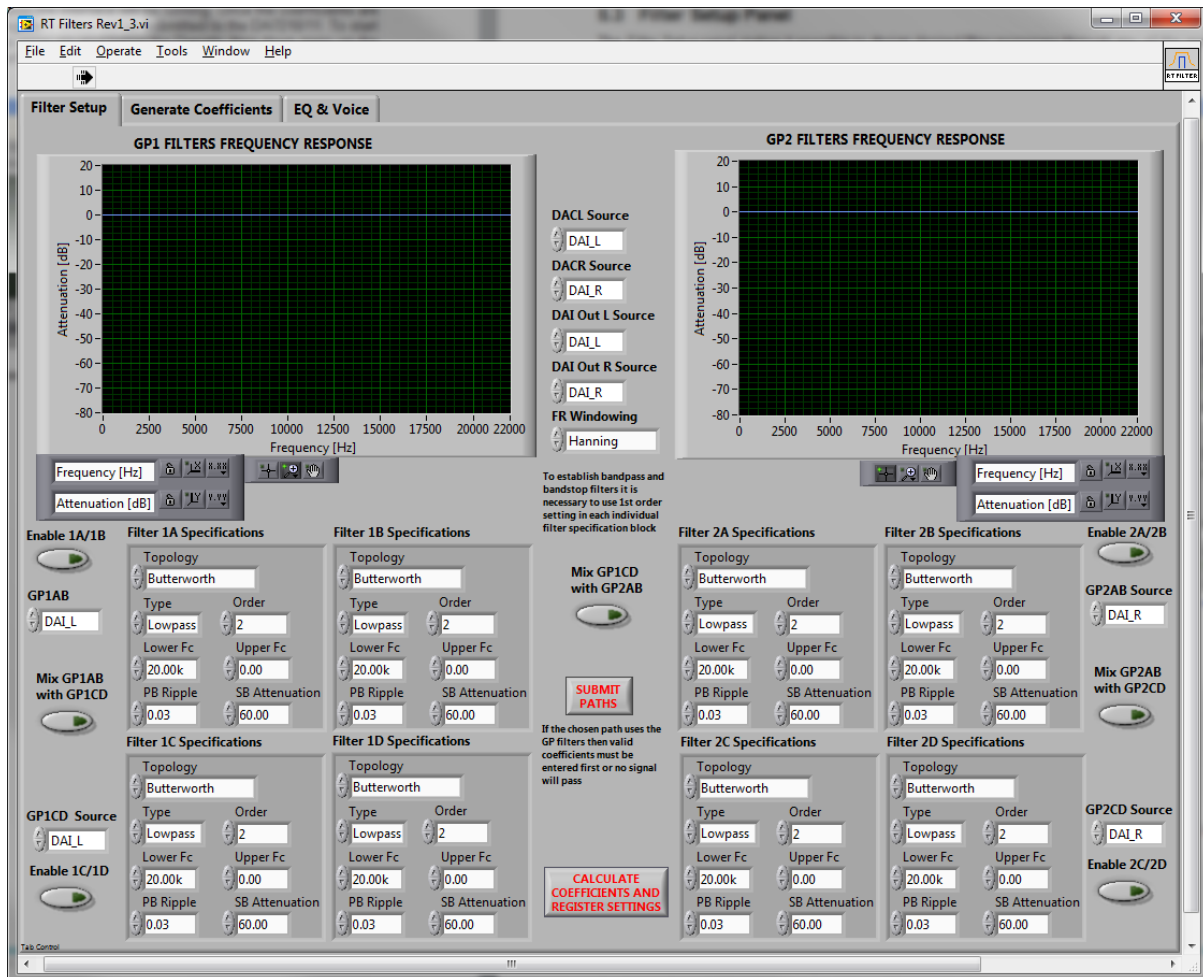


Figure 21 Filter Setup Panel

The *Filter Setup* panel controls the following realtime filter path selections:

- DACL and DACR input sources
- Enabling GP1AB, GP1CD, GP2AB and/or GP2CD
- GP1AB, GP1CD, GP2AB and GP2CD input sources
- Mixing of GP1AB and GP1CD, GP1CD and GP1CD or GP2AB and GP2CD

For each of the filter specifications blocks the following settings are available:

- Topology – Butterworth, Chebyshev, Inverse Chebyshev, Elliptic, Bessel
- Type – lowpass, highpass, bandpass, bandstop
- Order – order 2 should be used lowpass and highpass filters and order 1 for bandpass and bandstop filters only
- Lower Fc – lower frequency cut-off
- Upper Fc – upper frequency cut-off
- PB Ripple – passband ripple level
- SB attenuation – sideband attenuation level

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Pressing the *Submit Paths* button allows real-time selection of the filter path set-up while the interface is running.

The resultant coefficients from the selected filter responses can be calculated and submitted to the DA7210/11 by pressing the *Calculate Coefficients and Register Settings* button. The coefficients sent to the DA7210/11 are displayed on the *Coefficients* panel.

Important: Be aware that if any of the general purpose filter paths are selected and no coefficients have been entered, then the DA7210/11 will be unable to pass the signal to the selected output.

5.4 Coefficients Tab

The *Generate Coefficients* panel displays the forward and reverse coefficients for all of the general purpose filters and lists the register writes submitted to the DA7210/11. Here it is also necessary to enter the sample rate of the digital audio interface, so that the correct coefficient values are created; failure to do so will result either in zero entries or incorrect coefficient values.

The *Calculate Coefficients and Register Settings* button will perform the same action as the button of the same name on the *Filter Setup* panel.

The forward and reverse coefficients can be saved to file by selecting *Output Coefficients* button and by selecting a valid output file path. The spreadsheet file must already exist for the register values to be output.

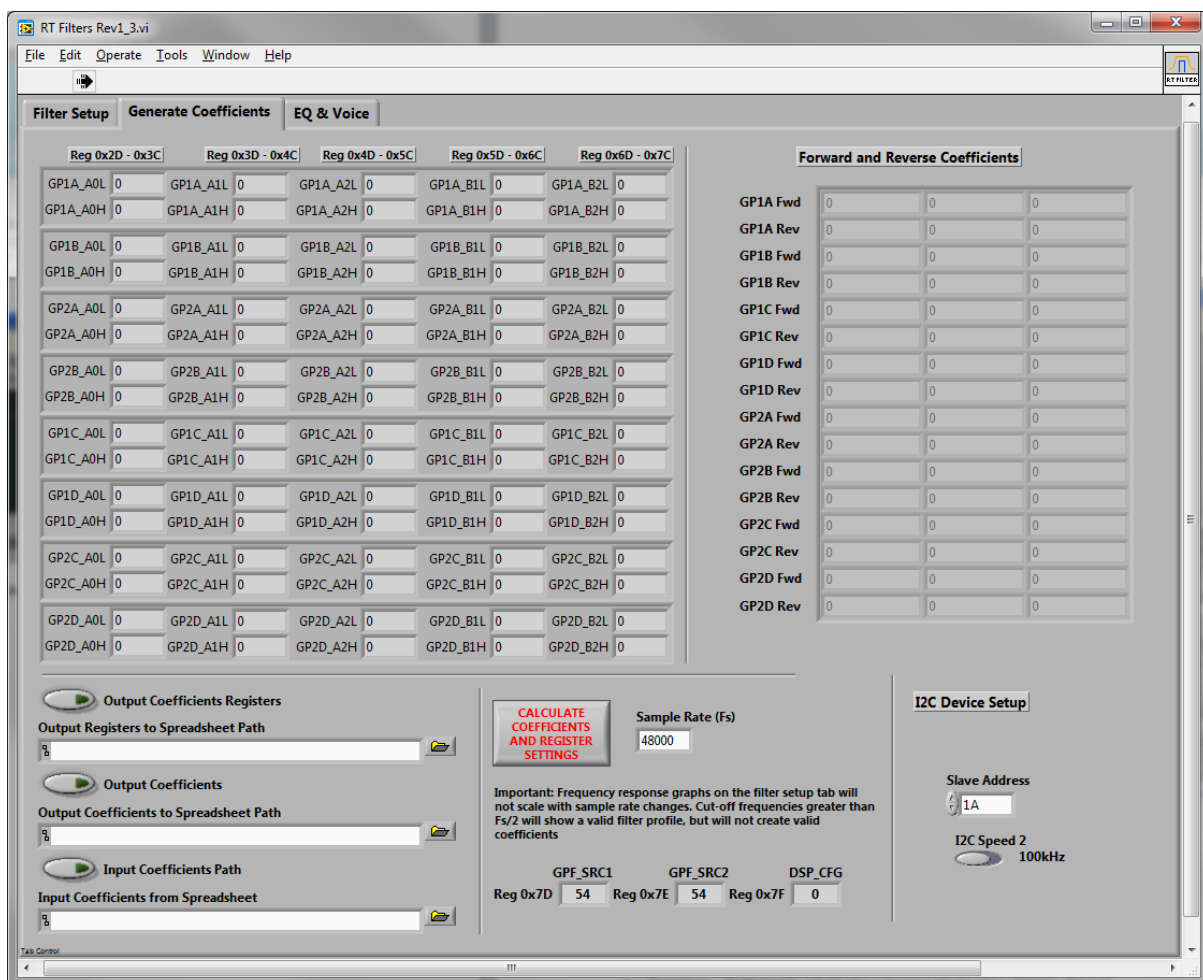
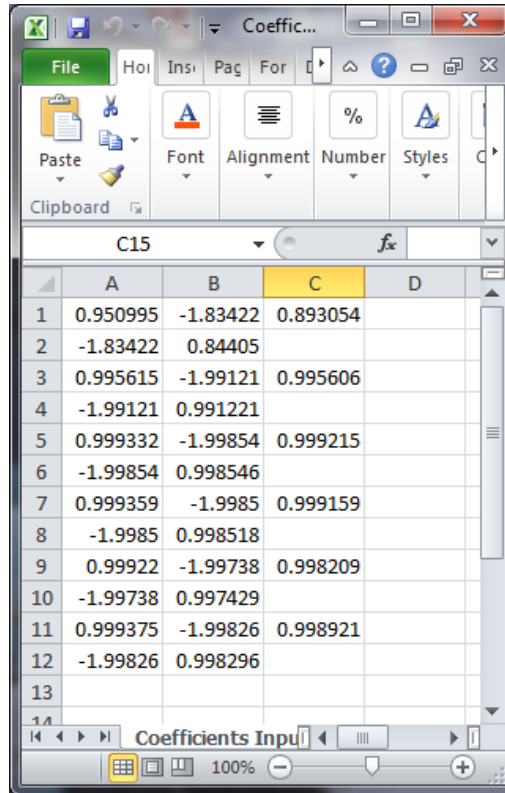


Figure 22 Coefficients Panel

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It is also possible to input coefficients to the device from spreadsheet by selecting *Input Coefficients* button and by selecting a valid input file path. Three forward and two reverse coefficients are required, an example is found in Figure 23.



| | A | B | C | D |
|----|----------|----------|----------|---|
| 1 | 0.950995 | -1.83422 | 0.893054 | |
| 2 | -1.83422 | 0.84405 | | |
| 3 | 0.995615 | -1.99121 | 0.995606 | |
| 4 | -1.99121 | 0.991221 | | |
| 5 | 0.999332 | -1.99854 | 0.999215 | |
| 6 | -1.99854 | 0.998546 | | |
| 7 | 0.999359 | -1.9985 | 0.999159 | |
| 8 | -1.9985 | 0.998518 | | |
| 9 | 0.99922 | -1.99738 | 0.998209 | |
| 10 | -1.99738 | 0.997429 | | |
| 11 | 0.999375 | -1.99826 | 0.998921 | |
| 12 | -1.99826 | 0.998296 | | |
| 13 | | | | |
| 14 | | | | |

Figure 23 Input Coefficient Spreadsheet Example

Another facility on the *Generate Coefficients* panel allows the register values to be output to spreadsheet by selecting the *Output Coefficient Registers* button and by selecting a valid output file path. The spreadsheet file must already exist for the register values to be output.

The I2C device address and access speed can also be entered here.

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5.5 Five-band Equaliser and Voice Filter Panel

The *EQ & Voice* panel contains the controls for selection of the ADC and DAC five-band equalisers and for the voice filters. These registers can be submitted real-time while the interface is running by pressing the *Submit* button.

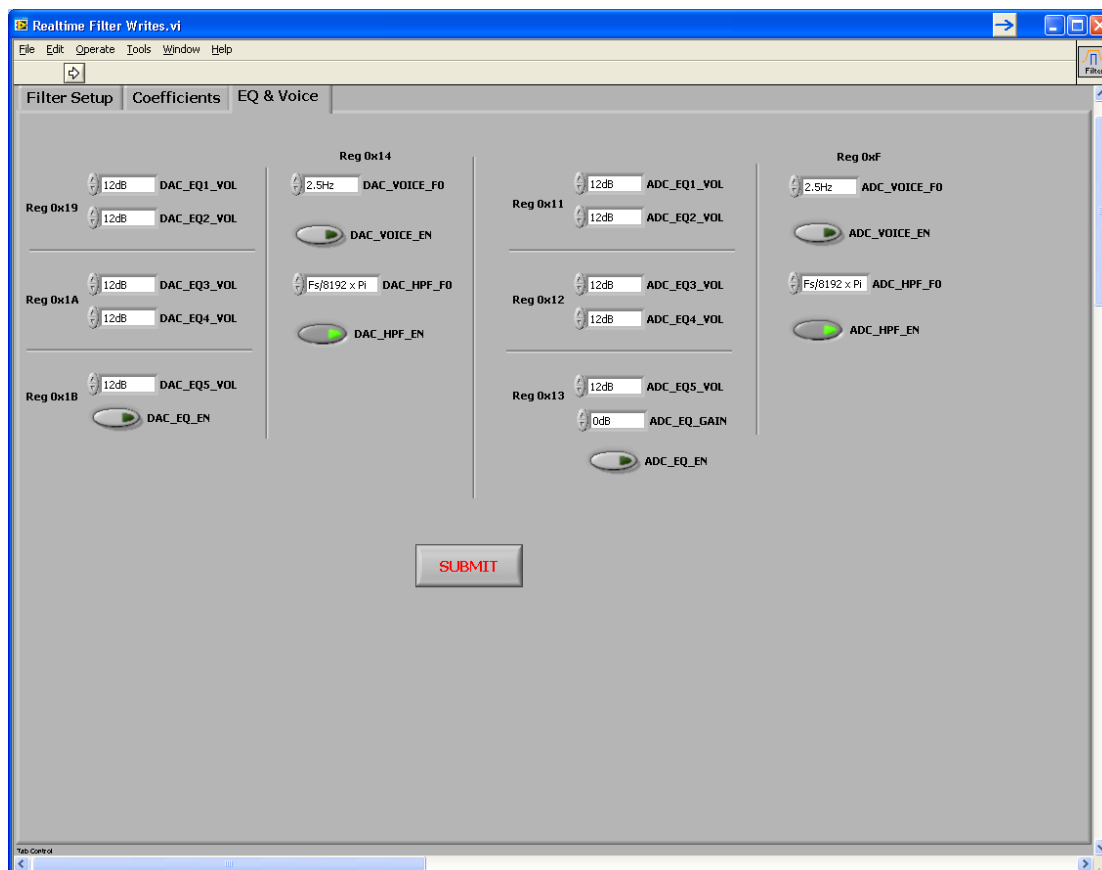


Figure 24 Five-band Equaliser and Voice Filter Panel