System PMIC for Mobile and Automotive Applications

General Description

DA9063 is a high current system PMIC suitable for dual- and quad-core processors used in smartphones, tablets, ultra-books, and other handheld and automotive applications that require up to 5 A core processor supply.

DA9063 contains six DC-DC buck converters designed for small external 1 µH inductors capable of supplying in total up to 12 A continuous output (0.3 V to 3.3 V). The buck converters do not require external Schottky diodes. They dynamically optimize their efficiency depending on the load current using an Automatic Sleep mode. The bucks incorporate pin and s/w controlled Dynamic Voltage Control (DVC) to support processor load adaptive adjustment of the supply voltage. One buck can also be used in a DDR memory termination mode.

Eleven SmartMirror™ programmable LDO regulators are incorporated, rated up to 300 mA. All support remote capacitor placement and can support operation from a low 1.5 V/1.8 V input voltage: this allows the linear regulators to be cascaded with a suitable buck supply to improve overall system efficiency.

Processor core leakage can be minimized by using the integrated rail switch controller for ultra-fast power domain isolation/reconnection while current limited switches provide support for external peripherals such as external accessory or memory cards.

There are five distinct operating modes consuming < 20 µA including a 1.5 µA RTC mode with alarm and wake-up. A system monitor watchdog can be enabled in ACTIVE mode.

The DA9063 provides an OTP start-up sequencing engine that offers autonomous hardware system start-up or software controlled start-up and configurable power modes. The on key detects the button press time and offers configurable key lock and application shutdown functions. Up to 16 freely configurable GPIO pins can perform system functions, including: keypad supervision, application wake-up, and timing controlled external regulator, power switch, or other IC enable.

An integrated 10-channel ADC includes advanced voltage monitoring, internal temperature supervision, three general-purpose channels with programmable high/low thresholds, an integrated current source for resistive measurements, and system voltage monitoring with a programmable low-voltage warning. The ADC has 8-bit resolution in AUTO mode and 10-bit resolution in manual conversion mode.

Three RGB-LED driver pins are provided with PWM control.

LDO8 can be configured as a 6-bit, PWM-controlled, vibration motor driver with automatic battery voltage correction.

System PMIC for Mobile and Automotive Applications

Key Features

- 6 DC-DC buck converters with DVC
  - 2.5 A BuckCore1 ┐ 5 A in dual phase mode
  - 2.5 A BuckCore2 ┘
  - 2.5 A BuckPro
  - 1.5 A BuckPeri
  - 1.5 A BuckMem ┐ 3 A in merged mode
  - 1.5 A BuckIO ┘
- 3 MHz switching frequency (±10 %) (allows use of low profile [1 mm] 1 µH inductors)
- 11 programmable LDO regulators:
  - 3 low noise, 4 with DVC, 5 with current limited switch mode
- Two rail switches
- Power Manager with programmable regulators, rail switch start-up, and configurable low power modes
- Multiple master application support via two independent control interfaces
- System monitor with watchdog timer
- Up to 16 flexible GPIO pins for enhanced wake-up and peripheral control
- RGB-LED driver with autonomous flashing
- PWM vibration motor driver
- 10-bit ADC with nine channels and configurable alarm thresholds
- Regulator supervision with automatic under-/over-voltage protection
- Coin cell/super-capacitor backup charger
- Ultra-low power, 1.5 µA RTC with alarm and oscillator circuitry with crystal frequency adjustment
- -40 °C to +125 °C junction temperature operation
- Two package variants:
  - 100 VFBGA 8.0 mm x 8.0 mm x 1.0 mm, 0.8 mm pitch, 0.30 mm balls
  - 100 TFBGA 8.0 mm x 8.0 mm x 1.2 mm 0.8 mm pitch, 0.45 mm balls
- Automotive AEC-Q100 Grade 2 available (DA9063-A)

Applications

- Smartphones
- Ultrabooks
- Tablets, e-books
- Car infotainment and ADAS
- Navigation devices
- Set-top boxes, TV, and media players
- Portable industrial and medical devices
- IoT devices

Contents

1 References

Dialog Semiconductor technical documentation is available on the web site:
Power Management ICs (PMICs).

[1] AN-PM-068, Application Note, VBBAT Current in RTC or DELIVERY Modes, Dialog Semiconductor.

[2] AN-PM-024, Application Note, DA9063 Voltage Monitoring, Dialog Semiconductor.

[3] AN-PM-010, Application Note, PCB Layout Guidelines, Dialog Semiconductor.

2 Block Diagram

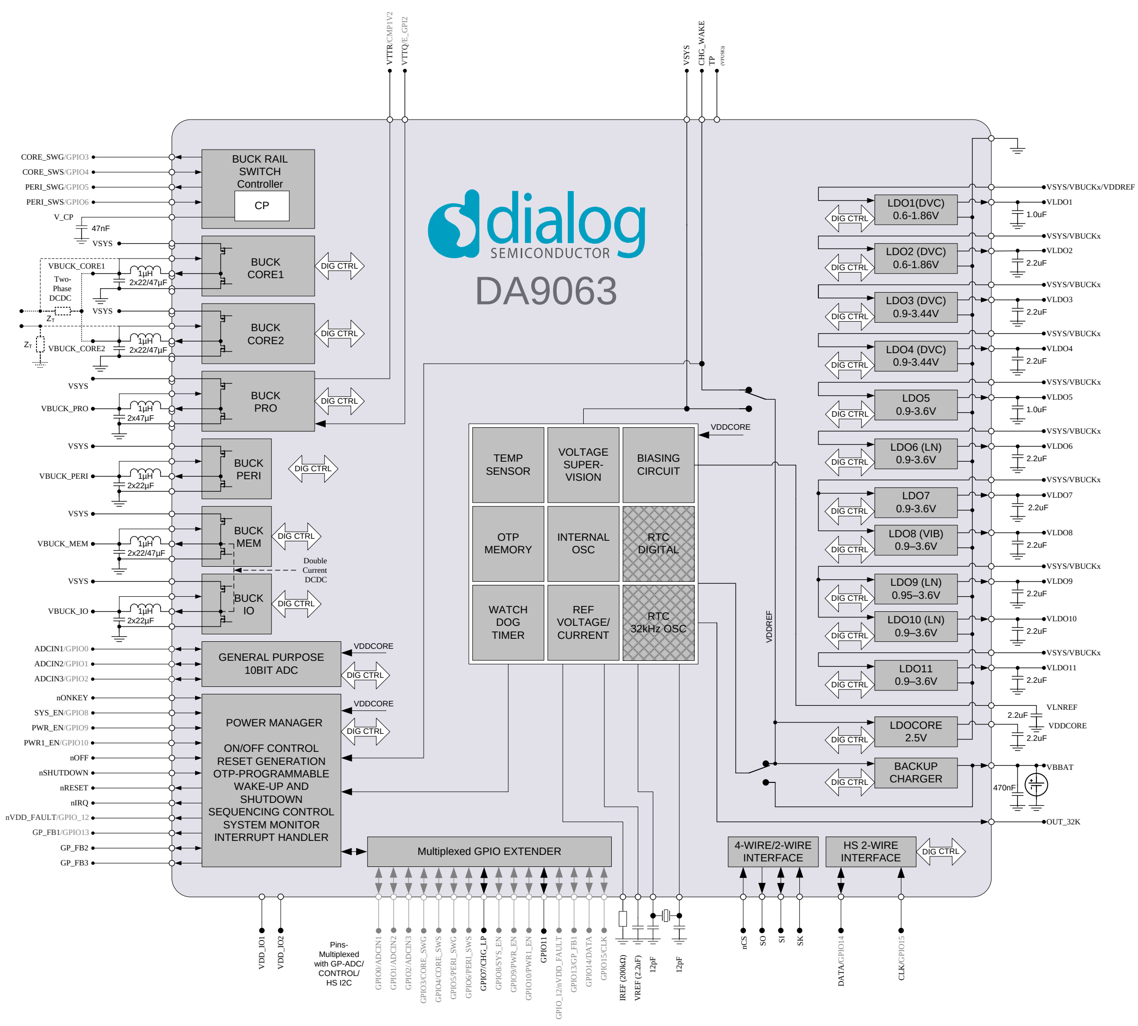


Figure 1: Block Diagram

3 Pinout

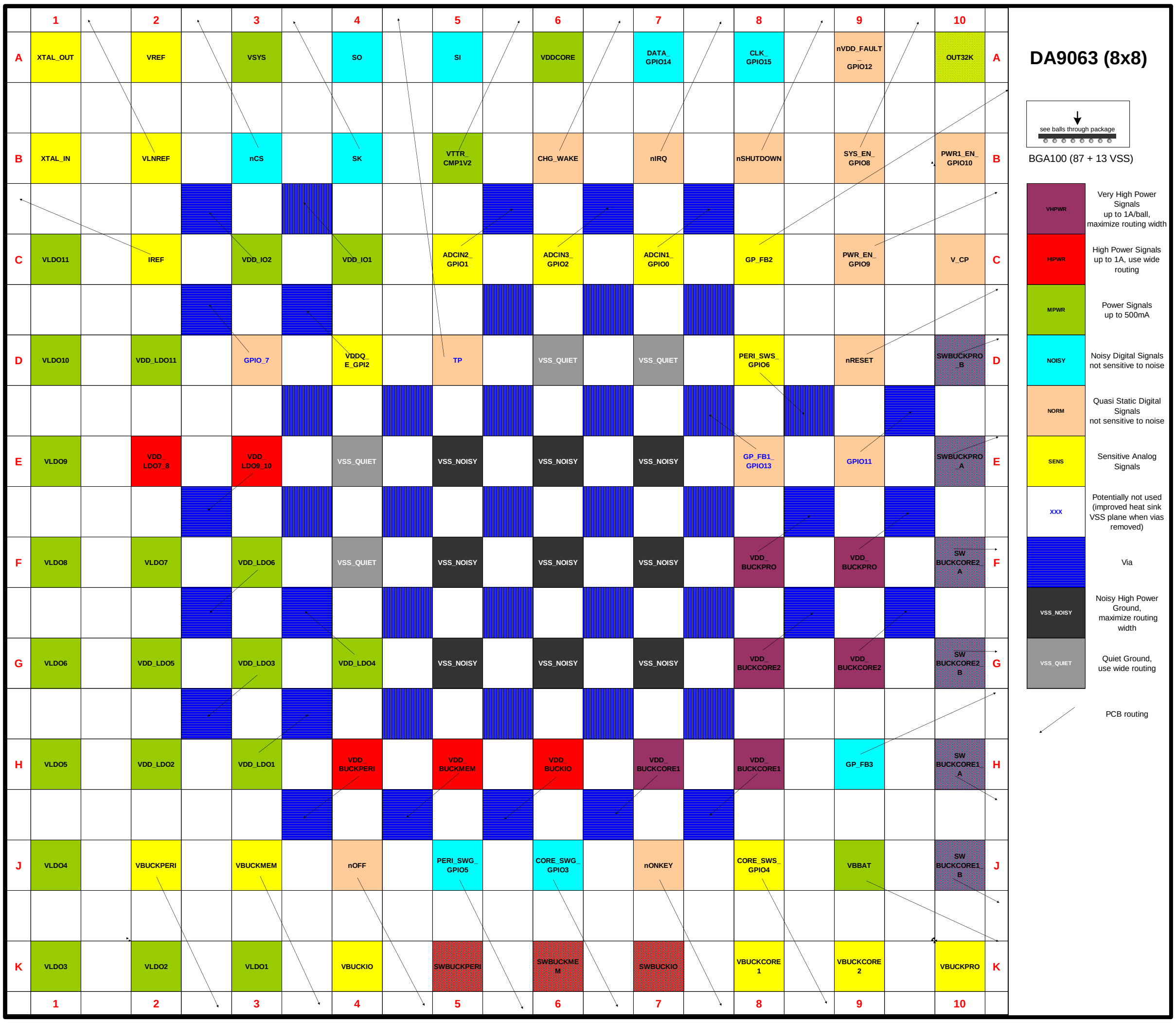


Figure 2: Connection Diagram

Table 1: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital input	AI	Analog input
DO	Digital output	AO	Analog output
DIO	Digital input/output	AIO	Analog input/output
PWR	Power supply	GND	Ground connection

Table 2: Pin Description

Pin	Pin Name	Alternate Function	Type (Table 1)	Description
Power Manager				
A9	nVDD_FAULT	GPIO12	DO/DIO	Indication for low supply voltage / GPIO12 / VDD_MON controlled GPO
B6	CHG_WAKE		DI/PWR	Wake-up signal from companion charger to trigger a start-up and temporary supply voltage for PMIC (VBUS_PROT in case of an inserted supply until charger Buck provides power to V_{SYS}). Connect to GND if not used.
B7	nIRQ		DO	IRQ line for host
B8	nSHUTDOWN		DI	Active-low input from switch or host to initiate shutdown
B9	SYS_EN	GPIO8	DI/DIO	Hardware enable of power domain SYSTEM/GPIO8
B10	PWR1_EN	GPIO10	DI/DIO	Hardware enable of power domain POWER1/GPIO10 with high power output / input for power sequencer WAIT ID
C3	VDD_IO2		PWR	Alternate supply I/O voltage
C4	VDD_IO1		PWR	First supply I/O voltage rail
C8	GP_FB2		DO/DI	PWR_OK status indicator: all supervised regulators are in-range / HW input for watchdog supervision / dual-phase BUCKCORE voltage sense at output capacitor
C9	PWR_EN	GPIO9	DI/DIO	Hardware enable of power domain power / sequencer controlled GPO
D3	GPIO7		DIO	Sequencer controlled GPO
D5	TP		DIO	Test pin: enables power commander boot mode and supply pin for OTP fusing voltage
D9	nRESET		DO	Active low reset for host
E8	GP_FB1	GPIO13	DO/DIO	Status indication for host of a valid wake-up event (EXT_WAKEUP) / indicator for on-going power mode transition (READY) / GPIO13, regulator HW control
E9	GPIO11		DIO	GPIO11 with high power output and blinking feature
H9	GP_FB3		DO/DO	Second 32 kHz oscillator output: OUT32_2 / VIB_BREAK control signal for vibration motor driver (LDO8)
J4	nOFF		DI	Active-low input from error indication line to initiate fast emergency shutdown
J7	nONKEY		DI	On/off key with optional long press shutdown

Pin	Pin Name	Alternate Function	Type (Table 1)	Description
4-Wire/2-Wire Interfaces				
A4	SO		DO	4-wire data output
A5	SI		DIO	4-wire data input / 2-wire data
A7	DATA	GPIO14	DIO	HS-2-WIRE data / GPIO14 (optional reset if long press in parallel with GPI15) with high power output and blinking feature
A8	CLK	GPIO15	DI	HS-2-WIRE clock / GPIO15 (optional reset if long press in parallel with GPI14) with high power output and blinking feature
B3	nCS		DI	4-wire (active low) chip select
B4	SK		DI	4-wire/2-wire clock
Voltage Regulators				
A3	VSYS		PWR	Supply voltage for PMIC and input for voltage supervision (decouple with 1.0 µF)
A6	VDDCORE		AO	Regulated supply for internal circuitry (2.2 V/2.5 V) (decouple with 2.2 µF)
C1	VLDO11		AO	Output voltage from LDO11
D1	VLDO10		AO	Output voltage from LDO10
D2	VDD_LDO11		PWR	Supply voltage for LDO11
E1	VLDO9		AO	Output voltage from LDO9
E2	VDD_LDO7_8		PWR	Supply voltage for LDO7 and LDO8
E3	VDD_LDO9_10		PWR	Supply voltage for LDO9 and LDO10
F1	VLDO8		AO	Output voltage from LDO8
F2	VLDO7		AO	Output voltage from LDO7
F3	VDD_LDO6		PWR	Supply voltage for LDO6
G1	VLDO6		AO	Output voltage from LDO6
G2	VDD_LDO5		PWR	Supply voltage for LDO5
G3	VDD_LDO3		PWR	Supply voltage for LDO3
G4	VDD_LDO4		PWR	Supply voltage for LDO4
H1	VLDO5		AO	Output voltage from LDO5
H2	VDD_LDO2		PWR	Supply voltage for LDO2
H3	VDD_LDO1		PWR	Supply voltage for LDO1
J1	VLDO4		AO	Output voltage from LDO4
K1	VLDO3		AO	Output voltage from LDO3
K2	VLDO2		AO	Output voltage from LDO2
K3	VLDO1		AO	Output voltage from LDO1

Pin	Pin Name	Alternate Function	Type (Table 1)	Description
DC/DC Buck Converters				
A1	XTAL_OUT		AIO	32 kHz crystal connection (adjust with 10 pF)
A2	VREF		AIO	Filter node for internal reference voltage (decouple with 0.22 µF)
A10	OUT_32K		DO	32 kHz oscillator buffer
B1	XTAL_IN		AIO	32 kHz crystal connection (adjust with 10 pF)
B2	VLNREF			Filter node for LN (low noise) (decouple with 0.22 µF)
B5	VTTR	CMP1V2	AO/DO	Memory bus termination reference voltage (50 % of VDDQ), COMP1V2 controlled GPO
C2	IREF		AO	Connection for bias setting (configure with high precision 200 kΩ resistor)
C5	ADCIN2	GPIO1	AI/DIO	Connection to GPADC channel 2 with 1.2 V HW comparator IRQ/GPIO1, regulator HW control
C6	ADCIN3	GPIO2	AI/DIO	Connection to GPADC channel 3/GPIO2, regulator HW control
C7	ADCIN1	GPIO0	AI/DIO	Connection to GPADC auto channel 1 with threshold IRQ and resistor measurement option/GPIO0
C10	V_CP		AIO	Charge pump output bypass (decouple with 10 nF)
D4	VDDQ	E_GPI2	AI/DO	BUCKPRO target voltage sense port / state of E_GPI2 controlled GPO
D8	PERI_SWS	GPIO6	AI/DO	BUCKPERI sense node from rail switch output/ GPIO6 Pulled down when switch is open
D10	SWBUCKPRO_B		AO	Switching node for BUCKPRO (full-current)
E10	SWBUCKPRO_A		AO	Switching node for BUCKPRO (half-current)
F8, F9	VDD_BUCKPRO		PWR	Supply voltage for buck To be connected to VSYS
F10	SWBUCKCORE2_A		AO	Switching node for BUCKCORE2 (half-current)
G8, G9	VDD_BUCKCORE2		PWR	Supply voltage for buck To be connected to VSYS
G10	SWBUCKCORE2_B		AO	Switching node for BUCKCORE2 (full-current)
H4	VDD_BUCKPERI		PWR	Supply voltage for buck To be connected to VSYS
H5	VDD_BUCKMEM		PWR	Supply voltage for buck To be connected to VSYS

Pin	Pin Name	Alternate Function	Type (Table 1)	Description
H6	VDD_BUCKIO		PWR	Supply voltage for buck To be connected to VSYS
H7, H8	VDD_BUCKCORE1		PWR	Supply voltage for buck To be connected to VSYS
H10	SWBUCKCORE1_A		AO	Switching node for BUCKCORE1 (half-current)
J2	VBUCKPERI		AI	Sense node for BUCKPERI
J3	VBUCKMEM		AI	Sense node for DC/DC BUCKMEM
J5	PERI_SWG	GPIO5	AIO/DIO	NMOS gate driver for buck rail switch/GPIO5
J6	CORE_SWG	GPIO3	AIO/DIO	NMOS gate driver for buck rail switch/GPIO3
J8	CORE_SWS	GPIO4	AI/DO	BUCKCORE sense node from rail switch output or output capacitor of dual-phase BUCKCORE/ connection of internal switch to the output of LDO1/GPIO4 Pulled down when switch is open
J10	SWBUCKCORE1_B		AO	Switching node for BUCKCORE1 (full-current)
K4	VBUCKIO		AI	Sense node for BUCKIO
K5	SWBUCKPERI		AO	Switching node for BUCKPERI
K6	SWBUCKMEM		AO	Switching node for BUCKMEM
K7	SWBUCKIO		AO	Switching node for BUCKIO To be connected to SWBUCKMEM for buck merge
K8	VBUCKCORE1		AI	Sense node for BUCKCORE1
K9	VBUCKCORE2		AI	Sense node for BUCKCORE2
K10	VBUCKPRO		AI	Sense node for BUCKPRO
Backup Battery Charger				
J9	VBBAT		AIO	Backup battery connection Coin-cell or super-cap (decouple with 470 nF)
Vss				
D6-7, E4, F4	GND		GND	VSS_LDO, VSS_ADC, VSS_CORE, VSUB
E5-7, F5-7, G5-7	GND		GND	VSS_BUCKCORE1_A, VSS_BUCKCORE1_B, VSS_BUCKCORE2_A, VSS_BUCKCORE2_B, VSS_BUCK_PRO_A, VSS_BUCK_PRO_B, VSS_BUCK_IO, VSS_BUCK_MEM, VSS_BUCK_PERI

4 Regulator Overview

Table 3: Regulators

Regulator	Supplied Pins	Supplied Voltage (V)	Supplied Max. Current (mA)	External Component	Notes
BUCKCORE1	VBUCKCORE1	0.3 to 1.57	1250/ 2500 (full-current mode) Note 1	1.0 µH/ 44 µF / 88 µF	• GPIO and host interface-controlled DVC with variable slew rate (10 mV in [0.5, 1.0, 2.0, 4.0] µs) • 10 mV steps • < 0.7 V PFM mode only • 2500 mA in full-current mode (double pass device and current limit) • Provides dual-phase buck with up to 5 A if combined with BUCKCORE2
BUCKCORE2	VBUCKCORE2	0.3 to 1.57	1250/ 2500 (full-current mode) Note 1	1.0 µH/ 44/88 µF	• GPIO and host interface-controlled DVC with variable slew rate (10 mV in [0.5/1.0/2.0/4.0] µs) • 10 mV steps • < 0.7 V PFM mode only • 2500 mA in full-current mode (double pass device and current limit) • Provides dual-phase Buck if combined with BUCKCORE1
BUCKPRO	VBUCKPRO	0.53 to 1.80	1250/ 2500 (full-current mode) Note 1	1.0 µH/ 44/88 µF	• GPIO and host interface-controlled DVC with variable slew rate, (10 mV in [0.5/1.0/2.0/4.0] µs) • 10 mV steps and VTT regulator mode • < 0.7 V PFM mode only • 2500 mA in full-current mode (double pass device and current limit)
BUCKMEM	VBUCKMEM	0.8 to 3.34	1500 Note 1	1.0 µH/ 44 µF	• GPIO and host interface-controlled DVC with variable slew rate (10 mV in [0.5/1.0/2.0/4.0] µs) • 20 mV steps • Can be merged with BUCK_IO towards single buck with up to 3 A output current

Regulator	Supplied Pins	Supplied Voltage (V)	Supplied Max. Current (mA)	External Component	Notes
BUCKIO	VBUCKIO	0.8 to 3.34	1500 Note 1	1.0 µH/ 44 µF	• GPIO and host interface-controlled DVC with variable slew rate (10 mV in [0.5/1.0/2.0/4.0] µs) • 20 mV steps, can be merged with BUCK_MEM
BUCKPERI	VBUCKPERI	0.8 to 3.34	1500 Note 1	1.0 µH/ 44 µF	• GPIO and host interface-controlled DVC with variable slew rate (10 mV in [0.5/1.0/2.0/4.0] µs) • 20 mV steps
LDO1	VLDO1	0.6 to 1.86	100	1.0 µF	• GPIO and host interface-controlled DVC with variable slew rate (10 mV in [0.5/1.0/2.0/4.0] µs) • 20 mV steps • Optional voltage tracking of BUCKCORE or BUCKPRO
LDO2	VLDO2	0.6 to 1.86	200	2.2 µF	• GPIO and host interface-controlled DVC with variable slew rate (10 mV in [0.5/1.0/2.0/4.0] µs) • 20 mV steps
LDO3	VLDO3	0.9 to 3.44	200	2.2 µF	• Bypass mode • GPIO and host interface-controlled DVC with variable slew rate (10 mV in [0.5/1.0/2.0/4.0] µs) • 20 mV steps
LDO4	VLDO4	0.9 to 3.44	200	2.2 µF	• Bypass mode • GPIO and host interface-controlled DVC with variable slew rate (10 mV in [0.5/1.0/2.0/4.0] µs) • 20 mV steps
LDO5	VLDO5	0.9 to 3.6	100	1.0 µF	50 mV steps
LDO6	VLDO6	0.9 to 3.6	200	2.2 µF	• Low noise • 50 mV steps
LDO7	VLDO7	0.9 to 3.6	200	2.2 µF	• Bypass mode • 50 mV steps • Common supply with LDO8

Regulator	Supplied Pins	Supplied Voltage (V)	Supplied Max. Current (mA)	External Component	Notes
LDO8	VLDO8	0.9 to 3.6	200	2.2 µF	• Bypass and switching vibration motor driver mode • 50 mV steps • Common supply with LDO7
LDO9	VLDO9	0.95 to 3.6	200	2.2 µF	• Low noise • 50 mV steps • OTP trimmed • Common supply with LDO10
LDO10	VLDO10	0.9 to 3.6	300	2.2 µF	• Low noise LDO • 50 mV steps • Common supply with LDO9
LDO11	VLDO11	0.9 to 3.6	300	2.2 µF	• Bypass mode • 50 mV steps
BACKUP	VBBAT	1.1 to 3.1	6	470 nF	• 100/200 mV steps • Configurable charge current between 100 µA and 6000 µA • Reverse current protection (RCP)
LDOCORE	Internal PMIC supply	2.5 ± 2 % accuracy	4	2.2 µF	• Internal LDO • OTP trimmed

Note 1 For short durations to meet peak current requirements I_{OUT} can be operated at up to 20 % higher than the specified maximum operating condition. The part should not be operated in this mode for extended periods and is not guaranteed for continuous operation.

5 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 4 lists the absolute maximum ratings of the device. Exceeding these ratings may cause permanent damage to the device. Device functionality is only guaranteed under the conditions listed in Sections 5.1 and 5.2. Operating the device in conditions exceeding those listed in Table 5 but compliant with the absolute maximum ratings listed in Table 4, for extended periods of time may affect device reliability.

Table 4: Absolute Maximum Ratings

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_{STG}	Storage temperature		-65		+150	°C
T_J	Junction temperature	Note 2	-40		+150	°C
V_{SYS}, V_{CHG_WAKE}	Supply voltage		-0.3		6.0	V
V_{BBAT}			-0.3		3.25	V
V_{TP}		Note 4	-0.3		8.0	V
All other pins		Note 3	-0.3		V_{DDREF} + 0.3	V
V_{ESD_HBM}	ESD protection - Human Body Model (HBM)		2000			V
V_{ESD_CDM}	ESD protection - Charged Device Model (CDM)	Corner pins	750			V
		All other pins	500			

Note 2 See Section 5.16 and Section 6.17.

Note 3 Maximum 6.0 V. An internal node V_{DDREF} is defined as the higher rail of CHG_WAKE and VSYS.

Note 4 Voltage on TP pin should be 0 V except during in-circuit programming.

5.2 Recommended Operating Conditions

All voltages are referenced to VSS unless otherwise stated. Currents flowing into DA9063 are deemed positive; currents flowing out are deemed negative. All parameters are valid over the recommended temperature range and power supply range unless otherwise stated. Please note that the power dissipation must be limited to avoid overheating of DA9063.

Table 5: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_J	Junction temperature		-40		+125	°C
V_{SYS}, V_{CHG_WAKE}	Supply voltage		0		5.5	V
V_{BBAT}	Backup supply voltage		0		3.15	V
$V_{DD\_IO1/2}$	Supply voltage IO	Note 1	1.2		3.6	V
V_{TP}	TP programming supply	Note 5	7.25	7.5	7.75	V
I_{OUT}	BUCKCORE1, BUCKCORE2, BUCKPRO	Note 2			2500	mA
I_{OUT}	BUCKMEM, BUCKIO, BUCKPERI	Note 2			1500	mA
R_{θ_JA}	Thermal resistance junction to ambient	100 VFBGA package Note 3		27.7		°C/W
		100 TFBGA package Note 4		17.2		°C/W
R_{θ_JB}	Thermal resistance junction to Board	100 TFBGA package Note 4		11.1		°C/W
R_{θ_JC}	Thermal resistance junction to case	100 TFBGA package Note 4		13.29		°C/W
P_D	Maximum power dissipation, see Section 5.2.1	100 VFBGA Derating factor above T_A = 70 °C: 36.1 mW/°C ($1/\theta_{JA}$)	2000			mW
		100 TFBGA Derating factor above T_A = 70 °C: 58.1 mW/°C ($1/\theta_{JA}$)	3770			mW

Note 1 $V_{DDIO1/2}$ must not exceed V_{DDREF}.

Note 2 For short durations to meet peak current requirements I_{OUT} can be operated at up to 20 % higher than the specified maximum operating condition. The part should not be operated in this mode for extended periods and is not guaranteed for continuous operation.

Note 3 Obtained from package thermal simulations, JEDEC 2S2P four layer board (76.2 mm x 114 mm x 1.6 mm), 70 µm (2 oz) copper thickness power planes, 35 µm (1 oz) copper thickness signal layer traces, natural convection (still air), see Section 9.1.

Note 4 Obtained from package thermal simulations, JEDEC 2S2P four layer board (101.6 mm x 114.3 mm x 1.6 mm), 70 µm (2 oz) copper thickness power planes, 35 µm (1 oz) copper thickness signal layer traces, natural convection (still air), see Section 9.1.

Note 5 Voltage on TP pin should be 0 V except during in-circuit programming.

5.2.1 Power Derating Curves

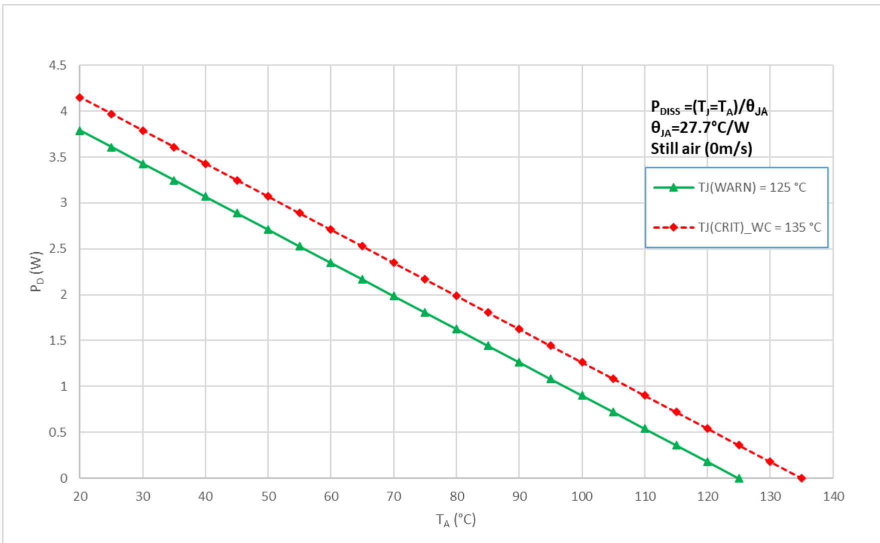


Figure 3: 100 VFBGA Power Derating Curve

Table 6: Typical Temperatures

	T_A = 70 °C	T_A = 85 °C	T_A = 105 °C
T_{J_WARN}	P_D = 1.99 W	P_D = 1.44 W	P_D = 0.72 W
$T_{J\_CRIT\_WC}$	P_D = 2.35 W	P_D = 1.81 W	P_D = 1.083 W

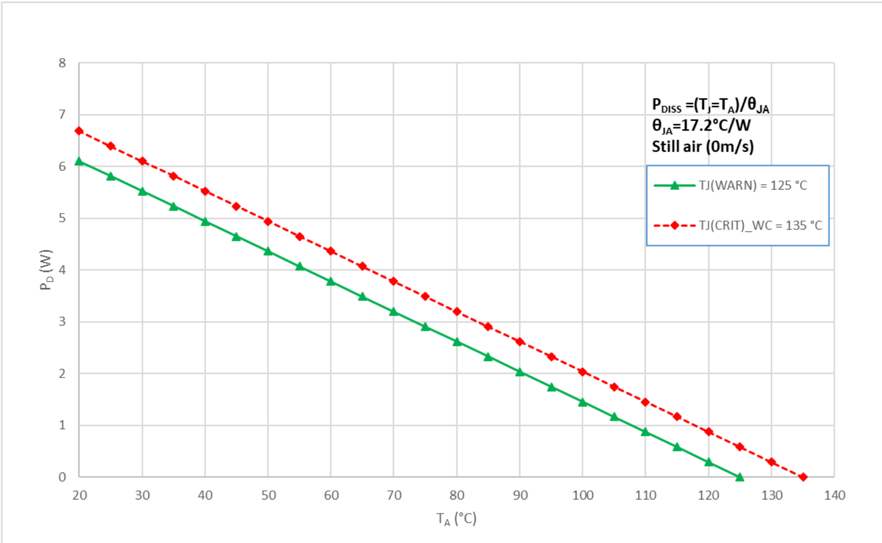


Figure 4:100 TFBGA Power Derating Curve

Table 7: Typical Temperatures

	T_A = 70 °C	T_A = 85 °C	T_A = 105 °C
T_{J_WARN}	P_D = 3.19 W	P_D = 2.32 W	P_D = 1.16 W
$T_{J\_CRIT\_WC}$	P_D = 3.77 W	P_D = 2.9 W	P_D = 1.74 W

5.3 Typical Current Consumption

Table 8: Typical Current Consumption

Operating Mode	Conditions (Note 1)	Backup Device	Battery	Unit
NO-POWER mode (POR)	2.4 V > V_{DDREF} > V_{BBAT} > 1.5 V	0	16	µA
DELIVERY mode Note 2	V_{BBAT} > V_{DDREF} > 1.5 V	0.5	0.4 Note 3	µA
	V_{DDREF} > V_{BBAT} > 1.5 V	0	1.5	
RTC mode Note 2	V_{BBAT} > V_{DDREF} > 2.0 V	1.4	1.06 Note 3	µA
	V_{DDREF} > V_{BBAT} > 2.0 V	0.05	7	
RESET mode	V_{DDREF} > 2.2 V, supplies off (except LDOCORE), RTC on, pulsed mode:			µA
	V_{BBAT} > V_{DDREF}	1.6	11	
	V_{BBAT} < V_{DDREF}	0.05	18	
LOW-POWER mode	V_{SYS} > $V_{DD\_FAULT\_LOWER}$, supplies off (except LDOCORE), all blocks in POWERDOWN mode, RTC on, pulsed mode with limited parametric compliance		18	µA
POWERDOWN mode (Hibernate)	V_{SYS} > $V_{DD\_FAULT\_LOWER}$, supplies off (except LDOCORE), all blocks in POWERDOWN mode, RTC on		40	µA
POWERDOWN mode (Standby)	BUCKCORE, LDOCORE, LDO2, 4, 5 enabled, RTC and GPIO unit on		65 Note 4	µA
ACTIVE mode	All supplies, GPIO, RTC and GPADC on		320	µA

Note 1 nONKEY/CHG_WAKE/V_{DDREF} detection circuit is enabled in all modes.

Note 2 See V_{BBAT} current in RTC or DELIVERY modes [1]

Note 3 0 µA if no main battery available.

Note 4 Regulators are running in SLEEP mode.

5.4 Digital I/O Characteristics

Table 9: Digital I/O Electrical Characteristics, T_J = -40 ºC to +125 ºC

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{IH}	GPI0 to GPI15, nOFF, nSHUTDOWN SYS_EN, PWR_EN, PWR1_EN Input High Voltage	VDDCORE mode	1.0		V_{SYS}	V
		VDD_IO2 mode	0.7*VDD_IO2		V_{SYS}	
V_{IL}	GPI0 to GPI15, nOFF, nSHUTDOWN SYS_EN, PWR_EN, PWR1_EN Input Low Voltage	VDDCORE mode	-0.3		0.4	V
		VDD_IO2 mode VDD_IO2 ≥ 1.5V	-0.3		0.3*VDD_IO2	
V_{IH}	nONKEY, CHG_WAKE Input High Voltage		1.0		V_{SYS}	V
V_{IL}	nONKEY, CHG_WAKE Input Low Voltage		-0.3		0.4	V
V_{IH}	CLK, DATA, SK, SI (2-WIRE mode) Input High Voltage	VDDCORE mode	1.0			V
		VDD_IO2 mode	0.7*VDD_IO2			
V_{IL}	CLK, DATA, SK, SI (2-WIRE mode) Input Low Voltage	VDDCORE mode			0.4	V
		VDD_IO2 mode VDD_IO2 ≥ 1.5V			0.3*VDD_IO2	
V_{IH}	SK, nCS, SI (4-WIRE mode) Input High Voltage		0.7*VDD_IOx			V
V_{IL}	SK, nCS, SI (4-WIRE mode) Input Low Voltage				0.3*VDD_IOx	V
V_{OH}	GPO0 to GPO15, nVDD_FAULT, SO, nRESET, nIRQ, E_GPI_2, COMP1V2, OUT_32K, OUT_32K_2 Output High Voltage	I_{OUT} = -1 mA VDD_IO1 ≥ 1.5 V VDD_IO1 mode	0.8*VDD_IO1			V
		I_{OUT} = -1 mA VDD_IO2 ≥ 1.5 V VDD_IO2 mode	0.8*VDD_IO2			
V_{OH}	GPO1, 3 to 6, 10, and 12 to 15, DATA, SI (2-WIRE mode) SO, nRESET, nIRQ, GP_FB2 Output High Voltage	Open drain			V_{DDREF}	V

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{OL}	GPO0 to GPO15, SO, nVDD_FAULT, nRESET (Note 1), nIRQ (Note 1), GP_FB2, E_GPI_2, COMP1V2, OUT_32K, OUT_32K_2, Output Low Voltage	I_{OUT} = 1 mA			0.3	V
V_{OL}	DATA, SI (2-WIRE mode) Output Low Voltage	I_{OUT} = 3 mA			0.24	V
V_{OL}	SI (2-WIRE mode) Output Low Voltage	I_{OUT} = 8 mA			0.4	V
C_{IN}	CLK, DATA, SK, SI Input Capacitance				10	pF
t_{fDA}	SI (2-WIRE MODE) Data Fall Time	Fast C_B < 550 pF	20 + 0.1 Cb		120	ns
		HS 10 < C_B < 100 pF	10		40	
		HS C_B < 400 pF	20		80	
	Sink current capability GPO 10, 11, 14, 15	V_{GPIO} = 0.4 V Note 2		11		mA
	Source current capability GPO 10, 11,14,15	V_{GPIO} = 0.8*VDD_IO1/2 Note 2		-4		mA
	Sink current capability GPO 0 to 9, 12, 13	V_{GPIO} = 0.3 V		1		mA
	Source current capability GPO 0 to 9, 12, 13	V_{GPIO} = 0.8*VDD_IO1/2 Note 3		-1		mA
	GPI pull-down resistor		50	100	250	kΩ
	GPO pull-up resistor Note 4	VDD_IO1/2 = 1.5 V	60	180	310	kΩ
		VDD_IO1/2 = 1.8 V	45	120	190	
		VDD_IO1/2 = 3.3 V	20	40	60	

Note 1 Electrical characteristics are guaranteed down to V_{DDREF} = 2.0 V (V_{POR_LOWER}). For lower voltages the port continues operating with reduced performance.

Note 2 At low V_{DDREF} values and high temperatures, the sink current capability is reduced.

Note 3 For VDD_IO1/2 < 1.5 V the source current capability is reduced.

Note 4 V(PAD) = 0 V.

5.5 Watchdog

Table 10: Watchdog, T_J = -40 ºC to +125 ºC

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_{WD_MIN}	Minimum Watchdog time	External 32 kHz oscillator			0.11	s
		Internal 25 kHz oscillator			0.2	s
T_{WD_MAX}	Maximum Watchdog time	External 32 kHz oscillator	2			s
		Internal 25 kHz oscillator	2.5			

5.6 Power Manager and HS-2-Wire Control Bus

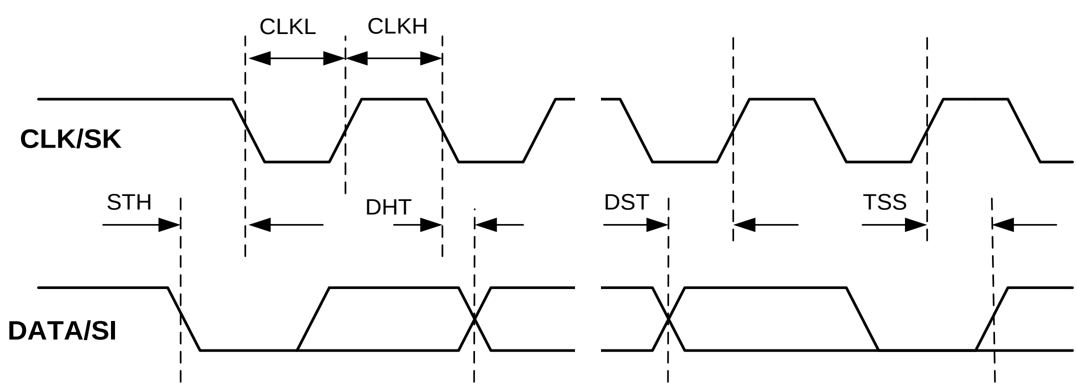


Figure 5: 2-Wire Bus Timing

Table 11: Power Manager and HS-2-Wire Control Bus Electrical Characteristics, T_J = -40 ºC to +125 ºC

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Bus free time STOP to START		0.5			µs
C_B	Bus line capacitive load				150	pF
Standard/Fast/Fast+ Mode						
	CLK clock frequency	VDD_IO2 ≥ 1.5 V Note 1	0		1000	kHz
	Bus free time STOP to START		0.5			µs
	Start condition set-up time		0.26			µs
STH	Start condition hold time		0.26			µs
CLKL	CLK low time		0.5			µs
CLKH	CLK high time		0.26			µs
	2-WIRE CLK and DATA rise time	(input requirement)			1000	ns

Parameter	Description	Conditions	Min	Typ	Max	Unit
	2-WIRE CLK and DATA fall time	(input requirement)			300	ns
DST	Data set-up time		50			ns
DHT	Data hold-time		0			ns
	Data valid time				0.45	µs
	Data valid time acknowledge				0.45	µs
TSS	Stop condition set-up time		0.26			µs
High Speed Mode						
	CLK clock frequency	VDD_IO2 ≥ 1.8 V Note 1	0		3400	kHz
	Start condition set-up time		160			ns
STH	Start condition hold time		160			ns
CLKL	CLK low time		160			ns
CLKH	CLK high time		60			ns
	2-WIRE CLKH and SDAH rise/fall time	Input requirement			160	ns
DST	Data set-up time		10			ns
DHT	Data hold-time		0			ns
TSS	Stop condition set-up time		160			ns

Note 1 Minimum clock frequency is 10 kHz if TWOWIRE_TO is enabled.

5.7 4-Wire Control Bus

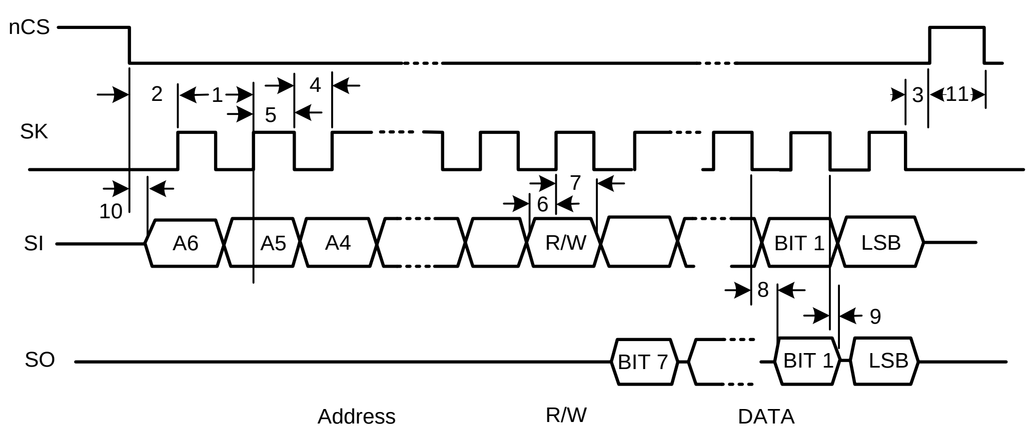


Figure 6: 4-Wire Bus Timing

Note 1 The above timing is valid for active-low and high CS.

Table 12: 4-Wire Control Bus, T_J = -40 ºC to +125 ºC

Parameter	Description	Label in Plot	Min	Typ	Max	Unit
C_B	Bus line capacitive load				100	pF
t_C	Cycle time	1	70			ns
t_{CSS}	Enable lead time	2, from nCS active to first SK edge	20			ns
t_{SCS}	Enable lag time	3, from last SK edge to nCS idle	20			ns
t_{CL}	Clock low time	4	0.4 * t_C			ns
t_{CH}	Clock high time	5	0.4 * t_C			ns
t_{SIS}	Data-in set-up time	6	5			ns
t_{SIH}	Data-in hold time	7	5			ns
t_{SOV}	Data-out valid time	8			22	ns
t_{SOH}	Data-out hold time	9	6			ns
t_{WCS}	CS inactive time	11	20			ns

5.8 LDO Voltage Regulators

5.8.1 LDO1

Table 13: LDO1, T_J = -40 °C to +125 °C

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage	$V_{DD} = V_{SYS}$	2.8		5.5	V
		If supplied from buck	1.5 Note 1			
V_{LDO}	Output voltage		0.6	Note 2	1.86	V
V_{LDO_ACC}	Output accuracy	$V_{DD} = V_{SYS}$ = 2.8 V to 5.5 V I_{OUT} = 100 mA Including static line/load regulation	-3		+3	%
C_{OUT}	Stabilization capacitor	Including voltage and temperature coefficient at configured VLDO1	-55 %	1.0	+35 %	µF
R_{COUT_ESR}	Output capacitor ESR	f > 1 MHz Including wiring parasitics	0		300	mΩ
I_{OUT_MAX}	Output current	$V_{DD} = V_{SYS}$ = 2.8 V to 5.5 V	100			mA
I_{SHORT}	Short circuit current			200		mA
I_{SLEEP}	Maximum forced sleep mode current	V_{DD} ≥ 1.8 V	10			mA
$V_{DROPOUT}$	Dropout voltage	$V_{DD} = V_{SYS}$ > 2.8 V I_{OUT} = 100 mA (V_{DD} = 1.5 V, $I_{OUT} = I_{MAX}/3$)		100	150	mV
V_{S_LINE}	Static line regulation	$V_{DD} = V_{SYS}$ = 3.0 V to 5.5 V I_{OUT} = 100 mA		1	5	mV
V_{S_LOAD}	Static load regulation	I_{OUT} = 1 mA to 100 mA		5	10	mV
V_{TR_LINE}	Line transient response	$V_{DD} = V_{SYS}$ = 3.0 V to 3.6 V I_{OUT} = 100 mA tr = tf = 10 µs		5	10	mV
V_{TR_LOAD}	Load transient response	V_{DD} = 3.6 V I_{OUT} = 1 mA to 100 mA tr = tf = 1 µs		30	50	mV
PSRR Note 3	PSRR	f = 10 Hz to 10 kHz, 25 °C V_{DD} = 3.6 V, $I_{OUT} = I_{MAX}/2$ $V_{DD} – V_{LDO}$ ≥ 0.6 V	50	60		dB
N	Output noise	$V_{DD} = V_{SYS}$ = 3.6 V, V_{LDO} = 1.8 V I_{OUT} = 5 mA to I_{MAX} f = 10 Hz to 100 kHz, 25 °C		70		µV rms
I_{Q_ON}	Quiescent current in ON mode	Note 4		9 + 0.7 % of I_{OUT}		µA

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{Q_SLEEP}	Quiescent current forced sleep mode			1.5 + 1.4% of I_{OUT}		µA
I_{Q_OFF}	Quiescent current OFF mode			1		µA
t_{ON}	Turn-on time	10 % to 90 %			300	µs
		SLEEP mode			390	
t_{OFF}	Turn off time	90 % to 10% Pull-down resistor enabled			1	ms
R_{OFF}	Pull-down resistance in OFF mode	Can be disabled via LDO1_PD_DIS		55		Ω

Note 1 Max output current is 30 % when the input voltage is 1.5 V.

Note 2 Programmable in 20 mV voltage steps.

Note 3 Measured at point of load.

Note 4 Internal regulator current flowing to ground.

5.8.2 LDO2

Table 14: LDO2, T_J = -40 °C to +125 °C

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage	V_{DD} = V_{SYS}	2.8		5.5	V
		If supplied from buck	1.5 Note 1			
V_{LDO}	Output voltage		0.6	Note 2	1.86	V
V_{LDO_ACC}	Output accuracy	V_{DD} = V_{SYS} = 2.8 V to 5.5 V I_{OUT} = 200 mA Including static line/load regulation	-3		+3	%
C_{OUT}	Stabilization capacitor	Including voltage and temperature coefficient at configured VLDO2	-55 %	2.2	+35 %	µF
R_{COUT_ESR}	Output capacitor ESR	f > 1 MHz including wiring parasitics	0		300	mΩ
I_{OUT_MAX}	Output current	V_{DD} = V_{SYS} = 2.8 V to 5.5 V	200			mA
I_{SHORT}	Short circuit current			400		mA
I_{SLEEP}	Maximum forced sleep mode current	V_{DD} ≥ 1.8 V	20			mA
$V_{DROPOUT}$	Dropout voltage	V_{DD} = V_{SYS} > 2.8 V I_{OUT} = 200 mA (V_{DD} = 1.5 V, I_{OUT} = I_{MAX}/3)		100	150	mV
V_{S_LINE}	Static line regulation	V_{DD} = V_{SYS} = 3.0 V to 5.5 V I_{OUT} = 200 mA		1	5	mV
V_{S_LOAD}	Static load regulation	I_{OUT} = 1 mA to 200 mA		5	10	mV

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{TR_LINE}	Line transient response	$V_{DD} = V_{SYS}$ = 3.0 V to 3.6 V I_{OUT} = 100 mA tr = tf = 10 µs		5	10	mV
V_{TR_LOAD}	Load transient response	V_{DD} = 3.6 V I_{OUT} = 1 mA to 200 mA tr = tf = 1 µs		30	50	mV
PSRR Note 3	PSRR	f = 10 Hz to 10 kHz , 25 °C V_{DD} = 3.6 V, $I_{OUT} = I_{MAX}/2$ $V_{DD} – V_{LDO} \geq 0.6$ V	50	60		dB
N	Output noise	$V_{DD} = V_{SYS}$ = 3.6 V V_{LDO} = 1.8 V I_{OUT} = 5 mA to I_{MAX} f = 10 Hz to 100 kHz, 25 °C		70		µV rms
I_{Q_ON}	Quiescent current in ON mode	Note 4		9 + 0.4% of I_{OUT}		µA
I_{Q_SLEEP}	Quiescent current forced sleep mode			1.5 + 0.9% of I_{OUT}		µA
I_{Q_OFF}	Quiescent current OFF mode			1		µA
t_{ON}	Turn-on time	10 to 90%			150	µs
		SLEEP mode			195	
t_{OFF}	Turn off time	90 to 10%, pull-down resistor enabled			1	ms
R_{OFF}	Pull-down resistance in OFF mode	Can be disabled via LDO2_PD_DIS		55		Ω

Note 1 Max output current is 30% when the input voltage is 1.5 V.

Note 2 Programmable in 20 mV voltage steps.

Note 3 Measured at point of load.

Note 4 Internal regulator current flowing to ground.

5.8.3 LDO3

Table 15: LDO3, T_J = -40 °C to +125 °C

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage	$V_{DD} = V_{SYS}$	2.8		5.5	V
		If supplied from buck	(1.5) Note 1			
V_{LDO}	Output voltage		0.9	Note 2	3.44	V
V_{LDO_ACC}	Output accuracy Note 3	$V_{DD} = V_{SYS}$ = 2.8V to 5.5 V I_{OUT} = 200 mA Including static line/load regulation	-3		+3	%

Parameter	Description	Conditions	Min	Typ	Max	Unit
C_{OUT}	Stabilization capacitor	Including voltage and temperature coefficient at configured VLDO3	-55%	2.2	+35%	µF
R_{COUT_ESR}	Output capacitor ESR	f > 1 MHz including wiring parasitics	0		300	mΩ
I_{OUT_MAX}	Output current	V_{DD} = V_{SYS} = 2.8 V to 5.5 V	200			mA
I_{SHORT}	Short circuit current			400		mA
I_{SLEEP}	Maximum forced sleep mode current	V_{DD} ≥ 1.8 V	20			mA
$V_{DROPOUT}$	Dropout voltage	V_{DD} = V_{SYS} > 2.8 V I_{OUT} = 100 mA (V_{DD} = 1.5 V, I_{OUT} = I_{MAX}/3)		100	150	mV
V_{S_LINE}	Static line regulation	V_{DD} = V_{SYS} = 3.0 V to 5.5 V I_{OUT} = 200 mA		1	5	mV
V_{S_LOAD}	Static load regulation	I_{OUT} = 1 mA to 200 mA		5	10	mV
V_{TR_LINE}	Line transient response	V_{DD} = V_{SYS} = 3.0 V to 3.6 V I_{OUT} = 100 mA tr = tf = 10 µs		5	10	mV
V_{TR_LOAD}	Load transient response	V_{DD} = 3.6 V I_{OUT} = 1 mA to 200 mA tr = tf = 1 µs		30	50	mV
PSRR Note 4	PSRR	f = 10 Hz to 10 kHz, 25 °C V_{DD} = 3.6 V, I_{OUT} = I_{MAX}/2 V_{DD} – V_{LDO} ≥ 0.6 V	50	60		dB
N	Output noise	V_{DD} = V_{SYS} = 3.6 V, V_{LDO} = 2.8 V I_{OUT} = 5 mA to I_{MAX} f = 10 Hz to 100 kHz, 25 °C		70		µV rms
I_{Q_ON}	Quiescent current in ON mode	Note 5		9 + 0.45% of I_{OUT}		µA
I_{Q_SLEEP}	Quiescent current forced sleep mode			1.5 + 1.0% of I_{OUT}		µA
I_{Q_OFF}	Quiescent current OFF mode			1		µA
t_{ON}	Turn-on time	10 to 90%			300	µs
		SLEEP mode			390	
t_{OFF}	Turn off time	90 % to 10 % Pull-down resistor enabled			1	ms
R_{OFF}	Pull-down resistance in OFF mode	Can be disabled via LDO3_PD_DIS		55		Ω
Bypass Mode						
R_{ON}	Bypass on-resistance	V_{DD} > 2.2 V		0.5	0.7	Ω

Parameter	Description	Conditions	Min	Typ	Max	Unit
		V_{DD} > 1.8 V			1.0	
I_{LIM}	Current limit in Bypass mode			380		mA
I_{Q_BYPASS}	Quiescent current in Bypass mode			50	100	µA

Note 1 Max output current is 30% when the input voltage is 1.5 V.

Note 2 Programmable in 20 mV voltage steps.

Note 3 Accuracy values not applicable if bypass mode has been configured.

Note 4 Measured at point of load.

Note 5 Internal regulator current flowing to ground.

5.8.4 LDO4

Table 16: LDO4, T_J = -40 ºC to +125 ºC

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage	$V_{DD} = V_{SYS}$	2.8		5.5	V
		If supplied from buck	1.5 Note 1			
V_{LDO}	Output voltage		0.9	Note 2	3.44	V
V_{LDO_ACC}	Output accuracy Note 3	$V_{DD} = V_{SYS}$ = 2.8 V to 5.5 V I_{OUT} = 200 mA Including static line/load regulation	-3		+3	%
C_{OUT}	Stabilization capacitor	Including voltage and temperature coefficient at configured VLDO4	-55 %	2.2	+35 %	µF
R_{COUT_ESR}	Output capacitor ESR	f > 1 MHz Including wiring parasitics	0		300	mΩ
I_{OUT_MAX}	Output current	$V_{DD} = V_{SYS}$ = 2.8 V to 5.5 V	200			mA
I_{SHORT}	Short circuit current			400		mA
I_{SLEEP}	Maximum forced sleep mode current	V_{DD} ≥ 1.8 V	30			mA
$V_{DROPOUT}$	Dropout voltage	$V_{DD} = V_{SYS}$ > 2.8 V I_{OUT} = 200 mA (V_{DD} = 1.5 V, $I_{OUT} = I_{MAX}/3$)		100	150	mV
V_{S_LINE}	Static line regulation	$V_{DD} = V_{SYS}$ = 3.0 V to 5.5 V I_{OUT} = 200 mA		1	5	mV
V_{S_LOAD}	Static load regulation	I_{OUT} = 1 mA to 200 mA		5	10	mV
V_{TR_LINE}	Line transient response	$V_{DD} = V_{SYS}$ = 3.0V to 3.6 V I_{OUT} = 100 mA tr = tf = 10 µs		5	10	mV
V_{TR_LOAD}	Load transient response	V_{DD} = 3.6 V I_{OUT} = 1 mA to 200 mA tr = tf = 1 µs		30	50	mV
PSRR Note 4	PSRR	f = 10 Hz to 10 kHz , 25 °C V_{DD} = 3.6 V, $I_{OUT} = I_{MAX}/2$ $V_{DD} – V_{LDO}$ ≥ 0.6 V	50	60		dB
N	Output noise	$V_{DD} = V_{SYS}$ = 3.6 V, V_{LDO} = 2.8 V I_{OUT} = 5 mA to I_{MAX} f = 10 Hz to 100 kHz, 25 °C		70		µV rms
I_{Q_ON}	Quiescent current in ON mode	Note 5		9 + 0.4% of I_{OUT}		µA
I_{Q_SLEEP}	Quiescent current forced sleep mode			1.5 + 1.0% of I_{OUT}		µA

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{Q_OFF}	Quiescent current OFF mode			1		µA
t_{ON}	Turn-on time	10 % to 90%			300	µs
		SLEEP mode			390	
t_{OFF}	Turn off time	90 % to 10% Pull-down resistor enabled			1	ms
R_{OFF}	Pull-down resistance in OFF mode	Can be disabled via LDO4_PD_DIS		55		Ω
Bypass mode						
R_{ON}	Bypass on-resistance	V_{DD} > 2.2 V		0.5	0.7	Ω
		V_{DD} > 1.8 V			1.0	
I_{LIM}	Current limit in Bypass mode			175		mA
I_{Q_BYPASS}	Quiescent current in Bypass mode			50	100	µA

Note 1 Max output current is 30% when the input voltage is 1.5 V.

Note 2 Programmable in 20 mV voltage steps.

Note 3 Accuracy values not applicable if bypass mode has been configured.

Note 4 Measured at point of load.

Note 5 Internal regulator current flowing to ground.

5.8.5 LDO5

Table 17: LDO5, T_J = -40 °C to +125 °C

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage	V_{DD} = V_{SYS}	2.8		5.5	V
		If supplied from buck	1.5 Note 1			
V_{LDO}	Output voltage		0.9	Note 2	3.6	V
V_{LDO_ACC}	Output accuracy	V_{DD} = V_{SYS} = 2.8 V to 5.5 V I_{OUT} = 100 mA Including static line/load regulation	-3		+3	%
C_{OUT}	Stabilization capacitor	Including voltage and temperature coefficient at configured VLDO5	-55 %	1.0	+35 %	µF
R_{COUT_ESR}	Output capacitor ESR	f > 1 MHz Including wiring parasitics	0		300	mΩ
I_{OUT_MAX}	Output current	V_{DD} = V_{SYS} = 2.8 V to 5.5 V	100			mA
I_{SHORT}	Short circuit current			200		mA
I_{SLEEP}	Maximum forced sleep mode current	V_{DD} ≥ 1.8 V	20			mA

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{DROPOUT}$	Dropout voltage	$V_{DD} = V_{SYS} > 2.8$ V $I_{OUT} = 100$ mA ($V_{DD} = 1.5$ V, $I_{OUT} = I_{MAX}/3$)		100	150	mV
V_{S_LINE}	Static line regulation	$V_{DD} = V_{SYS} = 3.0$ V to 5.5 V $I_{OUT} = 100$ mA		1	5	mV
V_{S_LOAD}	Static load regulation	$I_{OUT} = 1$ mA to 100 mA		5	10	mV
V_{TR_LINE}	Line transient response	$V_{DD} = V_{SYS} = 3.0$ V to 3.6 V $I_{OUT} = 100$ mA tr = tf = 10 µs		5	10	mV
V_{TR_LOAD}	Load transient response	$V_{DD} = 3.6$ V $I_{OUT} = 1$ mA to 100 mA tr = tf = 1 µs		30	50	mV
PSRR Note 3	PSRR	f = 10 Hz to 10 kHz , 25 °C $V_{DD} = 3.6$ V, $I_{OUT} = I_{MAX}/2$ $V_{DD} – V_{LDO} \geq 0.6$ V	50	60		dB
N	Output noise	$V_{DD} = V_{sys} = 3.6$ V, $V_{LDO} = 2.8$ V $I_{OUT} = 5$ mA to I_{MAX} f = 10 Hz to 100 kHz, 25 °C		70		µV rms
I_{Q_ON}	Quiescent current in ON mode	Note 4		9 + 0.9 % of I_{OUT}		µA
I_{Q_SLEEP}	Quiescent current forced sleep mode			1.5 + 1.6 % of I_{OUT}		µA
I_{Q_OFF}	Quiescent current OFF mode			1		µA
t_{ON}	Turn-on time	10 % to 90 %			350	µs
		SLEEP mode			450	
t_{OFF}	Turn off time	90 % to 10 % Pull-down resistor enabled			1	ms
R_{OFF}	Pull-down resistance in OFF mode	Can be disabled via LDO5_PD_DIS		55		Ω

Note 1 Max output current is 30% when the input voltage is 1.5 V.

Note 2 Programmable in 50 mV voltage steps.

Note 3 Measured at point of load.

Note 4 Internal regulator current flowing to ground.

5.8.6 LDO6

Table 18: LDO6, T_J = -40 ºC to +125 ºC

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage	V_{DD} = V_{SYS}	2.8		5.5	V
		If supplied from buck	1.5 Note 1			
V_{LDO}	Output voltage		0.9	Note 2	3.6	V
V_{LDO_ACC}	Output accuracy	V_{DD} = V_{SYS} = 2.8 V o 5.5 V I_{OUT} = 200 mA Including static line/load regulation	-3		+3	%
C_{OUT}	Stabilization capacitor	Including voltage and temperature coefficient at configured VLDO6	-55%	2.2	+35%	µF
R_{COUT_ESR}	Output capacitor ESR	f > 1 MHz Including wiring parasitics	0		300	mΩ
I_{OUT_MAX}	Output current	V_{DD} = V_{SYS} = 2.8 V to 5.5 V	200			mA
I_{SHORT}	Short circuit current			400		mA
I_{SLEEP}	Maximum forced sleep mode current	V_{DD} ≥ 1.8 V	30			mA
$V_{DROPOUT}$	Dropout voltage	V_{DD} = V_{SYS} > 2.8 V I_{OUT} = 200 mA (V_{DD} = 1.5 V, I_{OUT} = I_{MAX}/3)		100	150	mV
V_{S_LINE}	Static line regulation	V_{DD} = V_{SYS} = 3.0 V to 5.5 V I_{OUT} = 200 mA		1	5	mV
V_{S_LOAD}	Static load regulation	I_{OUT} = 1 mA to 200 mA		5	10	mV
V_{TR_LINE}	Line transient response	V_{DD} = V_{SYS} = 3.0 V to 3.6 V I_{OUT} = 100 mA tr = tf = 10 µs		5	10	mV
V_{TR_LOAD}	Load transient response	V_{DD} = 3.6 V I_{OUT} = 1 mA to 200 mA tr = tf = 1 µs		30	50	mV
PSRR Note 3	PSRR	V_{DD} = 3.6 V, I_{OUT} = I_{MAX}/2 V_{DD} – V_{LDO} ≥ 0.6 V, 25 °C				dB
		f = 10 Hz to 1 kHz,	70	80		
		f = 1 kHz to 10 kHz	60	70		
		f = 10 kHz to 100 kHz	40	50		
N	Output noise	V_{DD} = V_{SYS} = 3.6 V, V_{LDO} = 2.8 V I_{OUT} = 5 mA to I_{MAX} f = 10 Hz to 100 kHz, 25 °C		35		µV rms

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{Q_ON}	Quiescent current in ON mode	Note 4		9+0.45 % of I_{OUT}		µA
I_{Q_SLEEP}	Quiescent current forced sleep mode			2+1.0 % of I_{OUT}		µA
I_{Q_OFF}	Quiescent current OFF mode			1		µA
t_{ON}	Turn-on time	10 % to 90 %			200	µs
		SLEEP mode			260	
t_{OFF}	Turn off time	90 % to 10 % Pull-down resistor enabled			1	ms
R_{OFF}	Pull-down resistance in OFF mode	Can be disabled via LDO6_PD_DIS		55		Ω

Note 1 Max output current is 30% when the input voltage is 1.5 V.

Note 2 Programmable in 50 mV voltage steps.

Note 3 Measured at point of load.

Note 4 Internal regulator current flowing to ground.

5.8.7 LDO7

Table 19: LDO7, T_J = -40 °C to 125 °C

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage	$V_{DD} = V_{SYS}$	2.8		5.5	V
		If supplied from buck	1.5 Note 1			
V_{LDO}	Output voltage		0.9	Note 2	3.6	V
V_{LDO_ACC}	Output accuracy Note 3	$V_{DD} = V_{SYS}$ = 2.8 V to 5.5 V I_{OUT} = 200 mA Including static line/load regulation	-3		+3	%
C_{OUT}	Stabilization capacitor	Including voltage and temperature coefficient at configured VLDO7	-55 %	2.2	+35 %	µF
R_{COUT_ESR}	ESR of capacitor	f > 1 MHz Including track impedance	0		300	mΩ
I_{OUT_MAX}	Maximum output current	$V_{DD} = V_{SYS}$ = 2.8 V to 5.5 V	200			mA
I_{SHORT}	Short circuit current			400		mA
I_{SLEEP}	Maximum forced sleep mode current	V_{DD} ≥ 1.8 V	30			mA
$V_{DROPOUT}$	Dropout voltage	$V_{DD} = V_{SYS}$ > 2.8 V I_{OUT} = 200 mA (V_{DD} = 1.5 V, $I_{OUT} = I_{MAX}/3$)		100	150	mV

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{S_LINE}	Static line regulation	$V_{DD} = V_{SYS}$ = 3.0V to 5.5 V I_{OUT} = 200 mA		1	5	mV
V_{S_LOAD}	Static load regulation	I_{OUT} = 1 mA to 200 mA		5	10	mV
V_{TR_LINE}	Line transient response	$V_{DD} = V_{SYS}$ = 3.0 V to 3.6 V I_{OUT} = 100 mA tr = tf = 10 µs		5	10	mV
V_{TR_LOAD}	Load transient response	V_{DD} = 3.6 V I_{OUT} = 1 mA to 200 mA tr = tf = 1 µs		30	50	mV
PSRR Note 4	PSRR	f = 10 Hz to 10 kHz, 25 °C V_{DD} = 3.6 V, $I_{OUT} = I_{MAX}/2$ $V_{DD} – V_{LDO}$ ≥ 0.6 V	50	60		dB
N	Output noise	$V_{DD} = V_{sys}$ = 3.6 V, V_{LDO} = 2.8 V I_{OUT} = 5 mA to I_{MAX} f = 10 Hz to 100 kHz, 25 °C		70		µV rms
I_{Q_ON}	Quiescent current in ON mode	Note 5		9+0.4 % of I_{OUT}		µA
I_{Q_SLEEP}	Quiescent current forced sleep mode			1.5+1.0% of I_{OUT}		µA
I_{Q_OFF}	Quiescent current OFF mode			1		µA
t_{ON}	Turn-on time	10 % to 90 %			300	µs
		SLEEP mode			390	
t_{OFF}	Turn off time	90 % to 10 % Pull-down resistor enabled			1	ms
R_{OFF}	Pull-down resistance in OFF mode	Can be disabled via LDO7_PD_DIS		55		Ω
Bypass mode						
R_{ON}	Bypass on-resistance	V_{DD} > 2.2 V		0.5	0.7	Ω
		V_{DD} > 1.8 V			1.0	
I_{LIM}	Current limit in Bypass mode			280		mA
I_{Q_BYPASS}	Quiescent current			50	100	µA

Note 1 Max output current is 30% when the input voltage is 1.5 V.

Note 2 Programmable in 50 mV voltage steps.

Note 3 Accuracy values not applicable if bypass mode has been configured.

Note 4 Measured at point of load.

Note 5 Internal regulator current flowing to ground.

5.8.8 LDO8

Table 20: LDO8, T_J = -40 ºC to +125 ºC

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage	$V_{DD} = V_{SYS}$	2.8		5.5	V
		If supplied from buck	1.5 Note 1			
V_{LDO}	Output voltage		0.9	Note 2	3.6	V
V_{LDO_ACC}	Output accuracy Note 3	$V_{DD} = V_{SYS}$ = 2.8 V to 5.5 V I_{OUT} = 200 mA Including static line/load regulation	-3		+3	%
C_{OUT}	Stabilization capacitor	Including voltage and temperature coefficient at configured VLDO8	-55 %	2.2	+35 %	µF
R_{COUT_ESR}	ESR of capacitor	f > 1 MHz Including track impedance	0		300	mΩ
I_{OUT_MAX}	Maximum output current	$V_{DD} = V_{SYS}$ = 2.8 V to 5.5 V	200			mA
I_{SHORT}	Short circuit current			400		mA
I_{SLEEP}	Maximum forced sleep mode current	V_{DD} ≥ 1.8 V	30			mA
$V_{DROPOUT}$	Dropout voltage	$V_{DD} = V_{SYS}$ > 2.8 V I_{OUT} = 200 mA (V_{DD} = 1.5 V, $I_{OUT} = I_{MAX}/3$)		100	150	mV
V_{S_LINE}	Static line regulation	$V_{DD} = V_{SYS}$ = 3.0 V to 5.5 V I_{OUT} = 200 mA		1	5	mV
V_{S_LOAD}	Static load regulation	I_{OUT} = 1 mA to 200 mA		5	10	mV
V_{TR_LINE}	Line transient response	$V_{DD} = V_{SYS}$ = 3.0 V to 3.6 V I_{OUT} = 100 mA tr = tf = 10 µs		5	10	mV
V_{TR_LOAD}	Load transient response	V_{DD} = 3.6 V I_{OUT} = 1 mA to 200 mA tr = tf = 1 µs		30	50	mV
PSRR Note 4	PSRR	f = 10 Hz to 10 kHz, 25 °C V_{DD} = 3.6 V, $I_{OUT} = I_{MAX}/2$ $V_{DD} - V_{LDO}$ ≥ 0.6 V	50	60		dB
N	Output noise	$V_{DD} = V_{SYS}$ = 3.6 V, V_{LDO} = 2.8 V I_{OUT} = 5 mA to I_{MAX} f = 10 Hz to 100 kHz, 25 °C		70		µV rms
I_{Q_ON}	Quiescent current in ON mode	Note 5		9 + 0.4 % of I_{OUT}		µA
I_{Q_SLEEP}	Quiescent current forced sleep mode			1.5 + 1.0 % of I_{OUT}		µA

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{Q_OFF}	Quiescent current OFF mode			1		µA
t_{ON}	Turn-on time	10 % to 90 %			300	µs
		SLEEP mode			390	
t_{OFF}	Turn off time	90 % to 10 % Pull-down resistor enabled			1	ms
R_{OFF}	Pull-down resistance in OFF mode	Can be disabled via LDO8_PD_DIS		55		Ω
Vibration Motor Driver Mode						
VIB_SET	Output voltage (average)	6-bit resolution	0		3	V
I_{MAX}	Maximum output current				300	mA
I_{SHORT}	Short circuit current			400		mA
R_{LOAD}	Load resistance		8	10	10000	Ω
Z_{LOAD}	Load impedance			200		µH
R_{PU}	Pull-up resistor			0.5		Ω
R_{PD}	Pull-down resistor			5		Ω
Bypass Mode						
R_{ON}	Bypass on-resistance	V_{DD} > 2.2 V		0.5	0.7	
		V_{DD} > 1.8 V			1.0	Ω
I_{LIM}	Current limit in Bypass mode			400		mA
I_{Q_BYPASS}	Quiescent current in Bypass mode			50	100	µA

Note 1 Max output current is 30% when the input voltage is 1.5 V.

Note 2 Programmable in 50 mV voltage steps.

Note 3 Accuracy values not applicable if bypass mode has been configured.

Note 4 Measured at point of load.

Note 5 Internal regulator current flowing to ground.

5.8.9 LDO9

Table 21: LDO9, T_J = -40 ºC to +125 ºC

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage	$V_{DD} = V_{SYS}$	2.8		5.5	V
		If supplied from buck	1.5 Note 1			
V_{LDO}	Output voltage		0.95	Note 2	3.6	V
V_{LDO_ACC}	Output accuracy Note 3	$V_{DD} = V_{SYS}$ = 2.8 V to 5.5 V I_{OUT} = 200 mA Including static line/load regulation	-3		+3	%
C_{OUT}	Stabilization capacitor	Including voltage and temperature coefficient at configured VLDO9	-55 %	2.2	+35 %	µF
R_{COUT_ESR}	ESR of capacitor	f > 1 MHz	0		300	mΩ
I_{OUT_MAX}	Maximum output current	$V_{DD} = V_{SYS}$ = 2.8 V to 5.5 V	200			mA
I_{SHORT}	Short circuit current			400		mA
I_{SLEEP}	Maximum forced sleep mode current	V_{DD} ≥ 1.8 V	30			mA
$V_{DROPOUT}$	Dropout voltage	$V_{DD} = V_{SYS}$ > 2.8 V I_{OUT} = 200 mA (V_{DD} = 1.5 V, $I_{OUT} = I_{MAX}/3$)		100	150	mV
V_{S_LINE}	Static line regulation	$V_{DD} = V_{SYS}$ = 3.0 V to 5.5 V I_{OUT} = 200 mA		1	5	mV
V_{S_LOAD}	Static load regulation	I_{OUT} = 1 mA to 200 mA		5	10	mV
V_{TR_LINE}	Line transient response	$V_{DD} = V_{SYS}$ = 3.0 V to 3.6 V I_{OUT} = 100 mA tr = tf = 10 µs		5	10	mV
V_{TR_LOAD}	Load transient response	V_{DD} = 3.6 V I_{OUT} = 1 mA to 200 mA tr = tf = 1 µs		30	50	mV
PSRR Note 4	PSRR	f = 10 Hz to 10 kHz , 25 °C V_{DD} = 3.6 V, $I_{OUT} = I_{MAX}/2$ $V_{DD} – V_{LDO}$ ≥ 0.6 V	60	70		dB
N	Output noise	$V_{DD} = V_{sys}$ = 3.6 V, V_{LDO} = 2.8 V I_{OUT} = 5 mA to I_{MAX} f = 10 Hz to 100 kHz, 25 °C		35		µV rms
I_{Q_ON}	Quiescent current in ON mode	Note 5		9+0.4% of I_{OUT}		µA
I_{Q_SLEEP}	Quiescent current forced sleep mode			2+1.0% of I_{OUT}		µA

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{Q_OFF}	Quiescent current OFF mode			1		µA
t_{ON}	Turn-on time	10 % to 90 %			200	µs
		SLEEP mode			260	
t_{OFF}	Turn off time	90 % to 10 % Pull-down resistor enabled			1	ms
R_{OFF}	Pull-down resistance in OFF mode	Can be disabled via LDO9_PD_DIS		55		Ω

Note 1 Max output current is 30 % when the input voltage is 1.5 V.

Note 2 Programmable in 50 mV voltage steps.

Note 3 At trimmed output voltage.

Note 4 Measured at point of load.

Note 5 Internal regulator current flowing to ground.

5.8.10 LDO10

Table 22: LDO10, T_J = -40 °C to 125 °C

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage	V_{DD} = V_{SYS}	2.8		5.5	V
		If supplied from buck	1.5 Note 1			
V_{LDO}	Output voltage		0.9	Note 2	3.6	V
V_{LDO_ACC}	Output accuracy	V_{DD} = V_{SYS} = 2.8 to 5.5 V I_{OUT} = 300 mA Including static line/load regulation	-3		+3	%
C_{OUT}	Stabilization capacitor	Including voltage and temperature coefficient configured VLDO10	-55%	2.2	+35%	µF
R_{COUT_ESR}	Output capacitor ESR	f > 1 MHz Including wiring parasitics	0		300	mΩ
I_{OUT_MAX}	Output current	V_{DD} = V_{SYS} = 2.8 V to 5.5 V	300			mA
I_{SHORT}	Short circuit current			600		mA
I_{SLEEP}	Maximum sleep mode current	V_{DD} ≥ 1.8 V	30			mA
$V_{DROPOUT}$	Dropout voltage	V_{DD} = V_{SYS} > 2.8 V I_{OUT} = 300 mA (V_{DD} = 1.5 V, I_{OUT} = I_{MAX}/3)		100	150	mV
V_{S_LINE}	Static line regulation	V_{DD} = V_{SYS} = 3.0 V to 5.5 V I_{OUT} = 300 mA		2	10	mV
V_{S_LOAD}	Static load regulation	I_{OUT} = 1 mA to 300 mA		5	20	mV

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{TR_LINE}	Line transient response	V_{DD} = V_{SYS} = 3.0 V to 3.6 V I_{OUT} = 300 mA tr = tf = 10 µs		5	10	mV
V_{TR_LOAD}	Load transient response	V_{DD} = 3.6 V I_{OUT} = 1 mA to 300 mA tr = tf = 1 µs		30	50	mV
PSRR Note 3	PSRR	V_{DD} = 3.6 V I_{OUT} = I_{MAX}/2 V_{DD} – V_{LDO} ≥ 0.6 V, 25 °C				dB
		f = 10 Hz to 1 kHz,	70	80		
		f = 1 kHz to 10 kHz	60	70		
		f = 10 kHz to 100 kHz	40	50		
N	Output noise	V_{DD} = V_{SYS} = 3.6 V, V_{LDO} = 2.8 V I_{OUT} = 5 mA to I_{MAX} f = 10 Hz to 100 kHz, 25 °C		35		µV rms
I_{Q_ON}	Quiescent current in ON mode	Note 4		9 + 0.34 % of I_{OUT}		µA
I_{Q_SLEEP}	Quiescent current forced sleep mode			2 + 0.7 % of I_{OUT}		µA
I_{Q_OFF}	Quiescent current OFF mode			1		µA
t_{ON}	Turn-on time	10 % to 90 %			200	µs
		SLEEP mode			300	
t_{OFF}	Turn off time	90 % to 10 % Pull-down resistor enabled			1	ms
R_{OFF}	Pull-down resistance in OFF mode	Can be disabled via LDO10_PD_DIS		55		Ω

Note 1 Max output current is 30 % when the input voltage is 1.5 V.

Note 2 Programmable in 50 mV voltage steps.

Note 3 Measured at point of load.

Note 4 Internal regulator current flowing to ground.

5.8.11 LDO11

Table 23: LDO11, T_J = -40 ºC to +125 ºC

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage	V_{DD} = V_{SYS}	2.8		5.5	V
		If supplied from buck	1.5 Note 1			
V_{LDO}	Output voltage		0.9	Note 2	3.6	V
V_{LDO_ACC}	Output accuracy Note 3	V_{DD} = V_{SYS} = 2.8V to 5.5 V I_{OUT} = 200 mA Including static line/load regulation	-3		+3	%
C_{OUT}	Stabilization capacitor	Including voltage and temperature coefficient at configured VLDO11	-55 %	2.2	+35 %	µF
R_{COUT_ESR}	ESR of capacitor	f > 1 MHz Including track impedance	0		300	mΩ
I_{OUT_MAX}	Maximum output current	V_{DD} = V_{SYS} = 2.8 V to 5.5 V	300			mA
I_{SHORT}	Short circuit current			600		mA
I_{SLEEP}	Maximum sleep mode current	V_{DD} ≥ 1.8 V	30			mA
$V_{DROPOUT}$	Dropout voltage	V_{DD} = V_{SYS} > 2.8 V I_{OUT} = 300 mA (V_{DD} = 1.5 V, I_{OUT} = I_{MAX}/3)		100	150	mV
V_{S_LINE}	Static line regulation	V_{DD} = V_{SYS} = 2.8 V to 5.5 V V_{LDO} = 1.86 V I_{OUT} = 300 mA		2	15	mV
V_{S_LOAD}	Static load regulation	I_{OUT} = 1 mA to 300 mA		5	20	mV
V_{TR_LINE}	Line transient response	V_{DD} = V_{SYS} = 2.8 V to 5.5 V V_{LDO} = 1.86 V I_{OUT} = 300 mA tr = tf = 10 µs		5	10	mV
V_{TR_LOAD}	Load transient response	V_{DD} = 3.6 V I_{OUT} = 1 mA to 300 mA tr = tf = 1 µs		30	50	mV
PSRR Note 4	PSRR	f = 10 Hz to 10 kHz, 25 °C V_{DD} = 3.6 V, I_{OUT} = I_{MAX}/2 V_{DD} – V_{LDO} ≥ 0.6 V	60	70		dB
N	Output noise	V_{DD} = V_{SYS} = 3.6 V, V_{LDO} = 2.8 V I_{OUT} = 5 mA to I_{MAX} f = 10 Hz to 100 kHz, 25 °C		70		µV rms
I_{Q_ON}	Quiescent current in ON mode	Note 5		9 + 0.45 % of I_{OUT}		µA

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{Q_SLEEP}	Quiescent current forced sleep mode			2 + 0.7 % of I_{OUT}		µA
I_{Q_OFF}	Quiescent current OFF mode			1		µA
t_{ON}	Turn-on time	10 % to 90 %			200	µs
		SLEEP mode			260	
t_{OFF}	Turn off time	90 % to 10 % Pull-down resistor enabled			1	ms
R_{OFF}	Pull-down resistance in OFF mode	Can be disabled via LDO11_PD_DIS		55		Ω
Bypass Mode						
R_{ON}	Bypass on-resistance	V_{DD} > 2.2 V		0.3	0.7	Ω
		V_{DD} > 1.8 V			1.0	
I_{LIM}	Current limit in Bypass mode			270		mA
I_{Q_BYPASS}	Quiescent current in Bypass mode			50	100	µA

Note 1 Max output current is 30% when the input voltage is 1.5 V.

Note 2 Programmable in 50 mV voltage steps.

Note 3 Accuracy values not applicable if bypass mode has been configured.

Note 4 Measured at point of load.

Note 5 Internal regulator current flowing to ground.

5.8.12 LDOCORE

Table 24: LDOCORE, T_J = -40 °C to 125 °C

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DDCORE}	Output voltage	Note 1	2.45	2.5	2.55	V
		RESET mode		2.2		V
C_{OUT}	Stabilization capacitor	Including voltage and temperature coefficient	-55 %	2.2	+35 %	µF
R_{COUT_ESR}	Output capacitor ESR	f > 1 MHz Including wiring parasitics	0		300	mΩ
$V_{DROPOUT}$	Dropout voltage	Note 2		50	100	mV

Note 1 Setting VDD_FAULT_LOWER ≥ 2.65 V avoids LDOCORE dropout, see Section 5.14.

Note 2 The LDOCORE supply, VSYS or CHG_WAKE, must be maintained above V_{DDCORE} + $V_{DROPOUT}$.

Note
LDOCORE is only used to supply internal circuits.

5.9 DC/DC Buck Converters

5.9.1 BUCKCORE1 and BUCKCORE2

Table 25: BUCKCORE1, T_J = -40 °C to +125 °C

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage	V_{DD} = V_{SYS}	2.8		5.5	V
C_{OUT}	Output capacitor	Including voltage and temperature coefficient				µF
		Half-current mode	-50 %	2 x 22	+30 %, Note 1	
		Full-current mode		2 x 47		
R_{COUT_ESR}	Output capacitor ESR	Including wiring parasitics f > 100 kHz				mΩ
		Half-current mode C_{OUT} = 2 * 22 µF		15	50	
		Full-current mode C_{OUT} = 2 * 47 µF		7.5	25	
L_{BUCK}	Inductor value	Including current and temperature dependence	0.7	1.0	1.3	µH
L_{ESR}	Inductor resistance			55	100	mΩ
PWM Mode						
V_{BUCK}	Output voltage	Programmable in 10 mV steps Note 2	0.3		1.57	V
V_{BUCK_ACC}	Output voltage accuracy	Excluding static line/load regulation and voltage ripple T_A = 25 °C V_{DD} = 4.2 V V_{BUCK} = 1.03 V	-1		+1	%
		Excluding static line/load regulation and voltage ripple T_A = -40 °C to +85 °C V_{DD} = 4.2 V V_{BUCK} = 1.03 V	-1.5		+1.5	
		Including static line/load regulation and voltage ripple I_{OUT} = I_{MAX} V_{BUCK} = 1.03 V L_{BUCK}, L_{ESR} = Typ	-2		+2	

Parameter	Description	Conditions	Min	Typ	Max	Unit
		Including static line/load regulation and voltage ripple $I_{OUT} = I_{MAX}$ Note 3	-3		+3	
V_{TR_LD}	Transient load regulation	V_{DD} = 3.6 V V_{BUCK} = 1.2 V I_{OUT} = 200 mA / 0.8 * I_{MAX} dI/dt = 3 A/µs L_{BUCK} = 1.0 µH Note 4	-4		+4	%
V_{TR_LINE}	Transient line regulation	V_{DD} = 3.0 V to 3.6 V I_{OUT} = 500 mA tr = tf = 10 µs		0.2	3	mV
	Parasitic track resistance	From output capacitor to sense connection at point-of-load		10		mΩ
	Parasitic track inductance	From output capacitor to sense connection at point-of-load		5		nH
Z_{FB}	Feedback Comparator input impedance		500			kΩ
I_{MAX}	Output current	Half-current mode	1250			mA
		Full-current mode	2500			
I_{LIM} Note 5	Current limit (programmable)	BCORE1_ILIM=0000	-20 %	500	+20 %	mA
		BCORE1_ILIM=1111	-20 %	2000	+20 %	mA
I_{Q_OFF}	Quiescent current in OFF mode				1	µA
I_{Q_ON}	Quiescent current in PWM mode	Half-current mode I_{OUT} = 0 mA		9.0		mA
		Full-current mode		11.0		
f	Switching frequency Note 6	OSC_FRQ = 0000	2.85	3	3.15	MHz
D	Switching duty cycle		10.5		84	%
t_{ON}	Turn on time	V_{BUCK} = 1.15 V BUCK_SLOWSTART = disabled SLEW_RATE = 10 mV/1 µs BUCK<x>_ILIM = 1500 mA		0.37	1.2	ms
R_{PD}	Output pull-down resistor	V_{BUCK} = 0.5 V Can be disabled via BCORE1_PD_DIS		80	200	Ω

Parameter	Description	Conditions	Min	Typ	Max	Unit
R_{PMOS}	PMOS ON resistance	Half-current mode Including pin and routing V_{SYS} = 3.6 V		160		mΩ
		Full-current mode Including pin and routing V_{SYS} = 3.6 V		80		
R_{NMOS}	NMOS ON resistance	Half-current mode Including pin and routing V_{SYS} = 3.6 V		60		mΩ
		Full-current mode Including pin and routing V_{SYS} = 3.6 V		30		
η	Efficiency Note 7	V_{DD} = 3.6 V V_{BUCK} = 1.2 V I_{OUT} = 0.1 to 0.7 * I_{MAX}		84		%
PFM Mode						
V_{BUCK}	Output voltage	Programmable in 10 mV steps	0.3		1.57	V
I_{AUTO_THR}	Typical automatic mode switching current			260		mA
I_{OUT_PFM}	Output current			300		mA
I_{LIM_PFM}	Current limit			600		mA
I_{Q_PFM}	Quiescent current	I_{OUT} = 0				µA
		Forced PFM mode		27	32	
		AUTO mode		35	42	
	Frequency of operation		0		3	MHz
η	Efficiency Note 7	V_{DD} = 3.6 V V_{BUCK} = 1.2 V I_{OUT} = 10 mA		86		%

Note 1 The purpose of the specified maximum C_{OUT} value is to ensure that the specified turn-on time, t_{ON}, can be met. Additional output rail capacitors can be added to reduce voltage ripple or to improve transient load regulation. However, this will compromise t_{ON} performance, create larger in-rush currents and will affect DVC slew rates.

Note 2 If BUCK<x>_MODE = 10 (synchronous) then the buck operates in PFM mode when V_{BUCK} < 0.7 V. For complete control of the buck mode (PWM versus PFM) use BUCK<x>_MODE = 00.

Note 3 Minimum tolerance 35 mV.

Note 4 Measured at C_{OUT}, depends on parasitics of PCB and external components when remote sensing.

Note 5 Current limit values are doubled in full-current mode.

Note 6 Generated from internal 6 MHz oscillator and can be adjusted by ± 10 % via control OSC_FRQ.

Note 7 Depends on external components and PCB routing.

5.9.2 BUCKPRO

Table 26: BUCKPRO, T_J = -40 ºC to +125 ºC

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage	$V_{DD} = V_{SYS}$	2.8		5.5	V
C_{OUT}	Output capacitor	Including voltage and temperature coefficient				µF
		Half-current mode	-50 %	2 * 22	+30 %, Note 1	
		Full-current mode		2 * 47		
R_{COUT_ESR}	Output capacitor ESR	Including wiring parasitics f > 100 kHz				mΩ
		Half-current mode C_{OUT} = 2 * 22 µF		15	50	
		Full-current mode C_{OUT} = 2 * 47 µF		7.5	25	
L_{BUCK}	Inductor value	Including current and temperature dependence	0.7	1.0	1.3	µH
L_{ESR}	Inductor resistance			55	100	mΩ
PWM Mode						
V_{BUCK}	Output voltage	Programmable in 10 mV steps Note 2	0.53		1.8	V
V_{BUCK_ACC}	Output voltage accuracy	Including static line/load regulation and voltage ripple $I_{OUT} = I_{MAX}$ Note 3	-3		+3	%
		Excluding static line/load regulation and voltage ripple T_A = 25 °C V_{BUCK} > 1 V V_{DD} = 5 V	-1		+1	
V_{TR_LD}	Transient load regulation	V_{DD} = 3.6 V V_{BUCK} = 1.2 V I_{OUT} = 200 mA / 0.8 * I_{MAX} dI/dt = 3 A/µs L_{BUCK} = 1.0 µH Note 4		20	50	mV
V_{TR_LINE}	Transient line regulation	V_{DD} = 3.0 V to 3.6 V I_{OUT} = 500 mA tr = tf = 10 µs		0.2	3	mV
I_{MAX}	Output current	Half-current mode	1250			mA
		Full-current mode	2500			
I_{LIM}	Current limit	BPRO_ILIM=0000	-20 %	500	+20 %	mA

Parameter	Description	Conditions	Min	Typ	Max	Unit
Note 7	(programmable)	BPRO_ILIM=1111	-20 %	2000	+20 %	mA
I_{Q_OFF}	Quiescent current in OFF mode				1	µA
I_{Q_ON}	Quiescent current in PWM mode	Half-current mode		9.0		mA
		Full-current mode		11.0		
f	Switching frequency Note 5	OSC_FRQ = 0000	2.85	3	3.15	MHz
D	Switching duty cycle		10.6		84	%
R_{PD}	Output pull-down resistor	@ V_{OUT} = 0.5 V Can be disabled via BPRO_PD_DIS		80	200	Ω
R_{PMOS}	PMOS ON resistance	Half-current mode Including pin and routing V_{SYS} = 3.6 V		160		mΩ
		Full-current mode Including pin and routing V_{SYS} = 3.6 V		80		
R_{NMOS}	NMOS ON resistance	Half-current mode Including pin and routing V_{SYS} = 3.6 V		60		mΩ
		Full-current mode Including pin and routing V_{SYS} = 3.6 V		30		
η	Efficiency Note 6	V_{DD} = 3.6 V V_{BUCK} = 1.2 V I_{OUT} = 0.1 mA to 0.7 * I_{MAX}		84		%
PFM Mode						
V_{BUCK}	Output voltage	Programmable in 10 mV steps	0.53		1.8	V
I_{AUTO_THR}	Typical automatic mode switching current			260		mA
I_{OUT_PFM}	Output current			300		mA
I_{LIM}	Current limit			600		mA
I_{Q_PFM}	Quiescent current	I_{OUT} = 0 mA				µA
		Forced PFM mode		22	25	
		AUTO mode		30	35	
f	Frequency of operation		0		3	MHz
η	Efficiency Note 6	V_{DD} = 3.6 V V_{BUCK} = 1.2 V I_{OUT} = 10 mA		86		%
VTT Mode						
V_{DD}	Input voltage	V_{DD} = V_{SYS}	2.8		5.5	V

Parameter	Description	Conditions	Min	Typ	Max	Unit
C_{OUT}	Output capacitor	Including voltage and temperature coefficient	-50 %	2 * 47	+30 %, Note 1	µF
R_{COUT_ESR}	Output capacitor ESR	ESR of C_{OUT} @ f > 100 kHz + track impedance		7.5	25	mΩ
L_{BUCK}	Inductor value	Including current and temperature dependence		0.25		µH
L_{ESR}	Inductor resistance			55	100	mΩ
V_{BUCK}	Output voltage	$V_{BUCK} = V_{DDQ}/2$	0.675		1.3	V
V_{BUCK_ACC}	Output voltage accuracy	Relative to VTTR Including static line and load regulation	- 3		4	%
V_{TR_LD}	Transient load regulation	Half-current mode V_{DD} = 3.6 V V_{BUCK} = 0.7 V I_{OUT} = 10 mA to 1 A I_{OUT} = -750 mA to -10 mA L_{BUCK} = 0.24 µH dI/dt = 3 A/µs		20	40	mV
		Full-current mode V_{DD} = 3.6 V V_{BUCK} = 0.75 V I_{OUT} = 10 mA to 1.4 A I_{OUT} = -10 mA to -1.4 A L_{BUCK} = 0.24 µH dI/dt = 3 A/µs		20	40	
		Full-current mode V_{DD} = 3.6 V V_{BUCK} = 0.7 V I_{OUT} = 10 mA to 1.1 A I_{OUT} = -10 mA to -1.1 A L_{BUCK} = 0.24 µH dI/dt = 3 A/µs		20	40	
		Full-current mode V_{DD} = 3.6 V V_{BUCK} = 0.675 V I_{OUT} = 10 mA to 900 mA I_{OUT} = -10 mA to -900 mA L_{BUCK} = 0.24 µH dI/dt = 3 A/µs		20	40	
I_{MAX}	Maximum output current	Half-current mode V_{BUCK} = 0.7 V	-550		1250	mA
		Full-current mode V_{BUCK} = 0.75	-1400		2500	mA
		Full-current mode V_{BUCK} = 0.7 V	-1100		2500	
		Full-current mode V_{BUCK} = 0.675 V	-900		2500	

Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{ON}	Turn-on time	V_{BUCK} = 0.75 V BUCK_SLOWSTART = disabled SLEW_RATE = 10 mV/1 µs BUCK4_ILIM = 1500 mA		0.33	1.2	Ms
VTTR Buffer						
V_{DDQ}	Feedback voltage	V_{DD} = V_{SYS}	1.35		2.6	V
V_{VTTR}	Output voltage	I_{OUT} = 0 mA to I_{VTTR}	0.675	V_{DDQ}/2	1.3	V
V_{VTTR_ACC}	Voltage accuracy	V_{VTTR_ACC} related to V_{DDQ} input voltage	-1	V_{DDQ}/2	+1	%
C_{OUT}	Output capacitor	Including voltage and temperature coefficient	-50 %	0.1	+30 %	µF
I_{OUT}	Sink/source current		-10		10	mA

Note 1 The purpose of the specified maximum C_{OUT} value is to ensure that the specified turn-on time, t_{ON}, can be met. Additional output rail capacitors can be added to reduce voltage ripple or to improve transient load regulation. However, this will compromise t_{ON} performance, create larger in-rush currents and will affect DVC slew rates.

Note 2 If BUCK<x>_MODE = 10 (synchronous) then the buck operates in PFM mode when V_{BUCK} < 0.7 V. For complete control of the buck mode (PWM versus PFM) use BUCK<x>_MODE = 00.

Note 3 Minimum tolerance 35 mV.

Note 4 Measured at C_{OUT}, depends on parasitics of PCB and external components when remote sensing.

Note 5 Generated from internal 6 MHz oscillator and can be adjusted by ± 10 % via control OSC_FRQ.

Note 6 Depends on external components and PCB routing.

Note 7 Current limit values are doubled in full-current mode.

5.9.3 BUCKMEM

Table 27: BUCKMEM, T_J = -40 ºC to +125 ºC

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage	V_{DD} = V_{SYS}	2.8		5.5	V
C_{OUT}	Output capacitor	Including voltage and temperature coefficient	-50 %	2 * 22	+30 %, Note 1	µF
		Merged mode		2 * 47		
R_{COUT_ESR}	Output capacitor ESR	Including wiring parasitics f > 100 kHz				
		C_{OUT} = 2 * 22 µF		15	50	mΩ
		C_{OUT} = 2 * 47 µF		7.5	25	
L_{BUCK}	Inductor value	Including current and temperature dependence	0.7	1.0	1.3	µH
L_{ESR}	Inductor resistance			55	100	mΩ
V_{BUCK}	Output voltage	Programmable in 20 mV steps	0.8		3.34, Note 7	V
V_{BUCK_ACC}	Output voltage accuracy	Including static line/load regulation and voltage ripple I_{OUT} = I_{MAX} Note 2	-3		+3	%
		Excluding static line/load regulation and voltage ripple T_A = 25 °C V_{DD} = 5 V V_{BUCK} > 1 V	-2		+2	
V_{TR_LD}	Transient load regulation	V_{DD} = 3.6 V V_{BUCK} = 1.2 V I_{OUT} = 200 mA / 0.8 * I_{MAX} dI/dt = 3 A/µs Note 3	-4		+4	%
V_{TR_LINE}	Transient line regulation	V_{DD} = 3.0 V to 3.6 V I_{OUT} = 500 mA tr = tf = 10 µs		0.2	3	mV
I_{MAX}	Output current		1500			mA
I_{LIM} Note 4	Current limit (programmable)	BMEM_ILIM = 0000	-20 %	1500	+20 %	mA
		BMEM_ILIM = 1111	-20 %	3000	+20 %	mA
I_{Q_OFF}	Quiescent current in OFF mode				1	µA
I_{Q_ON}	Quiescent current in PWM mode	I_{OUT} = 0 mA		9		mA
f_{SW}	Switching frequency Note 5	OSC_FRQ = 0000	2.85	3	3.15	MHz

Parameter	Description	Conditions	Min	Typ	Max	Unit
D	Switching duty cycle		14.5		100	%
	Output pull-down resistor	V_{BUCK} = 0.5 V Disabled via BMEM_PD_DIS		80	200	Ω
R_{PMOS}	PMOS ON resistance	Including pin and routing V_{SYS} = 3.6 V		160		mΩ
R_{NMOS}	NMOS ON resistance	Including pin and routing V_{SYS} = 3.6 V		60		mΩ
η	Efficiency Note 6	V_{DD} = 3.6 V V_{BUCK} = 1.2 V I_{OUT} = 0.1 mA to 0.7 * I_{MAX}		83		%
PFM Mode						
V_{BUCK}	Output voltage	Programmable in 20 mV steps	0.8		3.34 Note 7	V
	Typical automatic mode switching current			260		mA
I_{MAX}	Output current			300		mA
I_{LIM}	Current limit			600		mA
I_{Q_PFM}	Quiescent current	I_{OUT} = 0 mA				µA
		Forced PFM mode		22	25	µA
		AUTO mode		30	35	µA
f	Frequency of operation		0		3	MHz
η	Efficiency Note 6	V_{DD} = 3.6 V V_{BUCK} = 1.2 V I_{OUT} = 10 mA		86		%

Note 1 The purpose of the specified maximum C_{OUT} value is to ensure that the specified turn-on time, t_{ON}, can be met. Additional output rail capacitors can be added to reduce voltage ripple or to improve transient load regulation. However, this will compromise t_{ON} performance, create larger in-rush currents and will affect DVC slew rates.

Note 2 Minimum tolerance 35 mV.

Note 3 Measured at C_{OUT}, depends on parasitics of PCB and external components when remote sensing.

Note 4 The current limits are automatically doubled when BUCKMEM is merged with BUCKIO.

Note 5 Generated from internal 6 MHz oscillator and can be adjusted by ± 10 % via control OSC_FRQ.

Note 6 Depends on external components and PCB routing.

Note 7 Maximum V_{DD} - 0.7 V.

5.9.4 BUCKIO

Table 28: BUCKIO, T_J = -40 ºC to +125 ºC

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage	V_{DD} = V_{SYS}	2.8		5.5	V
C_{OUT}	Output capacitor	Including voltage and temperature coefficient	-50%	2x22	+30%, Note 1	µF
R_{COUT_ESR}	Output capacitor ESR	f > 100 kHz All caps + track impedance		15	50	mΩ
L_{BUCK}	Inductor value	Including current and temperature dependence	0.7	1.0	1.3	µH
L_{ESR}	Inductor resistance			55	100	mΩ
PWM Mode						
V_{BUCK}	Output voltage	Programmable in 20 mV steps Note 2	0.8		3.34 Note 3	V
V_{BUCK_ACC}	Output voltage accuracy	Including static line/load regulation and voltage ripple @ I_{OUT} = I_{MAX}	-3	Note 4	+3	%
		T_A = 25 °C I_{OUT} = 0 V_{OUT} > 1 V V_{DD} = 5 V	-2		+2	
V_{TR_LD}	Transient load regulation	I_{OUT} = 200 mA/0.8 * I_{MAX} dI/dt = 3 A/µs	-4	Note 5	+4	%
V_{TR_LINE}	Transient line regulation	V_{DD} = 3.0 V to 3.6 V I_{OUT} = 500 mA tr = tf = 10 µs		0.2	3	mV
I_{MAX}	Output current		1500			mA
I_{LIM}	Current limit (programmable)	BIO_ILIM=0000	-20 %	1500	20 %	mA
		BIO_ILIM=1111	-20 %	3000	20 %	mA
I_{Q_OFF}	Quiescent current in OFF mode				1	µA
I_{Q_ON}	Quiescent current in PWM mode			9		mA
f_{SW}	Switching frequency		2.85	3	3.15	MHz
D	Switching duty cycle		14.5		100	%
	Output pull-down resistor	V_{OUT} = 0.5 V Can be disabled via BIO_PD_DIS		80	200	Ω
R_{PMOS}	PMOS ON resistance	Including pin and routing V_{SYS} = 3.6 V		160		mΩ

Parameter	Description	Conditions	Min	Typ	Max	Unit
R_{NMOS}	NMOS ON resistance	Including pin and routing V_{SYS} = 3.6 V		60		mΩ
η	Efficiency Note 6	V_{DD} = 3.6 V V_{BUCK} = 1.8 V I_{OUT} = 0.1 to 0.7 * I_{MAX}		87		%
PFM Mode						
	Typical automatic mode switching current			260		mA
I_{MAX}	Output current			300		mA
I_{LIM}	Current limit			600		mA
I_{Q_PFM}	Quiescent current	I_{OUT} = 0 mA				µA
		Forced PFM mode		22	25	
		AUTO mode		30	35	
f	Frequency of operation		0		3	MHz
η	Efficiency Note 6	V_{DD} = 3.6 V V_{BUCK} = 1.8 V I_{OUT} = 10 mA		90		%

Note 1 The purpose of the specified maximum C_{OUT} value is to ensure that the specified turn-on time, t_{ON}, can be met. Additional output rail capacitors can be added to reduce voltage ripple or to improve transient load regulation. However, this will compromise t_{ON} performance, create larger in-rush currents and will affect DVC slew rates.

Note 2 If BUCK<x>_MODE = 10 (synchronous) then the buck operates in PFM mode when V_{BUCK} < 0.7 V. For complete control of the buck mode (PWM versus PFM) use BUCK<x>_MODE = 00.

Note 3 Maximum V_{DD} - 0.7 V.

Note 4 Minimum tolerance 35 mV.

Note 5 Measured at C_{OUT}, depends on parasitics of PCB and external components when remote sensing.

Note 6 Depends on external components and PCB routing.

5.9.5 BUCKPERI

Table 29: BUCKPERI, T_J = -40 ºC to +125 ºC

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage	$V_{DD} = V_{SYS}$	2.8		5.5	V
C_{OUT}	Output capacitor	Including voltage and temperature coefficient	-50 %	2 x 22	+30 %, Note 1	µF
R_{COUT_ESR}	Output capacitor ESR	f > 100 kHz All caps + track impedance		15	50	mΩ
L_{BUCK}	Inductor value	Including current and temperature dependence	0.7	1.0	1.3	µH
L_{ESR}	Inductor resistance			55	100	mΩ
V_{BUCK}	Output voltage	Programmable in 20 mV steps Note 2	0.8		3.34 Note 3	V
V_{BUCK_ACC}	Output voltage accuracy	Including static line/load regulation and voltage ripple $I_{OUT} = I_{MAX}$	-3	Note 4	+3	%
		T_A = 25 °C I_{OUT} = 0 V_{OUT} > 1 V V_{DD} = 5 V	-2		+2	
V_{TR_LD}	Transient load regulation	I_{OUT} = 200 mA/0.8 * I_{MAX} dI/dt = 3 A/µs	-4	Note 5	+4	%
V_{TR_LINE}	Transient line regulation	V_{DD} = 3.0 V to 3.6 V I_{OUT} = 500 mA tr = tf = 10 µs		0.2	3	mV
I_{MAX}	Output current		1500			mA
I_{LIM}	Current limit (programmable)	BPERI_ILIM = 0000	-20%	1500	+20%	mA
		BPERI_ILIM = 1111	-20%	3000	+20%	mA
I_{Q_OFF}	Quiescent current in OFF mode			1	µA	
I_{Q_ON}	Quiescent current in PWM mode			9		mA
f_{SW}	Switching frequency		2.85	3	3.15	MHz
D	Switching duty cycle		14.5		100	%
	Output pull-down resistor	V_{OUT} = 0.5 V Can be disabled via BPERI_PD_DIS		80	200	Ω
R_{PMOS}	PMOS ON resistance	Including pin and routing V_{SYS} = 3.6 V		160		mΩ
R_{NMOS}	NMOS ON resistance	Including pin and routing V_{SYS} = 3.6 V		60		mΩ

Parameter	Description	Conditions	Min	Typ	Max	Unit
η	Efficiency Note 6	V_{DD} = 3.6 V V_{BUCK} = 2.86 V I_{OUT} = 0.1 to 0.7 * I_{MAX}		91		%
PFM Mode						
	Typical automatic mode switching current			260		mA
I_{MAX}	Output current			300		mA
I_{LIM}	Current limit			600		mA
I_{Q_PFM}	Quiescent current	I_{OUT} = 0 mA				µA
		Forced PFM mode		22	25	µA
		AUTO mode		30	35	µA
f	Frequency of operation		0		3	MHz
η	Efficiency Note 6	V_{DD} = 3.6 V V_{BUCK} = 2.86 V I_{OUT} = 10 mA		93		%

Note 1 The purpose of the specified maximum C_{OUT} value is to ensure that the specified turn-on time, t_{ON}, can be met. Additional output rail capacitors can be added to reduce voltage ripple or to improve transient load regulation. However, this will compromise t_{ON} performance, create larger in-rush currents and will affect DVC slew rates.

Note 2 If BUCK<x>_MODE = 10 (synchronous) then the buck operates in PFM mode when V_{BUCK} < 0.7 V. For complete control of the buck mode (PWM versus PFM) use BUCK<x>_MODE = 00.

Note 3 Maximum V_{DD} - 0.7 V.

Note 4 Minimum tolerance 35 mV.

Note 5 Measured at C_{OUT}, depends on parasitics of PCB and external components when remote sensing.

Note 6 Depends on external components and PCB routing.

5.9.6 Typical Characteristics

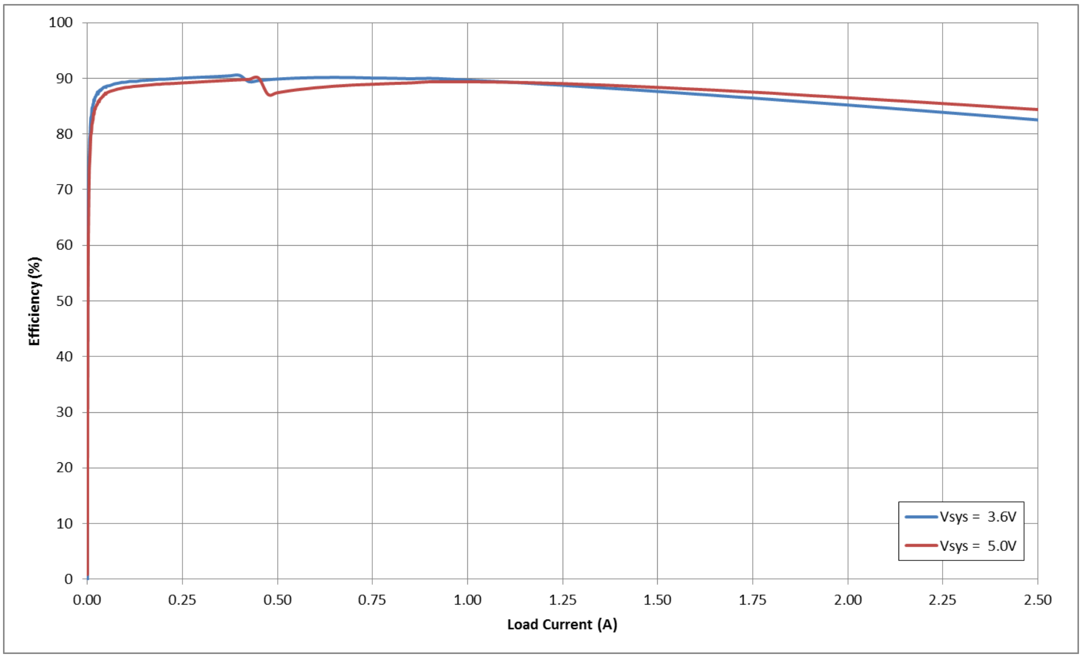


Figure 7: BUCKCORE1 Efficiency in AUTO Mode, V_{OUT} = 1.2 V

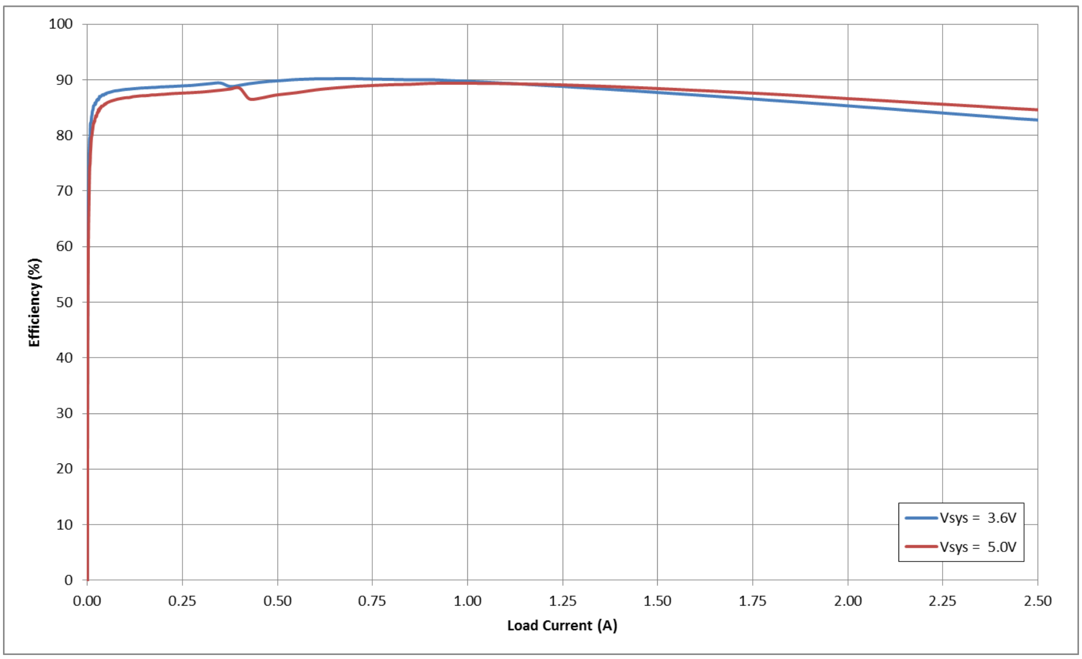


Figure 8: BUCKCORE2 Efficiency in AUTO Mode, V_{OUT} = 1.2 V

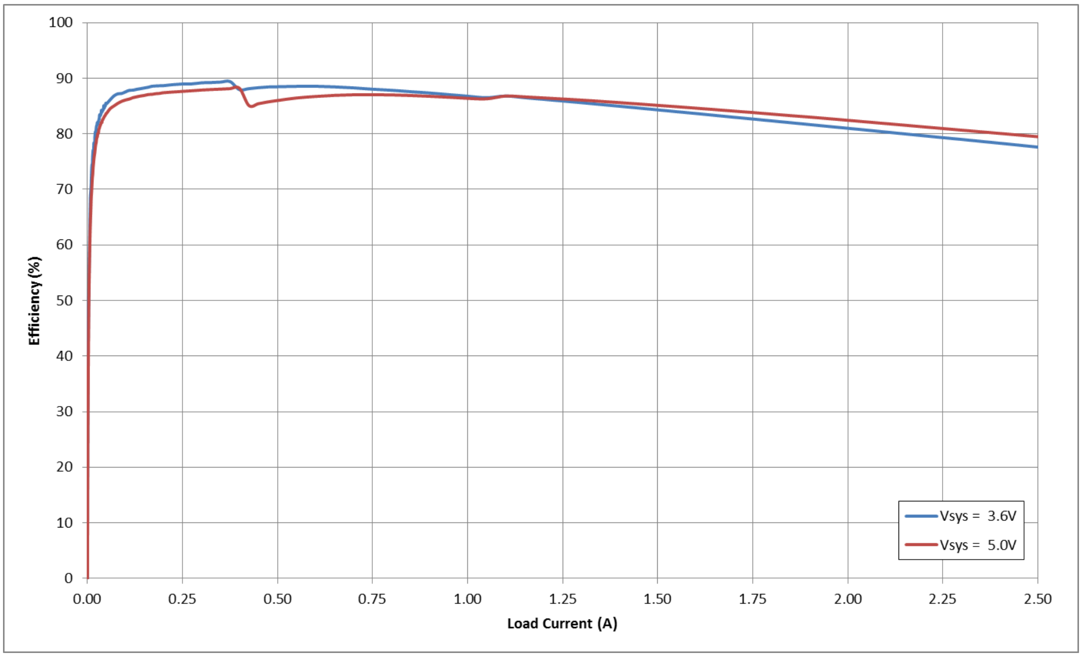


Figure 9: BUCKPRO Efficiency in AUTO Mode, V_{OUT} = 1.2 V

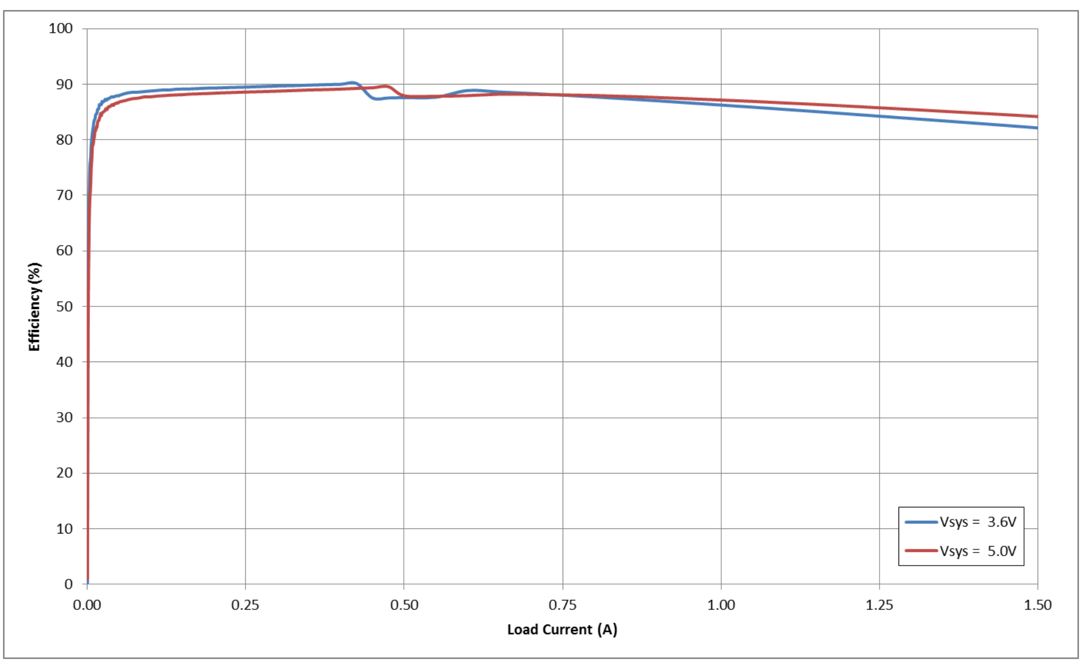


Figure 10: BUCKMEM Efficiency in AUTO Mode, V_{OUT} = 1.2 V

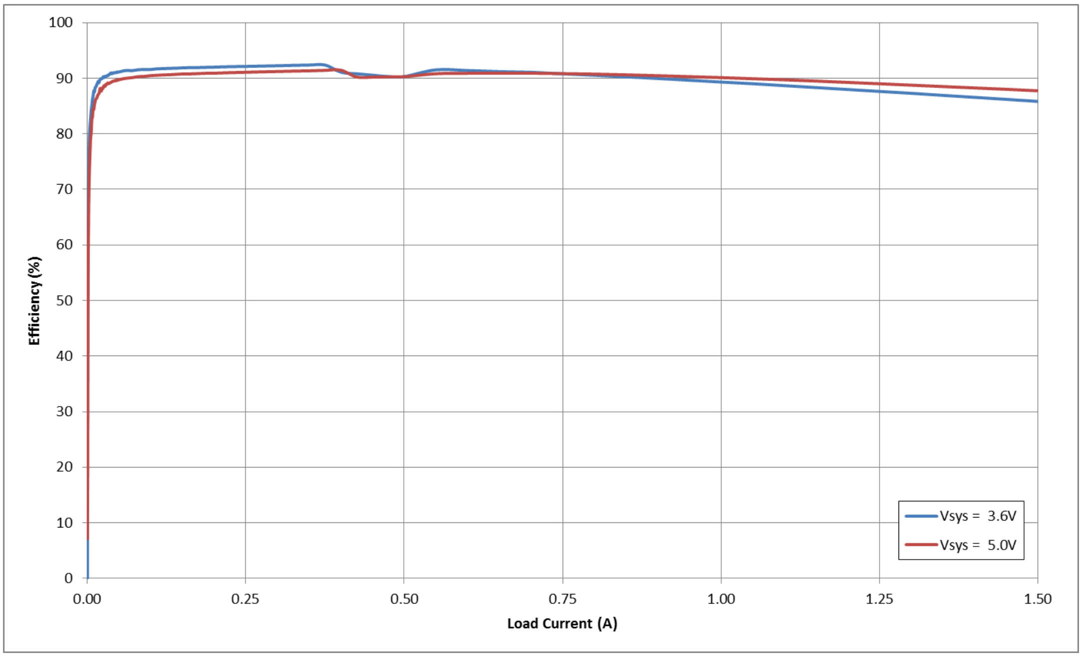


Figure 11: BUCKIO Efficiency in AUTO Mode, V_{OUT} = 1.8 V

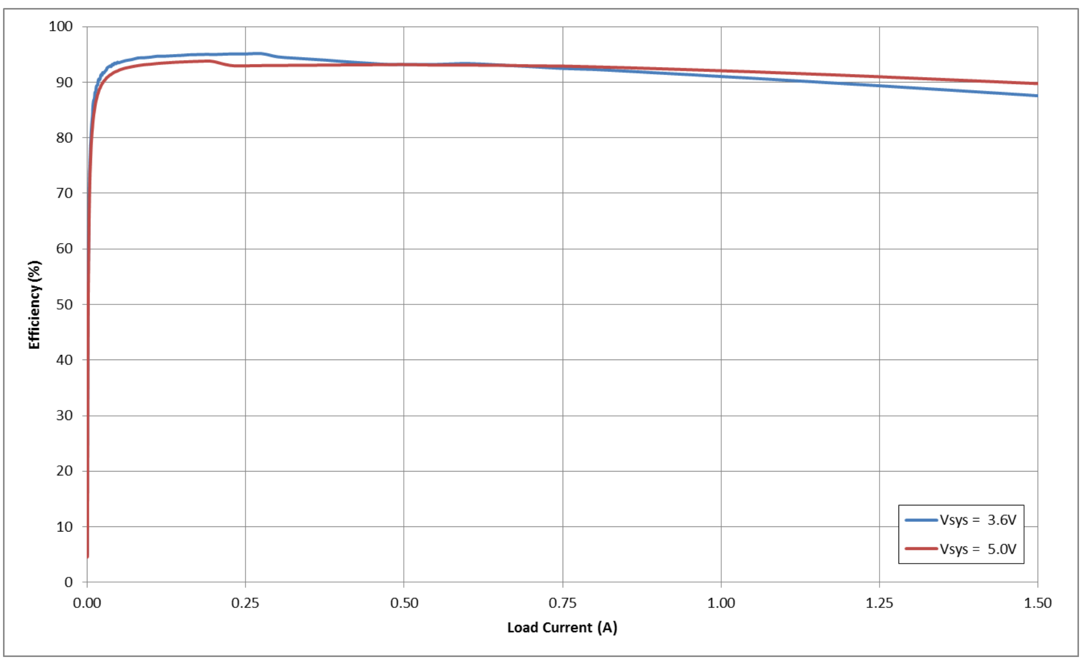


Figure 12: BUCKPERI Efficiency in AUTO Mode, V_{OUT} = 2.86 V

5.10 Buck Rail Switches

Table 30: Buck Rail Switches, T_J = -40 ºC to +125 ºC

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	Input voltage	V_{DD} = VDDCORE	2.45	2.5	2.55	V
C_{OUT}	Output capacitor	Including voltage and temperature coefficient	-30%	47		nF
V_CP	Output voltage	I_{OUT} = 10 µA	4.5	4.6		V
t_{ON}	Charge pump turn on time	20 to 80% of V_CP			0.6	ms
V_{BUCK}	NMOS input voltage				2.8	V
	Gate driver source current	Vgate = 4.4 V			5	µA
	Gate driver sink current	Vgate = 0.5 V			180	µA
	Voltage slew rate		1	1 Note 1	50	mV/µs
	Output pull-down resistor	@ V_{OUT} = 0.1 V		370		Ω

Note 1 OTP programmable via SWITCH_SR (register SWITCH_CONT).

5.11 Backup Battery Charger

Table 31: Backup Battery Charger, T_J = -40 ºC to +125 ºC

Parameter	Description	Conditions	Min	Typ	Max	Unit
BCHG_ISET	Backup battery charging current	V_{SYS} = 3.6 V, V_{BBAT} = 2.5 V	100	Note 1	6000	µA
BCHG_VSET	Charger termination voltage	V_{SYS} = 3.6 V	1.1	Note 2	3.1	V
	Backup battery short circuit current	V_{BBAT} = 0 V		6.8		mA
C_{OUT}	Stabilization capacitor		-55%	470	+35%	nF
R_{COUT_ESR}	ESR of capacitor	f > 1 MHz			100	mΩ
$V_{DROPOUT}$	Dropout voltage	I_{OUT} = 5 mA		150	200	mV
I_Q	Quiescent current	I_{OUT} > 50 µA		5.25+1.75% of I_{OUT}		µA
		I_{OUT} < 50 µA		5.25+1.5% of I_{OUT}		µA

Note 1 Programmable in 100 µA increments from 100 µA to 1000 µA and 1 mA increments from 1 mA to 6 mA.

Note 2 Programmable in steps of 100 mV /200 mV.

5.12 General Purpose ADC

Table 32: General Purpose ADC, T_J = -40 ºC to +125 ºC

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DD}	ADC reference voltage	V_{DD} = VDDCORE	2.45	2.5	2.55	V
	Off current				1	µA
	ADC resolution			10		bit
	ADC integral non linearity			± 2		LSB
	ADC differential non linearity			± 0.8		LSB
	ADC absolute accuracy	Note 4		13	15	mV
R_{SRC} Note 1	Maximum source impedance				120	kΩ
C_{IN}	Input capacitance	Total input capacitance		10.5		pF
	V_{SYS} voltage range Channel 0	V_{SYS} minus VDDCORE V_{SYS} = 3.125*(ADC/255)+2.5 (Auto) V_{SYS} = 3.125*(ADC/1023)+2.5 (Man)	2.5		5.5	V
	ADCIN1 to 3 voltage range Channel 1 to 3	V_{IN} = (ADC*2.5)/255 (Auto) V_{IN} = (ADC*2.5)/1023 (Man)	0		2.5	V
	Internal temperature sensor voltage range Channel 4	T_J = -0.398 * ADC +330	0		0.833	V
	V_{BBAT} voltage range Channel 5	V_{BBAT} = (ADC*5)/1023	0		5.0	V
	Regulator monitor voltage range Channel 8 to 10	V_{REG} = (ADC*5)/255	0		5.0	V
	Inter channel isolation	Note 2		60		dB
	ADCIN1,2 current source Note 3		-3%	1-40	3%	µA
	COMP1V2 comparator level Channel 2			1.2		V

Note 1 R_{SRC} is the impedance of the external source the ADC is sampling.

Note 2 80 dB for channel A2 (ADC_IN2).

Note 3 Variance guaranteed for 10 µA to 40 µA and up to 2 V output voltage.

Note 4 Excludes reference voltage variation.

5.13 32 kHz Oscillator

Table 33: 32 kHz Oscillator, T_J = -40 ºC to 125 ºC

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DDRTC}	Supply voltage		1.5		2.75	V
f_{OSC}	Oscillator crystal frequency			32.768		kHz
R_{OSC}	Crystal series resistance				100	kΩ
f_{OUT}	Output frequency			32.768		kHz
T_{START}	Start-up time for cell over the voltage range	V_{BBAT} = 1.5 V to 2.75 V		0.5	2.0	s
	Current consumption from backup device during RTC mode			0.5		µA
	Current consumption from V_{DDREF} with OUT_32K enabled			8		µA
	Cycle-to-cycle jitter (rms)	1000 pulse		20	35	ns
	Period jitter (rms)	10000 pulse		12	20	
Bypass Mode						
F_{IN}	Input frequency		-5%	32	+5%	kHz
D	Input duty cycle		40		60	%
V_{IH}	XTAL_IN Input high voltage	RTC_EN = 0	1.8		V_{SYS}	V
		RTC_EN = 1 $V_{BBAT} < V_{SYS}$	1.1			
		RTC_EN = 1 $V_{BBAT} > V_{SYS}$	0.7 * V_{BBAT}		V_{BBAT}	
V_{IL}	XTAL_OUT Input low voltage	RTC_EN = 0	-0.3		0.6	V
		RTC_EN = 1 $V_{BBAT} < V_{SYS}$			0.4	
		RTC_EN = 1 $V_{BBAT} > V_{SYS}$			0.2 * V_{BBAT}	
SR	Input slew rate	2 pF input capacitance	0.1			V/ns

5.14 Internal Oscillator

Table 34: Internal Oscillator, T_J = -40 ºC to +125 ºC

Parameter	Description	Conditions	Min	Typ	Max	Unit
f_{OSC}	Internal oscillator frequency	OSC_FRQ = 0000	5.7	6.0	6.3	MHz

Note 1 Oscillator frequency can be further adjusted by about ±10 %, see Section 6.15.

5.15 POR, Reference Generation, and Voltage Supervision

Table 35: POR, Reference Generation and Voltage/Temperature Supervision, T_J = -40 ºC to +125 ºC

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{POR_LOWER}	Deep discharge lockout lower threshold			2.0		V
V_{POR_UPPER}	Deep discharge lockout upper threshold			2.3		V
$V_{DD\_FAULT\_LOWER}$ Note 1	Under-voltage lower threshold		2.5	2.8	3.25	V
$V_{DD\_FAULT\_LOWER\_ACC}$	Under-voltage lower threshold accuracy			±2		%
$V_{DD\_FAULT\_UPPER}$ Note 2	Under-voltage upper threshold			$V_{DD\_FAULT\_LOWER}$ + VDD_HST_ADJ		V
V_{REF}	Reference voltage		-1.25%	1.2	+1%	V
VREF decoupling capacitor				0.22		µF
VLNREF decoupling capacitor				0.22		µF
I_{REF}	Reference current resistor		-1%	200	+1%	kΩ

Note 1 During production $V_{DD\_FAULT\_LOWER}$ voltage is configured via OTP over the range 2.5 V to 3.25 V in 50 mV steps.

Note 2 During production the hysteresis between $V_{DD\_FAULT\_LOWER}$ and $V_{DD\_FAULT\_UPPER}$ is configured via OTP over the range 100 mV to 450 mV in 50 mV steps, the hysteresis can be further changed through control VDD_HYST_ADJ.

5.16 Thermal Supervision

Parameter	Description	Conditions	Min	Typ	Max	Unit
TEMP_WARN	Thermal warning	Note 1	120	125	130	°C
TEMP_CRIT	Thermal shutdown	Note 1	135	140	145	°C
TEMP_POR	Thermal POR threshold	Note 1	145	150	155	°C

Note 1 Thermal thresholds are non-overlapping.

6 Functional Description

The DA9063 provides separate power domains for the host processor, memory, and peripherals to enable a flexible low-power system design. Multiple low-power modes permit varying combinations of peripherals to be powered off to conserve battery power. Other system components, such as DRAM and FLASH memory, RF transceivers, audio codec, and companion chips, are supplied from optimized regulators designed for dedicated power requirements. The DA9063 power supplies can be programmed to default voltages via OTP and provide system-configuration flexibility by selecting the power-up sequence of the regulators and switching converters.

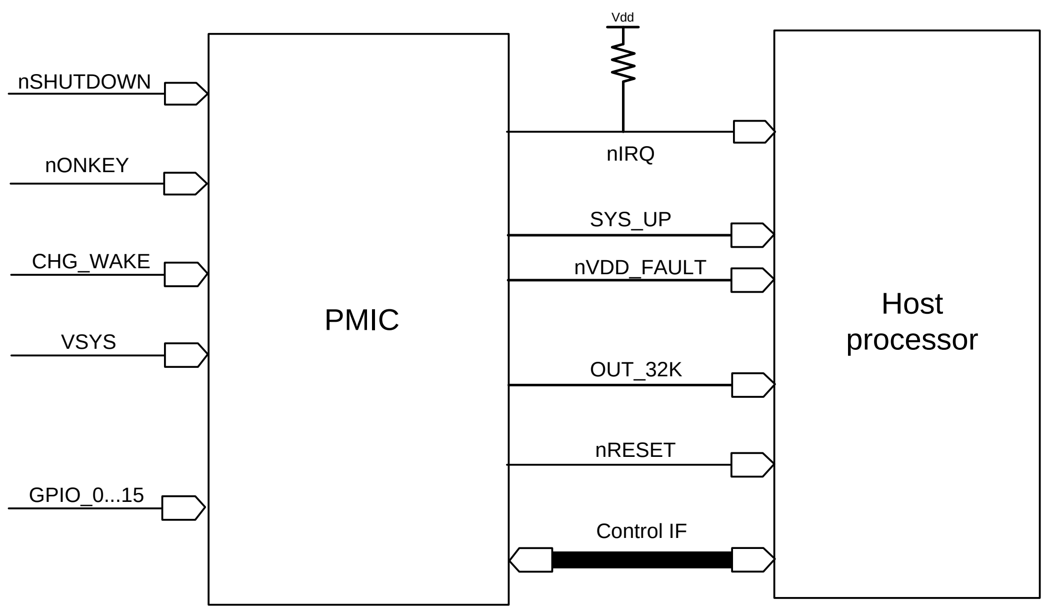


Figure 13: Control Ports and Interface

6.1 Power Manager IO Ports

The power manager input ports are supplied from either the internal rail VDDCORE or VDD_IO2, selected via PM_I_V. The output ports are supplied from VDD_IO1 or VDD_IO2, selected via PM_O_V (nVDD_FAULT, GP_FB1 via GPIO controls). During the initial start-up sequence all power manager IO ports (with the exception of nRESET and nIRQ) are in a high impedance (tri-state) mode until they are configured from OTP prior to reaching POWERDOWN mode. Output ports are push-pull except for nRESET and nIRQ, which can also be configured as open-drain via PM_O_TYPE. The nONKEY and CHG_WAKE signals for the RTC block are supplied from V_{DDREF}.

6.1.1 On/Off Port (nONKEY)

The nONKEY signal is a wake-up interrupt/event intended to power-on the application supplied by DA9063. The level of the debounced signal is provided by status flag nONKEY (asserted at low level). The nONKEY unit is always enabled so that the application can be powered-on when the GPIO extender is disabled. The IRQ assertion and wake-up event can be suppressed via the interrupt mask M_nONKEY.

nONKEY provides four modes of operation selected by field nONKEY_PIN in register CONFIG_I.

Table 36: nONKEY_PIN Settings

nONKEY_PIN	Description
00	An E_nONKEY event is generated when the debounced signal from port nONKEY goes low (asserting edge). If not masked, an interrupt is signaled to the host via nIRQ (with wake-up during POWERDOWN mode).
01	If (after powering up from POWERDOWN mode) the debounced signal from port nONKEY is low after an asserting edge for less than the key-press time (selected by KEY_DELAY, default 2 s), an E_nONKEY event is generated at the releasing edge. If the signal is low for longer than selected by KEY_DELAY, the DA9063 asserts the event E_nONKEY plus control nONKEY_LOCK when it reaches the selected key-press time.
10	If (after powering up from POWERDOWN mode) the debounced signal from port nONKEY is low after an asserting edge for less than the key-press time (selected by KEY_DELAY, default 2 s), an E_nONKEY event is generated at the releasing edge. If the signal is low for longer than selected by KEY_DELAY, the DA9063 asserts the event E_nONKEY plus control nONKEY_LOCK when it reaches the selected key-press time and powers down by clearing control SYSTEM_EN.
11	If (after powering up from POWERDOWN mode) the debounced signal from port nONKEY is low after an asserting edge for less than the key-press time (selected by KEY_DELAY, default 2 s), an E_nONKEY event is generated at the releasing edge. Control SYSTEM_EN is cleared and STANDBY asserted, which triggers a partial power down from a short press. If the signal is low for longer than selected by KEY_DELAY, the DA9063 asserts the event E_nONKEY plus control nONKEY_LOCK and clear SYSTEM_EN plus STANDBY when it reaches the selected pressing time (powers down to full POWERDOWN from a long press).

For nONKEY_PIN settings other than ‘00’, the wake-up is not suppressed by an asserted M_nONKEY. With an asserted nONKEY_LOCK, the wake-up is only executed if the debounced nONKEY signal is asserted for more than the key-press time (selected by KEY_DELAY, default 2 s). This behaves similarly to a keypad lock since any short (unintended) pressing of nONKEY does not wake the application. If the application also has wake-up from a short nONKEY press, the host has to clear nONKEY_LOCK before entering POWERDOWN mode. In mode ‘10’ when nONKEY key press is longer than the time selected by KEY_DELAY, SYSTEM_EN is re-asserted in mode ‘11’. SYSTEM_EN is re-asserted from any consecutive pressing of nONKEY. nONKEY_LOCK is automatically cleared by the DA9063 when powering up from POWERDOWN mode. POWERDOWN mode is described in Section 6.2.2.

Note
During RTC/DELIVERY-MODE, the functionality of nONKEY is restricted to a termination of this mode. To enable this feature, the pull-up resistor of nONKEY has to be connected to V_{SYS}. Asserting nONKEY stops the RTC/DELIVERY-MODE and triggers a start-up of the DA9063.

6.1.2 Wake-up Port (CHG_WAKE)

The CHG_WAKE signal is a rising edge sensitive, wake-up interrupt/event intended to wake the DA9063 from an event on the companion charger (for example, supply insertion). The CHG_WAKE port is always enabled so that the application can be powered-on with a disabled GPIO extender. The IRQ assertion and wake-up event can be suppressed via the interrupt mask M_WAKE. During RTC/DELIVERY mode, asserting CHG_WAKE terminates this mode.

6.1.3 Hardware Reset (nOFF, nSHUTDOWN, nONKEY, GPIO14, GPIO15, WATCHDOG)

The DA9063 nOFF port is an active-low input (no debouncing) typically initiated by an asserted error detection line. It asserts nSHUTDOWN in the fault register. The sequencer asserts port nRESET, and all domains and supplies of the DA9063 except LDOCORE (and possibly LDO1) are disabled in a fast emergency shutdown.

The DA9063 nSHUTDOWN port is an active-low input typically asserted from a host processor (or a push button switch). It asserts nSHUTDOWN in the fault register. The sequencer asserts port nRESET and then powers down all domains in reverse sequencer order down to slot 0 and all supplies of the DA9063 except LDOCORE (and possibly LDO1) are disabled. HOST_SD_MODE determines if normal power sequence timing or a fast shutdown is implemented.

The DA9063 includes a third hardware reset trigger that follows the debounced nONKEY signal after being asserted for a period greater than KEY_DELAY + SHUT_DELAY. The same can be achieved by a long parallel connection of GPI14 and GPI15 to ground. The long nONKEY shutdown and GPIO14/15 shutdown are enabled by the power manager control register bits nONKEY_SD and GPI14_15_SD.

If the hardware reset was initiated by a (debounced) press of nONKEY (or GPIO14 and GPIO15 together) longer than SD_DELAY, the DA9063 initially only asserts control bit KEY_RESET in the fault register and signals a non-maskable interrupt allowing the host to clear the armed reset sequence within 1 s. If the host does not clear KEY_RESET then a shutdown to RESET mode is executed. KEY_SD_MODE determines if normal power sequence timing or a fast shutdown is implemented.

The DA9063 then waits for a valid wake-up event (for example, a key press) or starts the power sequencer automatically if AUTO_BOOT is configured.

If the WATCHDOG has been disabled, this hardware reset can be used to turn off the application in the event of a software lock-up without removing the battery. This type of reset should only be used for severe hardware or software problems as it will completely reset the processor and could result in data loss.

6.1.4 Reset Output (nRESET)

The nRESET signal is an active-low output signal from DA9063 to the host processor that can either be push-pull or open drain (selected via PM_O_TYPE), which tells the host to enter the reset state. nRESET is always asserted at the beginning of a DA9063 cold start from NO-POWER, DELIVERY, and RTC modes. It is asserted in ACTIVE mode before the DA9063 starts powering down to RESET mode (triggered from user, host, or an error condition detected by the DA9063). nRESET may also be asserted (depending on nRES_MODE setting) as a soft reset before the sequencer starts powering down without progressing to RESET mode.

An assertion of nRESET from voltage supervised regulators being out-of-range can be enabled via control MON_RES (minimum assertion time 1 ms).

After being asserted, nRESET remains low until the reset timer has been started from the selected trigger signal and expires. The reset release timer trigger signal can be selected via RESET_EVENT to be EXT_WAKEUP, SYS_UP, PWR_UP, or leaving PMIC RESET state. The expiry time can be configured via RESET_TIMER from 1 ms to 1 s.

6.1.5 System Enable (SYS_EN)

SYS_EN is an input signal from the host processor to the DA9063 that enables the regulators in domain SYSTEM. The feature is enabled using GPIO8_PIN and configured as active-low or -high by GPIO8_TYPE. It asserts SYSTEM_EN and simultaneously generates an IRQ. It also triggers a wake-up event in POWERDOWN mode if enabled via GPIO8_WEN. De-asserting SYS_EN (changing from active to passive state) clears control SYSTEM_EN which triggers a power down sequence into hibernate/standby mode (without IRQ assertion or wake-up event trigger). By setting nRES_MODE, the port SYS_EN can be used as a soft reset input with the assertion of nRESET before powering down. With the exception of supplies that have the xxxx_CONF control bit asserted, all regulators in power domains POWER1, POWER, and SYSTEM are sequentially disabled in reverse order. Regulators with the <x>_CONF bit set remain on but change the active voltage control registers from V<x>_A to V<x>_B (if V<x>_B is not already selected).

The control register bit SYSTEM_EN can also be used to power down domain SYSTEM by a software command. It can be read and changed via the control interfaces and can be initialized from OTP when leaving POWERDOWN mode. The DA9063 will not process any changes on port SYS_EN or register control SYSTEM_EN until the sequencer has stopped processing IDs.

6.1.6 Power Enable (PWR_EN)

PWR_EN is an input signal from the host processor to the DA9063. The input signal can be configured as active-high or -low via GPIO9_TYPE, and to trigger a wake-up event from POWERDOWN mode if configured via GPIO9_WEN. Initialization, IRQ assertion and the direct control via register bit POWER_EN is similar to the function of SYS_EN in domain SYSTEM as described in Section 6.1.5. To ensure correct sequencing, SYSTEM_EN (SYS_EN) must be active before asserting PWR_EN/POWER_EN. When de-asserting PWR_EN/POWER_EN, the sequencer sequentially powers down POWER1 and POWER domains.

6.1.7 Power1 Enable (PWR1_EN)

PWR1_EN is an input signal from a host to the DA9063. The input signal can be configured as active-high or -low via GPIO10_TYPE, and to trigger a wake-up event in POWERDOWN mode if enabled via GPIO10_WEN. Initialization, IRQ assertion and the direct control via register bit POWER1_EN is similar to the function of SYS_EN in domain SYSTEM as described in Section 6.1.5. POWER1 is a general purpose power domain.

6.1.8 GP_FB1, General Purpose Signal 1 (EXT_WAKEUP/READY)

This port supports two different modes selected by the control PM_FB1_PIN.

Table 37: PM_FB1_PIN Settings

PM_FB1_PIN	Description
0	EXT_WAKEUP. This output signal to the host processor indicates a valid wake-up event during POWERDOWN mode. External signals that can trigger wake-up events are debounced before the EXT_WAKEUP signal is asserted. EXT_WAKEUP is released when register control SYSTEM_EN is asserted (minimum pulse duration = 500 µs).
1	READY. The READY signal indicates on-going DVC or power sequencer activities. The READY signal is asserted (typically active-low) from the DA9063 power sequencer when the processing of IDs commences, and is released when the target power state (final sequencer slot) has been reached. READY is also asserted during DVC voltage transitions.

The active level is configured via the control GPIO13_MODE. The logical threshold voltage is selected by GPIO13_TYPE.

6.1.9 GP_FB2, General Purpose Signal 2 (PWR_OK/KEEP_ACT)

The GP_FB2 port supports two different modes selected by the control PM_FB2_PIN.

Table 38: PM_FB2_PIN Settings

PM_FB2_PIN	Description
0	PWR_OK. In this mode the port is a regulator status indicator. The port is an open drain output asserted if none of the selected regulators are out-of-range. The regulator monitoring via ADC must be enabled and all regulators to be monitored must have supervision enabled with the selected persistence, and mask bit M_REG_UVOV must be asserted. In case at least one of the supervised regulators is out-of-range or regulator monitoring is disabled, the PWR_OK signal is low.
1	KEEP_ACT. If enabled, every assertion of the port (rising to active level edge sensitive) sets the watchdog trigger, similar to writing to bit WATCHDOG via the power manager bus. The host has to release KEEP_ACT before the next assertion during continuous watchdog supervision (if enabled). The minimum assertion and de-assertion cycle time is 150 µs.

The output active level (and driver type) can be configured via GP_FB2_TYPE.

Alternatively, with BCORE_MERGE = 1, FB in register BCORE1_CFG set to 0b000 and MERGE_SENSE = 0, the GP_FB2 pin becomes a voltage feedback signal for BUCKCORE.

6.1.10 GP_FB3, General Purpose Signal 3 (OUT32K_2/nVIB_BRAKE)

The GP_FB3 port supports two different modes selected by the control PM_FB3_PIN.

Table 39: PM_FB3_PIN Settings

PM_FB3_PIN	Description
0	OUT32K_2. This provides a second 32K signal output (push-pull).
1	nVIB_BRAKE. If LDO8 is configured as a vibrator motor driver, GP_FB3 can be configured to provide an external brake signal. The vibrator motor can be started or stopped by a change in the level on the nVIB_BRAKE signal. If the port is not used as a brake command, the vibration motor runs continuously at the speed configured by VIB_SET.

GP_FB3_TYPE defines the active level.

6.1.11 Supply Rail Fault (nVDD_FAULT)

nVDD_FAULT gives the status of the system supply monitoring, see Section 6.18. The assertion of nVDD_FAULT indicates that the main supply input voltage has been low ($V_{SYS} < V_{DD\_FAULT\_LOWER}$) for more than 100 ms and informs the host processor that the power will shut down. It can be configured to drive a GPO from the GPIO<x>_OUT controls. The driver type (push-pull, open-drain) selection and pull-up resistor control function normally. The GPIO<x>_MODE can be used to invert the incoming nVDD_FAULT signal.

The nVDD_FAULT port can alternatively be controlled by the state of the debounced V_{SYS} monitor inside the ADC (selected via GPIO12_PIN). The signal is asserted when the ADC detects three consecutive results below the configurable threshold VSYS_MON (it becomes passive after three consecutive results above VSYS_MON). This provides a variable power good signal to trigger boot activities on external ICs.

The active level/debounce, wake-up, and IO supply voltage can be selected via the controls GPIO12_MODE, GPIO12_WEN and GPIO12_TYPE, respectively.

6.1.12 Interrupt Request (nIRQ)

The nIRQ is an output signal that can either be push-pull or open drain (selected via PM_O_TYPE). If an active high IRQ signal is required, it can be achieved by asserting control IRQ_TYPE (recommended for push-pull mode). This port indicates that an interrupt-causing event has occurred and that event/status information is available in the EVENT and STATUS registers. Events are triggered by a status change at the monitored signals. When an event bit is set, the nIRQ signal is asserted (unless this interrupt is masked by a bit in the IRQ mask register). The nIRQ is not released until all event registers with asserted bits have been read and cleared. New events that occur during reading an event register are held until the event register is cleared, ensuring that the host processor does not miss them. The same happens to all events occurring while the sequencer processes time slots (that is, the generation of interrupts is delayed).

6.1.13 Real Time Clock Output (OUT_32K)

OUT_32K is a buffered output of the DA9063 32 kHz oscillator. If enabled via CRYSTAL, the 32 kHz oscillator always runs on the DA9063 following the initial start-up from NO-POWER or DELIVERY mode until the device has reached NO-POWER (or DELIVERY) mode again. The signal output buffer can be disabled manually via EN_32KOUT and paused during POWERDOWN mode by setting OUT32K_PAUSE. The 32K signal can additionally be made available at port GP_FB3.

6.1.14 IO Supply Voltage (VDD_IO1 and VDD_IO2)

VDD_IO1 and VDD_IO2 are two independent IO supply rail inputs of the DA9063 that can be individually assigned to the power manager interfaces (see control bit GPI_V), power manager IOs (see control bits PM_O_V, PM_I_V) and GPIOs (bits GPIOx_TYPE). The rail assignment determines the IO voltage levels and logical thresholds, see Section 5.4. The selection of the supply rail for GPIOs is also partially used for their alternate functions, see Table 1 and Table 2. As an example, GPIO13_TYPE determines the supply rail when this pin is configured as the GP_FB1 output.

Note
Maximum speed at 4-WIRE interface is only available if the selected supply rail is greater than 1.6 V, see Table 44.

6.2 Operating Modes

6.2.1 ACTIVE Mode

A running application is typically in ACTIVE mode. The DA9063 transitions to ACTIVE mode after the host processor performs at least one initial 'alive' watchdog write (or alternatively an initial assertion of the KEEP_ACT port) inside the target time window. If the WATCHDOG function is disabled by setting TWDSCALE to zero, the DA9063 transitions to ACTIVE mode when all of the sequencer IDs in the POWER domain are complete.

In ACTIVE mode, the PMIC core functions as LDOCORE, calendar counter and internal oscillator are running. Typically additional features are enabled, such as the GPADC. The DA9063 can send interrupt requests to the host via a dedicated interrupt port (nIRQ) and status information can be read from the host processor via the power manager interface. Temperature and voltages inside and outside the DA9063 can be monitored and fault conditions can be flagged to the host processor.

6.2.2 POWERDOWN Mode

The DA9063 is in POWERDOWN mode when the power domain SYSTEM is disabled (even partially). This can be achieved when progressing from NO-POWER/DELIVERY/RTC mode or by returning from ACTIVE mode. A return from ACTIVE mode is initiated by low power mode instructions from the host (for example, releasing signal SYS_EN or clearing register bit SYSTEM_EN), from the user by asserting nONKEY (if nONKEY_PIN='1x') or as an interim state during a shutdown to RESET mode.

During POWERDOWN mode LDOCORE, VREF reference voltage, the nONKEY pin, CHG_WAKE port, and the calendar counter are active. Dedicated power supplies can be kept enabled during POWERDOWN mode if their xxx_CONF bits are asserted (supply voltage settings are taken from the respective Vxxx_B registers).

GPIO ports, the GPADC, and the control interfaces also remain active in POWERDOWN mode if not configured otherwise via register PD_DIS. Disabling these blocks during POWERDOWN mode reduces quiescent current, especially if all blocks that require an oscillator clock are disabled (CLDR_PAUSE, HS2WIRE_DIS, PMIF_DIS, GPADC_PAUSE,GPI_DIS, PMCONT_DIS). If required, the application supervision by the WATCHDOG timer can be continued in POWERDOWN mode via WATCHDOG_PD. If the host will not communicate with the DA9063 during POWERDOWN mode, then the control interfaces may also be temporarily disabled (see controls PMIF_DIS/HS2WIRE_DIS).

If the sequencer pointer has stopped at position PART_DOWN (inside domain SYSTEM) it results in a partial power down. When on the way down the sequencer pointer reaches position 0, relevant regulators/rail switches with corresponding position 0 IDs that have cleared control Bxxx_CONF/LDOxx_CONF/xxx_SW_CONF are disabled, otherwise the regulator voltages change to the values defined in VBxxx_B/VLDOxx_B when control DEF_SUPPLY is asserted. When DEF_SUPPLY is released, slot 0 is not processed by the sequencer, hence regulators/rail switches with an ID pointing to slot 0 remain unchanged. Following the next wake-up event Vxxx_A voltage levels and the sequencer power domain controls/timers are set to their default OTP values if OTPREAD_EN is asserted.

Position 0 also allows an automatic transition into a dedicated RTC mode, where all features of the DA9063 (including LDOCORE) are disabled except for the RTC oscillator and calendar. This mode is armed via control RTC_MODE_PD and terminated by an RTC alarm/tick asserting nONKEY/CHG_WAKE, or if V_{DDREF} rises above 2.6 V, this automatically re-enables LDOCORE and the full-power manager logic.

If POWERDOWN mode is reached in response to a long nONKEY press, RTC mode is not entered until the key is released. When nONKEY_SD is asserted and the key is continuously pressed for longer than the time selected by KEY_DELAY + SHUT_DELAY, it asserts KEY_RESET to indicate that the transition to RESET mode was triggered by a long nONKEY, see Section 6.1.1.

When the device is in POWERDOWN or RESET mode, asserting ECO_MODE enables low power. This is achieved internally by using a pulsed mode for VDDCORE and reference voltage generation. This maintains basic functionality but full parametric compliance is no longer guaranteed (as it affects ADC precision, buck performance, LDO voltage resolution, and so on). When the DA9063 is connected to a 32 kHz crystal (and enabled via control CRYSTAL), the pulsed mode timing is generated from this source. Otherwise the pulsed mode is driven from a (free-running) low-power on-chip oscillator.

6.2.3 RESET Mode

The DA9063 is in RESET mode when a complete application shutdown is required. The RESET mode can be triggered by the user, a host processor or by an action on the DA9063, as outlined below:

- By the user:
  - from a long press of nONKEY (interruptible by host)
  - from a long parallel assertion of GPIO14 and GPIO15 (interruptible by host)
- By pressing a reset switch connected to port nSHUTDOWN (non-interruptible)
- Forced from the host processor (non-interruptible) by:
  - asserting port nSHUTDOWN (falling edge)
  - writing to register bit SHUTDOWN
- By an error condition that forces a RESET mode (non-interruptible):
  - no WATCHDOG write (KEEP_ACT signal assertion) from the host inside the watchdog time window (if watchdog was enabled)
  - an under-voltage detected at V_{SYS} (V_{SYS} < VDD_FAULT_LOWER)
  - an internal die over-temperature
- Forced by the error detection line (non-interruptible):
  - by asserting port nOFF (falling edge)

The controls INT_SD_MODE, HOST_SD_MODE, and KEY_SD_MODE can be used to individually configure the shutdown sequences from an internal fault, host or user trigger. In each case, the sequence can be configured to implement either the reverse timing of the power-up sequence or an immediate transition into RESET mode, skipping any delay from the sequencer or dummy slot timers. Asserting nOFF always triggers a fast emergency shutdown. To allow the host to determine the reason for the reset, the source is recorded in FAULT_LOG (as either the KEY_RESET or nSHUT_DOWN bit). The host processor clears FAULT_LOG by writing asserted bits with a 1.

Note
• KEY_SD_MODE = 1 enables a full POR following a long press of ONKEY or a long assertion of GPIO14 and 15. • In the case of an aborted OTP read, the DA9063 enters RESET mode without asserting any bits in FAULT_LOG.

A shutdown to RESET mode begins with the DA9063 asserting the nRESET port. Then domain SYSTEM is completely powered down (sequencer position 0) at which time the device has reached RESET mode: this is a low current consumption state. The only circuits in RESET mode remaining active are LDOCORE (at a reduced level of 2.2 V), the control interfaces and GPIOs, the calendar counter, the VREF reference, and the comparators for over-temperature and V_{SYS} level. Except for LDO1 and the backup battery charger, other regulators and blocks are automatically disabled to avoid draining the battery. During the DA9063 RESET mode, the host processor can be held in a RESET state via port nRESET.

When entering RESET mode, all user and system events are cleared. When leaving RESET mode, the complete DA9063 register configuration is reloaded from OTP (with the exception of AUTO_BOOT in case of a VDD_START fault).

Note
FAULT_LOG, GP_ID_10 to GP_ID_19 and other non-OTP loaded registers (for example, RTC calendar and alarm) remain unchanged when leaving RESET mode. nRESET is always asserted low after a cold start from NO-POWER, RTC, or DELIVERY mode and can also be asserted (depending on configuration of nRES_MODE) before the sequencer starts to power down towards POWERDOWN mode.

Some reset conditions such as shutdown via register write, watchdog error, or over-temperature automatically expire (that is, are automatically cleared by the device as it shuts down). Other RESET triggers such as via port nOFF or nSHUTDOWN need to be released before the DA9063 can move from RESET to POWERDOWN mode. In the case that the application requires regulators to discharge in advance of a consecutive power-up sequence, a minimum duration of the RESET mode can be selected via RESET_DUR.

If the reset was initiated by user action from a long nONKEY key-press (or GPI14 and GPI15), bit KEY_RESET is set and the nIRQ port asserted. After 1 s the shutdown sequence is started, unless this is inhibited by the host clearing KEY_RESET within this 1 s period (by writing a 1 to the related bit in register FAULT_LOG). When the RESET condition has been removed, the DA9063 requires the presence of a good supply (V_{SYS} > VDD_FAULT_UPPER and able to provide enough power) before it can start-up again and move into POWERDOWN mode.

RESET mode is also used during an automatic transition by the device into RTC mode, as described in Section 6.2.4.

6.2.4 RTC Mode

The RTC mode is an ultra-low power mode intended to maintain only the application's system time inside the RTC block. It can be armed by asserting control RTC_EN from OTP or host register write. With RTC_MODE_PD enabled, the device enters RTC mode when the power sequencer reaches slot 0 in a power down sequence. All regulators (including LDOCORE) and most features on the DA9063 are disabled. Only the FAULT_LOG register, calendar counter, and their related registers (including the alarms) are maintained. With RTC_EN = 1, the DA9063 automatically enters RTC mode when a VDD_FAULT condition is present, when RTC_MODE_SD is asserted, or when V_{DDREF} drops below the POR threshold.

RTC mode is automatically terminated when asserting nONKEY or CHG_WAKE, or from an RTC tick/alarm. The same occurs when V_{DDREF} has risen above 2.6 V (for example, from insertion of an external supply or a pre-charged battery). LDOCORE is then switched on and a start-up sequence is triggered.

6.2.5 DELIVERY Mode

The DELIVERY mode provides the lowest possible quiescent current, allowing connected pre-charged batteries (backup or main battery) to maintain charge prior to the end-user starting the device for the first time. It is armed by setting RTC_EN = 0 and then entered by the same conditions as RTC mode. During DELIVERY mode, only the nONKEY, CHG_WAKE, and the V_{DDREF} detection circuitry is enabled. Connecting only a backup battery results in DELIVERY mode.

6.2.6 NO-POWER Mode

In the absence of a (charged) backup battery, the DA9063 enters NO-POWER mode when VDDCORE drops below the VPOR_LOWER threshold. As long as VDDCORE stays below the VPOR_UPPER threshold, an internal power-on-reset (nPOR) signal remains asserted. In this mode, only the VDDCORE threshold comparator is active. This comparator simply checks for a condition that allows the DA9063 to turn on again. When a good supply is subsequently available again on V_{DDREF} (> 2.4 V), VDDCORE is able to rise above VPOR_UPPER and the DA9063 leaves NO-POWER mode.

6.2.7 Power Commander Mode

This is a special mode for evaluation and configuration development. In Power Commander mode, the DA9063 is configured to load the control register default values from the HS 2-WIRE interface, instead of from the OTP cells, so that un-programmed DA9063 samples will power up, allowing evaluation and verification of a proposed user configuration.

Power Commander mode is enabled by connecting TP to a 3.3 V to 5.0 V voltage.

Note
In Power Commander mode, GPI14 and 15 are configured for HS-2-WIRE interface operation (with VDDCORE as the supply) and GPO12 is configured as an output for nVDD_FAULT. Any register writes or OTP loads which can change this configuration are ignored until DA9063 has exited from Power Commander mode.

After leaving the POR state, the DA9063 informs the system that it is waiting for a programming sequence by driving nVDD_FAULT low. The software running on the PC monitors nVDD_FAULT and responds by downloading the values into the configuration registers within DA9063. nVDD_FAULT is automatically released after the download is complete.

There are two programming sequences performed in Power Commander mode. The first takes place between RESET and POWERDOWN mode and the second between POWERDOWN and SYSTEM mode.

Note
To correctly configure DA9063, addresses 0x0A to 0x36, 0x82 to 0xCF, and 0x104 to 0x12E should be programmed during the first sequence. Registers 0x0E, 0x82, and 0xA3 to 0xB3 should be programmed during the second sequence.

When the first programming sequence is complete, DA9063 will be in POWERDOWN mode. Progression from this mode is determined by the values programmed for SYS_EN and AUTO_BOOT. If DA9063 has been directed to progress from POWERDOWN mode then it drives pin nVDD_FAULT low for a second time to request that the SW performs the second programming sequence.

Once the second programming sequence is complete, the progress of the power-up sequence is controlled by the values loaded during the programming sequence.

The programmed configuration can be identified by reading the fuse register CONFIG_ID.

Note
During Power Commander mode, the fault detection status bit VDD_FAULT and the level at the related pin nVDD-FAULT do not match and do not indicate a low voltage level at VDDOUT. An enabled shutdown from a 5 s assertion of GPIO14/15 will be ignored during POWER Commander mode. Any nIRQ and event assertion when accessing the HS 2-WIRE interface (E_GPI14) is suppressed in this mode.

6.3 Start-Up from NO-POWER Mode

6.3.1 Power-On-Reset (nPOR)

The DA9063 generates an internal power-on-reset nPOR (active low) following the initial connection of a supply to V_{DDREF}.

While the VDDCORE voltage is below the threshold VPOR_UPPER, the internal signal nPOR is driven low and the DA9063 will not start-up. This is NO-POWER mode. When the VDDCORE voltage rises above VPOR_UPPER, the following occur:

- The nPOR is driven high (flagged by the POR bit being set in register FAULT_LOG).
- The oscillator is enabled.
- The VREF reference is enabled.
- The complete OTP block is read and stored in the register bank.
- The DA9063 progresses into POWERDOWN mode.

From POWERDOWN mode, the DA9063 continues through the power-up sequence if either:

- the power domain SYSTEM was enabled by the input port, SYS_EN, or,
- the power domain SYSTEM was enabled in OTP settings and AUTO_BOOT was enabled.

With AUTO_BOOT disabled and the power domain SYSTEM enabled in OTP settings, a non-suppressed wake-up event allows the DA9063 to continue through the power-up sequence.

6.4 Exiting Reset Mode and Application Wake-up

Application startup requires a sufficient V_{SYS} supply, as determined by the VDD_START feature, and a wake-up event.

6.4.1 VDD_START

The DA9063 VDD_START feature prevents endless looping of false starts in a weakly-powered system. VDD_START limits the number of automatic restart attempts to three. With reference to Figure 14:

- Figure 14(a): The PMIC starts from NO-POWER mode.
- Figure 14(b): First startup attempt. The PMIC transitions to the ACTIVE state when V_{SYS} rises above $V_{DD\_FAULT\_UPPER}$.
- Figure 14(c): If, during the first startup attempt, the V_{SYS} supply drops below $V_{DD\_FAULT\_LOWER}$ for more than 100 ms, the PMIC shuts down to the SHUTDOWN state. $V_{DD\_FAULT\_UPPER}$ is increased automatically by 250 mV. However, the increased $V_{DD\_FAULT\_UPPER}$ is limited to a maximum of 3.70 V.
- Figure 14(d): Second startup attempt. If V_{SYS} rises above the new $V_{DD\_FAULT\_UPPER}$ threshold, then the PMIC will power-up to the ACTIVE state.
- Figure 14(e): If, during the second startup attempt, the V_{SYS} supply drops below $_{VDD\_FAULT\_LOWER}$ for more than 100 ms, the PMIC shuts down to the SHUTDOWN state. $V_{DD\_FAULT\_UPPER}$ is increased automatically by a further 250 mV (500 mV above its original setting). However, the increased $V_{DD\_FAULT\_UPPER}$ is limited to a maximum of 3.70 V.
- Figure 14(f): Third startup attempt. If V_{SYS} rises above the new $V_{DD\_FAULT\_UPPER}$ threshold, then the PMIC will power-up to the ACTIVE state.

- Figure 14(g): If, during the third startup attempt, the V_{SYS} supply drops below $V_{DD\_FAULT\_LOWER}$ for more than 100 ms, the PMIC shuts down. From then on, AUTO_BOOT and wake-up from non-user events are temporarily disabled. 'User events' are defined in Table 40.

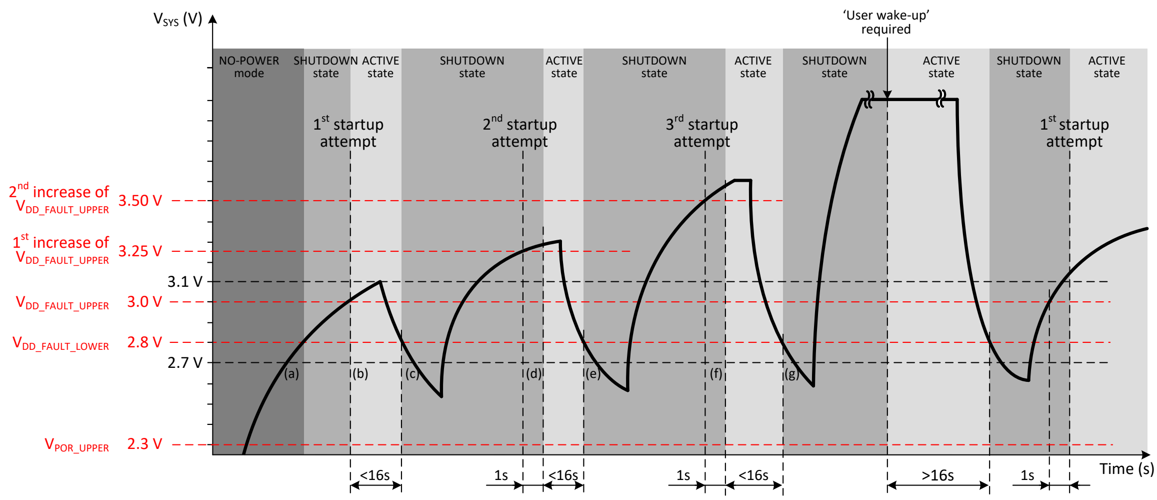


Figure 14: VDD_START Faults

NOTE
● During an attempt to restart, the entry into the ACTIVE state is delayed by 1 s. ● The ACTIVE state also includes POWER1 mode. The PMIC has the same VDD_START behavior from the POWERDOWN and SYSTEM modes as from the ACTIVE state. ● AUTO_BOOT and wake-up from non-user events are re-enabled after the application has successfully powered up to the ACTIVE state for more than 16 s. This also resets the start-up threshold to $V_{DD\_FAULT\_UPPER}$ + 0 mV.

Until the host has been booted, an OTP-enabled flashing LED may be driven from GPIO11, 14, or 15 to indicate to the user that the device is supplied with (insufficient) power. When CHG_WAKE is connected to a charger, the VDD_START-triggered LED flashing continues as long as an external supply is charging the battery. The flashing LED can be configured via controls RESET_BLINKING, BLINK_DUR, and BLINK_FRQ. After the application is running, the blinking LED can be stopped via a host register write.

6.4.2 Wake-Up Events

DA9063 offers two types of wake-up event, user events and system events (see Table 40). Non-suppressed user events (for example, nONKEY, CHG_WAKE or from GPIOs) are always processed and trigger a wake-up.

Wake-up events can be individually suppressed by setting the related nIRQ mask bit. When nONKEY_LOCK is asserted a wake-up requires the debounced signal from nONKEY to be low for a time longer than the configured KEY_DELAY. It is not recommended to mask system events, instead disable the unwanted event sources (for example, GPIs, GPADC, 1.2 V comparator). The wake-up from GPIOs (or selected alternate features that use a shared GPI event) has to be enabled via GPI<x>_WEN.

After a valid wake-up condition is detected, a subset of the OTP configuration is read and the values are used to reconfigure the regulator voltage registers Vxxx_A, the power domain enable settings (if not suppressed via SYSTEM_EN_RD) and the sequencer timer.

DA9063 then asserts the EXT_WAKEUP signal towards the host processors and configures regulators with an ID pointing at slot 0 to their target state. If the power domains are not pre-enabled from OTP settings, the host processor must control further application start-up (via the power domain enable ports, SYS_EN, PWR_EN and PWR1_EN). Alternatively the DA9063 continues powering-up the OTP-enabled domains via the power domain sequencer, but the power sequencer will not start to enable the system supplies unless SYSTEM_EN is asserted.

Progression to ACTIVE mode requires assertion of POWER_EN from the host via port PWR_EN, a register write, or enabled in OTP. After starting the WATCHDOG timer the host processor must assert the WATCHDOG bit within the configured time window. If this does not happen, the state-machine terminates ACTIVE mode and returns to RESET mode.

Table 40: Wake-up Events

Signal : Event	Wake-up	User Event	System Event	IRQ
V_{SYS} monitor : E_VDD_MON	X		X	X
VDD_FAULT pre-warning : E_VDD_WARN	X		X	X
RTC alarm : E_ALARM	X		X	X
RTC periodic tick : E_TICK	X		X	X
Voltage comparator flipped : E_COMP1V2	X		X	X
Pressed On key : E_nONKEY	X	X		X
Wake-up from companion charger : E_WAKE	X	X		X
LDO over current detect : E_LDO_LIM	X		X	X
Regulator voltage out-of-range : E_REG_UVOV	X		X	X
Critical junction temperature : E_TEMP	X		X	X
Power sequencing ready : E_SEQ_RDY			X	X
Voltage ramping ready : E_DVC_RDY			X	X
Manual ADC result ready : E_ADC_RDY			X	X
GPIOs passive to active transition : E_GPIx	X	X		X
ADC 1, 2, 3 threshold : via GPI0, 1, 2	X		X	X
SYS_EN, PWR_EN, PWR1_EN (passive to active transition) : via GPIO8, 9, 10	X		X	X
HS-2-WIRE interface : via GPIO14	X		X	X

6.5 Power Supply Sequencer

The DA9063 power supplies are enabled with a sequencer that contains a programmable step timer, a programmable ID array of slot pointers, and four predefined pointers (SYSTEM_END, POWER_END, MAX_COUNT, and PART_DOWN), as illustrated by Figure 15. The sequencer is able to control up to 32 IDs (six bucks, 11 LDOs, 7 external FET/IC controls, a Wait ID (GPI10), an EN_32K enable, and an ID to activate power down settings), which can be grouped to three power domains.

The power domains have configurable size and their borders are described by the location pointers SYSTEM_END, POWER_END, and MAX_COUNT.

The lowest level power domain SYSTEM starts at step 1 and ends at the step that is described by the location pointer SYSTEM_END. The second level domain POWER starts at the successive step and ends at POWER_END. The third level domain POWER1 starts at the consecutive step and ends at MAX_COUNT. The values of pointer SYSTEM_END, POWER_END, and MAX_COUNT are predefined in OTP registers and should be configured as SYSTEM_END < POWER_END < MAX_COUNT.

The domain system can be thought of as the minimum set of supplies required to enable the core of the target system.

If the control OTPREAD_EN is enabled, the regulator voltages, sequence domain enables (if not suppressed via control SYSTEM_EN_RD), and the sequence timer are reset to their OTP values during the transition from power down to system.

The second level domain POWER includes supplies that are required on top to trigger the application and set the DA9063 into ACTIVE mode. POWER1 can be understood as one of the POWER domains that can be used for further sequenced control of supply blocks during ACTIVE mode (for example, for a sub-application like WLAN or a baseband chipset).

Note
It is recommended that the system is configured to reach ACTIVE mode before running applications.

6.5.1 Powering Up

All buck converters and 11 LDOs of DA9063 have a unique sequencer ID. The power-up sequence is defined by an OTP register bank that contains a series of supplies (and other features), each of which point to a selected sequencer time slot. Several supplies can point to the same time slot which is therefore enabled in parallel by the sequencer. Time slots that have no IDs pointing at them are dummy steps that do nothing but insert a configurable time delay (marked in Figure 15 as D). Supplies/IDs that do not point to a sequencer time slot between 1 and MAX_COUNT are not enabled by the power sequencer but can be controlled individually by the host (via the power manager interface).

During power-up, the sequencer starts at slot 0. If DEF_SUPPLY is asserted, it checks all regulators/rail switches for an ID pointing to slot 0. Cleared LDOxx_AUTO/ BUCKxxx_AUTO/xxx_SW_AUTO bits are configured by setting the related control Bxxx_CONF/LDOxx_CONF/xxx_SW_CONF, otherwise the regulator is enabled. To minimize inrush currents, it is recommended to enable no more than a single default regulator via DEF_SUPPLY. During power-up, the regulator output voltage is taken from the VBxxx_A/VLDOxx_A registers. During power-down, regulators/rail switches with a cleared control in Bxxx_CONF/LDOxx_CONF/ xxx_SW_CONF are disabled, otherwise the regulator voltage is changed to VBxxx_B/VLDOxx_B when entering slot 0. When DEF_SUPPLY is released, slot 0 is not processed by the sequencer (regulators/rail switches with an ID pointing at slot 0 remain unchanged).

The progression of the sequencer to slot 1 is dependent on certain conditions:

- If AUTO_BOOT and SYSTEM_EN are both asserted (via port, by register write or in OTP), the sequencer asserts the READY signal (if GP_FB1 is so configured) and then continues by processing slot 1.
- If AUTO_BOOT is not asserted, the sequencer remains in a holding start state, waiting for either:
  - the assertion of SYSTEM_EN, or,
  - any other wake-up event if SYSTEM_EN is already enabled.

All supplies (and other sequenced features) that are pointing at slot 1 are then processed. This is similar to the processing of slot 0 with the exception that DEF_SUPPLY has no effect on slots apart from slot 0. From slot 1, the sequencer progresses until it reaches the position of pointer SYSTEM_END. At this point, all IDs of the first power domain SYSTEM are enabled and, if POWER_EN is not asserted, the DA9063 releases the READY signal (in combination with optional assertion of E_SEQ_RDY).

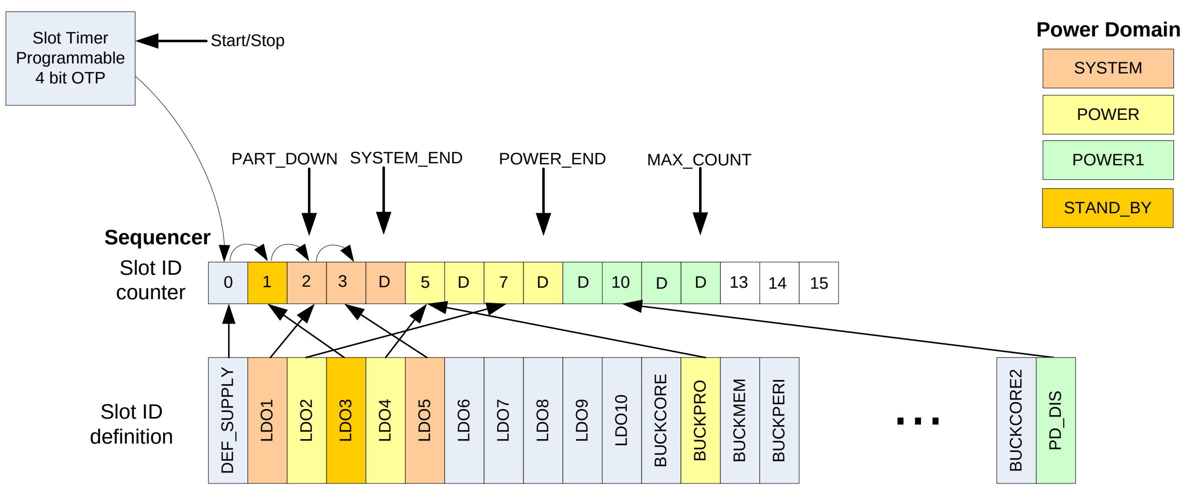


Figure 15: Assignment of Actions to Sequencer Slot IDs

Table 41: Power Sequencer Controlled Actions

Action	Sequencer Time Slot
Control LDO1	LDO1_STEP
Control LDO2	LDO2_STEP
Control LDO3	LDO3_STEP
Control LDO4	LDO4_STEP
Control LDO5	LDO5_STEP
Control LDO6	LDO6_STEP
Control LDO7	LDO7_STEP
Control LDO8	LDO8_STEP
Control LDO9	LDO9_STEP
Control LDO10	LDO10_STEP
Control LDO11	LDO11_STEP

Action	Sequencer Time Slot
Control BUCKCORE1	BUCKCORE1_STEP
Control BUCKCORE2	BUCKCORE2_STEP
Control BUCKPRO	BUCKPRO_STEP
Control BUCKIO	BUCK_IO_STEP
Control BUCKMEM	BUCKMEM_STEP
Control BUCKPERI	BUCKPERI_STEP
Control CORE_SW	CORE_SW_STEP
Control PERI_SW	BUCKPERI_STEP
Assert/Release GPIO2	GP_RISE1_STEP
Release/Assert GPIO2	GP_FALL1_STEP
Assert/Release GPIO7	GP_RISE2_STEP
Release/Assert GPIO7	GP_FALL2_STEP
Assert/Release GPIO8	GP_RISE3_STEP
Release/Assert GPIO8	GP_FALL3_STEP
Assert/Release GPIO9	GP_RISE4_STEP
Release/Assert GPIO9	GP_FALL4_STEP
Assert/Release GPIO11	GP_RISE5_STEP
Release/Assert GPIO11	GP_FALL5_STEP
Wait for active state at GPI 10	WAIT_STEP
Wait for stable oscillator signal	EN32K_STEP
PD_DIS	PD_DIS_STEP

On completion of domain SYSTEM, the sequencer waits for POWER_EN to be asserted (via the PWR_EN port, a register write or in OTP). When POWER_EN is asserted, the signal READY is asserted (if not already asserted) and regulators/IDs of domain POWER are enabled sequentially. The sequencer stops at the position of pointer POWER_END. At this point it also: releases the READY signal (if POWER1_EN is not asserted); optionally asserts E_SEQ_RDY; enables the initial WATCHDOG timer and waits for the first associated alive feedback from the host processor. After this, the start-up of the DA9063 progresses into ACTIVE mode.

A third power domain, POWER1, can be enabled via POWER1_EN (asserted by PWR1_EN port, register write or in OTP). It enables all consecutive IDs until the position of pointer MAX_COUNT has been reached. The READY signal is asserted as long as IDs are processed (if enabled) and E_SEQ_RDY is asserted when reaching MAX_COUNT.

On start-up, and if OUT_CLOCK is asserted, the sequencer waits at a slot containing ID EN32K_STEP until the 32 kHz clock stabilizes, see Section 6.14.1.1.

6.5.2 Power-Up Timing

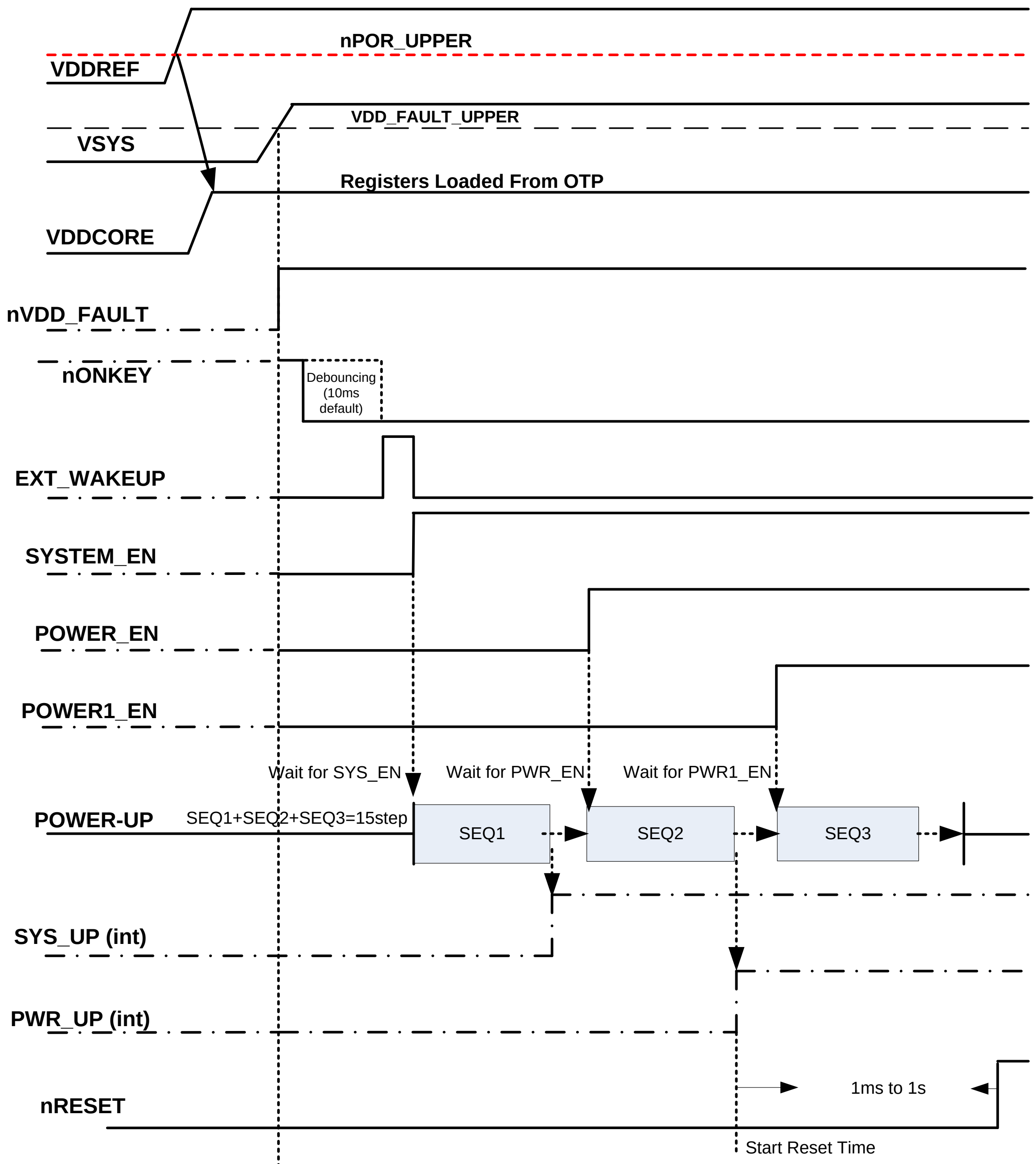


Figure 16: Power-Up Timing

6.5.3 Programmable Slot Delays

The delay between the slots of a sequence is controlled via the programmable value of SEQ_TIME in register SEQ_TIMER. This has a default delay of 128 µs per slot (min. 32 µs, max. 8 ms). The delay time between individual supplies can be extended by leaving a consecutive slot(s) with no IDs pointing to it: these are dummy slots. The dummy slots have an independent delay configured by SEQ_DUMMY. These delay times, in register SEQ_TIMER, are (re-)loaded from OTP every time domain SYSTEM begins to power-up.

6.5.4 Powering Down

When the DA9063 is powering down, the sequencer disables the supplies in reverse order and timing, asserts READY during sequencing, and triggers E_SEQ_RDY on reaching the target sequencer slot. Supplies that are configured to stay on (LDO<x>_CONF, B<x>_CONF, xxx_SW_CONF bit is set) are not disabled and are configured with the voltage setting from register VB<x>_B/VLDO<x>_B when the related time slot/ID is processed. The state of the regulators that are enabled for GPI control will not be changed by the sequencer when processing the related ID. This also applies for the selection of the related V<x>_A or V<x>_B voltage control register in case a regulator is enabled for GPI voltage selection.

If powering down is initiated by clearing POWER1_EN, the sequencer stops controlling IDs before the domain pointer POWER_END is reached. If POWER_EN is cleared, the domain POWER1 is powered down followed by POWER before the sequencer reaches pointer SYSTEM_END. These modes are used to temporarily disable optional features of a running application for reduced power (sleep mode).

If SYSTEM_EN is cleared the sequencer processes all IDs lower than the pointer position down to slot 0. The sequencer can be forced to stop the intended power down sequence prior to maturity at pointer position PART_DOWN via an asserted control STANDBY (PART_DOWN has to point into domain SYSTEM). In these cases the power sequencer has reached the application's POWERDOWN mode (hibernate/standby), which enables the option to reset regulator settings for the consecutive power-up sequence from OTP (enabled by OTPREAD_EN).

Wake-up events are enabled when the sequencer reaches slot 0 or pointer PART_DOWN (ignored outside of POWERDOWN mode). The assertion of nIRQ from events during POWERDOWN mode may be delayed until ACTIVE mode is reached the next time if configured by nIRQ_MODE. During processing slot 0, all supplies pointing into this step with a cleared control Bxxx_CONF/LDOxx_CONF/xxx_SW_CONF are disabled, otherwise the regulator voltage is changed to VBxxx_B/VLDOxx_B (if bit DEF_SUPPLY is asserted). Asserting control register bit SHUTDOWN first powers down to slot 0 and then forces the DA9063 into RESET mode. Autonomous features such as the 32K output buffer or the Auto-ADC measurement can be disabled temporarily for POWERDOWN mode via register PD_DIS. The timing for processing PD_DIS can be defined by selecting a step inside the sequence. Features asserted in PD_DIS are (re-)enabled when PD_DIS is processed during a power-up sequence.

Control nRES_MODE enables the assertion of nRESET before executing a power-down sequence and starting the reset timer during the consecutive powering up. This is also true for partial POWERDOWN mode, when the sequencer powers down to pointer position PART_DOWN. The reset timer starts to run from the selected RESET_EVENT and releases the nRESET port after the reset timer expires.

6.5.5 User Programmable Delay

A conditional mode transition can be achieved using ID WAIT_STEP. If pointing into the power sequence the progress of an initiated mode transition can be synchronized, for example with the state of a host. This is indicated by toggling the signal at GPI10 to its configured active state. 'To begin the wait step, the event bit E_GPI10 must be clear. This is the typical case for a system cold boot. The wait is terminated when an event is detected by the PMIC on GPI10. To use this feature during a warm boot, such as waking up after a power-down from ACTIVE to POWERDOWN, the E_GPI10 bit must first be cleared of any previous GPI10 event. A safety timeout of 500 ms can be selected in TIME_OUT to trigger a power-down to RESET mode (including the assertion of

WAIT_SHUT inside register FAULT_LOG) if E_GPI10 is not asserted in time. The ID WAIT_STEP provides an alternate timer mode, selected by WAIT_MODE and configured by WAIT_TIME, which provides a delay timer for a selected sequencer step. To enable symmetric sequence behavior, ID WAIT_STEP should not share a sequencer slot with other IDs. In the case of a shutdown sequence to RESET mode any waiting/delay at ID WAIT_STEP is skipped.

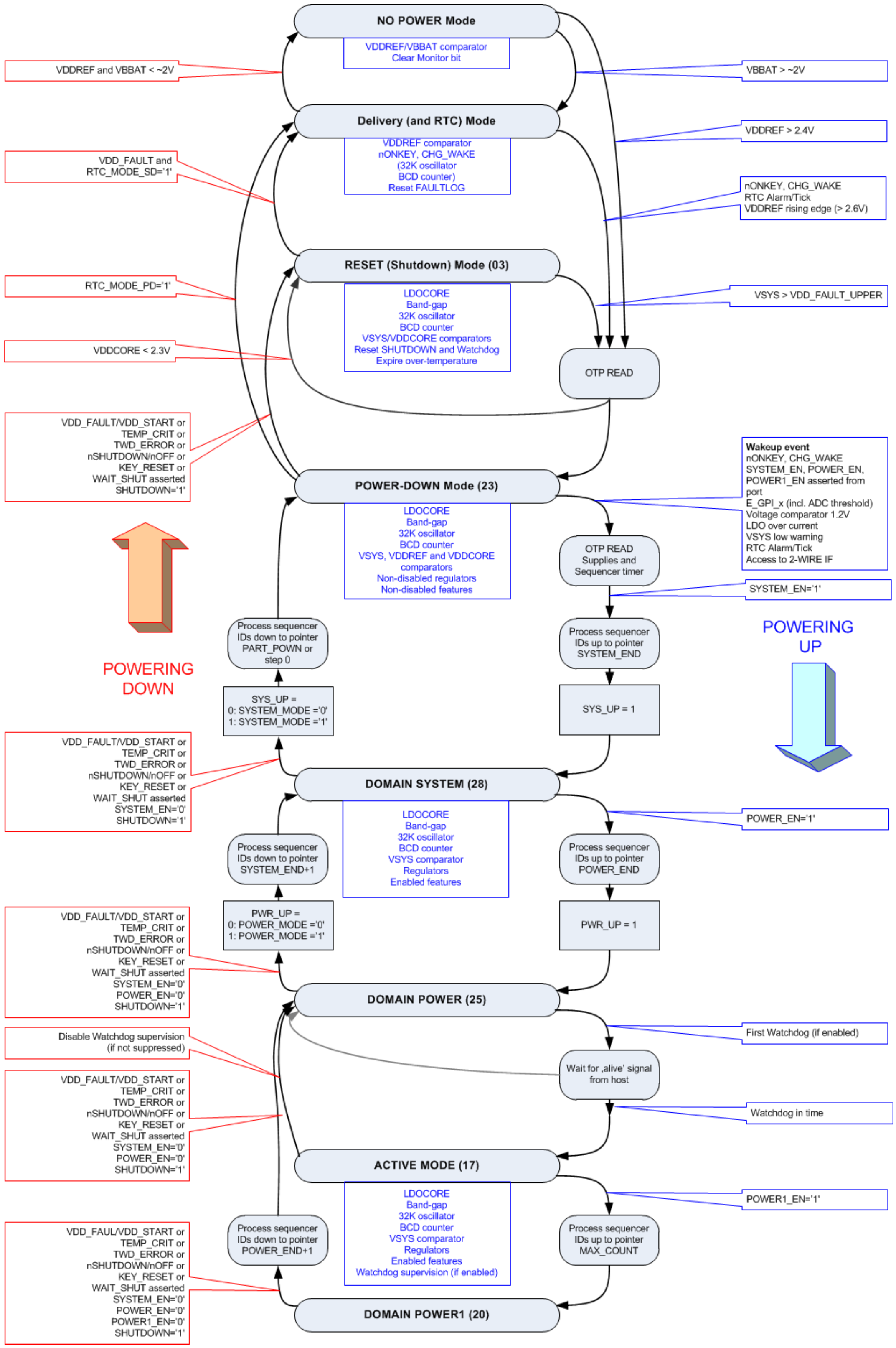


Figure 17: Power Mode Transitions

6.6 System Monitor (Watchdog)

After powering up domain POWER, the DA9063 can initiate a watchdog monitor function. The host processor must write a 1 within a configured t_{WD_MAX} time into control WATCHDOG, thereby indicating that the host is alive. If the host does not write 1 to this watchdog bit within the t_{WD_MAX} time, the DA9063 asserts TWD_ERROR in the FAULT_LOG register and powers down to RESET mode.

After this first write, the host must continue to write to this watchdog bit within the configured time or DA9063 powers down as described above. The time window has a minimum time t_{WD_MIN} fixed at 110 ms and a maximum time t_{WD_MAX}, nominally 2.048 s. The t_{WD_MAX} value can be extended by multiplying the nominal t_{WD_MAX} by the value of register bits TWDSCALE. TWDSCALE is used to extend the t_{WD_MAX} time by x1, x2, x4, x8, x16, x32, or x64.

Once in the ACTIVE state, the DA9063 continues to monitor the system unless it is disabled by setting TWDSCALE to zero. When powering down from ACTIVE mode, the watchdog monitor is stopped unless it enters POWERDOWN mode via WATCHDOG_PD.

If the WATCHDOG register bit is set to a 1 within the time window, the watchdog monitor resets the timer, sets the watchdog bit back to zero (this bit is always read as zero) and waits for the next watchdog signal. The watchdog trigger can also be asserted from the host by asserting KEEP_ACT in hardware. This mode is selected with control PM_FB2_PIN and removes the above requirement for the periodic setting of the watchdog bit.

The watchdog feature can be disabled by setting TWDSCALE to zero.

6.7 GPIO Extender

The DA9063 includes a GPIO extender that provides up to 16 V_{DDREF} -tolerant general purpose input/output ports, each controlled via registers from the host, see Table 42 and Figure 18.

The GPIO ports are pin-shared with ports from GPADC, HS-2-WIRE-interface and signals from the power manager. Configuration settings and events from GPIx ports are also shared with alternative features. For example, if GPIO1_PIN is configured to be ADCIN2, exceeding the configured ADC thresholds triggers a GPI1 event that generates a maskable GPI1 interrupt. The GPI active High/Low setting from the GPIOx_TYPE register and the selection of pull-up resistor is also applicable to the alternative port functions selected via GPIOx_PIN (for example, SYS_EN, PWR_EN and PWR1_EN). This is also true for GPIOx_WEN, which is used to enable triggering of a wake-up event (ADCIN1, ADCIN2, ADCIN3, SYS_EN, PWR_EN, PWR1_EN, HS-2-WIRE interface). When GPI ports are enabled (including being enabled by changing the setting of GPIOx_PIN), the GPI status bits are set to their non-active state. This ensures that any signals that are already active are detected and immediately generate any appropriate events.

In ACTIVE and POWERDOWN mode, the GPIO extender can continuously monitor the level of ports that are selected as general purpose inputs. GPIs are supplied from the internal rail VDDCORE or VDD_IO2 (selected via GPI_V) and can be configured to trigger events in active-high or active-low mode. The input signals can optionally be debounced (configurable via control DEBOUNCING, 10 ms default) and the resulting signal level is reflected by the status register GPIx. When the status has changed to its configured active state (edge sensitive) the assigned event register is set and the nIRQ signal is asserted (unless this nIRQ is masked). GPIs can be individually configured to generate a system wake-up via GPIxx_WEN.

If enabled via regulator controls LDOx_GPI/Bxxx_GPI, the ports GPI1, GPI2, and GPI13 can be used to enable/disable regulators or rail switches (that is, controlling LDOx_EN/Bxxx_EN/xxx_SW_EN). The GPI active level is selected via the related GPIxx_TYPE control. GPI ports that are selected for this hardware control of one or more regulators do not generate events (nIRQ). GPI1, 2, and 13 can alternatively be selected to toggle the VLDOx_SEL/VBxxxx_SEL. Apart from changing the regulator output voltage, this feature also allows hardware control of regulator mode (sync/sleep mode) via selection of the settings contained in xxxx_SL_A and xxxx_SL_B (but only for those bucks configured with Bxxxx_MODE = 00). When a regulator is controlled via GPI, its enable and voltage register selection are no longer controlled by the power sequencer (processing the related ID only affects non-GPI controlled functionality). However, these settings can still be changed via register writes from the control interface.

Events on GPI10 can be used to control the progress of the power sequencer. Processing ID WAIT_STEP causes the sequencer to wait until GPI10 changes into its active state.

Note
Supplies directly enabled/disabled from GPI1, 2, or 13 have to be excluded from the power sequencer control (IDs of these supplies should point into a slot higher than MAX_COUNT)

If defined as an output, GPO0, 1, 3 to 6, 10 to 11, and 13 to 15 can be configured to be open-drain instead of push-pull. The supply rail can be individually selected from either VDD_IO1 or VDD_IO2. By disabling the internal 120 kΩ pull-up resistor when in open-drain mode, the GPO can also be supplied from an external rail (see registers CONFIG_K and CONFIG_L). The GPO output state reflects the respective register bit GPIOx_MODE.

When configured as outputs, GPO 2, 7, 8, 9, and 11 can be controlled by the DA9063 power sequencer. Five pairs of level asserting and level releasing IDs (GP_RISE1_STEP/ GP_FALL1_STEP to GP_RISE5_STEP/GP_FALL5_STEP) may be assigned individually to slots of the power sequencer, which trigger the configured level transition on the GPOs when processing the related ID during powering up (see Table 41 for assignments). The configured level change is inverted when processing the IDs during powering down. These are intended for use as enable signals either for external regulators or other devices in the system.

When the GPIO unit is off (POR), all ports are configured as open drain output with high level (pass device switched off, high impedance state). When leaving POR, the pull-up or pull-down resistors are configured from registers CONFIG_K and CONFIG_L. When the GPIO unit is temporarily disabled by the power sequencer (via GPI_DIS or PMCONT_DIS) level transitions on inputs are no longer detected and I/O drivers keep their configuration and programmed levels.

GPO12 can be driven by the state of VDD_MON to provide an active high ‘Power good’ signal (selected via GPIO12_PIN).

GPO10, 11, 14, and 15 are extended power GPO ports, where the maximum sink current is 11 mA and the maximum source current is 4 mA. This enables driving LEDs. The output ports GPO11, GPO14, and GPO15 can be toggled with a configurable periodic pulse configured via BLINK_FRQ and BLINK_DUR and include an optional PWM control. The generated PWM signals have a duty cycle from 0 % to 100 % with a repetition frequency of 21 kHz and 95 steps (using one 2 MHz clock for each step). The duty cycle is set by the controls GPO11_PWM, GPO14_PWM, and GPO15_PWM, with any value larger than 0 enabling the PWM mode of operation. The PWM control can also be made to dim the brightness between its current value and a new value at a rate of 32 ms per step. Selection of this mode is set by GPO11_DIM, GPO14_DIM, and GPO15_DIM. When set to zero the PWM ratio immediately changes. This creates a common anode tricolor LED brightness control. Flashing is driven from the crystal oscillator when control CRYSTAL has been asserted; otherwise an auxiliary on-chip oscillator is used.

LEDs are recommended to be low-side driven (using the GPIOs in sink mode) which is configured by setting GPIOx_MODE = 1.

Table 42: GPIO Overview

GPIO	Alternate Port	Alternate Port Shared Resources	GPI Wake-up	Remark
0	ADCIN1	E_GPI0, M_GPI0, GPIO0_MODE	x	Auto measure ADC
1	ADCIN2	E_GPI1, M_GPI1, GPIO1_MODE	Regulator control x (in other modes)	Auto measure ADC/1.2V comparator, HW control of regulator
2	ADCIN3	E_GPI2, M_GPI2, GPIO2_MODE	Regulator control x (in other modes)	Auto measure ADC, HW control of regulator/ power sequencer controlled GPO
3	CORE_SWG		x	Power sequencer controlled ext. FET
4	CORE_SWS		x	Power sequencer controlled ext. FET voltage sense
5	PERI_SWG		x	Power sequencer controlled ext. FET
6	PERI_SWS		x	Power sequencer controlled ext. FET voltage sense
7			x	Power sequencer controlled GPO
8	SYS_EN	E_GPI8, M_GPI8, GPIO8_TYPE, GPIO8_WEN, GPIO8_MODE	x	Power sequencer controlled GPO
9	PWR_EN	E_GPI9, M_GPI9, GPIO9_TYPE, GPIO9_WEN, GPIO9_MODE	x	Power sequencer controlled GPO
10	PWR1_EN	E_GPI10, M_GPI10, GPIO10_TYPE, GPIO10_WEN, GPIO10_MODE	x	High power GPO, input signal for ID WAIT
11			x	High power GPO (LED flashing/PWM), Power Sequencer controlled GPO
12	nVDD_FAULT	GPIO12_TYPE, GPIO12_WEN, GPIO12_MODE	x	VDD_MON state controlled GPO (POWER_GOOD)
13	GP_FB1	GPIO13_TYPE, GPIO13_MODE	Regulator control x (in other modes)	HW control of regulator
14	DATA	E_GPI14, M_GPI14, GPIO14_TYPE, GPIO14_MODE	x	High power GPO (LED flashing/PWM), Reset via long assertion in parallel with GPI15, 2nd 2-WIRE or DVC Control Interface

GPIO	Alternate Port	Alternate Port Shared Resources	GPI Wake-up	Remark
15	CLK		x	High power GPO (LED flashing/PWM), Reset via long assertion in parallel with GPI14, 2nd 2-WIRE or DVC Control Interface

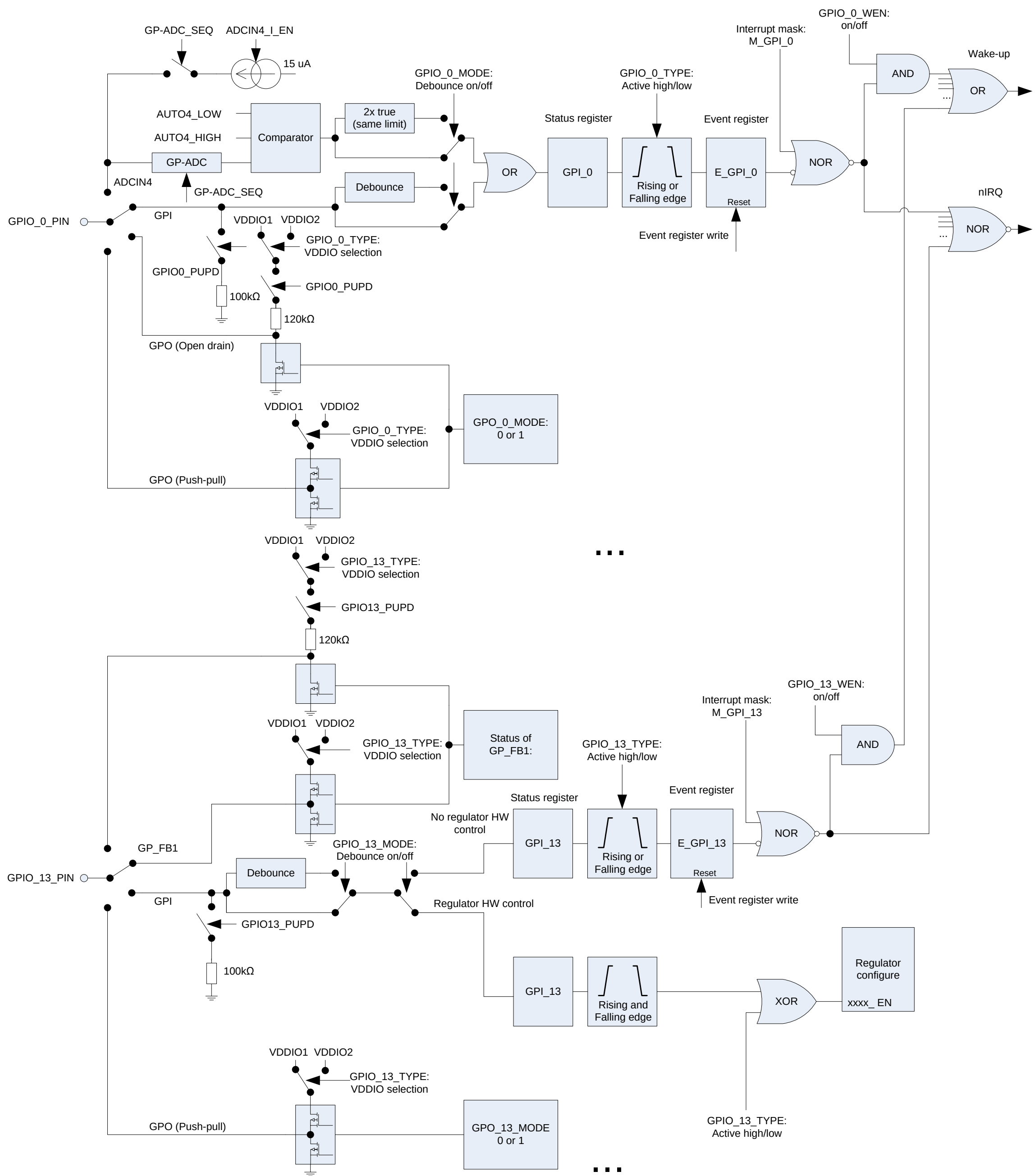


Figure 18: GPIO Principal Block Diagram (Example Paths)

6.8 Control Interfaces

The DA9063 is register controlled by the host software. The DA9063 offers two independent serial control interfaces to access these registers (Figure 19). The communication via the main power manager interface is selected via control IF_TYPE during the initial OTP read to be either a 2-WIRE (I^2C Compatible), or 4-WIRE (SPI compliant) connection. The alternate interface is a fixed 2-WIRE bus. Data is shifted into or out from DA9063 under the control of the host processor that also provides the serial clock. The interfaces are usually only configured once from OTP values, which are loaded during the initial start-up. The interface configuration can be changed by the host. However, care must be taken that changes are not made while the interface is active. If enabled, IF_RESET forces a reset of all control interfaces when port nSHUTDOWN is asserted.

6.8.1 Power Manager Interface (4- and 2-WIRE Control Bus)

This is the dedicated power control interface from the primary host processor. In 4-WIRE mode, the interface uses a chip-select line (nCS/nSS), a clock line (SK), a data input (SI), and a data output line (SO).

6.8.1.1 4-WIRE Communication

In 4-WIRE mode, the DA9063 register map is split into four pages with each page containing up to 128 registers. The register at address zero on each page is used as a page control register. The default active page after reset includes registers 0x01 to 0x7F. Writing to the page control register changes the active page for all subsequent read/write operations unless an automatic return to page 0 was selected by asserting control REVERT. Unless REVERT was asserted after modifying the active page it is recommended to read back the page control register to ensure that future data exchange accesses the intended registers.

The 4-WIRE interface features a half-duplex operation (data can be transmitted and received within a single 16-bit frame) with an enhanced clock speed (up to 14 MHz). It operates at the provided host clock frequencies.

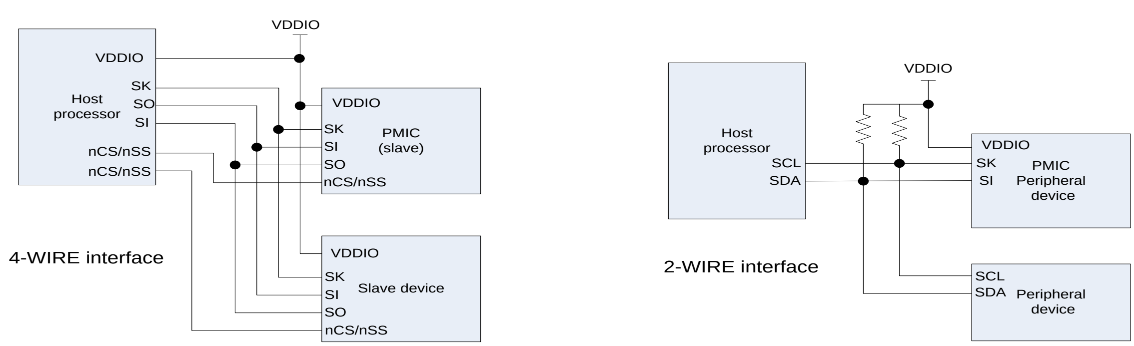


Figure 19: Schematic of 4- and 2-WIRE Power Manager Bus

A transmission begins when initiated by the host. Reading and writing is accomplished using an 8-bit command, which is sent by the host prior to the exchanged 8-bit data. The byte from the host begins shifting in on the SI pin under the control of the serial clock SK provided from the host. The first 7 bits specify the register address (0x01 to 0x7F) to be written or read by the host. The register address is automatically decoded after receiving the seventh address bit. The command word ends with a R/W bit which, together with the control bit R/W_POL, specifies the direction of the next data exchange. During register writing, the host continues sending out data during the following 8 SK clocks. For reading, the host stops transmitting and the 8-bit register is clocked out of the DA9063 during the consecutive 8 SK clocks of the frame. Address and data are transmitted MSB first. The polarity (active state) of nCS is defined by control bit nCS_POL. nCS resets the interface when inactive and it must be released between successive cycles.

The SO output from DA9063 is normally in a high-impedance state and active only during the second half of read cycles. A pull-up or pull-down resistor may be needed on the SO line if a floating logic signal can cause unintended current consumption inside other circuits.

Table 43: 4-WIRE Clock Configurations

CPOL Clock Polarity	CPHA Clock Phase	Output Data is Updated at SK Edge	Input Data is Registered at SK Edge
0 (idle low)	0	falling	rising
0 (idle low)	1	rising	falling
1 (idle high)	0	rising	falling
1 (idle high)	1	falling	rising

The DA9063 4-WIRE interface offers two further configuration bits. Clock polarity (CPOL) and clock phase (CPHA). CPOL determines whether SK idles high (CPOL = 1) or low (CPOL = 0). CPHA determines on which SK edge, data is shifted in and out. With CPOL = 0 and CPHA = 0, the DA9063 latches data on the SK rising edge. If CPHA = 1, the data is latched on the SK falling edge. The CPOL and CPHA states allow four different combinations of clock polarity and phase; each setting is incompatible with the other three. The host and DA9063 must be set to the same CPOL and CPHA states to communicate with each other.

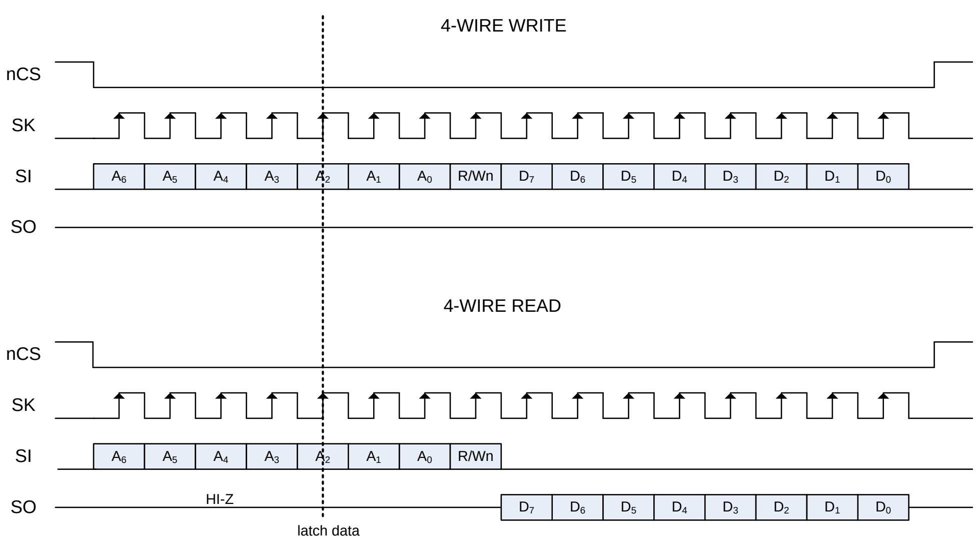


Figure 20: 4-WIRE Host Write and Read Timing (Ncs_POL = 0, CPOL = 0, CPHA = 0)

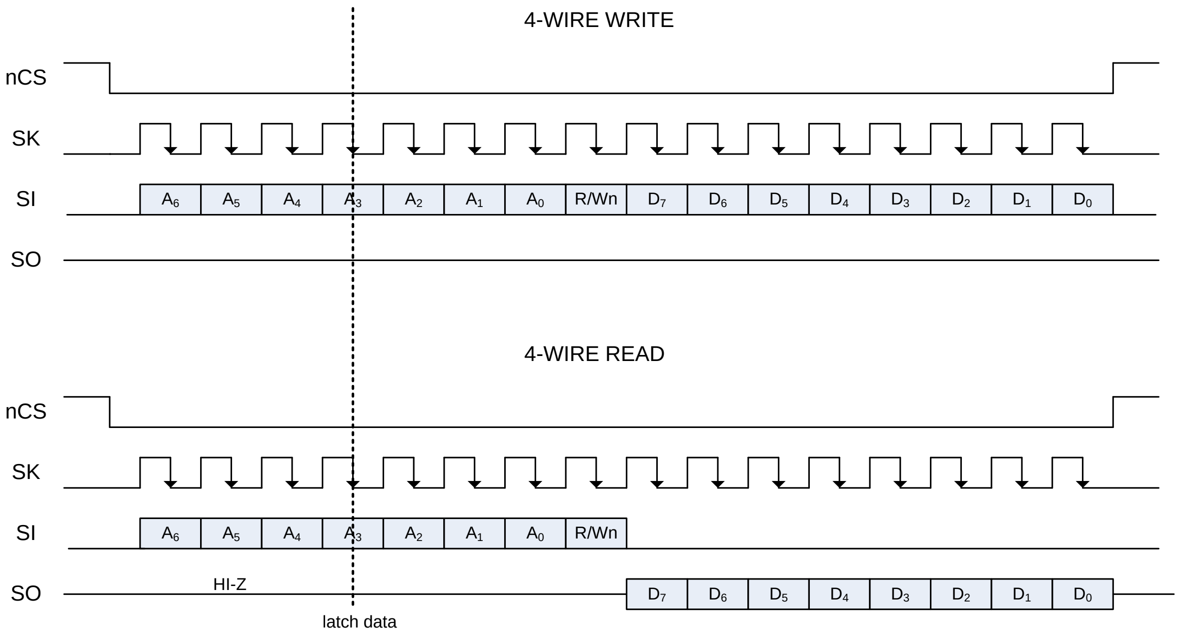


Figure 21: 4-WIRE Host Write and Read Timing (Ncs_POL = 0, CPOL = 0, CPHA = 1)

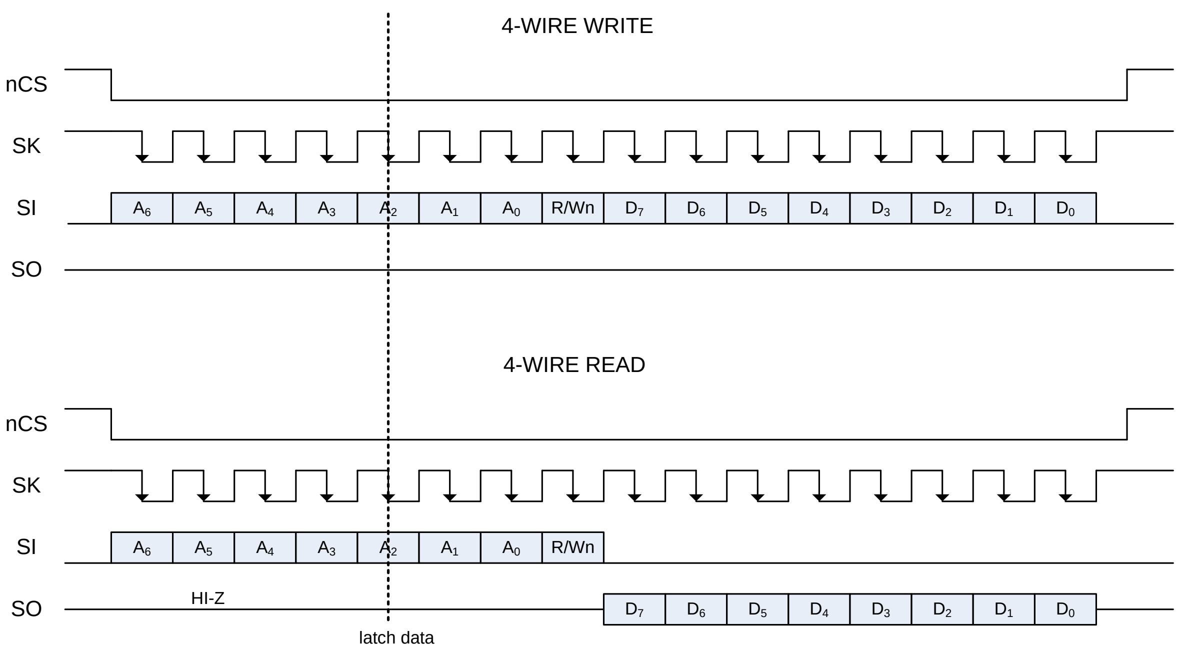


Figure 22: 4-WIRE Host Write and Read Timing (Ncs_POL = 0, CPOL = 1, CPHA = 0)

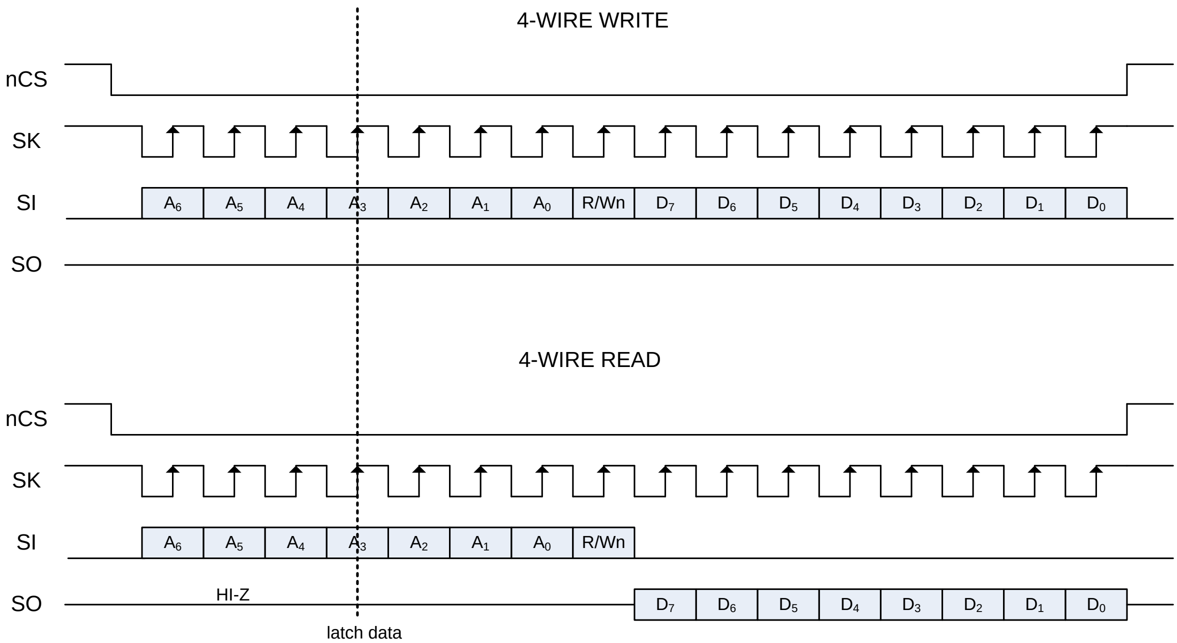


Figure 23: 4-WIRE Host Write and Read Timing (Ncs_POL = 0, CPOL = 1, CPHA = 1)

Table 44: 4-WIRE Interface Summary

Parameter		Description
Signal Lines	nCS	Chip select
	SI Serial input data	Master out, Slave in
	SO Serial output data	Master in, Slave out
	SK	Transmission clock
Interface	Push-pull with tri-state	
Supply voltage	Selected from VDD_IO1 / VDD_IO2	1.6 to 3.3 V
Data rate	Effective read/write data	Up to 7 Mbps
Transmission	Half-duplex	MSB first
	16-bit cycles	7-bit address, 1-bit read/write, 8-bit data
Configuration	CPOL	clock polarity
	CPHA	clock phase
	nCS_POL	nCS active-low / -high

6.8.1.2 2-WIRE Communication

With control IF_TYPE = 1, the DA9063 power manager interface is configured for 2-WIRE serial data exchange. It has a configurable device address IF_BASE_ADDR (default read address: 0xB1, write address 0xB0). For details of configurable addresses, see control IF_BASE_ADDR in Section A.4.2.

In 2-WIRE mode, SK is the clock (CLK) and SI is data (DATA). The 2-WIRE interface is open-drain, supporting multiple devices on a single line. The bus lines must be pulled high by external pull-up resistors (2 kΩ to 20 kΩ). The attached devices only drive the bus lines low by connecting them to ground. As a result, two devices cannot conflict if they drive the bus simultaneously. In standard/fast mode, the highest frequency of the bus is 400 kHz. The exact frequency can be determined by the application and does not have any relation to the DA9063 internal clock signals. The DA9063 follows the host clock speed within the described limitations and does not initiate any clock arbitration or slow down. Control TWOWIRE_TO enables an automatic interface RESET that is triggered when the clock signal ceases to toggle for >35 ms (compatible with SMBus $T_{TIMEOUT}$).

The interface supports operation compatible with Standard, Fast, Fast-Plus and High Speed modes of the I^2C-bus specification Rev 03 (UM10204_3). Bus clear, in the case of the DATA signal being stuck low, is achieved after receiving 9 clock pulses. Operation in High Speed mode at 3.4 MHz requires a minimum interface supply voltage of 1.8 V and a mode change in order to enable spike suppression and slope control characteristics compatible with the I^2C-bus specification. The high speed mode can be enabled on a transfer-by-transfer basis by sending the master code (0000 1XXX) at the beginning of the transfer. The DA9063 does not make use of clock stretching and delivers read data without additional delay up to 3.4 MHz.

Alternatively, the interface can be configured to continuously use High Speed mode via PM_IF_HSM, so that the master code is not required at the beginning of every transfer. This reduces communication overhead on the bus, but limits the attachable slaves to the bus to compatible devices.

Communication on the 2-WIRE bus always takes place between two devices, one acting as the master and the other as the slave. The DA9063 only operates as a slave. Opposite to the 4-WIRE mode, the 2-WIRE interface has direct access to two pages of the DA9063 register map (up to 256 addresses). The register at address zero on each page is used as a page control register (with the 2-WIRE bus ignoring the LSB of control REG_PAGE). Writing to the page control register changes the active page for all subsequent read/write operations unless an automatic return to page 0 was selected by asserting control REVERT. Unless REVERT was asserted after modifying the active page, a read-back of the page control register is recommended to ensure that future data exchange is accessing the intended registers.

In 2-WIRE operation, the DA9063 offers an alternative method to access register pages 2 and 3. These pages can be accessed directly by incrementing the device address by one (default read address 0xB3; write address 0xB2). This removes the need to write to the page register before access to pages 2 and 3, thus reducing the traffic on the 2-WIRE bus.

6.8.1.3 Details of the 2-WIRE Control Bus Protocol

All data is transmitted across the 2-WIRE bus in groups of 8 bits. To send a bit, the SI line is driven at the intended state while the SK is LOW (a low on SI indicates a zero bit). Once the SI has settled, the SK line is brought high and then low. This pulse on SK clocks the SI bit into the receiver's shift register, see Figure 24.

A two byte serial protocol is used containing one byte for address and one byte data. Data and address transfer is MSB transmitted first for both read and write operations. Transmission begins with the START condition from the master while the bus is idle. It is initiated by a high-to-low transition on the SI line while the SK is in the high state (a STOP condition is indicated by a low-to-high transition on the SI line while the SK is in the high state).

Figure 24: Timing of 2-WIRE START and STOP Condition

The 2-WIRE bus is monitored by the DA9063 for a valid slave address when the interface is enabled. It responds immediately when it receives its own slave address. This 'Acknowledge' is done by pulling the SI line low during the following clock cycle (see the white blocks marked A in Figure 25 to Figure 29).

The protocol for a register write from master to slave consists of a start condition, a slave address with read/write bit and the 8-bit register address followed by 8 bits of data terminated by a STOP condition (all bytes responded by DA9063 with Acknowledge), as illustrated in Figure 25.

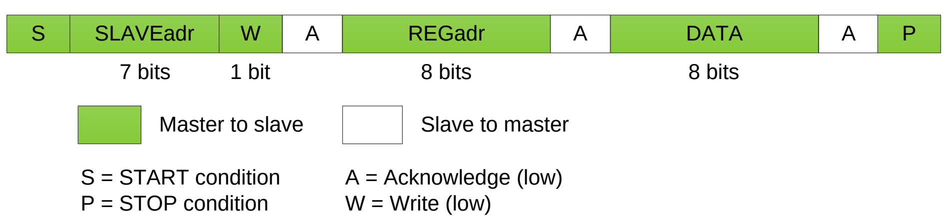


Figure 25: 2-WIRE Byte Write (SI/DATA Line)

When the host reads data from a register, it first has to write access the DA9063 with the target register address and then read access the DA9063 with a Repeated START or alternatively a second START condition. After receiving the data, the host sends Not Acknowledge and terminates the transmission with a STOP condition (Figure 26).

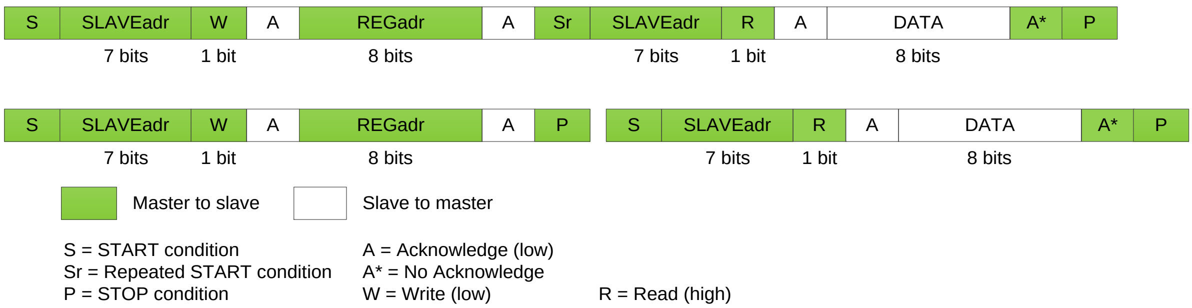


Figure 26: Examples of 2-WIRE Byte Read (SI/DATA Line)

Consecutive (page) read mode is initiated from the master by sending an Acknowledge instead of Not Acknowledge after receipt of the data word. The 2-WIRE control block then increments the address pointer to the next 2-WIRE address and sends the data to the master. This enables an unlimited read of data bytes until the master sends a Not Acknowledge directly after the receipt of data, followed by a subsequent STOP condition. If a non-existent 2-WIRE address is read then the DA9063 returns code zero (Figure 27).

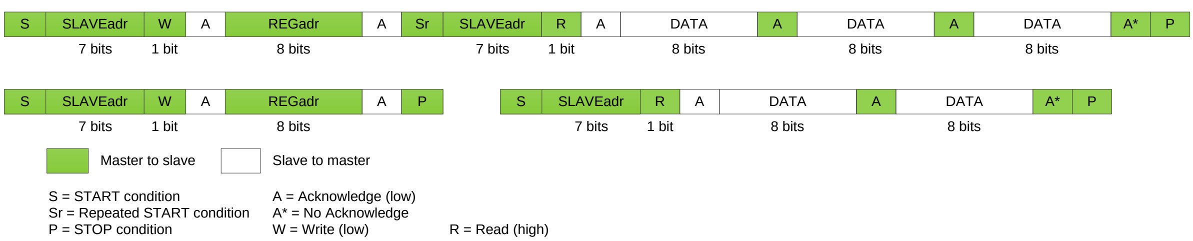


Figure 27: Examples of 2-WIRE Page Read (SI/DATA Line)

The slave address after the Repeated START condition must be the same as the previous slave address.

For enhanced data transfer efficiency, the DA9063 supports two write modes: Page Write mode and Repeated Write mode.

Page Write mode is used where the host has multiple bytes of data to be written to consecutive register addresses. It is selected by setting the WRITE MODE control to 0. For Page Write mode the master sends a device address followed by a register address then multiple data bytes. The 2-WIRE interface automatically increments the register address pointer after each data byte is received. The slave acknowledges each received byte of data until the master sends the STOP condition (Figure 28).

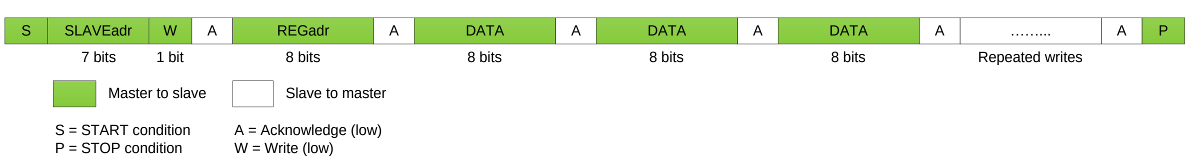


Figure 28: 2-WIRE Page Write (SI/DATA Line)

Repeated Write mode is used where the host has multiple bytes of data to be sent to non-consecutive registers. It is selected by setting the WRITE MODE control to 1. For Repeated Write mode the master sends a device address followed by multiple address-data pairs. The slave acknowledges each received byte until the master sends the STOP condition (Figure 29).

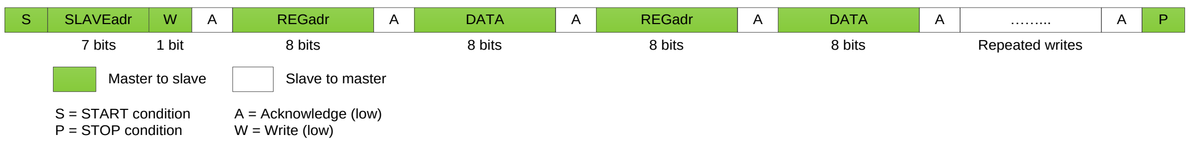


Figure 29: 2-WIRE Repeated Write (SI/DATA Line)

6.8.2 High Speed 2-WIRE Interface

The high speed HS 2-WIRE interface is the alternate serial control bus. It consists of DATA (data line) and CLK (clock line) and can be used as an independent control interface for data transactions between the DA9063 and a second host processor. The DA9063 high speed 2-WIRE interface has a configurable 8-bit write address (default 0xB4) and a configurable read address (default 0xB5). For details of configurable addresses see control IF_BASE_ADDR in Section A.4.2 The interface is enabled if HS2 DATA was selected via configuration control GPIO14_PIN. The bus lines have to be pulled high by external pull-up resistors (2 kΩ to 20 kΩ). GPIO14_TYPE defines the supply rail of the interface (used for input logic levels and the internal pull-up resistors). The controls GPIO15_PIN and GPIO15_WEN are disabled when enabling the interface via GPIO14_PIN.

When the interface receives a read or write command that includes a matching slave address, the DA9063 can trigger the assertion of nIRQ and an optional wake-up event (enabled via GPIO14_WEN). If the nIRQ assertion from interface access is enabled (E_GPI14), it should be masked as long as the HS 2-WIRE is in use. This nIRQ cannot be cleared via the HS 2-WIRE interface because every interface access triggers a re-assertion.

Except for the interface device addresses and the optional wake-up, the characteristics of the HS 2-WIRE interface are identical to the power manager 2-WIRE interface, see Section 6.8.1. High speed mode at 3.4 MHz can be enabled either via master code or continuously via PM_IF_HSM, but it does not support slope control for minimum tfDA specification.

6.9 Voltage Regulators

Three types of low drop-out regulators (LDOs) are integrated on the DA9063: for sensitive analog rails (for example, RF transceiver supply), the low noise regulators offer high PSRR across a wide frequency range; the LDOs provide an optimized PSRR and noise performance with lowest quiescent current. Quiescent current has been optimized for the always-on type regulators.

The regulators employ Dialog Semiconductor's Smart Mirror™ dynamic biasing that guarantees PSRR to be maintained across the full current range. Quiescent current consumption is dynamically adjusted to the load, which improves efficiency at light load conditions. Furthermore, Dialog Semiconductor's Smart Mirror™ technology allows the capacitor to be placed close to the load.

Note
When placing an LDO capacitor remotely from the DA9063, the voltage drop (= load current * parasitic PCB impedance) needs to be considered when configuring the LDO output voltage.

Table 45: Regulator Control

Regulator	Type	V_{OUT} Steps (mV)	Mode	Output Voltage (V)	Supplied Max. Current (mA)	Current Limit LDO/ Bypass (mA)	V_{OUT} Control	Notes
LDO1	Always-on	20		0.6 to 1.86	100	200	DVC variable slew rate	Optional voltage tracking
LDO2	Standard	20		0.6 to 1.86	200	400	DVC variable slew rate	
LDO3	Standard	20	Bypass	0.9 to 3.44	200	400/300	DVC variable slew rate	
LDO4	Standard	20	Bypass	0.9 to 3.44	200	400/200	DVC variable slew rate	
LDO5	Standard	50		0.9 to 3.6	100	200	V_{OUT} programmable	
LDO6	Low noise	50		0.9 to 3.6	200	400	V_{OUT} programmable	
LDO7	Standard	50	Bypass	0.9 to 3.6	200	400/300	V_{OUT} programmable	
LDO8	Standard	50	Bypass	0.9 to 3.6	200	400/400	V_{OUT} programmable	Switching vibration motor driver, common supply with LDO7
LDO9	Low noise	50		0.95 to 3.6	200	400	V_{OUT} programmable	Common supply with LDO10
LDO10	Low noise	50		0.9 to 3.6	300	400	V_{OUT} programmable	Common supply with LDO9
LDO11	Standard	50	Bypass	0.9 to 3.6	300	400/300	V_{OUT} programmable	
LDOCORE	Always-on			2.5 ±2% accuracy	4		V_{OUT} non-programmable	Internal LDO

6.9.1 Regulators Controlled by Software

The regulators can be programmed via the power manager interface. All regulators can be enabled or disabled by a write command to the enable bit LDOxx_EN. Each LDO has two voltage registers for output voltage A and B. The appropriate values are stored in the registers VLDOxx_A and VLDOxx_B. The specific output voltage is selected with the bit VLDOxx_SEL. Changes to this control result in immediate output voltage changes on non-DVC regulators and ramped voltage transitions on DVC-enabled regulators. The output voltage can also be changed by directly re-programming the voltage control register. The sequencer also uses these registers and may write to them: their contents can therefore be found to differ from previous write commands.

For security reasons, the re-programming of registers that may cause damage when being incorrectly programmed (for example, voltage settings) can be disabled with control V_LOCK. This disables write access to registers with an address higher than 0x7F.

6.9.2 Regulators Controlled by Hardware

All regulators can be enabled or disabled under hardware control using GPIO1, 2, or 13. The GPIO port used is defined in register LDOxx_GPI. The output voltages can be switched by the GPIO port between the A and B voltage. The specific GPIO port is defined in register VLDOxx_GPI. After detecting a rising or falling edge at the GPI, the DA9063 configures the related regulators with the status of GPI1, GPI2, or GPI13 (the event bit E_GPI1, E_GPI2, or E_GPI13 is automatically cleared). A parallel write access to the regulator control registers is delayed and later overrides the hardware configuration. The sequencer does not affect regulators controlled via GPIOs.

6.9.3 Power Sequencer Control of LDOs

The power sequencer can control LDO1 to LDO11. The specific time slot of each LDO is defined with bit LDOx_STEP in register bank starting at address 0x83. The sequencer enables and disables each LDO individually depending on the setting of each LDO’s bit LDOx_CONF and LDOx_AUTO. To limit the inrush current, it is recommended to enable a maximum of one regulator (including bucks) per time slot.

If the control OTPREAD_EN is set, the regulator control registers are reloaded from OTP before leaving POWERDOWN mode. During power-up, the sequencer always takes output voltage A (defined in register VLDOxx_A). Therefore it also clears all VLDOxx_SEL bits.

When powering down, the sequencer disables all LDOs, but the LDOs can be configured to remain on by setting bit LDOxx_CONF. In this case the output voltage B is always selected (value programmed in register VLDOxx_B). The related bit VLDOxx_SEL is set by the sequencer accordingly.

Table 46: LDO Power Sequence Voltage

LDO Output Voltage During Power-Up Sequencing			
LDOx_CONF	**LDOx_AUTO**	**LDO**	**Output Voltage**
-	1	gets enabled	A
1	0	gets enabled	A
0		disabled	-
LDO Output Voltage During Power-Down Sequencing			
LDOx_CONF	**LDOx_AUTO**	**LDO**	**Output Voltage**
1	-	remains enabled	B
0		gets disabled	-

The bit DEF_SUPPLY defines the sequencer action for time slot 0. If Bit DEF_SUPPLY is set, all LDOs configured to time slot 0 are enabled or disabled during power-up according to Table 46. If bit DEF_SUPPLY is not set, the LDOs configured to time slot 0 are disabled.

Note
When control bit LDOxx_SL_B is asserted, the LDO enters a forced sleep mode with the lowest quiescent current, but with a reduced maximum output current. The maximum current is reduced because a smaller output driver is used (a partial pass device). Asserting LDOxx_SL_A results in the same forced sleep mode for an LDO when using the type A voltage register. Before wake-up from POWERDOWN mode (processing time slots from domain SYSTEM), the sequencer can configure all regulators with default voltage values from OTP: this allows any previously altered VLDOxx_A and LDOxx_SL_A settings to be reset.

Entering RESET mode automatically disables all regulators except LDO1. LDO1 stays enabled when entering RESET mode and can be used as an always-on supply (staying on even when V_{SYS} drops below VDD_FAULT). However, LDO1 is disabled during NO-POWER, RTC and DELIVERY modes.

6.9.4 Dynamic Voltage Control

LDO1 to 4 include DVC:

- The output voltage can be programmed in 20 mV steps.
- If the feedback signal GP_FB1 is configured to be READY (by asserting PM_FB1_PIN), this port is asserted while slewing and asserts E_DVC_RDY after all voltage and buck regulators have completed slewing.

DVC voltage transitions are handled by the following registers:

- Output voltage setting registers VLDO1_A/VLDO1_B to VLDO4_A/VLDO4_B.
  When writing into a selected voltage control register the output voltage is immediately ramped to the new value. When writing into the non-selected voltage register the ramping is delayed until this register is selected by toggling VLDOxx_SEL.
- The voltage selection registers VLDOx_SEL activate a pre-configured transition to the alternate output voltage. These controls have been grouped together in registers DVC_1 and DVC_2 to better enable synchronized ramping of supply voltages.
- The DVC slew rate for all DVC-enabled regulators can be configured as 10 mV per (0.5, 1.0, 2.0, or 4.0) µs via control SLEW_RATE. Under light load conditions (< 10 mA), the slew rate is less than the programmed value when the output is close to the start and end of the slope This is especially the case for the fastest slew rate settings. The negative slew rate is load dependent and might be lower than the one mentioned above.

6.9.5 Voltage Tracking Mode LDO1

LDO1 is able to follow the output voltage of buck converters BUCKCORE1, BUCKCORE2, or BUCKPRO. The specific buck converter is selected and enabled with the bits LDO1_TRACK. The initial voltage delta between LDO1 and the DC-DC converter is captured and any voltage transition of the buck converter is mirrored to LDO1. Re-programming the LDO1 voltage register has no effect. Although LDO1 shares the ramping speed with the buck converter, the real LDO1 output voltage is also influenced by the load current. When the tracking mode is terminated via bit LDO1_TRACK or the selected buck converter enters shutdown, LDO1 returns to its default output voltage (that is, to the value set in register VLDO1_B or VLDO1_A).

When the buck converter ramping exceeds the maximum or minimum voltage capability of LDO1, further steps below 0.6 V or above 1.86 V result in the temporary saturation of the LDO1 output voltage. The tracked buck converter should not ramp to below 0.6 V while LDO1 tracking is enabled.

The minimum delta voltage between the output of LDO1 and BUCKCORE is achieved by connecting the output of LDO1 to port CORE_SWS_GPIO4 and enabling the internal rail switch for the output of BUCKCORE1 (or dual-phase BUCKCORE) through the assertion of control CORE_SW_INT. In this case, the settings of the CORE_SW rail controller are used to configure the internal switch with the result that this channel of the rail switch controller can no longer drive external switches (GPIO3 may be used as a standard GPIO). The configured LDO1 output voltage should be equal to or slightly lower than V_{BUCK} when closing the switch. DVC transitions on BUCKCORE1 (or BUCKCORE) during this mode require LDO1_TRACK to be programmed to 10.

6.9.6 Pull-Down Resistor

All LDOs have a pull-down resistor at the output when they are disabled. The pull-down resistor can be disabled with bit LDOxx_PD_DIS, and is required when LDOs are used in parallel with another supply. Otherwise the output is pulled to GND.

If an over-voltage occurs (LDO1 to 4: V_{OUT} > 109 % of nominal V_{OUT}, LDO5 to 11: V_{OUT} > 106 % of nominal V_{OUT}), the voltage regulators enable an internal load to discharge the output back to its configured voltage. This can be disabled via LDOxx_PD_DIS.

6.9.7 Bypass Mode and Current Limit

All LDOs feature a current limiting function. For LDOs with a bypass mode (LDO3, 4, 7, 8, and 11), an over-current is indicated with an interrupt. When at least one of these LDOs reaches the current limit for more than 10 ms, an interrupt is raised to the host (during POWERDOWN mode a wake-up sequence is initiated) and the event bit E_LDO_LIM is set. The interrupt IRQ can be suppressed via the mask bit M_LDO_LIM.

If the current limit condition persists for more than 200 ms (indicating a probable short circuit condition), the related LDO is disabled and its LDOx_EN bit is de-asserted. The LDO remains disabled until a new enable occurs (via hardware or software activation). The automatic shutdown of the LDO can be disabled via bit LDO_SD. The host processor can distinguish if the IRQ is related to a temporary over-current or to a permanent shutdown by polling the related bit LDOx_ILIM or checking LDO3_EN, LDO4_EN, LDO7_EN, LDO8_EN, and LDO11_EN.

If the current limit is hit for more than 10 ms but less than 200 ms, the IRQ is generated but the related LDO is not disabled. If the current limit is hit for more than 200 ms and the involved LDO is shut down, the LDO<x>_EN bit is de-asserted. If the over-current spike has stopped before the host is able to read the xx_LIM bits, the LDO that has been in current limit cannot be evaluated.

Changing from LDO to bypass mode and back triggers a change of the output voltage with some over/undershoot during the transition phase.

The LDO accuracy specification is not applicable if the LDO has been configured for bypass mode.

For LDOs operated in bypass mode it is recommended to configure the voltage in the VLDO<x>_A register to the expected output voltage of the LDO. When using the LDO above the normal operating range, it is recommended to set the VLDO<x>_A to 0x40 for LDO 3 and 4 and to 0x20 for LDO 7, 8, and 11.

6.9.8 LDO Supply from Buck Converter

LDO1 to LDO11 can optionally be supplied from a buck output (V_{DD} < 2.8 V). In this mode some specification parameters change:

- at V_{DD} = 1.8 V, the dropout voltage at I_{max} increases by 70 %
- for a supply voltage less than 1.8 V, the LDO dropout voltage is valid only for 1/3 of the standard I_{max} and the current capability decreases with the provided supply voltage.

LDO5 and LDO11 may be supplied from a rail higher than V_{SYS}/CHG_WAKE (for example, the output of a 5 V boost) as long as V_{DD} < 5.5 V.

6.9.9 LDO Sleep Mode for Reduced I_{OUT}

If the required output current is < 10 % of I_{MAX}, the quiescent power can be reduced by setting an LDO into sleep mode. In this mode, the output driver current capability is reduced to 10 % of I_{MAX}. Sleep mode can be set independently for the output voltage A and B by setting bit LDOxx_SL_A or bit LDOxx_SL_B. During LDO sleep mode, the over-current limit of the LDOs with a bypass function (LDO3, 4, 7, 8, and 11) is reduced to 50 %. As a benefit of Dialog Semiconductor's Smart Mirror™ technology, sleep mode is typically not required because the quiescent current taken by the regulator is automatically minimized when operating at low current demands.

6.9.10 Vibration Motor Driver

LDO8 provides a third mode dedicated to drive vibration motors selected via bit LDO8_MODE. In this mode, the voltage regulation circuitry is disabled and no external stabilization capacitor is needed. In comparison to LDO mode, the PWM control is more efficient and allows an instant on and off for the vibrator signal.

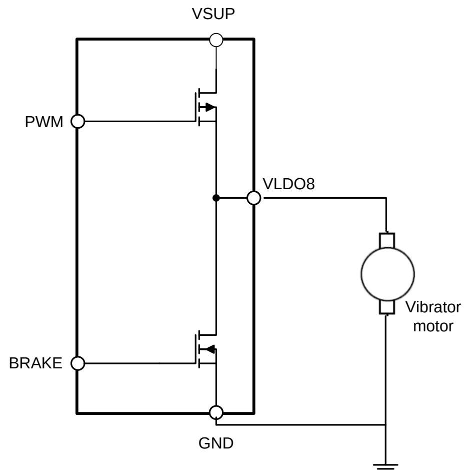


Figure 30: Vibration Motor Driver

The vibrator motor driver is a half-bridge PWM-controlled motor driver, with an automatic battery supply correction of the PWM duty cycle (Figure 30). The PWM base frequency can be selected by PWM_CLK to be either 1.0 MHz or 2.0 MHz (resulting in a PWM repetition rate of 15.6 kHz or 31.25 kHz). The vibration motor speed is determined by the effective output voltage which is set via control VIB_SET (6 bits giving 64 programmable speeds). Setting the output voltage to 0 turns on a braking NMOS transistor to stop the vibration motor immediately.

The motor can also be stopped and started by a level on port nVIB_BRAKE, if enabled via bit PM_FB3_PIN.

The PWM duty cycle is corrected automatically before it is enabled and after each breaking period. It is also automatically corrected every 10 s when it is running for longer periods. These corrections are done via autonomous V_{SYS} measurement via the internal GPADC (overrides control setting of AUTO_VSYS_EN). The duty cycle, D, is given by D = VIB_SET / V_{SYS}.

Note
The half-bridge driver transistors have an internal current limit of approximately 400 mA

6.9.11 Core Regulator LDOCORE

The LDOCORE is a 2.5 V supply dedicated for the internal logic of DA9063. It is used for running the state machine, GPIO pins with comparators, bias, reference, GPADC, OTP, and power manager registers. It is supplied from internal rail V_{DDREF}, powered from either CHG_WAKE or VSYS. When LDOCORE is supplied in RESET mode, its output voltage is temporarily reduced to 2.2 V. In general, LDOCORE is an always-on supply (remaining enabled during RESET mode), but for lowest dissipation power LDOCORE can also be disabled when progressing towards RTC or DELIVERY mode.

6.10 DC/DC Buck Converters

DA9063 includes six DC/DC buck converters with DVC.

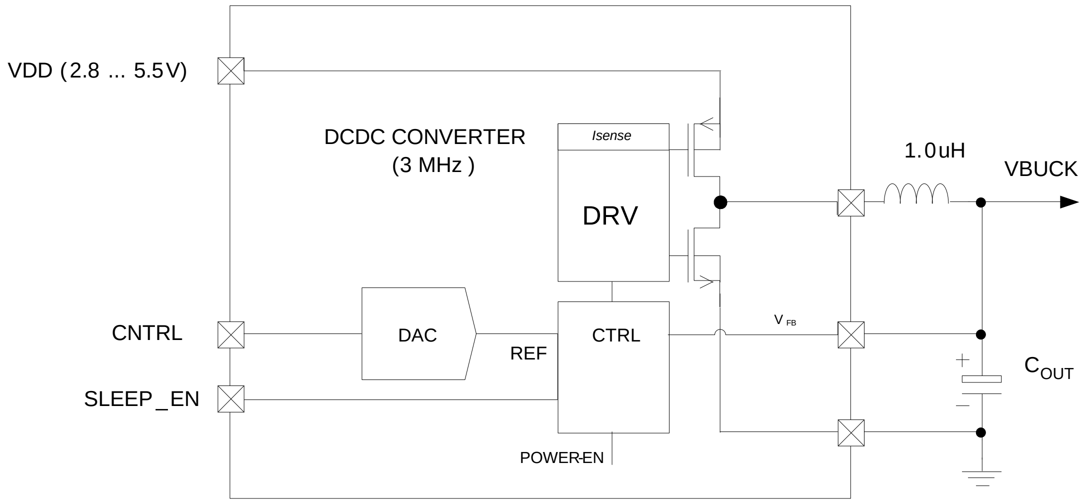


Figure 31: DC-DC Buck Converter

The converters are high efficiency synchronous step-down regulators, operating at a high frequency (3 MHz), supplying individual output voltages with ± 3 % accuracy. The default output voltage is loaded from OTP and can be set in 10 mV steps. To limit in-rush current from V_{SYS}, the buck converters perform a soft-start for up to 3 ms, when enabled via control SOFT_START. During this 3 ms period, the output current of the buck is limited. The use of the SOFT_START feature slows the start-up of the bucks. In the case where the load current exceeds the current limit during the first 3 ms, the output may fail to reach the programmed voltage until the end of the 3 ms period. The start-up sequence may have to be adjusted to take into account the SOFT_START behavior.

The DVC controller allows the following features:

- The buck converter output voltage is programmable over the power manager bus in 10 mV steps.
- If the feedback port GP_FB1 is configured as READY, this port is asserted while slewing and asserts E_DVC_RDY after all voltage and buck regulators have stopped slewing.
- Output voltages below 0.7 V are only supported in Pulse Frequency Modulation (PFM) mode. During a voltage reduction below 0.7 V, the slew rate control ends at 0.7 V and the buck mode is automatically changed to PFM mode.

The DVC control is handled by the following registers:

- Output voltage setting register VBxxxx_A/VBxxxx_B.
  When writing to the voltage control register that is in use by an enabled buck, the output immediately ramps to the new setting. When writing to the voltage control register that is not in use, the ramping is delayed until this register is selected by toggling VBxxxx_SEL.
- The voltage register selection VBxxxx_SEL.
  This activates a pre-configured transition to the alternate output voltage. These controls are grouped into registers DVC_1 and DVC_2 to better enable synchronized ramping of supply voltages.
- The DVC slew rate is programmable as at 10 mV per (4, 2, 1, or 0.5) µs via control SLEW_RATE. During PFM mode, the negative slew rate is load-dependent and might be lower than the programmed rate.

The supply current during PWM (synchronous) operation is in the order of 3.5 mA (quiescent current and charge/discharge current) and drops to <1 µA in shutdown. Switching frequency is chosen to be high enough (3 MHz) to allow the use of a small 1.0 µH inductor.

The operating mode of the buck converter is selected via the buck control register bits B<x>_MODE. The buck converter can be forced to operate in either PWM or PFM mode. Additionally, the buck converter has an automatic mode where it switches between PWM and PFM modes depending on the load current.

The switching converters can be enabled/disabled/configured via the power manager and HS 2-WIRE interface. Writing to Bxxxx_EN/VBxxxx_SEL unconditionally configures the regulator to the selected mode (enabled/disabled). Reading Bxxxx_EN/VBxxxx_SEL provides the actual state, which may differ from a previous write (in the case where the regulator state is changed from GPIO or power sequencer control). All bucks can be controlled with an ID from the power sequencer. If enabled in DEF_SUPPLY, supplies can be configured to default settings when the sequencer passes slot 0.

To limit the inrush current, it is recommended to select individual regulators (including LDOs) only with xxxx_DEF settings.

When powering up, the power sequencer clears VBxxxx_SEL for a buck when it has an ID pointing to the time slot being processed. This forces the regulator to ramp the output voltage to the value programmed inside the related register VBxxxx_A.

When powering down (for example, to POWERDOWN mode), sequencer-controlled supplies are usually disabled but can be configured to remain on by setting Bxxxx_CONF. In the latter case, the sequencer sets VBxxxx_SEL so that the regulator output voltage is ramped to the value programmed inside the related register VBxxxx_B. Disabled bucks can switch off their pull-down resistor, see Section 6.9.5. Before wake-up from POWERDOWN mode (processing time slots from domain SYSTEM), the sequencer can configure the bucks with default voltage values from OTP and reset any changed VBxxxx_A settings.

All buck converters provide an optional hardware enable/disable via GPIO1, 2, and 13. A regulator that has to be enabled/disabled from a GPI port selects this feature via its control Bxxxx_GPI. A change of the output voltage from the state of a GPI is enabled via control VBxxxx_GPI. After detecting a rising or falling edge at the GPI, the DA9063 configures the enabled regulators with the status of GPI1, GPI2, or GPI13 (the event bit E_GPI1, E_GPI2 or E_GPI13 is automatically cleared). A parallel write access to the regulator control registers is delayed and later overrides the HW configuration. The sequencer does not change regulator settings enabled for GPI control. Powering down to RESET mode automatically disables all buck converters. When the output of a buck converter is combined with a parallel low power LDO, its pull-down resistor needs to be disabled via Bxxxx_PD_DIS. Otherwise its output is discharged to GND when being disabled.

To allow DVC transitions under load, the buck current limit should be configured at least 40% higher than the required maximum continuous output current. See Table 47 as a guide to determining this limit.

Table 47: Selection of Buck Current Limit from Coil Parameters

Min. ISAT (mA)	Frequency (MHz)	Buck Current Limit (mA)	Max. Output Current (mA)
3800	3	3400	2400
3100	3	2800	2000
2400	3	2100	1500
1700	3	1700	1200

To ensure correct regulation, the buck converters require the supply voltage to be 0.7 V higher than the output voltage. As this is not always possible at higher output voltage settings, the converters BUCKMEM, BUCKIO, and BUCKPERI provide a follower mode where the electrical characteristics of the DC-DC converter no longer apply, but instead the PMOS output driver is fully-on and the output voltage simply follows the dropping input voltage. There will be a voltage drop between the buck VDD supply and the output which results from the on-resistance of the buck PMOS driver and the coil, with the voltage drop magnitude being depending on load current. Bucks running in follower mode will temporarily stop switching and by that process will generate PWM mode 3 MHz sub-harmonics.

6.10.1 Active Discharge

When switching off a buck converter the output rail can be actively discharged. This feature is enabled by setting BUCK_ACTV_DISCHRG. The discharge is implemented by ramping down the output voltage using DVC.

6.10.2 BUCKCORE1, BUCKCORE2, and BUCKPRO

BUCKCORE1, BUCKCORE2, and BUCKPRO include a full-current (previously overdrive) mode, individually enabled via control BCORE1_OD, BCORE2_OD, and BPRO_OD.

In full-current mode:

- The maximum current capability is 2500 mA
- The selected current limits are automatically doubled
- The quiescent current increases due to the increased switching losses

For full-current mode, the application requires two 47 µF output capacitors and an appropriate inductor that can sustain higher currents without heating up or suffering from inductance degradation.

BUCKCORE1 and 2 can also be merged as a dual-phase BUCKCORE with up to 5000 mA maximum output current. If enabled in OTP via BCORE_MERGE, the register controls of BUCKCORE2 (except BCORE2_PD_DIS) are automatically disabled and the output from both coils must be routed together. The feedback signal for both phases is taken from the sense node switch matrix of BUCKCORE1 (the VBUCKCORE2 pin may be left floating if the internal pull-down resistor is enabled by setting BCORE2_PD_DIS = 0). With BCORE1_FB programmed in OTP to 0b000, a differential remote sensing at the point-of-load can be enabled, using VBUCKCORE2 as a GND sense port. In this mode, the BUCKCORE output capacitor voltage has to be routed to port CORE_SWS or GP_FB_2 (selected via control MERGE_SENSE). Depending on the settings of BCORE1_OD, the dual-phase buck provides a maximum 2500 mA or 5000 mA, requiring two or four 47 µF output capacitors, respectively.

BUCKCORE2 always runs on the inverted clock (anti-phase) of BUCKCORE1. The switching node output of both phases must be connected symmetrically on the PCB (with matched routing inductances and resistances).

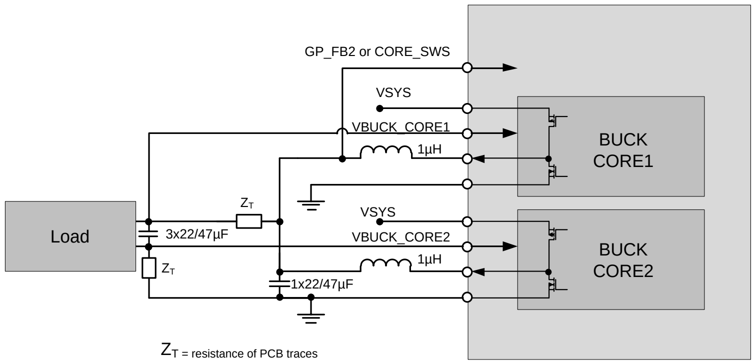


Figure 32: BUCKCORE1 and BUCKCORE2 in Dual-Phase Remote Sense Mode

6.10.3 BUCKPRO in DDR Memory Bus Termination Mode

If enabled via BPRO_VTT_EN, BUCKPRO offers an alternative mode to provide VTT bus termination for DDR memory. In this mode, its output voltage tracks 50 % of the VDDQ sense port voltage (Figure 33). In this mode, BUCKPRO must be set to sync mode either by the host or by OTP configuration. If enabled via BPRO_VTTR_EN, a second VTTR output provides the same voltage for a DDR VTTR reference rail, buffered with ± 10 mA source/sink capability (requires 0.1 µF stabilization capacitor). With BPRO_VTTR_EN being asserted in combination with BPRO_VTT_EN released, the DA9063 provides a VTTR reference buffer with BUCKPRO running in a normal output voltage control mode. If memory termination is not required (BPRO_VTTR_EN = 0), port VDDQ provides the state of event E_GPI2 and port VTTR provides the state of the 1.2 V comparator.

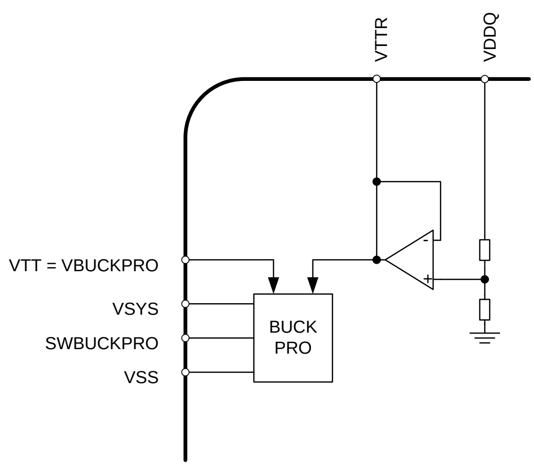


Figure 33: BUCKPRO Memory Bus Termination Mode

6.10.4 BUCKMEM and BUCKIO in Merged Mode

The converter BUCKMEM can be merged with BUCKIO via control BUCK_MERGE to form a single DC-DC converter with a maximum output current of 3000 mA (Figure 34). The routing of the switcher output pins to the common inductor must be symmetrical. The VBUCKIO feedback pin may be left floating in merged mode if its internal pull-down resistor is enabled by setting BIO_PD_DIS = 0. The inductor (1.0 µH) and the output capacitor have to be selected according to the increased output current configuration controls of BUCKIO are disabled by asserting the bit BUCK_MERGE; the selected current limits of BUCKMEM are automatically doubled.

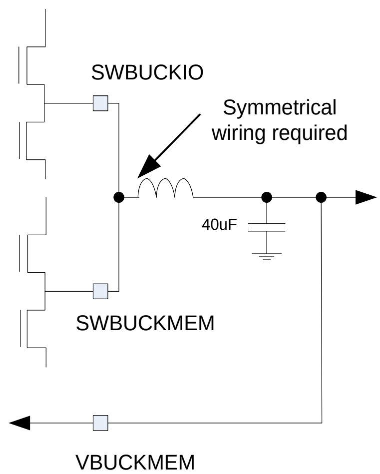


Figure 34: BUCKMEM Merged With BUCKIO

6.11 Buck Rail Switches

BUCKCORE and BUCKPERI offer a gate driver for an external NMOS that allows an output rail shutdown and re-enable independently from the state of the buck (Figure 35). If a switch is open, the associated pin is discharged to VSS by a pull-down resistor. All switch outputs require 100 nF decoupling. All switches provide a soft-start in the form of a slew-rate limit which can be programmed via control SWITCH_SR. The input surge current is therefore linearly proportional to the capacitance connected to the output of the switch.

When the switch is closed, the buck can be configured by control Bxxx_FB to select the switch output signal as a voltage sense node (instead of the buck output voltage) to compensate for losses in the switch. Otherwise, Bxxx_FB should be programmed as 0b001 (setting 0b000 is invalid).

Where a buck does not require a rail switch, it can be routed to the output of another buck. In this case, the feedback control should be programmed to 0b001. The feedback of the buck using both switches may be programmed to be taken from the output of CORE_SW (CORE_SWS) or the output of PERI_SW (PERI_SWS), or even from a mix of both (averaged). When a switch is opened, its signal is automatically disconnected from the feedback path. When all switches selected for the feedback signal mix are open, the buck automatically switches the feedback back to its output.

Before any of the rail switches can be closed, a charge pump must be enabled via control CP_EN. Depending on the setting of CP_EN_MODE, it may be automatically disabled when all buck rail switches are opened. During charge pump automatic mode, closing the first switch is delayed until the charge pump has stabilized its output voltage (< 700 µs).

The state of each switch is controlled via its control xxx_SW_EN. These bits can be modified by a register write or via GPI1, 2, or 13 if enabled by register SWITCH_CONT. Alternatively, they can be controlled from the power sequencer by programming controls xxx_SW_STEP into the intended time slot (which closes the switches on power-up and opens the switches on power-down). By asserting xxx_SW_CONF, the sequencer can be forced to leave the switch closed when powering down.

If a buck rail switch is not required, its ports can instead be used as a GPIO (selected via GPIOxx_TYPE).

Additional rail switches are available by using LDOs 3, 4, 7, 8, and 11 in bypass mode.

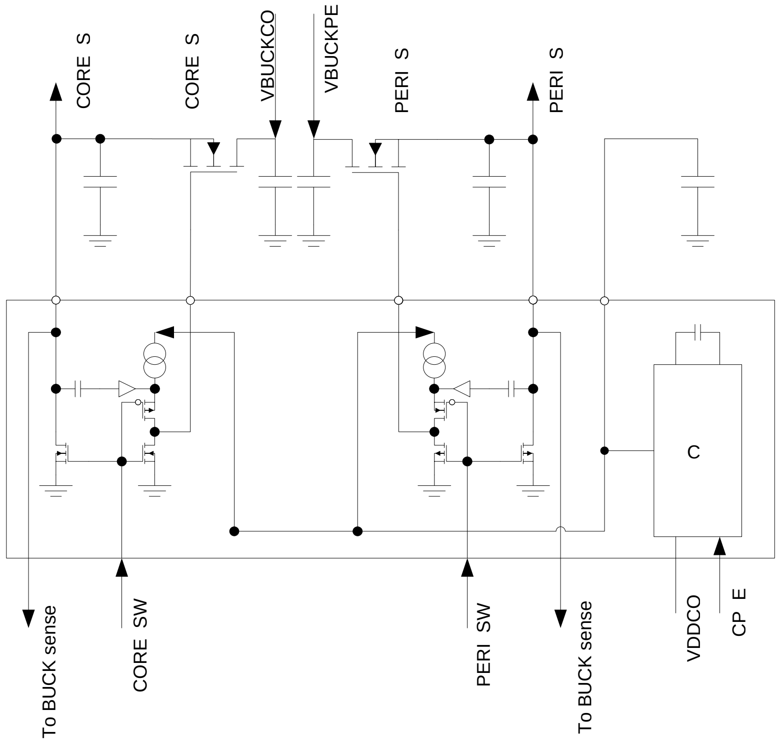


Figure 35: Buck Rail Switches

6.12 Backup Battery Charger/RTC Supply Rail Generator

The backup battery charger provides a constant charge current with a programmable top-up charging voltage for charging of Lithium-Manganese coin cell batteries and super capacitors. Charging current is programmable via BCHG_ISET from 100 to 1000 µA (in 100 µA steps) and from 1 mA to 6 mA (in 1 mA steps). End-of-charge termination voltage is programmable in 100 mV/200 mV steps from 1.1 V to 3.1 V. The backup battery charger is enabled by setting BCHG_VSET and BCHG_ISET to a non-zero value. When enabled, the charger aims to maintain the backup battery at its target voltage. The backup battery charger can be temporarily disabled in POWERDOWN mode via control bit BBAT_DIS and it switches off automatically during a POR.

The backup battery charger includes reverse current protection and can also be used as an ultra-low quiescent always-on supply for low voltage/power rails (may stay on during RESET mode).

The backup battery rail follower provides the internal supply voltage VDDRTC for the 32 kHz oscillator and RTC digital whenever being powered from V_{DDREF} (V_{DDREF} > 2.4 V) or from a backup battery (V_{BBAT} > 2.0 V), depending on the following conditions:

- If only the backup battery is applied (for example, in case of a deep discharged or removed main battery) the switch automatically connects the RTC block to the backup battery.
- If both the system rail V_{DDREF} and the backup battery are present, the RTC block is powered by the higher of these two voltage sources. This implementation allows for maximum utilization of the energy left in the main battery, thus extending the life of the lower capacity backup battery. A seamless transition is achieved by the VDDRTC follower by generating a replica of the backup battery voltage from V_{DDREF} (min. 1.45 V). To limit the oscillation while switching between V_{BBAT} and the internal replica voltage, the backup battery switch has a built-in hysteresis of 75 mV.

6.13 General Purpose ADC

6.13.1 ADC Overview

The Analog to Digital Converter (ADC) uses a sample and hold successive approximation switched capacitor architecture. It is supplied from VDDCORE (2.5 V). Configured via control ADC_MODE, it can be used either in high-speed mode with measurement sequences repeated every 1 ms or in economy mode with sequences repeated every 10 ms.

6.13.2 ADC Input MUX

The DA9063 provides an ADC with 10-bit resolution and track and hold circuitry combined with an analog input multiplexer (Figure 36). The analog input multiplexer allows conversion of up to nine different inputs. The track and hold circuit ensures stable input voltages at the input of the ADC during the conversion.

The ADC is used to measure the following inputs:

- Channel 0: VSYS_RES – measurement of the system VDD (2.5 to 5.5 V)
- Channel 1: ADCIN1_RES – high impedance input (0 to 2.5 V)
- Channel 2: ADCIN2_RES – high impedance input (0 to 2.5 V)
- Channel 3: ADCIN3_RES – high impedance input (0 to 2.5 V)
- Channel 4: T_J – measurement of internal temperature sensor
- Channel 5: V_{BBAT} – measurement of the backup battery voltage (0 to 5.0 V)
- Channel 8: MON_A8_RES – group 1 internal regulators voltage (0 to 5.0 V)
- Channel 9: MON_A9_RES – group 2 internal regulators voltage (0 to 5.0 V)
- Channel 10: MON_A10_RES – group 3 internal regulators voltage (0 to 5.0 V)

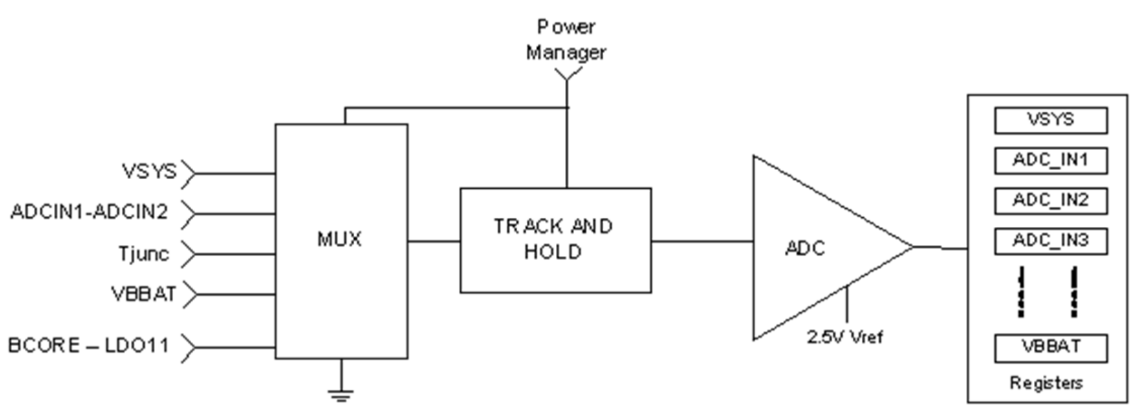


Figure 36: ADC Block Diagram

The MUX selects from and isolates the nine inputs, and presents the channel to be measured to the ADC input. When selected, an input amplifier on the V_{SYS} channel subtracts the VDDCORE reference voltage and scales the signal to the correct value for the ADC.

6.13.3 Manual Conversion Mode

Manual measurements by the ADC are initiated by an ADC_MAN bit register write. The ADC powers up, one conversion is done on the channel specified by ADC_MUX and the 10-bit result is stored in the ADC_RES_H and ADC_RES_L registers. After the conversion is completed, the ADC powers down again, ADC_MAN bit is reset and an IRQ event flag is set (E_ADC_RDY). The generation of this IRQ can be masked by the IRQ mask M_ADC_RDY.

6.13.4 Automatic Measurements Scheduler

The automatic measurement scheduler allows monitoring of the system voltage V_{SYS}, the auxiliary channels ADCIN1 to 3 and the output voltage supervision of embedded regulators. The results are automatically compared with upper and lower thresholds set by power manager registers to give an nIRQ event if a measurement is outside these levels. All measurements are handled by the scheduler system detailed below.

The scheduler performs a sequence of 10 slots continually repeated according to the configured mode. A slot requires 100 µs. The pattern of measurements over the 10 slots depends upon the enabled automatic measurements. Additional manual measurement opportunities are available in slots where automatic measurements have been disabled by control bits in ADC_CONT. Automatic measurements only store the eight MSBs of the ADC measurement.

Figure 37 shows (with typical configurations) how the different measurements are scheduled.

Example sequence of AUTO-ADC measurements

Slot No	0	1	2	3	4	5	6	7	8	9
	A0	A8	M	A1	A9	M	A2	A10	M	A3

Each Slot allows 1 automatic or manual measurement to be made
A0 - Automatic measurement of VSYS (mux channel 0)
A1 - Automatic measurement of ADCIN1 (mux channel 1)
A2 - Automatic measurement of ADCIN2 (mux channel 2)
A3 - Automatic measurement of ADCIN3 (mux channel 3)

A8 - Automatic measurement of multiplexed regulator output voltages (mux channel 8)
A9 - Automatic measurement of multiplexed regulator output voltages (mux channel 9)
A10 - Automatic measurement of multiplexed regulator output voltages (mux channel 10)

M indicates time slots when a Manual measurement can be made

Figure 37: ADC Sequence

6.13.4.1 A0: V_{SYS} Voltage nIRQ Measurement Mode

V_{SYS} is measured, stored in VSYS_RES and compared with the VSYS_MON threshold. If the result of the comparison is different to its previous state (being either lower or higher) for three consecutive readings, an E_VDD_MON event is generated. Glitches of a duration less than three consecutive measurements do not update the state; events are triggered at rising and falling edges of the state signal. This multiple reading debounces the V_{SYS} voltage before issuing an nIRQ. After the nIRQ assertion, the automatic measurement of channel V_{SYS} is paused for reading. The host must clear the associated event flag to re-enable the supervision of V_{SYS}. The event-causing value is kept in the result register.

If selected via GPIO12_PIN, the debounced comparator state can be indicated via the GPO12 port, representing a power good signal that can be used, for example, to trigger boot activities on external ICs. If no action is taken to restore the V_{SYS} voltage (that is, discharging of the battery continues), the host may consider switching off optional 'always-on' blocks (for example, backup battery) to save energy later on. V_{SYS} measurements are enabled via control AUTO_VSYS_EN.

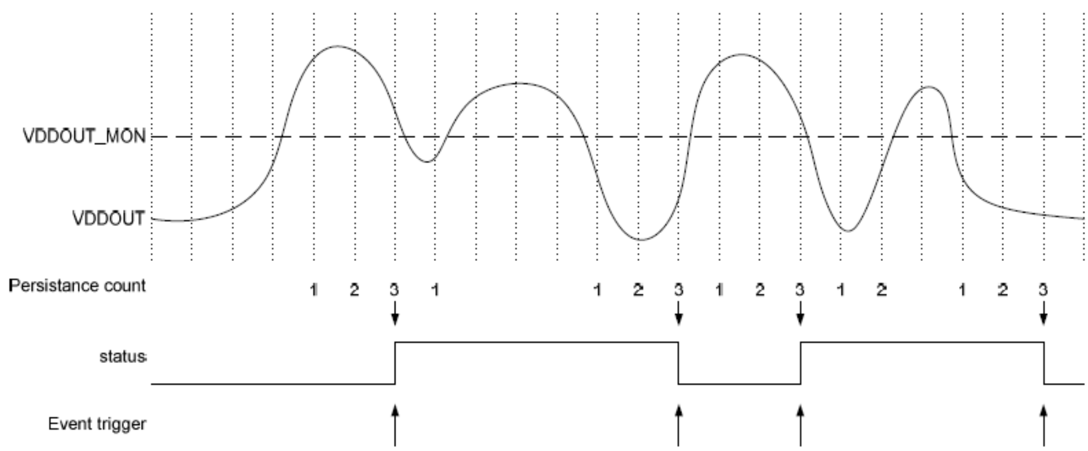


Figure 38: V_{SYS} Monitor Persistence Behavior

6.13.4.2 A1, A2, A3: Automatic Measurement and High/Low Threshold Warning nIRQ Mode

The automatic measurement result of channel ADC_IN1 is stored in the ADCIN1_RES register. If a reading of A1 is less than AUTO1_LOW or greater than AUTO1_HIGH, then the event flag E_GPI0 is set. If nIRQ is asserted, the automatic measurement of channel ADC_IN1 is paused until the host has cleared the associated event flag (the event-causing value is kept in the result register). The assertion of nIRQ can be masked by IRQ mask M_GPI0, which also disables the pausing of automatic measurements. If debouncing is selected via ADCIN1_DEB the event is only asserted if two consecutive measurements override the same threshold. The automatic measurement is enabled by register AUTO_AD1_EN. In addition, it is possible to use ADCIN_1 with a 1 µA to 40 µA current source that allows automatic measurement of a resistor value (programmed via ADCIN1_CUR). The current source is enabled by AD1_ISRC_EN. During automatic measurements the enabled current source is dynamically switched off at the end of the conversion and switched on one slot prior to the next ADCIN_1 measurement (to enable minimum current consumption, and allow any external capacitance voltage to settle); otherwise its status is static.

A similar functionality is available at ADC_IN2 and ADC_IN3. ADC_IN2 provides notification to the processor via a fixed voltage comparator (also available when ADC is powered down) but the ADCIN2 current source is static (no dynamic switch-off at the end of automatic conversion). The input selection switch of ADC_IN2 provides an enhanced isolation (80 dB typ.) between the externally-connected circuit and the internal ADC block (for example, allowing the DC supervision of noise sensitive audio lines).

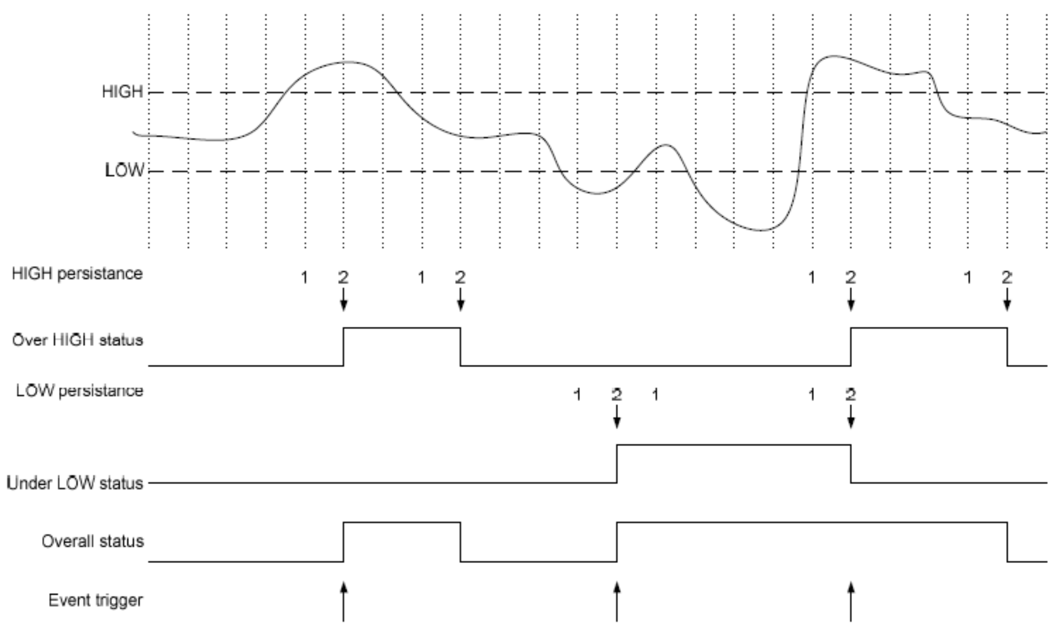


Figure 39: A1, A2, A3 Persistence Behavior

6.13.4.3 A8, A9, A10: Automatic Regulator Monitor with Under- Or Over-Voltage Shutdown

DA9063 provides the capability to monitor the output voltage of internal regulators. In case of a catastrophic failure, the related regulator is disabled. This feature is enabled using control MON_MODE. Each internal regulator is assigned to a GPADC input channel and can be individually enabled for monitoring via controls BCORE1_MON_EN to LDO11_MON_EN. For example, if ADC channel A8 is connected to an enabled regulator and it is also enabled for monitoring, the ADC automatically measures the regulator output voltage every 1 ms (10 ms in ADC economy mode). Simultaneously, two relative thresholds are calculated from the regulator nominal output voltage (supporting DVC). If the regulator is out of range, the voltage measurement is stored inside MON_A8_RES, the regulator ID is recorded inside the index MON_A8_IDX and the event flag E_REG_UVOV is set. To secure a stable output voltage, the monitoring is delayed after regulators are switched on and when changing their voltage level to a new target (that is, during DVC slewing, after writing into the active regulator voltage register, or when the active voltage control register is changing between Vxxx_A and Vxxx_B). This delay is programmable using control UVOV_DELAY.

If debouncing is selected via MON_DEB, an event is only created if two consecutive measurements exceed the same threshold. The feature is also available for channels A9 and A10.

Table 48: Assignment of Regulators for Voltage Monitoring

ADC Channel	Regulator	Enable
A8	BUCKCORE1 BUCKCORE2 BUCKPRO LDO3 LDO4 LDO11	BCORE1_MON_EN BCORE2_MON_EN BPRO_MON_EN LDO3_MON_EN LDO4_MON_EN LDO11_MON_EN
A9	BUCKIO BUCKMEM BUCKPERI LDO1 LDO2 LDO5	BIO_MON_EN BMEM_MON_EN BPERI_MON_EN LDO1_MON_EN LDO2_MON_EN LDO5_MON_EN
A10	LDO6 LDO7 LDO8 LDO9 LDO10	LDO6_MON_EN LDO7_MON_EN LDO8_MON_EN LDO9_MON_EN LDO10_MON_EN

If more than one regulator is assigned to A8, A9, or A10, the regulator measurements are sequentially multiplexed on this channel (elongates the measurement period of 1 ms or 10 ms by each additional assigned regulator). In the case of an E_REG_UVOV event, the regulator monitoring continues and shuts down rails facing catastrophic failure (voltage and IDX controls contain information for determining the cause of the most recently detected under- or over-voltage). When clearing E_REG_UVOV via a host write, the related regulator index controls are reset. In the unlikely case in which several regulators from a sequenced ADC channel have triggered an under- or over-voltage condition before the host was able to read the related controls, all monitored supplies may be checked for their actual state (enabled or shutdown) to detect if further supplies have also been shut down in addition to the one captured by the index control.

The assertion of nIRQ can be masked by IRQ mask M_REG_UVOV. With a masked nIRQ from regulator supervision, the setting of MON_RES determines whether an out-of-range detection disables the related regulator or triggers the assertion of port nRESET. In the latter case, nRESET is asserted for 1 ms and continues to be asserted until the regulator returns to being in range (regulators that are not enabled but are selected for monitoring do not trigger the assertion of nRESET). With a masked nIRQ, GP_FB2 can be configured to flag PWR_OK, indicating that all monitored regulator voltages are in-range. Selecting disabled regulators for monitoring suppresses the assertion of PWR_OK.

Note
Voltage monitoring function cannot be used for any LDO in bypass mode.

The regulator monitor unit provides alternative modes selected via MON_MODE. In measurement-only mode, the event flag E_REG_UVOV is set for every automatic measurement result being available on either A8, A9, or A10 (with a maximum of one regulator per channel being enabled for measurements). When enabled, an auto-measurement on A8, A9, or A10 allows the host to get its actual output voltage from registers MON_A8_RES to MON_A10_RES. When multiple ADC channels are enabled for automatic regulator voltage measurements, the burst measurement mode may reduce the control interface traffic and number of nIRQ assertions. When the ADC time slot of A10 has finished, the event flag E_REG_UVOV is set (independent of A10 being enabled for auto-measurements). The host can then read the measurement results stored inside MON_A8_RES - MON_A10_RES as a block. During measurement modes, there are no threshold comparisons or regulator shutdowns. If the nIRQ line was asserted, automatic measurements on channels A8 (A9 and A10) are paused until the host has cleared the associated event flag (the event-causing value is kept in the result registers). During measurement modes, E_REG_UVOV is cleared by writing the read value into register EVENT_B. To sequentially measure other regulators on ADC input channels A8, A9, and A10, the host has to set the monitor enable for the next measurement slot to the required regulator before clearing the event. The assertion of nIRQ can be masked by IRQ mask M_REG_UVOV, which also disables the pausing of automatic measurements. For further information about voltage monitoring, please see DA9063 Voltage Monitoring [2].

Note
Voltage monitoring function cannot be used for any LDO in bypass mode.

6.13.4.4 A4 and A5: Manual Measurement T_J and V_{BBAT}

The 10-bit result of manual measurements is stored in the registers ADC_RES_L and ADC_RES_H. Channel 4 (T_J) is used to measure the output of the internal temperature sensor (generated from a proportional to absolute temperature (PTAT) current using a bandgap reference circuit). The ADC measurement result and the T_OFFSET value can be used by the host to calculate the internal junction temperature, defined by the following formula:

$$T_J\ [°C] = -0.398 * (ADC - T\_OFFSET) + 330$$

Channel 5 can be used to measure the voltage of the backup battery.

Manual measurements on A8 to A10 are possible, but require disabling the automatic measurements on these channels and also ensuring that only one regulator is connected to each of these ADC channels.

NOTE
The T_OFFSET value is stored in the T_OFFSET register at address 0x104 during manufacture.

6.13.5 Fixed Threshold Comparator

A comparator with a threshold of 1.2 V is connected to the input of ADC channel 2. The comparator is asserted when the input voltage exceeds or drops below 1.2 V for at least 10 ms (debouncing). After being enabled via COMP1V2_EN, the status flag COMP1V2 indicates the actual state and a maskable interrupt request E_COMP1V2 is generated at the falling and rising edge state transitions.

The comparator may be disabled via COMP1V2_EN when auto-measurements with high resolution are executed on ADCIN2.

6.14 Real Time Clock

The RTC circuit maintains the real time clock and alarm functions. The variable RTC supply voltage, VDDRTC, is derived from V_{BBAT}. Generally, the RTC block is powered from V_{DDREF}, but with RTC_EN asserted, the DA9063 enters a special low-power RTC mode under the following conditions:

- Unconditionally, when the V_{BBAT} (the backup battery supply) is the only available voltage source in the system (no external charger or main battery). DA9063 enters RTC mode automatically since all the other supply domains are down (V_{DDREF} < VPOR_LOWER).
- If the RTC_MODE_PD control bit is set (from OTP or host) and the power sequencer reaches slot 0 during a power transition from ACTIVE to POWERDOWN mode. The above condition disables LDOCORE and powers down all blocks (that are unrelated to the RTC circuit operation).
- Similar to the above case, the device goes in to RTC mode if RTC_MODE_SD control bit is set (from OTP or host) and the main PM control logic reaches RESET mode in the presence of a V_{SYS} fault.

The following conditions (edge sensitive) that re-enable the DA9063's full control logic (terminating RTC mode):

- V_{DDREF} rising to > 2.6 V (unconditionally)

  There is no dedicated event bit. A start-up with POR asserted but no asserted E_WAKE, E_nONKEY, E_TICK, or E_ALARM event bit indicates main battery insertion. Depending on the V_{SYS} rise timing and final level, an E_VDD_WARN or E_VDD_MON wake-up event may be triggered which, if not masked via M_VDD_WARN and M_VDD_MON in OTP, will cause an application power-up, even when AUTO_BOOT is cleared in OTP.
- External charger insertion via CHG_WAKE in the presence of a valid V_{DDREF} supply (V_{DDREF} > 2.6 V)
- Assertion of nONKEY in the presence of a valid V_{DDREF} supply (V_{DDREF} > 2.6 V)
- Alarm/tick event when there is a valid V_{DDREF} supply (V_{DDREF} > 2.6 V; alarm event is otherwise stored in case this condition later becomes true)

The above assertions from nONKEY or CHG_WAKE must remain until LDOCORE is able to leave the POR state, otherwise the DA9063 relapses back into RTC mode.

6.14.1 32 kHz Oscillator

The clock oscillator circuit is used to drive the RTC. It works with an external piezoelectric oscillator crystal at 32.768 kHz and is enabled via control CRYSTAL. If enabled, the DA9063 biases the crystal when leaving DELIVERY or NO-POWER mode, which starts up the oscillator. By asserting RTC_EN, the crystal remains biased (the RTC continues to run).

Note
When the 32 kHz oscillator is disabled, an external oscillator signal may be applied to port XOUT (the signal is forwarded phase-inverted).

In order to achieve the desired crystal frequency, an external capacitor (10 pF to 20 pF, depending on the parasitic capacitance of the board) should be connected to ground from each of the crystal pins. The start-up time of the oscillator is typically 0.5 s to 1 s. The XTAL pins should be grounded when the crystal is not mounted and when not being driven by an external oscillator signal. The 32 kHz clock signal is available at the OUT_32K port and the buffer can be enabled/disabled from the host via control EN_32KOUT. The 32 kHz signal can also be made available at GP_FB3 (enabled via control PM_FB3_PIN).

6.14.1.1 First Power-Up Sequencing after Enable of 32 kHz Oscillator (ID EN32K_STEP)

When the oscillator is enabled (when asserting control CRYSTAL, or when leaving DELIVERY or NO-POWER mode with CRYSTAL already asserted), OUT_CLOCK determines whether the clock provision at OUT_32K (GP_FB3) is gated by a timer. This enables the clock output only when the oscillator signal has become stable. The control RTC_CLOCK provides a similar gating function prior to the clock signal being fed into the internal RTC counter. The stabilization timer (configured via STABILIZATION_TIME) can either be started immediately or be configured to wait until the clock's duty cycle is within the range 30-70% (selected via DELAY_MODE). When powering up before the stabilization timer has expired, ID EN32K_STEP forces the sequencer to wait for timer expiry, which allows a correlation of the 32 kHz signal being provided to outputs with other power up actions following the enable of the 32 kHz oscillator. When reaching ID EN32K_STEP with OUT_CLOCK being released, the gating of the 32 kHz signal is terminated immediately. ID EN32K_STEP is not processed by the sequencer powering-down, nor during consecutive sequencing powering-up.

6.14.1.2 Other Power-Up and -Down Sequencing (ID PD_DIS_STEP)

If the power sequence does not contain the sequencer ID EN32K_STEP, the control OUT_32K_PAUSE from ID PD_DIS_STEP can be used to control the dedicated clock output port OUT_32K in relation to other sequencer actions when powering up and down. The same is true for any sequencing following the first signal provision to port OUT_32K in case the power sequence contains ID EN32K_STEP.

Clearing control crystal enables the provision of the 32 kHz signal from an external clock source connected to the XOUT pin, see Table 49. The provision of external clock signals is not timing controlled and the sequencer ID EN_32K immediately progresses in this case. The crystal input pins can withstand leakage currents corresponding to connected resistances at least as low as 10 MΩ, connected between the pin and any signal level between V_{DDREF} and GND.

Table 49: 32 kHz Oscillator Modes

Power Mode	Conditions	V_{DDREF}	V_{BBAT}	VDDCORE	RTC_EN	CRYSTAL	RTC clock	OUT_32K
NO-POWER	No operation, supplies < ~2V	0	0	0	x	x	-	-
DELIVERY	No operation, though powered	0	1	0	0	x	-	-
		1	x	0 Note 1	0	x	-	-
RTC	Only RTC and Alarm operating from external clock	1	x	0 Note 1	1	0	EXT	-
		x	1					
	Only RTC and Alarm operating from internal crystal oscillator	1	x	0 Note 1	1	1	OSC	-
		x	1					

Power Mode	Conditions	V_{DDREF}	V_{BBAT}	VDDCORE	RTC_EN	CRYSTAL	RTC clock	OUT_32K
ACTIVE	Half-current operation, RTC and alarm off using external clock	1	x	1 Note 2	0	0	-	EXT
	Half-current operation, RTC and alarm on using external clock	1	x	1 Note 3	1	0	EXT	EXT
	Half-current operation, RTC and alarm off using internal crystal oscillator	1	x	1 Note 2	0	1	-	OSC Note 4
	Half-current operation, RTC and alarm on using internal crystal oscillator	1	x	1 Note 3	1	1	OSC	OSC

Note 1 Requires nOFF or nSHUTDOWN to be asserted during V_{DDREF} rising, or a power-down transition from ACTIVE mode with RTC_MODE_PD or RTC_MODE_SD being enabled

Note 2 Triggered from nONKEY press, assertion of CHG_WAKE or V_{DDREF} rising towards > 2.6 V

Note 3 Triggered from nONKEY press, assertion of CHG_WAKE, alarm/tick event or V_{DDREF} rising towards > 2.6 V

Note 4 RTC_EN = 0 causes an initially unstable clock signal when entering half-current mode

The timekeeping error from the frequency variance of crystal oscillators (typ. ±20 ppm) can be trimmed individually during the application end test via the OTP-programmable register TRIM_CLDR by ± 242 ppm with a resolution of 1.9 ppm (1/[32768 * 16]). More advanced solutions can dynamically correct even the temperature related oscillator frequency drift (> 100 ppm) using a periodic temperature measurement located close to the crystal. The timekeeping correction is applied only to the RTC calendar counter. Because of potential clock jitter issues, the 32 kHz clock signal at the OUT_32K pin provides the original frequency of the crystal.

6.14.2 RTC Counter and Alarm

The RTC counter counts the number of 32 kHz clock periods, providing a sec, min, hrs, day, month, and year output. Year 0 corresponds to 2000. It is able to count up to 63 years. The value of the RTC calendar is read-/write-able via the power manager communication. A read of COUNT_S (seconds) latches the current RTC calendar count into the registers COUNT_S through to COUNT_Y (coherent for approx. 0.5 s), so to obtain an updated calendar value requires a read of COUNT_S. Registers are only valid when RTC_READ status bit is asserted (assertion may take several milliseconds from leaving POR).

There is an alarm register containing sec, min, hrs, day, month, and year. When the RTC counter register value corresponds to the value set in the alarm, an IRQ event is triggered and a wake-up is triggered if the DA9063 is in POWERDOWN mode. The trigger also sets a bit in an event register to notify that an alarm has occurred. The alarm can alternatively be asserted from a periodic ‘tick’ signal that, depending on control TICK_TYPE, is either asserted every second or minute.

Note
After modifying TICK_TYPE or TICK_WAKE, a write to register ALARM_Y is required to activate the new settings.

The power manager controls, ALARM_ON and TICK_ON, enable/disable the alarm and tick.

The power manager register bit MONITOR is set to 0 each time the RTC is powered up. Software should set this bit to 1 when setting the time and date which allows software to detect a subsequent loss of the clock. Values written into the RTC calendar and alarm registers must be valid for the associated units of calendar time, for example less than 60 for second and minute registers, see register description for further details.

The RTC registers SECOND_A to SECOND_D define a 32-bit seconds counter (approx. 136 years) that can only be reset after powering up from NO-POWER mode. A read of SECOND_A (seconds counter LSBs) latches the full 32-bit counter into the registers SECOND_A to SECOND_D (coherent for approx. 0.5 s), so that receiving an updated counter value requires a read of SECOND_A. After MONITOR has been set, any host write to CRYSTAL and RTC_EN is prohibited to ensure that the SECOND_A to SECOND_D counters are never stopped.

6.15 Adjustable Frequency Internal Oscillator

An internal oscillator provides a nominal 6.0 MHz clock that is divided down to 3.0 MHz for the buck converters. It is divided down to control the digital core, timers, PWM units, charge pump and ADC. The frequency of the internal oscillator is adjusted during the initial start-up sequence of the DA9063 to within 5 % of the nominal 6.0 MHz. It can be adjusted further within ±10% via register control OSC_FRQ. The tolerance of this frequency affects most absolute timer values and PWM repetition rates (for example, LED and vibrator mode drivers) of the DA9063.

6.16 Reference Voltage Generation: VREF, VLNREF

The DA9063 includes a temperature-independent voltage reference circuit which is derived from an internal band-gap reference and OTP-trimmed buffer amplifier. The output voltage on VREF is trimmed to 1.2 V and the reference is decoupled by an external capacitor on the VREF pin. A lower voltage instance of VREF is provided at VLNREF (0.9 V) and used for the LDOs. These pins must not be loaded. The IREF pin provides the internally used accurate current bias and requires an external 200 kΩ precision resistor.

6.17 Thermal Supervision

The application must ensure that the DA9063 junction temperature does not exceed 125 °C. To protect the DA9063 from damage due to excessive power dissipation, the internal temperature is continuously monitored. Whenever the junction temperature is higher than TEMP_WARN = 125 °C, an E_TEMP event is asserted and an IRQ is generated for the host. If this occurs during POWERDOWN mode, a wake-up is triggered.

The host may then check the exact junction temperature by a manual measurement on GPADC channel 4. An 8-bit OTP register (T_OFFSET) can be used to store its offset at a known temperature (for example 50 °C) to improve the absolute accuracy, which should then be ±7 °C of the measured silicon die junction temperature. This T_OFFSET can be used by the host to calculate the absolute die temperature.

The absolute die junction temperature can be calculated by the host using the result from the ADC channel 4 measurement result and the T_OFFSET trim values.

When the junction temperature exceeds 125 °C, it is recommended to shut down optional functions of the application allowing the DA9063 to cool. When the junction temperature increases further, exceeding TEMP_CRIT = 140 °C, the fault flag TEMP_CRIT is asserted in the FAULT_LOG register and the DA9063 immediately shuts down to RESET mode. The fault condition remains as long as the junction temperature is higher than TEMP_WARN. The TEMP_CRIT flag can be evaluated by the application after the next power up. Whenever the junction temperature exceeds TEMP_POR = 150 °C, a POR to the digital core is immediately asserted and this stops all functions of the DA9063 except for the RTC. This is necessary to prevent the possibility of permanent device damage.

6.18 Main System Rail Voltage Supervision

Two comparators supervise the system supply V_{SYS}. One is monitoring the under-voltage level ($V_{DD\_FAULT\_LOWER}$) and the other is indicating a good system supply ($V_{DD\_FAULT\_UPPER}$). The $V_{DD\_FAULT\_LOWER}$ threshold is OTP configurable and can be set via the VDD_FAULT_ADJ register from 2.5 V to 3.25 V in 50 mV steps. The $V_{DD\_FAULT\_UPPER}$ threshold is also OTP configurable and can be set via the VDD_HYST_ADJ register from 100 mV to 450 mV higher than the $V_{DD\_FAULT\_LOWER}$ threshold. V_{SYS} dropping below the $V_{DD\_FAULT\_UPPER}$ threshold asserts the event E_VDD_WARN. If the event is not masked, this issues an interrupt, which can be used by the host processor as an indication to decrease its activity.

If V_{SYS} drops below $V_{DD\_FAULT\_LOWER}$ for more than 100 ms, the supply error flag VDD_FAULT (in register FAULT_LOG) is asserted and a shutdown sequence to RESET mode is triggered, see Section 6.2.3. The nRESET output is asserted at the beginning of the shutdown sequence. The status can also be reported using a dedicated nVDD_FAULT signal, see Section 6.1.11.

7 Register Map

This section provides an overview of the registers. A description of each register is provided in 11.

Hex	Register	7	6	5	4	3	2	1	0
PAGE 0									
00	PAGE_CON	Revert	WRITE_MODE	Reserved			REG_PAGE		
System Control and Event Registers (SYSMON)									
01	STATUS_A	Reserved				COMP1V2	DVC_BUSY	WAKE	nONKEY
02	STATUS_B	GPI7	GPI6	GPI5	GPI4	GPI3	GPI2	GPI1	GPI0
03	STATUS_C	GPI15	GPI14	GPI13	GPI12	GPI11	GPI10	GPI9	GPI8
04	STATUS_D	LDO11_LIM	LDO8_LIM	LDO7_LIM	LDO4_LIM	LDO3_LIM	Reserved		
05	FAULT_LOG	WAIT_SHUT	nSHUTDOWN	KEY_RESET	TEMP_CRIT	VDD_START	VDD_FAULT	POR	TWD_ERROR
06	EVENT_A	EVENTS_D	EVENTS_C	EVENTS_B	E_SEQ_RDY	E_ADC_RDY	E_TICK	E_ALARM	E_nONKEY
07	EVENT_B	E_VDD_WARN	E_VDD_MON	E_DVC_RDY	E_REG_UVOV	E_LDO_LIM	E_COMP_1V2	E_TEMP	E_WAKE
08	EVENT_C	E_GPI7	E_GPI6	E_GPI5	E_GPI4	E_GPI3	E_GPI2	E_GPI1	E_GPI0
09	EVENT_D	E_GPI15	E_GPI14	E_GPI13	E_GPI12	E_GPI11	E_GPI10	E_GPI9	E_GPI8
0A	IRQ_MASK_A	Reserved			M_SEQ_RDY	M_ADC_RDY	M_TICK	M_ALARM	M_nONKEY
0B	IRQ_MASK_B	M_VDD_WARN	M_VDD_MON	M_DVC_RDY	M_REG_UVOV	M_LDO_LIM	M_COMP_1V2	M_TEMP	M_WAKE
0C	IRQ_MASK_C	M_GPI7	M_GPI6	M_GPI5	M_GPI4	M_GPI3	M_GPI2	M_GPI1	M_GPI0
0D	IRQ_MASK_D	M_GPI15	M_GPI14	M_GPI13	M_GPI12	M_GPI11	M_GPI10	M_GPI9	M_GPI8
0E	CONTROL_A	CP_EN	M_POWER1_EN	M_POWER_EN	M_SYSTEM_EN	STANDBY	POWER1_EN	POWER_EN	SYSTEM_EN
0F	CONTROL_B	BUCK_SLOWSTART	Reserved		nONKEY_LOCK	nRES_MODE	RESET_BLINKING	WATCHDOG_DIS	CHG_SEL
10	CONTROL_C	DEF_SUPPLY	SLEW_RATE		OTPREAD_EN	AUTO_BOOT	DEBOUNCING		
11	CONTROL_D	BLINK_DUR		BLINK_FRQ			TWDSCALE		
12	CONTROL_E	V_LOCK	PM_FB3_PIN	PM_FB2_PIN	PM_FB1_PIN	ECO_MODE	RTC_EN	RTC_MODE_SD	RTC_MODE_PD

Hex	Register	7	6	5	4	3	2	1	0
13	CONTROL_F	Reserved					WAKE_UP	SHUTDOWN	WATCHDOG
14	PD_DIS	PMCONT_DIS	OUT32K_PAUSE	BBAT_DIS	Reserved	HS2IF_DIS	PMIF_DIS	GPADC_PAUSE	GPI_DIS
GPIO Control Registers (GPIO)									
15	GPIO0-1	GPIO1_WEN	GPIO1_TYPE	GPIO1_P IN		GPIO0_WEN	GPIO0_TYPE	GPIO0_P IN	
16	GPIO2-3	GPIO3_WEN	GPIO3_TYPE	GPIO3_P IN		GPIO2_WEN	GPIO2_TYPE	GP IO2_P IN	
17	GPIO4-5	GPIO5_WEN	GPIO5_TYPE	GP IO5_P IN		GPIO4_WEN	GPIO4_TYPE	GP IO4_P IN	
18	GPIO6-7	GPIO7_WEN	GPIO7_TYPE	GPIO7_P IN		GPIO6_WEN	GPIO6_TYPE	GPIO6_P IN	
19	GPIO8-9	GPIO9_WEN	GPIO9_TYPE	GPIO9_PIN		GPIO8_WEN	GPIO8_TYPE	GPIO8_P IN	
1A	GPIO10-11	GPIO11_WEN	GPIO11_TYPE	GPIO11_P IN		GPIO10_WEN	GPIO10_TYPE	GPIO10_P IN	
1B	GPIO12-13	GPIO13_WEN	GPIO13_TYPE	GPIO13_P IN		GPIO12_WEN	GPIO12_TYPE	GPIO12_P IN	
1C	GPIO14-15	GPIO15_WEN	GPIO15_TYPE	GPIO15_P IN		GPIO14_WEN	GPIO14_TYPE	GP IO14_P IN	
1D	GPIO_MODE0-7	GPIO7_MODE	GPIO6_MODE	GPIO5_MODE	GPIO4_MODE	GPIO3_MODE	GPIO2_MODE	GPIO1_MODE	GPIO0_MODE
1E	GPIO_MODE8-15	GPIO15_MODE	GPIO14_MODE	GPIO13_MODE	GPIO12_MODE	GPIO11_MODE	GPIO10_MODE	GPIO9_MODE	GPIO8_MODE
1F	SWITCH_CONT	CP_EN_MODE	CORE_SW_INT	SWITCH_SR				CORE_SW_GP I	
Regulator Control Registers (REG)									
20	BCORE2_CONT	Reserved	VBCORE2_GPI		Reserved	BCORE2_CONF	BCORE2_GPI		BCORE2_EN
21	BCORE1_CONT	CORE_SW_CONF	VBCORE1_GPI		CORE_SW_EN	BCORE1_CONF	BCORE1_GPI		BCORE1_EN
22	BPRO_CONT	Reserved	VBPRO_GPI		Reserved	BPRO_CONF	BPRO_GPI		BPRO_EN
23	BMEM_CONT	Reserved	VBMEM _GPI		Reserved	BMEM_CONF	BMEM_GPI		BMEM_EN
24	BIO_CONT	Reserved	VBIO_GPI		Reserved	BIO_CONF	BIO_GPI		BIO_EN
25	BPERI_CONT	PERI_SW_CONF	BPERI_GP I		PERI_SW_EN	BPERI_CONF	PERI_SW_GPI		BPERI_EN
26	LDO1_CONT	LDO1_CONF	VLDO1_GPI		Reserved	LDO1_PD_DIS	LDO1_GPI		LDO1_EN
27	LDO2_CONT	LDO2_CONF	VLDO2_GPI		Reserved	LDO2_PD_DIS	LDO2_GPI		LDO2_EN

Hex	Register	7	6	5	4	3	2	1	0
28	LDO3_CONT	LDO3_CONF	VLDO3_GPI		Reserved	LDO3_PD_DIS	LDO3_GPI		LDO3_EN
29	LDO4_CONT	LDO4_CONF	VLDO4_GPI		Reserved	LDO4_PD_DIS	LDO4_GPI		LDO4_EN
2A	LDO5_CONT	LDO5_CONF	VLDO5_GPI		VLDO5_SEL	LDO5_PD_DIS	LDO5_GPI		LDO5_EN
2B	LDO6_CONT	LDO6_CONF	VLDO6_GPI		VLDO6_SEL	LDO6_PD_DIS	LDO6_GPI		LDO6_EN
2C	LDO7_CONT	LDO7_CONF	VLDO7_GPI		VLDO7_SEL	LDO7_PD_DIS	LDO7_GPI		LDO7_EN
2D	LDO8_CONT	LDO8_CONF	VLDO8_GPI		VLDO8_SEL	LDO8_PD_DIS	LDO8_GPI		LDO8_EN
2E	LDO9_CONT	LDO9_CONF	VLDO9_GPI		VLDO9_SEL	LDO9_PD_DIS	LDO9_GPI		LDO9_EN
2F	LDO10_CONT	LDO10_CONF	VLDO10_GPI		VLDO10_SEL	LDO10_PD_DIS	LDO10_GPI		LDO10_EN
30	LDO11_CONT	LDO11_CONF	VLDO11_GPI		VLDO11_SEL	LDO11_PD_DIS	LDO11_GPI		LDO11_EN
31	VIB	Reserved		VIB_SET					
32	DVC_1	VLDO3_SEL	VLDO2_SEL	VLDO1_SEL	VBPERI_SEL	VBMEM_SEL	VBPRO_SEL	VBCORE2_SEL	VBCORE1_SEL
33	DVC_2	VLDO4_SEL	Reserved						VBIO_SEL
GP-ADC Control Registers (GPADC)									
34	ADC_MAN	Reserved	Reserved	ADC_MODE	ADC_MAN	ADC_M UX			
35	ADC_CONT	COMP1V2_EN	AD3_ISRC_EN	AD2_ISRC_EN	AD1_ISRC_EN	AUTO_AD3_EN	AUTO_AD2_EN	AUTO_AD1_EN	AUTO_VSYS_EN
36	VSYS_MON	VSYS_MON							
37	ADC_RES_L	ADC_RES_LSB		Reserved					
38	ADC_RES_H	ADC_RES_H							
39	VSYS_RES	VSYS_RES							
3A	ADCIN1_RES	ADCIN1_RES							
3B	ADCIN2_RES	ADCIN2_RES							
3C	ADCIN3_RES	ADCIN3_RES							
3D	MON_A8_RES	MON_A8_RES							
3E	MON_A9_RES	MON_A9_RES							

Hex	Register	7	6	5	4	3	2	1	0
3F	MON_A10_RES	MON_A10_RES							
RTC Calendar and Alarm Registers (RTC)									
40	COUNT_S	RTC_READ	Reserved	COUNT_SEC					
41	COUNT_MI	Reserved		COUNT_MIN					
42	COUNT_H	Reserved			COUNT_HOUR				
43	COUNT_D	Reserved			COUNT_DAY				
44	COUNT_MO	Reserved				COUNT_MONTH			
45	COUNT_Y	Reserved	MONITOR	COUNT_YEAR					
46	ALARM_S	ALARM_TYPE		ALARM_SEC					
47	ALARM_MI	Reserved		ALARM_MIN					
48	ALARM_H	Reserved			ALARM_HOUR				
49	ALARM_D	Reserved			ALARM_DAY				
4A	ALARM_MO	Reserved		TICK_WAKE	TICK_TYPE	ALARM_MONTH			
4B	ALARM_Y	TICK_ON	ALARM_ON	ALARM_YEAR					
System Control and Event Registers (SYSMON)									
4C	SECOND_A	SECONDS_A							
4D	SECOND_B	SECONDS_B							
4E	SECOND_C	SECONDS_C							
4F	SECOND_D	SECONDS_D							

Hex	Register	7	6	5	4	3	2	1	0
PAGE 1									
80	PAGE_CON	Revert	WRITE_MODE	Reserved			REG_PAGE		
Sequencer Control Registers (SEQ)									
81	SEQ	NXT_SEQ_START				SEQ_POINTER			
82	SEQ_TIMER	SEQ_DUMM				SEQ_TIME			
83	ID_2_1	LDO2_STEP				LDO1_STEP			
84	ID_4_3	LDO4_STEP				LDO3_STEP			
85	ID_6_5	LDO6_STEP				LDO5_STEP			
86	ID_8_7	LDO8_STEP				LDO7_STEP			
87	ID_10_9	LDO10_STEP				LDO9_STEP			
88	ID_12_11	PD_DIS_STEP				LDO11_STEP			
89	ID_14_13	BUCKCORE2_STEP				BUCKCORE1_STEP			
8A	ID_16_15	BUCKIO_STEP				BUCKPRO_STEP			
8B	ID_18_17	BUCKPERI_STEP				BUCKMEM_STEP			
8C	ID_20_19	PERI_SW_STEP				CORE_SW_STEP			
8D	ID_22_21	GP_FALL1_STEP				GP_RISE1_STEP			
8E	ID_24_23	GP_FALL2_STEP				GP_RISE2_STEP			
8F	ID_26_25	GP_FALL3_STEP				GP_RISE3_STEP			
90	ID_28_27	GP_FALL4_STEP				GP_RISE4_STEP			
91	ID_30_29	GP_FALL5_STEP				GP_RISE5_STEP			
92	ID_32_31	EN32K_STEP				WAIT_STEP			
93	RESERVED	Reserved				Reserved			
94	RESERVED	Reserved				Reserved			
95	SEQ_A	POWER_END				SYSTEM_END			

Hex	Register	7	6	5	4	3	2	1	0
96	SEQ_B	PART_DOWN				MAX_COUNT			
97	WAIT	WAIT_DIR		TIME_OUT	WAIT_MODE	WAIT_TIME			
98	EN_32K	OUT_32K_EN	RTC_CLOCK	OUT_CLOCK	DELAY_MODE	CRYSTAL	STABILIZATION_TIME		
99	RESET	RESET_EVENT		RESET_TIMER					
Regulator Setting Registers (REG)									
9A	BUCK_ILIM_A	BMEM_ILIM				BIO_ILIM			
9B	BUCK_ILIM_B	BPERI_ILIM				BPRO_ILIM			
9C	BUCK_ILIM_C	BCORE2_ILIM				BCORE1_ILIM			
9D	BCORE2_CONF	BCORE2_MODE		BCORE2_PD_DIS	Reserved		BCORE2_FB		
9E	BCORE1_CONF	BCORE1_MODE		BCORE1_PD_DIS	Reserved		BCORE1_FB		
9F	BPRO_CONF	BPRO_MODE		BPRO_PD_DIS	BPRO_VTT_EN	BPRO_VTTR_EN	BPRO_FB		
A0	BIO_CONF	BIO_MODE		BIO_PD_DIS	Reserved		BIO_FB		
A1	BMEM_CONF	BMEM_MODE		BMEM_PD_DIS	Reserved		BMEM_FB		
A2	BPERI_CONF	BPERI_MODE		BPERI_PD_DIS	Reserved		BPERI_FB		
A3	VBCORE2_A	BCORE2_SL_A	VBCORE2_A						
A4	VBCORE1_A	BCORE1_SL_A	VBCORE1_A						
A5	VBPRO_A	BCPRO_SL_A	VBPRO_A						
A6	VBMEM_A	BMEM_SL_A	VBMEM_A						
A7	VBIO_A	BIO_SL_A	VBIO_A						
A8	VBPERI_A	BPERI_SL_A	VBPERI_A						
A9	VLDO1_A	LDO1_SL_A	Reserved	VLDO1_A					
AA	VLDO2_A	LDO2_SL_A	Reserved	VLDO2_A					
AB	VLDO3_A	LDO3_SL_A	VLDO3_A						

Hex	Register	7	6	5	4	3	2	1	0
AC	VLDO4_A	LDO4_SL_A	VLDO4_A						
AD	VLDO5_A	LDO5_SL_A	Reserved	VLDO5_A					
AE	VLDO6_A	LDO6_SL_A	Reserved	VLDO6_A					
AF	VLDO7_A	LDO7_SL_A	Reserved	VLDO7_A					
B0	VLDO8_A	LDO8_SL_A	Reserved	VLDO8_A					
B1	VLDO9_A	LDO9_SL_A	Reserved	VLDO9_A					
B2	VLDO10_A	LDO10_SL_A	Reserved	VLDO10_A					
B3	VLDO11_A	LDO11_SL_A	Reserved	VLDO11_A					
B4	VBCORE2_B	BCORE2_SL_B	VBCORE2_B						
B5	VBCORE1_B	BCORE1_SL_B	VBCORE1_B						
B6	VBPRO_B	BCPRO_SL_B	VBPRO_B						
B7	VBMEM_B	BMEM_SL_B	VBMEM_B						
B8	VBIO_B	BIO_SL_B	VBIO_B						
B9	VBPERI_B	BPERI_SL_B	VBPERI_B						
BA	VLDO1_B	LDO1_SL_B	Reserved	VLDO1_B					
BB	VLDO2_B	LDO2_SL_B	Reserved	VLDO2_B					
BC	VLDO3_B	LDO3_SL_B	VLDO3_B						
BD	VLDO4_B	LDO4_SL_B	VLDO4_B						
BE	VLDO5_B	LDO5_SL_B	Reserved	VLDO5_B					
BF	VLDO6_B	LDO6_SL_B	Reserved	VLDO6_B					
C0	VLDO7_B	LDO7_SL_B	Reserved	VLDO7_B					
C1	VLDO8_B	LDO8_SL_B	Reserved	VLDO8_B					
C2	VLDO9_B	LDO9_SL_B	Reserved	VLDO9_B					
C3	VLDO10_B	LDO10_SL_B	Reserved	VLDO10_B					

Hex	Register	7	6	5	4	3	2	1	0
C4	VLDO11_B	LDO11_SL_B	Reserved	VLDO11_B					
Backup Battery Charger Control Register (BBAT)									
C5	BBAT_CONT	BCHG_ISET				BCHG_VSET			
GPIO PWM (LED)									
C6	GPO11_LED	GPO11_DIM	GPO11_PWM						
C7	GPO14_LED	GPO14_DIM	GPO14_PWM						
C8	GPO15_LED	GPO15_DIM	GPO15_PWM						
GP-ADC Threshold Registers (GPADC)									
C9	ADC_CONT	ADCIN3_DEB	ADCIN2_DEB	ADCIN1_DEB	ADCIN3_CUR	ADCIN2_CUR		ADCIN1_CUR	
CA	AUTO1_HIGH	AUTO1_HIGH							
CB	AUTO1_LOW	AUTO1_LOW							
CC	AUTO2_HIGH	AUTO2_HIGH							
CD	AUTO2_LOW	AUTO2_LOW							
CE	AUTO3_HIGH	AUTO3_HIGH							
CF	AUTO3_LOW	AUTO3_LOW							

Hex	Register	7	6	5	4	3	2	1	0
PAGE 2									
100	PAGE_CON	REVERT	WRITE_MODE	Reserved			REG_PAGE		
OTP									
101	OTP_CONT	GP_WRITE_DIS	OTP_CONF_LOCK	OTP_APPS_LOCK	OTP_GP_LOCK	PC_DONE	OTP_APPS_RD	OTP_GP_RD	OTP_TIM
102	OTP_ADDR	OTP_ADDR							
103	OTP_DATA	OTP_DATA							
Customer Trim and Configuration Registers									
104	T_OFFSET	T_OFFSET							
105	INTERFACE	IF_BASE_ADDR				R/W_POL	CPHA	CPOL	nCS_POL
106	CONFIG_A	IF_TYPE	PM_IF_HSM	PM_IF_FMP	PM_IF_V	IRQ_TYPE	PM_O_TYPE	PM_O_V	PM_I_V
107	CONFIG_B	CHG_CLK_MODE	VDD_HYST_ADJ			VDD_FAULT_ADJ			
108	CONFIG_C	BPERI_CLK_INV	BIO_CLK_INV	BMEM_CLK_INV	BPRO_CLK_INV	BCORE1_CLK_INV	BUCK_ACTV_DISCHG	LDO1_TRACK	
109	CONFIG_D	GP_FB3_TYPE	GP_FB2_TYPE	FORCE_RESET	HS_IF_HSM	HS_IF_FMP	SYSTEM_EN_RD	nIRQ_MODE	GPI_V
10A	CONFIG_E	PERI_SW_AUTO	CORE_SW_AUTO	BPERI_AUTO	BIO_AUTO	BMEM_AUTO	BPRO_AUTO	BCORE2_AUTO	BCORE1_AUTO
10B	CONFIG_F	LDO11_BYP	LDO8_BYP	LDO7_BYP	LDO4_BYP	LDO3_BYP	LDO11_AUTO	LDO10_AUTO	LDO9_AUTO
10C	CONFIG_G	LDO8_AUTO	LDO7_AUTO	LDO6_AUTO	LDO5_AUTO	LDO4_AUTO	LDO3_AUTO	LDO2_AUTO	LDO1_AUTO
10D	CONFIG_H	BUCK_MERGE	BCORE1_OD	BCORE2_OD	BPRO_OD	BCORE_MERGE	MERGE_SENSE	LDO8_MODE	PWM_CLK
10E	CONFIG_I	LDO_SD	INT_SD_MODE	HOST_SD_MODE	KEY_SD_MODE	GPI14_15_SD	nONKEY_SD	nONKEY_PIN	
10F	CONFIG_J	IF_RESET	TWOWIRE_TO	RESET_DURATION		SHUT_DELAY		KEY_DELAY	
110	CONFIG_K	GPI7_PUPD	GPI6_PUPD	GPI5_PUPD	GPI4_PUPD	GPI3_PUPD	GPIO2_PUPD	GPIO1_PUPD	GPIO0_PUPD
111	CONFIG_L	GPIO15_PUPD	GPIO14_PUPD	GPIO13_PUPD	GPIO12_PUPD	GPIO11_PUPD	GPIO10_PUPD	GPIO9_PUPD	GPIO8_PUPD

Hex	Register	7	6	5	4	3	2	1	0
112	CONFIG_M	OSC_FREQ		Reserved					
113	CONFIG_N	Reserved							
114	MON_REG_1	UVOV_DELAY		MON_MODE		MON_DEB	MON_RES	MON_THRES	
115	MON_REG_2	LDO8_MON_EN	LDO7_MON_EN	LDO6_MON_EN	LDO5_MON_EN	LDO4_MON_EN	LDO3_MON_EN	LDO2_MON_EN	LDO1_MON_EN
116	MON_REG_3	Reserved					LDO11_MON_EN	LDO10_MON_EN	LDO9_MON_EN
117	MON_REG_4	Reserved		BPERI_MON_EN	BMEM_MON_EN	BIO_MON_EN	BPRO_MON_EN	BCORE2_MON_EN	BCORE1_MON_EN
118	RESERVED	Reserved							
119	RESERVED	Reserved							
11A	RESERVED	Reserved							
11B	RESERVED	Reserved							
11C	RESERVED	Reserved							
11D	RESERVED	Reserved							
11E	MON_REG_5	Reserved	MONA9_IDX			Reserved	MONA8_IDX		
11F	MON_REG_6	Reserved					MONA10_IDX		
120	TRIM_CLDR	TRIM_CLDR							
General Purpose Registers (GP)									
121	GP_ID_0	GP_0							
122	GP_ID_1	GP_1							
123	GP_ID_2	GP_2							
124	GP_ID_3	GP_3							
125	GP_ID_4	GP_4							
126	GP_ID_5	GP_5							
127	GP_ID_6	GP_6							

Hex	Register	7	6	5	4	3	2	1	0
128	GP_ID_7	GP_7							
129	GP_ID_8	GP_8							
12A	GP_ID_9	GP_9							
12B	GP_ID_10	GP_10							
12C	GP_ID_11	GP_11							
12D	RESERVED	Reserved							
12E	RESERVED	Reserved							
12F	RESERVED	Reserved							
130	RESERVED	Reserved							
131	RESERVED	Reserved							
132	RESERVED	Reserved							
133	RESERVED	Reserved							
134	RESERVED	Reserved							
Internal Debug Registers									
135	RESERVED	Reserved							
136	RESERVED	Reserved							
137	RESERVED	Reserved							
138	RESERVED	Reserved							
139	RESERVED	Reserved							
13A	RESERVED	Reserved							
13B	RESERVED	Reserved							
13C	RESERVED	Reserved							
13D	RESERVED	Reserved							
13E	RESERVED	Reserved							

<table>
<tr><th>Hex</th><th>Register</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>13F</td><td>MISC_SUPP</td><td colspan="6">Reserved</td><td>CRYSTAL_OK</td><td>OTP_CLK_ON</td></tr>
<tr><td colspan="10">PAGE 3</td></tr>
<tr><td>180</td><td>PAGE_CON</td><td>REVERT</td><td>WRITE_MODE</td><td colspan="3">Reserved</td><td colspan="3">REG_PAGE</td></tr>
<tr><td colspan="10">Chip Identification Registers</td></tr>
<tr><td>181</td><td>DEVICE_ID</td><td colspan="8">DEVICE_ID</td></tr>
<tr><td>182</td><td>VARIANT_ID</td><td colspan="4">MRC</td><td colspan="4">VRC</td></tr>
<tr><td>183</td><td>CUSTOMER_ID</td><td colspan="8">CUST_ID</td></tr>
<tr><td>184</td><td>CONFIG_ID</td><td colspan="8">CONFIG_REV</td></tr>
<tr><td>1A8</td><td>PMIC_STATUS</td><td>PC_DONE</td><td colspan="2">Reserved</td><td colspan="5">Status</td></tr>
</table>

Most register bits are reset to defaults (zero in most cases) when powering up from RESET mode. An exception is for example FAULT_LOG that is not loaded from OTP. Register fields shown in BOLD are loaded from OTP.

8 Definitions

8.1 Power Dissipation and Thermal Design

When designing with the DA9063, consideration must be given to power dissipation as the level of integration of the device can result in high power when all functions are operating with high battery voltages. Exceeding the package power dissipation capabilities results in the internal thermal sensor shutting down the device until it has sufficiently cooled.

The package includes a thermal management paddle to improve heat spreading into the PCB.

For Linear Regulators:

Linear regulators operating with a high current and high differential voltage between input and output dissipate the following power:

$$P_{diss} = (V_{in} - V_{out}) \times I_{out}$$

Example: a regulator supplying 150 mA at 2.8 V from a fully-charged lithium battery (V_{DD} = 4.1 V):

$$P_{diss} = (4.1V - 2.8\,V) \times 0.15\,A = 195\,mW$$

For Switching Regulators:

$$P_{out} = P_{in} \times Efficiency$$

Therefore,

$$P_{diss} = P_{in} - P_{out}$$

$$P_{diss} = \frac{P_{out}}{Efficiency} - P_{out}$$

$$P_{diss} = P_{out} \times \left(\frac{1}{Efficiency} - 1\right)$$

$$P_{diss} = I_{out} \times V_{out} \times \left(\frac{1}{Efficiency} - 1\right)$$

Example: an 85 % efficient buck converter supplying 1.2 V at 400 mA:

$$P_{diss} = 1.2\,V \times 0.4\,A \times \left(\frac{1}{0.85} - 1\right) = 85\,mW$$

As the DA9063 has multiple regulators, each supply must be separately considered and their powers summed to give the total device dissipation (current drawn from the reference and control circuitry can be considered negligible in these calculations).

8.2 Regulator Parameter - Dropout Voltage

In the DA9063, a regulator's dropout voltage is defined as the minimum voltage differential between the input and output voltages whilst regulation still takes place. Within the regulator, voltage control takes place across a PMOS pass transistor and, when entering the dropout condition, the transistor is fully turned on and therefore cannot provide any further voltage control. When the transistor is fully turned on, the output voltage tracks the input voltage and regulation ceases. As the DA9063 is a CMOS device and uses a PMOS pass transistor, the dropout voltage is directly related to the on-resistance of the device. In the device, the pass transistors are sized to provide the optimum balance between required performance and silicon area. By employing a 0.25 µm process, Dialog Semiconductor is able to achieve very small pass transistor sizes for superior performance.

$$V_{dropout} = V_{in} - V_{out} = R_{dson} \times I_{out}$$

When defining dropout voltage, it is specified in relation to a minimum acceptable change in output voltage. For example, all Dialog Semiconductor regulators have dropout voltage defined as the point at which the output voltage drops 10 mV below the output voltage at the minimum guaranteed operating voltage. The worst case conditions for dropout are high temperature (highest on-resistance for the internal pass device) and maximum current load.

8.3 Regulator Parameter - Power Supply Rejection

Power supply rejection (PSRR) is especially important in the supplies to the RF and audio parts of the telephone. In a TDMA system such as GSM, the 217 Hz transmit burst from the power amplifier results in significant current pulses being drawn from the battery. These can peak at up to 2 Amps before reaching a steady state of 1.4 Amps (see below). Due to the battery having a finite internal resistance (typically 0.5 Ω), these current peaks induce ripple on the battery voltage of up to 500 mV. Since the supplies to the audio and RF are derived from this supply, it is essential that this ripple is removed otherwise it would show as a 217 Hz tone in the audio and could also affect the transmit signal. Power supply rejection should always be specified under worst case conditions – when the battery is at its minimum operating voltage and when there is minimum headroom available due to dropout.

8.4 Regulator Parameter - Line Regulation

Static line regulation is a measurement that indicates a change in the regulator output voltage, ΔVreg (regulator operating with a constant load current), in response to a change in the input voltage, ΔVin. Transient line regulation is a measurement of the peak change, ΔVreg, in regulated voltage seen when the line input voltage changes.

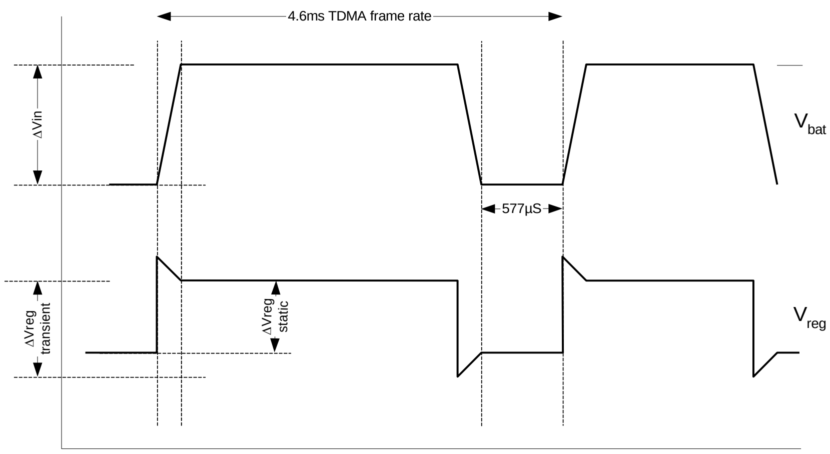


Figure 40: Line Regulation

8.5 Regulator Parameter - Load Regulation

Static load regulation is a measurement that indicates a change in the regulator output voltage, ΔVreg, in response to a change in the regulator loading, Δload, whilst the regulator input voltage remains constant. Transient load regulation is a measurement of the peak change in regulated voltage, ΔVreg, seen when the regulator load changes.

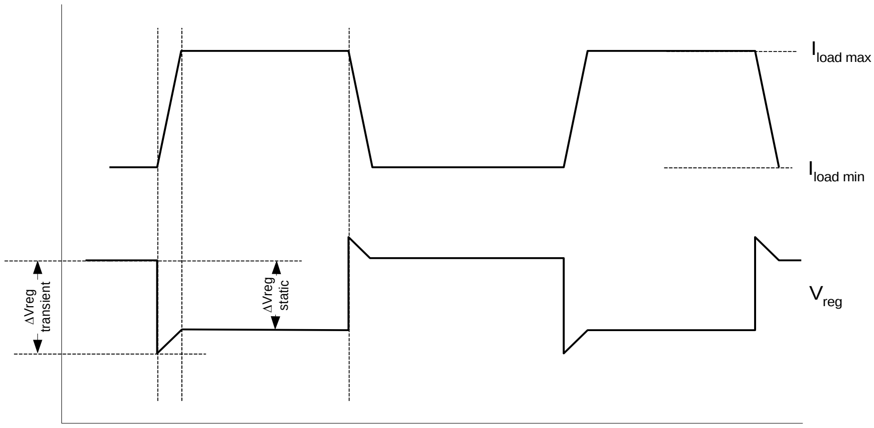


Figure 41: Load Regulation

Please contact Dialog Semiconductor for latest application information on the DA9063 and other power management devices.

9 Package Information

9.1 Package Outlines

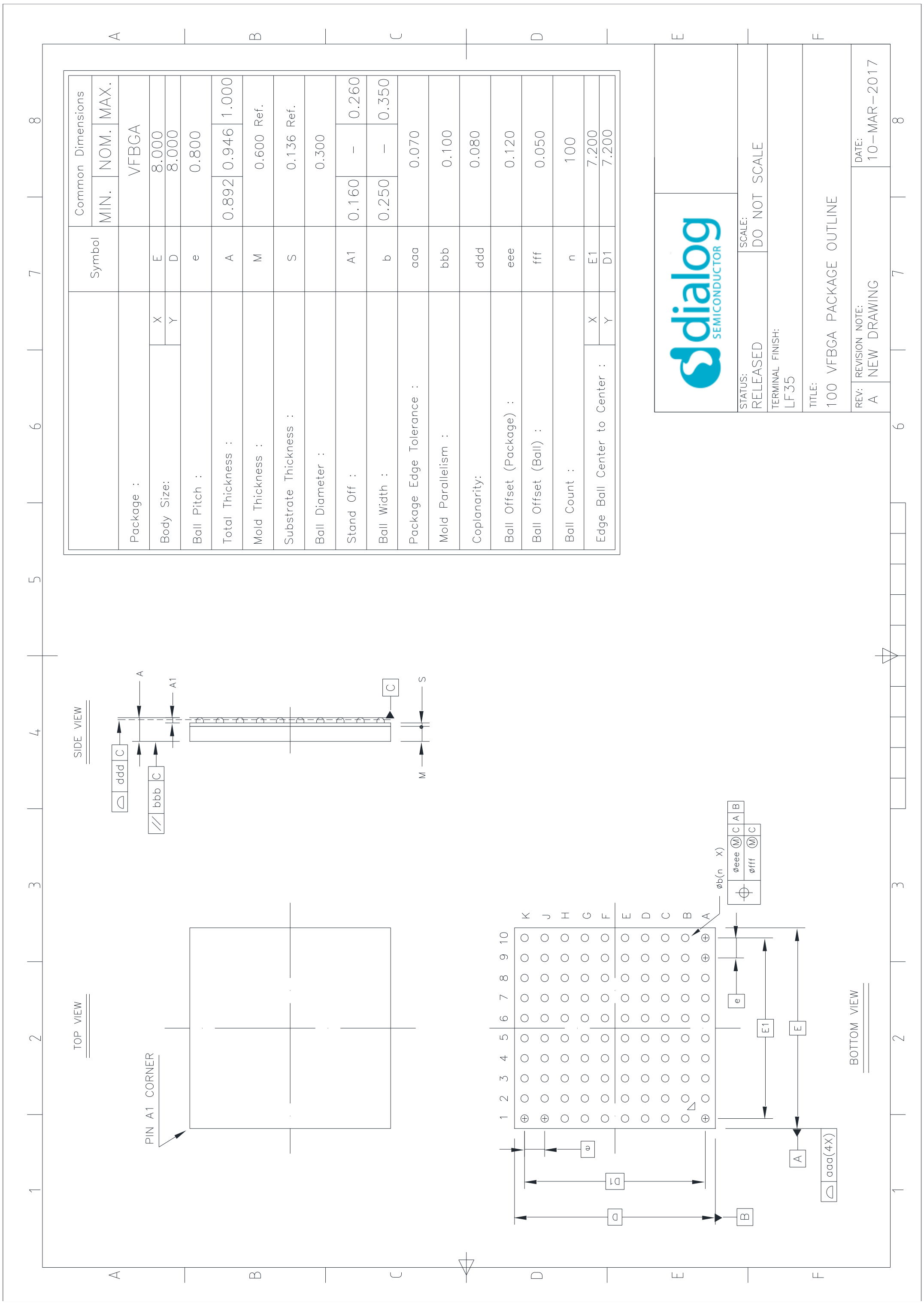
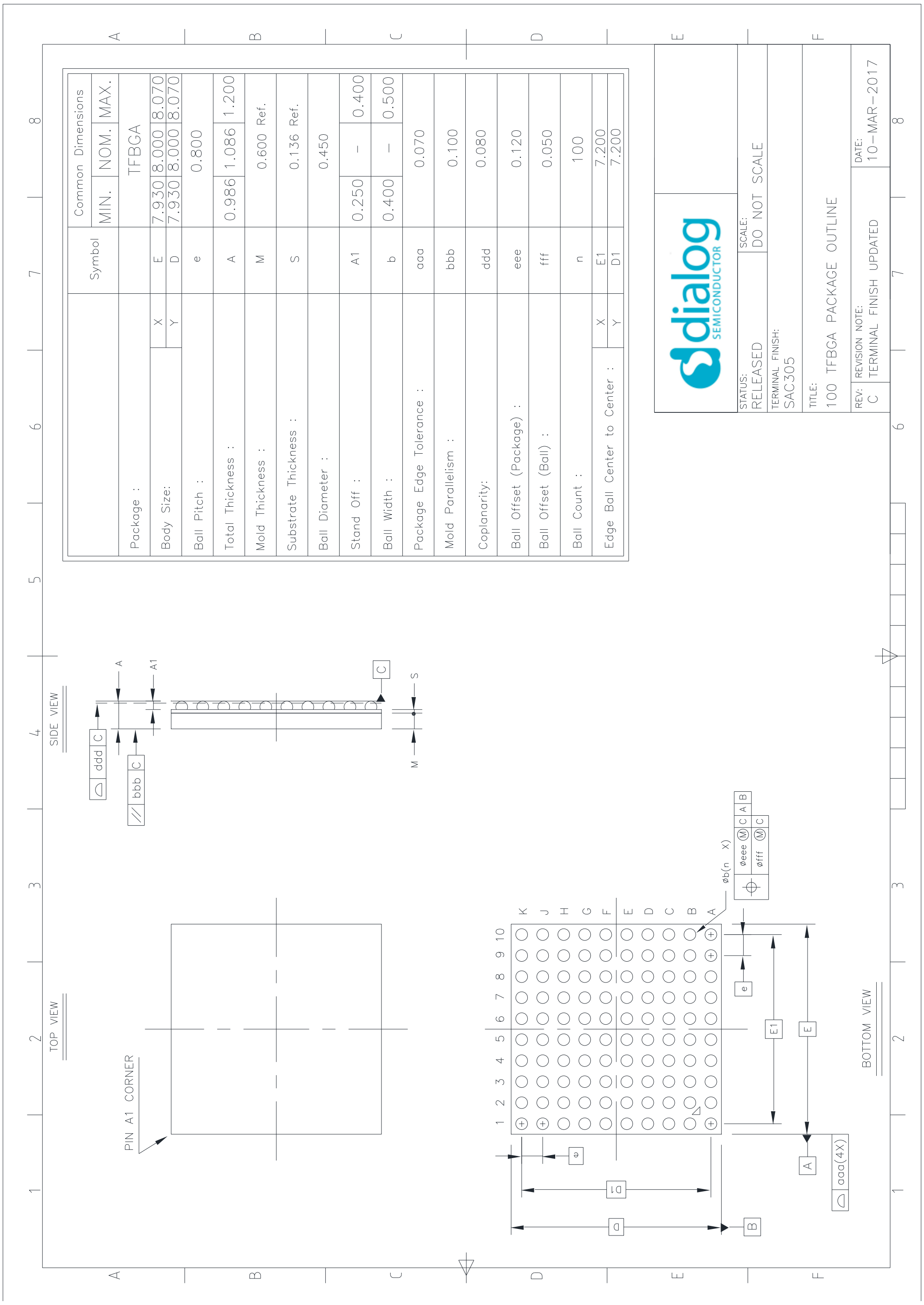


Figure 42: Package Outline Drawing 100 VFBGA 0.3 mm Ball Diameter



		Symbol	MIN.	NOM.	MAX.
			Common Dimensions		
Package :				TFBGA	
Body Size:	X	E	7.930	8.000	8.070
	Y	D	7.930	8.000	8.070
Ball Pitch :		e		0.800	
Total Thickness :		A	0.986	1.086	1.200
Mold Thickness :		M		0.600 Ref.	
Substrate Thickness :		S		0.136 Ref.	
Ball Diameter :				0.450	
Stand Off :		A1	0.250	-	0.400
Ball Width :		b	0.400	-	0.500
Package Edge Tolerance :		aaa		0.070	
Mold Parallelism :		bbb		0.100	
Coplanarity:		ddd		0.080	
Ball Offset (Package) :		eee		0.120	
Ball Offset (Ball) :		fff		0.050	
Ball Count :		n		100	
Edge Ball Center to Center :	X	E1		7.200	
	Y	D1		7.200	

Figure 43: Package Outline Drawing 100 TFBGA 0.45 mm Ball Diameter

9.2 Package Marking

Package Marking		
A1 Corner >	Marking Content	Format
1st	•	Orientation
2nd	dialog e1	Logo
3rd	D A 9 0 6 3	Part No.
4th	x x v v - A T	OTP/Silicon Version/Option
5th	y y w w z z z z	Date Code
Date Code Format: yy = Year, ww = Week, zzzz = Traceability		
xx identifies the OTP Variant, vv may be used to show the silicon version.		
-A and -AT optionally indicate the Automotive and Automotive high temp test options.		

9.3 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in Table 50.

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from http://www.jedec.org.

The VFBGA are TFBGA packages are qualified for MSL 3.

Table 50: MSL Classification

MSL Level	Floor Lifetime	Conditions
MSL 4	72 hours	30 °C / 60 % RH
MSL 3	168 hours	30 °C / 60 % RH
MSL 2A	4 weeks	30 °C / 60 % RH
MSL 2	1 year	30 °C / 60 % RH
MSL 1	Unlimited	30 °C / 85 % RH

10 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult Dialog Semiconductor's website or your local sales representative.

Table 51: Ordering Information

Part Number	Package	Shipment Form	Pack Quantity
Consumer / Industrial: 0.30 mm ball diameter, 25 °C production testing			
DA9063-xxHK1 Note 2	100 VFBGA, 8.0 mm x 8.0 mm x 1.0 mm, 0.8 mm pitch, Pb-free/green	Tray	260
DA9063-xxHK2 Note 2	100 VFBGA, 8.0 mm x 8.0 mm x 1.0 mm, 0.8 mm pitch, Pb-free/green	T&R	2500
Consumer / Industrial: 0.45 mm ball diameter, 25 °C production testing			
DA9063-xxHO1	100 TFBGA, 8.0 mm x 8.0 mm x 1.2 mm, 0.8 mm pitch, Pb-free/green	Tray	260
DA9063-xxHO2	100 TFBGA, 8.0 mm x 8.0 mm x 1.2 mm, 0.8 mm pitch, Pb-free/green	T&R	2500
Automotive AEC-Q100 Grade 2: 0.30 mm ball diameter, 25 °C production testing Note 1			
DA9063-xxHK1-A Note 2	100 VFBGA, 8.0 mm x 8.0 mm x 1.0 mm, 0.8 mm pitch, Pb-free/green	Tray	260
DA9063-xxHK2-A Note 2	100 VFBGA, 8.0 mm x 8.0 mm x 1.0 mm, 0.8 mm pitch, Pb-free/green	T&R	2500
Automotive AEC-Q100 Grade 2: 0.45 mm ball diameter, 25 °C production testing Note 1			
DA9063-xxHO1-A	100 TFBGA, 8.0 mm x 8.0 mm x 1.2 mm, 0.8 mm pitch, Pb-free/green	Tray	260
DA9063-xxHO2-A	100 TFBGA, 8.0 mm x 8.0 mm x 1.2 mm, 0.8 mm pitch, Pb-free/green	T&R	2500
Automotive AEC-Q100 Grade 2: 0.45 mm ball diameter, high temperature production testing Note 1			
DA9063-xxHO1-AT	100 TFBGA, 8.0 mm x 8.0 mm x 1.2 mm, 0.8 mm pitch, Pb-free/green	Tray	260
DA9063-xxHO2-AT	100 TFBGA, 8.0 mm x 8.0 mm x 1.2 mm, 0.8 mm pitch, Pb-free/green	T&R	2500

Note 1 Operating temperature is defined in Section 5.2. Automotive qualification temperature is defined by the Automotive Electronics Council AEC-Q100 specification.

Note 2 The 0.30 mm ball diameter version is not recommended for new designs.

10.1 Variants Ordering Information

DA9063 supports delivery of variants indicated by xx in the part number above, where xx is replaced with the actual variant number. Please contact your local Dialog Semiconductor office or representative to discuss requirements.

11 Application Information

The following recommended components are examples selected from requirements of a typical application. The electrical characteristics (for example, supported voltage/current range) have to be cross-checked and component types may need to be adapted from the individual needs of the target circuitry.

11.1 Capacitor Selection

Ceramic capacitors are used as bypass capacitors at all VDD and output rails. When selecting a capacitor, especially for types with high capacitance at smallest physical dimension, the DC bias characteristic has to be taken into account. On the VSYS main supply rail a minimum distributed capacitance of 40 µF (actual capacitance after voltage and temperature derating) is required. For example, a typical design might use:

- 22 µF within 1.5 mm of each BUCKCORE1, BUCKCORE2 and BUCKPRO supply pin.
- 10 µF within 1.5 mm of each BUCKPERI, BUCKIO and BUCKMEM supply pin or 1 x 22 µF if all are attached to a PCB power/split plane.
- 2 x 1 µF shared by all VDD_LDOx pins if they are all close together, for example, all attached to a power/split plane.
- 1 µF close to the VSYS pin.
- Buck output capacitors should be close to the buck inductors.

The amount of decoupling required will be dependent on the specific application.

Table 52: Recommended Capacitor Types

Application	Value	Tol. (%)	Size	Height (mm)	Temp. Char.	Rated Voltage (V)	Type (Murata/Samsung)
VLDO1, VLDO5	1.0 µF	± 10	0402	0.55	X5R ±15 %	10	GRM155R61A105KE15
VDDCORE, VLDO2, VLDO3, VLDO4, VLDO6, VLDO7, VLDO8. VLDO9, VLDO10, VLDO11	2.2 µF	± 20	0402	0.55	X5R ±15 %	6.3	GRM155R60J225ME95
VBUCKPER, VBUCKIO, VBUCKMEM, VSYS	22 µF	± 20	0805	0.95	X5R ±15 %	6.3	GRM219R60J226M***
		± 20	0402	0.5	X5R ±15 %	4.0	CL05A226MR5NZNC
	47 µF	± 20	0805	0.95	X5R ±15 %	4.0	GRM219R60G476M***
		± 20	0603	0.8	X5R ±15 %	4.0	CL10A476MR8NZN
VBUCKCORE 1 and 2, VBUCKPRO (using full-current mode)	22 µF	± 20	0603	1.0	X5R ±15 %	6.3	GRM188R60J226MEA0 Note 1
		± 20	0402	0.5	X5R ±15 %	4.0	CL05A226MR5NZNC
	47 µF	± 20	0805	0.95	X5R ±15 %	4.0	GRM219R60G476M***61
		± 20	0603	0.8	X5R ±15 %	4.0	CL10A476MR8NZN
VSYS	1.0 µF	± 10	0402	0.5	X5R ±15 %	10	GRM155R61A105KE15

Application	Value	Tol. (%)	Size	Height (mm)	Temp. Char.	Rated Voltage (V)	Type (Murata/Samsung)
VBBAT	470 nF	± 10	0402	0.5	X5R ±15 %	50	GRM155R61A474KE11
VREF, VLNREF	0.22 µF	± 10	0402	0.5	X7R ±15 %	16	GRM155R71C224KA12
VDDCORE	2.2 µF	± 20	0402	0.5	X5R ±15 %	6.3	GRM155R60J225ME95
XIN, XOUT	12 pF	± 5	0402	0.5	C0G	50	GRM1555C1H120JA01D
V_CP	47 nF	± 10	0402	0.5	X7R ±15 %	10	GRM155R71A473KA01

Note 1 For output voltages > 1.4 V Murata GRM219R60J226M is recommended.

Table 53: Recommended Automotive Capacitor Types

Application	Value	Tol. (%)	Size	Height (mm)	Temp. Char.	Rated Voltage (V)	Type (Murata/Samsung)
VLDO1, VLDO5	1.0 µF	± 10	0805	1.25	X7R	16	GCM21BR71C105KA58
VDDCORE, VLDO2, VLDO3, VLDO4, VLDO6, VLDO7, VLDO8. VLDO9, VLDO10, VLDO11	2.2 µF	± 20	0402	1.25	X7R	10	GCM21BR71A225MA37
VBUCKPER, VBUCKIO, VBUCKMEM, VSYS	22 µF	± 20	1206	1.6	X7R	6.3	GCM31CR70J226ME23
	47 µF	± 10	1206	1.6	X7R	6.3	GCM32ER70J476KE19
VBUCKCORE 1 and 2, VBUCKPRO (using full-current mode)	22 µF	± 20	1206	1.6	X7R	6.3	GCM31CR70J226ME23
	47 µF	± 10	1206	1.6	X7R	6.3	GCM32ER70J476KE19
VSYS	10 µF	± 10	0805	1.25	X7R	10	GCM21BR71A106ME22
	1.0 µF	± 10	0805	1.25	X7R	16	GCM21BR71C105KA58
VBBAT	470 nF	± 10	0402	0.5	X7R	10	GCM155C71A474KE36D
VREF, VLNREF	0.22 µF	± 10	0402	0.5	X7R	16	GCM155R71C224ME02
VDDCORE	2.2 µF	± 20	0402	1.25	X7R	10	GCM21BR71A225MA37
XIN, XOUT	12 pF	± 5	0402	0.5	C0G	50	GRM1555C1H120JA01D
V_CP	47 nF	± 10	0402	0.5	X7R	10	GRM155R71A473KA01

11.2 Backup Device

The backup battery charger supports Lithium coin cells as well as Supercaps/Goldcaps. The RTC will require approximately 1.5 µA between 3.1 V and 2 V for each hour that the RTC should stay alive with the main supply removed. The choice of backup device is dependent on application requirements.

Table 54: Example Backup Devices

Type	Size (mm)	Manufacturer
Lithium Battery (rechargeable) MS412FE-FL26E, 2.3 mAh, 3.0 V	4.8 (dia.) x 1.2	Seiko Instruments
Starcap SC SM 2R8, 0.1 F, 2.8 V	4.8 (dia.) x 1.4	Korchip
Lithium Battery (rechargeable) ML614, 3.4 mAh, 3.0 V	6.8 (dia.) x 1.4	Panasonic

11.3 Inductor Selection

Inductors should be selected based upon the following parameters:

- Rated maximum current: Usually a coil provides two current limits: ISAT of an Inductor specifies the current required to cause a reduction in the Inductance by a specified amount, typically 30 %, IRMS of an Inductor specifies the current required to affect a temperature rise of a maximum specified amount.
- DC resistance: Critical to converter efficiency at high current and should therefore be minimized.
- ESR at the buck switching frequency: Critical to converter efficiency in PFM mode and should therefore be minimized.
- Inductance: Given by converter electrical characteristics; 1.0 µH for all DA9063 switched-mode step-down converters.

Table 55: Recommended Inductor Types

Application	Value (µH)	Tol. (%)	ISAT (A)	IRMS (A)	DCR (Typ.) (mΩ)	Size (mm)	Type
BUCKPERI, BUCKMEM, BUCKIO, BUCKCORE1, BUCKCORE2	1.0	±30	2.7	2.3	55	2.0x1.6x1.0	Toko 1285AS-H-1R0N
		±20	2.65	2.45	60	2.0x1.6x1.0	Tayo Yuden MAKK2016T1R0M (Reference)
		±20	3.9	3.1	50	2.0x1.6x1.0	TDK TFM201610ALM-1R0MTAA
BUCKPRO, BUCKCORE1 and 2 using full-current mode or merged BUCKMEM/ BUCKIO	1.0	±30	3.4	3.0	60	2.5x2.0x1.0	Toko 1269AS-H-1R0N
		±20	3.6	3.1	45	2.5x2.0x1.2	Tayo Yuden MAMK2520T1R0M
		±20	3.8	3.5	45	2.5x2.0x1.2	Toko 1239AS-H-1R0N (Reference)
		±30	3.9	3.1	48	3.2x2.5x1.0	Toko 1276AS-H-1R0N
		±20	4.5	3.6	38	2.5x2.0x1.0	TDK TFM252010ALM-1R0MTAA

Application	Value (µH)	Tol. (%)	ISAT (A)	IRMS (A)	DCR (Typ.) (mΩ)	Size (mm)	Type
		±20	4.2	3.7	35	2.5x2.0x1.2	TDK TFM252012ALMA-1R0MTAA (AECQ200)
		±20	3.35	2.5	52	3.0x3.0x1.2	Cyntec PST031B-1R0MS
		±20	8.8	12.0	8.2	4.0x4.0x2.1	Coilcraft XGL4020-102ME (AEC-Q200)
BUCKPRO, (VTT mode)	0.24	±30	1.65	2.3	49	1.6×0.8×1.0	Taiyo Yuden MBKK1608TR24N
	0.25	±20	9.7	11.45	7.64	4.0×4.0×1.2	Coilcraft XFL4012-251ME

11.4 Resistors

Table 56: Recommended Resistor Types

Application	Value	Size	Tolerance	P_{MAX}	Type
IREF bias current reference	200 kΩ	0402	±1%	100 mW	Panasonic ERJ2RKF2003x

11.5 External Pass Transistors

Table 57: Recommended External Pass Transistor Types

Application	Package	Type
BUCK Rail Switches	WLCSP 1.6 mm x1.6 mm x 0.55 mm	Fairchild FDME410NZT

11.6 Crystal

The Real Time Clock module requires an external 32.768 kHz crystal. For correct component selection, the effective load capacitance must to be taken into account: this includes both external capacitors on pins XIN and XOUT in series combination, plus the PCB and DA9063 stray capacitances. For example, if two 12 pF external capacitors are used, giving a series combination of 6 pF, and the stray capacitances are 3 pF, then a crystal type that specifies a load capacitance of 9 pF should be chosen. Different stray capacitances may require different external capacitors and/or a different crystal type. Furthermore, the series resistance of the crystal must not exceed 100 kΩ.

Table 58: Example Crystal Type

Type	Size	Manufacturer
CC7V-T1A 32.768 kHz 9.0 pF ±30 ppm	3.2x1.5x0.9 mm	Micro Crystal

12 Layout Guidelines

12.1 General Recommendations

- Appropriate trace width and quantity of vias should be used for all power supply paths.

  Too high trace resistances can prevent the system from achieving the best performance, for example, the efficiency and the current ratings of switch-mode converters and charger might be degraded. Furthermore, the PCB may be exposed to thermal hot spots, which can lead to critical overheating due to the positive temperature coefficient of copper.

  Special care must be taken with the DA9063 pad connections. The traces of the outer row should be connected with the same width as the pads and should become wider as soon as possible. For supply pins in the second row, connection to an inner board layer is recommended (depending on the maximum current two or more vias might be required).
- A common ground plane should be used, which allows proper electrical and thermal performance. Noise sensitive references such as the VREF/VLNREF capacitors and IREF resistor should be referred to a silent ground which is connected at a star point underneath or close to the DA9063 main ground connection.
- Generally, all power tracks with discontinuous/high currents should be kept as short as possible.
- Noise sensitive analog signals such as feedback lines or crystal connections should be kept away from traces carrying pulsed analog or digital signals. This can be achieved by separation (distance) or shielding with quiet signals or ground traces.

12.2 LDOs and Switched Mode Supplies

- The placement of the distributed capacitors on the V_{SYS} rail must ensure that all VDD inputs – and especially to the VSYS pin, the buck converters and LDOs – are connected to a bypass capacitor close to the pads. It is recommended placing at least two 1 µF capacitors close to the LDO supply pads and at least one 10 µF close to the buck VDD rail.

  Using a local power plane underneath the chip for V_{SYS} might be considered.
- Transient current loops in the area of the switched mode converters should be minimized.
- The common references (IREF resistor, VREF/VLNREF capacitors) should be placed close to the DA9063 and cross coupling to any noisy digital or analog trace must be avoided.
- Output capacitors of the LDOs can be placed close to the input pins of the supplied devices (remote from the DA9063).
- Care must be taken with trace routing to ensure that no current is carried on feedback lines of the buck output voltages V_{BUCK}.
- The inductor placement is less critical since parasitic inductances have negligible effect.

12.3 Crystal Oscillator

- The crystal and its load capacitors should be placed as close as possible to the IC with short and symmetric traces.
- The traces must be isolated from noisy signals, especially from clocked digital ones. Ideally the lines should be buried between two ground layers, surrounded by additional ground traces.

12.4 Thermal Connection, Land Pad, and Stencil Design

- The DA9063 provides a central ground area of balls, which are soldered to the PCB's central ground pad. This PCB ground pad must be connected with as many vias and as direct as possible to the PCB's main ground plane in order to achieve good thermal performance.
- Solder mask openings for the ball landing pads must be arranged to prohibit solder balls flowing into vias.

For further PCB layout guidance, see PCB Layout Guidelines [3].

Appendix A Register Descriptions

This appendix describes the registers summarized in Section 7.

A.1 Register Page Control

Table 59: PAGE_CON

Register Address	Bit	Type	Label	Description
0x00 PAGE_CON	7	RW	REVERT	Resets REG_PAGE to 00 after read/write access has finished
	6	RW	WRITE_MODE	2-WIRE multiple write mode 0: Page Write Mode 1: Repeated Write Mode
	5:3	RW	Reserved	
	2:0	RW	REG_PAGE	000: Selects Register 0x01 to 0x3F 001: Selects Register 0x81 to 0xCF 010: Selects Register 0x101 to 0x13F 011: Reserved for production and test

The PAGE_CON register is located at address 0x00 of each register page (0x00 and 0x80). Each of the control interfaces (4-WIRE and the two 2-WIRE) provides an individual instance of the PAGE_CON register.

A.2 Register Page 0

A.2.1 Power Manager Control and Monitoring

The STATUS register reports the current value of the various signals at the time that it is read out. All the status bits have the same polarity as their corresponding signals.

Table 60: STATUS_A

Register Address	Bit	Type	Label	Description
0x01 STATUS_A	7:4	R	Reserved	
	3	R	COMP1V2	Output state of 1.2 V comparator
	2	R	DVC	Asserted as long as at least one DVC supply performs voltage ramping
	1	R	WAKE	CHG_WAKE level
	0	R	nONKEY	Asserted as long nONKEY is pressed (low level)

Table 61: STATUS_B

Register Address	Bit	Type	Label	Description
0x02 STATUS_B	7	R	GPI7	GPI7 level
	6	R	GPI6	GPI6 level
	5	R	GPI5	GPI5 level
	4	R	GPI4	GPI4 level
	3	R	GPI3	GPI3 level
	2	R	GPI2	GPI2 level or ADCIN3 threshold indicator (1 when overriding high limit)

Register Address	Bit	Type	Label	Description
	1	R	GPI1	GPI1 level or ADCIN2 threshold indicator (1 when overriding high limit)
	0	R	GPI0	GPI0 level or ADCIN1 threshold indicator (1 when overriding high limit)

Table 62: STATUS_C

Register Address	Bit	Type	Label	Description
0x03 STATUS_C	7	R	GPI15	GPI15 level
	6	R	GPI14	GPI14 level
	5	R	GPI13	GPI13/ EXT_WAKEUP/READY level
	4	R	GPI12	GPI12/nVDD_FAULT/VDD_MON level
	3	R	GPI11	GPI11 level
	2	R	GPI10	GPI10/PWR1_EN level
	1	R	GPI9	GPI9/PWR_EN level
	0	R	GPI8	GPI8/SYS_EN level

Table 63: STATUS_D

Register Address	Bit	Type	Label	Description
0x04 STATUS_D	7	R/W	LDO11_LIM	Asserted as long LDO11 hits its over-current limit
	6	R/W	LDO8_LIM	Asserted as long LDO8 hits its over-current limit
	5	R/W	LDO7_LIM	Asserted as long LDO7 hits its over-current limit
	4	R/W	LDO4_LIM	Asserted as long LDO4 hits its over-current limit
	3	R/W	LDO3_LIM	Asserted as long LDO3 hits its over-current limit
	2:0	R/W	Reserved	

Table 64: FAULT_LOG

Register Address	Bit	Type Note 1	Label	Description
0x05 FAULT_LOG	7	R	WAIT_SHUT	Power down by time out of ID WAIT
	6	R	nSHUT_DOWN	Power down by assertion of port nOFF, nSHUTDOWN
	5	R	KEY_RESET	Power down from a long press of nONKEY or GPIO14/15
	4	R	TEMP_CRIT	Junction over-temperature detected
	3	R	VDD_START	Power down by V_{SYS} under-voltage detect before or within 16 seconds after entering ACTIVE mode
	2	R	VDD_FAULT	Power down by V_{SYS} under-voltage detect
	1	R	POR	DA9063 starts up from NO-POWER or RTC/DELIVERY mode

Register Address	Bit	Type Note 1	Label	Description
	0	R	TWD_ERROR	Watchdog time violated

Note 1 Cleared from the host by writing back the read value.

The EVENT registers hold information about events that have occurred in the DA9063. Events are triggered by a change in the status registers that contains the status of monitored signals. When an EVENT bit is set in the event register the nIRQ signal is asserted (unless the nIRQ is to be masked by a bit in the IRQ mask register). The nIRQ is also masked during the power-up sequence and is not released until the event registers have been cleared. The IRQ triggering event register is cleared from the host by writing back its read value. The event registers may be read in page/repeated mode. New events that occur during clearing are delayed before they are passed to the event register, ensuring that the host controller does not miss them.

Table 65: EVENT_A

Register Address	Bit	Type	Label	Description
0x06 EVENT_A	7	R	EVENTS_D	Asserted when register EVENT_B to EVENT_D have at least one event bit asserted
	6	R	EVENTS_C	Asserted when register EVENT_B to EVENT_C have at least one event bit asserted
	5	R	EVENTS_B	Asserted when register EVENT_B has at least one event bit asserted
	4	R Note 1	E_SEQ_RDY	Sequencer reached final position caused event
	3	R Note 1	E_ADC_RDY	ADC manual conversion result ready caused event
	2	R Note 1	E_TICK	RTC tick caused event
	1	R Note 1	E_ALARM	RTC alarm caused event
	0	R Note 1	E_nONKEY	nONKEY caused event

Note 1 Cleared from the host by writing back the read value.

Table 66: EVENT_B

Register Address	Bit	Type Note 1	Label	Description
0x07 EVENT_B	7	R	E_VDD_WARN	V_{SYS} dropped below VDD_FAULT_UPPER threshold
	6	R	E_VDD_MON	V_{SYS} less or higher than VSYS_MON threshold caused event
	5	R	E_DVC_RDY	Finish of all DVC voltage ramping event
	4	R	E_REG_UVOV	Event triggered from a monitored regulator voltage being out of selected range or from new regulator voltage measurement being available (depends on settings of MON_MODE)
	3	R	E_LDO_LIM	LDO3, 4, 7, 8 or 11 current limit exceeded for more than 10 ms
	2	R	E_COMP1V2	1.2 V comparator caused event

Register Address	Bit	Type Note 1	Label	Description
	1	R	E_TEMP	Junction high temp caused event
	0	R	E_WAKE	Detected rising edge on CHG_WAKE

Note 1 Cleared from the host by writing back the read value.

Table 67: EVENT_C

Register Adress	Bit	Type Note 1	Label	Description
0x08 EVENT_C	7	R	E_GPI7	GPI event according to active state setting
	6	R	E_GPI6	GPI event according to active state setting
	5	R	E_GPI5	GPI event according to active state setting
	4	R	E_GPI4	GPI event according to active state setting
	3	R	E_GPI3	GPI event according to active state setting
	2	R	E_GPI2	GPI event according to active state setting / ADCIN3 high / low threshold exceeded caused event
	1	R	E_GPI1	GPI event according to active state setting / ADCIN2 high / low threshold exceeded caused event
	0	R	E_GPI0	GPI event according to active state setting / ADCIN1 high / low threshold exceeded caused event

Note 1 Cleared from the host by writing back the read value.

Table 68: EVENT_D

Register Address	Bit	Type Note 1	Label	Description
0x09 EVENT_D	7	R	E_GPI15	GPI event according to active state setting
	6	R	E_GPI14	GPI event according to active state setting/Event caused from host addressing HS-2-WIRE interface
	5	R	E_GPI13	GPI event according to active state setting
	4	R	E_GPI12	GPI event according to active state setting
	3	R	E_GPI11	GPI event according to active state setting
	2	R	E_GPI10	GPI/PWR1_EN event according to active state setting
	1	R	E_GPI9	GPI/PWR_EN event according to active state setting
	0	R	E_GPI8	GPI/SYS_EN event according to active state setting

Note 1 Cleared from the host by writing back the read value.

The nIRQ line is released only when all events have been cleared from the host processor by writing the read value into all registers with an asserted event bit.

Table 69: IRQ_MASK_A

Register Address	Bit	Type	Label	Description
0x0A IRQ_MASK_A	7:5	R/W	**Reserved**	
	4	R/W	**M_SEQ_RDY**	Mask nIRQ from finishing power sequencing
	3	R/W	**M_ADC_RDY**	Mask ADC manual conversion result ready caused nIRQ
	2	R/W	**M_TICK**	Mask RTC tick caused nIRQ
	1	R/W	**M_ALARM**	Mask RTC alarm caused nIRQ
	0	R/W	**M_nONKEY**	Mask nONKEY caused nIRQ

Table 70: IRQ_MASK_B

Register Address	Bit	Type	Label	Description
0x0B IRQ_MASK_B	7	R/W	**M_VDD_WARN**	Mask VDDFAULT _UPPER comparator triggered event
	6	R/W	**M_VDD_MON**	Mask V_{SYS} caused nIRQ
	5	R/W	**M_DVC_RDY**	Mask DVC voltage ramping triggered event
	4	R/W	**M_REG_UVOV**	Mask events generated from regulator output voltage monitoring
	3	R/W	**M_LDO_LIM**	Mask LDO current limit exceeded caused nIRQ
	2	R/W	**M_COMP1V2**	Mask 1.2 V comparator caused nIRQ
	1	R/W	**M_TEMP**	Mask junction over temp caused nIRQ
	0	R/W	**M_WAKE**	Mask companion charger caused event

Table 71: IRQ_MASK_C

Register Address	Bit	Type	Label	Description
0x0C IRQ_MASK_C	7	R/W	**M_GPI7**	Mask GPI caused nIRQ
	6	R/W	**M_GPI6**	Mask GPI caused nIRQ
	5	R/W	**M_GPI5**	Mask GPI caused nIRQ
	4	R/W	**M_GPI4**	Mask GPI caused nIRQ
	3	R/W	**M_GPI3**	Mask GPI caused nIRQ
	2	R/W	**M_GPI2**	Mask GPI caused / ADCIN3 high / low threshold exceeded caused nIRQ
	1	R/W	**M_GPI1**	Mask GPI caused / ADCIN2 high / low threshold exceeded caused nIRQ
	0	R/W	**M_GPI0**	Mask GPI caused / ADCIN1 high / low threshold exceeded caused nIRQ

Table 72: IRQ_MASK_D

Register Address	Bit	Type	Label	Description
0x0D IRQ_MASK_D	7	R/W	**M_GPI15**	Mask GPI caused nIRQ
	6	R/W	**M_GPI14**	Mask GPI/HS-2-WIRE caused nIRQ

Register Address	Bit	Type	Label	Description
	5	R/W	**M_GPI13**	Mask GPI caused nIRQ
	4	R/W	**M_GPI12**	Mask GPI caused nIRQ
	3	R/W	**M_GPI11**	Mask GPI caused nIRQ
	2	R/W	**M_GPI10**	Mask GPI/PWR1_EN caused nIRQ
	1	R/W	**M_GPI9**	Mask GPI/PWR_EN caused nIRQ
	0	R/W	**M_GPI8**	Mask GPI/SYS_EN caused nIRQ

Table 73: CONTROL_A

Register Address	Bit	Type	Label	Description
0xE CONTROL_A	7	R/W	**CP_EN**	When asserted charge pump for rail switches is enabled
	6	R/W	M_POWER1_EN	Mask the update of POWER1_EN when writing to CONTROL_A
	5	R/W	M_POWER_EN	Mask the update of POWER_EN when writing to CONTROL_A
	4	R/W	M_SYSTEM_EN	Mask the update of SYSTEM_EN when writing to CONTROL_A
	3	R/W	**STANDBY**	Clearing SYSTEM_EN/releasing port SYS_EN press will 0: completely power down to Slot 0 (Hibernate) 1: stop powering down at pointer PART_DOWN (Standby)
	2	R/W	**POWER1_EN**	Target status of power domain POWER1: controlled from OTP/PM interface and port PWR1_EN
	1	R/W	**POWER_EN**	Target status of power domain POWER: controlled from OTP/PM interface and port PWR_EN
	0	R/W	**SYSTEM_EN**	Target status of power domain SYSTEM: controlled from OTP/PM interface and port SYS_EN

Table 74: CONTROL_B

Register Address	Bit	Type	Label	Description
0xF CONTROL_B	7	R/W	**BUCK_SLOWSTART**	**Enables soft-start for buck converters (recommended for application instant-on with discharged battery and weak external supply)** Note 1
	6:5	R/W	**Reserved**	
	4	R/W	**nONKEY_LOCK**	0: Half-current POWERDOWN mode **1: Wake-up from POWERDOWN mode requires the nONKEY signal being low for longer than selected in KEY_DELAY** (automatically cleared during power-up sequence)

Register Address	Bit	Type	Label	Description
	3	R/W	**nRES_MODE**	0: No assertion of nRESET for power down sequence **1: Assert nRESET before starting power down sequence (release after leaving POWERDOWN mode in case RESET_EVENT < '11')**
	2	R/W	**RES_BLINKING**	Enables (time limited) VDD_START triggered GPO11/4/15 flashing in case of no connected external supply
	1	R/W	**WATCHDOG_PD**	**0: Discontinue Watchdog timer during POWERDOWN mode** 1: Watchdog timer continues during POWERDOWN mode
	0	R/W	**CHG_SEL**	**Port CHG_WAKE is connected to** 0: Dialog charger WAKE port **1: Charger SAFE_OUT**

Note 1 Increases buck start-up time up to 3 ms.

Table 75: CONTROL_C

Register Address	Bit	Type	Label	Description
0x10 CONTROL_C	7	R/W	**DEF_SUPPLY**	When asserted all supplies (except LDOCORE) are enabled/disabled from OTP default mode when entering sequencer Slot 0.
	6:5	R/W	**SLEW_RATE**	DVC slewing (bucks and LDOs) is executed at 00: 10 mV every 4.0 µs 01: 10 mV every 2.0 µs **10: 10 mV every 1.0 µs** 11: 10 mV every 0.5 µs
	4	R/W	**OTPREAD_EN**	0: OTP read after POWERDOWN mode disabled **1: Power supplies are configured with OTP values when leaving POWERDOWN mode**
	3	R/W	**AUTO_BOOT**	**0: Start-up of power sequencer after progressing from RESET mode requires a valid wake-up event** 1: PMIC automatically starts power sequencer after progressing from RESET mode
	2:0	R/W	**DEBOUNCING**	GPI, nONKEY and nSHUTDOWN debounce time 000: no debounce time 001: 0.1 ms 010: 1.0 ms **011: 10.2 ms** 100: 51.2 ms 101: 256 ms 110: 512 ms 111: 1024 ms

Table 76: CONTROL_D

Register Address	Bit	Type	Label	Description
0x11 CONTROL_D	7:6	R/W	**BLINK_DUR**	GPO10/GPO11 flashing on-time 00: 10 ms **01: 20 ms** 10: 40 ms 11: 20 ms double stroke (180 ms period)
	5:3	R/W	**BLINK_FRQ**	GPO11/4/15 flashing frequency 000: no blinking (GPO11/14/15 state selected via GPIOxx_MODE) 001: every second 010: every two seconds 011: every four seconds 100: every 180 ms (flicker mode) **101: every two seconds enabled by VDD_START** 110: every four seconds enabled by VDD_START 111: every 180 ms enabled by VDD_START Note 1
	2:0	R/W	**TWDSCALE**	**000: Watchdog disabled** 001: 1x scaling applied to t_{WD_MAX} period 010: 2x 011: 4x 100: 8x 101: 16x 110: 32x 111: 64x

Note 1 Blinking from OTP settings 001 to 100 continues as long as an active charger is connected to port CHG_WAKE. In the absence of a battery charger a time limited blinking can be enabled via RES_BLINKING.

Table 77: CONTROL_E

Register Address	Bit	Type	Label	Description
0x12 CONTROL_E	7	R/W	**V_LOCK**	**0: Allows host writes into registers 0x81 to 0x120** 1: Disables register 0x81 to 0x120 re-programming from host interfaces
	6	R/W	**PM_FB3_PIN**	**0: 2nd 32 kHz signal output** 1: Feedback pin is used as an input signal to stop and start the vibration motor (active low nVIB_BRAKE)
	5	R/W	**PM_FB2_PIN**	**0: Feedback pin indicates the status of regulators being selected for voltage supervision (PWR_OK)** 1: Feedback pin is used as KEEP_ACT signal for the Watchdog unit
	4	R/W	**PM_FB1_PIN**	**0: Feedback pin indicates the detection of a wake-up event (EXT_WAKEUP)** 1: Feedback pin is used as an indicator, signaling via low level ongoing power mode transitions (power sequencer and DVC) (READY)
	3	R/W	**ECO_MODE**	When asserted DA9063 is armed for the pulsed mode when entering RESET

Register Address	Bit	Type	Label	Description
	2	R/W	**RTC_EN**	Enables the power supply of the 32 kHz oscillator and RTC (for DA9063 the DELIVERY mode if cleared under certain pre-conditions, locked from the assertion of control MONITOR
	1	R/W	**RTC_MODE_SD**	When asserted all supplies (including LDOCORE) and functional blocks except of the RTC are disabled when reaching RESET mode with a VDDFAULT condition
	0	R/W	**RTC_MODE_PD**	When asserted all supplies (including LDOCORE) and functional blocks except of the RTC are disabled when reaching POWERDOWN mode

Table 78: CONTROL_F

Register Address	Bit	Type	Label	Description
0x13 CONTROL_F	7:3	R/W	Reserved	
	2	R/W	WAKE_UP	If set to 1 PMU wakes up from POWERDOWN mode. The bit is cleared back to 0 automatically 16 sec after entering ACTIVE mode
	1	R/W	SHUTDOWN	If set to 1 the sequencer powers down to RESET mode. The bit is cleared back to 0 automatically when entering the RESET mode
	0	R/W	WATCHDOG	If set to 1 watchdog timer is reset. The bit is cleared back to 0 automatically.

Table 79: PD_DIS

Register Address	Bit	Type	Label	Description
0x14 PD_DIS	7	R/W	**PMCONT_DIS**	**0: SYS_EN, PWR_EN, PWR1_EN enabled during power down** 1: Auto-Disable of SYS_EN, PWR_EN and PWR1_EN during POWERDOWN mode and force the detection hidden transition when re-enabling the control from ports
	6	R/W	**OUT_32K_PAUSE**	**0: Enables OUT_32K during power down** 1: Auto-Disable OUT_32K output buffer during POWERDOWN mode
	5	R/W	**BBAT_DIS**	**0: Enables Backup battery charger during POWERDOWN mode** 1: Auto-disable backup battery charger during power down
	4	R/W	**CLDR_PAUSE**	0: Calendar/Clock readout registers are updated during POWERDOWN mode **1: Update of Calendar/Clock readout registers is paused during POWERDOWN mode**
	3	R/W	**HS2WIRE_DIS**	**0: HS-2-WIRE not disabled during power down** 1: Auto-disable of HS-2-WIRE interface during POWERDOWN mode

Register Address	Bit	Type	Label	Description
	2	R/W	**PMIF_DIS**	**0: Power manager interface not disabled during power down** 1: Auto-disable of power manager interface during POWERDOWN mode
	1	R/W	**GPADC_PAUSE**	0: ADC measurements continue during power down as configured **1: Auto-PAUSE auto measurements on A0, A1, A2 and A3 and manual measurement during POWERDOWN mode; if no autonomous auto-measurements are required (V_{SYS} from vibration motor driver) switch off the ADC completely**
	0	R/W	**GPI_DIS**	**0: GPIO extender enabled during power down** 1: Auto-disable of features configured as GPI pins during POWERDOWN mode and force the detection hidden transition when re-enabling the pin

Note 1 When the related ID is configured to be 1 < PD_DIS_STEP ≤ MAX_COUNT the value of the above controls define whether functions are switched on when entering POWERDOWN mode from POR or wait until ID PD_DIS_STEP is processed.

A.2.2 GPIO Control

Table 80: GPIO_0_1

Register Address	Bit	Type	Label	Description
0x15 GPIO_0_1	7	R/W	**GPIO1_WEN**	**0: Passive to active transition triggers a wake-up** 1: Wake-up suppressed
	6	R/W	**GPIO1_TYPE**	**0: GPI: active low** GPO: supplied from VDD_IO1 1: GPI: active high GPO: supplied from VDD_IO2
	5:4	R/W	**GPIO1_PIN**	PIN assigned to **00: ADCIN2/1.2 V comparator** 01: GPI (optional regulator HW control) 10: GPO mode controlled (Open drain) 11: GPO mode controlled (Push-pull)
	3	R/W	**GPIO0_WEN**	0: Passive to active transition triggers a wake-up 1: Wake-up suppressed
	2	R/W	**GPIO0_TYPE**	0: GPI: active low GPO: supplied from VDD_IO1 1: GPI: active high GPO: supplied from VDD_IO2
	1:0	R/W	**GPIO0_PIN**	PIN assigned to **00: ADCIN1** 01: GPI 10: GPO mode controlled (Open drain) 11: GPO mode controlled (Push-pull)

Table 81: GPIO_2_3

Register Address	Bit	Type	Label	Description
0x16 GPIO_2_3	7	R/W	**GPIO3_WEN**	0: Passive to active transition triggers a wake-up 1: Wake-up suppressed
	6	R/W	**GPIO3_TYPE**	0: GPI: active low GPO: supplied from VDD_IO1 1: GPI: active high GPO: supplied from VDD_IO2
	5:4	R/W	**GPIO3_PIN**	PIN assigned to **00: CORE_SWG** 01: GPI 10: GPO mode controlled (Open drain) 11: GPO mode controlled (Push-pull)
	3	R/W	**GPIO2_WEN**	0: Passive to active transition triggers a wake-up 1: Wake-up suppressed
	2	R/W	**GPIO2_TYPE**	0: GPI: active low GPO: supplied from VDD_IO1 **1: GPI: active high** GPO: supplied from VDD_IO2
	1:0	R/W	**GPIO2_PIN**	PIN assigned to 00: ADCIN3 **01: GPI (optional regulator HW control)** 10: GPO Sequencer controlled (Push-pull) 11: GPO mode controlled (Push-pull)

Table 82: GPIO_4_5

Register Address	Bit	Type	Label	Description
0x17 GPIO_4_5	7	R/W	**GPIO5_WEN**	0: Passive to active transition triggers a wake-up 1: Wake-up suppressed
	6	R/W	**GPIO5_TYPE**	0: GPI: active low GPO: supplied from VDD_IO1 1: GPI: active high GPO: supplied from VDD_IO2
	5:4	R/W	**GPIO5_PIN**	PIN assigned to **00: PERI_SWG** 01: GPI 10: GPO mode controlled (Open drain) 11: GPO mode controlled (Push-pull)
	3	R/W	**GPIO4_WEN**	0: Passive to active transition triggers a wake-up 1: Wake-up suppressed
	2	R/W	**GPIO4_TYPE**	0: GPI: active low GPO: supplied from VDD_IO1 1: GPI: active high GPO: supplied from VDD_IO2

Register Address	Bit	Type	Label	Description
	1:0	R/W	**GPIO4_PIN**	PIN assigned to **00: CORE_SWS** 01: GPI 10: GPO mode controlled (Open drain) 11: GPO mode controlled (Push-pull)

Table 83: GPIO_6_7

Register Address	Bit	Type	Label	Description
0x18 GPIO_6_7	7	R/W	**GPIO7_WEN**	0: Passive to active transition triggers a wake-up 1: Wake-up suppressed
	6	R/W	**GPIO7_TYPE**	0: GPI: active low **GPO: supplied from VDD_IO1** 1: GPI: active high GPO: supplied from VDD_IO2
	5:4	R/W	**GPIO7_PIN**	PIN assigned to 00: Reserved 01: GPI **10: GPO Sequencer controlled (Push-pull)** 11: GPO mode controlled (Push-pull)
	3	R/W	**GPIO6_WEN**	0: Passive to active transition triggers a wake-up 1: Wake-up suppressed
	2	R/W	**GPIO6_TYPE**	0: GPI: active low GPO: supplied from VDD_IO1 1: GPI: active high GPO: supplied from VDD_IO2
	1:0	R/W	**GPIO6_PIN**	PIN assigned to **00: PERI_SWS** 01: GPI 10: GPO mode controlled (Open drain) 11: GPO mode controlled (Push-pull)

Table 84: GPIO_8_9

Register Address	Bit	Type	Label	Description
0x19 GPIO_8_9	7	R/W	**GPIO9_WEN**	**0: Passive to active transition triggers a wake-up** 1: Wake-up suppressed
	6	R/W	**GPIO9_TYPE**	**0: GPI/PWR_EN: active low** GPO: supplied from VDD_IO1 1: GPI/PWR_EN: active high GPO: supplied from VDD_IO2
	5:4	R/W	**GPIO9_PIN**	PIN and status register bit assigned to 00: GPI with PWR_EN **01: GPI** 10: GPO Sequencer controlled (Push-pull) 11: GPO mode controlled (Push-pull)
	3	R/W	**GPIO8_WEN**	**0: Passive to active transition triggers a wake-up** 1: Wake-up suppressed

Register Address	Bit	Type	Label	Description
	2	R/W	**GPIO8_TYPE**	**0: GPI/SYS_EN: active low** GPO: supplied from external/VDD_IO1 1: GPI/SYS_EN: active high GPO: supplied from VDD_IO2
	1:0	R/W	**GPIO8_PIN**	PIN and status register bit assigned to 00: GPI with SYS_EN **01: GPI** 10: GPO Sequencer controlled (Push-pull) 11: GPO mode controlled (Push-pull)

Table 85: GPIO_10_11

Register Address	Bit	Type	Label	Description
0x1A GPIO_10_11	7	R/W	GPIO11_WEN	0: Passive to active transition triggers a wake-up 1: Wake-up suppressed
	6	R/W	GPIO11_TYPE	**0:** GPI: active low **GPO: supplied from external/VDD_IO1** 1: GPI: active high GPO: supplied from VDD_IO2
	5:4	R/W	GPIO11_PIN	PIN assigned to 00: GPO (Open drain, with optional blinking) 01: GPI **10: GPO GPO Sequencer controlled (Push-pull)** 11: GPO mode controlled (Push-pull)
	3	R/W	GPIO10_WEN	**0: Passive to active transition triggers a wake-up** 1: Wake-up suppressed
	2	R/W	GPIO10_TYPE	**0: GPI/PWR1_EN: active low** GPO: supplied from external/VDD_IO1 1: GPI/PWR1_EN: active high GPO: supplied from VDD_IO2
	1:0	R/W	GPIO10_PIN	PIN and status register bit assigned to 00: GPI with PWR1_EN **01: GPI** 10: GPO (Open drain) 11: GPO mode controlled (Push-pull)

Table 86: GPIO_12_13

Register Address	Bit	Type	Label	Description
0x1B GPIO_12_13	7	R/W	**GPIO13_WEN**	0: Passive to active transition triggers a wake-up 1: Wake-up suppressed
	6	R/W	**GPIO13_TYPE**	**0:** GPI: active low **GPO/GP_FB1: supplied from external/VDD_IO1** 1: GPI: active high GPO/GP_FB1: supplied from VDD_IO2

Register Address	Bit	Type	Label	Description
	5:4	R/W	**GPIO13_PIN**	PIN and status register bit assigned to 00: GPO controlled by state of GP_FB1 (EXT_WAKEUP/READY) (Push-pull) 01: GPI (optional regulator HW control) 10: GPO controlled by state of GP_FB1 (EXT_WAKEUP/READY) (Open drain) **11: GPO mode controlled (Push-pull)**
	3	R/W	**GPIO12_WEN**	0: Passive to active transition triggers a wake-up 1: Wake-up suppressed
	2	R/W	**GPIO12_TYPE**	**0:** GPI: active low **GPO/ nVDD_FAULT/V_{SYS} monitor: supplied from VDD_IO1** 1: GPI: active high GPO/DD_FAULT/V_{SYS} monitor: supplied from VDD_IO2
	1:0	R/W	**GPIO12_PIN**	PIN assigned to **00: nVDD_FAULT (Push-pull)** 01: GPI 10: GPO controlled by the state of V_{SYS} monitor (Push-pull) 11: GPO mode controlled (Push-pull)

Table 87: GPIO_14_15

Register Address	Bit	Type	Label	Description
0x1C GPIO_14_15	7	R/W	**GPIO15_WEN**	**0: Passive to active transition triggers a wake-up** 1: Wake-up suppressed
	6	R/W	**GPIO15_TYPE**	**0:** GPI: active low **GPO: supplied from external/VDD_IO1** 1: GPI: active high GPO: supplied from VDD_IO2
	5:4	R/W	**GPIO15_PIN**	PIN assigned to 00: GPO (Open drain, with optional blinking) 01: GPI **10: CLK (configured via GPIO14_PIN)** 11: GPO mode controlled (Open drain)
	3	R/W	**GPIO14_WEN**	**0: Passive to active transition triggers a wake-up** 1: Wake-up suppressed
	2	R/W	**GPIO14_TYPE**	**0:** GPI: active low **GPO: supplied from external/VDD_IO1** DATA/CLK supplied from VDD_IO1 (Note 1) 1: GPI: active high GPO: supplied from VDD_IO2 DATA/CLK supplied from VDD_IO2 (Note 1)
	1:0	R/W	**GPIO14_PIN**	PIN assigned to 00: GPO(Open drain, with optional blinking) 01: GPI **10: DATA (assigns GPIO15_PIN to CLK)** 11: GPO mode controlled (Push-pull)

Note 1 When using as HS-2-WIRE IF input logic levels are derived from VDDCORE.

Table 88: GPIO_MODE0_7

Register Address	Bit	Type	Label	Description
0x1D GPIO_MODE0_7	7	R/W	**GPIO7_ MODE**	0: GPI: debouncing off GPO: Sets output to low level (active low for sequencer control) 1: GPI: debouncing on GPO: Sets output to high level (active high for sequencer control)
	6	R/W	**GPIO6_ MODE**	0: GPI: debouncing off GPO: Sets output to low level (active low for sequencer control) 1: GPI: debouncing on GPO: Sets output to high level (active high for sequencer control)
	5	R/W	**GPIO5_ MODE**	0: GPI: debouncing off GPO: Sets output to low level 1: GPI: debouncing on GPO: Sets output to high level
	4	R/W	**GPIO4_ MODE**	0: GPI: debouncing off GPO: Sets output to low level(active low for sequencer control) 1: GPI: debouncing on GPO: Sets output to high level (active high for sequencer control)
	3	R/W	**GPIO3_ MODE**	0: GPI: debouncing off GPO: Sets output to low level (active low for sequencer control) 1: GPI: debouncing on GPO: Sets output to high level (active high for sequencer control)
	2	R/W	**GPIO2_MODE**	0: GPI: debouncing off GPO: Sets output to low level 1: GPI: debouncing on GPO: Sets output to high level
	1	R/W	**GPIO1_ MODE**	0: GPI: debouncing off GPO: Sets output to low level 1: GPI: debouncing on GPO: Sets output to high level
	0	R/W	**GPIO0_ MODE**	0: GPI: debouncing off GPO: Sets output to low level 1: GPI: debouncing on GPO: Sets output to high level

Table 89: GPIO_MODE8_15

Register Address	Bit	Type	Label	Description
0x1E GPIO_MODE8_15	7	R/W	**GPIO15_ MODE**	0: GPI: debouncing off GPO: Sets output to low level (active high for blinking) 1: GPI: debouncing on GPO: Sets output to high level (active low for blinking)

Register Address	Bit	Type	Label	Description
	6	R/W	**GPIO14_ MODE**	0: GPI: debouncing off GPO: Sets output to low level (active high for blinking) 1: GPI:debouncing on GPO: Sets output to high level (active low for blinking)
	5	R/W	**GPIO13_ MODE**	0: GPI: debouncing off GPO: Sets output to low level (active low for GP_FB1) 1: GPI: debouncing on GPO: Sets output to high level (active high for GP_FB1)
	4	R/W	**GPIO12_ MODE**	0: GPI: debouncing off GPO: Sets output to low level (active low for nVDD_FAULT, V_{SYS} monitor state) 1: GPI: debouncing on GPO: Sets output to high level (active high for nVDD_FAULT, V_{SYS} monitor state)
	3	R/W	**GPIO11_ MODE**	0: GPI: : debouncing off GPO: Sets output to low level (active high for blinking) 1: GPI: : debouncing on GPO: Sets output to high level (active low for blinking)
	2	R/W	**GPIO10_ MODE**	0: GPI/PWR1_EN: debouncing off GPO: Sets output to low level 1: GPI/PWR1_EN: debouncing on GPO: Sets output to high level
	1	R/W	**GPIO9_ MODE**	0: GPI/PWR_EN: debouncing off GPO: Sets output to low level (active low for sequencer control) 1: GPI/PWR_EN debouncing on GPO: Sets output to high level (active high for sequencer control)
	0	R/W	**GPIO8_ MODE**	0: GPI/SYS_EN: debouncing off GPO: Sets output to low level 1: GPI/SYS_EN: debouncing on GPO: Sets output to high level

Table 90: SWITCH_CONT

Register Address	Bit	Type	Label	Description
0x1F SWITCH_CONT	7	R/W	**CP_EN_MODE**	Rail switch charge pump is enabled **0: static** (does not shut down, when all switches are open) 1: auto, CP enabled before closing the first switch, CP disabled after last switch was opened
	6	R/W	**CORE_SW_INT**	Changes the CORE external switch controller into an internal switch between the output of BUCKCORE1 and port CORE_SWS/GPIO4

Register Address	Bit	Type	Label	Description
	5:4	R/W	**SWITCH_SR**	Maximum slew rate when closing the rail switch: **00: 1 mV/µs** 01: 5 mV/µs 10: 10 mV/µs 11: as fast as possible
	3:2	R/W	**PERI_SW_GPI**	GPIO closes PERI_SW on passive to active state transition, opens PERI_SW on active to passive state transition **00: Not controlled by GPIO** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	1:0	R/W	**CORE_SW_GPI**	GPIO closes CORE_SW on passive to active state transition, opens CORE_SW on active to passive state transition **00: Not controlled by GPIO** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled

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Table 91: BCORE2_CONT

Register Address	Bit	Type	Label	Description
0x20 BCORE2_CONT Note 1	7	R/W	**Reserved**	
	6:5	R/W	**VBCORE2_GPI**	GPIO select target voltage VBCORE2_A on passive to active transition, selects target voltage VBCORE2_B on active to passive transition (ramping) **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	4	R/W	Reserved	
	3	R/W	**BCORE2_CONF**	Sequencer target state of BCORE2_EN
	2:1	R/W	**BCORE2_GPI**	GPIO enables BUCKCORE2 on passive to active state transition, disables BUCKCORE2 on active to passive state transition **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	0	R/W	BCORE2_EN	**0: BUCKCORE2 disabled** 1: BUCKCORE2 enabled

Note 1 Disabled in BUCKCORE dual-phase mode.

Table 92: BCORE1_CONT

Register Address	Bit	Type	Label	Description
0x21 BCORE1_CONT	7	R/W	**CORE_SW_CONF**	Sequencer target state of CORE_SW_EN
	6:5	R/W	**VBCORE1_GPI**	GPIO select target voltage VBCORE1_A on passive to active transition, selects target voltage VBCORE1_B on active to passive transition (ramping) **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	4	R/W	CORE_SW_EN	**0: CORE_SW opened** 1: CORE_SW closed
	3	R/W	**BCORE1_CONF**	Sequencer target state of BCORE1_EN
	2:1	R/W	**BCORE1_GPI**	GPIO enables BUCKCORE1 on passive to active state transition, disables BUCKCORE1 on active to passive state transition **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	0	R/W	BCORE1_EN	**0: BUCKCORE1 disabled** 1: BUCKCORE1 enabled

Table 93: BPRO_CONT

Register Address	Bit	Type	Label	Description
0x22 BPRO_CONT	7	R/W	**Reserved**	
	6:5	R/W	**VBPRO_GPI**	GPIO select target voltage VBPRO_A on passive to active transition, selects target voltage VBPRO_B on active to passive transition (ramping) **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	4	R/W	Reserved	
	3	R/W	**BPRO_CONF**	Sequencer target state of BPRO_EN
	2:1	R/W	**BPRO_GPI**	GPIO enables BUCKPRO on passive to active state transition, disables BUCKPRO on active to passive state transition **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	0	R/W	BPRO_EN	**0: BUCKPRO disabled** 1: BUCKPRO enabled

Table 94: BMEM_CONT

Register Address	Bit	Type	Label	Description
0x23 BMEM_CONT	7	R/W	**Reserved**	
	6:5	R/W	**VBMEM_GPI**	GPIO select target voltage VBMEM_A on passive to active transition, selects target voltage VBMEM_B on active to passive transition (ramping) **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	4	R/W	Reserved	
	3	R/W	**BMEM_CONF**	Sequencer target state of BMEM_EN in case of being a default supply)
	2:1	R/W	**BMEM_GPI**	GPIO enables BUCKMEM on passive to active state transition, disables BUCKMEM on active to passive state transition **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	0	R/W	BMEM_EN	**0: BUCKMEM disabled** 1: BUCKMEM enabled

Table 95: BIO_CONT

Register Address	Bit	Type	Label	Description
0x24 BIO_CONT	7	R/W	**Reserved**	
	6:5	R/W	**VBIO_GPI**	GPIO select target voltage VBIO_A on passive to active transition, selects target voltage VBIO_B on active to passive transition (ramping) **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	4	R/W	Reserved	
	3	R/W	**BIO_CONF**	Sequencer target state of BIO_EN
	2:1	R/W	**BIO_GPI**	GPIO enables BUCKIO on passive to active state transition, disables BUCKIO on active to passive state transition **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	0	R/W	BIO_EN	**0: BUCKIO disabled** 1: BUCKIO enabled

Table 96: BPERI_CONT

Register Address	Bit	Type	Label	Description
0x25 BPERI_CONT	7	R/W	**PERI_SW_CONF**	Sequencer target state of PERI_SW_EN
	6:5	R/W	**VBPERI_GPI**	GPIO select target voltage VBPERI_A on passive to active transition, selects target voltage VBPERI_B on active to passive transition (ramping) **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	4	R/W	PERI_SW_EN	**0: PERI_SW opened** 1: PERI_SW closed
	3	R/W	**BPERI_CONF**	Sequencer target state of BPERI_EN
	2:1	R/W	**BPERI_GPI**	GPIO enables BUCKPERI on passive to active state transition, disables BUCKPERI on active to passive state transition **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	0	R/W	**BPERI_EN**	**0: BUCKPERI disabled** 1: BUCKPERI enabled

Table 97: LDO1_CONT

Register Address	Bit	Type	Label	Description
0x26 LDO1_CONT	7	R/W	**LDO1_CONF**	Sequencer target state of LDO1_EN
	6:5	R/W	**VLDO1_GPI**	GPIO select target voltage VLDO1_A on passive to active transition, selects target voltage VLDO1_B on active to passive transition (ramping) **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	4	R/W	Reserved	
	3	R/W	**LDO1_PD_DIS**	**0: Enable pull-down resistor** 1: No pull-down resistor in disabled mode
	2:1	R/W	**LDO1_GPI**	GPIO enables LDO1 on passive to active state transition, disables LDO1 on active to passive state transition **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	0	R/W	LDO1_EN	**0: LDO1 disabled** 1: LDO1 enabled

Table 98: LDO2_CONT

Register Address	Bit	Type	Label	Description
0x27 LDO2_CONT	7	R/W	**LDO2_CONF**	Sequencer target state of LDO2_EN
	6:5	R/W	**VLDO2_GPI**	GPIO select target voltage VLDO2_A on passive to active transition, selects target voltage VLDO2_B on active to passive transition (ramping) **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	4	R/W	Reserved	
	3	R/W	**LDO2_PD_DIS**	**0: Enable pull-down resistor** 1: No pull-down resistor in disabled mode
	2:1	R/W	**LDO2_GPI**	GPIO enables LDO2 on passive to active state transition, disables LDO2 on active to passive state transition **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	0	R/W	LDO2_EN	**0: LDO2 disabled** 1: LDO2 enabled

Table 99: LDO3_CONT

Register Address	Bit	Type	Label	Description
0x28 LDO3_CONT	7	R/W	**LDO3_CONF**	Sequencer target state of LDO3_EN
	6:5	R/W	**VLDO3_GPI**	GPIO select target voltage VLDO3_A on passive to active transition, selects target voltage VLDO3_B on active to passive transition (ramping) **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	4	R/W	Reserved	
	3	R/W	**LDO3_PD_DIS**	**0: Enable pull-down resistor** 1: No pull-down resistor in disabled mode
	2:1	R/W	**LDO3_GPI**	GPIO enables LDO3 on passive to active state transition, disables LDO3 on active to passive state transition **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	0	R/W	LDO3_EN	**0: LDO3 disabled** 1: LDO3 enabled

Table 100: LDO4_CONT

Register Address	Bit	Type	Label	Description
0x29 LDO4_CONT	7	R/W	**LDO4_CONF**	Sequencer target state of LDO4_EN
	6:5	R/W	**VLDO4_GPI**	GPIO select target voltage VLDO4_A on passive to active transition, selects target voltage VLDO4_B on active to passive transition (ramping) **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	4	R/W	Reserved	
	3	R/W	**LDO4_PD_DIS**	**0: Enable pull-down resistor** 1: No pull-down resistor in disabled mode
	2:1	R/W	**LDO4_GPI**	GPIO enables LDO4 on passive to active state transition, disables LDO4 on active to passive state transition **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	0	R/W	LDO4_EN	**0: LDO4 disabled** 1: LDO4 enabled

Table 101: LDO5_CONT

Register Address	Bit	Type	Label	Description
0x2A LDO5_CONT	7	R/W	**LDO5_CONF**	Sequencer target state of LDO5_EN
	6:5	R/W	**VLDO5_GPI**	GPIO select target voltage VLDO5_A on passive to active transition, selects target voltage VLDO5_B on active to passive transition (immediate voltage change) **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	4	R/W	VLDO5_SEL	LDO5 voltage is selected from (immediate change): **0: VLDO5_A** 1: VLDO5_B
	3	R/W	**LDO5_PD_DIS**	**0: Enable pull-down resistor** 1: No pull-down resistor in disabled mode
	2:1	R/W	**LDO5_GPI**	GPIO enables LDO5 on passive to active state transition, disables LDO6 on active to passive state transition **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled

Register Address	Bit	Type	Label	Description
	0	R/W	LDO5_EN	**0: LDO5 disabled** 1: LDO5 enabled

Table 102: LDO6_CONT

Register Address	Bit	Type	Label	Description
0x2B LDO6_CONT	7	R/W	**LDO6_CONF**	Sequencer target state of LDO6_EN
	6:5	R/W	**VLDO6_GPI**	GPIO select target voltage VLDO6_A on passive to active transition, selects target voltage VLDO6_B on active to passive transition (immediate voltage change) **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	4	R/W	VLDO6_SEL	LDO6 voltage is selected from (immediate change): **0: VLDO6_A** 1: VLDO6_B
	3	R/W	**LDO6_PD_DIS**	**0: Enable pull-down resistor** 1: No pull-down resistor in disabled mode
	2:1	R/W	**LDO6_GPI**	GPIO enables LDO6 on passive to active state transition, disables LDO6 on active to passive state transition **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	0	R/W	LDO6_EN	**0: LDO6 disabled** 1: LDO6 enabled

Table 103: LDO7_CONT

Register Address	Bit	Type	Label	Description
0x2C LDO7_CONT	7	R/W	**LDO7_CONF**	Sequencer target state of LDO7_EN
	6:5	R/W	**VLDO7_GPI**	GPIO select target voltage VLDO7_A on passive to active transition, selects target voltage VLDO7_B on active to passive transition (immediate voltage change) **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	4	R/W	VLDO7_SEL	LDO7 voltage is selected from (immediate change): **0: VLDO7_A** 1: VLDO7_B
	3	R/W	**LDO7_PD_DIS**	**0: Enable pull-down resistor** 1: No pull-down resistor in disabled mode

Register Address	Bit	Type	Label	Description
	2:1	R/W	**LDO7_GPI**	GPIO enables LDO7 on passive to active state transition, disables LDO7 on active to passive state transition **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	0	R/W	LDO7_EN	**0: LDO7 disabled** 1: LDO7 enabled

Table 104: LDO8_CONT

Register Address	Bit	Type	Label	Description
0x2D LDO8_CONT	7	R/W	**LDO8_CONF**	Sequencer target state of LDO8_EN
	6:5	R/W	**VLDO8_GPI**	GPIO select target voltage VLDO8_A on passive to active transition, selects target voltage VLDO8_B on active to passive transition (immediate voltage change) **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	4	R/W	VLDO8_SEL	LDO8 voltage is selected from (immediate change): **0: VLDO8_A** 1: VLDO8_B
	3	R/W	**LDO8_PD_DIS**	**0: Enable pull-down resistor** 1: No pull-down resistor in disabled mode
	2:1	R/W	**LDO8_GPI**	GPIO enables LDO8 on passive to active state transition, disables LDO8 on active to passive state transition **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	0	R/W	LDO8_EN	**0: LDO8 disabled** 1: LDO8 enabled

Table 105: LDO9_CONT

Register Address	Bit	Type	Label	Description
0x2E LDO9_CONT	7	R/W	**LDO9_CONF**	Sequencer target state of LDO9_EN
	6:5	R/W	**VLDO9_GPI**	GPIO select target voltage VLDO9_A on passive to active transition, selects target voltage VLDO9_B on active to passive transition (immediate voltage change) **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled

Register Address	Bit	Type	Label	Description
	4	R/W	VLDO9_SEL	LDO9 voltage is selected from (immediate change): **0: VLDO9_A** 1: VLDO9_B
	3	R/W	**LDO9_PD_DIS**	**0: Enable pull-down resistor** 1: No pull-down resistor in disabled mode
	2:1	R/W	**LDO9_GPI**	GPIO enables LDO9 on passive to active state transition, disables LDO9 on active to passive state transition **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	0	R/W	LDO9_EN	**0: LDO9 disabled** 1: LDO9 enabled

Table 106: LDO10_CONT

Register Address	Bit	Type	Label	Description
0x2F LDO10_CONT	7	R/W	**LDO10_CONF**	Sequencer target state of LDO10_EN
	6:5	R/W	**VLDO10_GPI**	GPIO select target voltage VLDO10_A on passive to active transition, selects target voltage VLDO10_B on active to passive transition (immediate voltage change) **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	4	R/W	VLDO10_SEL	LDO10 voltage is selected from (immediate change): **0: VLDO10_A** 1: VLDO10_B
	3	R/W	**LDO10_PD_DIS**	**0: Enable pull-down resistor** 1: No pull-down resistor in disabled mode
	2:1	R/W	**LDO10_GPI**	GPIO enables LDO10 on passive to active state transition, disables LDO10 on active to passive state transition **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	0	R/W	LDO10_EN	**0: LDO10 disabled** 1: LDO10 enabled

Table 107: LDO11_CONT

Register Address	Bit	Type	Label	Description
0x30 LDO11_CONT	7	R/W	**LDO11_CONF**	Sequencer target state of LDO11_EN
	6:5	R/W	**VLDO11_GPI**	GPIO select target voltage VLDO11_A on passive to active transition, selects target voltage VLDO11_B on active to passive transition (immediate voltage change) **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	4	R/W	**VLDO11_SEL**	LDO11 voltage is selected from (immediate change): **0: VLDO11_A** 1: VLDO11_B
	3	R/W	**LDO11_PD_DIS**	**0: Enable pull-down resistor** 1: No pull-down resistor in disabled mode
	2:1	R/W	**LDO11_GPI**	GPIO enables LDO11 on passive to active state transition, disables LDO11 on active to passive state transition **00: Not controlled by GPIO (sequencer control)** 01: GPIO1 controlled 10: GPIO2 controlled 11: GPIO13 controlled
	0	R/W	**LDO11_EN**	**0: LDO11 disabled** 1: LDO11 enabled

Table 108: VIB

Register Address	Bit	Type	Label	Description
0x31 VIB	7:6	R/W	**Reserved**	
	5:0	R/W	**VIB_SET**	000000: OFF-BREAK, NMOS on, PMOS off 000001: 47.55 mV 000010: 95.1 mV … Average output level set in a range of 0 to 3 V in steps of 3 V/63 … … **111111: 3.0 V**

Table 109: DVC_1

Register Address	Bit	Type	Label	Description
0x32 DVC_1	7	R/W	VLDO3_SEL	LDO3 voltage is selected from (ramping): **0: VLDO3_A** 1: VLDO3_B
	6	R/W	VLDO2_SEL	LDO2 voltage is selected from (ramping): **0: VLDO2_A** 1: VLDO2_B

Register Address	Bit	Type	Label	Description
	5	R/W	VLDO1_SEL	LDO1 voltage is selected from (ramping): **0: VLDO1_A** 1: VLDO1_B
	4	R/W	VBPERI_SEL	BUCKPERI voltage is selected from (ramping): **0: VBPERI_A** 1: VBPERI_B
	3	R/W	VBMEM_SEL	BUCKMEM voltage is selected from (ramping): **0: VBMEM_A** 1: VBMEM_B
	2	R/W	VBPRO_SEL	BUCKPRO voltage is selected from (ramping): **0: VBPRO_A** 1: VBPRO_B
	1	R/W	VBCORE2_SEL	BUCKCORE2 voltage is selected from (ramping): **0: VBCORE2_A** 1: VBCORE2_B
	0	R/W	VBCORE1_SEL	BUCKCORE1 voltage is selected from (ramping): **0: VBCORE1_A** 1: VBCORE1_B

Table 110: DVC_2

Register Address	Bit	Type	Label	Description
0x33 DVC_2	7	R/W	VLDO4_SEL	LDO4 voltage is selected from (ramping): **0: VLDO4_A** 1: VLDO4_B
	6:1	R/W	Reserved	
	0	R/W	VBIO_SEL	BUCKIO voltage is selected from (ramping): **0: VBIO_A** 1: VBIO_B

A.2.4 GPADC

Table 111: ADC_MAN

Register Address	Bit	Type	Label	Description
0x34 ADC_MAN	7:6	R/W	**Reserved**	
	5	R/W	**ADC_MODE**	**0: Measurement sequence interval 10 ms (economy mode)** 1: Measurement sequence interval 1 ms
	4	R/W	ADC_MAN	Perform manual conversion. Bit is reset to 0 when conversion is complete.
	3:0	R/W	**ADC_MUX**	Manual measurement selects: 0000: VSYS port 0001: ADCIN1 0010: ADCIN2 0011: ADCIN3 **0100: internal T-Sense** 0101: V_{BBAT}-voltage 0110: reserved 0111: reserved 1000: Group 1 regulators voltage 1001: Group 2 regulators voltage 1010: Group 3 regulators voltage > 1010: reserved

Table 112: ADC_CONT

Register Address	Bit	Type	Label	Description
0x35 ADC_CONT	7	R/W	**COMP1V2_EN**	**0: Disable 1.2 V comparator at ADCIN2** 1: Enable 1.2 V comparator
	6	R/W	**AD3_ISRC_EN**	**0: Disable ADCIN3 current source** 1: Enable ADCIN3 current source
	5	R/W	**AD2_ISRC_EN**	**0: Disable ADCIN2 current source** 1: Enable ADCIN2 current source
	4	R/W	**AD1_ISRC_EN**	**0: Disable ADCIN1 current source** 1: Enable ADCIN1 current source
	3	R/W	**AUTO_AD3_EN**	**0: ADCIN3 auto-measurements disabled** 1: ADCIN3 auto-measurements enabled
	2	R/W	**AUTO_AD2_EN**	**0: ADCIN2 auto-measurements disabled** 1: ADCIN2 auto-measurements enabled
	1	R/W	**AUTO_AD1_EN**	**0: ADCIN1 auto-measurements disabled** 1: ADCIN1 auto-measurements enabled
	0	R/W	**AUTO_VSYS_EN**	**0: VSYS auto-measurements disabled when charger/vibration motor driver is off** 1: VSYS auto-measurements enabled

Table 113: VSYS_MON

Register Address	Bit	Type	Label	Description
0x36 VSYS_MON	7:0	R/W	VSYS_MON	VSYS_MON threshold setting (8-bit). 00000000 corresponds to 2.5 V 11111111 corresponds to 5.5 V

A.2.5 ADC Results

Table 114: ADC_RES_L

Register Address	Bit	Type	Label	Description
0x37 ADC_RES_L	7:6	R	ADC_RES_LSB	10-bit manual conversion result (2 LSBs)
	5:0	R	Reserved	

Table 115: ADC_RES_H

Register Address	Bit	Type	Label	Description
0x38 ADC_RES_H	7:0	R	ADC_RES_MSB	10-bit manual conversion result (8 MSBs)

Table 116: VSYS_RES

Register Address	Bit	Type	Label	Description
0x39 VSYS_RES	7:0	R	VSYS_RES	0x00 – 0xFF: Auto VSYS conversion result (A0) 0x00 corresponds to 2.5 V 0xFF corresponds to 5.5 V

Table 117: ADCIN1_RES

Register Address	Bit	Type	Label	Description
0x3A ADCIN1_RES	7:0	R	ADCIN1_RES	0x00 – 0xFF: Auto ADC ADCIN1 conversion result

Table 118: ADCIN2_RES

Register Address	Bit	Type	Label	Description
0x3B ADCIN2_RES	7:0	R	ADCIN2_RES	0x00 – 0xFF: Auto ADC ADCIN2 conversion result

Table 119: ADCIN3_RES

Register Address	Bit	Type	Label	Description
0x3C ADCIN3_RES	7:0	R	ADCIN3_RES	0x00 – 0xFF: Auto ADC ADCIN3 conversion result

Table 120: MON_A8_RES

Register Address	Bit	Type	Label	Description
0x3D MON_A8_RES	7:0	R	MON_A8_RES	0x00 – 0xFF: Regulator output voltage monitor 1 (A8) conversion result 0x00 corresponds to 0.0 V 0xFF corresponds to 5.0 V

Table 121: MON_A9_RES

Register Address	Bit	Type	Label	Description
0x3E MON_A9_RES	7:0	R	MON_A9_RES	0x00 – 0xFF: Regulator output voltage monitor 2 (A9) conversion result 0x00 corresponds to 0.0 V 0xFF corresponds to 5.0 V

Table 122: MON_A10_RES

Register Address	Bit	Type	Label	Description
0x3F MON_A10_RES	7:0	R	MON_A10_RES	0x00 – 0xFF: Regulator output voltage monitor 3 (A10) conversion result 0x00 corresponds to 0.0 V 0xFF corresponds to 5.0 V

A.2.6 RTC Calendar and Alarm

Table 123: COUNT_S

Register Address	Bit	Type	Label	Description
0x40 COUNT_S	7	R	RTC_READ	Asserted when below registers have been transferred from RTC logic into host readable registers (for example, after leaving POR)
	6	R	Reserved	
	5:0	R/W	COUNT_SEC	0x00 – 0x3B: RTC seconds read-out. A read of this register latches the current RTC calendar count into the registers COUNT_S to COUNT_Y coherent for approx 0.5 s).

Table 124: COUNT_MI

Register Address	Bit	Type	Label	Description
0x41 COUNT_MI	7:6	R	Reserved	
	5:0	R/W	COUNT_MIN	0x00 – 0x3B: RTC minutes read-out

Table 125: COUNT_H

Register Address	Bit	Type	Label	Description
0x42 COUNT_H	7:5	R	Reserved	
	4:0	R/W	COUNT_HOUR	0x00 – 0x17: RTC hours read-out

Table 126: COUNT_D

Register Address	Bit	Type	Label	Description
0x43 COUNT_D	7:5	R	Reserved	
	4:0	R/W	COUNT_DAY	0x01 – 0x1F: RTC days read-out

Table 127: COUNT_MO

Register Address	Bit	Type	Label	Description
0x44	7:4	R	Reserved	

Register Address	Bit	Type	Label	Description
COUNT_MO	3:0	R/W	COUNT_MONTH	0x01 – 0x0C: RTC months read-out

Table 128: COUNT_Y

Register Address	Bit	Type	Label	Description
0x45 COUNT_Y	7	R	Reserved	
	6	R/W	MONITOR	Read-out 0 indicates that the power was lost. Read-out of 1 indicates that the clock is OK Set to 1 when setting time to arm RTC monitor function. Cannot be cleared via register write.
	5:0	R/W	COUNT_YEAR	0x00 – 0x3F: RTC years read-out (0 corresponds to year 2000). A write to this register latches the registers COUNT_S to COUNT_Y into the current RTC calendar counters.

Table 129: ALARM_S

Register Address	Bit	Type	Label	Description
0x46 ALARM_S	7:6	R	ALARM_TYPE	Alarm event caused by: 00: No alarm 01: Tick 10: Timer alarm 11: Both
	5:0	R/W	ALARM_SEC	0x00 – 0x3B: Alarm seconds setting

Table 130: ALARM_MI

Register Address	Bit	Type	Label	Description
0x47 ALARM_MI	7:6	R	Reserved	
	5:0	R/W	ALARM_MIN	0x00 – 0x3B: Alarm minutes setting

Table 131: ALARM_H

Register address	Bit	Type	Label	Description
0x48 ALARM_H	7:5	R	Reserved	
	4:0	R/W	ALARM_HOUR	0x00 – 0x17: Alarm hours setting

Table 132: ALARM_D

Register Address	Bit	Type	Label	Description
0x49 ALARM_D	7:5	R	Reserved	
	4:0	R/W	ALARM_DAY	0x01 – 0x1F: Alarm days setting

Table 133: ALARM_MO

Register Address	Bit	Type	Label	Description
0x4A	7:6	R	Reserved	

Register Address	Bit	Type	Label	Description
ALARM_MO	5	R/W	TICK_WAKE	Tick alarm wake-up 0: disabled 1: enabled
	4	R/W	TICK_TYPE	Tick alarm interval is: 0: one second 1: one minute
	3:0	R/W	ALARM_MONTH	0x01 – 0x0C: Alarm months setting

Table 134: ALARM_Y

Register Address	Bit	Type	Label	Description
0x4B ALARM_Y	7	R/W	TICK_ON	0: Tick function is disabled 1: Periodic tick alarm enabled
	6	R/W	ALARM_ON	0: Alarm function is disabled 1: Alarm enabled
	5:0	R/W	ALARM_YEAR	0x00 – 0x3F: Alarm years setting (0 corresponds to year 2000). A write to this register latches the registers ALARM_MI to ALARM_Y

Table 135: SECOND_A

Register Address	Bit	Type	Label	Description
0x4C SECOND_A	7:0	R	SECONDS_A	RTC seconds counter A (LSBs). A read of this register latches the current 32-bit counter into the registers SECOND_A to SECOND_D (coherent for approx. 0.5 s).

Table 136: SECOND_B

Register Address	Bit	Type	Label	Description
0x4D SECOND_B	7:0	R	SECONDS_B	RTC seconds counter B

Table 137: SECOND_C

Register Address	Bit	Type	Label	Description
0x4E SECOND_C	7:0	R	SECONDS_C	RTC seconds counter C

Table 138: SECOND_D

Register Address	Bit	Type	Label	Description
0x4F SECOND_D	7:0	R	SECONDS_D	RTC seconds counter D (MSBs)

Table 139: Co-PMIC

Register Address	Bit	Type	Label	Description
0x50 CoPMIC_S	7:0	R	Reserved	Reserved for Co-PMIC
0x67 CoPMIC_E	7:0	R	Reserved	Reserved for Co-PMIC

Table 140: CHG_Co

Register Address	Bit	Type	Label	Description
0x68 CHG_Co_S	7:0	R	Reserved	Reserved for companion charger
0x7F CHG_Co_E	7:0	R	Reserved	Reserved for companion charger

A.3 Register Page 1

Table 141: PAGE_CON

Register Address	Bit	Type	Label	Description
0x80 PAGE_CON	7	RW	REVERT	See register 0x00, Table 59
	6	RW	WRITE_MODE	
	5:3	RW	Reserved	
	2:0	RW	REG_PAGE	

A.3.1 Power Sequencer

Table 142: SEQ

Register Address	Bit	Type	Label	Description
0x81 SEQ	7:4	R/W	NXT_SEQ_START	Start time slot for first sequencing after being modified via register write
	3:0	R	SEQ_POINTER	Actual pointer position (time slot) of power sequencer

Table 143: SEQ_TIMER

Register Address	Bit	Type	Label	Description
0x82 SEQ_TIMER	7:4	R/W	**SEQ_DUMMY**	0000: 32 µs 0001: 64 µs 0010: 96 µs 0011: 128 µs 0100: 160 µs 0101: 192 µs 0110: 224 µs 0111: 256 µs 1000: 288 µs 1001: 384 µs 1010: 448 µs 1011: 512 µs 1100: 1.024 ms **1101: 2.048 ms** 1110: 4.096 ms 1111: 8.192 ms

Register Address	Bit	Type	Label	Description
	3:0	R/W	**SEQ_TIME**	0000: 32 µs 0001: 64 µs 0010: 96 µs 0011: 128 µs 0100: 160 µs 0101: 192 µs 0110: 224 µs 0111: 256 µs 1000: 288 µs 1001: 384 µs 1010: 448 µs 1011: 512 µs **1100: 1.024 ms** 1101: 2.048 ms 1110: 4.096 ms 1111: 8.192 ms

Table 144: ID_2_1

Register Address	Bit	Type	Label	Description
0x83 ID_2_1	7:4	R/W	**LDO2_STEP**	Power sequencer time slot for LDO2 control
	3:0	R/W	**LDO1_STEP**	Power sequencer time slot for LDO1 control

Table 145: ID_4_3

Register Address	Bit	Type	Label	Description
0x84 ID_4_3	7:4	R/W	**LDO4_STEP**	Power sequencer time slot for LDO4 control
	3:0	R/W	**LDO3_STEP**	Power sequencer time slot for LDO3 control

Table 146: ID_6_5

Register Address	Bit	Type	Label	Description
0x85 ID_6_5	7:4	R/W	**LDO6_STEP**	Power sequencer time slot for LDO6 control
	3:0	R/W	**LDO5_STEP**	Power sequencer time slot for LDO5 control

Table 147: ID_8_7

Register Address	Bit	Type	Label	Description
0x86 ID_8_7	7:4	R/W	**LDO8_STEP**	Power sequencer time slot for LDO8 control
	3:0	R/W	**LDO7_STEP**	Power sequencer time slot for LDO7 control

Table 148: ID_10_9

Register Address	Bit	Type	Label	Description
0x87 ID_10_9	7:4	R/W	**LDO10_STEP**	Power sequencer time slot for LDO10 control
	3:0	R/W	**LDO9_STEP**	Power sequencer time slot for LDO9 control

Table 149: ID_12_11

Register Address	Bit	Type	Label	Description
0x88 ID_12_11	7:4	R/W	**PD_DIS_STEP**	Power sequencer time slot for control of blocks to be disabled/paused during POWERDOWN mode

Register Address	Bit	Type	Label	Description
	3:0	R/W	**LDO11_STEP**	Power sequencer time slot for LDO11 control

Table 150: ID_14_13

Register Address	Bit	Type	Label	Description
0x89 ID_14_13	7:4	R/W	**BUCKCORE2_STEP**	Power sequencer time slot for control of BUCKCORE2 (disabled in BUCKCORE dual phase mode)
	3:0	R/W	**BUCKCORE1_STEP**	Power sequencer time slot for control of BUCKCORE1

Table 151: ID_16_15

Register Address	Bit	Type	Label	Description
0x8A ID_16_15	7:4	R/W	**BUCK_IO_STEP**	Power sequencer time slot for control of BUCKPRO
	3:0	R/W	**BUCKPRO_STEP**	Power sequencer time slot for control of BUCKPRO

Table 152: ID_18_17

Register Address	Bit	Type	Label	Description
0x8B ID_18_17	7:4	R/W	**BUCKPERI_STEP**	Power sequencer time slot for control of BUCKPERI
	3:0	R/W	**BUCKMEM_STEP**	Power sequencer time slot for control of BUCKMEM

Table 153: ID_20_19

Register Address	Bit	Type	Label	Description
0x8C ID_20_19	7:4	R/W	**PERI_SW_STEP**	Power sequencer time slot for control of PERI rail switch
	3:0	R/W	**CORE_SW_STEP**	Power sequencer time slot for control of CORE rail switch

Table 154: ID_22_21

Register Address	Bit	Type	Label	Description
0x8D ID_22_21	7:4	R/W	**GP_FALL1_STEP**	Power sequencer time slot for falling edge control of GPO2
	3:0	R/W	**GP_RISE1_STEP**	Power sequencer time slot for rising edge control of GPO2

Table 155: ID_24_23

Register Address	Bit	Type	Label	Description
0x8E ID_24_23	7:4	R/W	**GP_FALL2_STEP**	Power sequencer time slot for falling edge control of GPO7
	3:0	R/W	**GP_RISE2_STEP**	Power sequencer time slot for rising edge control of GPO7

Table 156: ID_26_25

Register Address	Bit	Type	Label	Description
0x8F ID_26_25	7:4	R/W	**GP_FALL3_STEP**	Power sequencer time slot for falling edge control of GPO8
	3:0	R/W	**GP_RISE3_STEP**	Power sequencer time slot for rising edge control of GPO8

Table 157: ID_28_27

Register Address	Bit	Type	Label	Description
0x90 ID_28_27	7:4	R/W	**GP_FALL4_STEP**	Power sequencer time slot for falling edge control of GPO9
	3:0	R/W	**GP_RISE4_STEP**	Power sequencer time slot for rising edge control of GPO9

Table 158: ID_30_29

Register Address	Bit	Type	Label	Description
0x91 ID_30_29	7:4	R/W	**GP_FALL5_STEP**	Power sequencer time slot for falling edge control of GPO11
	3:0	R/W	**GP_RISE5_STEP**	Power sequencer time slot for rising edge control of GPO11

Table 159: ID_32_31

Register Address	Bit	Type	Label	Description
0x92 ID_32_31	7:4	R/W	**EN32K_STEP**	Power sequencer time slot for enable/disable of 32K output signals
	3:0	R/W	**WAIT_STEP**	Power sequencer time slot that gates the progress with state of GPI10 (or used a dedicated delay timer)

Table 160: Reserved

Register Address	Bit	Type	Label	Description
0x93, 0x94	7:0	R/W	**Reserved**	

Table 161: SEQ_A

Register Address	Bit	Type	Label	Description
0x95 SEQ_A	7:4	R/W	**POWER_END**	OTP pointer to last supply of domain POWER
	3:0	R/W	**SYSTEM_END**	OTP pointer to last supply of domain SYSTEM

Table 162: SEQ_B

Register Address	Bit	Type	Label	Description
0x96 SEQ_B	7:4	R/W	**PART_DOWN**	OTP pointer for partial POWERDOWN mode
	3:0	R/W	**MAX_COUNT**	OTP pointer to last supply of domain POWER1

Table 163: WAIT

Register Address	Bit	Type	Label	Description
0x97 WAIT	7:6	R/W	**WAIT_DIR**	**00: No wait during power sequencing** 01: Wait during power-up sequence 10:: Wait during power-down sequence 11: Wait during power-up and power-down sequence
	5	R/W	**TIME_OUT**	**0: No time limit** 1: 500 ms time out for waiting GPIO10 to get active
	4	R/W	**WAIT_MODE**	0: Wait for GPIO10 to be active **1: Timer mode (start timer and wait for expire)**
	3:0	R/W	**WAIT_TIME**	0000: 0.0 µs 0001: 512 µs 0010: 1.0 ms 0011: 2.0 ms 0100: 4.1 ms 0101: 8.2 ms 0110: 16.4 ms 0111: 32.8 ms 1000: 65.5 ms 1001: 128 ms 1010: 256 ms **1011: 512 ms** 1100: 1.0 s 1101: 2.1 s 1110: 4.2 s 1111: 8.4 s

Table 164: EN_32K

Register Address	Bit	Type	Label	Description
0x98 EN_32K	7	R/W	**EN_32KOUT**	0: 32K clock buffer off (OUT_32K) **1: 32K clock buffer enabled** (OUT_32K), when powering up with a power sequence including EN32K_STEP the buffer is enabled when reaching EN32K_STEP, in case the power sequence includes PD_DIS_STEP with OUT_32K_PAUSE asserted the buffer enable is delayed until reaching PD_DIS_STEP on the way up Note: with OUT_CLOCK being asserted the buffer enable is delayed until 32 kHz oscillator signal is stable
	6	R/W	**RTC_CLOCK**	0: No gating of RTC calendar clock **1: Clock to RTC counter is gated until 32 kHz oscillator stabilization timer has expired**
	5	R/W	**OUT_CLOCK**	0: No gating of OUT_32K and clock signals at GP_FB3 **1: Clock to buffers is gated until 32 kHzoscillation stabilization timer has expired (indicating stable 32 kHz oscillator signal)**

Register Address	Bit	Type	Label	Description
	4	R/W	**DELAY_MODE**	**0: Start stabilization timer when duty cycle of oscillator signal is in between 30% and 70%** 1: Start stabilization timer when CRYSTAL is asserted, RTC_EN changed or when leaving DELIVERY/NO-POWER mode with CRYSTAL asserted
	3	R/W	**CRYSTAL**	0: No 32 kHz crystal connected (bypass via XOUT) **1: 32 kHz crystal connected**
	2:0	R/W	**STABILIZATION_TIME**	Time to allow crystal oscillator to stabilize: 000: 0.0 s (delay off) **001: 0.52 s** 010: 1.0 s 011: 1.5 s 100: 2.1 s 101: 2.6 s 110: 3.1 s 111: 3.6 s

Table 165: RESET

Register Address	Bit	Type	Label	Description
0x99 RESET	7:6	R/W	**RESET_EVENT**	RESET timer started by 00: EXT_WAKEUP **01: SYS_UP** 10: PWR_UP 11: leaving PMIC RESET state (do not use in combination with nRES_MODE = 1)
	5:0	R/W	**RESET_TIMER**	000000: 0.000 ms 000001: 1.024 ms 000010: 2.048 ms 000011: 3.072 ms 000100: 4.096 ms **000101: 5.120 ms** …. 011110: 30.720 ms 011111: 31.744 ms 100000: 32.768 ms 100001: 65.536 ms 100010: 98.304 ms ….. 111101: 983.040 ms 111110: 1015.808 ms 111111: 1048.576 ms

A.3.2 Regulator Settings

Table 166: BUCK_ILIM_A

Register Address	Bit	Type	Label	Description
0x9A BUCK_ILIM_A	7:4	R/W	**BMEM_ILIM**	BUCKMEM current limit (all limits x2 in MERGE mode) 0000:1500 mA 0001:1600 mA 0010:1700 mA 0011:1800 mA 0100:1900 mA 0101:2000 mA 0110:2100 mA 0111:2200 mA 1000:2300 mA 1001:2400 mA 1010:2500 mA 1011:2600 mA 1100:2700 mA 1101:2800 mA 1110:2900 mA 1111:3000 mA
	3:0	R/W	**BIO_ILIM**	BUCKIO current limit 0000:1500 mA 0001:1600 mA 0010:1700 mA 0011:1800 mA 0100:1900 mA 0101:2000 mA 0110:2100 mA 0111:2200 mA 1000:2300 mA 1001:2400 mA 1010:2500 mA 1011:2600 mA 1100:2700 mA 1101:2800 mA 1110:2900 mA 1111:3000 mA

Table 167: BUCK_ILIM_B

Register Address	Bit	Type	Label	Description
0x9B BUCK_ILIM_B	7:4	R/W	**BPERI_ILIM**	BUCKPERI current limit 0000:1500 mA 0001:1600 mA 0010:1700 mA 0011:1800 mA 0100:1900 mA 0101:2000 mA 0110:2100 mA 0111:2200 mA 1000:2300 mA 1001:2400 mA 1010:2500 mA 1011:2600 mA 1100:2700 mA 1101:2800 mA 1110:2900 mA 1111:3000 mA
	3:0	R/W	**BPRO_ILIM**	BUCKPRO current limit (all limits x2 in full-current mode) 0000:500 mA 0001:600 mA 0010:700 mA 0011:800 mA 0100:900 mA 0101:1000 mA 0110:1100 mA 0111:1200 mA 1000:1300 mA 1001:1400 mA 1010:1500 mA 1011:1600 mA 1100:1700 mA 1101:1800 mA 1110:1900 mA 1111:2000 mA

Table 168: BUCK_ILIM_C

Register Address	Bit	Type	Label	Description
0x9C BUCK_ILIM_C	7:4	R/W	**BCORE2_ILIM**	BUCKCORE2 current limit (all limits x2 in full-current mode) 0000:500 mA 0001:600 mA 0010:700 mA 0011:800 mA 0100:900 mA 0101:1000 mA 0110:1100 mA 0111:1200 mA 1000:1300 mA 1001:1400 mA 1010:1500 mA 1011:1600 mA 1100:1700 mA 1101:1800 mA 1110:1900 mA 1111:2000 mA

Register Address	Bit	Type	Label	Description
	3:0	R/W	**BCORE1_ILIM**	BUCKCORE1 current limit (all limits x2 in full-current mode) 0000:500 mA 0001:600 mA 0010:700 mA 0011:800 mA 0100:900 mA 0101:1000 mA 0110:1100 mA 0111:1200 mA 1000:1300 mA 1001:1400 mA 1010:1500 mA 1011:1600 mA 1100:1700 mA 1101:1800 mA 1110:1900 mA 1111:2000 mA

Table 169: BCORE2_CONF

Register Address	Bit	Type	Label	Description
0x9D BCORE2_CONF	7:6	R/W	**BCORE2_MODE**	00: Sleep/Synchronous mode controlled via voltage A and B registers 01: BUCKCORE2 always operates in Sleep mode 10: BUCKCORE2 always operates in Synchronous mode **11: BUCKCORE2 operates in Automatic mode**
	5	R/W	**BCORE2_PD_DIS**	**0: Enable pull-down resistor (automatically disabled in dual-phase mode)** 1: No pull-down resistor in disabled mode
	4:3		**Reserved**	
	2:0	R/W	**BCORE2_FB**	BUCKCORE2 feedback signal is created out of: xx1: VBUCKCORE2 x1x: CORE_SWS 1xx: PERI_SWS Each switch connected to the output of the buck may be selected; setting 0b000 is invalid

Table 170: BCORE1_CONF

Register Address	Bit	Type	Label	Description
0x9E BCORE1_CONF	7:6	R/W	**BCORE1_MODE**	00: Sleep/Synchronous mode controlled via voltage A and B registers 01: BUCKCORE1 always operates in Sleep mode 10: BUCKCORE1 always operates in Synchronous mode **11: BUCKCORE1 operates in Automatic mode**
	5	R/W	**BCORE1_PD_DIS**	**0: Enable pull-down resistor** 1: No pull-down resistor in disabled mode

Register Address	Bit	Type	Label	Description
	4:3		**Reserved**	
	2:0	R/W	**BCORE1_FB**	BUCKCORE feedback signal is created out of: 000: BCORE_MERGE= 0: VBUCKCORE1 BCORE_MERGE= 1: Differential remote sensing via VBUCKCORE1 – VBUCKCORE2 and output capacitor voltage sense via port CORE_SWS or GP_FB_2 xx1: VBUCKCORE1 x1x: CORE_SWS 1xx: PERI_SWS Each switch connected to the output of the buck may be selected; setting 0b000 disables sense voltage mixer for BUCKCORE

Table 171: BPRO_CONF

Register Address	Bit	Type	Label	Description
0x9F BPRO_CONF	7:6	R/W	**BPRO_MODE**	00: Sleep/Synchronous mode controlled via voltage A and B registers 10: BUCKPRO always operates in Sleep mode 10: BUCKPRO always operates in Synchronous **11: BUCKPRO operates in Automatic mode**
	5	R/W	**BPRO_PD_DIS**	**0: Enable pull-down resistor** 1: No pull-down resistor in disabled mode
	4	R/W	**BPRO_VTT_EN**	**0: Buck voltage mode** 1: VTT mode, buck target voltage tracks 50% of VDDQ sense port (requires BPRO_VTTR_EN to be asserted as well)
	3	R/W	**BPRO_VTTR_EN**	**0: VTTR port is assigned to E_CMP1V2, port VDDQ provides status of E_GPI2** 1: VTTR port provides 50% of VDDQ voltage
	2:0	R/W	**BPRO_FB**	BUCKPRO feedback signal is created out of: xx1: VBUCKPRO x1x: CORE_SWS 1xx: PERI_SWS Each switch connected to the output of the buck may be selected; setting 0b000 is invalid

Table 172: BIO_CONF

Register Address	Bit	Type	Label	Description
0xA0 BIO_CONF	7:6	R/W	**BIO_MODE**	00: Sleep/Synchronous mode controlled via voltage A and B registers 10: BUCKIO always operates in Sleep mode 10: BUCKIO always operates in Synchronous **11: BUCKIO operates in Automatic mode**
	5	R/W	**BIO_PD_DIS**	**0: Enable pull-down resistor** 1: No pull-down resistor in disabled mode
	4:3		**Reserved**	
	2:0	R/W	**BIO_FB**	BUCKIO feedback signal is created out of: xx1: VBUCKBIO x1x: CORE_SWS 1xx: PERI_SWS Each switch connected to the output of the buck may be selected; setting 0b000 is invalid

Table 173: BMEM_CONF

Register Address	Bit	Type	Label	Description
0xA1 BMEM_CONF	7:6	R/W	**BMEM_ MODE**	00: Sleep/Synchronous mode controlled via voltage A and B registers 01: BUCKMEM always operates in Sleep mode 10: BUCKMEM always operates in Synchronous mode **11: BUCKMEM operates in Automatic mode**
	5	R/W	**BMEM_PD_DIS**	**0: Enable pull-down resistor** 1: No pull-down resistor in disabled mode
	4:3		**Reserved**	
	2:0	R/W	**BMEM_FB**	BUCKMEM feedback signal is created out of: xx1: VBUCKMEM x1x: CORE_SWS 1xx: PERI_SWS Each switch connected to the output of the buck may be selected; setting 0b000 is invalid

Table 174: BPERI_CONF

Register Address	Bit	Type	Label	Description
0xA2 BPERI_CONF	7:6	R/W	**BPERI_ MODE**	00: Sleep/Synchronous mode controlled via voltage A and B registers 01: BUCKPERI always operates in Sleep mode 10: BUCKPERI always operates in Synchronous mode **11: BUCKPERI operates in Automatic mode**

Register Address	Bit	Type	Label	Description
	5	R/W	**BPERI_PD_DIS**	**0: Enable pull-down resistor** 1: No pull-down resistor in disabled mode
	4:3		**Reserved**	
	2:0	R/W	**BPERI_FB**	BUCKPERI feedback signal is created out of: xx1: VBUCKPERI x1x: CORE_SWS 1xx: PERI_SWS Each switch connected to the output of the buck may be selected; setting 0b0000 is invalid

Table 175: VBCORE2_A

<table>
<tr><th>Register Address</th><th>Bit</th><th>Type</th><th>Label</th><th colspan="2">Description</th></tr>
<tr><td rowspan="3">0xA3
VBCORE2_A</td><td>7</td><td>R/W</td><td>BCORE2_SL_A</td><td colspan="2">0: Configures BUCKCORE2 to Synchronous mode, when selecting A voltage settings
1: Configures BUCKCORE2 to Sleep mode, when selecting A voltage settings</td></tr>
<tr><td rowspan="2">6:0</td><td rowspan="2">R/W</td><td rowspan="2">VBCORE2_A</td><td colspan="2">0000000: 0.30 V
0000001: 0.31 V
0000010: 0.32 V
0000011: 0.33 V
0000100: 0.34 V
0000101: 0.35 V
…
0100101: 0.67 V
0100110: 0.68 V
0100111: 0.69 V</td></tr>
<tr><td>0101000: 0.70 V
0101001: 0.71 V
…
1010000: 1.10 V
…
1110011: 1.45 V
1110100: 1.46 V
1110101: 1.47 V
1110110: 1.48 V
1110111: 1.49 V
1111000: 1.50 V
1111001: 1.51 V
1111010: 1.52 V
1111011: 1.53 V
1111100: 1.54 V
1111101: 1.55 V
1111110: 1.56 V
1111111: 1.57 V</td><td>PWM mode voltage range</td></tr>
</table>

Table 176: VBCORE1_A

Register Address	Bit	Type	Label	Description
0xA4 VBCORE1_A	7	R/W	**BCORE1_SL_A**	**0: Configures BUCKCORE1 to Synchronous mode, when selecting A voltage settings** 1: Configures BUCKCORE1 to Sleep mode, when selecting A voltage settings

<table>
<tr><th>Register Address</th><th>Bit</th><th>Type</th><th>Label</th><th colspan="2">Description</th></tr>
<tr><td rowspan="2"></td><td rowspan="2">6:0</td><td rowspan="2">R/W</td><td rowspan="2">VBCORE1_A</td><td colspan="2">0000000: 0.30 V
0000001: 0.31 V
0000010: 0.32 V
0000011: 0.33 V
0000100: 0.34 V
0000101: 0.35 V
…
0100101: 0.67 V
0100110: 0.68 V
0100111: 0.69 V</td></tr>
<tr><td>0101000: 0.70 V
0101001: 0.71 V
…
1010000: 1.10 V
…
1110011: 1.45 V
1110100: 1.46 V
1110101: 1.47 V
1110110: 1.48 V
1110111: 1.49 V
1111000: 1.50 V
1111001: 1.51 V
1111010: 1.52 V
1111011: 1.53 V
1111100: 1.54 V
1111101: 1.55 V
1111110: 1.56 V
1111111: 1.57 V</td><td>PWM mode voltage range</td></tr>
</table>

Table 177: VBPRO_A

Register Address	Bit	Type	Label	Description
0xA5 VBPRO_A	7	R/W	**BPRO_SL_A**	**0: Configures BUCKPRO to Synchronous mode, when selecting A voltage settings** 1: Configures BUCKPRO to Sleep mode, when selecting A voltage settings
	6:0	R/W	**VBPRO_A**	0000000: 0.53 V 0000001: 0.54 V 0000010: 0.55 V 0000011: 0.56 V 0000100: 0.57 V 0000101: 0.58 V … 0010000: 0.69 V

Register Address	Bit	Type	Label	Description	
				0010001: 0.70 V 0010010: 0.71 V 0010011: 0.72 V 0010100: 0.73 V 0010101: 0.74 V 0010110: 0.75 V … **1000011: 1.20 V** … 1110011: 1.68 V 1110100: 1.69 V 1110101: 1.70 V 1110110: 1.71 V 1110111: 1.72 V 1111000: 1.73 V 1111001: 1.74 V 1111010: 1.75 V 1111011: 1.76 V 1111100: 1.77 V 1111101: 1.78 V 1111110: 1.79 V 1111111: 1.80 V	PWM mode voltage range

Table 178: VBMEM_A

Register Address	Bit	Type	Label	Description
0xA6 VBMEM_A	7	R/W	**BMEM_SL_A**	**0: Configures BUCKMEM to Synchronous mode, when selecting A voltage settings** 1: Configures BUCKMEM to Sleep mode, when selecting A voltage settings
	6:0	R/W	**VBMEM_A**	0000000: 0.80 V 0000001: 0.82 V 0000010: 0.84 V … **0010100: 1.20 V** … 0111100: 2.00 V 0111101: 2.02 V 0111110: 2.04 V 0111111: 2.06 V … 1111111: 3.34 V

Table 179: VBIO_A

Register Address	Bit	Type	Label	Description
0xA7 VBIO_A	7	R/W		**0: Configures BUCKIO to Synchronous mode, when selecting A voltage settings** 1: Configures BUCKIO to Sleep mode, when selecting A voltage settings

Register Address	Bit	Type	Label	Description
	6:0	R/W	**VBIO_A**	0000000: 0.80 V 0000001: 0.82 V 0000010: 0.84 V … **0010100: 1.20 V** … 0111100: 2.00 V 0111101: 2.02 V 0111110: 2.04 V 0111111: 2.06 V … 1111111: 3.34 V

Table 180: VBPERI_A

Register Address	Bit	Type	Label	Description
0xA8 VBPERI_A	7	R/W	**BPERI_SL_A**	**0: Configures BUCKPERI to Synchronous mode, when selecting A voltage settings** 1: Configures BUCKPERI to Sleep mode, when selecting A voltage settings
	6:0	R/W	**VBPERI_A**	0000000: 0.80 V 0000001: 0.82 V 0000010: 0.84 V … **0110010: 1.80 V** … 0111100: 2.00 V 0111101: 2.02 V 0111110: 2.04 V 0111111: 2.06 V … 1111111: 3.34 V

Table 181: VLDO1_A

Register Address	Bit	Type	Label	Description
0xA9 VLDO1_A	7	R/W	**LDO1_SL_A**	**0: Configures LDO to normal mode, when selecting A voltage settings** 1: Configures LDO to Sleep mode, when selecting A voltage settings
	6	R/W	**Reserved**	

Register Address	Bit	Type	Label	Description
	5:0	R/W	**VLDO1_A**	000000: 0.60 V 000001: 0.62 V 000010: 0.64 V 000011: 0.66 V 000100: 0.68 V 000101: 0.70 V 000110: 0.72 V 000111: 0.74 V 001000: 0.76 V 001001: 0.78 V 001010: 0.80 V 001011: 0.82 V 001100: 0.82 V 001101: 0.86 V 001110: 0.88 V 001111: 0.90 V 010000: 0.92 V 010001: 0.94 V 010010: 0.96 V 010011: 0.98 V 010100: 1.00 V 010101: 1.02 V 010110: 1.04 V 010111: 1.06 V 011000: 1.08 V 011001: 1.10 V 011010: 1.12 V 011011: 1.14 V 011100: 1.16 V 011101: 1.18 V **011110: 1.20 V** 011111: 1.22 V 100000: 1.24 V 100001: 1.26 V … 111000: 1.72 V 111001: 1.74 V 111010: 1.76 V 111011: 1.78 V 111100: 1.80 V 111101: 1.82 V 111110: 1.84 V 111111: 1.86 V

Table 182: VLDO2_A

Register Address	Bit	Type	Label	Description
0xAA VLDO2_A	7	R/W	**LDO2_SL_A**	**0: Configures LDO to normal mode, when selecting A voltage settings** 1: Configures LDO to Sleep mode, when selecting A voltage settings
	6	R/W	**Reserved**	

Register Address	Bit	Type	Label	Description
	5:0	R/W	**VLDO2_A**	000000: 0.60 V 000001: 0.62 V 000010: 0.64 V 000011: 0.66 V 000100: 0.68 V 000101: 0.70 V 000110: 0.72 V 000111: 0.74 V 001000: 0.76 V 001001: 0.78 V 001010: 0.80 V 001011: 0.82 V 001100: 0.82 V 001101: 0.86 V 001110: 0.88 V 001111: 0.90 V 010000: 0.92 V 010001: 0.94 V 010010: 0.96 V 010011: 0.98 V 010100: 1.00 V 010101: 1.02 V 010110: 1.04 V 010111: 1.06 V 011000: 1.08 V 011001: 1.10 V 011010: 1.12 V 011011: 1.14 V 011100: 1.16 V 011101: 1.18 V **011110: 1.20 V** 011111: 1.22 V 100000: 1.24 V 100001: 1.26 V … 111000: 1.72 V 111001: 1.74 V 111010: 1.76 V 111011: 1.78 V 111100: 1.80 V 111101: 1.82 V 111110: 1.84 V 111111: 1.86 V

Table 183: VLDO3_A

Register Address	Bit	Type	Label	Description
0xAB VLDO3_A	7	R/W	**LDO3_SL_A**	**0: Configures LDO to normal mode, when selecting A voltage settings** 1: Configures LDO to Sleep mode, when selecting A voltage settings
	6:0	R/W	**VLDO3_A**	0000000: 0.90 V 0000001: 0.92 V 0000010: 0.94 V 0000011: 0.96 V 0000100: 0.98 V 0000101: 1.00 V 0000110: 1.02 V 0000111: 1.04 V 0001000: 1.06 V 0001001: 1.08 V 0001010: 1.10 V 0001011: 1.12 V 0001100: 1.14 V 0001101: 1.16 V 0001110: 1.18 V **0001111: 1.20 V** 0010000: 1.22 V 0010001: 1.24 V 0010010: 1.26 V 0010011: 1.28 V 0010100: 1.30 V 0010101: 1.32 V ... 1110000: 3.14 V 1110001: 3.16 V 1110010: 3.18 V 1110011: 3.20 V 1110100: 3.22 V 1110101: 3.24 V 1110110: 3.26 V 1110111: 3.28 V 1111000: 3.30 V 1111001: 3.32 V 1111010: 3.34 V 1111011: 3.36 V 1111100: 3.38 V 1111101: 3.40 V 1111110: 3.42 V 1111111: 3.44 V

Table 184: VLDO4_A

Register Address	Bit	Type	Label	Description
0xAC VLDO4_A	7	R/W	**LDO4_SL_A**	**0: Configures LDO to normal mode, when selecting A voltage settings** 1: Configures LDO to Sleep mode, when selecting A voltage settings
	6:0	R/W	**VLDO4_A**	0000000: 0.90 V 0000001: 0.92 V 0000010: 0.94 V 0000011: 0.96 V 0000100: 0.98 V 0000101: 1.00 V 0000110: 1.02 V 0000111: 1.04 V 0001000: 1.06 V 0001001: 1.08 V 0001010: 1.10 V 0001011: 1.12 V 0001100: 1.14 V 0001101: 1.16 V 0001110: 1.18 V 0001111: 1.20 V 0010000: 1.22 V 0010001: 1.24 V 0010010: 1.26 V 0010011: 1.28 V 0010100: 1.30 V 0010101: 1.32 V ... 1110000: 3.14 V 1110001: 3.16 V 1110010: 3.18 V 1110011: 3.20 V 1110100: 3.22 V 1110101: 3.24 V 1110110: 3.26 V 1110111: 3.28 V **1111000: 3.30 V** 1111001: 3.32 V 1111010: 3.34 V 1111011: 3.36 V 1111100: 3.38 V 1111101: 3.40 V 1111110: 3.42 V 1111111: 3.44 V

Table 185: VLDO5_A

Register Address	Bit	Type	Label	Description
0xAD VLDO5_A	7	R/W	**LDO5_SL_A**	**0: Configures LDO to normal mode, when selecting A voltage settings** 1: Configures LDO to Sleep mode, when selecting A voltage settings
	6	R/W	**Reserved**	
	5:0	R/W	**VLDO5_A**	000000: 0.90 V 000001: 0.90 V 000010: 0.90 V 000011: 0.95 V 000100: 1.00 V 000101: 1.05 V 000110: 1.10 V 000111: 1.15 V 001000: 1.20 V 001001: 1.25 V 001010: 1.30 V 001011: 1.35 V 001100: 1.40 V 001101: 1.45 V 001110: 1.50 V 001111: 1.55 V 010000: 1.60 V 010001: 1.65 V 010010: 1.70 V 010011: 1.75 V 010100: 1.80 V 010101: 1.85 V ... 100010: 2.50 V 100011: 2.55 V 100100: 2.60 V 100101: 2.65 V 100110: 2.70 V 100111: 2.75 V 101000: 2.80 V 101001: 2.85 V 101010: 2.90 V 101011: 2.95 V 101100: 3.00 V 101101: 3.05 V 101110: 3.10 V 101111: 3.15 V 110000: 3.20 V 110001: 3.25 V **110010: 3.30 V** 110011: 3.35 V 110100: 3.40 V 110101: 3.45 V 110110: 3.50 V 110111: 3.55 V 111000: 3.60 V >111000: 3.60 V

Table 186: VLDO6_A

Register Address	Bit	Type	Label	Description
0xAE VLDO6_A	7	R/W	**LDO6_SL_A**	**0: Configures LDO to normal mode, when selecting A voltage settings** 1: Configures LDO to Sleep mode, when selecting A voltage settings
	6	R/W	**Reserved**	
	5:0	R/W	**VLDO6_A**	000000: 0.90 V 000001: 0.90 V 000010: 0.90 V 000011: 0.95 V 000100: 1.00 V 000101: 1.05 V 000110: 1.10 V 000111: 1.15 V 001000: 1.20 V 001001: 1.25 V 001010: 1.30 V 001011: 1.35 V 001100: 1.40 V 001101: 1.45 V 001110: 1.50 V 001111: 1.55 V 010000: 1.60 V 010001: 1.65 V 010010: 1.70 V 010011: 1.75 V **010100: 1.80 V** 010101: 1.85 V ... 100010: 2.50 V 100011: 2.55 V 100100: 2.60 V 100101: 2.65 V 100110: 2.70 V 100111: 2.75 V 101000: 2.80 V 101001: 2.85 V 101010: 2.90 V 101011: 2.95 V 101100: 3.00 V 101101: 3.05 V 101110: 3.10 V 101111: 3.15 V 110000: 3.20 V 110001: 3.25 V 110010: 3.30 V 110011: 3.35 V 110100: 3.40 V 110101: 3.45 V 110110: 3.50 V 110111: 3.55 V 111000: 3.60 V >111000: 3.60 V

Table 187: VLDO7_A

Register Address	Bit	Type	Label	Description
0xAF VLDO7_A	7	R/W	**LDO7_SL_A**	**0: Configures LDO to normal mode, when selecting A voltage settings** 1: Configures LDO to Sleep mode, when selecting A voltage settings
	6	R/W	**Reserved**	
	5:0	R/W	**VLDO7_A**	000000: 0.90 V 000001: 0.90 V 000010: 0.90 V 000011: 0.95 V 000100: 1.00 V 000101: 1.05 V 000110: 1.10 V 000111: 1.15 V 001000: 1.20 V 001001: 1.25 V 001010: 1.30 V 001011: 1.35 V 001100: 1.40 V 001101: 1.45 V 001110: 1.50 V 001111: 1.55 V 010000: 1.60 V 010001: 1.65 V 010010: 1.70 V 010011: 1.75 V 010100: 1.80 V 010101: 1.85 V ... 100010: 2.50 V 100011: 2.55 V 100100: 2.60 V 100101: 2.65 V 100110: 2.70 V 100111: 2.75 V **101000: 2.80 V** 101001: 2.85 V 101010: 2.90 V 101011: 2.95 V 101100: 3.00 V 101101: 3.05 V 101110: 3.10 V 101111: 3.15 V 110000: 3.20 V 110001: 3.25 V 110010: 3.30 V 110011: 3.35 V 110100: 3.40 V 110101: 3.45 V 110110: 3.50 V 110111: 3.55 V 111000: 3.60 V >111000: 3.60 V

Table 188: VLDO8_A

Register Address	Bit	Type	Label	Description
0xB0 VLDO8_A	7	R/W	**LDO8_SL_A**	**0: Configures LDO to normal mode, when selecting A voltage settings** 1: Configures LDO to Sleep mode, when selecting A voltage settings
	6	R/W	**Reserved**	
	5:0	R/W	**VLDO8_A**	000000: 0.90 V 000001: 0.90 V 000010: 0.90 V 000011: 0.95 V 000100: 1.00 V 000101: 1.05 V 000110: 1.10 V 000111: 1.15 V 001000: 1.20 V 001001: 1.25 V 001010: 1.30 V 001011: 1.35 V 001100: 1.40 V 001101: 1.45 V 001110: 1.50 V 001111: 1.55 V 010000: 1.60 V 010001: 1.65 V 010010: 1.70 V 010011: 1.75 V 010100: 1.80 V 010101: 1.85 V ... 100010: 2.50 V 100011: 2.55 V 100100: 2.60 V 100101: 2.65 V 100110: 2.70 V 100111: 2.75 V **101000: 2.80 V** 101001: 2.85 V 101010: 2.90 V 101011: 2.95 V 101100: 3.00 V 101101: 3.05 V 101110: 3.10 V 101111: 3.15 V 110000: 3.20 V 110001: 3.25 V 110010: 3.30 V 110011: 3.35 V 110100: 3.40 V 110101: 3.45 V 110110: 3.50 V 110111: 3.55 V 111000: 3.60 V >111000: 3.60 V

Table 189: VLDO9_A

Register Address	Bit	Type	Label	Description
0xB1 VLDO9_A	7	R/W	**LDO9_SL_A**	**0: Configures LDO to normal mode, when selecting A voltage settings** 1: Configures LDO to Sleep mode, when selecting A voltage settings
	6	R/W	**Reserved**	
	5:0	R/W	**VLDO9_A**	000000: not used 000001: 0.95 V 000010: 0.95 V 000011: 0.95 V 000100: 1.00 V 000101: 1.05 V 000110: 1.10 V 000111: 1.15 V 001000: 1.20 V 001001: 1.25 V 001010: 1.30 V 001011: 1.35 V 001100: 1.40 V 001101: 1.45 V 001110: 1.50 V 001111: 1.55 V 010000: 1.60 V 010001: 1.65 V 010010: 1.70 V 010011: 1.75 V 010100: 1.80 V 010101: 1.85 V ... **100010: 2.50 V** 100011: 2.55 V 100100: 2.60 V 100101: 2.65 V 100110: 2.70 V 100111: 2.75 V 101000: 2.80 V 101001: 2.85 V 101010: 2.90 V 101011: 2.95 V 101100: 3.00 V 101101: 3.05 V 101110: 3.10 V 101111: 3.15 V 110000: 3.20 V 110001: 3.25 V 110010: 3.30 V 110011: 3.35 V 110100: 3.40 V 110101: 3.45 V 110110: 3.50 V 110111: 3.55 V 111000: 3.60 V >111000: 3.60 V

Table 190: VLDO10_A

Register Address	Bit	Type	Label	Description
0xB2 VLDO10_A	7	R/W	**LDO10_SL_A**	**0: Configures LDO to normal mode, when selecting A voltage settings** 1: Configures LDO to Sleep mode, when selecting A voltage settings
	6	R/W	**Reserved**	
	5:0	R/W	**VLDO10_A**	000000: 0.90 V 000001: 0.90 V 000010: 0.90 V 000011: 0.95 V 000100: 1.00 V 000101: 1.05 V 000110: 1.10 V 000111: 1.15 V 001000: 1.20 V 001001: 1.25 V 001010: 1.30 V 001011: 1.35 V 001100: 1.40 V 001101: 1.45 V 001110: 1.50 V 001111: 1.55 V 010000: 1.60 V 010001: 1.65 V 010010: 1.70 V 010011: 1.75 V 010100: 1.80 V 010101: 1.85 V ... 100010: 2.50 V 100011: 2.55 V 100100: 2.60 V 100101: 2.65 V 100110: 2.70 V 100111: 2.75 V 101000: 2.80 V 101001: 2.85 V 101010: 2.90 V 101011: 2.95 V 101100: 3.00 V 101101: 3.05 V 101110: 3.10 V 101111: 3.15 V 110000: 3.20 V 110001: 3.25 V **110010: 3.30 V** 110011: 3.35 V 110100: 3.40 V 110101: 3.45 V 110110: 3.50 V 110111: 3.55 V 111000: 3.60 V >111000: 3.60 V

Table 191: VLDO11_A

Register Address	Bit	Type	Label	Description
0xB3 VLDO11_A	7:4	R/W	**LDO11_SL_A**	**0: Configures LDO to normal mode, when selecting A voltage settings** 1: Configures LDO to Sleep mode, when selecting A voltage settings
	6	R/W	**Reserved**	
	5:0	R/W	**VLDO11_A**	000000: 0.90 V 000001: 0.90 V 000010: 0.90 V 000011: 0.95 V 000100: 1.00 V 000101: 1.05 V 000110: 1.10 V 000111: 1.15 V 001000: 1.20 V 001001: 1.25 V 001010: 1.30 V 001011: 1.35 V 001100: 1.40 V 001101: 1.45 V 001110: 1.50 V 001111: 1.55 V 010000: 1.60 V 010001: 1.65 V 010010: 1.70 V 010011: 1.75 V 010100: 1.80 V 010101: 1.85 V ... 100010: 2.50 V 100011: 2.55 V 100100: 2.60 V 100101: 2.65 V 100110: 2.70 V 100111: 2.75 V 101000: 2.80 V 101001: 2.85 V 101010: 2.90 V 101011: 2.95 V 101100: 3.00 V 101101: 3.05 V 101110: 3.10 V 101111: 3.15 V 110000: 3.20 V 110001: 3.25 V **110010: 3.30 V** 110011: 3.35 V 110100: 3.40 V 110101: 3.45 V 110110: 3.50 V 110111: 3.55 V 111000: 3.60 V >111000: 3.60 V

Table 192: VBCORE2_B

<table>
<tr><th>Register Address</th><th>Bit</th><th>Type</th><th>Label</th><th colspan="2">Description</th></tr>
<tr><td rowspan="3">0xB4
VBCORE2_B</td><td>7</td><td>R/W</td><td>BCORE2_SL_B</td><td colspan="2">0: Configures BUCKCORE2 to Synchronous mode, when selecting B voltage settings
1: Configures BUCKCORE2 to Sleep mode, when selecting B voltage settings</td></tr>
<tr><td rowspan="2">6:0</td><td rowspan="2">R/W</td><td rowspan="2">VBCORE2_B</td><td colspan="2">0000000: 0.30 V
0000001: 0.31 V
0000010: 0.32 V
0000011: 0.33 V
0000100: 0.34 V
0000101: 0.35 V
…
0100101: 0.67 V
0100110: 0.68 V
0100111: 0.69 V</td></tr>
<tr><td>0101000: 0.70 V
0101001: 0.71 V
…
0111100: 0.90 V
…
1110011: 1.45 V
1110100: 1.46 V
1110101: 1.47 V
1110110: 1.48 V
1110111: 1.49 V
1111000: 1.50 V
1111001: 1.51 V
1111010: 1.52 V
1111011: 1.53 V
1111100: 1.54 V
1111101: 1.55 V
1111110: 1.56 V
1111111: 1.57 V</td><td>PWM mode voltage range</td></tr>
</table>

Table 193: VBCORE1_B

<table>
<tr><th>Register Address</th><th>Bit</th><th>Type</th><th>Label</th><th colspan="2">Description</th></tr>
<tr><td rowspan="3">0xB5
VBCORE1_B</td><td>7</td><td>R/W</td><td>BCORE1_SL_B</td><td colspan="2">0: Configures BUCKCORE1 to Synchronous mode, when selecting B voltage settings
1: Configures BUCKCORE1 to Sleep mode, when selecting B voltage settings</td></tr>
<tr><td rowspan="2">6:0</td><td rowspan="2">R/W</td><td rowspan="2">VBCORE1_B</td><td colspan="2">0000000: 0.30 V
0000001: 0.31 V
0000010: 0.32 V
0000011: 0.33 V
0000100: 0.34 V
0000101: 0.35 V
…
0100101: 0.67 V
0100110: 0.68 V
0100111: 0.69 V</td></tr>
<tr><td>0101000: 0.70 V
0101001: 0.71 V
…
0111100: 0.90 V
…
1110011: 1.45 V
1110100: 1.46 V
1110101: 1.47 V
1110110: 1.48 V
1110111: 1.49 V
1111000: 1.50 V
1111001: 1.51 V
1111010: 1.52 V
1111011: 1.53 V
1111100: 1.54 V
1111101: 1.55 V
1111110: 1.56 V
1111111: 1.57 V</td><td>PWM mode voltage range</td></tr>
</table>

Table 194: VBPRO_B

<table>
<tr><th>Register Address</th><th>Bit</th><th>Type</th><th>Label</th><th colspan="2">Description</th></tr>
<tr><td rowspan="3">0xB6
VBPRO_B</td><td>7</td><td>R/W</td><td>BPRO_SL_B</td><td colspan="2">0: Configures BUCKPRO to Synchronous mode, when selecting B voltage settings
1: Configures BUCKPRO to Sleep mode, when selecting B voltage settings</td></tr>
<tr><td rowspan="2">6:0</td><td rowspan="2">R/W</td><td rowspan="2">VBPRO_B</td><td colspan="2">0000000: 0.53 V
0000001: 0.54 V
0000010: 0.55 V
0000011: 0.56 V
0000100: 0.57 V
0000101: 0.58 V
…
0010000: 0.69 V</td></tr>
<tr><td>0010001: 0.70 V
0010010: 0.71 V
0010011: 0.72 V
0010100: 0.73 V
0010101: 0.74 V
0010110: 0.75 V
…
1000011: 1.20 V
…
1110011: 1.68 V
1110100: 1.69 V
1110101: 1.70 V
1110110: 1.71 V
1110111: 1.72 V
1111000: 1.73 V
1111001: 1.74 V
1111010: 1.75 V
1111011: 1.76 V
1111100: 1.77 V
1111101: 1.78 V
1111110: 1.79 V
1111111: 1.80 V</td><td>PWM mode voltage range</td></tr>
</table>

Table 195: VBMEM_B

Register Address	Bit	Type	Label	Description
0xB7 VBMEM_B	7	R/W	**BMEM_SL_B**	0: Configures BUCKMEM to Synchronous mode, when selecting B voltage settings **1: Configures BUCKMEM to Sleep mode, when selecting B voltage settings**
	6:0	R/W	**VBMEM_B**	0000000: 0.80 V 0000001: 0.82 V 0000010: 0.84 V … **0010100: 1.20 V** … 0111100: 2.00 V 0111101: 2.02 V 0111110: 2.04 V 0111111: 2.06 V … 1111111: 3.34 V

Table 196: VBIO_B

Register Address	Bit	Type	Label	Description
0xB8 VBIO_B	7	R/W	**BIO_SL_B**	**0: Configures BUCKIO to Synchronous mode, when selecting B voltage settings** 1: Configures BUCKIO to Sleep mode, when selecting B voltage settings
	6:0	R/W	**VBIO_B**	0000000: 0.80 V 0000001: 0.82 V 0000010: 0.84 V … **0010100: 1.20 V** … 0111100: 2.00 V 0111101: 2.02 V 0111110: 2.04 V 0111111: 2.06 V … 1111111: 3.34 V

Table 197: VBPERI_B

Register Address	Bit	Type	Label	Description
0xB9 VBPERI_B	7	R/W	**BPERI_SL_B**	0: Configures BUCKPERI to Synchronous mode, when selecting A voltage settings **1: Configures BUCKPERI to Sleep mode, when selecting B voltage settings**
	6:0	R/W	**VBPERI_B**	0000000: 0.80 V 0000001: 0.82 V 0000010: 0.84 V … **0110010: 1.80 V** … 0111100: 2.00 V 0111101: 2.02 V 0111110: 2.04 V 0111111: 2.06 V … 1111111: 3.34 V

Table 198: VLDO1_B

Register Address	Bit	Type	Label	Description
0xBA VLDO1_B	7	R/W	**LDO1_SL_B**	**0: Configures LDO to normal mode, when selecting B voltage settings** 1: Configures LDO to Sleep mode, when selecting B voltage settings
	6	R/W	**Reserved**	
	5:0	R/W	**VLDO1_B**	000000: 0.60 V 000001: 0.62 V 000010: 0.64 V 000011: 0.66 V 000100: 0.68 V 000101: 0.70 V 000110: 0.72 V 000111: 0.74 V 001000: 0.76 V 001001: 0.78 V 001010: 0.80 V 001011: 0.82 V 001100: 0.82 V 001101: 0.86 V 001110: 0.88 V 001111: 0.90 V 010000: 0.92 V 010001: 0.94 V 010010: 0.96 V 010011: 0.98 V 010100: 1.00 V 010101: 1.02 V 010110: 1.04 V 010111: 1.06 V 011000: 1.08 V 011001: 1.10 V 011010: 1.12 V 011011: 1.14 V 011100: 1.16 V 011101: 1.18 V **011110: 1.20 V** 011111: 1.22 V 100000: 1.24 V 100001: 1.26 V … 111000: 1.72 V 111001: 1.74 V 111010: 1.76 V 111011: 1.78 V 111100: 1.80 V 111101: 1.82 V 111110: 1.84 V 111111: 1.86 V

Table 199: VLDO2_B

Register Address	Bit	Type	Label	Description
0xBB VLDO2_B	7	R/W	**LDO2_SL_B**	**0: Configures LDO to normal mode, when selecting B voltage settings** 1: Configures LDO to Sleep mode, when selecting B voltage settings
	6	R/W	**Reserved**	
	5:0	R/W	**VLDO2_B**	000000: 0.60 V 000001: 0.62 V 000010: 0.64 V 000011: 0.66 V 000100: 0.68 V 000101: 0.70 V 000110: 0.72 V 000111: 0.74 V 001000: 0.76 V 001001: 0.78 V 001010: 0.80 V 001011: 0.82 V 001100: 0.82 V 001101: 0.86 V 001110: 0.88 V 001111: 0.90 V 010000: 0.92 V 010001: 0.94 V 010010: 0.96 V 010011: 0.98 V 010100: 1.00 V 010101: 1.02 V 010110: 1.04 V 010111: 1.06 V 011000: 1.08 V 011001: 1.10 V 011010: 1.12 V 011011: 1.14 V 011100: 1.16 V 011101: 1.18 V **011110: 1.20 V** 011111: 1.22 V 100000: 1.24 V 100001: 1.26 V … 111000: 1.72 V 111001: 1.74 V 111010: 1.76 V 111011: 1.78 V 111100: 1.80 V 111101: 1.82 V 111110: 1.84 V 111111: 1.86 V

Table 200: VLDO3_B

Register Address	Bit	Type	Label	Description
0xBC VLDO3_B	7	R/W	**LDO3_SL_B**	**0: Configures LDO to normal mode, when selecting B voltage settings** 1: Configures LDO to Sleep mode, when selecting B voltage settings
	6:0	R/W	**VLDO3_B**	0000000: 0.90 V 0000001: 0.92 V 0000010: 0.94 V 0000011: 0.96 V 0000100: 0.98 V 0000101: 1.00 V 0000110: 1.02 V 0000111: 1.04 V 0001000: 1.06 V 0001001: 1.08 V 0001010: 1.10 V 0001011: 1.12 V 0001100: 1.14 V 0001101: 1.16 V 0001110: 1.18 V **0001111: 1.20 V** 0010000: 1.22 V 0010001: 1.24 V 0010010: 1.26 V 0010011: 1.28 V 0010100: 1.30 V 0010101: 1.32 V ... 1110000: 3.14 V 1110001: 3.16 V 1110010: 3.18 V 1110011: 3.20 V 1110100: 3.22 V 1110101: 3.24 V 1110110: 3.26 V 1110111: 3.28 V 1111000: 3.30 V 1111001: 3.32 V 1111010: 3.34 V 1111011: 3.36 V 1111100: 3.38 V 1111101: 3.40 V 1111110: 3.42 V 1111111: 3.44 V

Table 201: VLDO4_B

Register Address	Bit	Type	Label	Description
0xBD VLDO4_B	7	R/W	**LDO4_SL_B**	**0: Configures LDO to normal mode, when selecting B voltage settings** 1: Configures LDO to Sleep mode, when selecting B voltage settings
	6:0	R/W	**VLDO4_B**	0000000: 0.90 V 0000001: 0.92 V 0000010: 0.94 V 0000011: 0.96 V 0000100: 0.98 V 0000101: 1.00 V 0000110: 1.02 V 0000111: 1.04 V 0001000: 1.06 V 0001001: 1.08 V 0001010: 1.10 V 0001011: 1.12 V 0001100: 1.14 V 0001101: 1.16 V 0001110: 1.18 V 0001111: 1.20 V 0010000: 1.22 V 0010001: 1.24 V 0010010: 1.26 V 0010011: 1.28 V 0010100: 1.30 V 0010101: 1.32 V ... 1110000: 3.14 V 1110001: 3.16 V 1110010: 3.18 V 1110011: 3.20 V 1110100: 3.22 V 1110101: 3.24 V 1110110: 3.26 V 1110111: 3.28 V **1111000: 3.30 V** 1111001: 3.32 V 1111010: 3.34 V 1111011: 3.36 V 1111100: 3.38 V 1111101: 3.40 V 1111110: 3.42 V 1111111: 3.44 V

Table 202: VLDO5_B

Register Address	Bit	Type	Label	Description
0xBE VLDO5_B	7	R/W	**LDO5_SL_B**	**0: Configures LDO to normal mode, when selecting B voltage settings** 1: Configures LDO to Sleep mode, when selecting B voltage settings
	6	R/W	**Reserved**	
	5:0	R/W	**VLDO5_B**	000000: 0.90 V 000001: 0.90 V 000010: 0.90 V 000011: 0.95 V 000100: 1.00 V 000101: 1.05 V 000110: 1.10 V 000111: 1.15 V 001000: 1.20 V 001001: 1.25 V 001010: 1.30 V 001011: 1.35 V 001100: 1.40 V 001101: 1.45 V 001110: 1.50 V 001111: 1.55 V 010000: 1.60 V 010001: 1.65 V 010010: 1.70 V 010011: 1.75 V 010100: 1.80 V 010101: 1.85 V ... 100010: 2.50 V 100011: 2.55 V 100100: 2.60 V 100101: 2.65 V 100110: 2.70 V 100111: 2.75 V 101000: 2.80 V 101001: 2.85 V 101010: 2.90 V 101011: 2.95 V 101100: 3.00 V 101101: 3.05 V 101110: 3.10 V 101111: 3.15 V 110000: 3.20 V 110001: 3.25 V **110010: 3.30 V** 110011: 3.35 V 110100: 3.40 V 110101: 3.45 V 110110: 3.50 V 110111: 3.55 V 111000: 3.60 V >111000: 3.60 V

Table 203: VLDO6_B

Register Address	Bit	Type	Label	Description
0xBF VLDO6_B	7	R/W	**LDO6_SL_B**	**0: Configures LDO to normal mode, when selecting B voltage settings** 1: Configures LDO to Sleep mode, when selecting B voltage settings
	6	R/W	**Reserved**	
	5:0	R/W	**VLDO6_B**	000000: 0.90 V 000001: 0.90 V 000010: 0.90 V 000011: 0.95 V 000100: 1.00 V 000101: 1.05 V 000110: 1.10 V 000111: 1.15 V 001000: 1.20 V 001001: 1.25 V 001010: 1.30 V 001011: 1.35 V 001100: 1.40 V 001101: 1.45 V 001110: 1.50 V 001111: 1.55 V 010000: 1.60 V 010001: 1.65 V 010010: 1.70 V 010011: 1.75 V **010100: 1.80 V** 010101: 1.85 V ... 100010: 2.50 V 100011: 2.55 V 100100: 2.60 V 100101: 2.65 V 100110: 2.70 V 100111: 2.75 V 101000: 2.80 V 101001: 2.85 V 101010: 2.90 V 101011: 2.95 V 101100: 3.00 V 101101: 3.05 V 101110: 3.10 V 101111: 3.15 V 110000: 3.20 V 110001: 3.25 V 110010: 3.30 V 110011: 3.35 V 110100: 3.40 V 110101: 3.45 V 110110: 3.50 V 110111: 3.55 V 111000: 3.60 V >111000: 3.60 V

Table 204: VLDO7_B

Register Address	Bit	Type	Label	Description
0xC0 VLDO7_B	7	R/W	**LDO7_SL_B**	**0: Configures LDO to normal mode, when selecting B voltage settings** 1: Configures LDO to Sleep mode, when selecting B voltage settings
	6	R/W	**Reserved**	
	5:0	R/W	**VLDO7_B**	000000: 0.90 V 000001: 0.90 V 000010: 0.90 V 000011: 0.95 V 000100: 1.00 V 000101: 1.05 V 000110: 1.10 V 000111: 1.15 V 001000: 1.20 V 001001: 1.25 V 001010: 1.30 V 001011: 1.35 V 001100: 1.40 V 001101: 1.45 V 001110: 1.50 V 001111: 1.55 V 010000: 1.60 V 010001: 1.65 V 010010: 1.70 V 010011: 1.75 V 010100: 1.80 V 010101: 1.85 V ... 100010: 2.50 V 100011: 2.55 V 100100: 2.60 V 100101: 2.65 V 100110: 2.70 V 100111: 2.75 V **101000: 2.80 V** 101001: 2.85 V 101010: 2.90 V 101011: 2.95 V 101100: 3.00 V 101101: 3.05 V 101110: 3.10 V 101111: 3.15 V 110000: 3.20 V 110001: 3.25 V 110010: 3.30 V 110011: 3.35 V 110100: 3.40 V 110101: 3.45 V 110110: 3.50 V 110111: 3.55 V 111000: 3.60 V >111000: 3.60 V

Table 205: VLDO8_B

Register Address	Bit	Type	Label	Description
0xC1 VLDO8_B	7	R/W	**LDO8_SL_B**	**0: Configures LDO to normal mode, when selecting B voltage settings** 1: Configures LDO to Sleep mode, when selecting B voltage settings
	6	R/W	**Reserved**	
	5:0	R/W	**VLDO8_B**	000000: 0.90 V 000001: 0.90 V 000010: 0.90 V 000011: 0.95 V 000100: 1.00 V 000101: 1.05 V 000110: 1.10 V 000111: 1.15 V 001000: 1.20 V 001001: 1.25 V 001010: 1.30 V 001011: 1.35 V 001100: 1.40 V 001101: 1.45 V 001110: 1.50 V 001111: 1.55 V 010000: 1.60 V 010001: 1.65 V 010010: 1.70 V 010011: 1.75 V 010100: 1.80 V 010101: 1.85 V ... 100010: 2.50 V 100011: 2.55 V 100100: 2.60 V 100101: 2.65 V 100110: 2.70 V 100111: 2.75 V **101000: 2.80 V** 101001: 2.85 V 101010: 2.90 V 101011: 2.95 V 101100: 3.00 V 101101: 3.05 V 101110: 3.10 V 101111: 3.15 V 110000: 3.20 V 110001: 3.25 V 110010: 3.30 V 110011: 3.35 V 110100: 3.40 V 110101: 3.45 V 110110: 3.50 V 110111: 3.55 V 111000: 3.60 V >111000: 3.60 V

Table 206: VLDO9_B

Register Address	Bit	Type	Label	Description
0xC2 VLDO9_B	7	R/W	**LDO9_SL_B**	**0: Configures LDO to normal mode, when selecting B voltage settings** 1: Configures LDO to Sleep mode, when selecting B voltage settings
	6	R/W	**Reserved**	
	5:0	R/W	**VLDO9_B**	000000: 0.95 V 000001: 0.95 V 000010: 0.95 V 000011: 0.95 V 000100: 1.00 V 000101: 1.05 V 000110: 1.10 V 000111: 1.15 V 001000: 1.20 V 001001: 1.25 V 001010: 1.30 V 001011: 1.35 V 001100: 1.40 V 001101: 1.45 V 001110: 1.50 V 001111: 1.55 V 010000: 1.60 V 010001: 1.65 V 010010: 1.70 V 010011: 1.75 V 010100: 1.80 V 010101: 1.85 V ... **100010: 2.50 V** 100011: 2.55 V 100100: 2.60 V 100101: 2.65 V 100110: 2.70 V 100111: 2.75 V 101000: 2.80 V 101001: 2.85 V 101010: 2.90 V 101011: 2.95 V 101100: 3.00 V 101101: 3.05 V 101110: 3.10 V 101111: 3.15 V 110000: 3.20 V 110001: 3.25 V 110010: 3.30 V 110011: 3.35 V 110100: 3.40 V 110101: 3.45 V 110110: 3.50 V 110111: 3.55 V 111000: 3.60 V >111000: 3.60 V

Table 207: VLDO10_B

Register Address	Bit	Type	Label	Description
0xC3 VLDO10_B	7	R/W	**LDO10_SL_B**	**0: Configures LDO to normal mode, when selecting B voltage settings** 1: Configures LDO to Sleep mode, when selecting B voltage settings
	6	R/W	**Reserved**	
	5:0	R/W	**VLDO10_B**	000000: 0.90 V 000001: 0.90 V 000010: 0.90 V 000011: 0.95 V 000100: 1.00 V 000101: 1.05 V 000110: 1.10 V 000111: 1.15 V 001001: 1.25 V 001010: 1.30 V 001011: 1.35 V 001100: 1.40 V 001101: 1.45 V 001110: 1.50 V 001111: 1.55 V 010000: 1.60 V 010001: 1.65 V 010010: 1.70 V 010011: 1.75 V 010100: 1.80 V 010101: 1.85 V ... 100010: 2.50 V 100011: 2.55 V 100100: 2.60 V 100101: 2.65 V 100110: 2.70 V 100111: 2.75 V 101000: 2.80 V 101001: 2.85 V 101010: 2.90 V 101011: 2.95 V 101100: 3.00 V 101101: 3.05 V 101110: 3.10 V 101111: 3.15 V 110000: 3.20 V 110001: 3.25 V **110010: 3.30 V** 110011: 3.35 V 110100: 3.40 V 110101: 3.45 V 110110: 3.50 V 110111: 3.55 V 111000: 3.60 V >111000: 3.60 V

Table 208: VLDO11_B

Register Address	Bit	Type	Label	Description
0xC4 VLDO11_B	7:4	R/W	**LDO1_SL_B**	**0: Configures LDO to normal mode, when selecting B voltage settings** 1: Configures LDO to Sleep mode, when selecting B voltage settings
	6	R/W	**Reserved**	
	5:0	R/W	**VLDO11_B**	000000: 0.90 V 000001: 0.90 V 000010: 0.90 V 000011: 0.95 V 000100: 1.00 V 000101: 1.05 V 000110: 1.10 V 000111: 1.15 V 001001: 1.25 V 001010: 1.30 V 001011: 1.35 V 001100: 1.40 V 001101: 1.45 V 001110: 1.50 V 001111: 1.55 V 010000: 1.60 V 010001: 1.65 V 010010: 1.70 V 010011: 1.75 V 010100: 1.80 V 010101: 1.85 V ... 100010: 2.50 V 100011: 2.55 V 100100: 2.60 V 100101: 2.65 V 100110: 2.70 V 100111: 2.75 V 101000: 2.80 V 101001: 2.85 V 101010: 2.90 V 101011: 2.95 V 101100: 3.00 V 101101: 3.05 V 101110: 3.10 V 101111: 3.15 V 110000: 3.20 V 110001: 3.25 V **110010: 3.30 V** 110011: 3.35 V 110100: 3.40 V 110101: 3.45 V 110110: 3.50 V 110111: 3.55 V 111000: 3.60 V >111000: 3.60 V

A.3.3 Backup Battery Charger

Table 209: BBAT_CONT

Register Address	Bit	Type	Label	Description
0xC5 BBAT_CONT	7:4	R/W	**BCHG_ISET**	**0000: disabled** 0001: 100 µA 0010: 200 µA 0011: 300 µA 0100: 400 µA 0101: 500 µA 0110: 600 µA 0111: 700 µA 1000: 800 µA 1001: 900 µA 1010: 1 mA 1011: 2 mA 1100: 3 mA 1101: 4 mA 1110: 5 mA 1111: 6 mA
	3:0	R/W	**BCHG_VSET**	0000: disabled 0001: 1.1 V 0010: 1.2 V 0011: 1.4 V 0100: 1.6 V 0101: 1.8 V 0110: 2.0 V 0111: 2.2 V 1000: 2.4 V 1001: 2.5 V 1010: 2.6 V 1011: 2.7 V 1100: 2.8 V 1101: 2.9 V **1110: 3.0 V** 1111: 3.1 V

A.3.4 High Power GPO PWM

Table 210: GPO11_LED

Register Address	Bit	Type	Label	Description
0xC6 GPO11_LED	7	R/W	**GPO11_DIM**	**0: PWM ratio changes instantly** 1: GPO ramps between changes in PWM ratio with 32 ms per step
	6:0	R/W	**GPO11_PWM**	GPO11 LED on-time (low level at GPIO 11, period 21 kHz = 95 cycles of 0.5 µs) **0000000: off** 0000001: 1% 0000010: 2% (1 µs bursts) 0000011: 3% 0000100: 4% 0000101: 5% 0000110: 6% 0000111: 7% 0001000: 8% 0001001: 9% 0001010: 10% 0001011: 11% 0001100: 12% 0001101: 13% 0001110: 14% 0001111: 15% 0010000: 16% .... 1011111: 100% >1011111: 100%

Table 211: GPO14_LED

Register Address	Bit	Type	Label	Description
0xC7 GPO14_LED	7	R/W	**GPO14_DIM**	**0: PWM ratio changes instantly** 1: GPO ramps between changes in PWM ratio with 32 ms per step
	6:0	R/W	**GPO14_PWM**	GPO14 LED on-time (low level at GPIO 14, period 21 kHz = 95 cycles of 0.5 µs) **0000000: off** 0000001: 1% 0000010: 2% (1 µs bursts) 0000011: 3% 0000100: 4% 0000101: 5% 0000110: 6% 0000111: 7% 0001000: 8% 0001001: 9% 0001010: 10% 0001011: 11% 0001100: 12% 0001101: 13% 0001110: 14% 0001111: 15% 0010000: 16% .... 1011111: 100% >1011111: 100%

Table 212: GPO15_LED

Register Address	Bit	Type	Label	Description
0xC8 GPO15_LED	7	R/W	**GPO15_DIM**	**0: PWM ratio changes instantly** 1: GPO ramps between changes in PWM ratio with 32 ms per step
	6:0	R/W	**GPO15_PWM**	GPO15 LED on-time (low level at GPIO 15, period 21 kHz = 95 cycles of 0.5 µs) **0000000: off** 0000001: 1% 0000010: 2% (1 µs bursts) 0000011: 3% 0000100: 4% 0000101: 5% 0000110: 6% 0000111: 7% 0001000: 8% 0001001: 9% 0001010: 10% 0001011: 11% 0001100: 12% 0001101: 13% 0001110: 14% 0001111: 15% 0010000: 16% .... 1011111: 100% >1011111: 100%

A.3.5 GPADC Thresholds

Table 213: ADC_CFG

Register Address	Bit	Type	Label	Description
0xC9 ADC_CFG	7	R/W	**ADCIN3_DEB**	0: ADCIN3: debouncing off **1: ADCIN3: debouncing on**
	6	R/W	**ADCIN2_DEB**	0: ADCIN2: debouncing off **1: ADCIN2: debouncing on**
	5	R/W	**ADCIN1_DEB**	0: ADCIN1: debouncing off **1: ADCIN1: debouncing on**
	4	R/W	**ADCIN3_CUR**	ADCIN3 current source: **0: 10 µA** 1: 40 µA
	3:2	R/W	**ADCIN2_CUR**	ADCIN2 current source: 00: 1 µA 01: 2.5 µA **10: 10 µA** 11: 40 µA
	1:0	R/W	**ADCIN1_CUR**	ADCIN1 current source: 00: 1 µA 01: 2.5 µA **10: 10 µA** 11: 40 µA

Table 214: AUTO1_HIGH

Register Address	Bit	Type	Label	Description
0xCA AUTO1_HIGH	7:0	R/W	**AUTO1_HIGH**	00000000 – 11111111: ADCIN1 high level threshold

Table 215: AUTO1_LOW

Register Address	Bit	Type	Label	Description
0xCB AUTO1_LOW	7:0	R/W	**AUTO1_LOW**	00000000 – 11111111: ADCIN1 low level threshold

Table 216: AUTO2_HIGH

Register Address	Bit	Type	Label	Description
0xCC AUTO2_HIGH	7:0	R/W	**AUTO2_HIGH**	00000000 – 11111111: ADCIN2 high level threshold

Table 217: AUTO2_LOW

Register Address	Bit	Type	Label	Description
0xCD AUTO2_LOW	7:0	R/W	**AUTO2_LOW**	00000000 – 11111111: ADCIN2 low level threshold

Table 218: AUTO3_HIGH

Register Address	Bit	Type	Label	Description
0xCE AUTO3_HIGH	7:0	R/W	**AUTO3_HIGH**	00000000 – 11111111: ADCIN3 high level threshold

Table 219: AUTO3_LOW

Register Address	Bit	Type	Label	Description
0xCF AUTO3_LOW	7:0	R/W	**AUTO3_LOW**	00000000 – 11111111: ADCIN3 low level threshold

Table 220: Copmic_S to Copmic_E

Register Address	Bit	Type	Label	Description
0xD0 CoPMIC_S	7:0	R	Reserved	Reserved for Co-PMIC
0xDF CoPMIC_E	7:0	R	Reserved	Reserved for Co-PMIC

Table 221: CHG_Co_S to CHG_Co_E

Register Address	Bit	Type	Label	Description
0xE0 CHG_Co_S	7:0	R	Reserved	Reserved for companion charger
0xFF CHG_Co_E	7:0	R	Reserved	Reserved for companion charger

A.4 Register Page 2

Table 222: PAGE_CON

Register Address	Bit	Type	Label	Description
0x100 PAGE_CON	7	RW	REVERT	See register 0x00, Table 59
	6	RW	WRITE_MODE	
	5:3	RW	Reserved	
	2:0	RW	REG_PAGE	

A.4.1 OTP

Table 223: OTP_CONT

Register Address	Bit	Type	Label	Description
0x101 OTP_CONT	7	R	**GP_WRITE_DIS**	**0: Enables write access to GP_ID registers** 1: GP_ID_0to GP_ID_9 registers are 'read only'
	6	R	**OTP_CONF_LOCK**	0: Registers 0x0A to 0x36 and 0x82 to 0xCF are not locked for OTP programming (only for evaluation samples) **1: OTP registers 0x0A to 0x36 and 0x82 to 0xCF are locked in OTP (set for all mass production parts, no further fusing possible)**
	5	R	**OTP_APPS_LOCK**	0: Registers 0x104 to 0x117are not locked for OTP programming (only for evaluation samples) **1: OTP registers 0x104 to 0x117 are locked in OTP (set for all mass production parts, no further fusing possible)**
	4	R	**OTP_GP_LOCK**	**0: Registers 0x120 to 0x134 are not locked for OTP programming** 1: Registers 0x120 to 0x134 are locked in OTP (no further fusing possible if once fused with 1)
	3	R/W	**PC_DONE**	Asserted from Power Commander SW after emulated OTP read has finished (control shared with Co-PMIC), automatically cleared when leaving emulated OTP read
	2	R/W	**OTP_APPS_RD**	Reads on assertion application specific registers (0x104 to 0x117 and OTP_APPS_LOCK) from OTP
	1	R/W	**OTP_GP_RD**	Reads on assertion device specific registers 0x120 to 0x134 (plus GP_WRITE_DIS and OTP_GP_LOCK) from OTP
	0	R/W	**OTP_TIM**	OTP read timing **0: normal read** 1: marginal read (for OTP fuse verification)

Table 224: OTP_ADDR

Register Address	Bit	Type	Label	Description
0x102 OTP_ADDR	7:0	R/W	OTP_ADDR	OTP Array address (shared with Companion ICs)

Table 225: OTP_DATA

Register Address	Bit	Type	Label	Description
0x103 OTP_DATA	7:0	R/W	OTP_DATA	OTP read/write data (shared with Companion ICs) OTP_DATA written to OTP_ADDR selects the IC and accepts unlock sequence (1 + 3 bytes)

A.4.2 Customer Trim and Configuration

Table 226: T_OFFSET

Register Address	Bit	Type	Label	Description
0x104 T_OFFSET	7:0	R	**T_OFFSET**	10000000 – 01111111: signed two's complement calibration offset for junction temperature measurement (loaded from the OTP memory, must be programmed during production)

Table 227: INTERFACE

Register Address	Bit	Type Note 1	Label	Description
0x105 INTERFACE	7:4	R	**IF_BASE_ADDR**	4 MSB of 2-WIRE control interfaces base address XXXX0000 **1011**0000 = 0xB0 write address of PM 2-WIRE interface (page 0 and 1) **1011**0001 = 0xB1 read address of PM 2-WIRE interface (page 0 and 1) **1011**0010 = 0xB2 write address of PM-2-WIRE interface (page 2 and 3) **1011**0011 = 0xB3 read address of PM-2-WIRE interface (page 2 and 3) **1011**0100 = 0xB4 write address of HS 2-WIRE interface (page 0 and 1) **1011**0101 = 0xB5 read address of HS 2-WIRE interface (page 0 and 1) **1011**0110 = 0xB6 write address of HS-2-WIRE interface (page 2 and 3) **1011**0111 = 0xB7 read address of HS-2-WIRE interface (page 2 and 3) Code '0000' is reserved for unprogrammed OTP (triggers start-up with hardware default interface address)
	3	R	**R/W_POL**	4-WIRE: Read/Write bit polarity 0: Host indicates reading access via R/W bit = 0 **1: Host indicates reading access via R/W bit = 1**

Register Address	Bit	Type Note 1	Label	Description
	2	R	**CPHA**	4-WIRE IF clock phase (see Table 43)
	1	R	**CPOL**	4-WIRE IF clock polarity **0: SK is low during idle** 1: SK is high during idle
	0	R	**nCS_POL**	4-WIRE chip select polarity 0: nCS is active low **1: nCS is active high**

Note 1 The interface configuration can be written/modified only for unmarked samples which do not have the control OTP_APPS_LOCK asserted/fused.

Table 228: CONFIG_A

Register Address	Bit	Type	Label	Description
0x106 CONFIG_A	7	R Note 1	**IF_TYPE**	0: Power manager IF is 4-WIRE **1: Power manager IF is 2-WIRE**
	6	R/W	**PM_IF_HSM**	Enables continuous High Speed mode on PM 2-WIRE IF if asserted (no master code required)
	5	R/W	**PM_IF_FMP**	Selects fast-mode+ timings for PM 2-WIRE IF if asserted
	4	R/W	**PM_IF_V**	**0: Power manager IF in 4-WIRE mode is supplied from VDD_IO1, in 2-WIRE mode from VDDCORE** 1: Power manager IF (4-WIRE/2-WIRE) supplied from VDD_IO2
	3	R/W	**IRQ_TYPE**	nIRQ output is: **0: Active low** 1: Active high (invert signal)
	2	R/W	**PM_O_TYPE**	nRESET, nIRQ output are: 0: Push-pull **1: Open drain (requires external pull-up resistor)**
	1	R/W	**PM_O_V**	OUT_32K, OUT_32K_2, E_GPI_2, COMP1V2, nRESET, nIRQ are supplied from: 0: VDD_IO1 **1: VDD_IO2**
	0	R/W	**PM_I_V**	nOFF, nSHUTDOWN, SYS_EN, PWR_EN, PWR1_EN, KEEP_ACT, nVIB_BRAKE are supplied from: **0: VDDCORE** 1: VDD_IO2

Note 1 The interface configuration can be written/modified only for unmarked samples which do not have the control OTP_APPS_LOCK asserted/fused.

Table 229: CONFIG_B

Register Address	Bit	Type	Label	Description
0x107 CONFIG_B	7	R/W	**Reserved**	
	6:4	R/W	**VDD_HYST_ADJ**	Hysteresis adjust of VDD_FAULT comparator (VDD_FAULT_UPPER) in 50 mV steps 000: 100 mV **001: 150 mV** … 111: 450 mV
	3:0	R/W	**VDD_FAULT_ADJ**	Setting of VDD_FAULT_LOWER comparator in 50 mV steps 0000: 2.50 V 0001: 2.55 V … **0110: 2.80 V** … 1110: 3.20 V 1111: 3.25 V

Table 230: CONFIG_C

Register Address	Bit	Type	Label	Description
0x108 CONFIG_C	7	R/W	**BPERI_CLK_INV**	BUCKPERI clock polarity 0: Normal 1: Inverted
	6	R/W	**BIO_CLK_INV**	BUCKIO clock polarity 0: Normal 1: Inverted
	5	R/W	**BMEM_CLK_INV**	BUCKMEM clock polarity 0: Normal 1: Inverted
	4	R/W	**BPRO_CLK_INV**	BUCKPRO clock polarity (should be configured opposite to BUCKMEM clock polarity) 0: Normal 1: Inverted
	3	R/W	**BCORE1_CLK_INV**	BUCKCORE1 clock polarity (BUCKCORE2 always runs on opposite clock polarity) 0: Normal 1: Inverted
	2	R/W	**BUCK_ACTV_DISCHG**	Enable active discharge of buck rails
	1:0	R/W	**LDO1_TRACK**	LDO1 follows voltage transitions of **00: none** 01:VBUCK_PRO 10:VBUCK_CORE1 11:VBUCK_CORE2

Table 231: CONFIG_D

Register Address	Bit	Type	Label	Description
0x109 CONFIG_D	7	R/W	**GP_FB3_TYPE**	GP_FB3 output is: **0: Active low** 1: Active high (invert signal)
	6	R/W	**GP_FB2_TYPE**	GP_FB2 output is: 0: Active low (invert signal, push-pull for PWR_OK) **1: Active high (open drain for PWR_OK)**
	5	R/W	**FORCE_RESET**	Asserts port nRESET in case of being set
	4	R/W	**HS_IF_HSM**	Enables continuous High Speed mode on HS 2-WIRE IF (no master code required)
	3	R/W	**HS_IF_FMP**	Selects fast-mode+ timings for HS 2-WIRE IF if asserted
	2	R/W	**SYSTEM_EN_RD**	During second OTP read control SYSTEM_EN is **0: updated from OTP** 1: not changed
	1	R/W	**nIRQ_MODE**	nIRQ will be asserted from events during POWERDOWN mode (and modes lower than ACTICE) **0: immediately** 1: after powering up to ACTIVE mode
	0	R/W	**GPI_V**	GPIs (not configured as Power Manager control inputs) and HS-2-WIRE IF are supplied from: **0: VDDCORE** 1: VDD_IO2

Table 232: CONFIG_E

Register Address	Bit	Type	Label	Description
0x10A CONFIG_E	7	R/W	**PERI_SW_AUTO**	Selects PERI_SW (during powering up): 0: configured from PERI_SW_CONF 1: enabled
	6	R/W	**CORE_SW_AUTO**	Selects CORE_SW (during powering up): 0: configured from CORE_SW_CONF 1: enabled
	5	R/W	**BPERI_AUTO**	Selects BUCKPERI (during powering up): 0: configured from BPERI_CONF 1: enabled
	4	R/W	**BIO_AUTO**	Selects BUCKIO (during powering up): 0: configured from BIO_CONF 1: enabled
	3	R/W	**BMEM_AUTO**	Selects BUCKMEM (during powering up): 0: configured from BMEM_CONF 1: enabled
	2	R/W	**BPRO_AUTO**	Selects BUCKPRO (during powering up): 0: configured from BPRO_CONF 1: enabled

Register Address	Bit	Type	Label	Description
	1	R/W	**BCORE2_AUTO**	Selects BUCKCORE2 (during powering up): 0: configured from BCORE2_CONF 1: enabled
	0	R/W	**BCORE1_AUTO**	Selects BUCKCORE1 (during powering up): 0: configured from BCORE1_CONF 1: enabled

Table 233: CONFIG_F

Register Address	Bit	Type	Label	Description
0x10B CONFIG_F	7	R/W	**LDO11_BYP**	**0: LDO11 is configured for regulator mode** 1: LDO11 bypass mode enabled
	6	R/W	**LDO8_BYP**	**0: LDO8 is configured for regulator mode** 1: LDO8 bypass mode enabled
	5	R/W	**LDO7_BYP**	**0: LDO7 is configured for regulator mode** 1: LDO7 bypass mode enabled
	4	R/W	**LDO4_BYP**	**0: LDO4 is configured for regulator mode** 1: LDO4 bypass mode enabled
	3	R/W	**LDO3_BYP**	**0: LDO3 is configured for regulator mode** 1: LDO3 bypass mode enabled
	2	R/W	**LDO11_AUTO**	Selects LDO11 (during powering up): 0: configured from LDO11_CONF 1: enabled
	1	R/W	**LDO10_AUTO**	Selects LDO10 (during powering up): 0: configured from LDO10_CONF 1: enabled
	0	R/W	**LDO9_AUTO**	Selects LDO9 (during powering up): 0: configured from LDO9_CONF 1: enabled

Table 234: CONFIG_G

Register Address	Bit	Type	Label	Description
0x10C CONFIG_G	7	R/W	**LDO8_AUTO**	Selects LDO8 (during powering up): 0: configured from LDO8_CONF 1: enabled
	6	R/W	**LDO7_AUTO**	Selects LDO7 (during powering up): 0: configured from LDO7_CONF 1: enabled
	5	R/W	**LDO6_AUTO**	Selects LDO6 (during powering up): 0: configured from LDO6_CONF 1: enabled
	4	R/W	**LDO5_AUTO**	Selects LDO5 (during powering up): 0: configured from LDO5_CONF 1: enabled
	3	R/W	**LDO4_AUTO**	Selects LDO4 (during powering up): 0: configured from LDO4_CONF 1: enabled

Register Address	Bit	Type	Label	Description
	2	R/W	**LDO3_AUTO**	Selects LDO3 (during powering up): 0: configured from LDO3_CONF 1: enabled
	1	R/W	**LDO2_AUTO**	Selects LDO2 (during powering up): 0: configured from LDO2_CONF 1: enabled
	0	R/W	**LDO1_AUTO**	Selects LDO1 (during powering up): 0: configured from LDO1_CONF 1: enabled

Table 235: CONFIG_H

Register Address	Bit	Type	Label	Description
0x10D CONFIG_H	7	R/W	**BUCK_MERGE**	Has to be set if the outputs of BUCKMEM and BUCKIO are merged towards a single coil; the control from BUCKIO registers is disabled
	6	R/W	**BCORE1_OD**	If set, BUCKCORE1 changes to full-current mode (double pass device and current limit)
	5	R/W	**BCORE2_OD**	If set, BUCKCORE2 changes to full-current mode (double pass device and current limit)
	4	R/W	**BPRO_OD**	If set, BUCKPRO changes to full-current mode (double pass device and current limit)
	3	R/W	**BCORE_MERGE**	Has to be set if the outputs of BUCKCORE1 and BUCKCORE2 are merged towards a dual phase buck; the control from BUCKCORE2 registers is disabled
	2	R/W	**MERGE_SENSE**	In case BUCKCORE is merged and configured for remote sensing the output capacitor voltage rail is routed to port: **0: GP_FB_2 (setting disables normal GP_FB_2 functionality)** 1: CORE_SWS (setting disables CORE rail switch pull-down functionality) Note: In case MERGE_SENSE is asserted all Bxxx_FB control settings 0bx1x are invalid
	1	R/W	**LDO8_MODE**	**0: LDO mode (external capacitor required)** 1: Vibration motor driver (no external capacitor)
	0	R/W	**PWM_CLK**	**0: 2.0 MHz (31.25 kHz repetition frequency)** 1: 1.0 MHz (15.6 kHz repetition frequency)

Table 236: CONFIG_I

Register Address	Bit	Type	Label	Description
0x10E CONFIG_I	7	R/W	**LDO_SD**	If asserted LDO3, 4, 7, 8 and 11 will shut down after current limit was hit for more than 200 ms
	6	R/W	**INT_SD_MODE**	Shut down sequence from internal fault condition is: **0: Normal** 1: Fast (skipping seq and dummy slot timers)
	5	R/W	**HOST_SD_MODE**	Shut down sequence from SHUTDOWN (register bit or port nSHUTDOWN) is: 0: Normal **1: Fast (skipping seq and dummy slot timers)**
	4	R/W	**KEY_SD_MODE**	User triggered (nONKEY, GPIO14/15) shutdown sequence is: **0: Normal** 1: PMU POR: triggers an instant disable of all regulators incl. LDOCORE (RTC and FAULTLOG registers remain unchanged). After leaving POR automatically the RESET_DURATION timer must expire before starting a power-up sequence.
	3	R/W	**GPI14_15_SD**	**0: Disables shutdown via parallel assertion of GPI14 and GPI15** 1: Enables shutdown via GPI14 & GPI15
	2	R/W	**nONKEY_SD**	nONKEY is configured **0: without shutdown via long press of nONKEY** 1: with shutdown via long press of nONKEY
	1:0	R/W	**nONKEY_PIN**	nONKEY is configured to 00: Port mode **01: Key mode with key lock during SW triggered POWERDOWN mode** 10: Key mode with key locked autonomous powering down (multi-functional key) 11: Key mode with autonomous powering down to partial or key locked full POWERDOWN mode (dedicated power key) Details: see Section 6.1.1

Table 237: CONFIG_J

Register Address	Bit	Type	Label	Description
0x10F CONFIG_J	7	R/W	**IF_RESET**	Enables automatic reset of all control interfaces when port nSHUTDOWN is asserted
	6	R/W	**TWOWIRE_TO**	Enables automatic reset of 2-WIRE-IF in case of clock ceases to toggle for >19 ms

Register Address	Bit	Type	Label	Description
	5:4	R/W	**RESET_DURATION**	Power controller stays in RESET mode for minimum duration of 00: 20 ms 01: 100 ms **10: 500 ms** 11: 1000 ms
	3:2	R/W	**SHUT_DELAY**	Long press time threshold for shutdown feature from nONKEY and GPIO14/15: 00: KEY_DELAY + 0 s 01: KEY_DELAY + 4 s **10: KEY_DELAY + 5 s** 11: KEY_DELAY + 6 s
	1:0	R/W	**KEY_DELAY**	Long press threshold for nONKEY lock: 00: nONKEY_LOCK after 1 s 01: nONKEY_LOCK after 1.5 s **10: nONKEY_LOCK after 2 s** 11: nONKEY_LOCK after 7 s

Note 1 This setting may trigger glidges on regulator outputs and disable the automatic RESET/POR of slave PMUs).

Table 238: CONFIG_K

Register Address	Bit	Type	Label	Description
0x110 CONFIG_K	7	R/W	**GPIO7_PUPD**	**0: GPI: pull-down resistor disabled GPO (open drain): pull-up resistor disabled (external pull-up resistor)** 1: GPI: pull-down resistor enabled GPO (open drain): pull-up resistor enabled (supply rail selected via GPIOx_TYPE)
	6	R/W	**GPIO6_PUPD**	**0: GPI: pull-down resistor disabled GPO (open drain): pull-up resistor disabled (external pull-up resistor)** 1: GPI: pull-down resistor enabled GPO (open drain): pull-up resistor enabled (supply rail selected via GPIOx_TYPE)
	5	R/W	**GPIO5_PUPD**	**0: GPI: pull-down resistor disabled GPO (open drain): pull-up resistor disabled (external pull-up resistor)** 1: GPI: pull-down resistor enabled GPO (open drain): pull-up resistor enabled (supply rail selected via GPIOx_TYPE)
	4	R/W	**GPIO4_PUPD**	**0: GPI: pull-down resistor disabled GPO (open drain): pull-up resistor disabled (external pull-up resistor)** 1: GPI: pull-down resistor enabled GPO (open drain): pull-up resistor enabled (supply rail selected via GPIOx_TYPE)
	3	R/W	**GPIO3_PUPD**	**0: GPI: pull-down resistor disabled GPO (open drain): pull-up resistor disabled (external pull-up resistor)** 1: GPI: pull-down resistor enabled GPO (open drain): pull-up resistor enabled (supply rail selected via GPIOx_TYPE)

Register Address	Bit	Type	Label	Description
	2	R/W	**GPIO2_PUPD**	**0: GPI: pull-down resistor disabled GPO (open drain): pull-up resistor disabled (external pull-up resistor)** 1: GPI: pull-down resistor enabled GPO (open drain): pull-up resistor enabled (supply rail selected via GPIOx_TYPE)
	1	R/W	**GPIO1_PUPD**	**0: GPI: pull-down resistor disabled GPO (open drain): pull-up resistor disabled (external pull-up resistor)** 1: GPI: pull-down resistor enabled GPO (open drain): pull-up resistor enabled (supply rail selected via GPIOx_TYPE)
	0	R/W	**GPIO0_PUPD**	**0: GPI: pull-down resistor disabled GPO (open drain): pull-up resistor disabled (external pull-up resistor)** 1: GPI: pull-down resistor enabled GPO (open drain): pull-up resistor enabled (supply rail selected via GPIOx_TYPE)

Table 239: CONFIG_L

Register Address	Bit	Type	Label	Description
0x111 CONFIG_L	7	R/W	**GPIO15_PUPD**	**0: GPI: pull-down resistor disabled GPO (open drain): pull-up resistor disabled (external pull-up resistor)** 1: GPI: pull-down resistor enabled GPO (open drain): pull-up resistor enabled (supply rail selected via GPIOx_TYPE)
	6	R/W	**GPIO14_PUPD**	**0: GPI: pull-down resistor disabled GPO (open drain): pull-up resistor disabled (external pull-up resistor)** 1: GPI: pull-down resistor enabled GPO (open drain): pull-up resistor enabled (supply rail selected via GPIOx_TYPE)
	5	R/W	**GPIO13_PUPD**	**0: GPI: pull-down resistor disabled GPO (open drain): pull-up resistor disabled (external pull-up resistor)** 1: GPI: pull-down resistor enabled GPO (open drain): pull-up resistor enabled (supply rail selected via GPIOx_TYPE)
	4	R/W	**GPIO12_PUPD**	**0: GPI: pull-down resistor disabled GPO (open drain): pull-up resistor disabled (external pull-up resistor)** 1: GPI: pull-down resistor enabled GPO (open drain): pull-up resistor enabled (supply rail selected via GPIOx_TYPE)
	3	R/W	**GPIO11_PUPD**	**0: GPI: pull-down resistor disabled GPO (open drain): pull-up resistor disabled (external pull-up resistor)** 1: GPI: pull-down resistor enabled GPO (open drain): pull-up resistor enabled (supply rail selected via GPIOx_TYPE)

Register Address	Bit	Type	Label	Description
	2	R/W	**GPIO10_PUPD**	**0: GPI: pull-down resistor disabled GPO (open drain): pull-up resistor disabled (external pull-up resistor)** 1: GPI: pull-down resistor enabled GPO (open drain): pull-up resistor enabled (supply rail selected via GPIOx_TYPE)
	1	R/W	**GPIO9_PUPD**	**0: GPI: pull-down resistor disabled GPO (open drain): pull-up resistor disabled (external pull-up resistor)** 1: GPI: pull-down resistor enabled GPO (open drain): pull-up resistor enabled (supply rail selected via GPIOx_TYPE)
	0	R/W	**GPIO8_PUPD**	**0: GPI: pull-down resistor disabled GPO (open drain): pull-up resistor disabled (external pull-up resistor)** 1: GPI: pull-down resistor enabled GPO (open drain): pull-up resistor enabled (supply rail selected via GPIOx_TYPE)

Table 240: CONFIG_M

Register Address	Bit	Type	Label	Description
0x112 CONFIG_M	7:4	R/W	**OSC_FRQ**	Offset for internal HF oscillator frequency 1000: -10.67 % … 1111: -1.33 % 0000: 0.00 % 0001: 1.33 % … 0111: 9.33 %
	3:0	R/W	**Reserved**	

Table 241: Reserved

Register Address	Bit	Type	Label	Description
0x113	7:0	R/W	**Reserved**	

Table 242: MON_REG_1

Register Address	Bit	Type	Label	Description
0x114 MON_REG_1	7:6	R/W	**UVOV_DELAY**	Range comparison is enabled after regulator enable: 00: immediately 01: with one measurement delay 10: with two measurements delay 11: with four measurements delay

Register Address	Bit	Type	Label	Description
	5:4	R/W	**MON_MODE**	Regulator monitor executes **00: Under-voltage/Over-voltage lockout with an E_REG_UVOV event (nIRQ assertion) and regulator shutdown from an output voltage being out of the selected range** 01: Normal auto measurement with an E_REG_UVOV event (nIRQ assertion) from any finished auto measurement on A8, A9 and A10 10: Burst auto measurement with an E_REG_UVOV event (nIRQ assertion) generated after the time slot of A10 has been processed 11: reserved
	3	R/W	**MON_DEB**	0: Regulator monitor (A8, 9, 10): debouncing off **1: Regulator monitor (A8, 9, 10): debouncing on**
	2	R/W	**MON_RES**	Control requires M_REG_UVOV = 1: 1: Enables assertion of nRESET from out-of-range detection Note: It is not recommended to assert this control inside OTP
	1:0	R/W	**MON_THRES**	Regulator Monitor Threshold 00: Approx = 25 % 01: Approx = 12.5 % 10: Approx = 6.25 % 11: Approx = 3.125 %

Table 243: MON_REG_2

Register Address	Bit	Type	Label	Description
0x115 MON_REG_2	7	R/W	**LDO8_MON_EN**	Enable LDO8 regulator monitoring
	6	R/W	**LDO7_MON_EN**	Enable LDO7 regulator monitoring
	5	R/W	**LDO6_MON_EN**	Enable LDO6 regulator monitoring
	4	R/W	**LDO5_MON_EN**	Enable LDO5 regulator monitoring
	3	R/W	**LDO4_MON_EN**	Enable LDO4 regulator monitoring
	2	R/W	**LDO3_MON_EN**	Enable LDO3 regulator monitoring
	1	R/W	**LDO2_MON_EN**	Enable LDO2 regulator monitoring
	0	R/W	**LDO1_MON_EN**	Enable LDO1 regulator monitoring

Table 244: MON_REG_3

Register Address	Bit	Type	Label	Description
0x116 MON_REG_3	7:3	R/W	**Reserved**	
	2	R/W	**LDO11_MON_EN**	Enable LDO11 regulator monitoring
	1	R/W	**LDO10_MON_EN**	Enable LDO10 regulator monitoring
	0	R/W	**LDO9_MON_EN**	Enable LDO9 regulator monitoring

Table 245: MON_REG_4

Register Address	Bit	Type	Label	Description
0x117 MON_REG_4	7	R/W	**BPERI_MON_EN**	Enable BUCKPERI regulator monitoring
	6	R/W	**BMEM_MON_EN**	Enable BUCKMEM regulator monitoring
	5	R/W	**BIO_MON_EN**	Enable BUCKIO regulator monitoring
	4	R/W	**BPRO_MON_EN**	Enable BUCKPRO regulator monitoring
	3	R/W	**BCORE2_MON_EN**	Enable BUCKCORE2 regulator monitoring
	2	R/W	**BCORE1_MON_EN**	Enable BUCKCORE1 regulator monitoring
	1:0	R/W	**Reserved**	

Table 246: MON_REG_5

Register Address	Bit	Type	Label	Description
0x11E MON_REG_5	7	R	Reserved	
	6:4	R/W	MON_A9_IDX	Latest measurement at channel A9 was: 000: none 001: BUCKIO 010: BUCKMEM 011: BUCKPERI 100: LDO1 101: LDO2 101: LDO5 > 110: reserved
	3	R/W	Reserved	
	2:0	R/W	MON_A8_IDX	Latest measurement at channel A8 was: 000: none 001: BUCKCORE1 010: BUCKCORE2 011: BUCKPRO 100: LDO3 101: LDO4 110: LDO11 > 110: reserved

Table 247: MON_REG_6

Register Address	Bit	Type	Label	Description
0x11F MON_REG_6	7:3	R/W	Reserved	
	2:0	R/W	MON_A10_IDX	Latest measurement at channel A10 was: 000: none 001: LDO6 010: LDO7 011: LDO8 100: LDO9 101: LDO10 > 101: reserved

Table 248: TRIM_CLDR

Register Address	Bit	Type	Label	Description
0x120 TRIM_CLDR	7:0	R/W	**TRIM_32K**	Bits for correction of the 32K oscillator frequency for internal calendar: 10000000: -244.1 ppm … 11111111: -1.9 ppm **00000000: off** 00000001: 1.9 ppm (1/(32768*16)) … 01111111: 242.2 ppm

Table 249: GP_ID_0

Register Address	Bit	Type	Label	Description
0x121 GP_ID_0	7:0	R/W Note 1	**GP_0**	Data from fuse array (OTP)

Note 1 Write access can be disabled by OTP if required.

Table 250: GP_ID_1

Register Address	Bit	Type	Label	Description
0x122 GP_ID_1	7:0	R/W Note 1	**GP_1**	Data from fuse array (OTP)

Note 1 Write access can be disabled by OTP if required.

Table 251: GP_ID_2

Register Address	Bit	Type	Label	Description
0x123 GP_ID_2	7:0	R/W Note 1	**GP_2**	Data from fuse array (OTP)

Note 1 Write access can be disabled by OTP if required.

Table 252: GP_ID_3

Register Address	Bit	Type	Label	Description
0x124 GP_ID_3	7:0	R/W Note 1	**GP_3**	Data from fuse array (OTP)

Note 1 Write access can be disabled by OTP if required.

Table 253: GP_ID_4

Register Address	Bit	Type	Label	Description
0x125 GP_ID_4	7:0	R/W Note 1	**GP_4**	Data from fuse array (OTP)

Note 1 Write access can be disabled by OTP if required.

Table 254: GP_ID_5

Register Address	Bit	Type	Label	Description
0x126 GP_ID_5	7:0	R/W Note 1	**GP_5**	Data from fuse array (OTP)

Note 1 Write access can be disabled by OTP if required.

Table 255: GP_ID_6

Register Address	Bit	Type	Label	Description
0x127 GP_ID_6	7:0	R/W Note 1	**GP_6**	Data from fuse array (OTP)

Note 1 Write access can be disabled by OTP if required.

Table 256: GP_ID_7

Register Address	Bit	Type	Label	Description
0x128 GP_ID_7	7:0	R/W Note 1	**GP_7**	Data from fuse array (OTP)

Note 1 Write access can be disabled by OTP if required.

Table 257: GP_ID_8

Register Address	Bit	Type	Label	Description
0x129 GP_ID_8	7:0	R/W Note 1	**GP_8**	Data from fuse array (OTP)

Note 1 Write access can be disabled by OTP if required.

Table 258: GP_ID_9

Register Address	Bit	Type	Label	Description
0x12A GP_ID_9	7:0	R/W Note 1	**GP_9**	Data from fuse array (OTP)

Note 1 Write access can be disabled by OTP if required.

Table 259: GP_ID_10

Register Address	Bit	Type	Label	Description
0x12B GP_ID_10	7:0	R/W	**GP_10**	Data from fuse array (OTP), no OTP reload after powering up from NO-POWER mode

Table 260: GP_ID_11

Register Address	Bit	Type	Label	Description
0x12C GP_ID_11	7:0	R/W	**GP_11**	Data from fuse array (OTP)

Table 261: Reserved

Register Address	Bit	Type	Label	Description
0x12D – 0x134 Reserved	7:0	R	Reserved	Reserved

Table 262: Co-PMIC2

Register Address	Bit	Type	Label	Description
0x140 CoPMIC2_S	7:0	R	Reserved	Reserved for Co-PMIC

Register Address	Bit	Type	Label	Description
0x14F CoPMIC2_E	7:0	R	Reserved	Reserved for Co-PMIC

Table 263: CHG_Co2

Register Address	Bit	Type	Label	Description
0x150 CHG_Co_S2	7:0	R	Reserved	Reserved for companion charger
0x17F CHG_Co_E2	7:0	R	Reserved	Reserved for companion charger

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Table 264: PAGE_CON

Register Address	Bit	Type	Label	Description
0x180 PAGE_CON	7	RW	REVERT	See register 0x00, Table 59
	6	RW	WRITE_MODE	
	5:3	RW	Reserved	
	2:0	RW	REG_PAGE	

Table 265: DEVICE_ID

Register Address	Bit	Type	Label	Description
0x181 DEVICE_ID	7:0	R	DEVICE_ID	Read back of chip ID

Table 266: VARIANT_ID

Register Address	Bit	Type	Label	Description
0x182 VARIANT_ID	7:4	R	MRC	Read back of mask revision code (MRC)
	3:0	R	**VRC**	Read back of package variant code (VRC)

Table 267: CUSTOMER_ID

Register Address	Bit	Type	Label	Description
0x183 CUSTOMER_ID	7:0	R	**CUSTOMER_ID**	ID for customer and target application platform, written during production of variant

Table 268: CONFIG_ID

Register Address	Bit	Type	Label	Description
0x184 CONFIG_ID	7:0	R	**CONFIG_REV**	ID for revision of OTP settings, written during production of variant 00000000 – OTP unprogrammed (RESERVED) > 00000000 – OTP configuration revision xxx

Table 269: PMIC_STATUS

Register Address	Bit	Type	Label	Description
0x1A8 PMIC_STATUS	7	R	**PC_DONE**	Power Commander download complete
	6:5	R/W	**Reserved**	
	4:0	R	**STATUS**	Decimal Decode: 03 = RESET (Shutdown) 28 = SYSTEM 25 = POWER 23 = POWER-DOWN 20 = POWER1 17 = ACTIVE

System PMIC for Mobile and Automotive Applications

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
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