500kHz and 1MHz High Efficiency 1.5A Switching Regulators

FEATURES

- **Faster Switching with Increased Efficiency**
- **Uses Small Inductors: 4.7µH**
- All Surface Mount Components
- Only 0.5 Square Inch of Board Space
- Low Minimum Supply Voltage: 2.7V
- Quiescent Current: 4mA Typ
- Current Limited Power Switch: 1.5A
- Regulates Positive or Negative Outputs
- Shutdown Supply Current: 12µA Typ
- Easy External Synchronization
- 8-Pin SO or PDIP Packages

APPLICATIONS

- Boost Regulators
- CCFL Backlight Driver
- Laptop Computer Supplies
- Multiple Output Flyback Supplies
- Inverting Supplies

DESCRIPTION

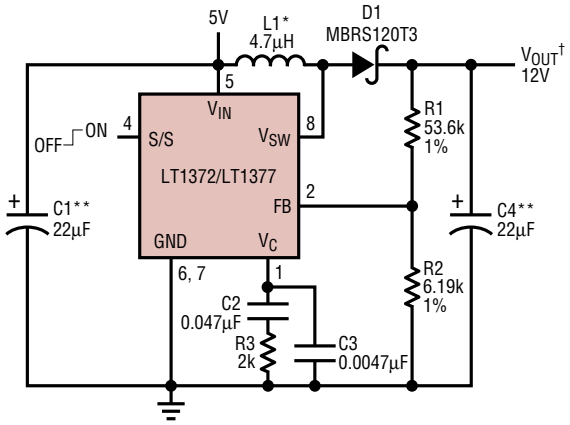
The LT®1372/LT1377 are monolithic high frequency switching regulators. They can be operated in all standard switching configurations including boost, buck, flyback, forward, inverting and "Cuk." A 1.5A high efficiency switch is included on the die, along with all oscillator, control and protection circuitry. All functions of the LT1372/LT1377 are integrated into 8-pin SO/PDIP packages.

The LT1372/LT1377 typically consumes only 4mA quiescent current and has higher efficiency than previous parts. High frequency switching allows for very small inductors to be used. All surface mount components consume less than 0.5 square inch of board space.

New design techniques increase flexibility and maintain ease of use. Switching is easily synchronized to an external logic level source. A logic low on the shutdown pin reduces supply current to 12µA. Unique error amplifier circuitry can regulate positive or negative output voltage while maintaining simple frequency compensation techniques. Nonlinear error amplifier transconductance reduces output overshoot on start-up or overload recovery. Oscillator frequency shifting protects external components during overload conditions.

TYPICAL APPLICATION

5V-to-12V Boost Converter



*FOR LT1372 USE 10µH
COILCRAFT DO1608-472 (4.7µH) OR
COILCRAFT DT3316-103 (10µH) OR
SUMIDA CD43-4R7 (4.7µH) OR
SUMIDA CD73-100KC (10µH) OR

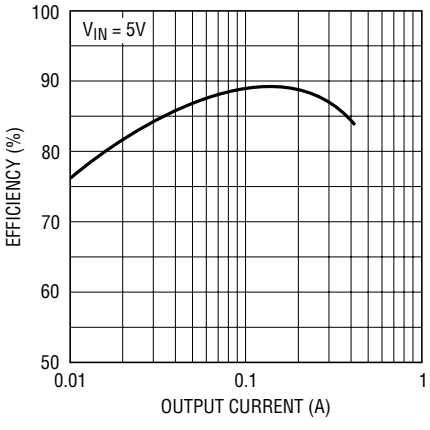
**AVX TPSD226M025R0200

†MAX I_{OUT}

L1	I_{OUT} (LT1377)	I_{OUT} (LT1372)
4.7µH	0.25A	NA
10µH	0.35A	0.29A

LT1372 • TA01

12V Output Efficiency



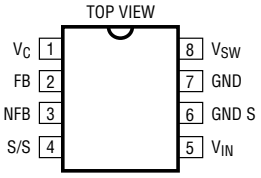
LT1372 • TA02

ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage 30V
Switch Voltage
  LT1372/LT1377 ..... 35V
  LT1372HV 42V
S/S Pin Voltage 30V
Feedback Pin Voltage (Transient, 10ms) ..... ±10V
Feedback Pin Current 10mA
Negative Feedback Pin Voltage
  (Transient, 10ms) ..... ±10V
Operating Junction Temperature Range
  Commercial ..... 0°C to 125°C*
  Industrial ..... –40°C to 125°C
  Short Circuit ..... 0°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PDIP

S8 PACKAGE
8-LEAD PLASTIC SO

T_{JMAX} = 125°C, θ_{JA} = 100°C/W (N8)
T_{JMAX} = 125°C, θ_{JA} = 120°C/W (S8)

ORDER PART NUMBER	
LT1372CN8	LT1372HVIN8
LT1372HVCN8	LT1372IS8
LT1372CS8	LT1372HVIS8
LT1372HVCS8	LT1377CS8
LT1372IN8	LT1377IS8

S8 PART MARKING		
1372	1372H	1377
1372I	1372HI	1377I

Consult factory for parts specified with wider operating temperature ranges.
*Units shipped prior to Date Code 9552 are rated at 100°C maximum operating temperature.

ELECTRICAL CHARACTERISTICS

The ● denotes specifcatons which appy over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, V_C = 0.6V, V_{FB} = V_{REF}, V_{SW}, S/S and NFB pins open, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REF}	Reference Voltage	Measured at Feedback Pin		1.230	1.245	1.260	V
		V_C = 0.8V	●	1.225	1.245	1.265	V
I_{FB}	Feedback Input Current	V_{FB} = V_{REF}			250	550	nA
			●			900	nA
	Reference Voltage Line Regulation	2.7V ≤ V_{IN} ≤ 25V, V_C = 0.8V	●		0.01	0.03	%/V
V_{NFB}	Negative Feedback Reference Voltage	Measured at Negative Feedback Pin		–2.540	–2.490	–2.440	V
		Feedback Pin Open, V_C = 0.8V	●	–2.570	–2.490	–2.410	V
I_{NFB}	Negative Feedback Input Current	V_{NFB} = V_{NFR}	●	–45	–30	–15	µA
	Negative Feedback Reference Voltage Line Regulation	2.7V ≤ V_{IN} ≤ 25V, V_C = 0.8V	●		0.01	0.05	%/V
g_m	Error Amplifier Transconductance	ΔI_C = ±25µA		1100	1500	1900	µmho
			●	700		2300	µmho
	Error Amplifier Source Current	V_{FB} = V_{REF} – 150mV, V_C = 1.5V	●	120	200	350	µA
	Error Amplifier Sink Current	V_{FB} = V_{REF} + 150mV, V_C = 1.5V	●		1400	2400	µA
	Error Amplifier Clamp Voltage	High Clamp, V_{FB} = 1V		1.70	1.95	2.30	V
		Low Clamp, V_{FB} = 1.5V		0.25	0.40	0.52	V
A_V	Error Amplifier Voltage Gain				500		V/V
	V_C Pin Threshold	Duty Cycle = 0%		0.8	1	1.25	V
f	Switching Frequency	2.7V ≤ V_{IN} ≤ 25V					
		LT1372		450	500	550	kHz
		0°C ≤ T_J ≤ 125°C	●	430	500	580	kHz
		–40°C ≤ T_J < 0°C (I Grade)		400		580	kHz
		LT1377		0.90	1	1.10	MHz
		0°C ≤ T_J ≤ 125°C	●	0.86	1	1.16	MHz
		–40°C ≤ T_J < 0°C (I Grade)		0.80		1.16	MHz

ELECTRICAL CHARACTERISTICS

The ● denotes specifcatons which appy over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, V_C = 0.6V, V_{FB} = V_{REF}, V_{SW}, S/S and NFB pins open, unless otherwise noted.

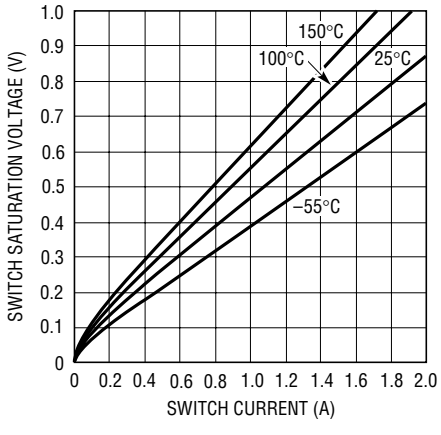
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Maximum Switch Duty Cycle		●	85	95		%
	Switch Current Limit Blanking Time				130	260	ns
BV	Output Switch Breakdown Voltage	LT1372/LT1377 LT1372HV 0°C ≤ T_J ≤ 125°C –40°C ≤ T_J < 0°C (I Grade)	● ● 	35 42 40	47 47 	 	V V V
V_{SAT}	Output Switch "On" Resistance	I_{SW} = 1A	●		0.5	0.8	Ω
I_{LIM}	Switch Current Limit	Duty Cycle = 50% Duty Cycle = 80% (Note 2)	● ●	1.5 1.3	1.9 1.7	2.7 2.5	A A
$\frac{\Delta I_{IN}}{\Delta I_{SW}}$	Supply Current Increase During Switch On-Time				15	25	mA/A
	Control Voltage to Switch Current Transconductance				2		A/V
	Minimum Input Voltage		●		2.4	2.7	V
I_Q	Supply Current	2.7V ≤ V_{IN} ≤ 25V	●		4	5.5	mA
	Shutdown Supply Current	2.7V ≤ V_{IN} ≤ 25V, $V_{S/S}$ ≤ 0.6V 0°C ≤ T_J ≤ 125°C –40°C ≤ T_J < 0°C (I Grade)	 ● 		 12 	 30 50	 µA µA
	Shutdown Threshold	2.7V ≤ V_{IN} ≤ 25V	●	0.6	1.3	2	V
	Shutdown Delay		●	5	12	25	µs
	S/S Pin Input Current	0V ≤ $V_{S/S}$ ≤ 5V	●	–10		15	µA
	Synchronization Frequency Range	LT1372 LT1377	● ●	600 1.2		800 1.6	kHz MHz

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: For duty cycles (DC) between 50% and 90%, minimum guaranteed switch current is given by I_{LIM} = 0.667 (2.75 – DC).

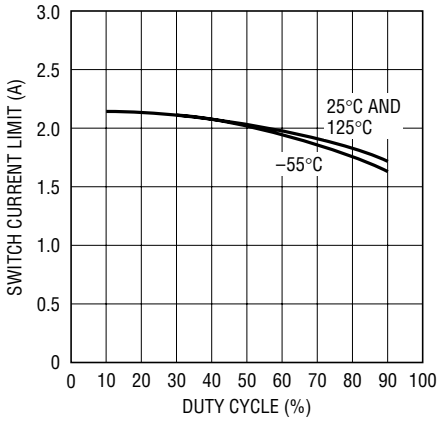
TYPICAL PERFORMANCE CHARACTERISTICS

Switch Saturation Voltage vs Switch Current



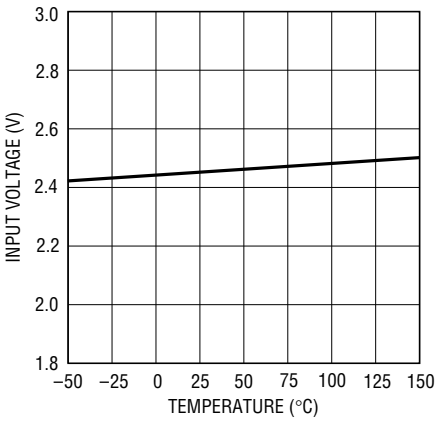
LT1372 • G01

Switch Current Limit vs Duty Cycle



LT1372 • G02

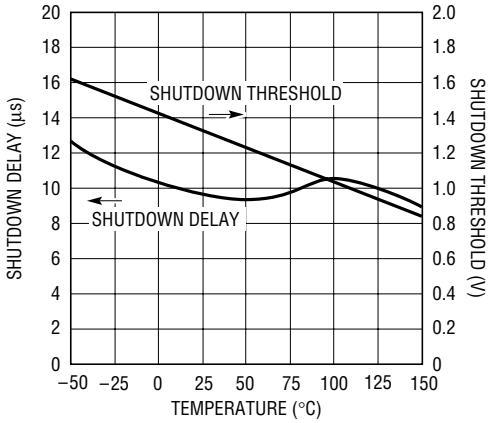
Minimum Input Voltage vs Temperature



LT1372 • G03

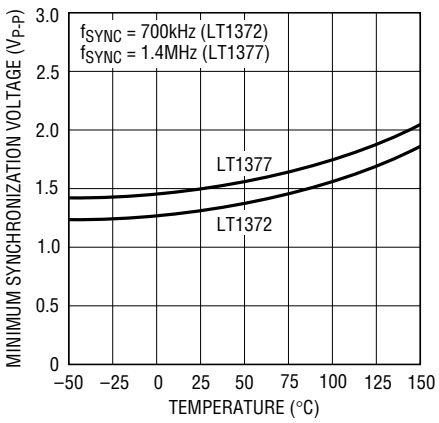
TYPICAL PERFORMANCE CHARACTERISTICS

Shutdown Delay and Threshold vs Temperature



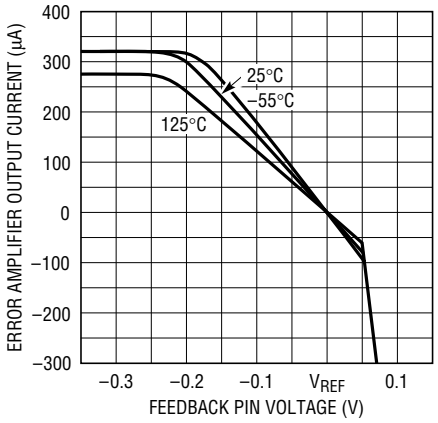
LT1372 • G04

Minimum Synchronization Voltage vs Temperature



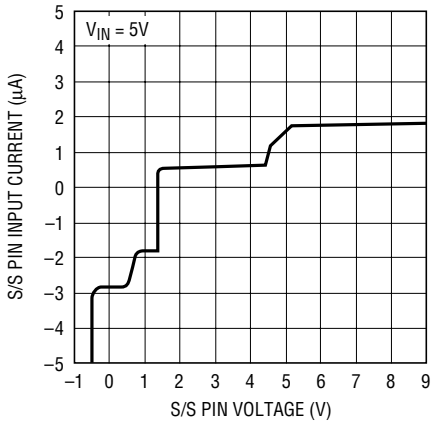
LT1372 • G05

Error Amplifier Output Current vs Feedback Pin Voltage



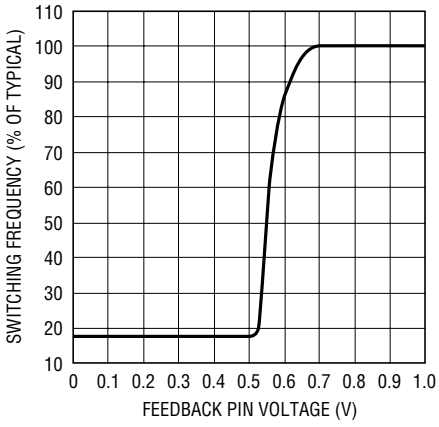
LT1372 • G06

S/S Pin Input Current vs Voltage



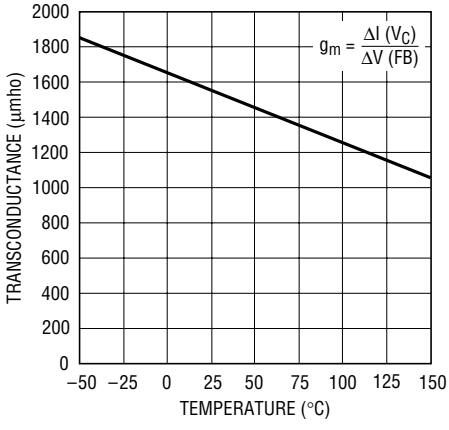
LT1372 • G07

Switching Frequency vs Feedback Pin Voltage



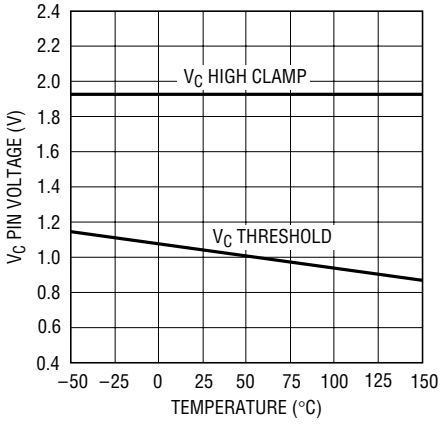
LT1372 • G08

Error Amplifier Transconductance vs Temperature



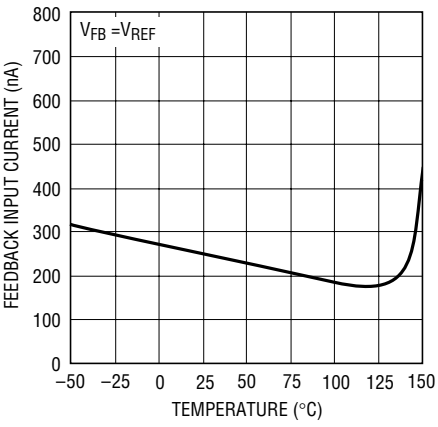
LT1372 • G09

V_C Pin Threshold and High Clamp Voltage vs Temperature



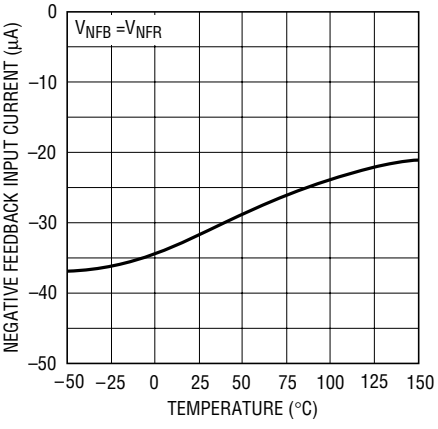
LT1372 • G10

Feedback Input Current vs Temperature



LT1372 • G11

Negative Feedback Input Current vs Temperature



LT1372 • G12

PIN FUNCTIONS

V_C (Pin 1): The compensation pin is used for frequency compensation, current limiting and soft start. It is the output of the error amplifier and the input of the current comparator. Loop frequency compensation can be performed with an RC network connected from the V_C pin to ground.

FB (Pin 2): The feedback pin is used for positive output voltage sensing and oscillator frequency shifting. It is the inverting input to the error amplifier. The noninverting input of this amplifier is internally tied to a 1.245V reference. Load on the FB pin should not exceed 250µA when the NFB pin is used. See Applications Information.

NFB (Pin 3): The negative feedback pin is used for negative output voltage sensing. It is connected to the inverting input of the negative feedback amplifier through a 100k source resistor.

S/S (Pin 4): Shutdown and Synchronization Pin. The S/S pin is logic level compatible. Shutdown is active low and the shutdown threshold is typically 1.3V. For normal operation, pull the S/S pin high, tie it to V_{IN} or leave it floating. To synchronize switching, drive the S/S pin between 600kHz and 800kHz (LT1372) or 1.2MHz to 1.6MHz (LT1377).

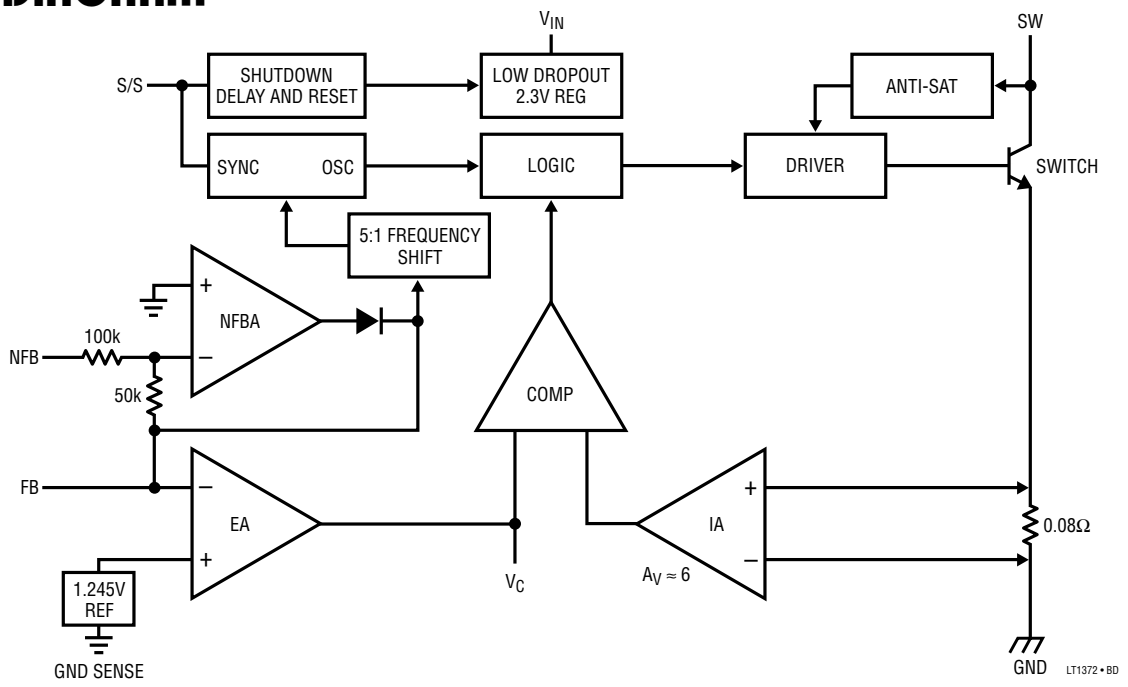
V_{IN} (Pin 5): Bypass input supply pin with 10µF or more. The part goes into undervoltage lockout when V_{IN} drops below 2.5V. Undervoltage lockout stops switching and pulls the V_C pin low.

GND S (Pin 6): The ground sense pin is a "clean" ground. The internal reference, error amplifier and negative feedback amplifier are referred to the ground sense pin. Connect it to ground. Keep the ground path connection to the output resistor divider and the V_C compensation network free of large ground currents.

GND (Pin 7): The ground pin is the emitter connection of the power switch and has large currents flowing through it. It should be connected directly to a good quality ground plane.

V_{SW} (Pin 8): The switch pin is the collector of the power switch and has large currents flowing through it. Keep the traces to the switching components as short as possible to minimize radiation and voltage spikes.

BLOCK DIAGRAM



OPERATION

The LT1372/LT1377 are current mode switchers. This means that switch duty cycle is directly controlled by switch current rather than by output voltage. Referring to the block diagram, the switch is turned "On" at the start of each oscillator cycle. It is turned "Off" when switch current reaches a predetermined level. Control of output voltage is obtained by using the output of a voltage sensing error amplifier to set current trip level. This technique has several advantages. First, it has immediate response to input voltage variations, unlike voltage mode switchers which have notoriously poor line transient response. Second, it reduces the 90° phase shift at mid-frequencies in the energy storage inductor. This greatly simplifies closed-loop frequency compensation under widely varying input voltage or output load conditions. Finally, it allows simple pulse-by-pulse current limiting to provide maximum switch protection under output overload or short conditions. A low dropout internal regulator provides a 2.3V supply for all internal circuitry. This low dropout design allows input voltage to vary from 2.7V to 25V with virtually no change in device performance. A 500kHz (LT1372) or 1MHz (LT1377) oscillator is the basic clock for all internal timing. It turns "On" the output switch via the logic and driver circuitry. Special adaptive anti-sat circuitry detects onset of saturation in the power switch and adjusts driver current instantaneously to limit switch saturation. This minimizes driver dissipation and provides very rapid turn-off of the switch.

A 1.245V bandgap reference biases the positive input of the error amplifier. The negative input of the amplifier is brought out for positive output voltage sensing. The error amplifier has nonlinear transconductance to reduce output overshoot on start-up or overload recovery. When the feedback voltage exceeds the reference by 40mV, error amplifier transconductance increases ten times, which reduces output overshoot. The feedback input also invokes oscillator frequency shifting, which helps protect components during overload conditions. When the feedback voltage drops below 0.6V, the oscillator frequency is reduced 5:1. Lower switching frequency allows full control of switch current limit by reducing minimum switch duty cycle.

Unique error amplifier circuitry allows the LT1372/LT1377 to directly regulate negative output voltages. The negative feedback amplifier's 100k source resistor is brought out for negative output voltage sensing. The NFB pin regulates at –2.49V while the amplifier output internally drives the FB pin to 1.245V. This architecture, which uses the same main error amplifier, prevents duplicating functions and maintains ease of use. Consult Linear Technology Marketing for units that can regulate down to –1.25V.

The error signal developed at the amplifier output is brought out externally. This pin (V_C) has three different functions. It is used for frequency compensation, current limit adjustment and soft starting. During normal regulator operation this pin sits at a voltage between 1V (low output current) and 1.9V (high output current). The error amplifier is a current output (g_m) type, so this voltage can be externally clamped for lowering current limit. Likewise, a capacitor coupled external clamp will provide soft start. Switch duty cycle goes to zero if the V_C pin is pulled below the control pin threshold, placing the LT1372/LT1377 in an idle mode.

APPLICATIONS INFORMATION

Positive Output Voltage Setting

The LT1372/LT1377 develops a 1.245V reference (V_{REF}) from the FB pin to ground. Output voltage is set by connecting the FB pin to an output resistor divider (Figure 1). The FB pin bias current represents a small error and can usually be ignored for values of R2 up to 7k. The suggested value for R2 is 6.19k. The NFB pin is normally left open for positive output applications.

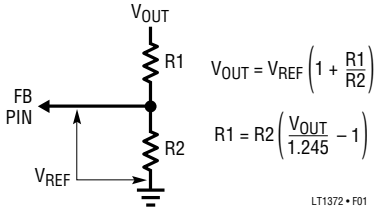


Figure 1. Positive Output Resistor Divider

APPLICATIONS INFORMATION

Positive fixed voltage versions are available (consult Linear Technology marketing).

Negative Output Voltage Setting

The LT1372/LT1377 develops a –2.49V reference (V_{NFR}) from the NFB pin to ground. Output voltage is set by connecting the NFB pin to an output resistor divider (Figure 2). The –30µA NFB pin bias current (I_{NFB}) can cause output voltage errors and should not be ignored. This has been accounted for in the formula in Figure 2. The suggested value for R2 is 2.49k. The FB pin is normally left open for negative output application. See Dual Polarity Output Voltage Sensing for limitatins on FB pin loading when using the NFB pin.

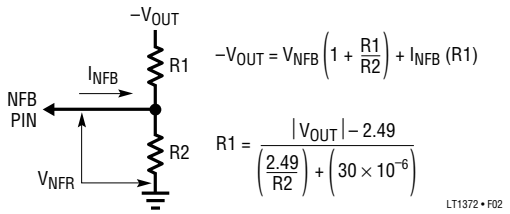


Figure 2. Negative Output Resistor Divider

Dual Polarity Output Voltage Sensing

Certain applications benefit from sensing both positive and negative output voltages. One example is the "Dual Output Flyback Converter with Overvoltage Protection" circuit shown in the Typical Applications section. Each output voltage resistor divider is individually set as described above. When both the FB and NFB pins are used, the LT1372/LT1377 acts to prevent either output from going beyond its set output voltage. For example in this application, if the positive output were more heavily loaded than the negative, the negative output would be greater and would regulate at the desired set-point voltage. The positive output would sag slightly below its set-point voltage. This technique prevents either output from going unregulated high at no load. Please note that the load on the FB pin should not exceed 250µA when the NFB pin is used. This situation occurs when the resistor dividers are used at *both* FB and NFB. True load on FB is not the full divider current unless the positive output is shorted to ground. See Dual Output Flyback Converter application.

Shutdown and Synchronization

The dual function S/S pin provides easy shutdown and synchronization. It is logic level compatible and can be pulled high, tied to V_{IN} or left floating for normal operation. A logic low on the S/S pin activates shutdown, reducing the part's supply current to 12µA. Typical synchronization range is from 1.05 to 1.8 times the part's natural switching frequency, but is only guaranteed between 600kHz and 800kHz (LT1372) or 1.2MHz and 1.6MHz (LT1377). At start-up, the synchronization signal should not be applied until the feedback pin is above the frequency shift voltage of 0.7V. If the NFB pin is used, synchronization should not be applied until the NFB pin is more negative than –1.4V. A 12µs resetable shutdown delay network guarantees the part will not go into shutdown while receiving a synchronization signal.

Caution should be used when synchronizing above 700kHz (LT1372) or 1.4MHz (LT1377) because at higher sync frequencies the amplitude of the internal slope compensation used to prevent subharmonic switching is reduced. This type of subharmonic switching only occurs when the duty cycle of the switch is above 50%. Higher inductor values will tend to eliminate problems.

Thermal Considerations

Care should be taken to ensure that the worst-case input voltage and load current conditions do not cause excessive die temperatures. The packages are rated at 120°C/W for SO (S8) and 130°C/W for PDIP (N8).

Average supply current (including driver current) is:

$I_{IN} = 4mA + DC\ (I_{SW}/60 + I_{SW} \times 0.004)$

I_{SW} = switch current

DC = switch duty cycle

Switch power dissipation is given by:

$P_{SW} = (I_{SW})^2 \times R_{SW} \times DC$

R_{SW} = output switch "On" resistance

Total power dissipation of the die is the sum of supply current times supply voltage plus switch power:

$P_{D(TOTAL)} = (I_{IN} \times V_{IN}) + P_{SW}$

APPLICATIONS INFORMATION

Choosing the Inductor

For most applications the inductor will fall in the range of 2.2µH to 22µH. Lower values are chosen to reduce physical size of the inductor. Higher values allow more output current because they reduce peak current seen by the power switch, which has a 1.5A limit. Higher values also reduce input ripple voltage and reduce core loss.

When choosing an inductor you might have to consider maximum load current, core and copper losses, allowable component height, output voltage ripple, EMI, fault current in the inductor, saturation, and of course, cost. The following procedure is suggested as a way of handling these somewhat complicated and conflicting requirements.

1. Assume that the average inductor current for a boost converter is equal to load current times V_{OUT}/V_{IN} and decide whether or not the inductor must withstand continuous overload conditions. If average inductor current at maximum load current is 0.5A, for instance, a 0.5A inductor may not survive a continuous 1.5A overload condition. Also be aware that boost converters are not short circuit protected, and that under output short conditions, inductor current is limited only by the available current of the input supply.
2. Calculate peak inductor current at full load current to ensure that the inductor will not saturate. Peak current can be significantly higher than output current, especially with smaller inductors and lighter loads, so don't omit this step. Powdered iron cores are forgiving because they saturate softly, whereas ferrite cores saturate abruptly. Other core materials fall in between somewhere. The following formula assumes continuous mode operation but it errors only slightly on the high side for discontinuous mode, so it can be used for all conditions.

$$I_{PEAK} = I_{OUT} \times \frac{V_{OUT}}{V_{IN}} + \frac{V_{IN}(V_{OUT} - V_{IN})}{2(f)(L)(V_{OUT})}$$

   V_{IN} = Minimum Input Voltage
   f = 500kHz Switching Frequency (LT1372) or
   1MHz Switching Frequency (LT1377)

3. Decide if the design can tolerate an "open" core geometry like a rod or barrel, which have high magnetic field radiation, or whether it needs a closed core like a toroid to prevent EMI problems. One would not want an open core next to a magnetic storage media for instance! This is a tough decision because the rods or barrels are temptingly cheap and small, and there are no helpful guidelines to calculate when the magnetic field radiation will be a problem.
4. Start shopping for an inductor which meets the requirements of core shape, peak current (to avoid saturation), average current (to limit heating) and fault current. If the inductor gets too hot, wire insulation will melt and cause turn-to-turn shorts. Keep in mind that all good things like high efficiency, low profile and high temperature operation will increase cost, sometimes dramatically.
5. After making an initial choice, consider the secondary things like output voltage ripple, second sourcing, etc. Use the experts in the Linear Technology application department if you feel uncertain about the final choice. They have experience with a wide range of inductor types and can tell you about the latest developments in low profile, surface mounting, etc.

Output Capacitor

The output capacitor is normally chosen by its effective series resistance, (ESR), because this is what determines output ripple voltage. At 500kHz, any polarized capacitor is essentially resistive. To get low ESR takes *volume*, so physically smaller capacitors have high ESR. The ESR range for typical LT1372 and LT1377 applications is 0.05Ω to 0.5Ω. A typical output capacitor is an AVX type TPS, 22µF at 25V, with a guaranteed ESR less than 0.2Ω. This is a "D" size surface mount solid tantalum capacitor. TPS capacitors are specially constructed and tested for low ESR, so they give the lowest ESR for a given volume. To further reduce ESR, multiple output capacitors can be used in parallel. The value in microfarads is not particularly critical, and values from 22µF to greater than 500µF work well, but you cannot cheat mother nature on ESR. If you find a tiny 22µF solid tantalum capacitor, it will have high ESR, and output ripple voltage will be terrible. Table 1 shows some typical solid tantalum surface mount capacitors.

APPLICATIONS INFORMATION

Table 1. Surface Mount Solid Tantalum Capacitor ESR and Ripple Current

E CASE SIZE	ESR (MAX Ω)	RIPPLE CURRENT (A)
AVX TPS, Sprague 593D	0.1 to 0.3	0.7 to 1.1
AVX TAJ	0.7 to 0.9	0.4
D CASE SIZE		
AVX TPS, Sprague 593D	0.1 to 0.3	0.7 to 1.1
AVX TAJ	0.9 to 2.0	0.36 to 0.24
C CASE SIZE		
AVX TPS	0.2 (Typ)	0.5 (Typ)
AVX TAJ	1.8 to 3.0	0.22 to 0.17
B CASE SIZE		
AVX TAJ	2.5 to 10	0.16 to 0.08

Many engineers have heard that solid tantalum capacitors are prone to failure if they undergo high surge currents. This is historically true and type TPS capacitors are specially tested for surge capability, but surge ruggedness is not a critical issue with the *output* capacitor. Solid tantalum capacitors fail during very high *turn-on* surges, which do not occur at the output of regulators. High *discharge* surges, such as when the regulator output is dead shorted, do not harm the capacitors.

Single inductor boost regulators have large RMS ripple current in the output capacitor, which must be rated to handle the current. The formula to calculate this is:

Output Capacitor Ripple Current (RMS)

$$I_{RIPPLE}\ (RMS) = I_{OUT}\sqrt{\frac{DC}{1-DC}}$$

$$= I_{OUT}\sqrt{\frac{V_{OUT}-V_{IN}}{V_{IN}}}$$

Input Capacitors

The input capacitor of a boost converter is less critical due to the fact that the input current waveform is triangular and does not contain large squarewave currents as is found in the output capacitor. Capacitors in the range of 10µF to 100µF with an ESR of 0.3Ω or less work well up to full 1.5A switch current. Higher ESR capacitors may be acceptable at low switch currents. Input capacitor ripple current for boost converter is :

$$I_{RIPPLE} = \frac{0.3(V_{IN})(V_{OUT}-V_{IN})}{(f)(L)(V_{OUT})}$$

f = 500kHz Switching frequency (LT1372) or,
1MHz Switching frequency (LT1377)

The input capacitor can see a very high surge current when a battery or high capacitance source is connected "live" and solid tantalum capacitors can fail under this condition. Several manufacturers have developed a line of solid tantalum capacitors specially tested for surge capability (AVX TPS series, for instance), but even these units may fail if the input voltage approaches the maximum voltage rating of the capacitor. AVX recommends derating capacitor voltage by 2:1 for high surge applications. Ceramic and aluminum electrolytic capacitors may also be used and have a high tolerance to turn-on surges.

Ceramic Capacitors

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. These are tempting for switching regulator use because of their very low ESR. Unfortunately, the ESR is so low that it can cause loop stability problems. Solid tantalum capacitor ESR generates a loop "zero" at 5kHz to 50kHz that is instrumental in giving acceptable loop phase margin. Ceramic capacitors remain capacitive to beyond 300kHz and usually resonate with their ESL before ESR becomes effective. They are appropriate for input bypassing because of their high ripple current ratings and tolerance of turn-on surges. Linear Technology plans to issue a Design Note on the use of ceramic capacitors in the near future.

Output Diode

The suggested output diode (D1) is a 1N5818 Schottky or its Motorola equivalent, MBR130. It is rated at 1A average forward current and 30V reverse voltage. Typical forward voltage is 0.42V at 1A. The diode conducts current only during switch off time. Peak reverse voltage for boost converters is equal to regulator output voltage. Average forward current in normal operation is equal to output current.

APPLICATIONS INFORMATION

Frequency Compensation

Loop frequency compensation is performed on the output of the error amplifier (V_C pin) with a series RC network. The main pole is formed by the series capacitor and the output impedance (≈500kΩ) of the error amplifier. The pole falls in the range of 2Hz to 20Hz. The series resistor creates a "zero" at 1kHz to 5kHz, which improves loop stability and transient response. A second capacitor, typically one-tenth the size of the main compensation capacitor, is sometimes used to reduce the switching frequency ripple on the V_C pin. V_C pin ripple is caused by output voltage ripple attenuated by the output divider and multiplied by the error amplifier. Without the second capacitor, V_C pin ripple is:

$$V_C \text{ Pin Ripple} = \frac{1.245(V_{RIPPLE})(g_m)(R_C)}{(V_{OUT})}$$

V_{RIPPLE} = Output ripple (V_{P-P})
g_m = Error amplifier transconductance (≈1500μmho)
R_C = Series resistor on V_C pin
V_{OUT} = DC output voltage

To prevent irregular switching, V_C pin ripple should be kept below $50mV_{P-P}$. Worst-case V_C pin ripple occurs at maximum output load current and will also be increased if poor quality (high ESR) output capacitors are used. The addition of a 0.0047μF capacitor on the V_C pin reduces switching frequency ripple to only a few millivolts. A low value for R_C will also reduce V_C pin ripple, but loop phase margin may be inadequate.

Switch Node Considerations

For maximum efficiency, switch rise and fall time are made as short as possible. To prevent radiation and high frequency resonance problems, proper layout of the components connected to the switch node is essential. B field (magnetic) radiation is minimized by keeping output diode, switch pin, and output bypass capacitor leads as short as possible. E field radiation is kept low by minimizing the length and area of all traces connected to the switch pin. A ground plane should always be used under the switcher circuitry to prevent interplane coupling.

The high speed switching current path is shown schematically in Figure 3. Minimum lead length in this path is essential to ensure clean switching and low EMI. The path including the switch, output diode, and output capacitor is the only one containing nanosecond rise and fall times. Keep this path as short as possible.

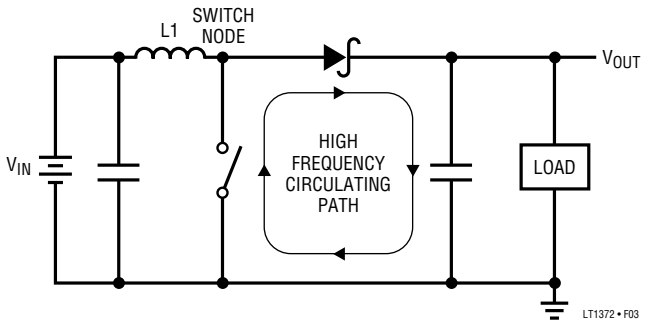


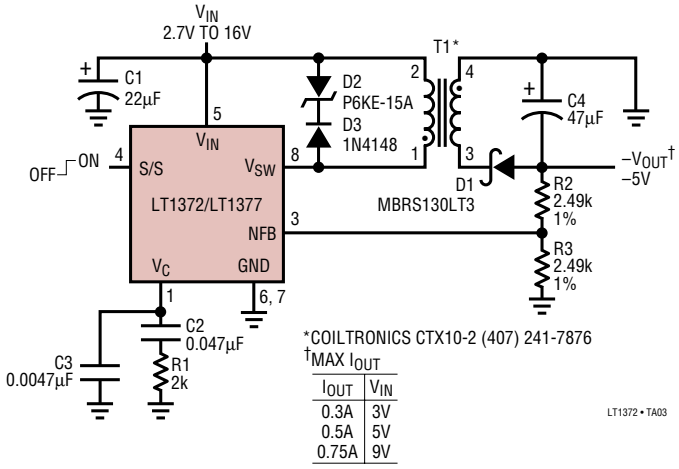
Figure 3

More Help

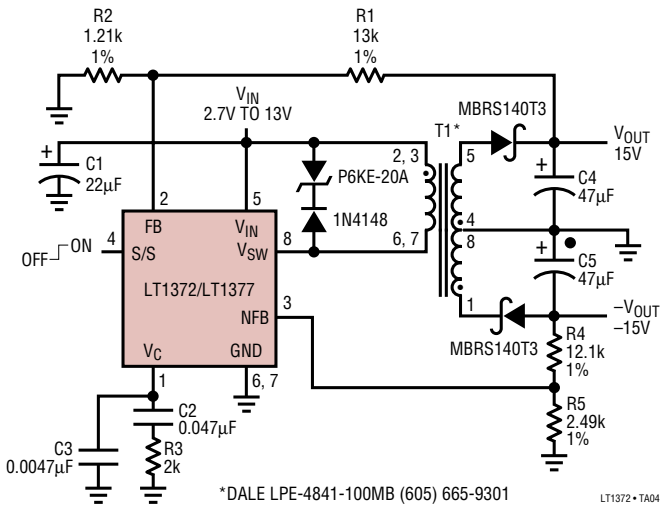
For more detailed information on switching regulator circuits, please see Application Note 19. Linear Technology also offers a computer software program, SwitcherCAD, to assist in designing switching converters. In addition, our applications department is always ready to lend a helping hand.

TYPICAL APPLICATIONS

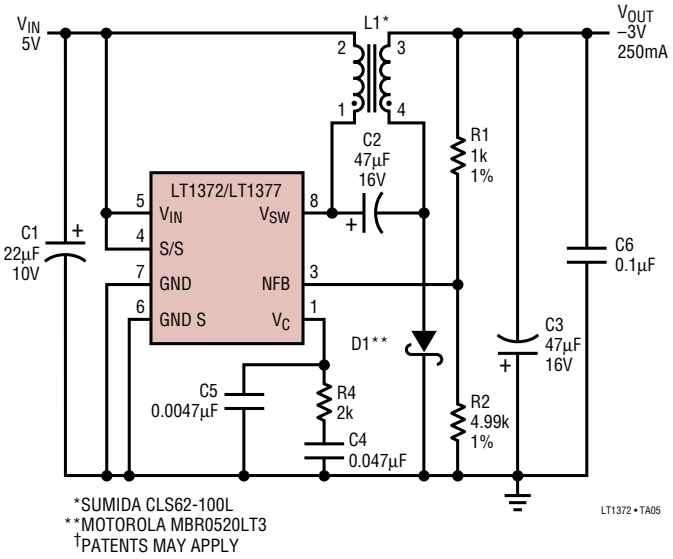
Positive-to-Negative Converter with Direct Feedback



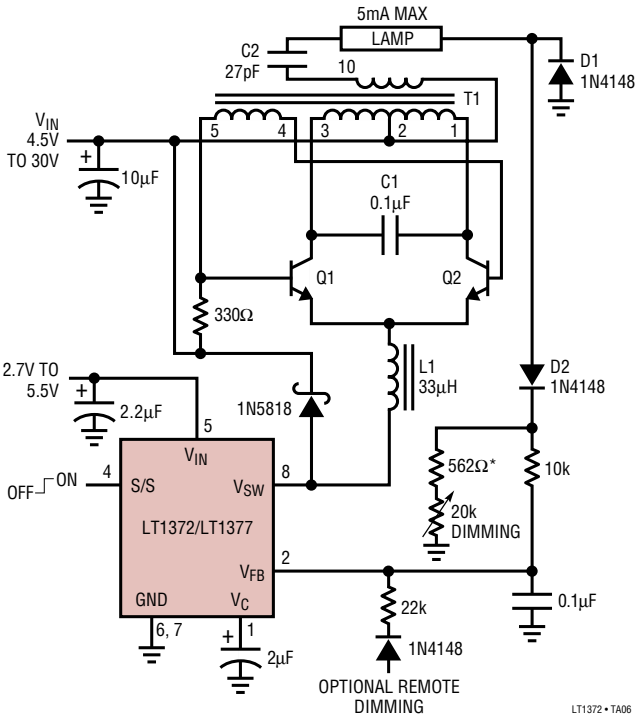
Dual Output Flyback Converter with Overvoltage Protection



Low Ripple 5V to –3V "Cuk"† Converter



90% Efficient CCFL Supply



C1 = WIMA MKP-20
L1 = COILCRAFT DT3316-333
Q1, Q2 = ZETEX ZTX849 OR ROHM 2SC5001
T1 = COILTRONICS CTX 110609
* = 1% FILM RESISTOR

DO NOT SUBSTITUTE COMPONENTS

COILTRONICS (407) 241-7876
COILCRAFT (708) 639-6400

CCFL BACKLIGHT APPLICATION CIRCUITS CONTAINED IN THIS DATA SHEET ARE COVERED BY U.S. PATENT NUMBER 5408162 AND OTHER PATENTS PENDING