Isolated No-Opto Synchronous Flyback Controller

FEATURES

- **Senses Output Voltage Directly from Primary Side Winding—No Optoisolator Required**
- **Synchronous Driver for High Efficiency**
- **Supply Voltage Range 4.5V to 20V**
- Accurate Regulation Without User Trims
- Programmable Switching Frequency from 50kHz to 250kHz
- Synchronizable
- Load Compensation
- Undervoltage Lockout
- Available in a Thermally Enhanced 16-Lead TSSOP Package

APPLICATIONS

- Isolated Medium Power (10W to 60W) Supplies
- Instrumentation Power Supplies
- Isolated Medical Supplies

DESCRIPTION

The LT®3837 is an isolated switching regulator controller designed for medium power flyback topologies. A typical application is 10W to 60W with the part powered from a DC supply.

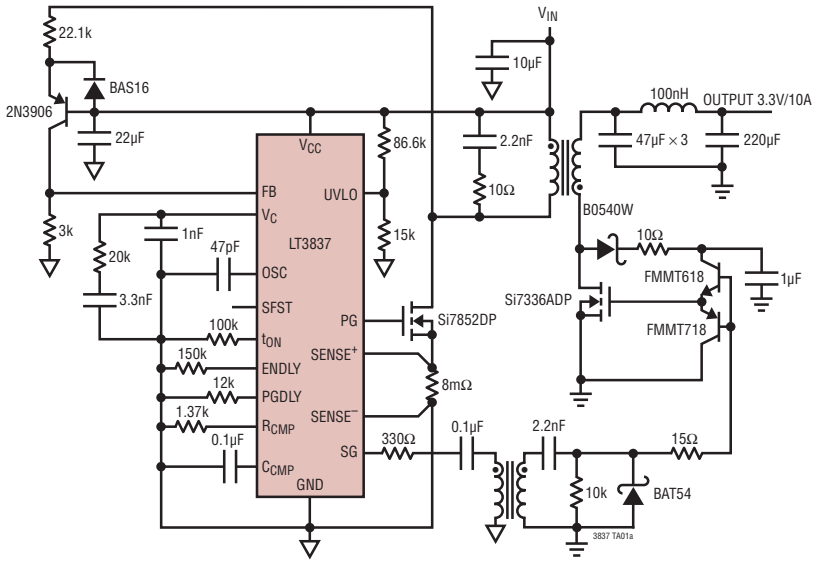
The LT3837 is a current mode controller that regulates an output voltage based on sensing the secondary voltage via a transformer winding during flyback. This allows for tight output regulation without the use of an optoisolator, improving dynamic response and reliability. Synchronous rectification increases converter efficiency and improves output cross regulation in multiple output converters.

The LT3837 operates in forced continuous conduction mode which improves cross regulation in multiple winding applications. Switching frequency is user programmable and can be externally synchronized. The part also has load compensation, undervoltage lockout and soft-start circuitry.

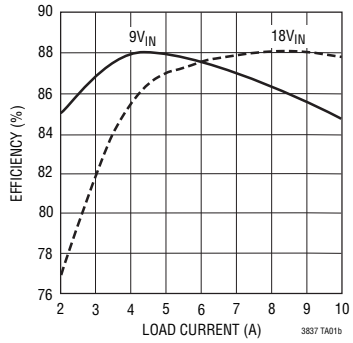
The LT3837 is available in a thermally enhanced 16-pin TSSOP package.

TYPICAL APPLICATION

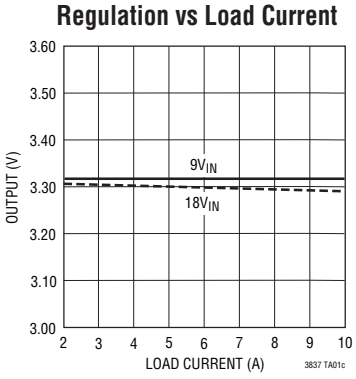
9V –18V to 3.3V at 10A Isolated Converter



Efficiency vs Load Current



Regulation vs Load Current

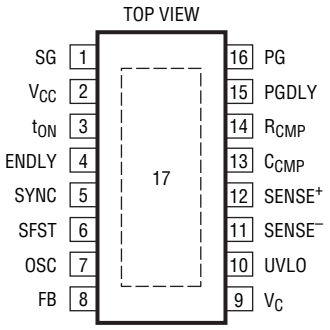


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC} to GND ..... –0.3V to 22V
UVLO, SYNC Pin Voltage ..... –0.3V to V_{CC}
$SENSE^-$, $SENSE^+$ Pin Voltage..... –0.5V, +0.5V
FB Pin Current..... ±2mA
V_C Pin Current..... ±1mA
Operating Junction Temperature Range
(Notes 2, 3, 4)..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)..... 300°C

PIN CONFIGURATION



FE PACKAGE
16-LEAD PLASTIC TSSOP

T_{JMAX} = 125°C, θ_{JA} = 40°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 17) IS GND,MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3837EFE#PBF	LT3837EFE#TRPBF	3837EFE	16-Lead Plastic TSSOP	–40°C to 125°C
LT3837IFE#PBF	LT3837IFE#TRPBF	3837FE	16-Lead Plastic TSSOP	–40°C to 125°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING**	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LT3837EFE	LT3837EFE#TR	3837EFE	16-Lead Plastic TSSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating junction temperature range, otherwise specifications are T_A = 25°C. V_{CC} = 14V; PG, SG Open; V_C = 1.4V, V_{SENSE} = 0, R_{CMP} = 1k, R_{TON} = 90k, R_{PGDLY} = 27.4k, R_{ENDLY} = 90k, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply						
V_{CC} Operating Range		●	4.5		20	V
V_{CC} Supply Current (I_{CC}) (Note 5)	V_C = Open	●	4	6.4	10	mA
V_{CC} Shutdown Current	V_C = Open, V_{UVLO} = OV	●		50	150	µA
Feedback Amplifier						
Feedback Regulation Voltage (V_{FB})		●	1.220	1.237	1.251	V
Feedback Pin Input Bias Current	R_{CMP} Open			200		nA
Feedback Amplifier Transconductance	ΔI_C = ±10µA	●	700	1000	1400	µmho
Feedback Amplifier Source or Sink Current		●	25	55	90	µA
Feedback Amplifier Clamp Voltage	V_{FB} = 0.9 V_{FB} = 1.4			2.56 0.84		V V
Reference Voltage Line Regulation	12V ≤ V_{IN} ≤ 18V	●		0.005	0.05	%V

ELECTRICAL CHARACTERISTICS

The ● denotes specifications which apply over the full operating junction temperature range, otherwise specifications are T_A = 25°C. V_{CC} = 14V; PG, SG Open; V_C = 1.4V, V_{SENSE} = 0, R_{CMP} = 1k, R_{TON} = 90k, R_{PGDLY} = 27.4k, R_{ENDLY} = 90k, unless otherwise specified.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Feedback Amplifier Voltage Gain	V_C = 1.2V to 1.7V			1400		V/V
Soft-Start Charging Current	V_{SFST} = 1.5V		16	20	25	µA
Soft-Start Discharge Current	V_{SFST} = 1.5V, V_{UVLO} = 0V		0.7	1.3		mA
Control Pin Threshold (V_C)	Duty Cycle = Min			1.0		V
Gate Outputs						
PG, SG Output High Level PG, SG Output Low Level		● ●	6.6	7.4 0.01	8.0 0.05	V V
PG, SG Output Shutdown Strength	V_{UVLO} = 0V; I_{PG}, I_{SG} = 20mA	●		1.6	2.3	V
PG Rise Time	C_{PG} = 1nF			11		ns
SG Rise Time	C_{SG} = 1nF			15		ns
PG, SG Fall Time	C_{PG}, C_{SG} = 1nF			10		ns
Current Amplifier						
Switch Current Limit at Maximum V_C	V_{SENSE} +	●	88	98	110	mV
$\Delta V_{SENSE}/\Delta V_C$				0.07		V/V
Sense Voltage Overcurrent Fault Voltage	V_{SENSE} +			206	230	mV
Timing						
Switching Frequency (f_{OSC})	C_{OSC} = 100pF	●	84	100	110	kHz
Oscillator Capacitor Value (C_{OSC})	(Note 6)		33		200	pF
Minimum Switch On Time ($t_{ON(MIN)}$)				200		ns
Flyback Enable Delay Time (t_{ED})				265		ns
PG Turn-On Delay Time (t_{PGDLY})				200		ns
Maximum Switch Duty Cycle		●	85	88		%
SYNC Pin Threshold		●		1.53	2.1	V
SYNC Pin Input Resistance				40		kΩ
Load Compensation						
Load Comp to V_{SENSE} Offset Voltage	V_{RCMP} with V_{SENSE+} = 0			0.8		mV
Feedback Pin Load Compensation Current	V_{SENSE}+ = 20mV			20		µA
UVLO Function						
UVLO Pin Threshold (V_{UVLO})		●	1.215	1.240	1.265	V
UVLO Pin Bias Current	V_{UVLO} = 1.2V V_{UVLO} = 1.3V		–0.25 –4.50	0.1 –3.4	0.25 –2.50	µA µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 3: The LT3837E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3837I is guaranteed to meet performance specifications over the full –40°C to 125°C operating junction temperature range.

Note 4: T_J is calculated from the ambient temperature T_A and power dissipation PD according to the following formula:

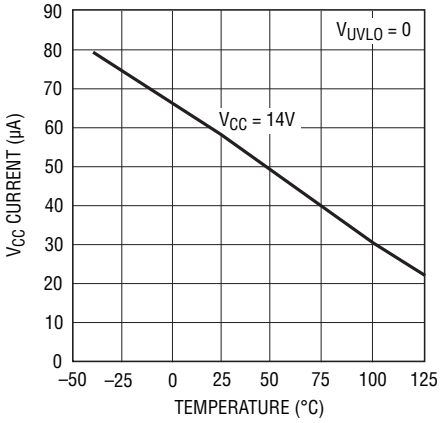
$$T_J = T_A + (P_D \bullet 40°C/W)$$

Note 5: Supply current does not include gate charge current to the MOSFETs. See the Applications Information section.

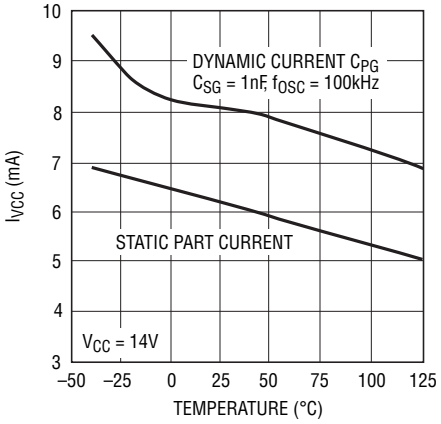
Note 6: Component value range guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

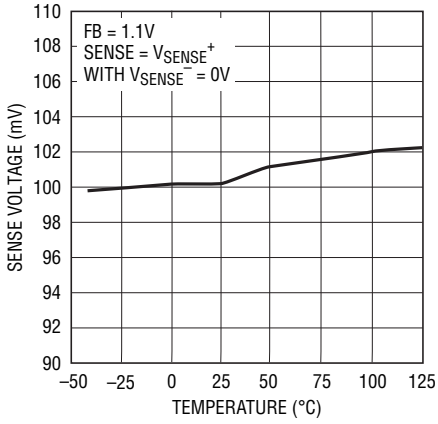
V_{CC} Shutdown Current vs Temperature



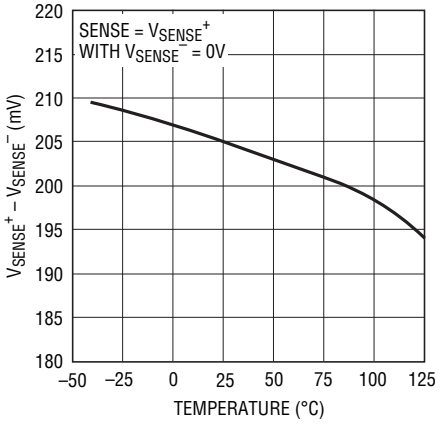
V_{CC} Current vs Temperature



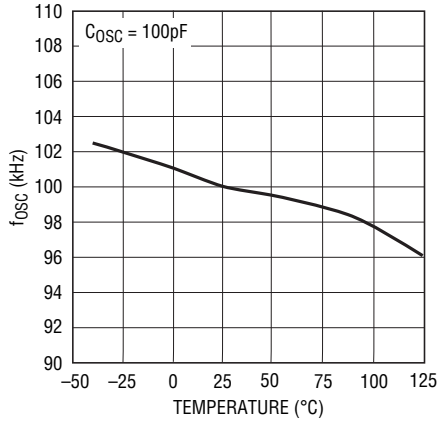
SENSE Voltage vs Temperature



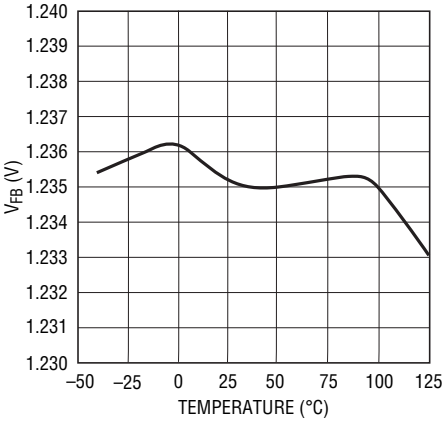
SENSE Fault Voltage vs Temperature



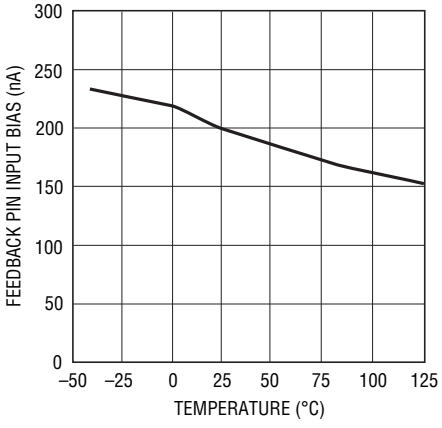
Oscillator Frequency vs Temperature



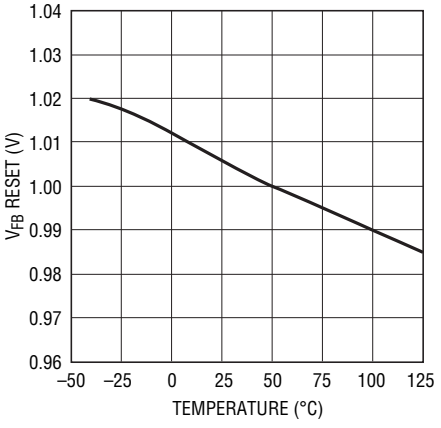
V_{FB} vs Temperature



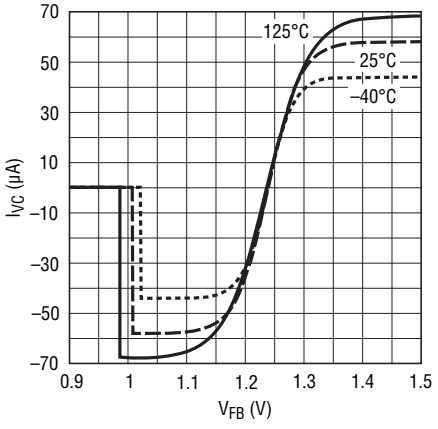
Feedback Pin Input Bias vs Temperature



V_{FB} Reset vs Temperature

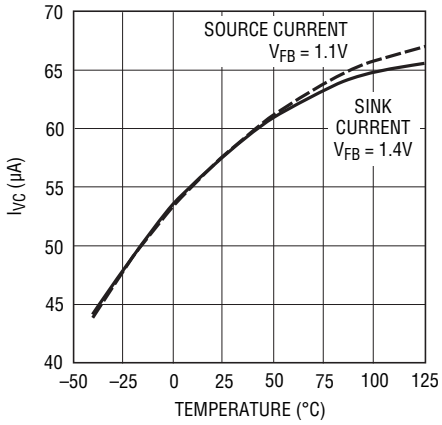


Feedback Amplifier Output Current vs V_{FB}

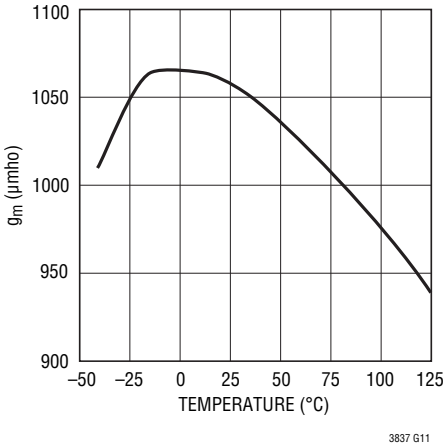


TYPICAL PERFORMANCE CHARACTERISTICS

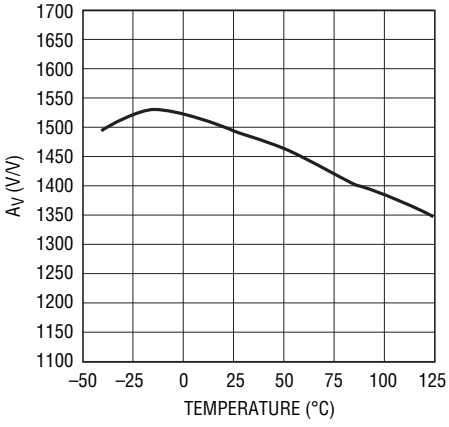
Feedback Amplifier Source and Sink Current vs Temperature



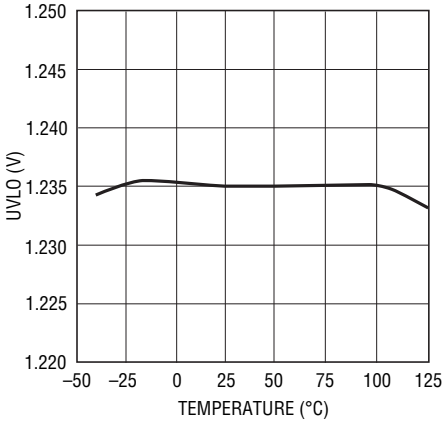
Feedback Amplifier g_m vs Temperature



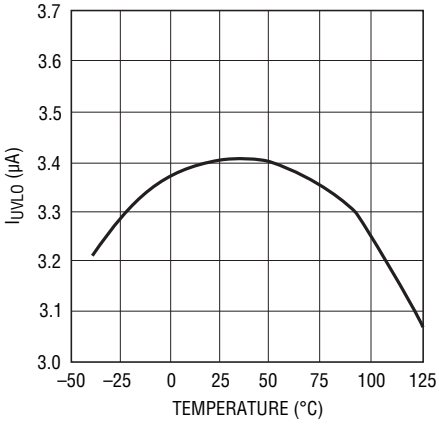
Feedback Amplifier Voltage Gain vs Temperature



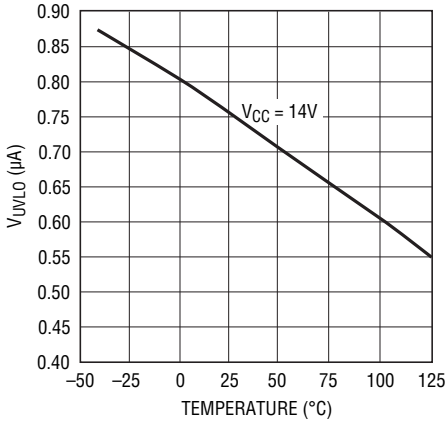
UVLO vs Temperature



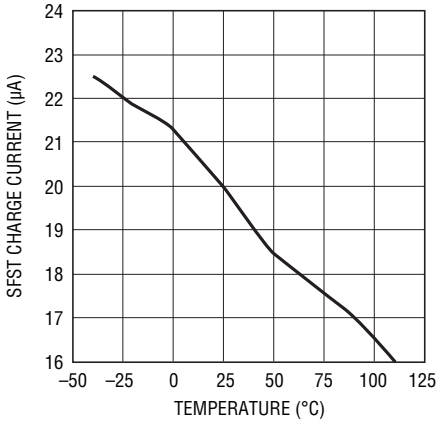
I_{UVLO} Hysteresis vs Temperature



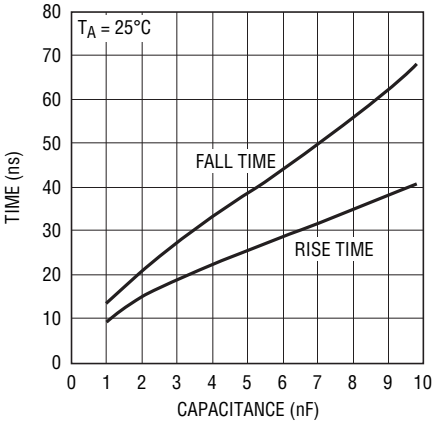
UVLO Shutdown Threshold vs Temperature



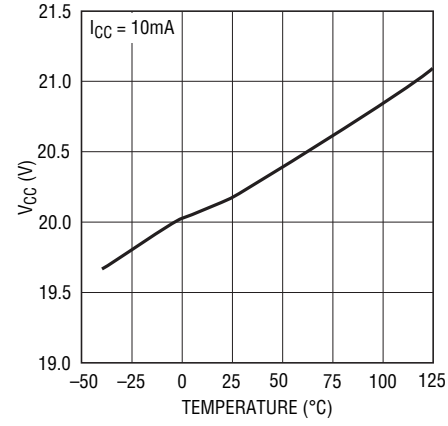
Soft-Start Charge Current vs Temperature



PG, SG Rise and Fall Times vs Load Capacitance

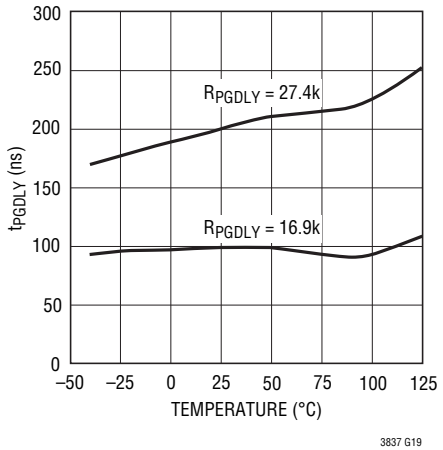


Minimum On-Time vs Temperature

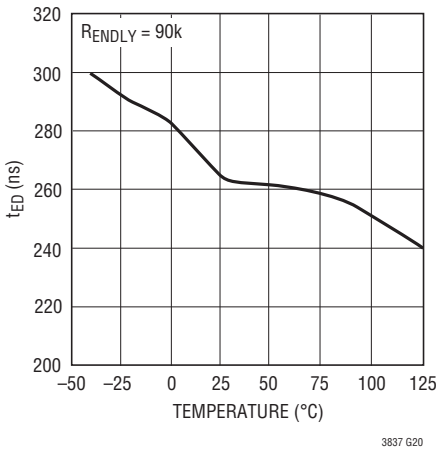


TYPICAL PERFORMANCE CHARACTERISTICS

PG Delay Time vs Temperature



Enable Delay Time vs Temperature



PIN FUNCTIONS

SG (Pin 1): Synchronous gate drive output. This pin provides an output signal for a secondary-side synchronous switch. Large dynamic currents may flow during voltage transitions. See the Applications Information section for details.

V_{CC} (Pin 2): Supply voltage pin. Bypass this pin to ground with a 4.7µF capacitor or more.

t_{ON} (Pin 3): Pin for external programming resistor to set the minimum time that the primary switch is on for each cycle. Minimum turn-on facilitates the isolated feedback method. See the Applications Information section for details.

ENDLY (Pin 4): Pin for external programming resistor to set enable delay time. The enable delay time disables the feedback amplifier for a fixed time after the turn-off of the primary-side MOSFET. This allows the leakage inductance voltage spike to be ignored for flyback voltage sensing. See the Applications Information section for details.

SYNC (Pin 5): Pin for synchronizing the internal oscillator with an external clock. The positive edge on a pulse causes the oscillator to discharge causing PG to go low (off) and SG high (on). The sync threshold is typically 1.53V. See the Applications Information section for details. Tie to ground if unused.

SFST (Pin 6): This pin, in conjunction with a capacitor to ground, controls the ramp-up of peak primary current as sensed through the sense resistor. This is used to control converter inrush current at start-up. The V_C pin voltage cannot exceed the SFST pin voltage, so as SFST increases, the maximum voltage on V_C increases commensurately, allowing higher peak currents. Total V_C ramp time is approximately 70ms per µF of capacitance. Leave pin open if not using the soft-start function.

OSC (Pin 7): This pin in conjunction with an external capacitor defines the controller oscillator frequency. The frequency is approximately 100kHz • $100/C_{OSC}$(pF).

FB (Pin 8): Pin for the feedback node for the power supply feedback amplifier. Feedback is sensed via a transformer winding and enabled during the flyback period. This pin also sinks additional current to compensate for load current variation as set by the R_{CMP} pin. Keep the Thevenin equivalent resistance of the feedback divider at roughly 3k.

PIN FUNCTIONS

V_C (Pin 9): Pin used for frequency compensation for the switcher control loop. It is the output of the feedback amplifier and the input to the current comparator. Switcher frequency compensation components are normally placed on this pin to ground. The voltage on this pin is proportional to the peak primary switch current. The feedback amplifier output is enabled during the synchronous switch on time.

UVLO (Pin 10): A resistive divider from V_{IN} to this pin sets an undervoltage lockout based upon V_{IN} level (not V_{CC}). When the UVLO pin is below its threshold, the gate drives are disabled, but the part draws its normal quiescent current from V_{CC}. The V_{CC} undervoltage lockout supersedes this function so V_{CC} must be great enough to start the part.

The bias current on this pin has hysteresis such that the bias current is sourced when the UVLO threshold is exceeded. This introduces a hysteresis at the pin equivalent to the bias current change times the impedance of the upper divider resistor. The user can control the amount of hysteresis by adjusting the impedance of the divider. See the Applications Information section for details. Tie the UVLO pin to V_{CC} if you are not using this function.

$SENSE^-$ (Pin 11), $SENSE^+$ (Pin 12): These pins are used to measure primary side switch current through an external sense resistor. Peak primary side current is used in the converter control loop. Make Kelvin connections to the sense resistor to reduce noise problems. $SENSE^-$ connects to the ground side. At maximum current (V_C at its maximum voltage) it has a 98mV threshold. The signal is blanked (ignored) during the minimum turn-on time.

C_{CMP} (Pin 13): Pin for external filter capacitor for the optional load compensation function. Load compensation reduces the effects of parasitic resistances in the feedback sensing path. A 0.1µF ceramic capacitor suffices for most applications. Short this pin to GND in less demanding applications that don't require load compensation.

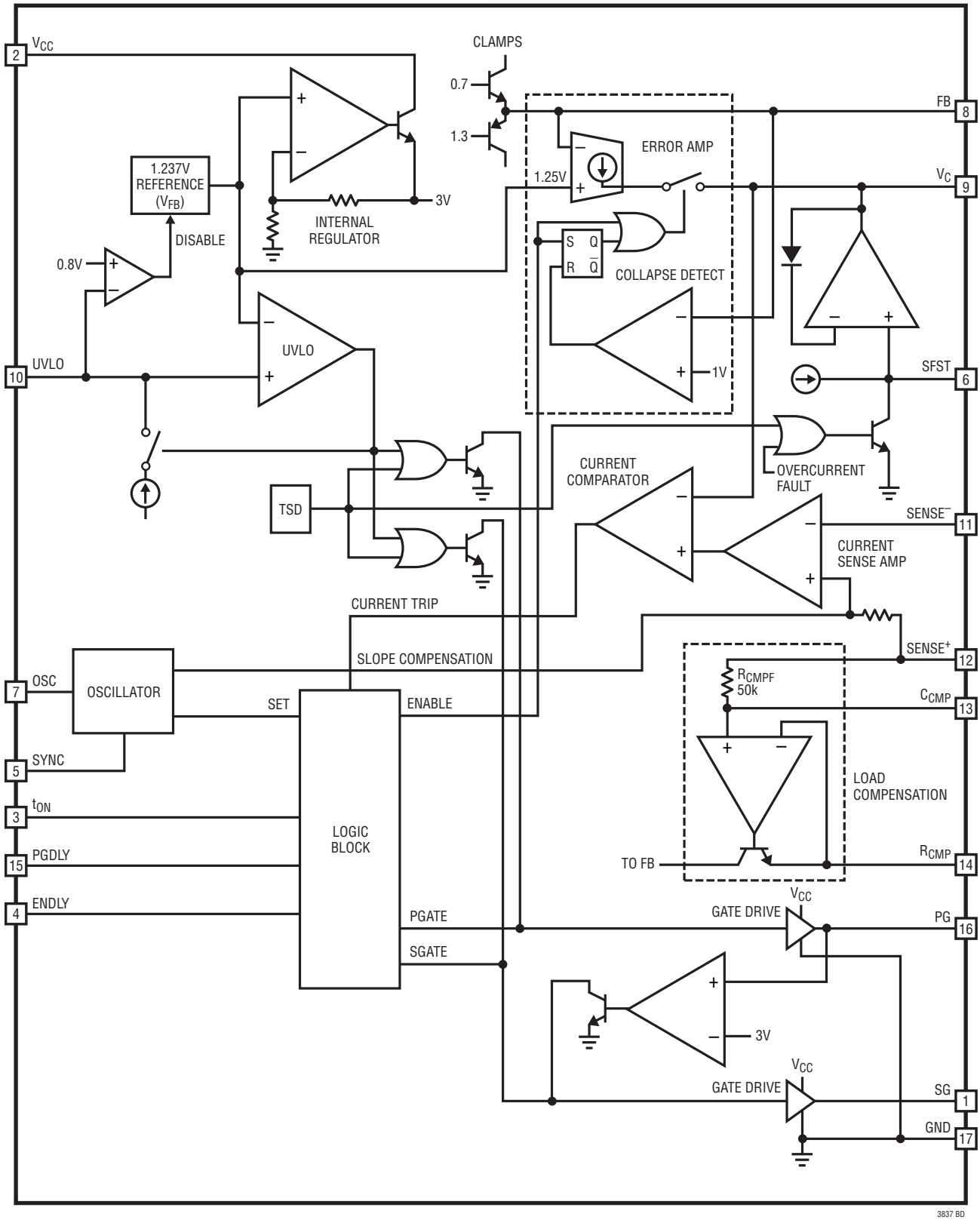
R_{CMP} (Pin 14): Pin for optional external load compensation resistor. Use of this pin allows for nominal compensation of parasitic resistances in the feedback sensing path. In less demanding applications, this resistor is not needed and this pin can be left open. See the Applications Information section for details.

PGDLY (Pin 15): Pin for external programming resistor to set delay from synchronous gate turn-off to primary gate turn-on. See the Applications Information section for details.

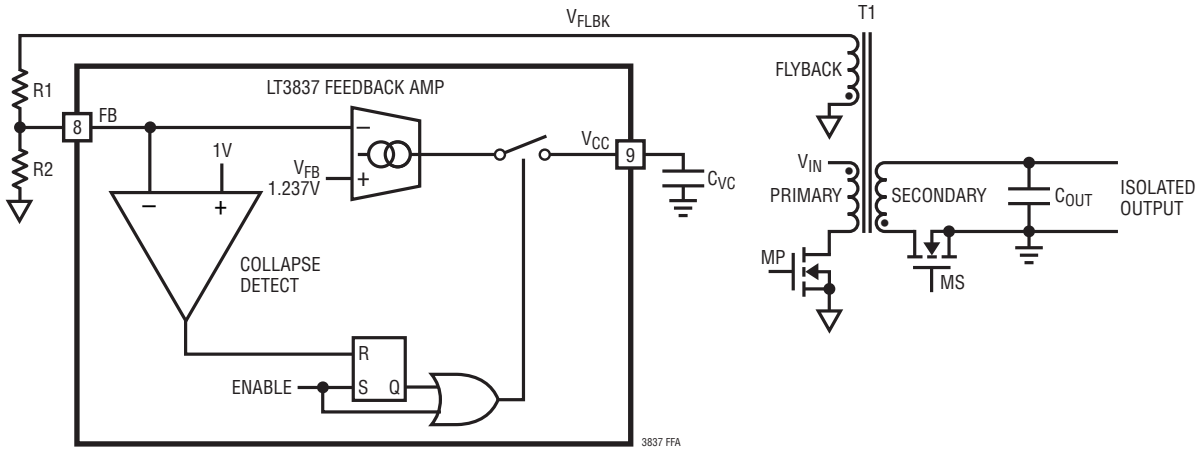
PG (Pin 16): Gate drive pin for the primary side MOSFET Switch. Large dynamic currents flow during voltage transitions. See the Applications Information section for details.

GND (Exposed Pad Pin 17): This is the ground connection for both signal ground and gate driver grounds. This GND should be connected to the PCB ground plane for electrical contact and rated thermal performance. Careful attention must be paid to ground layout. See the Applications Information section for details.

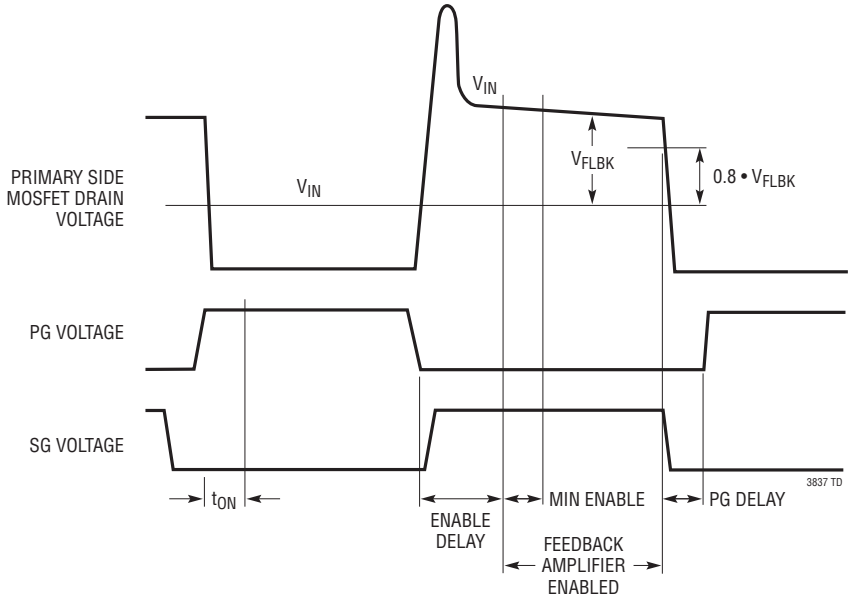
BLOCK DIAGRAM



FLYBACK FEEDBACK AMPLIFIER



TIMING DIAGRAM



OPERATION

The LT3837 is a current mode switcher controller IC designed specifically for use in an isolated flyback topology employing synchronous rectification. The LT3837 operation is similar to traditional current mode switchers. The major difference is that output voltage feedback is derived via sensing the output voltage through the transformer. This precludes the need of an optoisolator in isolated designs greatly improving dynamic response and reliability. The LT3837 has a unique feedback amplifier that samples a transformer winding voltage during the flyback period and uses that voltage to control output voltage.

The internal blocks are similar to many current mode controllers. The differences lie in the flyback feedback amplifier and load compensation circuitry. The logic block also contains circuitry to control the special dynamic requirements of flyback control.

See Application Note 19 for more information on the basics of current mode switcher/controllers and isolated flyback converters.

Feedback Amplifier—Pseudo DC Theory

For the following discussion refer to the simplified Flyback Feedback Amplifier diagram. When the primary side MOSFET switch MP turns off, its drain voltage rises above the V_{IN} rail. Flyback occurs when the primary MOSFET is off and the synchronous secondary MOSFET is on. During flyback the voltage on nondriven transformer pins is determined by the secondary voltage. The amplitude of this flyback pulse as seen on the third winding is given as:

$$V_{FLBK} = \frac{V_{OUT} + I_{SEC} \bullet \left(ESR + R_{DS(ON)}\right)}{N_{SF}}$$

$R_{DS(ON)}$ = on resistance of the synchronous MOSFET M_S

I_{SEC} = transformer secondary current

ESR = impedance of secondary circuit capacitor, winding and traces

N_{SF} = transformer effective secondary-to-feedback winding turns ratio (i.e., N_S/N_{FLBK})

The flyback voltage is then scaled by an external resistive divider R1/R2 and presented at the FB pin. The feedback amplifier then compares the voltage to the internal bandgap reference. The feedback amp is actually a transconductance amplifier whose output is connected to V_C only during a period in the flyback time. An external capacitor on the V_C pin integrates the net feedback amp current to provide the control voltage to set the current mode trip point.

The regulation voltage at the FB pin is nearly equal to the bandgap reference V_{FB} because of the high gain in the overall loop. The relationship between V_{FLBK} and V_{FB} is expressed as:

$$V_{FLBK} = \frac{R1+R2}{R2} \bullet V_{FB}$$

Combining this with the previous V_{FLBK} expression yields an expression for V_{OUT} in terms of the internal reference, programming resistors and secondary resistances:

$$V_{OUT} = \left(\frac{R1+R2}{R2} \bullet V_{FB} \bullet N_{SF}\right) - I_{SEC} \bullet \left(ESR + R_{DS(ON)}\right)$$

Rearranging yields the equation for R1.

$$R1 = R2 \bullet \left[\frac{V_{OUT} + I_{SEC} \bullet \left(ESR + R_{DS(ON)}\right)}{\left(N_{SF}\right)\left(V_{FB}\right)} - 1\right]$$

The effect of nonzero secondary output impedance is discussed in further detail; see Load Compensation Theory. The practical aspects of applying this equation for V_{OUT} are found in the Applications Information section.

Feedback Amplifier Dynamic Theory

So far, this has been a pseudo-DC treatment of flyback feedback amplifier operation. But the flyback signal is a pulse, not a DC level. Provision must be made to enable the flyback amplifier only when the flyback pulse is present. This is accomplished by the “Enable” line in the diagram. Timing signals are then required to enable and disable the flyback amplifier. There are several timing signals which are required for proper LT3837 operation. Please refer to the Timing Diagram.

OPERATION

Minimum Output Switch On-Time ($t_{ON(MIN)}$)

The LT3837 affects output voltage regulation via flyback pulse action. If the output switch is not turned on, there is no flyback pulse and output voltage information is not available. This causes irregular loop response and start-up/latch-up problems. The solution is to require the primary switch to be on for an absolute minimum time per each oscillator cycle. If the output load is less than that developed under these conditions, forced continuous operation normally occurs. See the Applications Information section for further details.

Enable Delay (ENDLY)

The flyback pulse appears when the primary side switch shuts off. However, it takes a finite time until the transformer primary side voltage waveform represents the output voltage. This is partly due to rise time on the primary side MOSFET drain node but, more importantly, is due to transformer leakage inductance. The latter causes a voltage spike on the primary side, not directly related to output voltage. Some time is also required for internal settling of the feedback amplifier circuitry. In order to maintain immunity to these phenomena, a fixed delay is introduced between the switch turn-off command and the enabling of the feedback amplifier. This is termed "enable delay." In certain cases where the leakage spike is not sufficiently settled by the end of the enable delay period, regulation error may result. See the Applications Information section for further details.

Collapse Detect

Once the feedback amplifier is enabled, some mechanism is then required to disable it. This is accomplished by a collapse detect comparator, which compares the flyback voltage (FB referred) to a fixed reference, nominally 80% of V_{FB}. When the flyback waveform drops below this level, the feedback amplifier is disabled.

Minimum Enable Time

The feedback amplifier, once enabled, stays enabled for a fixed minimum time period termed "minimum enable time." This prevents lockup, especially when the output voltage is abnormally low; e.g., during start-up. The minimum enable time period ensures that the V_C node is able to pump up and increase the current mode trip point to the level where the collapse detect system exhibits proper operation. This time is internally set.

Effects of Variable Enable Period

The feedback amplifier is enabled during only a portion of the cycle time. This can vary from the fixed minimum enable time described to a maximum of roughly the "off" switch time minus the enable delay time. Certain parameters of flyback amp behavior are directly affected by the variable enable period. These include effective transconductance and V_C node slew rate.

Load Compensation Theory

The LT3837 uses the flyback pulse to obtain information about the isolated output voltage. An error source is caused by transformer secondary current flow through the synchronous MOSFET $R_{DS(ON)}$ and real life nonzero impedances of the transformer secondary and output capacitor. This was represented previously by the expression "I_{SEC} • (ESR + $R_{DS(ON)}$)." However, it is generally more useful to convert this expression to effective output impedance. Because the secondary current only flows during the off portion of the duty cycle (DC), the effective output impedance equals the lumped secondary impedance divided by OFF time DC.

Since the OFF time duty cycle is equal to 1 – DC then:

$$R_{S(OUT)} = \frac{ESR + R_{DS(ON)}}{1 - DC}$$

where:

$R_{S(OUT)}$ = effective supply output impedance

DC = duty cycle

$R_{DS(ON)}$ and ESR are as defined previously

This impedance error may be judged acceptable in less critical applications, or if the output load current remains relatively constant. In these cases the external FB resistive divider is adjusted to compensate for nominal expected error. In more demanding applications, output impedance error is minimized by the use of the load compensation function.

OPERATION

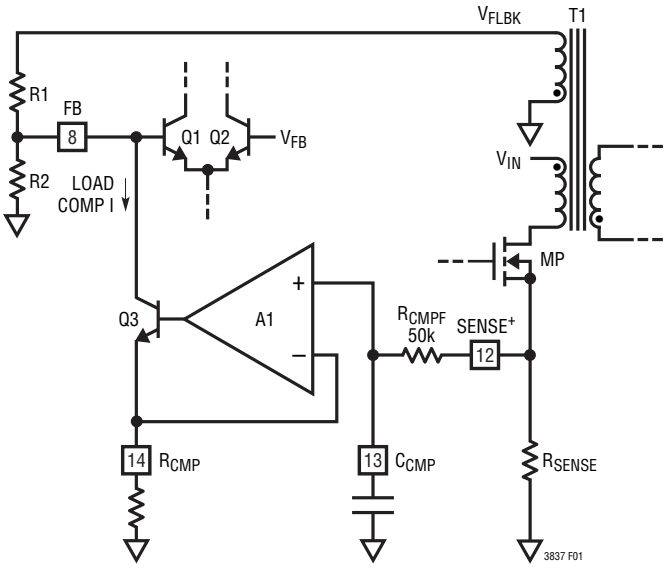


Figure 1. Load Compensation Diagram

Figure 1 shows the block diagram of the load compensation function. Switch current is converted to voltage by the external sense resistor, averaged and lowpass filtered by the internal 50k resistor R_{CMPF} and the external capacitor on C_{CMP}. This voltage is then impressed across the external R_{CMP} resistor by op amp A1 and transistor Q3. This produces a current at the collector of Q3 that is subtracted from the FB node. This action effectively increases the voltage required at the top of the R1/R2 feedback divider to achieve equilibrium.

The average primary side switch current increases to maintain output voltage regulation as output loading increases. The increase in average current increases the R_{CMP} resistor current which affects a corresponding increase in sensed output voltage, compensating for the IR drops.

Assuming a relatively fixed power supply efficiency, Eff, power balance gives:

$$P_{OUT} = Eff \bullet P_{IN}$$

$$V_{OUT} \bullet I_{OUT} = Eff \bullet V_{IN} \bullet I_{IN}$$

Average primary side current is expressed in terms of output current as follows:

$$I_{IN} = K1 \bullet I_{OUT}$$

where:

$$K1 = \frac{V_{OUT}}{V_{IN} \bullet Eff}$$

So the effective change in V_{OUT} target is:

$$\Delta V_{OUT} = K1 \bullet \Delta I_{OUT} \bullet \frac{R_{SENSE}}{R_{CMP}} \bullet R1 \bullet N_{SF}$$

thus:

$$\frac{\Delta V_{OUT}}{\Delta I_{OUT}} = K1 \bullet \frac{R_{SENSE}}{R_{CMP}} \bullet R1 \bullet N_{SF}$$

where:

K1 = dimensionless variable related to V_{IN}, V_{OUT} and efficiency as explained above

R_{SENSE} = external sense resistor

Nominal output impedance cancellation is obtained by equating this expression with $R_{S(OUT)}$:

$$K1 \bullet \frac{R_{SENSE}}{R_{CMP}} \bullet R1 \bullet N_{SF} = \frac{ESR + R_{DS(ON)}}{1 - DC}$$

Solving for R_{CMP} gives:

$$R_{CMP} = K1 \bullet \frac{R_{SENSE} \bullet (1 - DC)}{ESR + R_{DS(ON)}} \bullet R1 \bullet N_{SF}$$

The practical aspects of applying this equation to determine an appropriate value for the R_{CMP} resistor are found in the Applications Information section.

APPLICATIONS INFORMATION

Primary Winding Feedback

The previous work was developed using a separate winding for voltage feedback. It is possible to use the primary winding as the feedback winding as well. This can simplify the design of the transformer.

When using the primary winding the feedback voltage will be added to the V_{IN} voltage so:

$$V_{FLYBK} = \frac{V_{OUT} + I_{OUT} \bullet \left(ESR + R_{DS(ON)}\right)}{N_{SP}}$$

where N_{SP} is the transformer effective secondary to primary winding turns ratio. Use the circuit of Figure 2 to get more accurate output regulation. In this case the regulation equations becomes:

$$R1 = \frac{R2}{V_{FB}} \bullet \left[\frac{V_{OUT} + I_{OUT} \bullet \left(ESR + R_{DS(ON)}\right)}{N_{SP}} - V_{BE} \right]$$

where V_{BE} is the base emitter drop of the PNP (approximately 0.7V).

Likewise the load compensation equation needs to be changed to use N_{SP} instead of N_{SF} so:

$$R_{CMP} = K1 \bullet \frac{R_{SENSE} \bullet (1-DC)}{ESR + R_{DS(ON)}} \bullet R1 \bullet N_{SF}$$

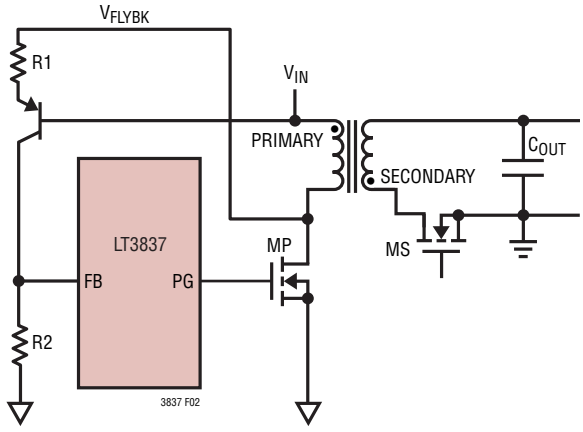


Figure 2

Transformer Design

Transformer design/specification is the most critical part of a successful application of the LT3837. The following sections provide basic information about designing the transformer and potential tradeoffs.

If you need help, the LTC Applications group is available to assist in the choice and/or design of the transformer.

Turns Ratios

The design of the transformer starts with determining duty cycle (DC). DC impacts the current and voltage stress on the power switches, input and output capacitor RMS currents and transformer utilization (size vs power).

The ideal turns ratio is:

$$N_{IDEAL} = \frac{V_{OUT}}{V_{IN}} \bullet \frac{1-DC}{DC}$$

Avoid extreme duty cycles as they, in general, increase current stresses. A reasonable target for duty cycle is 50% at nominal input voltage.

For instance, if we wanted a 9V to 3.3V converter at 50% DC then:

$$N_{IDEAL} = \frac{3.3}{9} \bullet \frac{1-0.5}{0.5} = \frac{1}{2.72}$$

In general, better performance is obtained with a lower turns ratio. A DC of 52% yields a 1:3 ratio.

Note the use of the external feedback resistive divider ratio to set output voltage provides the user additional freedom in selecting a suitable transformer turns ratio. Turns ratios that are the simple ratios of small integers; e.g., 1:1, 2:1, 3:2 help facilitate transformer construction and improve performance.

When building a supply with multiple outputs derived through a multiple winding transformer, lower duty cycle can improve cross regulation by keeping the synchronous rectifier on longer, and thus, keep secondary windings coupled longer.

For a multiple output transformer, the turns ratio between output windings is critical and affects the accuracy of the voltages. The ratio between two output voltages is set with the formula $V_{OUT2} = V_{OUT1} \bullet N21$ where N21 is the turns

APPLICATIONS INFORMATION

ratio of between the two windings. Also keep the secondary MOSFET $R_{DS(ON)}$ small to improve cross regulation.

Leakage Inductance

Transformer leakage inductance (on either the primary or secondary) causes a spike after the primary side switch turn-off. This is increasingly prominent at higher load currents, where more stored energy is dissipated. Higher flyback voltage may break down the MOSFET switch if it has too low a BV_{DSS} rating.

One solution to reducing this spike is to use a snubber circuit to suppress the voltage excursion. However, suppressing the voltage extends the flyback pulse width. If the flyback pulse extends beyond the enable delay time, output voltage regulation is affected. The feedback system has a deliberately limited input range, roughly ±50mV referred to the FB node. This rejects higher voltage leakage spikes because once a leakage spike is several volts in amplitude, a further increase in amplitude has little effect on the feedback system.

So it is advisable to arrange the snubber circuit to clamp at as high a voltage as possible, observing MOSFET breakdown, such that leakage spike duration is as short as possible. Application Note 19 provides a good reference on snubber design.

As a rough guide, total leakage inductances of several percent (of mutual inductance) or less may require a snubber, but exhibit little to no regulation error due to leakage spike behavior. Inductances from several percent up to perhaps ten percent cause increasing regulation error.

Avoid double digit percentage leakage inductances as there is a potential for abrupt loss of control at high load current. This curious condition potentially occurs when the leakage spike becomes such a large portion of the flyback waveform that the processing circuitry is fooled into thinking that the leakage spike itself is the real flyback signal!

It then reverts to a potentially stable state whereby the top of the leakage spike is the control point, and the trailing edge of the leakage spike triggers the collapse detect circuitry. This typically reduces the output voltage abruptly to a fraction, roughly one-third to two-thirds of its correct value.

Once load current is reduced sufficiently, the system snaps back to normal operation. When using transformers with considerable leakage inductance, exercise this worst-case check for potential bistability:

1. Operate the prototype supply at maximum expected load current.
2. Temporarily short-circuit the output.
3. Observe that normal operation is restored.

If the output voltage is found to hang up at an abnormally low value, the system has a problem. This is usually evident by simultaneously viewing the primary side MOSFET drain voltage to observe firsthand the leakage spike behavior.

A final note—the susceptibility of the system to bistable behavior is somewhat a function of the load current/voltage characteristics. A load with resistive—i.e., I = V/R behavior—is the most apt to be bistable. Capacitive loads that exhibit $I = V^2/R$ behavior are less susceptible.

Secondary Leakage Inductance

Leakage inductance on the secondary forms an inductive divider on the transformer secondary, reducing the size of the feedback flyback pulse. This increases the output voltage target by a similar percentage.

Note that unlike leakage spike behavior, this phenomenon is independent of load. Since the secondary leakage inductance is a constant percentage of mutual inductance (within manufacturing variations), the solution is to adjust the feedback resistive divider ratio to compensate.

Winding Resistance Effects

Primary or secondary winding resistance acts to reduce overall efficiency (P_{OUT}/P_{IN}). Secondary winding resistance increases effective output impedance degrading load regulation. Load compensation can mitigate this to some extent but a good design keeps parasitic resistances low.

Bifilar Winding

A bifilar or similar winding is a good way to minimize troublesome leakage inductances. Bifilar windings also improve coupling coefficients and thus improve cross regulation in multiple winding transformers. However,

APPLICATIONS INFORMATION

tight coupling usually increases primary-to-secondary capacitance and limits the primary-to-secondary breakdown voltage, so it isn't always practical.

Primary Inductance

The transformer primary inductance, L_P, is selected based on the peak-to-peak ripple current ratio (X) in the transformer relative to its maximum value. As a general rule, keep X in the range of 50% to 70% ripple current (i.e., X = 0.5 to 0.7). Higher values of ripple will increase conduction losses, while lower values will require larger cores.

Ripple current and percentage ripple is largest at minimum duty cycle; in other words, at the highest input voltage. L_P is calculated from:

$$L_P = \frac{\left(V_{IN(MAX)} \bullet DC_{MIN}\right)^2}{f_{OSC} \bullet X_{MAX} \bullet P_{IN}} = \frac{\left(V_{IN(MAX)} \bullet DC_{MIN}\right)^2 \bullet Eff}{f_{OSC} \bullet X_{MAX} \bullet P_{OUT}}$$

where:

f_{OSC} is the OSC frequency

DC_{MIN} is the DC at maximum input voltage

X_{MAX} is ripple current ratio at maximum input voltage

Continuing with the 9V to 3.3V example, let us assume a 10A output, 9V to 18V input power with 88% efficiency. Using X = 0.7, and f_{OSC} = 200kHz:

$$P_{IN} = \frac{3.3 \bullet 10A}{88\%} = 37.5W$$

$$DC_{MIN} = \frac{1}{1 + \frac{N \bullet V_{IN(MAX)}}{V_{OUT}}} = \frac{1}{1 + \frac{1}{3} \bullet \frac{18}{3.3}} = 35.5\%$$

$$L_P = \frac{(18V \bullet 0.355)^2}{200kHz \bullet 0.7 \bullet 37.5W} = 7.8\mu H$$

Optimization might show that a more efficient solution is obtained at higher peak current but lower inductance and the associated winding series resistance. A simple spreadsheet program is useful for looking at tradeoffs.

Transformer Core Selection

Once L_P is known, the type of transformer is selected. High efficiency converters use ferrite cores to minimize core loss. Actual core loss is independent of core size for a fixed inductance, but decreases as inductance increases. Since increased inductance is accomplished through more turns of wire, copper losses increase. Thus transformer design balances core and copper losses. Remember that increased winding resistance will degrade cross regulation and increase the amount of load compensation required.

The main design goals for core selection are reducing copper losses and preventing saturation. Ferrite core material saturates hard, rapidly reducing inductance when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and, consequently, output voltage ripple. **Do not allow the core to saturate!** The maximum peak primary current occurs at minimum V_{IN}:

$$I_{PK} = \frac{P_{IN}}{V_{IN(MIN)} \bullet DC_{MAX}} \bullet \left(1 + \frac{X_{MIN}}{2}\right)$$

now:

$$DC_{MAX} = \frac{1}{1 + \frac{N \bullet V_{IN(MIN)}}{V_{OUT}}} = \frac{1}{1 + \frac{1}{3} \bullet \frac{9}{3.3}} = 52.4\%$$

$$X_{MIN} = \frac{\left(V_{IN(MIN)} \bullet DC_{MAX}\right)^2}{f_{OSC} \bullet L_P \bullet P_{IN}} = \frac{(9 \bullet 0.52)^2}{200kHz \bullet 7.8\mu H \bullet 37.5W} = 0.380$$

Using the example numbers leads to:

$$I_{PK} = \frac{37.5W}{9V \bullet 0.524} \bullet \left(1 + \frac{0.380}{2}\right) = 9.47A$$

Multiple Outputs

One advantage that the flyback topology offers is that additional output voltages can be obtained simply by adding windings. Designing a transformer for such a situation is beyond the scope of this document. For multiple windings, realize that the flyback winding signal is a combination of activity on all the secondary windings. Thus load regulation is affected by each windings load. Take care to minimize cross regulation effects.

APPLICATIONS INFORMATION

Setting Feedback Resistive Divider

Use the equation developed in the Operation section for the feedback divider.

It is recommended that the Thevenin impedance of the resistors on the FB Pin is roughly 3k for bias current cancellation and other reasons.

For the example using primary winding sensing if ESR = 0.002 and $R_{DS(ON)}$ = 0.004 then:

$$R1 = \frac{3k}{1.237} \bullet \left[\left(\frac{(3.3+10 \bullet (0.002+0.004))}{(1/3)} \right) - 0.7 \right] = 22.75k$$

So, choose 22.1k.

Current Sense Resistor Considerations

The external current sense resistor is used to control peak primary switch current, which controls a number of key converter characteristics including maximum power and external component ratings. Use a noninductive current sense resistor (no wire-wound resistors). Mounting the resistor directly above an unbroken ground plane connected with wide and short traces keeps stray resistance and inductance low.

The dual sense pins allow for a fully Kelvined connection. Make sure that $SENSE^+$ and $SENSE^-$ are isolated and connect close to the sense resistor to preserve this.

Peak current occurs at 98mV of sense voltage V_{SENSE}. So the nominal sense resistor is V_{SENSE}/I_{PK}. For example, a peak switch current of 10A requires a nominal sense resistor of 0.010Ω. Note that the instantaneous peak power in the sense resistor is 1W, and that it is rated accordingly. The use of parallel resistors can help achieve low resistance, low parasitic inductance and increased power capability.

Size R_{SENSE} using worst-case conditions, minimum L_P, V_{SENSE} and maximum V_{IN}. Continuing the example, let us assume that our worst-case conditions yield an I_{PK} 10% above nominal so I_{PK} = 10.41A . If there is a 5% tolerance on R_{SENSE} and minimum V_{SENSE} = 80mV, then R_{SENSE} • 105% = 88mV/10.41A and nominal R_{SENSE} = 8.05mΩ. Round to the nearest available lower value 8.0mΩ.

Selecting the Load Compensation Resistor

The expression for R_{CMP} was derived in the Operation section for primary winding sensing as:

$$R_{CMP} = K1 \bullet \frac{R_{SENSE} \bullet (1-DC)}{ESR + R_{DS(ON)}} \bullet R1 \bullet N_{SP} = R_{S(OUT)}$$

Continuing the example:

$$K1 = \left(\frac{V_{OUT}}{V_{IN} \bullet Eff} \right) = \frac{3.3}{9(88\%)} = 0.417$$

If $ESR = 0.002\Omega$ and $R_{DS(ON)} = 0.004\Omega$

$$R_{CMP} = 0.417 \bullet \frac{8.0m\Omega \bullet (1-0.52)}{0.002\Omega + 0.004\Omega} \bullet 22.1k\Omega \bullet 0.33$$

$$= 1.93k\Omega$$

This value for R_{CMP} is a good starting point, but empirical methods are required for producing the best results. This is because several of the required input variables are difficult to estimate precisely. For instance, the ESR term above includes that of the transformer secondary, but its effective ESR value depends on high frequency behavior, not simply DC winding resistance. Similarly, K1 appears as a simple ratio of V_{IN} to V_{OUT} times (differential) efficiency, but theoretically estimating efficiency is not a simple calculation.

The suggested empirical method is as follows:

1. Build a prototype of the desired supply including the actual secondary components.
2. Temporarily ground the C_{CMP} pin to disable the load compensation function. Measure output voltage while sweeping output current over the expected range. Approximate the voltage variation as a straight line, $\Delta V_{OUT}/\Delta I_{OUT} = R_{S(OUT)}$.
3. Calculate a value for the K1 constant based on V_{IN}, V_{OUT} and the measured (differential) efficiency.
4. Compute:

$$R_{CMP} = K1 \bullet \frac{R_{SENSE}}{R_{S(OUT)}} \bullet R1 \bullet N_{SP} \text{ or } N_{SF}$$

APPLICATIONS INFORMATION

5. Verify this result by connecting a resistor of this value from the R_{CMP} pin to ground.

6. Disconnect the ground short to C_{CMP} and connect the requisite 0.1µF filter capacitor to ground. Measure the output impedance $R_{S(OUT)} = \Delta V_{OUT}/\Delta I_{OUT}$ with the new compensation in place. $R_{S(OUT)}$ should have decreased significantly. Fine tuning is accomplished experimentally by slightly altering R_{CMP}. A revised estimate for R_{CMP} is:

$$R'_{CMP} = R_{CMP} \bullet \left(1 + \frac{R_{S(OUT)CMP}}{R_{S(OUT)}}\right)$$

where R'_{CMP} is the new value for the load compensation resistor, $R_{S(OUT)CMP}$ is the output impedance with R_{CMP} in place and $R_{S(OUT)}$ is the output impedance with no load compensation (from step 2).

Setting Frequency

The switching frequency of the LT3837 is set by an external capacitor connected between the OSC pin and ground. Recommended values are between 200pF and 33pF, yielding switching frequencies between 50kHz and 250kHz. Figure 3 shows the nominal relationship between external capacitance and switching frequency. Place the capacitor as close as possible to the IC and minimize OSC trace length and area to minimize stray capacitance and potential noise pickup.

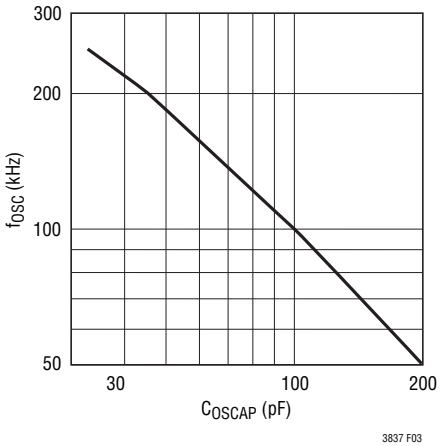


Figure 3. f_{OSC} vs OSC Capacitor Values

You can synchronize the oscillator frequency to an external frequency. This is done with a signal on the SYNC pin. Set the LT3837 frequency 10% slower than the desired external frequency using the OSC pin capacitor, then use a pulse on the SYNC pin of amplitude greater than 2V and with the desired period. The rising edge of the SYNC signal initiates an OSC capacitor discharge forcing primary MOSFET off (PG voltage goes low). If the oscillator frequency is much different from the sync frequency, problems may occur with slope compensation and system stability. Keep the sync pulse width greater than 500ns.

Selecting Timing Resistors

There are three internal "one-shot" times that are programmed by external application resistors: minimum on-time, enable delay time and primary MOSFET turn-on delay. These are all part of the isolated flyback control technique, and their functions are previously outlined in the Theory of Operation section.

The following information should help in selecting and/or optimizing these timing values.

Minimum On-Time ($t_{ON(MIN)}$)

Minimum on-time is the programmable period during which current limit is blanked (ignored) after the turn on of the primary side switch. This improves regulator performance by eliminating false tripping on the leading edge spike in the switch, especially at light loads. This spike is due to both the gate/source charging current and the discharge of drain capacitance. The isolated flyback sensing requires a pulse to sense the output. Minimum on-time ensures that there is always a signal to close the feedback loop. The LT3837 does not employ cycle skipping at light loads. Therefore, minimum on-time along with synchronous rectification sets the switch over in forced continuous mode operation.

The $t_{ON(MIN)}$ resistor is set with the following equation:

$$R_{tON(MIN)}(k\Omega) = \frac{t_{ON(MIN)}(ns) - 104}{1.063}$$

Keep $R_{tON(MIN)}$ greater than 70k. A good starting value is 160k.

APPLICATIONS INFORMATION

Enable Delay Time (ENDLY)

Enable delay time provides a programmable delay between turn-off of the primary gate drive node and the subsequent enabling of the feedback amplifier. As discussed earlier, this delay allows the feedback amplifier to ignore the leakage inductance voltage spike on the primary side.

The worst-case leakage spike pulse width is at maximum load conditions. So set the enable delay time at these conditions.

While the typical applications for this part use forced continuous operation, it is conceivable that a secondary-side controller might cause discontinuous operation at light loads. Under such conditions the amount of energy stored in the transformer is small. The flyback waveform becomes "lazy" and some time elapses before it indicates the actual secondary output voltage. The enable delay time should be made long enough to ignore the "irrelevant" portion of the flyback waveform at light load.

Even though the LT3837 has a robust gate drive, the gate transition-time slows with very large MOSFETs. Increase delay time is as required when using such MOSFETs.

The enable delay resistor is set with the following equation:

$$R_{ENDLY}(k\Omega) = \frac{t_{ENDLY}(ns) - 30}{2.616}$$

Keep R_{ENDLY} greater than 40k. A good starting point is 56k.

Primary Gate Delay Time (PGDLY)

Primary gate delay is the programmable time from the turn-off of the synchronous MOSFET to the turn-on of the primary side MOSFET. Correct setting eliminates overlap between the primary side switch and secondary side synchronous switch(es) and the subsequent current spike in the transformer. This spike will cause additional component stress and a loss in regulator efficiency.

The primary gate delay resistor is set with the following equation:

$$R_{PGDLY}(k\Omega) = \frac{t_{PGDLY}(ns) + 47}{9.01}$$

A good starting point is 27k.

Soft-Start Functions

The LT3837 contains an optional soft-start function that is enabled by connecting an external capacitor between the SFST pin and ground. Internal circuitry prevents the control voltage at the V_C pin from exceeding that on the SFST pin. There is an initial pull-up circuit to quickly bring the SFST voltage to approximately 0.8V. From there it charges to approximately 2.8V with a 20µA current source.

The SFST node is then discharged to 0.8V when a fault occurs. A fault is V_{CC} too low (undervoltage lockout), current sense voltage greater than 200mV or the IC's thermal (overtemperature) shutdown is tripped. When SFST discharges, the V_C node voltage is also pulled low to below the minimum current voltage. Once discharged, the SFST recharges up again.

In this manner, switch currents are reduced and the stresses in the converter are reduced during fault conditions.

The time it takes to fully charge soft-start is:

$$t_{SS} = \frac{C_{SFST} \bullet 1.4V}{20\mu A} = 70ms \bullet C_{SFST}\ (\mu F)$$

UVLO Pin Function

The UVLO pin provides a user programming undervoltage lockout. This is usually used to provide undervoltage lockout based on V_{IN}. The gate drivers are disabled when UVLO is below the 1.24V UVLO threshold. An external resistive divider between the input supply and ground is used to set the turn-on voltage.

The bias current on this pin depends on the pin voltage and UVLO state. The change provides the user with adjustable UVLO hysteresis. When the pin rises above the UVLO threshold a small current is sourced out of the pin, increasing the voltage on the pin. As the pin voltage drops below this threshold, the current is stopped, further

APPLICATIONS INFORMATION

dropping the voltage on UVLO. In this manner, hysteresis is produced.

Referring to Figure 4, the voltage hysteresis at V_{IN} is equal to the change in bias current times R_A. The design procedure is to select the desired V_{IN} referred voltage hysteresis, V_{UVHYS}. Then:

$$R_A = \frac{V_{UVHYS}}{I_{UVLO}}$$

where:

$I_{UVLO} = I_{UVLOL} - I_{UVLOH}$ is approximately 3.4µA

R_B is then selected with the desired turn-on voltage:

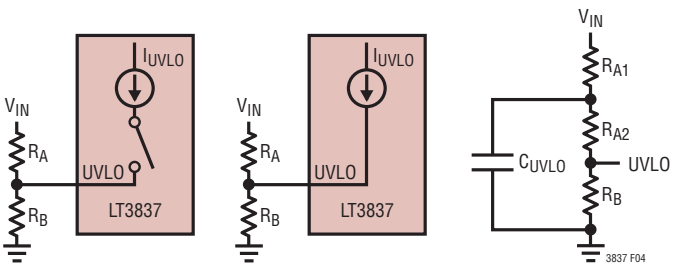
$$R_B = \frac{R_A}{\left(\frac{V_{IN(ON)}}{V_{UVLO}} - 1\right)}$$

If we wanted a V_{IN}-referred trip point of 8.4V, with 0.3V of hysteresis (on at 8.4V, off at 8.1V):

$$R_A = \frac{0.3V}{3.4\mu A} = 88.2k, \text{ use } 86.6k$$

$$R_B = \frac{86.6k}{\left(\frac{8.4V}{1.24V} - 1\right)} = 14.99k, \text{ use } 15k$$

Even with good board layout, board noise may cause problems with UVLO. You can filter the divider but keep large capacitance off the UVLO node because it will slow the hysteresis produced from the change in bias current. Figure 4c shows an alternate method of filtering by splitting the R_A resistor with the capacitor. The split should put more of the resistance on the UVLO side.



(4a) UV Turning ON (4b) UV Turning OFF (4c) UV Filtering

Figure 4

Control Loop Compensation

Loop frequency compensation is performed by connecting a capacitor network from the output of the feedback amplifier (V_C pin) to ground as shown in Figure 5. Because of the sampling behavior of the feedback amplifier, compensation is different from traditional current mode switcher controllers. Normally only C_{VC} is required. R_{VC} can be used to add a "zero" but the phase margin improvement traditionally offered by this extra resistor is usually already accomplished by the nonzero secondary circuit impedance. C_{VC2} can be used to add an additional high frequency pole and is usually sized at 0.1 times C_{VC}.

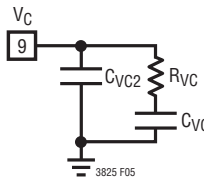


Figure 5. V_C Compensation Network

In further contrast to traditional current mode switchers, V_C pin ripple is generally not an issue with the LT3837. The dynamic nature of the clamped feedback amplifier forms an effective track/hold type response, whereby the V_C voltage changes during the flyback pulse, but is then held during the subsequent switch-on portion of the next cycle. This action naturally holds the V_C voltage stable during the current comparator sense action (current mode switching).

AN19 provides a method for empirically tweaking frequency compensation. Basically, it involves introducing a load current step and monitoring the response.

Slope Compensation

This part incorporates current slope compensation. Slope compensation is required to ensure current loop stability when the DC is greater than 50%. In some switcher controllers, slope compensation reduces the maximum peak current at higher duty cycles. The LT3837 eliminates this need by having circuitry that compensates for the slope compensation so that maximum current sense voltage is constant across all duty cycles.

APPLICATIONS INFORMATION

Minimum Load Considerations

At light loads, the LT3837 derived regulator goes into forced continuous conduction mode. The primary side switch always turns on for a short time as set by the $t_{ON(MIN)}$ resistor. If this produces more power than the load requires, power will flow back into the primary during the "off" period when the synchronization switch is on. This does not produce any inherently adverse problems, though light load efficiency is reduced.

Maximum Load Considerations

The current mode control uses the V_C node voltage and amplified sense resistor voltage as inputs to the current comparator. When the amplified sense voltage exceeds the V_C node voltage, the primary side switch is turned off.

In normal use, the peak switch current increases while FB is below the internal reference. This continues until V_C reaches its 2.56V clamp. At clamp, the primary side MOSFET will turn off at the rated 98mV V_{SENSE} level. This repeats on the next cycle.

It is possible for the peak primary switch currents as referred across R_{SENSE} to exceed the max 98mV rating because of the minimum switch-on time blanking. If the voltage on V_{SENSE} reaches 206mV after the minimum turn-on time, the SFST capacitor is discharged, which also discharges the V_C capacitor. This then reduces the peak current on the next cycle and will reduce overall stress in the primary switch.

Short-Circuit Conditions

Loss of current limit is possible under certain conditions such as an output short-circuit. If the duty cycle exhibited by the minimum on-time is greater than the ratio of secondary winding voltage (referred-to-primary) divided by input voltage, then peak current is not controlled at the nominal value. It ratchets up cycle-by-cycle to some higher level. Expressed mathematically, the requirement to maintain short-circuit control is:

$$DC_{MIN} = t_{ON(MIN)} \bullet f_{OSC} < \frac{I_{SC} \bullet \left(R_{SEC} + R_{DS(ON)}\right)}{V_{IN} \bullet N_{SP}}$$

where:

$t_{ON(MIN)}$ = primary side switch minimum on-time

I_{SC} = short-circuit output current

Other variables as previously defined.

Trouble is typically encountered only in applications with a relatively high product of input voltage times secondary-to-primary turns ratio and/or a relatively long minimum switch-on time. Additionally, several real world effects such as transformer leakage inductance, AC winding losses, and output switch voltage drop combine to make this simple theoretical calculation a conservative estimate. Prudent design evaluates the switcher for short-circuit protection and adds any additional circuitry to prevent destruction.

Output Voltage Error Sources

The LT3837's feedback sensing introduces additional sources of errors. The following is a summary list.

The internal bandgap voltage reference sets the reference voltage for the feedback amplifier. The specifications detail its variation.

The external feedback resistive divider ratio proportional directly affects regulated voltage. Use 1% components.

Leakage inductance on the transformer secondary reduces the effective secondary-to-feedback winding turns ratio (N_S/N_F) from its ideal value. This increases the output voltage target by a similar percentage. Since secondary leakage inductance is constant from part to part (with a tolerance) adjust the feedback resistor ratio to compensate.

The transformer secondary current flows through the impedances of the winding resistance, synchronous MOSFET $R_{DS(ON)}$ and output capacitor ESR. The DC equivalent current for these errors is higher than the load current because conduction occurs only during the converter's "off" time. So divide the load current by (1 – DC).

APPLICATIONS INFORMATION

If the output load current is relatively constant, the feedback resistive divider is used to compensate for these losses. Otherwise, use the LT3837 load compensation circuitry (see Load Compensation).

If multiple output windings are used, the flyback winding will have a signal that represents an amalgamation of all these windings impedances. Take care that you examine worst-case loading conditions when tweaking the voltages.

Power MOSFET Selection

The power MOSFETs are selected primarily on the criteria of on-resistance $R_{DS(ON)}$, input capacitance, drain-to-source breakdown voltage (BV_{DSS}), maximum gate voltage (VGS) and maximum drain current ($I_{D(MAX)}$).

For the primary-side power MOSFET, the peak current is:

$$I_{PK} = \frac{I_{OUT}}{1-DC_{MAX}} \bullet \left(1+\frac{X_{MIN}}{2}\right)$$

where X is peak-to-peak current ratio as defined earlier.

For each secondary-side power MOSFET, the peak current is:

$$I_{PK} = \frac{I_{OUT}}{1-DC_{MAX}} \bullet \left(1+\frac{X_{MIN}}{2}\right)$$

Select a primary-side power MOSFET with a B_{VDSS} greater than:

$$BV_{DSS} \geq I_{PK}\sqrt{\frac{L_{LKG}}{C_P}} + V_{IN(MAX)} + \frac{V_{OUT(MAX)}}{N_{SP}}$$

where N_{SP} reflects the turns ratio of that secondary-to-primary winding. L_{LKG} is the primary-side leakage inductance and C_P is the primary-side capacitance (mostly from the C_{OSS} of the primary-side power MOSFET). A snubber may be added to reduce the leakage inductance spike as discussed earlier.

For each secondary-side power MOSFET, the BV_{DSS} should be greater than:

$$BV_{DSS} \geq V_{OUT} + V_{IN(MAX)} \bullet N_{SP}$$

Choose the primary side MOSFET $R_{DS(ON)}$ at the nominal gate drive voltage (7.5V). The secondary side MOSFET gate drive voltage depends on the gate drive method.

Primary side power MOSFET RMS current is given by:

$$I_{RMSPRI} = \frac{P_{IN}}{V_{IN(MIN)}\sqrt{DC_{MAX}}}$$

For each secondary-side power MOSFET RMS current is given by:

$$I_{RMSSEC} = \frac{I_{OUT}}{\sqrt{1-DC_{MAX}}}$$

Calculate MOSFET power dissipation next. Because the primary-side power MOSFET may operate at high V_{DS}, a transition power loss term is included for accuracy. C_{MILLER} is the most critical parameter in determining the transition loss, but is not directly specified on the data sheets.

C_{MILLER} is calculated from the gate charge curve included on most MOSFET data sheets (Figure 6).

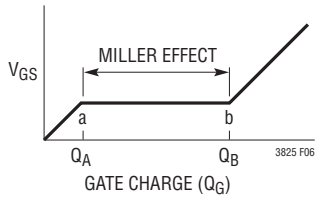


Figure 6. Gate Charge Curve

The flat portion of the curve is the result of the Miller (gate-to-drain) capacitance as the drain voltage drops. The Miller capacitance is computed as:

$$C_{MILLER} = \frac{Q_B - Q_A}{V_{DS}}$$

The curve is done for a given V_{DS}. The Miller capacitance for different V_{DS} voltages are estimated by multiplying the computed C_{MILLER} by the ratio of the application V_{DS} to the curve specified V_{DS}.

APPLICATIONS INFORMATION

With C_{MILLER} determined, calculate the primary-side power MOSFET power dissipation:

$$P_{DPRI} = I_{RMS(PRI)}^2 \bullet R_{DS(ON)}(1+\delta) + V_{IN(MAX)} \bullet \frac{P_{IN(MAX)}}{DC_{IN}} \bullet R_{DR} \bullet \frac{C_{MILLER}}{V_{GATE(MAX)} - V_{TH}} \bullet f_{OSC}$$

where:

R_{DR} is the gate driver resistance approximately 10Ω

V_{TH} is the MOSFET gate threshold voltage

f_{OSC} is the operating frequency.

(1 + δ) is generally given for a MOSFET in the form of a normalized RDS(ON) vs temperature curve. If you don't have a curve, use δ = 0.005/°C as an estimate.

The secondary-side power MOSFETs typically operate at substantially lower V_{DS}, so you can neglect transition losses. The dissipation is calculated using:

$$P_{D(SEC)} = I_{RMS(SEC)}^2 \bullet R_{DS(ON)}(1 + \delta)$$

With power dissipation known, the MOSFETs' junction temperatures are obtained from the equation:

$$T_J = T_A + P_D \bullet \theta_{JA}$$

where T_A is the ambient temperature and θ_{JA} is the MOSFET junction to ambient thermal resistance.

Once you have T_J, iterate your calculations recomputing δ, power dissipations until convergence.

Gate Drive Node Consideration

The PG and SG gate drivers are strong drives to minimize gate drive rise and fall times. This improves efficiency but the high frequency components of these signals can cause problems. Keep the traces short and wide to reduce parasitic inductance.

The parasitic inductance creates an LC tank with the MOSFET gate capacitance. In less than ideal layouts, a series resistance of 5Ω or more may help to dampen the ringing at the expense of slightly slower rise and fall times and efficiency.

The LT3837 gate drives will clamp the max gate voltage to roughly 7.4V, so you can safely use MOSFETs with max V_{GS} of 10V or larger.

Synchronous Gate Drive

There are several different ways to drive the synchronous gate MOSFET. Full converter isolation requires the synchronous gate drive to be isolated. This is usually accomplished by way of a pulse transformer. Usually the pulse driver is used to drive a buffer on the secondary as shown in the application on the front page of this data sheet.

However, other schemes are possible. There are gate drivers and secondary side synchronous controllers available that provide the buffer function as well as additional features.

Capacitor Selection

In a flyback converter, the input and output current flows in pulses, placing severe demands on the input and output filter capacitors. The input and output filter capacitors are selected based on RMS current ratings and ripple voltage.

Select an input capacitor with a ripple current rating greater than:

$$I_{RMS} = \frac{P_{IN}}{V_{IN(MIN)}} \sqrt{\frac{1-DC_{MAX}}{DC_{MAX}}}$$

Continuing the example:

$$I_{RMS} = \frac{37.5W}{9V} \sqrt{\frac{1-52.4\%}{52.4\%}} = 3.97A$$

Input capacitor series resistance (ESR) and inductance (ESL) need to be small as they affect electromagnetic interference suppression. In some instances, high ESR can also produce stability problems because flyback converters exhibit a negative input resistance characteristic. Refer to Application Note 19 for more information.

The output capacitor is sized to handle the ripple current and to ensure acceptable output voltage ripple. The output capacitor should have an RMS current rating greater than:

$$I_{RMS} = I_{OUT} \sqrt{\frac{DC_{MAX}}{1-DC_{MAX}}}$$

Continuing the example:

$$I_{RMS} = 10A \sqrt{\frac{52.4\%}{1-52.4\%}} = 10.5A$$

This is calculated for each output in a multiple winding application.

APPLICATIONS INFORMATION

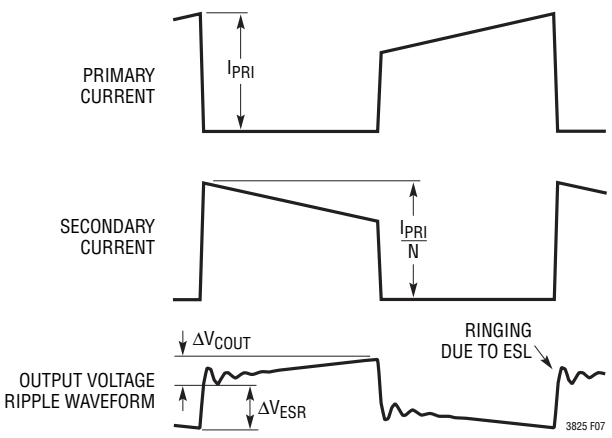


Figure 7. Typical Flyback Converter Waveforms

ESR and ESL along with bulk capacitance directly affect the output voltage ripple. The waveforms for a typical flyback converter are illustrated in Figure 7.

The maximum acceptable ripple voltage (expressed as a percentage of the output voltage) is used to establish a starting point for the capacitor values. For the purpose of simplicity we will choose 2% for the maximum output ripple, divided equally between the ESR step and the charging/discharging ΔV. This percentage ripple changes, depending on the requirements of the application. You can modify the following equations.

For a 1% contribution to the total ripple voltage, the ESR of the output capacitor is determined by:

$$ESR_{COUT} \le 1\% \bullet \frac{V_{OUT} \bullet (1 - DC_{MAX})}{I_{OUT}}$$

The other 1% is due to the bulk C component, so use:

$$C_{OUT} \ge \frac{I_{OUT}}{1\% \bullet V_{OUT} \bullet f_{OSC}}$$

In many applications the output capacitor is created from multiple capacitors to achieve desired voltage ripple, reliability and cost goals. For example, a low ESR ceramic capacitor can minimize the ESR step, while an electrolytic capacitor satisfies the required bulk C.

Continuing our example, the output capacitor needs:

$$ESR_{COUT} \le 1\% \bullet \frac{3.3V \bullet (1 - 52.4\%)}{10A} = 1.6m\Omega$$

$$C_{OUT} \ge \frac{10A}{1\% \bullet 3.3 \bullet 200kHz} = 1515\mu F$$

These electrical characteristics require paralleling several low ESR capacitors possibly of mixed type.

Most capacitor ripple current ratings are based on 2000 hour life. This makes it advisable to derate the capacitor or to choose a capacitor rated at a higher temperature than required.

One way to reduce cost and improve output ripple is to use a simple LC filter. Figure 8 shows an example of the filter.

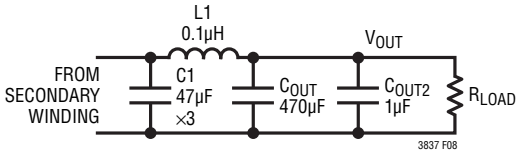


Figure 8

The design of the filter is beyond the scope of this data sheet. However, as a starting point, use these general guide lines. Start with a C_{OUT} 1/4 the size of the nonfilter solution. Make C1 1/4 of C_{OUT} to make the second filter pole independent of C_{OUT}. The smaller C1 may be best implemented with multiple ceramic capacitors. Make L1 smaller than the output inductance of the transformer. In general, a 0.1µH filter inductor is sufficient. Add a small ceramic capacitor (C_{OUT2}) for high frequency noise on V_{OUT}. For those interested in more details refer to "Second-Stage LC Filter Design," Ridley, Switching Power Magazine, July 2000, p8-10.

Circuit simulation is a way to optimize output capacitance and filters, just make sure to include the component parasitics. LTC SwitcherCAD™ is a terrific free circuit simulation tool that is available at www.linear.com. Final optimization of output ripple must be done on a dedicated PC board. Parasitic inductance due to poor layout can significantly impact ripple. Refer to the PC Board Layout section for more details.

SwitcherCAD is a trademark of Linear Technology Corporation.

APPLICATIONS INFORMATION

IC Thermal Considerations

Take care to ensure that the LT3837 junction temperature does not exceed 125°C. Power is computed from the average supply current, the sum of quiescent supply current (I_{CC} in the specifications) plus gate drive currents.

The primary gate drive current is computed as:

$$f_{OSC} \bullet Q_G$$

where Q_G is the total gate charge at max V_{GS} (obtained from the gate charge curve) and f is the switching frequency.

Since the synchronous driver is usually driving a capacitive load, the power dissipation is:

$$f_{OSC} \bullet C_S \bullet V_{SGMAX}$$

where C_S is the SG capacitive load and V_{SGMAX} is the SG pin max voltage.

So total IC dissipation is computed as:

$$P_{D(TOTAL)} = V_{CC} \bullet (I_{CC} + f \bullet (Q_{GPRI} + C_S \bullet V_{SGMAX}))$$

V_{CC} is the worst-case LT3837 supply voltage.

Junction temperature is computed as:

$$T_J = T_A + P_D \bullet \theta_{JA}$$

where:

T_A is the ambient temperature

θ_{JA} is the FE16 package junction-to-ambient thermal impedance (40°C/W).

PC Board Layout Considerations

In order to minimize switching noise and improve output load regulation, connect the GND pin of the LT3837 directly to the ground terminal of the V_{CC} decoupling capacitor, the bottom terminal of the current sense resistor, the ground terminal of the input capacitor, and the ground plane (multiple vias). Place the V_{CC} capacitor immediately adjacent to the V_{CC} and GND pins on the IC package. This capacitor carries high di/dt MOSFET gate drive currents. Use a low ESR ceramic capacitor.

Take care in PCB layout to keep the traces that conduct high switching currents short, wide and with minimal overall loop area. These are typically the traces associated with the switches. This reduces the parasitic inductance and also minimizes magnetic field radiation. Figure 9 outlines the critical paths.

Keep electric field radiation low by minimizing the length and area of traces (keep stray capacitances low). The drain of the primary side MOSFET is the worst offender in this category. Always use a ground plane under the switcher circuitry to prevent coupling between PCB planes.

Check that the maximum BV_{DSS} ratings of the MOSFETs are not exceeded due to inductive ringing. This is done by viewing the MOSFET node voltages with an oscilloscope. If it is breaking down either choose a higher voltage device, add a snubber or specify an avalanche-rated MOSFET.

Place the small-signal components away from high frequency switching nodes. This allows the use of a pseudo-Kelvin connection for the signal ground, where high di/dt gate driver currents flow out of the IC ground pin in one direction (to the bottom plate of the V_{CC} decoupling capacitor) and small-signal currents flow in the other direction.

Keep the trace from the feedback divider tap to the FB short to preclude inadvertent pickup.

For applications with multiple switching power converters connected to the same input supply, make sure that the input filter capacitor for the LTC3837 is not shared with other converters. AC input current from another converter could cause substantial input voltage ripple and this could interfere with the LT3837 operation. A few inches of PC trace or wire ($L \cong 100nH$) between the C_{IN} of the LT3837 and the actual source V_{IN} is sufficient to prevent current sharing problems.

APPLICATIONS INFORMATION

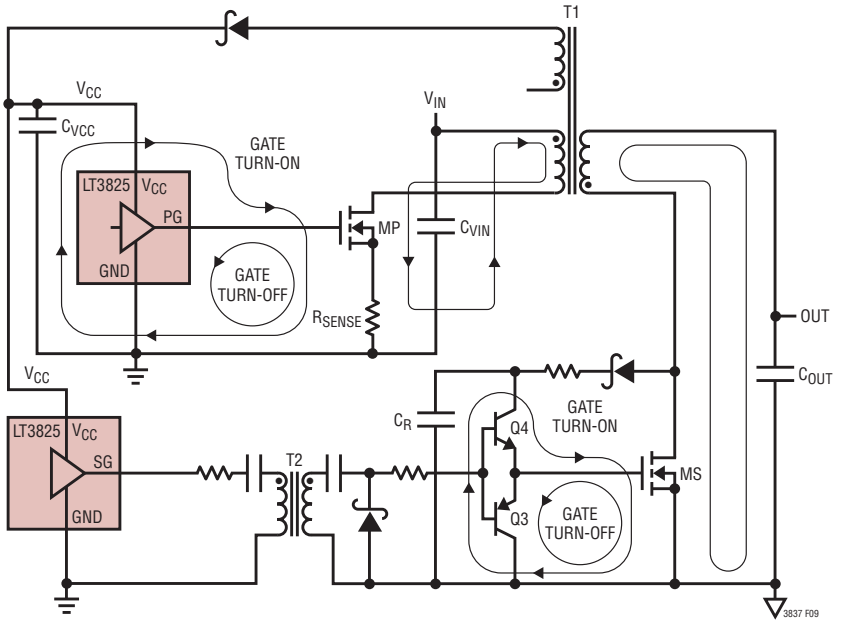
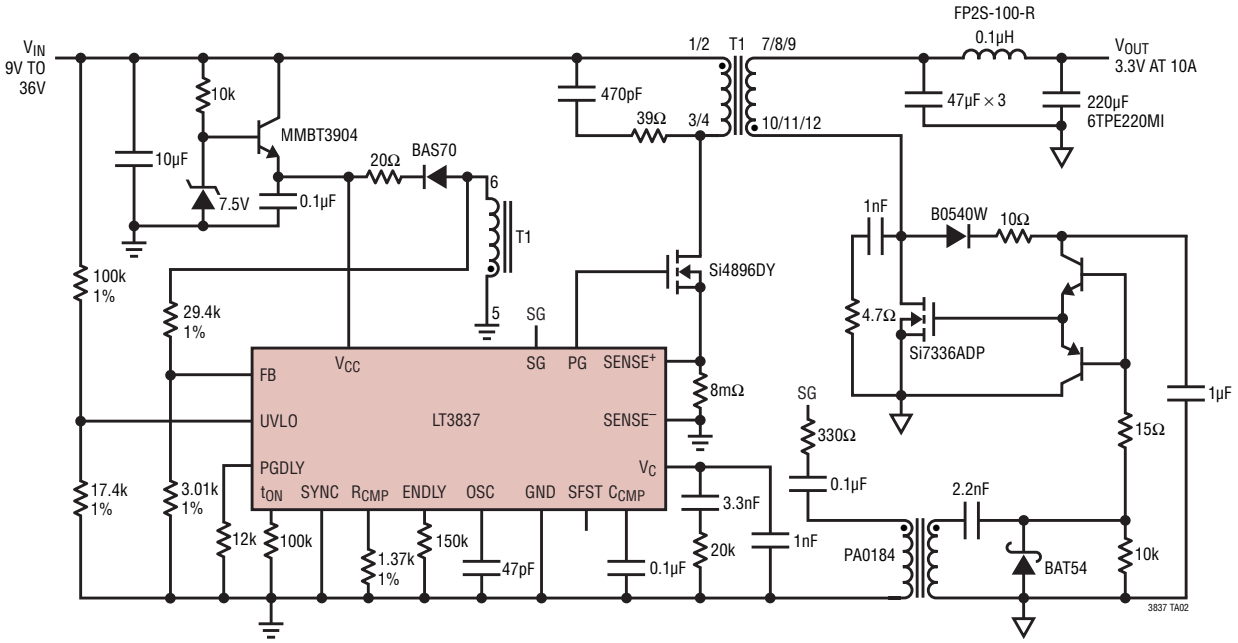
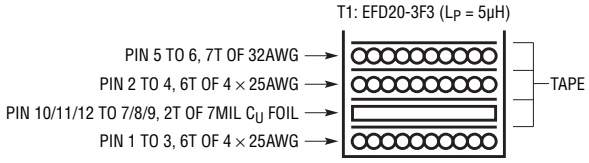


Figure 9. High Current Paths

TYPICAL APPLICATION

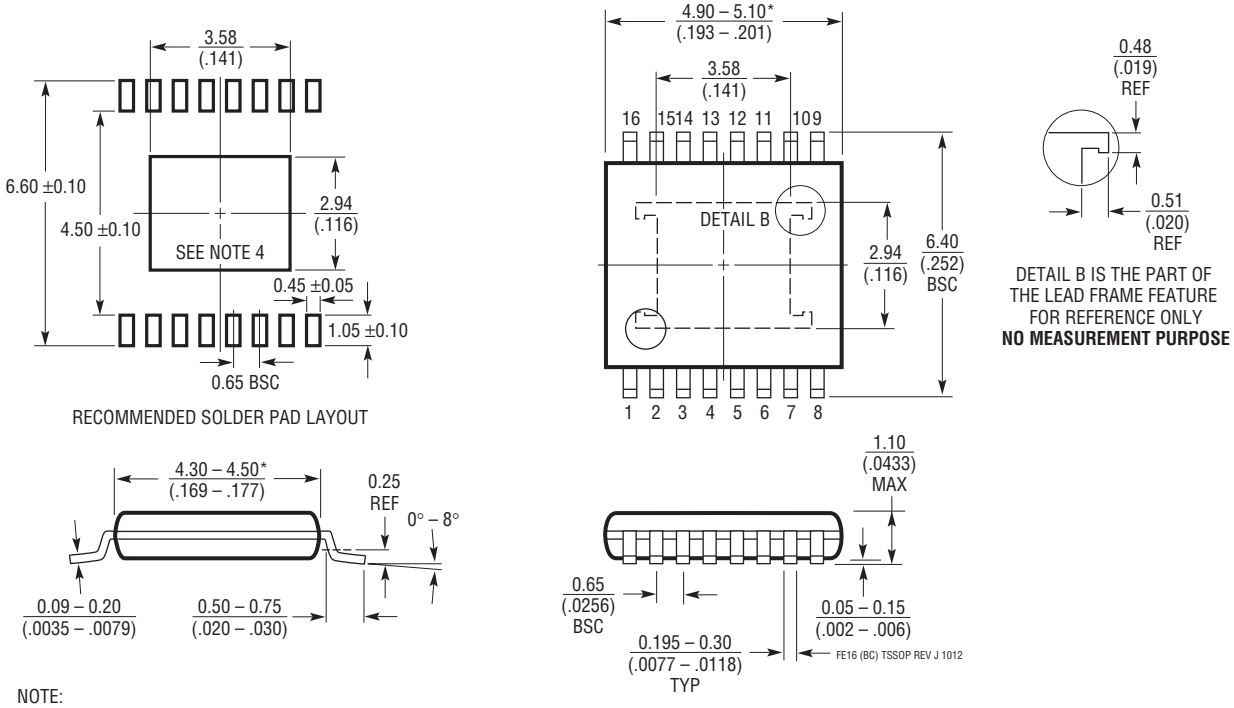
9V – 36V to 3.3V at 10A Isolated Converter





PACKAGE DESCRIPTION

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev J)
Exposed Pad Variation BC



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	11/09	Change to Absolute Maximum Ratings	2
		Change to Electrical Characteristics	2,3
		Change to Pin Functions	6
		Change to Block Diagram	8
		Change to Flyback Feedback Amplifier	9
		Text Change to Applications Information	23
		Changes to Related Parts	28
D	12/12	Updated G20 graph	6
		Updated package	26