# 250mA Universal Nine Channel LED Driver

## FEATURES

- **Multimode Charge Pump Provides Up to 91% Efficiency**
- **Slew Limited Switching Reduces Conducted and Radiated Noise (EMI)**
- **Up to 250mA Total Output Current**
- **Nine 28mA Universal Current Sources with 64-Step Linear Brightness Control**
- **Independent On/Off, Brightness Level, Blinking and Gradation Control for Each Current Source Using 2-Wire I²C™ Interface**
- **Internal Current Reference**
- Configurable ENU Pin for Asynchronous LED On/Off Control
- Low Noise Charge Pump Operates in 1x, 1.5x or 2x Mode for Optimal Efficiency*
- Automatic or Forced Mode Switching
- Internal Soft-Start Limits Inrush Current
- Short-Circuit/Thermal Protection
- 3mm × 3mm 20-Lead QFN Plastic Package

## APPLICATIONS

- Video Phones with QVGA+ Displays

## DESCRIPTION

The LTC®3219 is a highly integrated multidisplay LED driver. The device contains a high efficiency, low noise charge pump to provide power to nine universal LED current sources. The LTC3219 requires only five small ceramic capacitors to form a complete LED power supply and current controller.

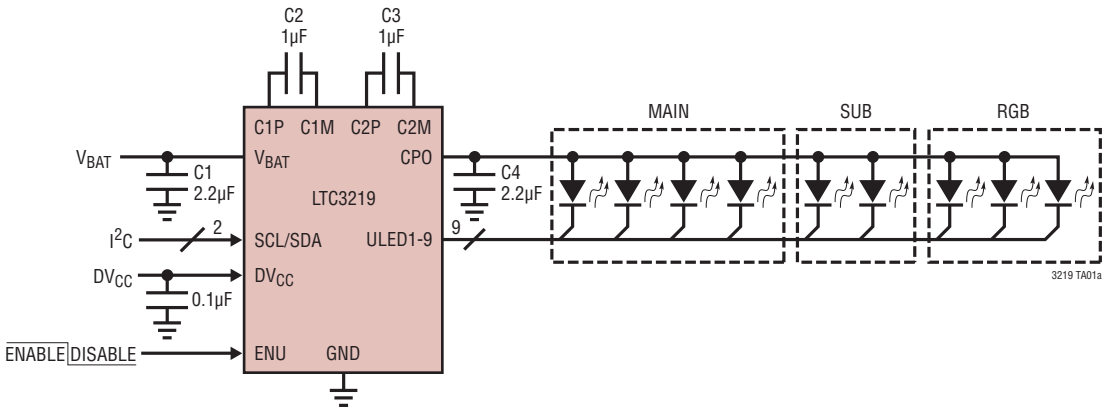
The maximum display currents are set by an internal precision current reference. Independent dimming, On/Off, blinking and gradation control for all current sources is achieved via the I²C serial interface. 6-bit linear DACs are available for adjusting brightness levels for each universal LED current source.

The LTC3219 charge pump optimizes efficiency based on the voltage across the LED current sources. The device powers up in 1x mode and will automatically switch to boost mode whenever any enabled LED current source begins to enter dropout. The first dropout switches the IC into 1.5x mode and a subsequent dropout switches the LTC3219 into 2x mode. The part resets to 1x mode whenever a data register is updated via the I²C port.



## TYPICAL APPLICATION

**4-LED Main, 2-LED Sub and RGB**

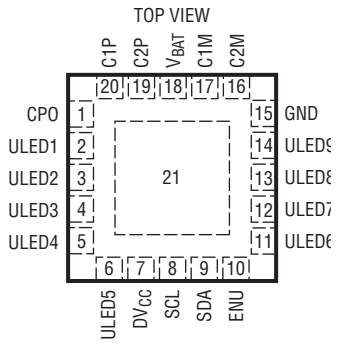


## ABSOLUTE MAXIMUM RATINGS

**(Notes 1, 4)**

$V_{BAT}$, $DV_{CC}$, CPO ..... –0.3V to 6V
ULED1-ULED9 ..... –0.3V to 6V
SDA, SCL, ENU .....–0.3V to ($DV_{CC}$ + 0.3V)
$I_{CPO}$ (Note 2) .....250mA
CPO Short-Circuit Duration ..... Indefinite
Operating Temperature Range (Note 3).... –40°C to 85°C
Storage Temperature Range..... –65°C to 125°C

## PIN CONFIGURATION




UD PACKAGE
20-LEAD (3mm × 3mm) PLASTIC QFN
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 68°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC3219EUD#PBF | LTC3219EUD#TRPBF | LCJV | 20-Lead (3mm × 3mm) Plastic QFN | –40°C to 85°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{BAT}$ = 3.6V, $DV_{CC}$ = 3V, ENU = Hi, C1/C4 = 2.2µF, C2, C3 = 1µF, unless otherwise noted.**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{BAT}$ Operating Voltage | | ● | 2.9 | | 5.5 | V |
| $I_{VBAT}$ Operating Current | $I_{CPO}$ = 0, 1x Mode<br>$I_{CPO}$ = 0, 1.5x Mode<br>$I_{CPO}$ = 0, 2x Mode | | | 0.4<br>1.7<br>2.1 | | mA<br>mA<br>mA |
| $V_{BAT}$ UVLO Threshold | | | | 1.5 | | V |
| $DV_{CC}$ Operating Voltage | | ● | 1.5 | | 5.5 | V |
| $DV_{CC}$ UVLO Threshold | | | | 1 | | V |
| $V_{BAT}$ Shutdown Current | | | | 3.2 | | µA |
| $DV_{CC}$ Shutdown Current | | ● | | | 1 | µA |
| **Universal LED Current, 6-Bit Linear DACs, ULED = 1V** | | | | | | |
| Full-Scale LED Current | | ● | 25 | 28 | 31 | mA |
| Minimum LED Current | Data Code = 1 | | | 0.51 | | mA |
| LED Current Matching | Any Two Outputs | | | 2 | | % |
| Blink Rate Period | REG 11, D3 and D4 | | | 1.25<br>2.5 | | s<br>s |
| ULED Up/Down Gradation Ramp Times | REG11, D1 and D2 | | | 0.24<br>0.48<br>0.96 | | s<br>s<br>s |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{BAT}$ = 3.6V, $DV_{CC}$ = 3V, ENU = Hi, C1/C4 = 2.2µF, C2, C3 = 1µF, unless otherwise noted.**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Gradation Period | REG11, D1 and D2 | | | 0.325 | | s |
| | | ● | | | 0.45 | s |
| | | | | 0.65 | | s |
| | | ● | | | 0.9 | s |
| | | | | 1.30 | | s |
| | | ● | | | 1.8 | s |
| $V_{OL}$ General Purpose Output Mode (GPO) | $I_{OUT}$ = 1mA, Single Output Enabled | | | 10 | | mV |
| **Charge Pump (CPO)** | | | | | | |
| 1x Mode Output Impedance | | | | 1 | | Ω |
| 1.5x Mode Output Impedance | $V_{BAT}$ = 3V, $V_{CPO}$ = 4.2V (Notes 5, 7) | | | 5.2 | | Ω |
| 2x Mode Output Impedance | $V_{BAT}$ = 3V, $V_{CPO}$ = 4.8V (Notes 5, 7) | | | 6.2 | | Ω |
| CPO Regulation Voltage | 1.5x Mode, $I_{CPO}$ = 20mA<br>2x Mode, $I_{CPO}$ = 20mA | | | 4.53<br>5.04 | | V<br>V |
| Clock Frequency | | ● | 0.65 | 0.85 | 1.05 | MHz |
| **SDA, SCL, ENU** | | | | | | |
| $V_{IL}$ | | ● | | | 0.3 • $DV_{CC}$ | V |
| $V_{IH}$ | | ● | 0.7V • $DV_{CC}$ | | | V |
| $I_{IH}$ | SDA, SCL, ENU = $DV_{CC}$ | ● | –1 | | 1 | µA |
| $I_{IL}$ | SDA, SCL, ENU = 0V | ● | –1 | | 1 | µA |
| $V_{OL}$, Digital Output Low (SDA) | $I_{PULLUP}$ = 3mA | ● | | 0.12 | 0.4 | V |
| **Serial Port Timing (Notes 6, 7)** | | | | | | |
| $t_{SCL}$ | Clock Operating Frequency | | | | 400 | kHz |
| $t_{BUF}$ | Bus Free Time Between Stop and Start Condition | | 1.3 | | | µs |
| $t_{HD,STA}$ | Hold Time After (Repeated) Start Condition | | 0.6 | | | µs |
| $t_{SU,STA}$ | Repeated Start Condition Setup Time | | 0.6 | | | µs |
| $t_{SU,STO}$ | Stop Condition Setup Time | | 0.6 | | | µs |
| $t_{HD,DAT(OUT)}$ | Data Hold Time | | 0 | | 900 | ns |
| $t_{HD,DAT(IN)}$ | Input Data Hold Time | | 0 | | | ns |
| $t_{SU,DAT}$ | Data Setup Time | | 100 | | | ns |
| $t_{LOW}$ | Clock Low Period | | 1.3 | | | µs |
| $t_{HIGH}$ | Clock High Period | | 0.6 | | | µs |
| $t_f$ | Clock Data Fall Time | | 20 | | 300 | ns |
| $t_r$ | Clock Data Rise Time | | 20 | | 300 | ns |
| $t_{SP}$ | Spike Suppression Time | | 50 | | | ns |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** Based on long-term current density limitations.

**Note 3:** The LTC3219 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

**Note 4:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

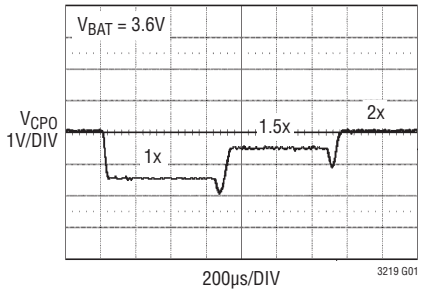
**Note 5:** 1.5x mode output impedance is defined as $(1.5V_{BAT} – V_{CPO})/I_{OUT}$. 2x mode output impedance is defined as $(2V_{BAT} – V_{CPO})/I_{OUT}$.

**Note 6:** All values are referenced to $V_{IH}$ and $V_{IL}$ levels.

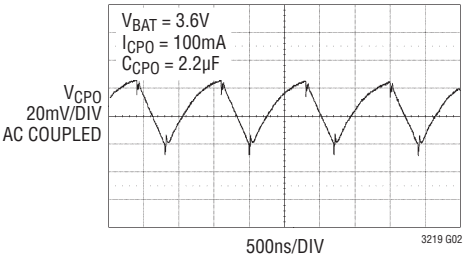
**Note 7:** Guaranteed by design.

## TYPICAL PERFORMANCE CHARACTERISTICS $T_A$ = 25°C unless otherwise noted.

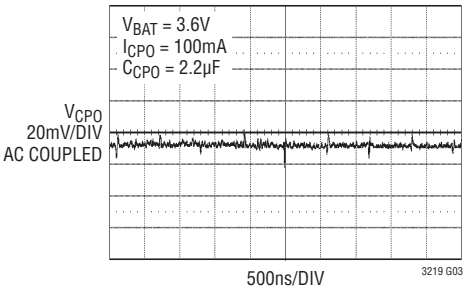
### Mode Switch Dropout Times



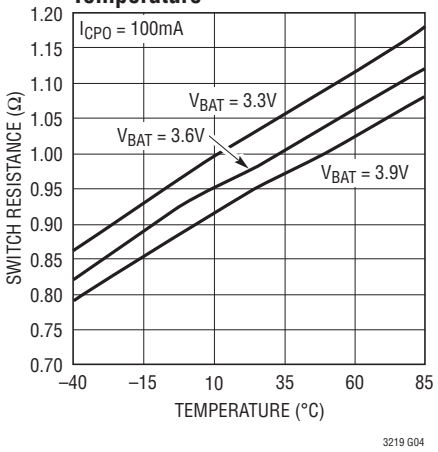

### 1.5x Mode CPO Ripple



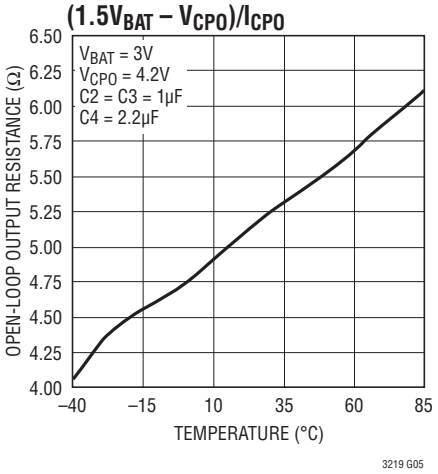

### 2x Mode CPO Ripple



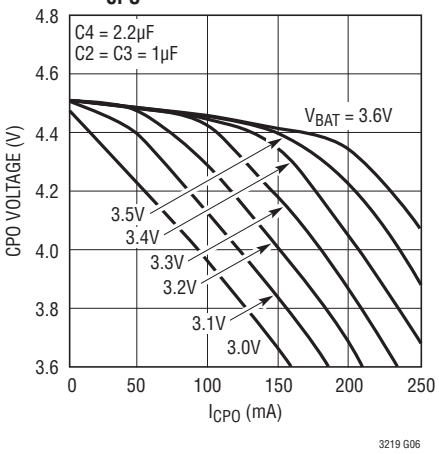

### 1x Mode Switch Resistance vs Temperature



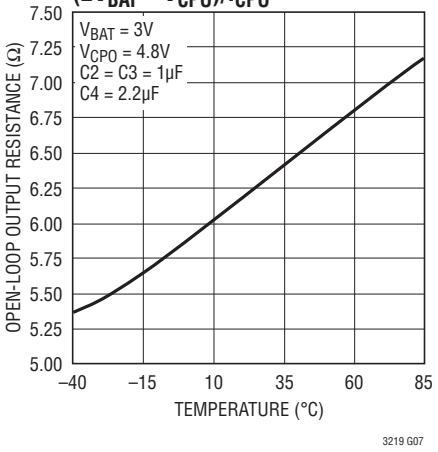

### 1.5x Mode Charge Pump Open-Loop Output Resistance vs Temperature $(1.5V_{BAT} – V_{CPO})/I_{CPO}$



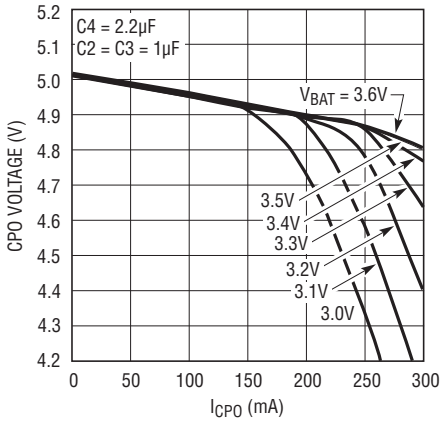

### 1.5x Mode CPO Voltage vs $I_{CPO}$



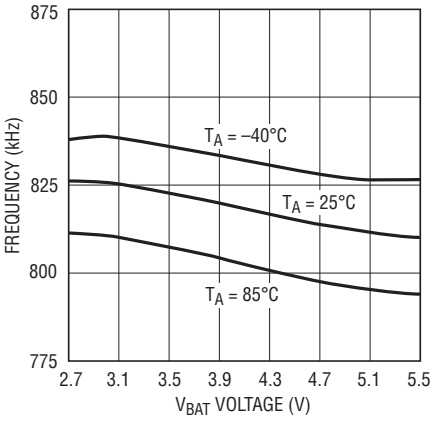

### 2x Mode Charge Pump Open-Loop Output Resistance vs Temperature $(2V_{BAT} – V_{CPO})/I_{CPO}$




### 2x Mode CPO Voltage vs $I_{CPO}$



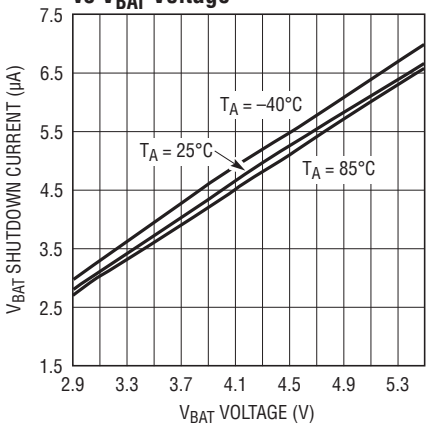

### Oscillator Frequency vs $V_{BAT}$ Voltage



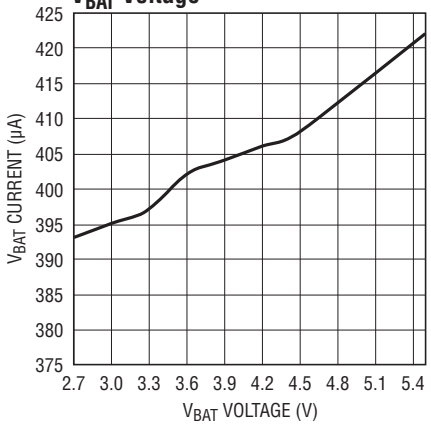
## TYPICAL PERFORMANCE CHARACTERISTICS

$T_A$ = 25°C unless otherwise noted.

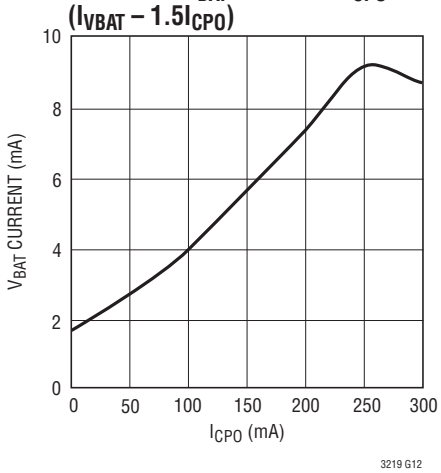
### $V_{BAT}$ Shutdown Current vs $V_{BAT}$ Voltage



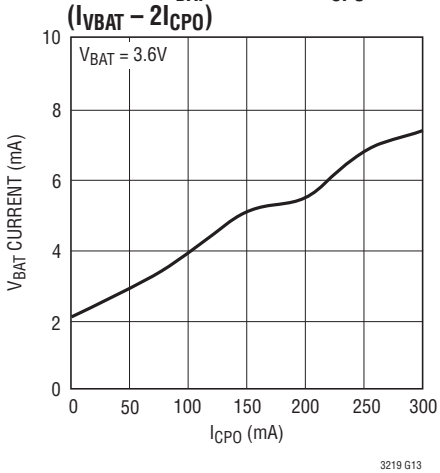

### 1x Mode No Load $V_{BAT}$ Current vs $V_{BAT}$ Voltage



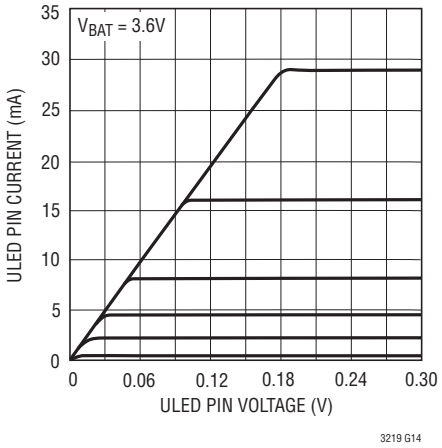

### 1.5x Mode $V_{BAT}$ Current vs $I_{CPO}$ ($I_{VBAT} – 1.5I_{CPO}$)



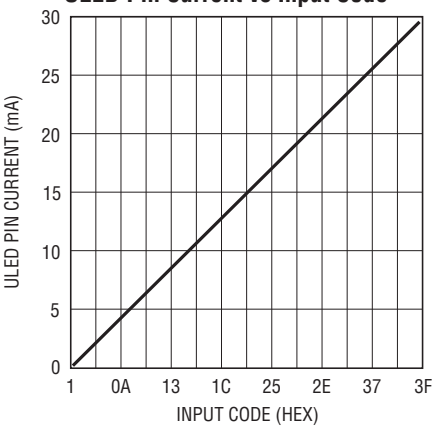

### 2x Mode $V_{BAT}$ Current vs $I_{CPO}$ ($I_{VBAT} – 2I_{CPO}$)



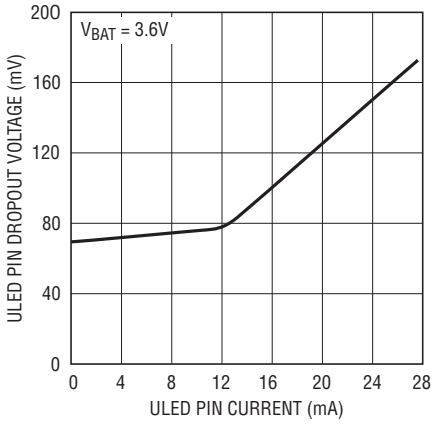

### ULED Pin Current vs ULED Pin Voltage



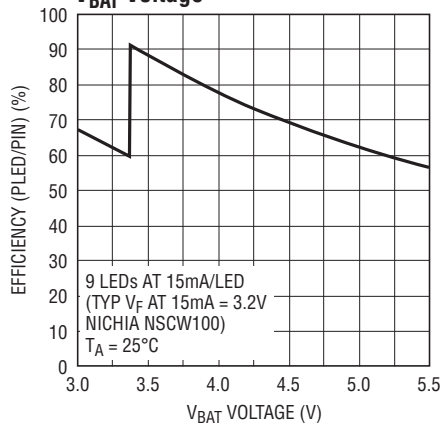

### ULED Pin Current vs Input Code




### ULED Pin Dropout Voltage vs ULED Pin Current




### 9-LED ULED Display Efficiency vs $V_{BAT}$ Voltage



## PIN FUNCTIONS

**CPO (Pin 1):** Output of the Charge Pump Used to Power all LEDs. A 2.2µF X5R or X7R ceramic capacitor should be connected to ground.

**ULED1-ULED9 (Pins 2 to 6, Pins 11 to 14):** Current Source Outputs for Driving LEDs. The LED current can be set from 0mA to 28mA in 64 steps via software control and internal 6-bit linear DAC. Each output can be disabled by setting the associated data register REG1-REG9 to 0. ULED1-ULED9 can also be used as $I^2C$ controlled open-drain outputs. Connect unused outputs to ground.

**$DV_{CC}$ (Pin 7):** Supply Voltage for All Digital I/O Lines. This pin sets the logic reference level of the LTC3219. $DV_{CC}$ will reset the data registers when set below the undervoltage lockout threshold, which is the recommended method for resetting the part after power-up. A 0.1µF X5R or X7R ceramic capacitor should be connected to ground.

**SCL (Pin 8):** $I^2C$ Clock Input. The logic level for SCL is referenced to $DV_{CC}$.

**SDA (Pin 9):** Input Data for the Serial Port. Serial data is shifted in one bit per clock to control the LTC3219. The logic level is referenced to $DV_{CC}$.

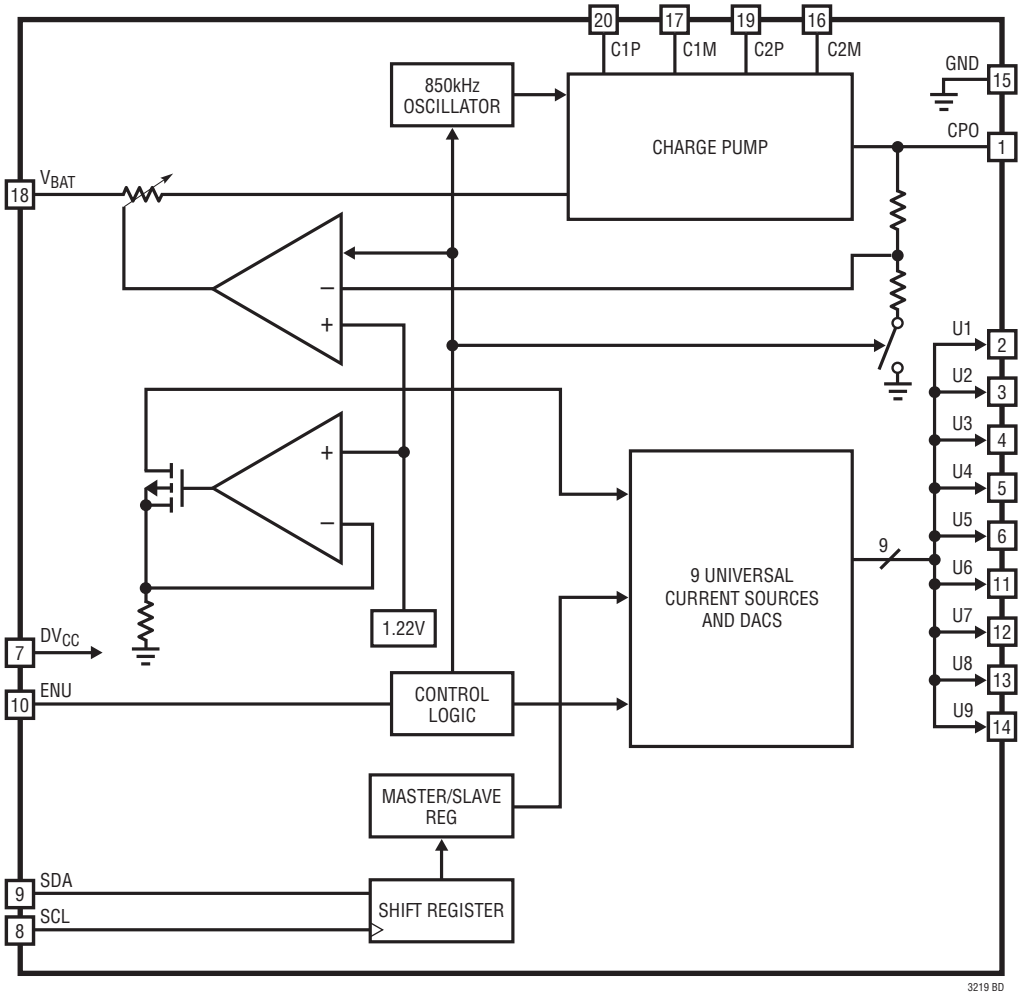
**ENU (Pin 10):** Input. Used to enable or disable the pre-selected ULED outputs. When the pin is toggled from low (disable) to high (enable), the LTC3219 illuminates the pre-selected LEDs. When ENU is controlling selected outputs and other outputs have been enabled, the charge pump mode will be reset to 1x on the falling edge of ENU. When ENU is controlling selected outputs and no other outputs are active, the part will go from enabled to shutdown. The ENU logic level is referenced to $DV_{CC}$. This pin is connected to ground if unused.

**GND (Pin 15, 21):** System Ground. Connect Pin 15 and the Exposed Pad (Pin 21) to the ground plane.

**C1P, C2P, C1M, C2M (Pins 20, 19, 17, 16):** Charge Pump Flying Capacitor Pins. A 1µF X7R or X5R ceramic capacitor should be connected from C1P to C1M and C2P to C2M.

**$V_{BAT}$ (Pin 18):** Supply Voltage for the Entire Device. This pin should be bypassed with a single 2.2µF low ESR ceramic capacitor.

## BLOCK DIAGRAM



## OPERATION

### Power Management

The LTC3219 uses a switched capacitor charge pump to boost CPO to as much as 2 times the input voltage up to 5.04V. The part starts up in 1x mode. In this mode $V_{BAT}$ is connected directly to CPO. This mode provides maximum efficiency and minimum noise. The LTC3219 will remain in 1x mode until an LED current source drops out. Dropout occurs when a current source voltage becomes too low for the programmed current to be supplied. When dropout is detected, the LTC3219 will switch into 1.5x mode. The CPO voltage will then start to increase and attempt to reach 1.5x $V_{BAT}$, up to 4.53V. Any subsequent dropout will cause the part to enter the 2x mode. The CPO voltage will attempt to reach 2x $V_{BAT}$, up to 5.04V.

A 2-phase non-overlapping clock activates the charge pump switches. In the 2x mode, the flying capacitors are charged on alternate clock phases from $V_{BAT}$ to minimize CPO voltage ripple. In 1.5x mode, the flying capacitors are charged in series during the first clock phase and stacked in parallel on $V_{BAT}$ during the second phase. This sequence of charging and discharging the flying capacitors continues at a constant frequency of 850kHz.

The current delivered by each LED current source is controlled by an associated DAC. Each DAC is programmed via the $I^2C$ port.

### Soft-Start

Initially, when the part is in shutdown, a weak switch connects $V_{BAT}$ to CPO. This allows $V_{BAT}$ to slowly charge the CPO output capacitor and to prevent large charging currents from occurring.

The LTC3219 also employs a soft-start feature on its charge pump to prevent excessive inrush current and supply droop when switching into the step-up modes. The current available to the CPO pin is increased linearly over a typical period of 125µs. Soft-start occurs at the start of both 1.5x and 2x mode changes.

### Charge Pump Strength

When the LTC3219 operates in either 1.5x mode or 2x mode, the charge pump can be modeled as a Thevenin-equivalent circuit to determine the amount of current available from the effective input voltage and effective open-loop output resistance, $R_{OL}$ (Figure 1).

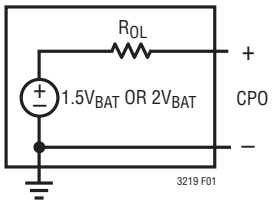



**Figure 1. Equivalent Open-Loop**

$R_{OL}$ is dependent on a number of factors including the switching term, $1/(2f_{OSC} \bullet C_{FLY})$, internal switch resistances and the non-overlap period of the switching circuit. However, for a given $R_{OL}$, the amount of current available is directly proportional to the advantage voltage of $1.5V_{BAT}$ – CPO for 1.5x mode and $2V_{BAT}$ – CPO for 2x mode. Consider the example of driving LEDs from a 3.1V supply. If the LED forward voltage is 3.8V and the current sources require 100mV, the advantage voltage for 1.5x mode is 3.1V •1.5 – 3.8V – 0.1V or 750mV. Notice that if the input voltage is raised to 3.2V, the advantage voltage jumps to 900mV, a 20% improvement in available strength.

From Figure 1, for 1.5x mode the available current is given by:

$$I_{OUT} = \frac{1.5V_{BAT} - V_{CPO}}{R_{OL}} \quad (1)$$

For 2x mode, the available current is given by:

$$I_{OUT} = \frac{2V_{BAT} - V_{CPO}}{R_{OL}} \quad (2)$$

Notice that the advantage voltage in this case is 3.1V • 2 – 3.8V – 0.1V = 2.3V. $R_{OL}$ is higher in 2x mode but a significant overall increase in available current is achieved.

## OPERATION

### Mode Switching

The LTC3219 will automatically switch from 1x mode to 1.5x mode and subsequently to 2x mode whenever a dropout condition is detected at an LED pin. Dropout occurs when an active current source voltage becomes too low for the programmed current to be supplied. The mode change will not occur unless dropout has existed for approximately 400µs. This delay will allow the LEDs to warm up and achieve the final LED forward voltage value.

The mode will automatically switch back to 1x whenever a register is updated via the $I^2C$ port, when gradation completes ramping down, on the falling edge of ENU, and after each blink period.

The part can be forced to operate in 1x, 1.5x or 2x mode by writing the appropriate bits into REG0. This feature may be used for powering loads from CPO. Automatic mode switching is diabled.

Non-programmed current sources do not affect dropout. In addition, ENU controlled current sources do not affect dropout when ENU is low.

### Universal Current Sources (ULED1 to ULED9)

There are nine universal 28mA current sources. Each current source has a 6-bit linear DAC for current control. The output current range is 0 to full-scale in 64 steps.

Each current source is disabled when an all zero data word is written. The supply current for that source is reduced to zero. Connect unused outputs to ground.

ULED1 to ULED9 can also be used as general purpose outputs (GPO). GPO outputs can be used as $I^2C$ controlled open-drain drivers. The GPO mode is selected by programming REG1 to REG9, Bit 6 and Bit 7 to a logic one. In the GPO mode dropout detection is disabled, output swings to ground will not cause mode switching.

### Blinking

Each universal output (ULED1 to ULED9) can be set to blink on for 0.156s or 0.625s with a period of 1.25s or 2.5s via the $I^2C$ port. The blinking rate is selected via REG11 and ULED outputs are selected via REG1 to REG9. Blinking and gradation rates are independent. Blink resets the charge pump to 1x mode after each period. Please refer to Application Note 111 for detailed information and programming examples on blinking.

### Gradation

Universal LED outputs ULED1 to ULED9 can be set to have the current ramp up and down at 0.24s, 0.48s and 0.96s rates via the $I^2C$ port. Each of these outputs can have either blinking or gradation enabled. The gradation time is set via REG11 and ULED outputs are selected via REG1 to REG9. The ramp direction is controlled via REG0. Setting the UP bit high causes gradation to ramp up, setting this bit to a low causes gradation to ramp down.

When gradation is disabled the LED output current remains at the programmed value. The gradation enable bit must be cleared when the gradation timer is disabled. The charge pump mode is reset to 1x after gradation completes ramping down.

Please refer to Application Note 111 for detailed information and examples on programming gradation.

### External Enable Control (ENU)

The ENU pin can be used to enable or disable the LTC3219 without re-accessing the $I^2C$ port. This might be useful to indicate an incoming phone call without waking the micro-controller. ENU can be programmed to independently control all pre-selected displays. LED displays are controlled with ENU by setting the appropriate data bits in REG1 to REG9 and control bits in REG10 and REG11.

## OPERATION

To use the ENU pin, the $I^2C$ port must first be configured to select the desired LED outputs. When ENU is high, the selected displays will be enabled as per the REG10 and REG11 settings. When ENU is Low the selected displays will be off. If no other displays are programmed to be enabled, the chip will be in shutdown.

Gradation can also be pre-programmed for control by the ENU pin. The registers are written as required per the gradation description and the UP bit is ignored. The registers are programmed when ENU is low. When ENU is set high, the part will become enabled and the selected LED outputs will ramp up. When ENU is set low the selected LED outputs will ramp low to zero current and then the part will shut down. The charge pump must not be in a forced mode if shutdown is required.

If the ENU pin is not used, it is connected to ground. If ENU is used and other ULED outputs are active then ENU will reset the charge pump mode to 1x on the falling edge. Please refer to Application Note 111 for detailed information and examples on programming ENU control.

### Shutdown Current

Shutdown occurs when all the current source data bits have been written to zero, $DV_{CC}$ is set below the undervoltage lockout voltage or when ENU switches low (all other outputs disabled). The charge pump must also be in auto mode.

Although the LTC3219 is designed to have very low shutdown current, it will draw about 3.2µA from $V_{BAT}$ when in shutdown. Internal logic ensures that the LTC3219 is in shutdown when $DV_{CC}$ is low. Note, however that all of the logic signals that are referenced to $DV_{CC}$ (SCL, SDA, ENU) will need to be at $DV_{CC}$ or below (i.e., ground) to avoid violation of the absolute maximum specifications on these pins.

### EMI Reduction

The flying capacitor pins C1M, C1P, C2M and C2P have controlled slew rates to reduce conducted and radiated noise.

### Serial Port

The microcontroller compatible $I^2C$ serial port provides all of the command and control inputs for the LTC3219. Data on the SDA input is loaded on the rising edge of SCL. D7 is loaded first and D0 last. There are 12 data registers, one address register and one sub-address register. Once all address bits have been clocked into the address register acknowledge occurs. The sub-address register is then written followed by writing the data register. Each data register has a sub-address. After the data register has been written a load pulse is created after the stop bit. The load pulse transfers all of the data held in the data registers to the DAC registers. The stop bit can be delayed until all of the data master registers have been written. At this point the LED current will be changed to the new settings. The serial port uses static logic registers so there is no minimum speed at which it can be operated.

# OPERATION

## I²C Interface

The LTC3219 communicates with a host (master) using the standard I²C 2-wire interface. The Timing Diagram (Figure 2) shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources, such as the LTC1694 SMBus accelerator, are required on these lines.

The LTC3219 is a receive-only (slave) device.

**Write Word Protocol Used by the LTC3219**

| 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|
| S | Slave Address | Wr | A | *Sub-Address | A | Data Byte | A | P** |

S = Start Condition, Wr = Write Bit = 0, A = Acknowledge,
P = Stop Condition
*The sub-address uses only the first four bits, D0, D1, D2 and D3
**Stop can be delayed until all of the data registers have been written

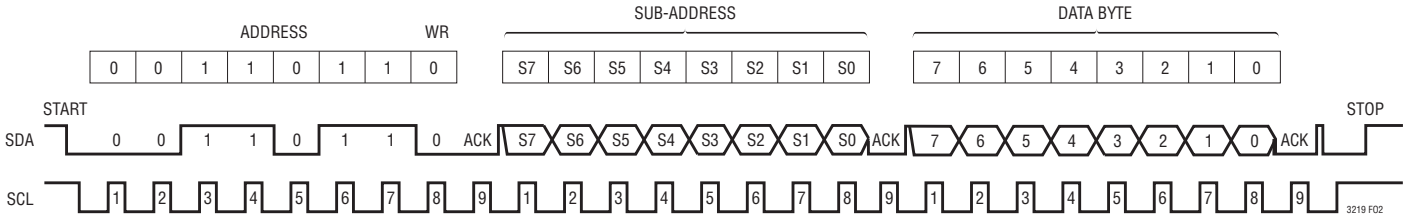



**Figure 2. Bit Assignments**

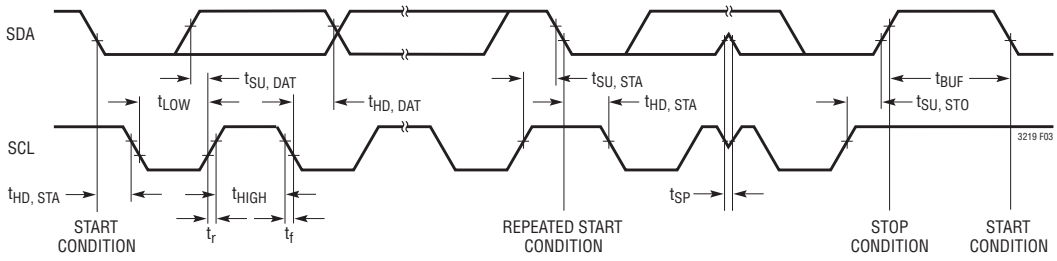



**Figure 3. Timing Parameters**

## OPERATION

**Sub-Address Byte**

| MSB | | | | | | | LSB | | |
|---|---|---|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Register | Function |
| X | X | X | X | 0 | 0 | 0 | 0 | REG0 | COMMAND |
| X | X | X | X | 0 | 0 | 0 | 1 | REG1 | ULED1 |
| X | X | X | X | 0 | 0 | 1 | 0 | REG2 | ULED2 |
| X | X | X | X | 0 | 0 | 1 | 1 | REG3 | ULED3 |
| X | X | X | X | 0 | 1 | 0 | 0 | REG4 | ULED4 |
| X | X | X | X | 0 | 1 | 0 | 1 | REG5 | ULED5 |
| X | X | X | X | 0 | 1 | 1 | 0 | REG6 | ULED6 |
| X | X | X | X | 0 | 1 | 1 | 1 | REG7 | ULED7 |
| X | X | X | X | 1 | 0 | 0 | 0 | REG8 | ULED8 |
| X | X | X | X | 1 | 0 | 0 | 1 | REG9 | ULED9 |
| X | X | X | X | 1 | 0 | 1 | 0 | REG10 | ENU |
| X | X | X | X | 1 | 0 | 1 | 1 | REG11 | B/G/ENU |

**REG0, Command Byte, Sub-Address = 0000**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Unused | Reserved | Reserved | Reserved | Force2x | Force1p5 | Quick Write | UP |

| | | |
|---|---|---|
| UP | 0<br>1 | Gradation counts down<br>Gradation counts up |
| Quick Write | 0<br>1 | Normal write to each register<br>Quick write, REG1 data is written to all nine universal registers |
| Force1p5 | 1<br>0 | Forces charge pump into 1.5x mode<br>Enables mode logic to control mode charges based on dropout signal |
| Force2x | 1<br>0 | Forces charge pump into 2x mode<br>Enables mode logic to control mode changes based on dropout signal |
| Force1x | | D2 (Force1p5x) = 1<br>D3 (Force2x) = 1<br>} Forces Charge Pump Into 1x Mode |
| Reserved | X | |
| Reserved | X | |
| Reserved | X | |
| Unused | X | |

Note: X = Don't Care

# OPERATION

## Data Bytes

REG1 to REG9, Universal LED 6-bit linear DAC data with blink/gradation.

**Sub-Address 0001 TO 1001 per Sub-Address Table Above**

| ULED Mode Enable Bits | | | LED Current Data | | | | | |
|---|---|---|---|---|---|---|---|---|
| | MSB | | | | | | | LSB |
| | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| Normal | 0 | 0 | D5 | D4 | D3 | D2 | D1 | D0 |
| Blink Enabled | 0 | 1 | D5 | D4 | D3 | D2 | D1 | D0 |
| Gradation Enabled | 1 | 0 | D5 | D4 | D3 | D2 | D1 | D0 |
| GPO Mode (Gradation/Blink/Dropout Off) | 1 | 1 | D5 | D4 | D3 | D2 | D1 | D0 |

## REG10, ENU

Setting bits D0 to D7 high selects the ULED outputs to be controlled by ENU.

**Register Sub-Address = 1010**

| MSB | | | | | | | LSB |
|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| ULED8 | ULED7 | ULED6 | ULED5 | ULED4 | ULED3 | ULED2 | ULED1 |

## REG11, Gradation and Blink Times

Setting bit D0 high selects ULED9 to be controlled by ENU,
Bits D1 to D4 control gradation and blink times.
The gradation ramp time is the time that the current ramps.
The gradation period is the total time that is required to start and end a gradation timer.

**Sub-Address = 1011**

| Blink Times and Period | | | | Gradation Ramp Times and Period | | | | ENU Select |
|---|---|---|---|---|---|---|---|---|
| D4 | D3 | On-Time | Period | D2 | D1 | Ramp Time | Period | D0 |
| 0 | 0 | 0.625s | 1.25s | 0 | 0 | Disabled | Disabled | ULED9 |
| 0 | 1 | 0.156s | 1.25s | 0 | 1 | 0.24s | 0.325s | |
| 1 | 0 | 0.625s | 2.5s | 1 | 0 | 0.48s | 0.65s | |
| 1 | 1 | 0.156s | 2.5s | 1 | 1 | 0.96s | 1.30s | |

## OPERATION

### Bus Speed

The I²C port is designed to be operated at speeds of up to 400kHz. It has built-in timing delays to ensure correct operation when addressed from an I²C compliant master device. It also contains input filters designed to suppress glitches should the bus become corrupted.

### Start and Stop Conditions

A bus-master signals the beginning of a communication to a slave device by transmitting a Start condition.

A Start condition is generated by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a Stop condition by transitioning SDA from low to high while SCL is high. The bus is then free for communication with another I²C device.

### Byte Format

Each byte sent to the LTC3219 must be eight bits long followed by an extra clock cycle for the Acknowledge bit to be returned by the LTC3219. The data should be sent to the LTC3219 most significant bit (MSB) first.

### Acknowledge

The Acknowledge signal is used for handshaking between the master and the slave. An Acknowledge (active Low) generated by the slave (LTC3219) lets the master know that the latest byte of information was received. The Acknowledge related clock pulse is generated by the master. The master releases the SDA line (High) during the Acknowledge clock cycle. The slave-receiver must pull down the SDA line during the Acknowledge clock pulse so that it remains a stable Low during the High period of this clock pulse.

### Slave Address

The LTC3219 responds to only one 7-bit address which has been factory programmed to 0011011. The eighth bit of the address byte (R/W) must be 0 for the LTC3219 to recognize the address since it is a write only device. This effectively forces the address to be eight bits long where the least significant bit of the address is 0. If the correct seven bit address is given but the R/W bit is 1, the LTC3219 will not respond.

### Bus Write Operation

The master initiates communication with the LTC3219 with a START condition and a 7-bit address followed by the Write Bit R/W = 0. If the address matches that of the LTC3219, the LTC3219 returns an Acknowledge. The master should then deliver the most significant sub-address byte for the data register to be written. Again the LTC3219 acknowledges and then the data is delivered starting with the most significant bit. This cycle is repeated until all of the required data registers have been written. Any number of data latches can be written. Each data byte is transferred to an internal holding latch upon the return of an Acknowledge. After all data bytes have been transferred to the LTC3219, the master may terminate the communication with a Stop condition. Alternatively, a Repeat-Start condition can be initiated by the master and another chip on the I²C bus can be addressed. This cycle can continue indefinitely and the LTC3219 will remember the last input of valid data that it received. Once all chips on the bus have been addressed and sent valid data, a global Stop condition can be sent and the LTC3219 will update all registers with the data that it had received.

In certain circumstances the data on the I²C bus may become corrupted. In these cases the LTC3219 responds appropriately by preserving only the last set of complete data that it has received. For example, assume the LTC3219 has been successfully addressed and is receiving data when a Stop condition mistakenly occurs. The LTC3219 will ignore this stop condition and will not respond until a new Start condition, correct address, sub-address and new set of data and Stop condition are transmitted.

Likewise, if the LTC3219 was previously addressed and sent valid data but not updated with a Stop, it will respond

## OPERATION

to any Stop that appears on the bus with only one exception, independent of the number of Repeat-Start's that have occurred. If a Repeat-Start is given and the LTC3219 successfully acknowledges its address and first byte, it will not respond to a Stop until all bytes of the new data have been received and acknowledged.

### Quick Write

Registers REG1 to REG9 can be written in parallel by setting Bit 1 of REG 0 high. When this bit is set high the next write sequence to REG1 will write the data to REG1 through REG9 which is all of the universal LED registers.

## APPLICATIONS INFORMATION

### $V_{BAT}$, CPO Capacitor Selection

The style and value of the capacitors used with the LTC3219 determine several important parameters such as regulator control loop stability, output ripple, charge pump strength and minimum start-up time.

To reduce noise and ripple, it is recommended that low equivalent series resistance (ESR) ceramic capacitors are used for both $C_{VBAT}$ and $C_{CPO}$. Tantalum and aluminum capacitors are not recommended due to high ESR.

The value of $C_{CPO}$ directly controls the amount of output ripple for a given load current. Increasing the size of $C_{CPO}$ will reduce output ripple at the expense of higher start-up current. The peak-to-peak output ripple of the 1.5x mode is approximately given by the expression:

$$V_{RIPPLEP-P} = \frac{I_{OUT}}{3f_{OSC} \bullet C_{CPO}} \quad (3)$$

where $f_{OSC}$ is the LTC3219 oscillator frequency, typically 850kHz, and $C_{CPO}$ is the output storage capacitor.

The output ripple in 2x mode is very small due to the fact that load current is supplied on both cycles of the clock.

Both style and value of the output capacitor can significantly affect the stability of the LTC3219. As shown in the Block Diagram, the LTC3219 uses a control loop to adjust the strength of the charge pump to match the required output current. The error signal of the loop is stored directly on the output capacitor. The output capacitor also serves as the dominant pole for the control loop. To prevent ringing or instability, it is important for the output capacitor to maintain at least 1.6µF of capacitance over all conditions and the ESR should be less than 80mΩ.

Multilayer ceramic chip capacitors typically have exceptional ESR performance. MLCC's combined with a tight board layout will result in very good stability. As the value of $C_{CPO}$ controls the amount of output ripple, the value of $C_{VBAT}$ controls the amount of ripple present at the input pin, $V_{BAT}$. The LTC3219 input current will be relatively constant while the charge pump is either in the input charging phase or the output charging phase but will drop to zero during the clock nonoverlap times. Since the nonoverlap time is small (~25ns), these missing "notches" will result in only a small perturbation on the input power supply line. Note that a higher ESR capacitor such as tantalum will have higher input noise due to the higher ESR. Therefore, ceramic capacitors are recommended for low ESR. Input noise can be further reduced by powering the LTC3219 through a very small series inductor as shown in Figure 4. A 10nH inductor will reject the fast current notches, thereby presenting a nearly constant current load to the input power supply. For economy, the 10nH inductor can be fabricated on the PC board with about 1cm (0.4") of PC board trace.

## APPLICATIONS INFORMATION

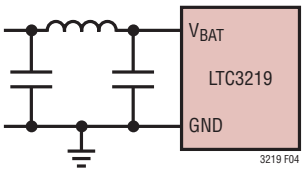



**Figure 4. 10nH Inductor Used for Input Noise Reduction (Approximately 1cm of Board Trace)**

### Flying Capacitor Selection

**Warning: Polarized capacitors such as tantalum or aluminum should never be used for the flying capacitors since their voltage can reverse upon start-up of the LTC3219. Ceramic capacitors should always be used for the flying capacitors.**

The flying capacitors control the strength of the charge pump. In order to achieve the rated output current it is necessary to have at least 1µF of capacitance for each of the flying capacitors. Capacitors of different materials lose their capacitance with higher temperature and voltage at different rates. For example, a ceramic capacitor made of X7R material will retain most of its capacitance from –40°C to 85°C whereas a Z5U or Y5V style capacitor will lose considerable capacitance over that range. Z5U and Y5V capacitors may also have a very poor voltage coefficient causing them to lose 60% or more of their capacitance when the rated voltage is applied. Therefore, when comparing different capacitors, it is often more appropriate to compare the amount of achievable capacitance for a given case size rather than comparing the specified capacitance value. For example, over rated voltage and temperature conditions, a 1µF, 10V, Y5V ceramic capacitor in a 0603 case may not provide any more capacitance than a 0.22µF, 10V, X7R available in the same case. The capacitor manufacturer's data sheet should be consulted to determine what value of capacitor is needed to ensure minimum capacitances at all temperatures and voltages.

Table 1 shows a list of ceramic capacitor manufacturers and how to contact them:

**Table 1. Recommended Capacitor Vendors**

| | |
|---|---|
| AVX | www.avxcorp.com |
| Kemet | www.kemet.com |
| Murata | www.murata.com |
| Taiyo Yuden | www.t-yuden.com |
| Vishay | www.vishay.com |

### Layout Considerations and Noise

The LTC3219 has been designed to minimize EMI. However due to its high switching frequency and the transient currents produced by the LTC3219, careful board layout is necessary. A true ground plane and short connections to all capacitors will improve performance and ensure proper regulation under all conditions.

The flying capacitor pins C1P, C2P, C1M and C2M have controlled edge rate waveforms. The large dv/dt on these pins can couple energy capacitively to adjacent PCB runs. Magnetic fields can also be generated if the flying capacitors are not close to the LTC3219 (i.e., the loop area is large). To decouple capacitive energy transfer, a Faraday shield may be used. This is a grounded PCB trace between the sensitive node and the LTC3219 pins. For a high quality AC ground, it should be returned to a solid ground plane that extends all the way to the LTC3219.

## APPLICATIONS INFORMATION

### Power Efficiency

To calculate the power efficiency (η) of an LED driver chip, the LED power should be compared to the input power. The difference between these two numbers represents lost power whether it is in the charge pump or the current sources. Stated mathematically, the power efficiency is given by:

$$\eta = \frac{P_{LED}}{P_{IN}} \quad (4)$$

The efficiency of the LTC3219 depends upon the mode in which it is operating. Recall that the LTC3219 operates as a pass switch, connecting $V_{BAT}$ to CPO, until dropout is detected at the $I_{LED}$ pin. This feature provides the optimum efficiency available for a given input voltage and LED forward voltage. When it is operating as a switch, the efficiency is approximated by:

$$\eta = \frac{P_{LED}}{P_{IN}} = \frac{V_{LED} \bullet I_{LED}}{V_{BAT} \bullet I_{BAT}} = \frac{V_{LED}}{V_{BAT}} \quad (5)$$

since the input current will be very close to the sum of the LED currents.

At moderate to high output power, the quiescent current of the LTC3219 is negligible and the expression above is valid.

Once dropout is detected at any LED pin, the LTC3219 enables the charge pump in 1.5x mode.

In 1.5x boost mode, the efficiency is similar to that of a linear regulator with an effective input voltage of 1.5 times the actual input voltage. This is because the input current for a 1.5x charge pump is approximately 1.5 times the load current. In an ideal 1.5x charge pump, the power efficiency would be given by:

$$\eta_{IDEAL} = \frac{P_{LED}}{P_{IN}} = \frac{V_{LED} \bullet I_{LED}}{V_{BAT} \bullet 1.5 \bullet I_{LED}} = \frac{V_{LED}}{1.5 \bullet V_{BAT}}$$

Similarly, in 2x boost mode, the efficiency is similar to that of a linear regulator with an effective input voltage of 2 times the actual input voltage. In an ideal 2x charge pump, the power efficiency would be given by:

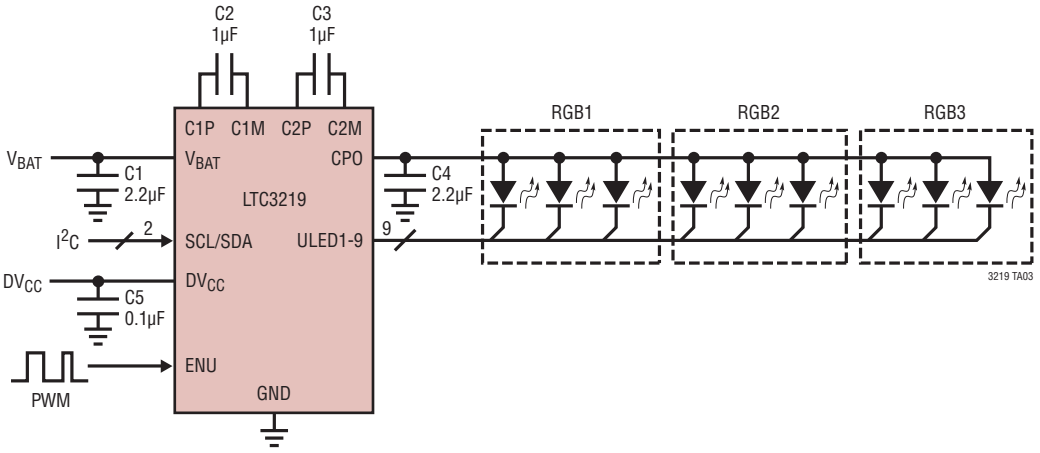
$$\eta_{IDEAL} = \frac{P_{LED}}{P_{IN}} = \frac{V_{LED} \bullet I_{LED}}{V_{BAT} \bullet 2 \bullet I_{LED}} = \frac{V_{LED}}{2 \bullet V_{BAT}}$$

### Thermal Management

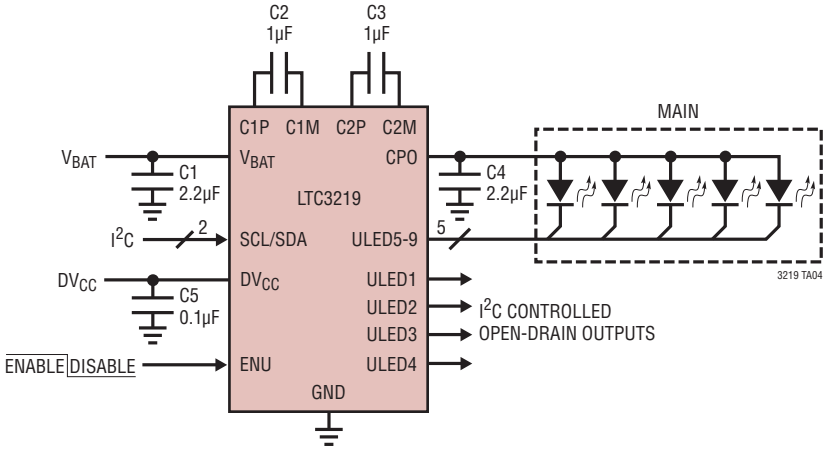
For higher input voltages and maximum output current, there can be substantial power dissipation in the LTC3219. If the junction temperature increases above approximately 150°C the thermal shutdown circuitry will automatically deactivate the output current sources and charge pump. To reduce maximum junction temperature, a good thermal connection to the PC board is recommended. Connecting the Exposed Pad to a ground plane and maintaining a solid ground plane under the device will reduce the thermal resistance of the package and PC board considerably.

# TYPICAL APPLICATIONS

### Three RGB LED Groups

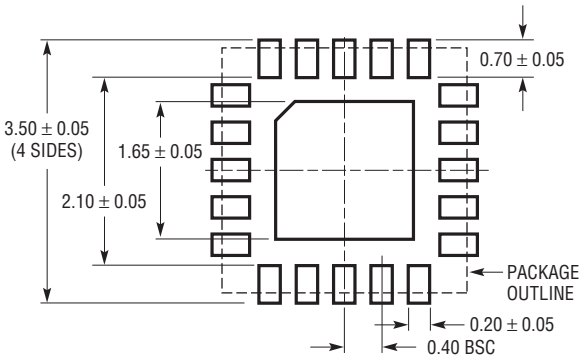



### 5-LED Main, 4 General Purpose Open-Drain Outputs



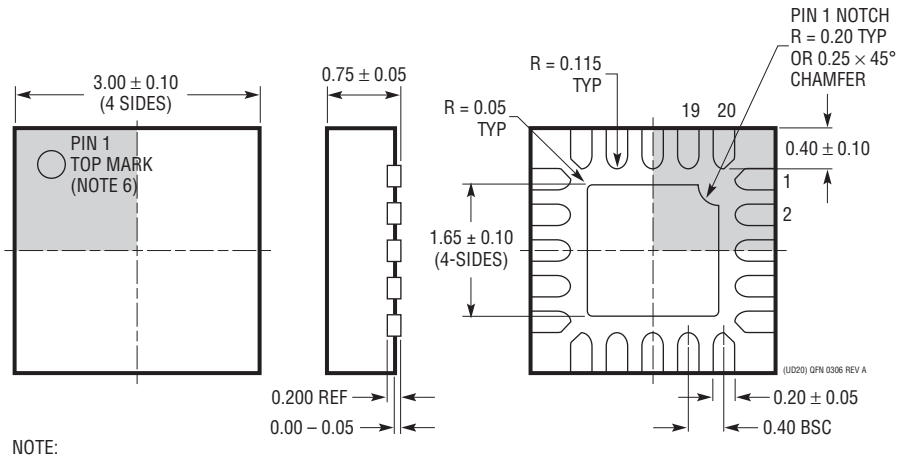
# PACKAGE DESCRIPTION

**UD Package**
**20-Lead Plastic QFN (3mm × 3mm)**
(Reference LTC DWG # 05-08-1720 Rev A)




RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

BOTTOM VIEW—EXPOSED PAD




NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE