Dual Input USB/AC Adapter Li-Ion Battery Charger with 600mA Buck Converter

FEATURES

- **Charges Single-Cell Li-Ion Battery from Wall Adapter and USB Inputs**
- **Automatic Input Power Detection and Selection**
- **Charge Current Programmable Up to 950mA from Wall Adapter Input**
- **Adjustable Output, High Efficiency 600mA Synchronous DC/DC Converter**
- **No External MOSFET, Sense Resistor or Blocking Diode Needed**
- Thermal Regulation Maximizes Charge Rate Without Risk of Overheating*
- Preset Charge Voltage with ±0.6% Accuracy
- Programmable Charge Current Termination
- 1.5MHz Constant Frequency Operation (Step-Down Converter)
- 18µA USB Suspend Current in Shutdown
- "Power Present" Status Output
- Charge Status Output
- Automatic Recharge
- Available in a Thermally Enhanced, Low Profile (0.75mm) 16-Lead (5mm × 3mm) DFN Package

APPLICATIONS

- Cellular Telephones

DESCRIPTION

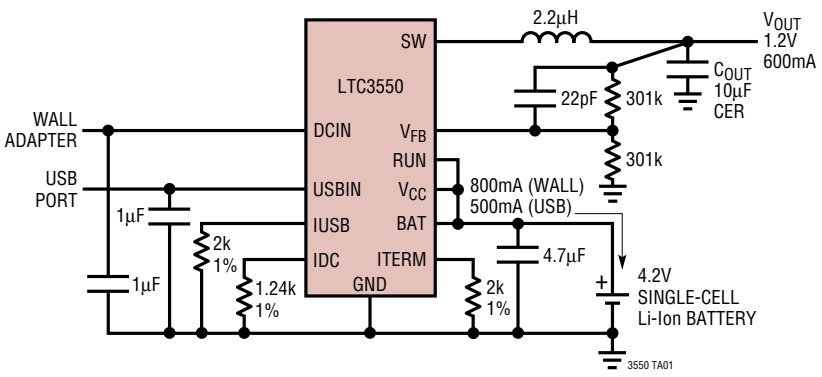
The LTC®3550 is a standalone linear charger with a 600mA monolithic synchronous buck converter. It is capable of charging a single-cell Li-Ion battery from both wall adapter and USB inputs. The charger automatically selects the appropriate power source for charging.

Internal thermal feedback regulates the battery charge current to maintain a constant die temperature during high power operation or high ambient temperature conditions. The float voltage is fixed at 4.2V and the charge currents are programmed with external resistors. The LTC3550 terminates the charge cycle when the charge current drops below the programmed termination threshold after the final float voltage is reached. With power applied to both inputs, the LTC3550 can be put into shutdown mode reducing the DCIN supply current to 20µA, the USBIN supply current to 10µA, and the battery drain current to less than 2µA.

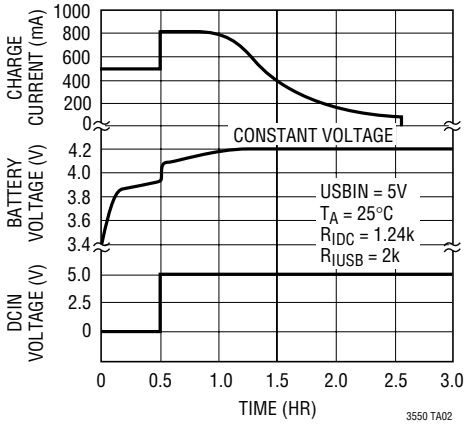
The DC/DC converter switching frequency is internally set at 1.5MHz, allowing the use of small surface mount inductors and capacitors.

TYPICAL APPLICATION

Dual Input Battery Charger and DC/DC Converter



Complete Charge Cycle (1100mA Battery)

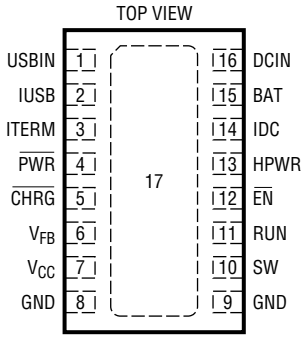


ABSOLUTE MAXIMUM RATINGS

(Note 1)

DCIN, USBIN ..... –0.3V to 10V
$\overline{EN}$, $\overline{CHRG}$, $\overline{PWR}$, HPWR ..... –0.3V to 10V
BAT, IDC, IUSB, ITERM ..... –0.3V to 7V
V_{CC} ..... –0.3V to 6V
RUN, V_{FB} ..... –0.3V to V_{CC}
SW (DC) ..... –0.3V to (V_{CC} + 0.3V)
DCIN Pin Current (Note 2) 1A
USBIN Pin Current (Note 2) 700mA
BAT Pin Current (Note 2) 1A
P-Channel SW Source Current (DC) 800mA
N-Channel SW Source Current (DC) 800mA
Peak SW Sink and Source Current 1.3A
Operating Temperature Range (Note 3) ... –40°C to 85°C
Maximum Junction Temperature ..... 125°C
Storage Temperature Range ..... –65°C to 125°C

PACKAGE/ORDER INFORMATION



DHC PACKAGE
16-LEAD (5mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 40°C (NOTE 4)
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER PART NUMBER	DHC PART MARKING
LTC3550EDHC	3550

Order Options Tape and Reel: Add #TR
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DCIN} = 5V, V_{USBIN} = 5V, V_{CC} = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DCIN}	Wall Adapter Input Supply Voltage		●	4.3		8	V
V_{USBIN}	USB Port Input Supply Voltage		●	4.3		8	V
V_{CC}	Buck Regulator Input Supply Voltage		●	2.5		5.5	V
$V_{\overline{EN}}$	$\overline{EN}$ Input Threshold Voltage			0.4	0.7	1.0	V
$R_{\overline{EN}}$	$\overline{EN}$ Pull-Down Resistance			1.2	2	5	MΩ
V_{RUN}	RUN Threshold Voltage		●	0.3	1	1.5	V
I_{RUN}	RUN Leakage Current		●		±0.01	±1	µA
$V_{\overline{CHRG}}$	$\overline{CHRG}$ Output Low Voltage	$I_{\overline{CHRG}}$ = 5mA			0.35	0.6	V
$V_{\overline{PWR}}$	$\overline{PWR}$ Output Low Voltage	$I_{\overline{PWR}}$ = 5mA			0.35	0.6	V
V_{HPWR}	HPWR Input Threshold Voltage			0.4	0.7	1	V
R_{HPWR}	HPWR Pull-Down Resistance		●	1	2	5	MΩ
V_{UVDC}	DCIN Undervoltage Lockout Voltage	From Low to High Hysteresis		4.0	4.15 200	4.3	V mV
V_{UVUSB}	USBIN Undervoltage Lockout Voltage	From Low to High Hysteresis		3.8	3.95 200	4.1	V mV
V_{ASD-DC}	V_{DCIN} – V_{BAT} Lockout Threshold Voltage	V_{DCIN} from Low to High, V_{BAT} = 4.2V V_{DCIN} from High to Low, V_{BAT} = 4.2V		140 20	180 50	220 80	mV mV
$V_{ASD-USB}$	V_{USBIN} – V_{BAT} Lockout Threshold Voltage	V_{USBIN} from Low to High, V_{BAT} = 4.2V V_{USBIN} from High to Low, V_{BAT} = 4.2V		140 20	180 50	220 80	mV mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DCIN} = 5V, V_{USBIN} = 5V, V_{CC} = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Battery Charger							
I_{DCIN}	DCIN Supply Current						
	Charge Mode (Note 5)	R_{IDC} = 10k	●		250	800	µA
	Standby Mode	Charge Terminated	●		50	100	µA
	Shutdown Mode	ENABLE = 5V			20	40	µA
I_{USBIN}	USBIN Supply Current						
	Charge Mode (Note 6)	R_{IUSB} = 10k, V_{DCIN} = 0V	●		250	800	µA
	Standby Mode	Charge Terminated	●		50	100	µA
	Shutdown Mode	V_{DCIN} = 0V, ENABLE = 0V			18	36	µA
	Shutdown Mode	V_{DCIN} > V_{USBIN}			10	20	µA
V_{FLOAT}	Regulated Output (Float) Voltage	I_{BAT} = 1mA		4.175	4.2	4.225	V
		I_{BAT} = 1mA, 0°C < T_A < 85°C		4.158	4.2	4.242	V
I_{BAT}	BAT Pin Current						
	Constant-Current Mode	R_{IDC} = 1.25k	●	760	800	840	mA
	Constant-Current Mode	R_{IUSB} = 2.1k	●	450	476	500	mA
	Constant-Current Mode	R_{IDC} = 10k or R_{IUSB} = 10k	●	93	100	107	mA
	Standby Mode	Charge Terminated			–3	–6	µA
	Shutdown Mode	Charger Disabled			–1	–2	µA
	Sleep Mode	DCIN = 0V, USBIN = 0V			±1	±2	µA
V_{IDC}	IDC Pin Regulated Voltage	Constant-Current Mode		0.95	1.0	1.05	V
V_{IUSB}	IUSB Pin Regulated Voltage	Constant-Current Mode		0.95	1.0	1.05	V
$I_{TERMINATE}$	Charge Current Termination Threshold	R_{ITERM} = 1k	●	90	100	110	mA
		R_{ITERM} = 2k	●	45	50	55	mA
		R_{ITERM} = 10k	●	8.5	10	11.5	mA
		R_{ITERM} = 20k	●	4	5	6	mA
I_{TRIKL}	Trickle Charge Current	V_{BAT} < V_{TRIKL}; R_{IDC} = 1.25k		60	80	100	mA
		V_{BAT} < V_{TRIKL}; R_{IUSB} = 2.1k		30	47.5	65	mA
V_{TRIKL}	Trickle Charge Threshold Voltage	V_{BAT} Rising		2.8	2.9	3	V
		Hysteresis			100		mV
ΔV_{RECHRG}	Recharge Battery Threshold Voltage	V_{FLOAT} – V_{RECHRG}, 0°C < T_A < 85°C		65	100	135	mV
t_{RECHRG}	Recharge Comparator Filter Time	V_{BAT} from High to Low		3	6	9	ms
$t_{TERMINATE}$	Termination Comparator Filter Time	I_{BAT} Drops Below Termination Threshold		0.8	1.5	2.2	ms
t_{SS}	Soft-Start Time	I_{BAT} = 10% to 90% Full-Scale		175	250	325	µs
R_{ON-DC}	Power FET On-Resistance (Between DCIN and BAT)				400		mΩ
R_{ON-USB}	Power FET On-Resistance (Between USBIN and BAT)				550		mΩ
T_{LIM}	Junction Temperature in Constant-Temperature Mode				105		°C
Switching Regulator							
V_{FB}	Regulated Feedback Voltage	T_A = 25°C		0.5880	0.6	0.6120	V
		0°C ≤ T_A ≤ 85°C		0.5865	0.6	0.6135	V
		–40°C ≤ T_A ≤ 85°C	●	0.5850	0.6	0.6150	V
ΔV_{FB}	Reference Voltage Line Regulation		●		0.04	0.4	%/V
I_{PK}	Peak Inductor Current	V_{CC} = 3V, V_{FB} = 0.5V		0.75	1	1.25	A
$V_{LOADREG}$	Output Voltage Load Regulation				0.5		%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{DCIN} = 5V, V_{USBIN} = 5V, V_{CC} = 3.6V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_S	V_{CC} Supply Current Active Mode Sleep Mode Shutdown	(Note 7) V_{FB} = 0.5V, I_{LOAD} = 0A V_{FB} = 0.62V, I_{LOAD} = 0A V_{RUN} = 0V, V_{CC} = 5.5V			 300 20 0.1	 400 35 1	 µA µA µA
f_{OSC}	Oscillator Frequency	V_{FB} = 0.6V V_{FB} = 0V		1.2	1.5 210	1.8	MHz kHz
R_{PFET}	$R_{DS(ON)}$ of P-Channel FET				0.4		Ω
R_{NFET}	$R_{DS(ON)}$ of N-Channel FET				0.35		Ω
I_{LSW}	SW Leakage Current				0.01	±1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Guaranteed by long term current density limitations.

Note 3: The LTC3550E is guaranteed to meet the performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 4: Failure to solder the exposed backside of the package to the PC board will result in a thermal resistance much higher than 40°C/W. See Thermal Considerations.

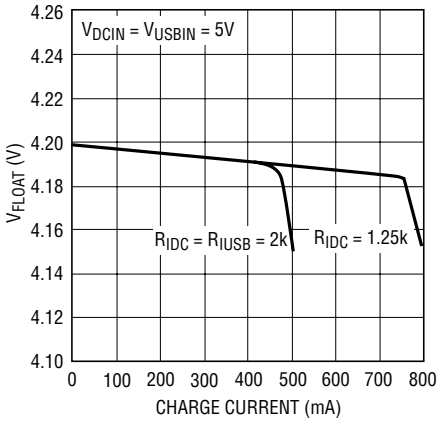
Note 5: Supply Current includes IDC and ITERM pin current (approximately 100µA each) but does not include any current delivered to the battery through the BAT pin (approximately 100mA).

Note 6: Supply Current includes IUSB and ITERM pin current (approximately 100µA each) but does not include any current delivered to the battery through the BAT pin (approximately 100mA).

Note 7: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

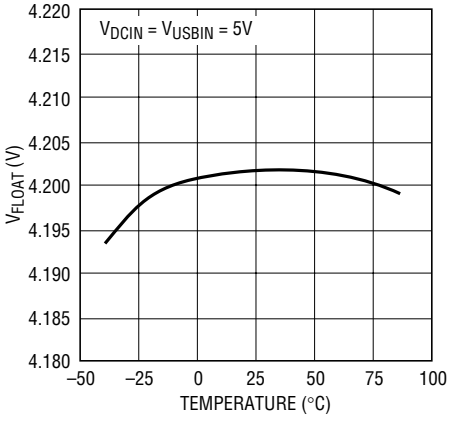
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Regulated Charger Output (Float) Voltage vs Charge Current



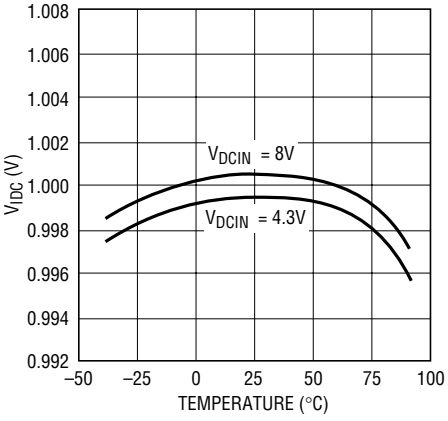
3550 G01

Regulated Charger Output (Float) Voltage vs Temperature



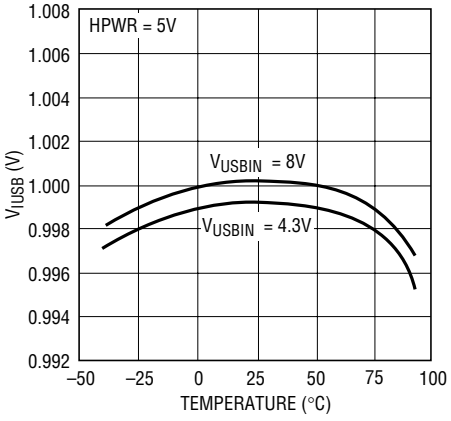
3550 G02

IDC Pin Voltage vs Temperature (Constant-Current Mode)



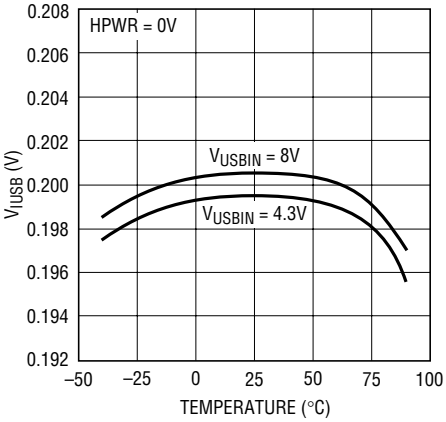
3550 G03

IUSB Pin Voltage vs Temperature (Constant-Current Mode)



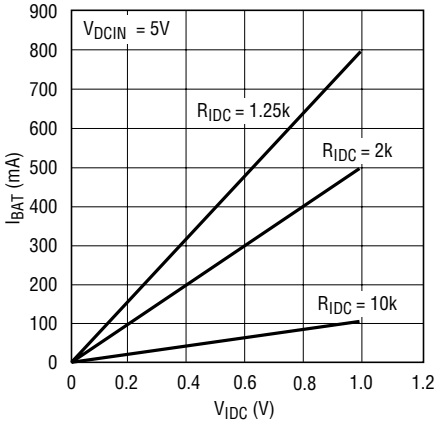
3550 G04

IUSB Pin Voltage vs Temperature (Constant-Current Mode)



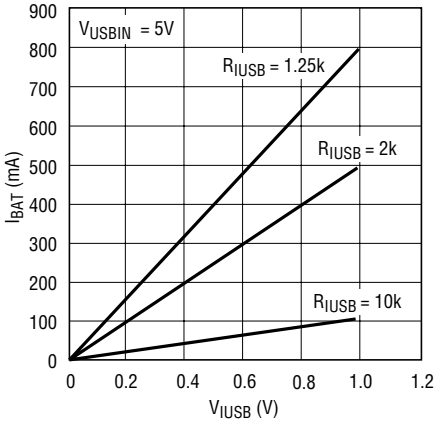
3550 G43

Charge Current vs IDC Pin Voltage



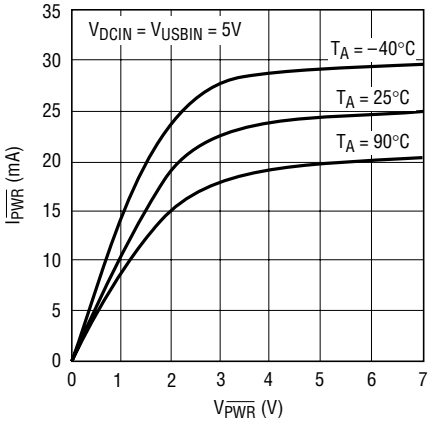
3550 G05

Charge Current vs IUSB Pin Voltage



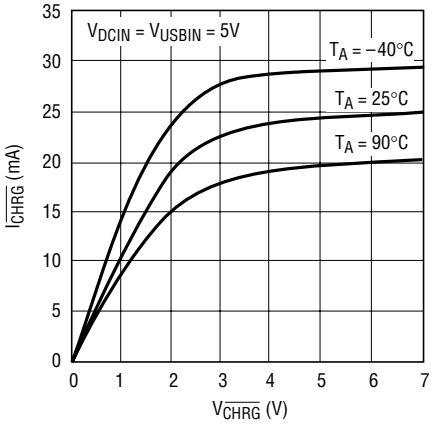
3550 G06

$\overline{PWR}$ Pin I-V Curve



3550 G07

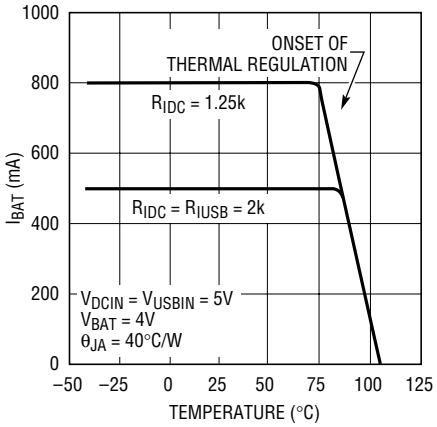
$\overline{CHRG}$ Pin I-V Curve



3550 G08

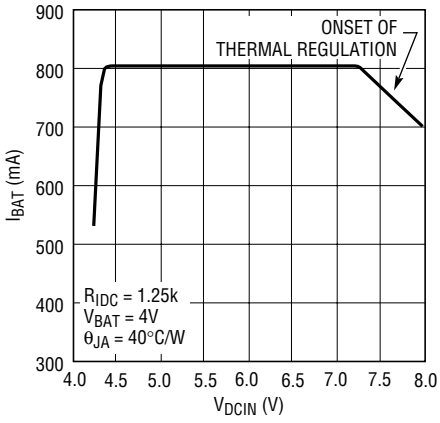
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Charge Current vs Ambient Temperature



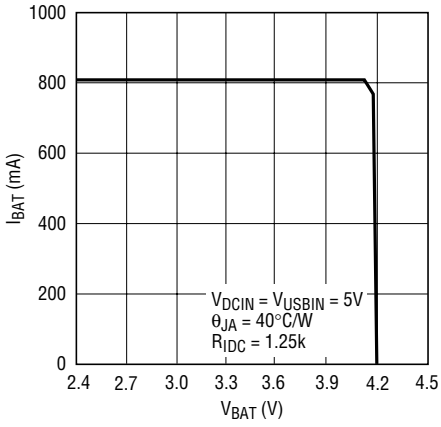
3550 G10

Charge Current vs DCIN Voltage



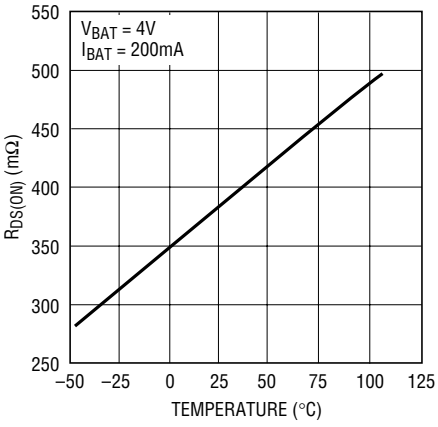
3550 G11

Charge Current vs Battery Voltage



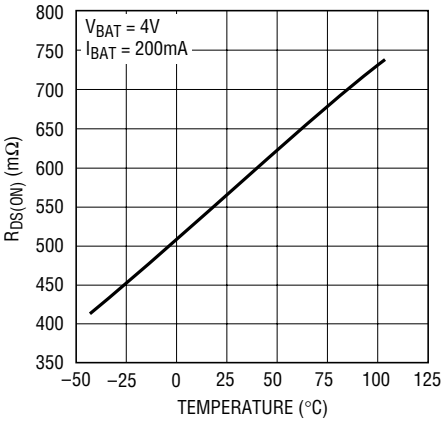
3550 G12

DCIN Power FET On-Resistance vs Temperature



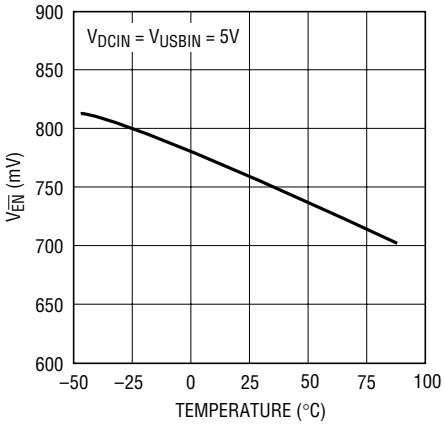
3550 G13

USBIN Power FET On-Resistance vs Temperature



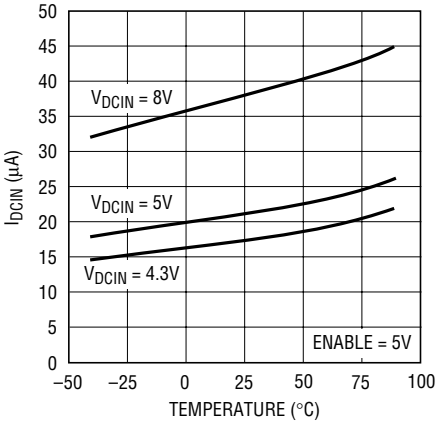
3550 G14

$\overline{EN}$ Pin Threshold Voltage (On-to-Off) vs Temperature



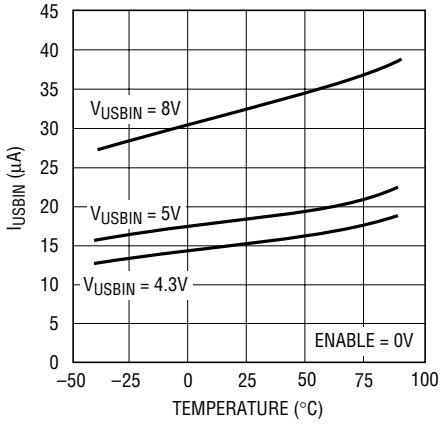
3550 G15

DCIN Shutdown Current vs Temperature



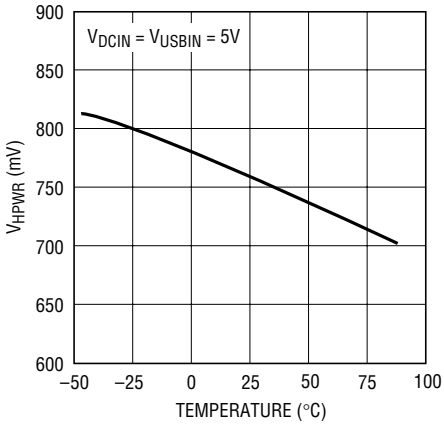
3550 G16

USBIN Shutdown Current vs Temperature



3550 G17

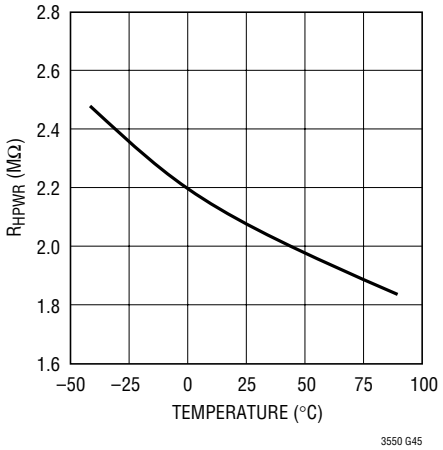
HPWR Pin Threshold Voltage (Rising) vs Temperature



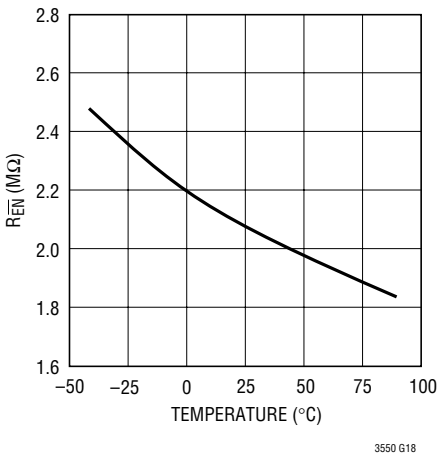
3550 G44

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

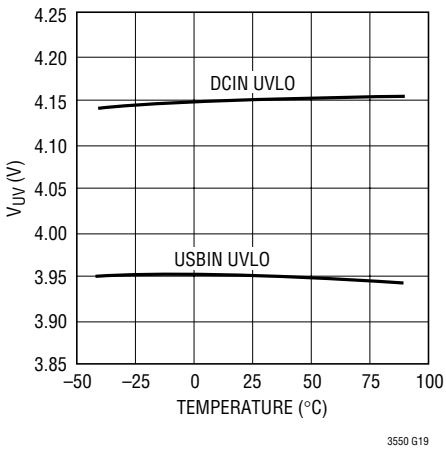
HPWR Pin Pull-Down Resistance vs Temperature



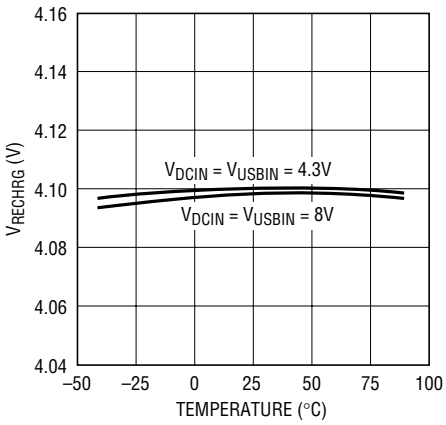
$\overline{EN}$ Pin Pull-Down Resistance vs Temperature



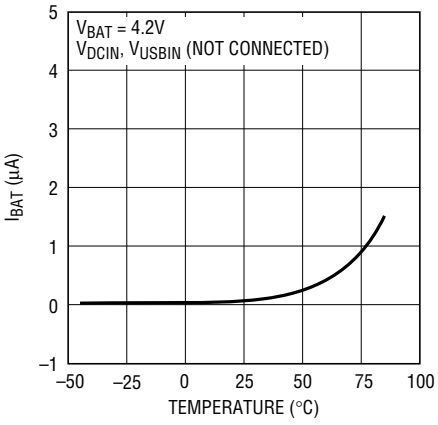
Undervoltage Lockout Threshold vs Temperature



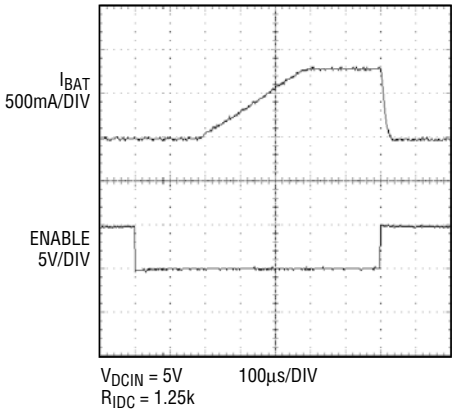
Recharge Threshold Voltage vs Temperature



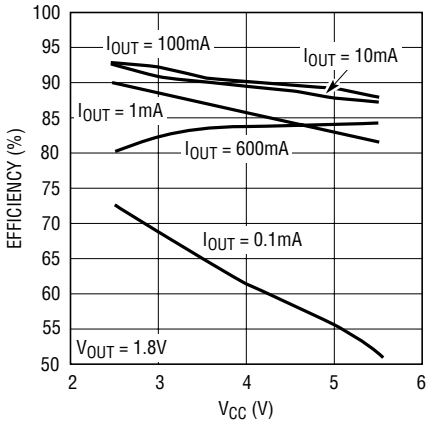
Battery Drain Current vs Temperature



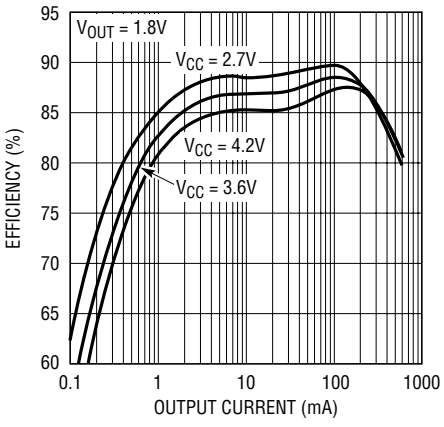
Charge Current During Turn-On and Turn-Off



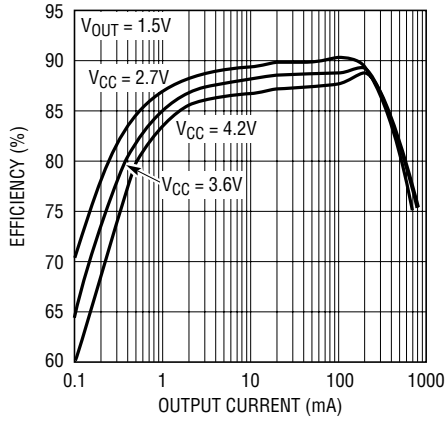
Buck Regulator Efficiency vs V_{CC}



Buck Regulator Efficiency vs Output Current



Buck Regulator Efficiency vs Output Current



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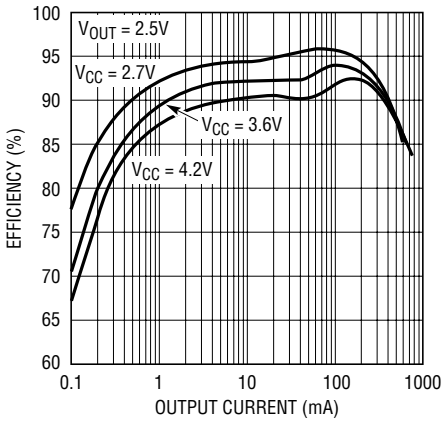
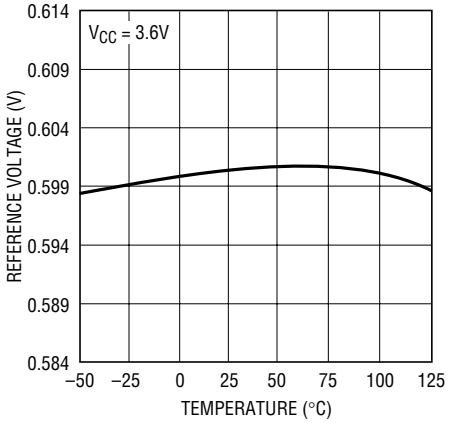
Buck Regulator Efficiency vs Output Current



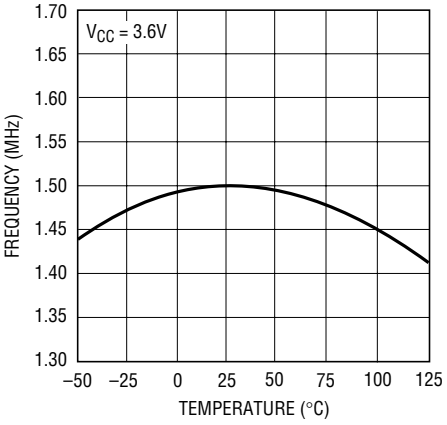
3550 G26

Buck Regulator Reference Voltage vs Temperature



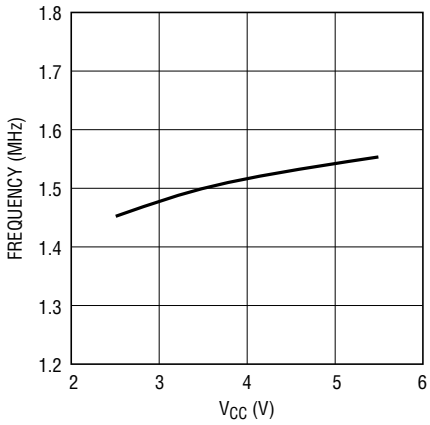
3550 G27

Oscillator Frequency vs Temperature



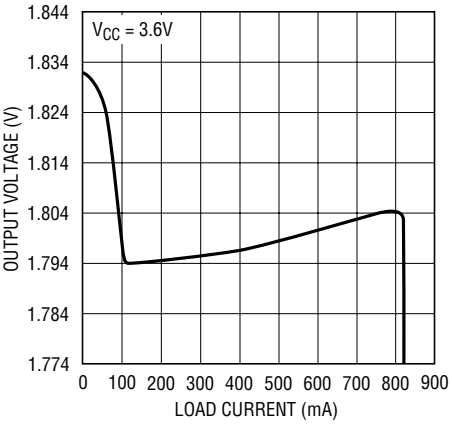
3550 G28

Oscillator Frequency vs V_{CC}



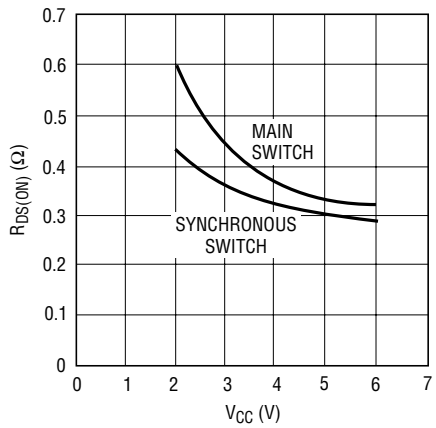
3550 G29

Buck Regulator Output Voltage vs Load Current



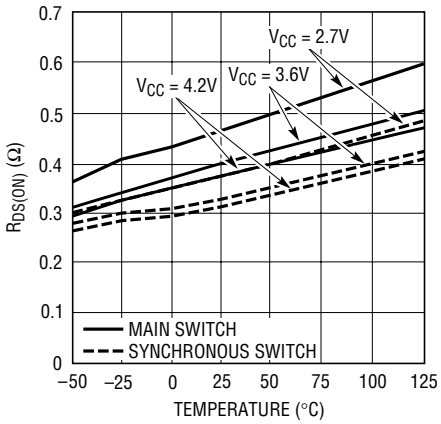
3550 G30

$R_{DS(ON)}$ vs V_{CC}



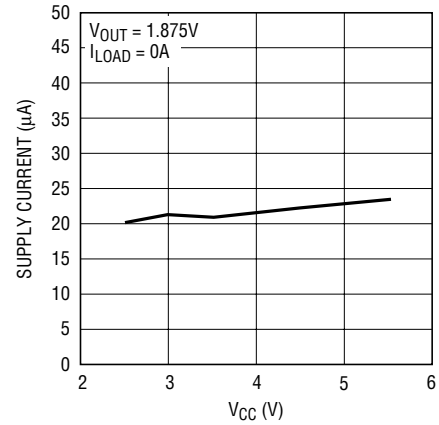
3550 G31

Buck Regulator Switches $R_{DS(ON)}$ vs Temperature



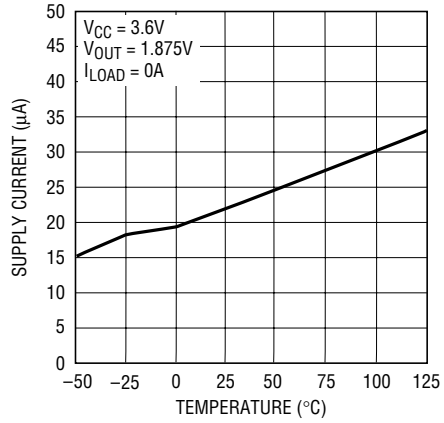
3550 G32

Buck Regulator Supply Current vs V_{CC}



3550 G33

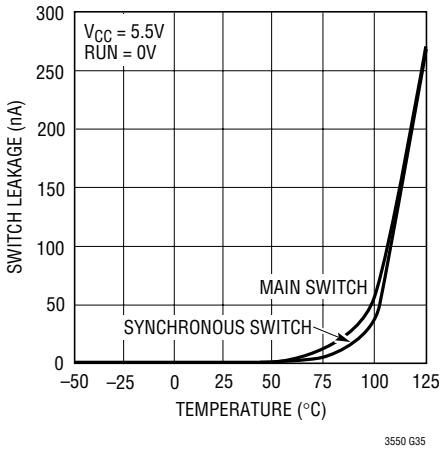
Buck Regulator Supply Current vs Temperature



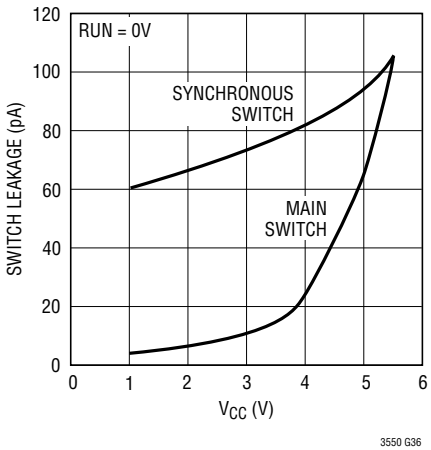
3550 G34

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

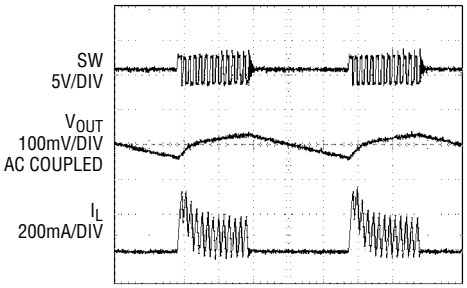
Switch Leakage Current vs Temperature



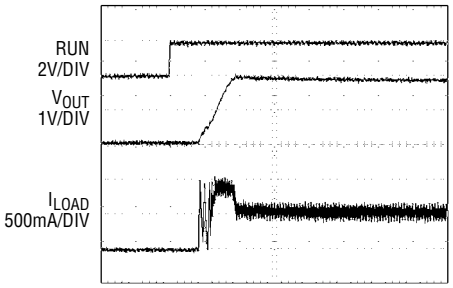
Switch Leakage Current vs V_{CC}



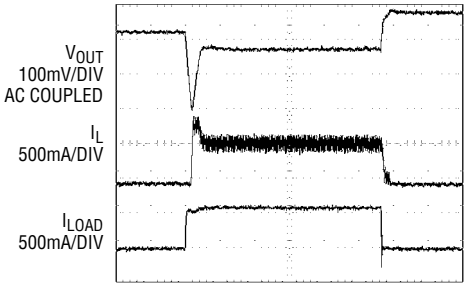
Burst Mode Operation



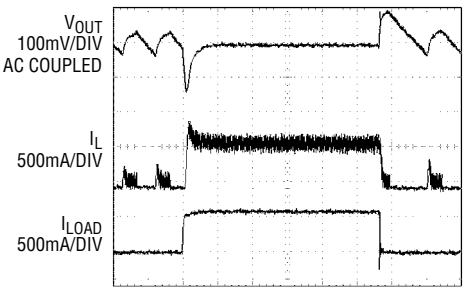
Start-Up from Shutdown



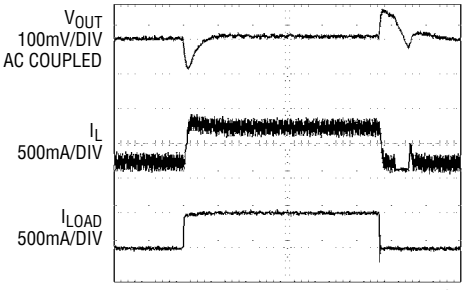
Load Step



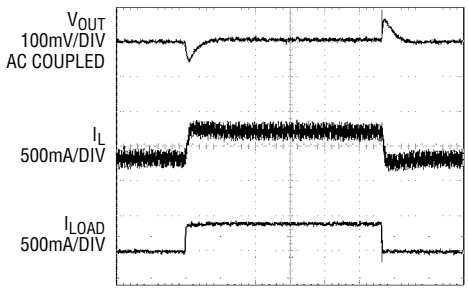
Load Step



Load Step



Load Step



PIN FUNCTIONS

USBIN (Pin 1): USB Input Supply Pin. Provides power to the battery charger. The maximum supply current is 650mA. This should be bypassed with a 1µF capacitor.

IUSB (Pin 2): USB Charge Current Program and Monitor Pin. The charge current can be set by connecting a resistor, R_{IUSB}, to ground. When charging in constant-current mode, this pin servos to 1V. The voltage on this pin can be used to measure the charge current delivered from the USB input using the following formula:

$$I_{BAT} = \frac{V_{IUSB}}{R_{IUSB}} \bullet 1000$$

ITERM (Pin 3): Termination Current Threshold Program Pin. The current termination threshold, $I_{TERMINATE}$, can be set by connecting a resistor, R_{ITERM}, to ground. $I_{TERMINATE}$ is set by the following formula:

$$I_{TERMINATE} = \frac{100V}{R_{ITERM}}$$

When the charge current, I_{BAT}, falls below the termination threshold, charging stops and the $\overline{CHRG}$ output becomes high impedance.

This pin is internally clamped to approximately 1.5V. Driving this pin to voltages beyond the clamp voltage should be avoided.

$\overline{PWR}$ (Pin 4): Open-Drain Power Supply Status Output. When the DCIN or USBIN pin voltage is sufficient to begin charging (i.e., when the supply is greater than the undervoltage lockout threshold and at least 180mV above the battery terminal), the $\overline{PWR}$ pin is pulled low by an internal N-channel MOSFET. Otherwise, $\overline{PWR}$ is high impedance. The output is capable of sinking up to 10mA, making it suitable for driving an LED.

$\overline{CHRG}$ (Pin 5): Open-Drain Charge Status Output. When the LTC3550 is charging, the $\overline{CHRG}$ pin is pulled low by an internal N-channel MOSFET. When the charge cycle is completed, $\overline{CHRG}$ becomes high impedance. This output is capable of sinking up to 10mA, making it suitable for driving an LED.

V_{FB} (Pin 6): Voltage Feedback Pin. Receives the feedback voltage from an external resistor divider across the buck regulator output.

V_{CC} (Pin 7): Buck Regulator Input Supply Pin. Must be closely decoupled to GND (Pins 8, 9) with a 2.2µF or greater ceramic capacitor.

GND (Pins 8, 9): Ground.

SW (Pin 10): Buck Regulator Switch Node Connection to Inductor. This pin connects to the drains of the internal main (top) and synchronous (bottom) power MOSFET switches.

RUN (Pin 11): Buck Regulator Run Control Input. Forcing this pin above 1.5V enables the regulator. Forcing this pin below 0.3V shuts it down. In shutdown, all buck regulator functions are disabled drawing <1µA supply current from V_{CC}. Do not leave RUN floating.

$\overline{EN}$ (Pin 12): Charger Enable Input. A logic low on this pin enables the charger. If this input is left floating, an internal 2MΩ pull-down resistor defaults the LTC3550 to charge mode. Pull this pin high to disable the charger.

HPWR (Pin 13): USB High/Low Power Mode Select Input. Used to control the amount of current drawn from the USB port. A logic high on the HPWR pin sets the charge current to 100% of the current programmed by the IUSB pin. A logic low on the HPWR pin sets the charge current to 20% of the current programmed by the IUSB pin. An internal 2MΩ pull-down resistor defaults the charger to its low current state.

IDC (Pin 14): Wall Adapter Charge Current Program and Monitor Pin. The charge current is set by connecting a resistor, R_{IDC}, to ground. When charging in constant-current mode, this pin servos to 1V. The voltage on this pin can be used to measure the charge current using the following formula:

$$I_{BAT} = \frac{V_{IDC}}{R_{IDC}} \bullet 1000$$

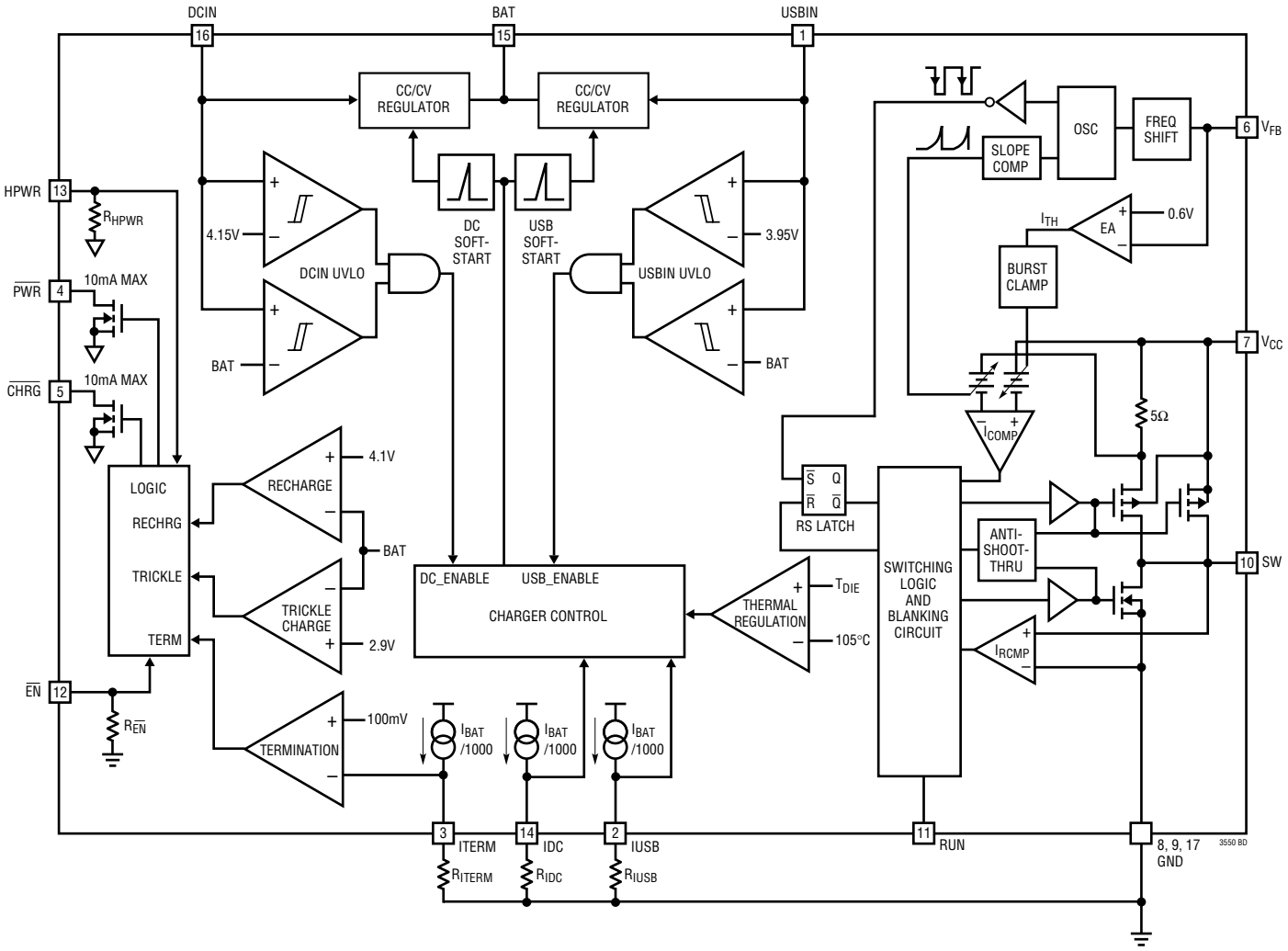
BAT (Pin 15): Charger Output. This pin provides charge current to the battery and regulates the final float voltage to 4.2V.

PIN FUNCTIONS

DCIN (Pin 16): Wall Adapter Input Supply Pin. Provides power to the battery charger. The maximum supply current is 950mA. This should be bypassed with a 1µF capacitor.

Exposed Pad (Pin 17): GND. The exposed backside of the package is ground and must be soldered to the PCB ground for electrical connection and maximum heat transfer.

BLOCK DIAGRAM



OPERATION

The LTC3550 consists of two main blocks: a lithium-ion battery charger and a high-efficiency buck converter that can be powered from the battery. The charger is designed to efficiently manage charging of a single-cell lithium-ion battery from two separate power sources: a wall adapter and USB power bus. The internal P-channel MOSFETs can supply up to 950mA from the wall adapter source and 500mA from the USB power source. The final float voltage accuracy is ±0.6%.

The buck converter uses a constant frequency, current mode step-down architecture. Both the main (P-channel MOSFET) and synchronous (N-channel MOSFET) switches for the buck converter are internal. The LTC3550 requires no external diodes or sense resistors.

Lithium-Ion Battery Charger

A charge cycle begins when the voltage at either the DCIN pin or USBIN pin rises above the UVLO threshold level and the charger is enabled through the $\overline{EN}$ pin. When either input is supplying power, logic low enables the charger and logic high disables it (a 2MΩ pull-down defaults the charger to the charging state). The DCIN input draws 20µA when the charger is in shutdown. The USBIN input draws 18µA during shutdown if no power is applied to DCIN, but draws only 10µA when $V_{DCIN} > V_{USBIN}$.

Once the charger is enabled, it enters constant-current mode, where the programmed charge current is supplied to the battery. When the BAT pin approaches the final float voltage (4.2V), the charger enters constant-voltage

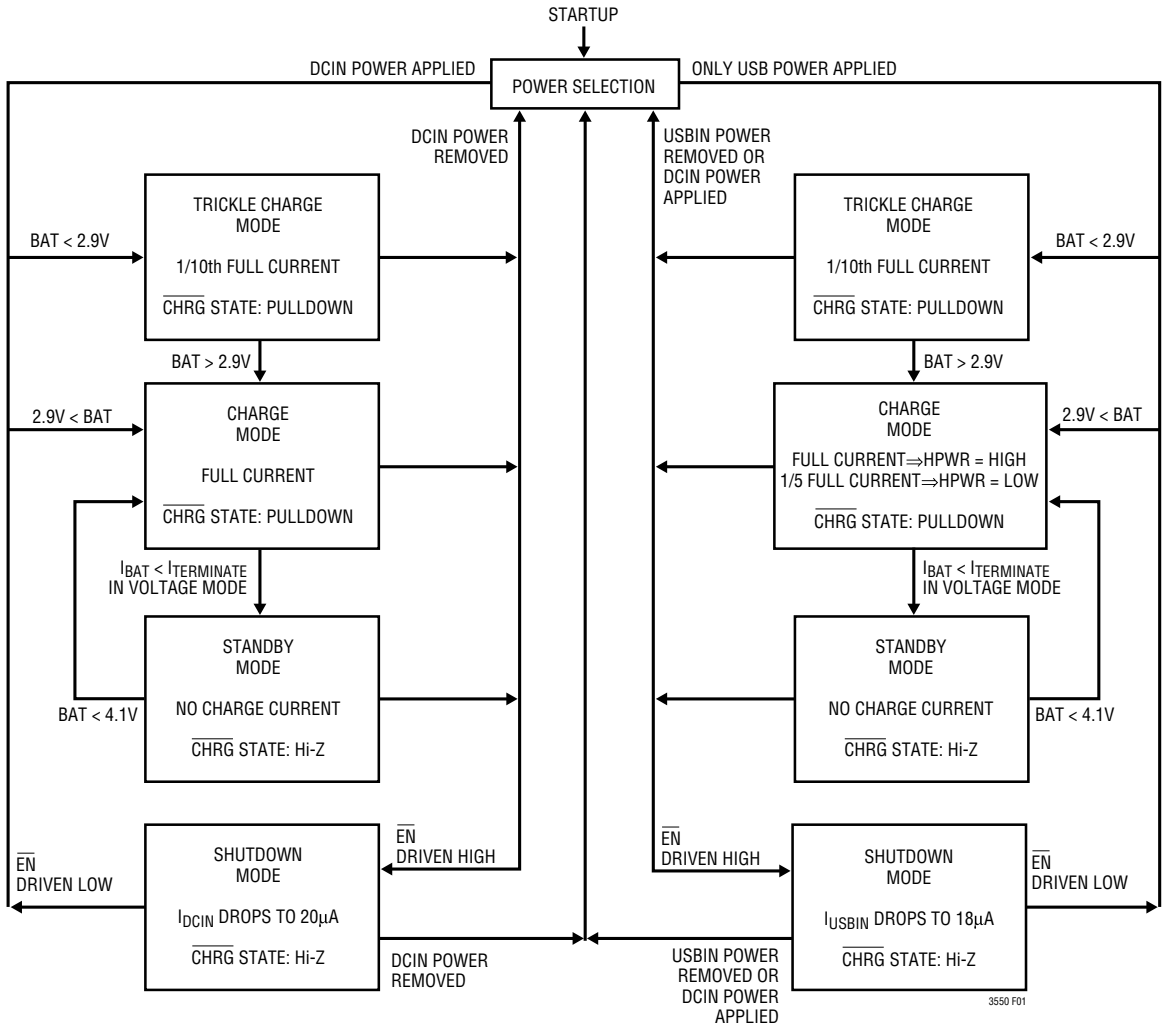


Figure 1. LTC3550 State Diagram of a Charge Cycle

OPERATION

mode and the charge current begins to decrease. Once the charge current drops below the programmed termination threshold (set by the external resistor R_{ITERM}), the internal P-channel MOSFET is shut off and the charger enters standby mode.

In standby mode, the charger sits idle and monitors the battery voltage using a comparator with a 6ms filter time (t_{RECHRG}). A charge cycle automatically restarts when the battery voltage falls below 4.1V (which corresponds to approximately 80% to 90% battery capacity). This ensures that the battery is kept near a fully charged condition and eliminates the need for periodic charge cycle initiations. Figure 1 uses a state diagram to describe the behavior of the LTC3550 battery charger.

600mA Step-Down Regulator

The LTC3550 regulator uses a constant frequency, current mode step-down architecture. Both the top (P-channel MOSFET) and bottom (N-channel MOSFET) switches are internal. During normal operation, the internal top power MOSFET is turned on each cycle when the oscillator sets the RS latch, and is turned off when the current comparator, I_{COMP}, resets the RS latch. The peak inductor current at which I_{COMP} resets the RS latch, is controlled by the output of error amplifier EA. When the load current increases, it causes a slight decrease in the output voltage (V_{OUT}), relative to the internal reference, which in turn causes the EA amplifier's output voltage to increase until the average inductor current matches the new load current. While the top MOSFET is off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current reversal comparator I_{RCMP}, or the beginning of the next clock cycle.

Burst Mode® Operation

The LTC3550 buck regulator is capable of Burst Mode operation in which the internal power MOSFETs operate intermittently based on load current demand.

In Burst Mode operation, the peak current of the inductor is set to approximately 200mA regardless of the output load. Each burst event can last from a few cycles at light loads to almost continuously cycling with short sleep intervals at moderate loads. In between these burst events, the power MOSFETs and any unneeded circuitry are turned off, reducing the quiescent current to 20µA. In this sleep state, the load current is being supplied solely from the output capacitor. As the output voltage droops, the EA amplifier's output rises above the sleep threshold signaling the BURST comparator to trip and turn the top MOSFET on. This process repeats at a rate that is dependent on the load demand.

Dropout Operation

As the input supply voltage decreases to a value approaching the output voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage forces the main switch to remain on for more than one cycle until it reaches 100% duty cycle. The output voltage will then be determined by the input voltage minus the voltage drop across the P-channel MOSFET and the inductor.

An important detail to remember is that at low input supply voltages, the $R_{DS(ON)}$ of the P-channel switch increases (see Typical Performance Characteristics). Therefore, the user should calculate the power dissipation when the LTC3550 is used at 100% duty cycle with low input voltage (See Thermal Considerations in the Applications Information section).

Short-Circuit Protection

When the regulator output is shorted to ground, the frequency of the oscillator is reduced to about 210kHz, one seventh the nominal frequency. This frequency foldback ensures that the inductor current has more time to decay, thereby preventing runaway. The oscillator's frequency will progressively increase to 1.5MHz when V_{FB} rises above 0V.

Burst Mode is a registered trademark of Linear Technology Corporation.

OPERATION

Battery Charger Power Source Selection

The LTC3550 can charge a battery from either the wall adapter input or the USB port input. The charger automatically senses the presence of voltage at each input. If both power sources are present, the charger defaults to the wall adapter source provided sufficient power is present at the DCIN input. "Sufficient power" is defined as:

- Supply voltage is greater than the UVLO threshold.
- Supply voltage is greater than the battery voltage by 50mV (180mV rising, 50mV falling).

Table 1 describes the behavior of the $\overline{PWR}$ status output.

Table 1. Power Source Selection

	V_{USBIN} > 3.95V and V_{USBIN} > BAT + 50mV	V_{USBIN} < 3.95V or V_{USBIN} < BAT + 50mV
V_{DCIN} > 4.15V and V_{DCIN} > BAT + 50mV	Charger Powered from Wall Adapter Source; USBIN Current < 25µA $\overline{PWR}$: LOW	Charger Powered from Wall Adapter Source $\overline{PWR}$: LOW
V_{DCIN} < 4.15V or V_{DCIN} < BAT + 50mV	Charger Powered from USB Source; $\overline{PWR}$: LOW	No Charging $\overline{PWR}$: Hi-Z

Status Indicators

The charge status output ($\overline{CHRG}$) has two states: pull-down and high impedance. The pull-down state indicates that the LTC3550 is in a charge cycle. Once the charge cycle has terminated or the LTC3550 is disabled, the pin state becomes high impedance. The pull-down state is strong enough to drive an LED and is capable of sinking up to 10mA.

The power supply status output ($\overline{PWR}$) has two states: pull-down and high impedance. The pull-down state indicates that power is present at either DCIN or USBIN. If no power is applied at either pin, the $\overline{PWR}$ pin is high impedance, indicating that the LTC3550 lacks sufficient power to charge the battery. The pull-down state is strong enough to drive an LED and is capable of sinking up to 10mA.

Low-Battery Charge Conditioning (Trickle Charge)

This feature ensures that deeply discharged batteries are gradually charged before applying full charge current . If the BAT pin voltage is below 2.9V, the LTC3550 supplies 1/10th of the full charge current to the battery until the BAT pin rises above 2.9V. For example, if the charger is programmed to charge at 800mA from the wall adapter input and 500mA from the USB input, the charge current during trickle charge mode would be 80mA and 50mA, respectively.

Thermal Limiting

An internal thermal feedback loop reduces the programmed charge current if the die temperature attempts to rise above a preset value of approximately 105°C. This feature protects the LTC3550 from excessive temperature and allows the user to push the limits of the power handling capability of a given circuit board without risk of damaging the device. The charge current can be set according to typical (not worst-case) ambient temperature with the assurance that the charger will automatically reduce the current in worst case conditions. DFN package power considerations are discussed further in the Applications Information section.

Charge Current Soft-Start and Soft-Stop

The battery charger includes a soft-start circuit to minimize the inrush current at the start of a charge cycle. When a charge cycle is initiated, the charge current ramps from zero to full-scale current over a period of 250µs. Likewise, internal circuitry ramps the charge current from full-scale to zero in approximately 30µs when the charger shuts down or self terminates. This minimizes the transient current load on the power supply during start-up and shutdown.

APPLICATIONS INFORMATION

Figure 2 shows the basic LTC3550 application circuit. External component selection is driven by the charging requirements and the buck regulator load requirements.

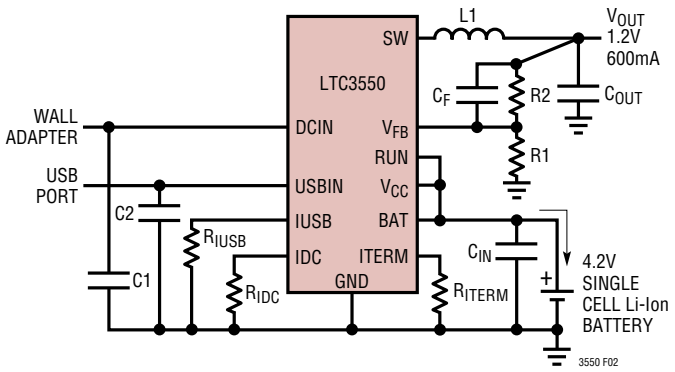


Figure 2. LTC3550 Basic Circuit

Programming and Monitoring Charge Current

The charge current delivered to the battery from the wall adapter supply is programmed using a single resistor from the IDC pin to ground.

$$R_{IDC} = \frac{1000V}{I_{CHRG(DC)}},\ I_{CHRG(DC)} = \frac{1000V}{R_{IDC}}$$

Similarly, the charge current from the USB supply is programmed using a single resistor from the IUSB pin to ground. Setting HPWR pin to its high state will select 100% of the programmed charge current, while setting HPWR to its low state will select 20% of the programmed charge current.

$$R_{IUSB} = \frac{1000V}{I_{CHRG(USB)}}\ (HPWR = HIGH)$$

$$I_{CHRG(USB)} = \frac{1000V}{R_{IUSB}}\ (HPWR = HIGH)$$

$$I_{CHRG(USB)} = \frac{200V}{R_{IUSB}}\ (HPWR = LOW)$$

Charge current out of the BAT pin can be determined at any time by monitoring the IDC or IUSB pin voltage and using the following equations:

$$I_{BAT} = \frac{V_{IDC}}{R_{IDC}} \bullet 1000,\ (charging\ from\ wall\ adapter)$$

$$I_{BAT} = \frac{V_{IUSB}}{R_{IUSB}} \bullet 1000,\ (charging\ from\ USB\ supply,\ HPWR = HIGH)$$

$$I_{BAT} = \frac{V_{IUSB}}{R_{IUSB}} \bullet 200,\ (charging\ from\ USB\ supply,\ HPWR = LOW)$$

Programming Charge Termination

The charge cycle terminates when the charge current falls below the programmed termination threshold during constant-voltage mode. This threshold is set by connecting an external resistor, R_{ITERM}, from the ITERM pin to ground. The charge termination current threshold ($I_{TERMINATE}$) is set by the following equation:

$$R_{ITERM} = \frac{100V}{I_{TERMINATE}},\ I_{TERMINATE} = \frac{100V}{R_{ITERM}}$$

The termination condition is detected by using an internal filtered comparator to monitor the ITERM pin. When the ITERM pin voltage drops below 100mV* for longer than $t_{TERMINATE}$ (typically 1.5ms), charging is terminated. The charge current is latched off and the LTC3550 enters standby mode.

When charging, transient loads on the BAT pin can cause the ITERM pin to fall below 100mV for short periods of time before the DC charge current has dropped below the programmed termination current. The 1.5ms filter time ($t_{TERMINATE}$) on the termination comparator ensures that transient loads of this nature do not result in premature charge cycle termination. Once the average charge current drops below the programmed termination threshold, the LTC3550 terminates the charge cycle and stops providing any current out of the BAT pin. In this state, any load on the BAT pin must be supplied by the battery.

*Any external sources that hold the ITERM pin above 100mV will prevent the LTC3550 from terminating a charged cycle.

APPLICATIONS INFORMATION

Buck Regulator Inductor Selection

For most applications, the value of the inductor will fall in the range of 1µH to 4.7µH. Its value is chosen based on the desired inductor ripple current. Large value inductors lower ripple current and small value inductors result in higher ripple currents. Higher V_{CC} or V_{OUT} also increases the ripple current as shown in Equation 1. A reasonable starting point for setting ripple current is ΔI_L = 240mA (40% of 600mA).

$$\Delta I_L = \frac{V_{OUT}}{f_0 \bullet L} \bullet \left(1 - \frac{V_{OUT}}{V_{CC}}\right) \quad (1)$$

The DC current rating of the inductor should be at least equal to the maximum load current plus half the ripple current to prevent core saturation. Thus, a 720mA rated inductor should be enough for most applications (600mA + 120mA). For best efficiency, choose a low DC-resistance inductor.

The inductor value also has an effect on Burst Mode operation. The transition to low current operation begins when the inductor current peaks fall to approximately 200mA. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to increase.

Inductor Core Selection

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs size requirements and any radiated field/EMI requirements than on what the LTC3550 requires to operate. Table 2 shows some typical surface mount inductors that work well in LTC3550 applications.

Table 2. Representative Surface Mount Inductors

PART NUMBER	VALUE (µH)	DCR (Ω MAX)	MAX DC CURRENT (A)	SIZE W × L × H (mm)
Sumida CDRH3D16	1.5 2.2 3.3 4.7	0.043 0.075 0.110 0.162	1.55 1.20 1.10 0.90	3.8 × 3.8 × 1.8
Sumida CMD4D06	2.2 3.3 4.7	0.116 0.174 0.216	0.950 0.770 0.750	3.5 × 4.3 × 0.8
Panasonic ELT5KT	3.3 4.7	0.17 0.20	1.00 0.95	4.5 × 5.4 × 1.2
Murata LQH32CN	1.0 2.2 4.7	0.060 0.097 0.150	1.00 0.79 0.65	2.5 × 3.2 × 2.0

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle V_{OUT}/V_{CC}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ required } I_{RMS} \cong I_{OMAX} \frac{\sqrt{V_{OUT}\left(V_{CC} - V_{OUT}\right)}}{V_{CC}} \quad (2)$$

This formula has a maximum at $V_{CC} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that the capacitor manufacturer's ripple current ratings are often based on 2000 hours of life. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Always consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the required effective series resistance (ESR).

Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. The output ripple ΔV_{OUT} is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left(ESR + \frac{1}{8fC_{OUT}}\right) \quad (3)$$

APPLICATIONS INFORMATION

where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. For a fixed output voltage, the output ripple voltage is highest at maximum input voltage since ΔI_L increases with input voltage.

Aluminum electrolytic and solid tantalum capacitors are both available in surface mount configurations. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum. These are specially constructed and tested for low ESR so they give the lowest ESR for a given volume. Other capacitor types include Sanyo POSCAP, Kemet T510 and T495 series, and Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.

Using Ceramic Input and Output Capacitors

Higher capacitance values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. Because the LTC3550's control loop does not depend on the output capacitor's ESR for stable operation, ceramic capacitors can be used **freely** to achieve very low output ripple and small circuit size.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Output Voltage Programming

The output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} = 0.6V\left(1+\frac{R2}{R1}\right) \quad (4)$$

The external resistive divider is connected to the output, allowing remote voltage sensing as shown in Figure 3.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Efficiency can be expressed as:

Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

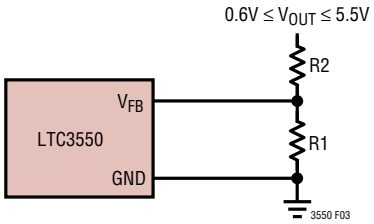


Figure 3. Setting the LTC3550 Output Voltage

Although all dissipative elements in the circuit produce losses, two main sources usually account for most of the losses in LTC3550 circuits: V_{CC} quiescent current and I^2R losses. The V_{CC} quiescent current loss dominates the efficiency loss at very low load currents whereas the I^2R loss dominates the efficiency loss at medium to high load currents. In a typical efficiency plot, the efficiency curve at very low load currents can be misleading since the actual power lost is of no consequence as illustrated in Figure 4.

1. The V_{CC} quiescent current is due to two components: the DC bias current as given in the Electrical Characteristics and the internal main switch and synchronous

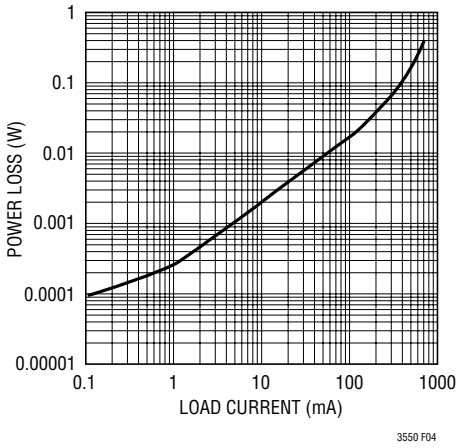


Figure 4. Power Lost vs Load Current

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switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each time the gate is switched from high to low to high again, a packet of charge, dQ, moves from V_{CC} to ground. The resulting dQ/dt is the current out of V_{CC} that is typically larger than the DC bias current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$ where Q_T and Q_B are the gate charges of the internal top and bottom switches. Both the DC bias and gate charge losses are proportional to V_{CC} and thus their effects will be more pronounced at higher supply voltages.

2. I^2R losses are calculated from the resistances of the internal switches, R_{SW}, and external inductor R_L. In continuous mode, the average output current flowing through inductor L is "chopped" between the main switch and the synchronous switch. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)TOP})(DC) + (R_{DS(ON)BOT})(1 - DC)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses, simply add R_{SW} to R_L and multiply the result by the square of the average output current. Other losses including C_{IN} and C_{OUT} ESR dissipative losses and inductor core losses generally account for less than 2% total additional loss.

Thermal Considerations

The battery charger's thermal regulation feature and the buck regulator's high efficiency make it unlikely that enough power will be dissipated to exceed the LTC3550 maximum junction temperature. Nevertheless, it is a good idea to do some thermal analysis for worst-case conditions. The junction temperature, T_J, is given by: $T_J = T_A + T_{RISE}$ where T_A is the ambient temperature. The temperature rise is given by:

$$T_{RISE} = P_D \bullet \theta_{JA}$$

where P_D is the power dissipated and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature.

In most applications the buck regulator does not dissipate much heat due to its high efficiency. The majority of the LTC3550 power dissipation occurs when charging a battery. Fortunately, the LTC3550 automatically reduces the charge current during high power conditions using a patented thermal regulation circuit. Thus, there is no need to design for worst-case power dissipation scenarios because the LTC3550 ensures that the battery charger power dissipation never raises the junction temperature above a preset value of 105°C. In the unlikely case that the junction temperature is forced above 105°C (due to abnormally high ambient temperatures or excessive buck regulator power dissipation), the battery charge current will be reduced to zero and thus dissipate no heat. As an added measure of protection, even if the junction temperature reaches approximately 150°C, the buck regulator's power switches will be turned off and the SW node will become high impedance.

The conditions that cause the LTC3550 to reduce charge current through thermal feedback can be approximated by considering the power dissipated in the IC. The approximate ambient temperature at which the thermal feedback begins to protect the IC is:

$$T_A = 105°C - T_{RISE}$$

$$T_A = 105°C - (P_D \bullet \theta_{JA})$$

$$T_A = 105°C - (P_{D(CHARGER)} + P_{D(BUCK)}) \bullet \theta_{JA} \quad (5)$$

Most of the charger's power dissipation is generated from the internal charger MOSFET. Thus, the power dissipation is calculated to be:

$$P_{D(CHARGER)} = (V_{IN} - V_{BAT}) \bullet I_{BAT} \quad (6)$$

V_{IN} is the charger supply voltage (either DCIN or USBIN), V_{BAT} is the battery voltage and I_{BAT} is the charge current.

Example: An LTC3550 operating from a 5V wall adapter (on the DCIN input) is programmed to supply 650mA full-scale current to a discharged Li-Ion battery with a voltage of 3V.

The charger power dissipation is calculated to be:

$$P_{D(CHARGER)} = (5V - 3V) \bullet 650mA = 1.3W$$

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For simplicity, assume the buck regulator is disabled and dissipates no power ($P_{D(BUCK)} = 0$). For a properly soldered DHC16 package, the thermal resistance (θ_{JA}) is 40°C/W. Thus, the ambient temperature at which the LTC3550 charger will begin to reduce the charge current is:

$T_A = 105°C – (1.3W • 40°C/W)$

$T_A = 105°C – 52°C$

$T_A = 53°C$

The LTC3550 can be used above 53°C ambient, but the charge current will be reduced from 650mA. Assuming no power dissipation from the buck converter, the approximate current at a given ambient temperature can be approximated by:

$$I_{BAT} = \frac{105°C - T_A}{(V_{IN} - V_{BAT}) \bullet \theta_{JA}} \quad (7)$$

Using the previous example with an ambient temperature of 60°C, the charge current will be reduced to approximately:

$$I_{BAT} = \frac{105°C - 60°C}{(5V - 3V) \bullet 40°C/W} = \frac{45°C}{80°C/A}$$

$I_{BAT} = 563mA$

Because the regulator typically dissipates significantly less power than the charger (even in worst-case situations), the calculations here should work well as an approximation. However, the user may wish to repeat the previous analysis to take the buck regulator's power dissipation into account. Equation (7) can be modified to take into account the temperature rise due to the buck regulator:

$$I_{BAT} = \frac{105°C - T_A - (P_{D(BUCK)} \bullet \theta_{JA})}{(V_{IN} - V_{BAT}) \bullet \theta_{JA}} \quad (8)$$

For optimum performance, it is critical that the exposed metal pad on the backside of the LTC3550 package is properly soldered to the PC board ground. When correctly soldered to a 2500mm^2 double sided 1oz copper board, the LTC3550 has a thermal resistance of approximately 40°C/W. Failure to make thermal contact between the exposed pad on the backside of the package and the copper board will result in thermal resistances far greater than 40°C/W. As an example, a correctly soldered LTC3550 can deliver over 800mA to a battery from a 5V supply at room temperature. Without a good backside thermal connection, this number would drop to much less than 500mA.

Battery Charger Stability Considerations

The constant-voltage mode feedback loop is stable without any compensation provided a battery is connected to the charger output. When the charger is in constant-current mode, the charge current program pin (IDC or IUSB) is in the feedback loop, not the battery. The constant-current mode stability is affected by the impedance at the charge current program pin. With no additional capacitance on this pin, the charger is stable with program resistor values as high as 20k (I_{CHG} = 50mA); however, additional capacitance on these nodes reduces the maximum allowed program resistor value.

Checking Regulator Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to (ΔI_{LOAD} • ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, which generates a feedback error signal. The regulator loop then acts to return V_{OUT} to its steady state value. During this recovery time V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem. For a detailed explanation of switching control loop theory, see Application Note 76.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the load switch resistance is low and it is driven quickly. The only solution is to limit the rise time of the switch drive so that the load rise time is limited to approximately (25 • C_{LOAD}). Thus, a 10µF capacitor charging to 3.3V would require a 250µs rise time, limiting the charging current to about 130mA.

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Protecting the USB Pin and Wall Adapter Input from Overvoltage Transients

Caution must be exercised when using ceramic capacitors to bypass the USBIN pin or the wall adapter inputs. High voltage transients can be generated when the USB or wall adapter is hot-plugged. When power is supplied via the USB bus or wall adapter, the cable inductance along with the self resonant and high Q characteristics of ceramic capacitors can cause substantial ringing which could exceed the maximum voltage ratings and damage the LTC3550. Refer to Linear Technology Application Note 88, entitled "Ceramic Input Capacitors Can Cause Overvoltage Transients" for a detailed discussion of this problem. The long cable lengths of most wall adapters and USB cables makes them especially susceptible to this problem. To bypass the USB and the wall adapter inputs, add a 1Ω resistor in series with a ceramic capacitor to lower the effective Q of the network and greatly reduce the ringing. A tantalum, OS-CON, or electrolytic capacitor can be used in place of the ceramic and resistor, as their higher ESR reduces the Q, thus reducing the voltage ringing.

The oscilloscope photograph in Figure 5 shows how serious the overvoltage transient can be for the USB and wall adapter inputs. For both traces, a 5V supply is hot-plugged using a three foot long cable. For the top trace, only a 4.7µF ceramic X5R capacitor (without the recommended 1Ω series resistor) is used to locally bypass the input. This trace shows excessive ringing when the 5V cable is inserted, with the overvoltage spike reaching 10V. For the bottom trace, a 1Ω resistor is added in series with the 4.7µF ceramic capacitor to locally bypass the 5V input. This trace shows the clean response resulting from the addition of the 1Ω resistor.

Even with the additional 1Ω resistor, bad design techniques and poor board layout can often make the overvoltage problem even worse. System designers often add extra inductance in series with input lines in an attempt to minimize the noise fed back to those inputs by the application. In reality, adding these extra inductances only makes the overvoltage transients worse. Since cable inductance is one of the fundamental causes of the excessive ringing, adding a series ferrite bead or inductor increases the effective cable inductance, making the problem even worse. For this reason, **do not** add additional inductance (ferrite beads or inductors) in series with the USB or wall adapter inputs. For the most robust solution, 6V transorbs or zener diodes may also be added to further protect the USB and wall adapter inputs. Two possible protection devices are the SM2T from STMicroelectronics and the EDZ series devices from ROHM.

Always use an oscilloscope to check the voltage waveforms at the USBIN and DCIN pins during USB and wall adapter hot-plug events to ensure that overvoltage transients have been adequately removed.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3550. These items are also illustrated graphically in Figures 6 and 7. Check the following in your layout:

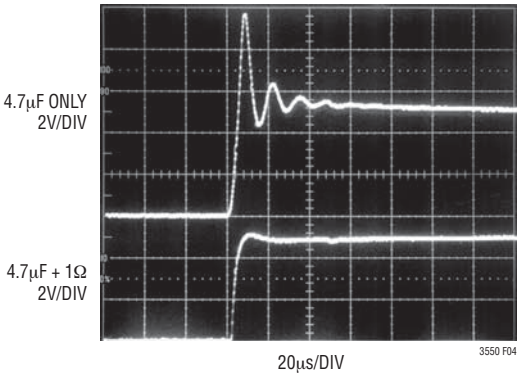

Figure 5. Waveforms Resulting from Hot-Plugging a 5V Input Supply When Using Ceramic Bypass Capacitors

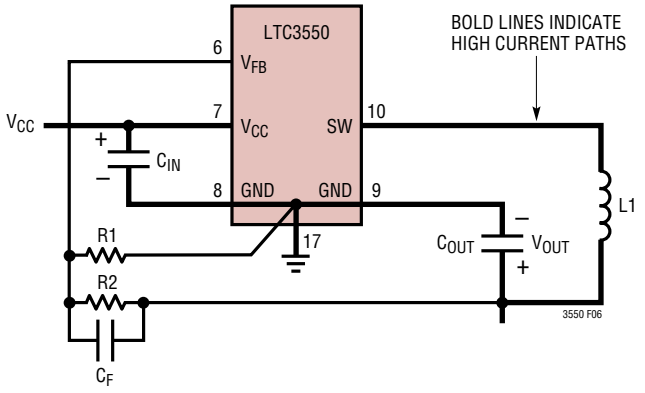

Figure 6. DC-DC Converter Layout Diagram

APPLICATIONS INFORMATION

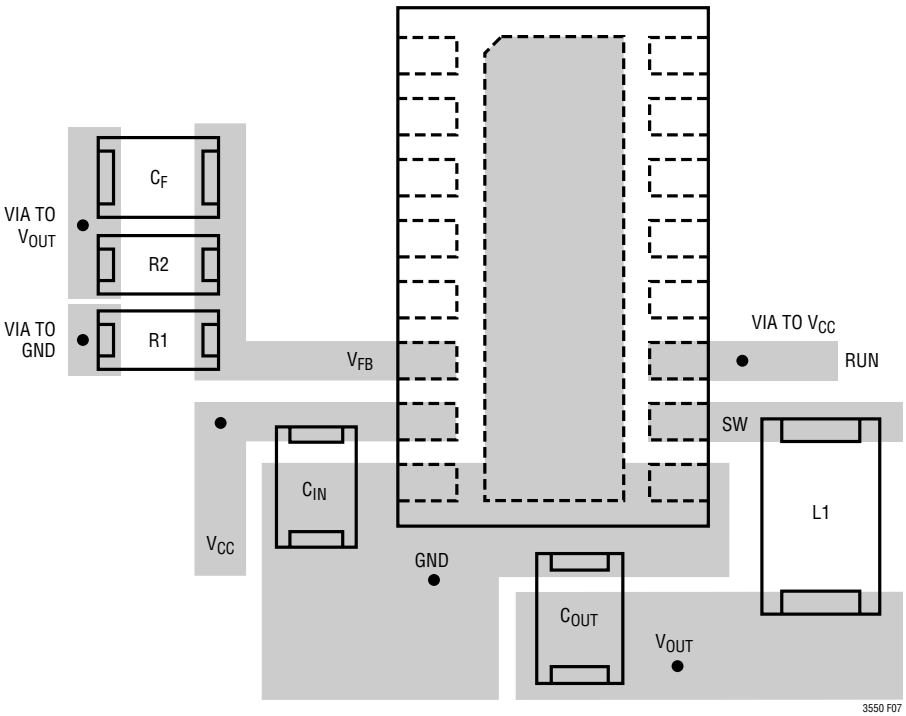

Figure 7. DC-DC Converter Suggested Layout

1. The power traces, consisting of the GND trace, the SW trace and the V_{CC} trace should be kept short, direct and wide.
2. Does the V_{FB} pin connect directly to the feedback resistors? The resistive divider R1/R2 must be connected between the (+) plate of C_{OUT} and ground.
3. Does the (+) plate of C_{IN} connect to V_{CC} as closely as possible? This capacitor provides the AC current to the internal power MOSFETs.
4. Keep the switching node, SW, away from the sensitive V_{FB} node.
5. Keep the (–) plates of C_{IN} and C_{OUT} as close as possible.
6. Solder the exposed pad on the backside of the package to PC board ground for optimum thermal performance. The thermal resistance of the package can be further enhanced by increasing the area of the copper used for PC board ground.

Design Example

As a design example, assume the LTC3550 is used in a single lithium-ion battery-powered cellular phone application. The battery is charged by either plugging a wall adapter cable into the phone or putting the phone in a USB cradle. The optimum charge current for this particular lithium-ion battery is determined to be 800mA. The buck regulator output voltage needs to be 1.8V.

Starting with the charger, choosing R_{IDC} to be 1.24k programs the charger for 806mA. Choosing R_{IUSB} to be 2.1k programs the charger for 475mA when charging from the USB cradle, ensuring that the charger never exceeds the 500mA maximum current supplied by the USB port. A good rule of thumb for $I_{TERMINATE}$ is one-tenth the full charge current, so R_{ITERM} is picked to be 1.24k ($I_{TERMINATE}$ = 80mA).

Moving on to the step-down converter, V_{CC} will be powered from the battery which can range from a maximum of 4.2V down to about 2.7V. The load current requirement

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is a maximum of 600mA but most of the time it will be in standby mode, requiring only 2mA. Efficiency at both low and high load currents is important. With this information we can calculate L using Equation (1),

$$\Delta I_L = \frac{V_{OUT}}{f_O \bullet L} \bullet \left(1 - \frac{V_{OUT}}{V_{CC}}\right)$$

Substituting V_{OUT} = 1.8V, V_{CC} = 4.2V, ΔI_L = 240mA and f_O = 1.5MHz in Equation (3) gives:

$$L = \frac{1.8V}{1.5MHz \bullet (240mA)} \bullet \left(1 - \frac{1.8V}{4.2V}\right) = 2.86\mu H$$

A 2.2µH inductor works well for this application. For best efficiency choose a 720mA or greater inductor with less than 0.2Ω series resistance. C_{IN} will require an RMS current rating of at least 0.3A = $I_{LOAD(MAX)}/2$ at temperature and C_{OUT} will require an ESR of less than 0.25Ω. In most cases, a ceramic capacitor will satisfy this requirement.

For the feedback resistors, choose R1 = 301k. R2 can then be calculated from equation (4) to be:

$$R2 = R1\left(\frac{V_{OUT}}{0.6} - 1\right) = 604k$$

Figure 8 shows the complete circuit along with its efficiency curve.

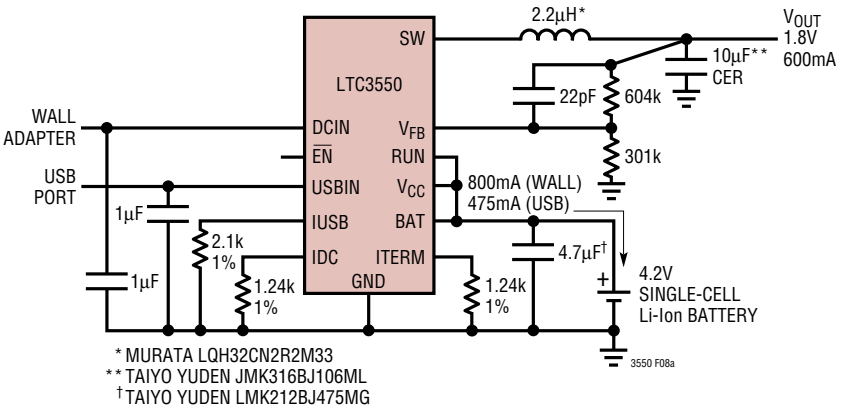


Figure 8a. Design Example Circuit

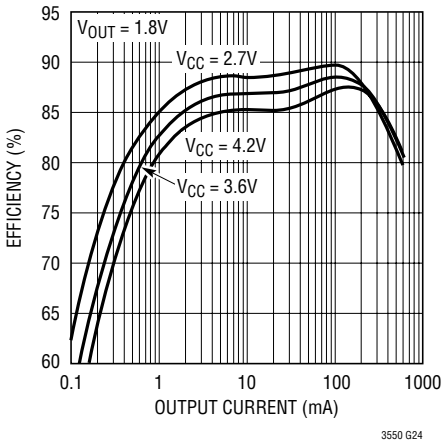
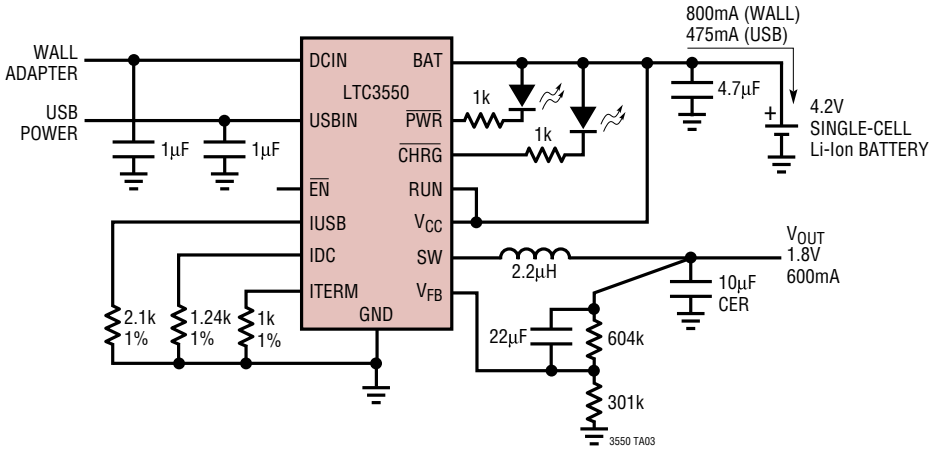


Figure 8b. Buck Regulator Efficiency vs Output Current

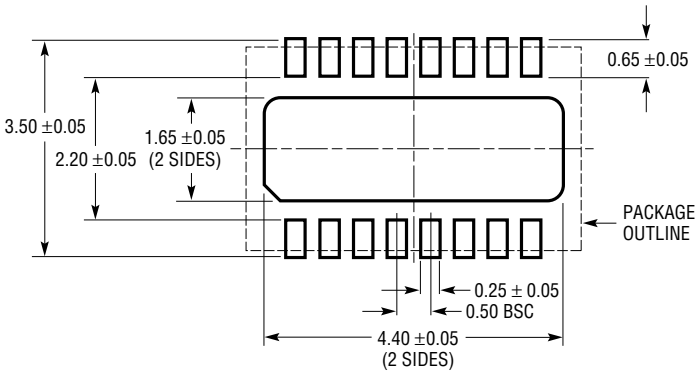
TYPICAL APPLICATIONS

Full Featured Dual Input Charger Plus Step-Down Converter

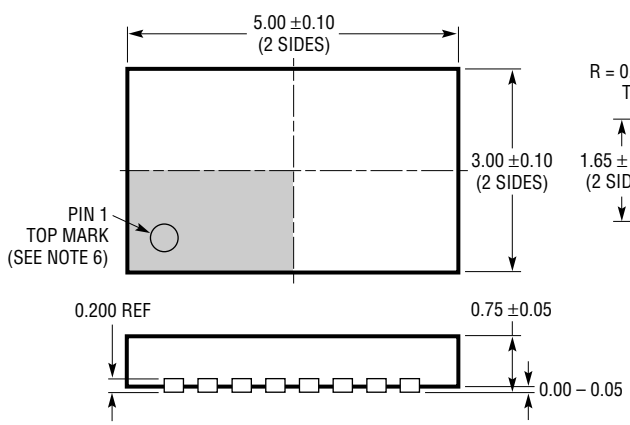


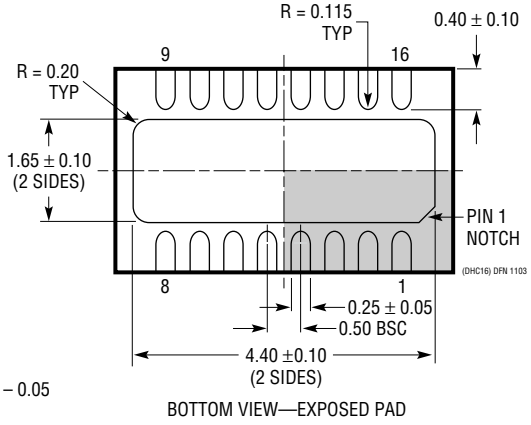
PACKAGE DESCRIPTION

DHC Package
16-Lead Plastic DFN (5mm × 3mm)
(Reference LTC DWG # 05-08-1706)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS





BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WJED-1) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE