High Power PD With Synchronous No-Opto Flyback Controller

FEATURES

- **Robust 35W PD Front End**
- **IEEE 802.3af Compliant**
- **Rugged 750mA Power MOSFET With Precision Dual Level Current Limit**
- **High Performance Synchronous Flyback Controller**
- **IEEE Isolation Obtained Without an Opto-Isolator**
- **Adjustable Frequency from 50kHz to 250kHz**
- **Tight Multi-Output Regulation With Load Compensation**
- Onboard 25k Signature Resistor
- Programmable Classification Current to 75mA
- Complete Thermal and Over-Current Protection
- Available in Compact 32-Pin 7mm × 4mm DFN Package

APPLICATIONS

- VoIP Phones With Advanced Display Options
- Dual-Radio Wireless Access Points
- PTZ Security Cameras
- RFID Readers
- Industrial Controls
- Magnetic Card Readers
- High Power PoE Systems

DESCRIPTION

The LTC®4268-1 is an integrated Powered Device (PD) controller and switching regulator intended for IEEE 802.3af and high power PoE applications up to 35W. By including a precision dual current limit, the LTC4268-1 keeps inrush below IEEE 802.3af current limit levels to ensure interoperability success while enabling high power applications with a 750mA operational current limit.

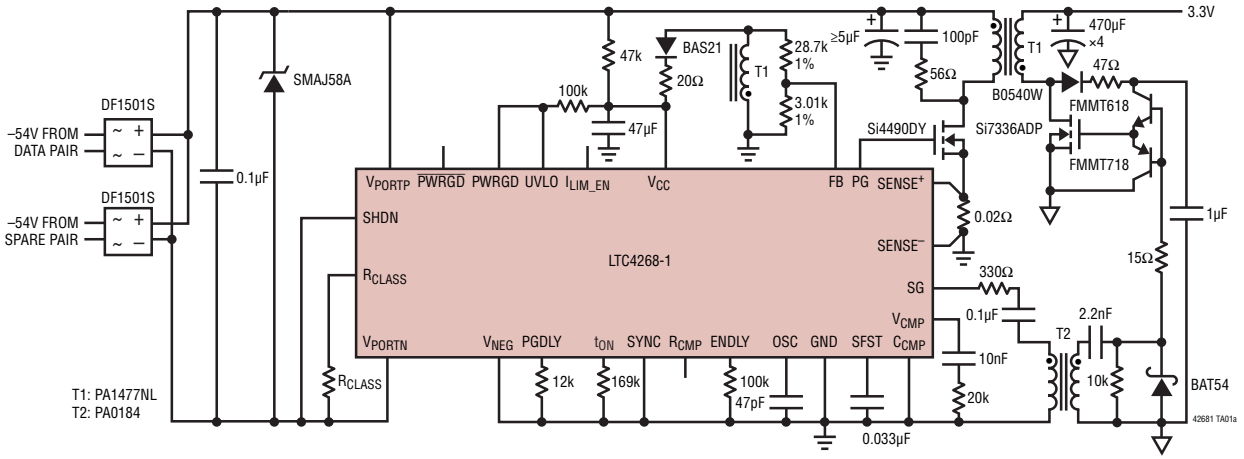
The LTC4268-1 synchronous, current-mode, flyback controller generates multiple supply rails in a single conversion providing for the highest system efficiency while maintaining tight regulation across all outputs. The LTC4268-1 includes Linear Technology's patented No-Opto feedback topology to provide full IEEE 802.3af isolation without the need of opto-isolator circuitry.

The oversized power path and high performance flyback controller of the LTC4268-1 combine to make the ultimate solution for power hungry PoE applications such as WAPs, PTZ security cameras, RFID readers and ultra-efficient 802.3af applications running near the 12.95W limit.

The LTC4268-1 is available in a space saving 32-pin DFN package.

TYPICAL APPLICATION

35W High Efficiency PD Solution

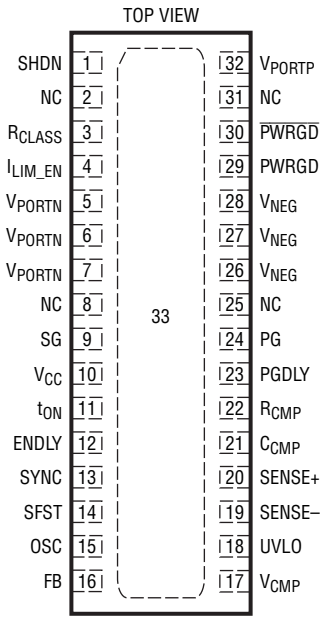


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

V_{PORTN} Voltage ..... 0.3V to –90V
V_{NEG} Voltage ..... V_{PORTN} + 90V to V_{PORTN} –0.3V
V_{CC} to GND Voltage (Note 3)
  Low Impedance Source ..... –0.3V to 18V
  Current Fed ..... 30mA into V_{CC}
R_{CLASS}, I_{LIM_EN} Voltage .. V_{PORTN} + 7V to V_{PORTN} – 0.3V
SHDN Voltage ..... V_{PORTN} + 90V to V_{PORTN} – 0.3V
PWRGD Voltage (Note 3)
  Low Impedance Source .... V_{NEG} + 11V to V_{NEG} – 0.3V
  Current Fed 5mA
$\overline{PWRGD}$ Voltage ..... V_{PORTN} + 80V to V_{PORTN} – 0.3V
$\overline{PWRGD}$ Current 10mA
R_{CLASS} Current 100mA
$SENSE^-$, $SENSE^+$ Voltage ..... –0.5V to +0.5V
UVLO, SYNC Voltage ..... –0.3V to V_{CC}
FB Current ..... ±2mA
V_{CMP} Current ..... ±1mA
Operating Ambient Temperature Range (Notes 4, 5)
  LTC4268-1C ..... 0°C to 70°C
  LTC4268-1I ..... –40°C to 85°C
Junction Temperature (Note 5) ..... 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DKD32 PACKAGE
32-LEAD (7mm × 4mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 49°C/W, θ_{JC} = 4.7°C/W
EXPOSED PAD (PIN 33) MUST BE SOLDERED TO
HEAT SINKING PLANE THAT IS ELECTRICALLY CONNECTED TO GND

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4268CDKD-1#PBF	LTC4268CDKD-1#TRPBF	42681	32-Lead (7mm × 4mm) Plastic DFN	0°C to 70°C
LTC4268IDKD-1#PBF	LTC4268IDKD-1#TRPBF	42681	32-Lead (7mm × 4mm) Plastic DFN	–40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC4268CDKD-1	LTC4268CDKD-1#TR	42681	32-Lead (7mm × 4mm) Plastic DFN	0°C to 70°C
LTC4268IDKD-1	LTC4268IDKD-1#TR	42681	32-Lead (7mm × 4mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 14V, SG open, V_{CMP} = 1.5V, V_{SENSE} = 0V, R_{CMP} = 1k, R_{tON} = 90k, R_{PGDLY} = 27.4k, R_{ENDLY} = 90k, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{PORT}	Supply Voltage	Voltage With Respect to V_{PORTP} Pin (Notes 6, 7, 8, 9, 10)					
	IEEE 802.3af System		●			–57	V
	Signature Range		●	–1.5		–10.1	V
	Classification Range		●	–12.5		–21	V
	UVLO Turn-On Voltage		●	–37.7	–38.9	–40.2	V
	UVLO Turn-Off Voltage		●	–29.8	–30.6	–31.5	V
V_{TURNON}	V_{CC} Turn-On Voltage	Voltage With Respect to GND	●	14	15.3	16.6	V
$V_{TURNOFF}$	V_{CC} Turn-Off Voltage	Voltage With Respect to GND	●	8	9.7	11	V
V_{HYST}	V_{CC} Hysteresis	$V_{TURNON} – V_{TURNOFF}$	●	4	5.6	7.2	V
V_{CLAMP}	V_{CC} Shunt Regulator Voltage	I_{VCC} = 15mA, V_{UVLO} = 0V, Voltage With Respect to GND	●	19.5	20.2		V
I_{VCC}	V_{CC} Supply Current	V_{CMP} = Open (Note 11)	●	4	6.4	10	mA
I_{VCC_START}	V_{CC} Start-Up Current	V_{CC} = 10V	●		180	400	µA
V_{FB}	Feedback Regulation Voltage		●	1.22	1.237	1.251	V
I_{FB_BIAS}	Feedback Pin Input Bias Current	R_{CMP} Open			200		nA
g_m	Feedback Amplifier Transconductance		●	700	1000	1400	A/V
I_{FB}	Feedback Amplifier Source or Sink Current		●	25	55	90	µA
$V_{FBCLAMP}$	Feedback Amplifier Clamp Voltage	V_{FB} = 0.9V V_{FB} = 1.4V			2.56 0.84		V V
$\%V_{REF}$	Reference Voltage Line Regulation	12V ≤ V_{CC} ≤ 18V	●		0.005	0.02	%/V
A_V	Feedback Amplifier Voltage Gain	V_{CMP} = 1.2V to 1.7V			1500		V/V
I_{SFST}	Soft-Start Charging Current	V_{SFST} = 1.5V		16	20	25	µA
I_{SFST}	Soft-Start Discharge Current	V_{SFST} = 1.5V, V_{UVLO} = 0V		0.8	1.3		mA
V_{CMP_THLD}	Control Pin Threshold (VCMP)	Duty Cycle = Min			1		V
V_{PG_HIGH}, V_{SG_HIGH}	PG, SG, Output High Level		●	6.6	7.4	8	V
V_{PG_LOW}, V_{SG_LOW}	PG, SG, Output Low Level		●		0.01	0.05	V
V_{PG_SHDN}, V_{SG_SHDN}	PG, SG, Output Shutdown Strength	V_{UVLO} = 0V; I_{PG}, I_{SG} = 20mA	●		1.4	2.3	V
t_{PG_RISE}, t_{SG_RISE}	PG, SG Rise Time	C_{PG}, C_{SG} = 1nF			15		ns
t_{PG_FALL}, t_{SG_FALL}	PG, SG Fall Time	C_{PG}, C_{SG} = 1nF			15		ns
V_{SENSE_LIM}	Switch Current Threshold at Maximum V_{CMP}	Measured at V_{SENSE+}	●	88	100	110	mV
$\Delta V_{SENSE}/\Delta V_{CMP}$	Sense Threshold vs V_{CMP}				0.07		V/V
V_{SENSE_OC}	Sense Pin Overcurrent Fault Voltage	V_{SENSE+}, V_{SFST} < 1V	●		205	230	mV
V_{IH_SHDN}	Shutdown High Level Input Voltage	With Respect to V_{PORTN} High Level = Shutdown (Note 12)	●	3		57	V
V_{IL_SHDN}	Shutdown Low Level Input Voltage	With Respect to V_{PORTN}	●			0.45	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 14V, SG open, V_{CMP} = 1.5V, V_{SENSE} = 0V, R_{CMP} = 1k, R_{tON} = 90k, R_{PGDLY} = 27.4k, R_{ENDLY} = 90k, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
R_{INPUT_SHDN}	Shutdown Input Resistance	With Respect to V_{PORTN}	●	100			kΩ
V_{IH_ILIM}	I_{LIM_EN} High Level Input Voltage	With Respect to V_{PORTN} (Note 13) High Level Enables Current Limit	●	4			V
V_{IL_ILIM}	I_{LIM_EN} Low Level Input Voltage	With Respect to V_{PORTN} (Note 13)	●			1	V
I_{VPORTN}	V_{PORTN} Supply Current	V_{PORTN} = –54V	●			3	mA
I_{IN_CLASS}	IC Supply Current During Classification	V_{PORTN} = –17.5V, V_{NEG} Tied to V_{PORTP} (Note 14)	●	0.55	0.62	0.70	mA
ΔI_{CLASS}	Current Accuracy During Classification	10mA < I_{CLASS} < 75mA –12.5V ≤ V_{PORTN} ≤ –21V (Notes 15, 16)	●			±3.5	%
$R_{SIGNATURE}$	Signature Resistance	–1.5V ≤ V_{PORTN} ≤ –10.1V, SHDN Tied to V_{PORTN}, IEEE 802.3af Two-Point Measurement (Notes 8, 9)	●	23.25		26	kΩ
$R_{INVALID}$	Invalid Signature Resistance	–1.5V ≤ V_{PORTN} ≤ –10.1V, SHDN Tied to V_{PORTP}, IEEE 802.3af Two-Point Measurement (Notes 8, 9)			10	11.8	kΩ
$V_{\overline{PWRGD}\_OUT}$	Active Low Power Good Output Voltage	I = 1mA, V_{PORTN} = –54V, $\overline{PWRGD}$ Referenced to V_{PORTN}	●			0.5	V
$I_{\overline{PWRGD}\_LEAK}$	Active Low Power Good Output Leakage	V_{PORT} = 0V, $V_{\overline{PWRGD}}$ = 57V	●			1	µA
V_{PWRGD_OUT}	Active High Power Good Output Voltage	I = 0.5mA, V_{PORTN} = –52V, V_{NEG} = –4V PWRGD Referenced to V_{NEG} (Note 17)	●			0.35	V
V_{PWRGD_VCLAMP}	Active High Power Good Voltage Limiting Clamp	I = 2mA, V_{NEG} = 0V, PWRGD Referenced to V_{NEG} (Note 3)	●	12	14	16.5	V
I_{PWRGD_LEAK}	Active High Power Good Output Leakage	V_{PWRGD} = 11V With Respect to V_{NEG}, V_{NEG} = V_{PORTN} = –54V	●			1	µA
R_{ON}	On-Resistance	I = 700mA, V_{PORTN} = –48V, Measured from V_{PORTN} to V_{NEG} (Note 16)	●		0.5	0.6 0.8	Ω Ω
I_{OUT_LEAK}	V_{OUT} Leakage	V_{PORTN} = –57V, V_{PORTP} = SHDN = V_{NEG} = 0V (Note 15)	●			1	µA
I_{LIM_HI}	Input Current Limit, High Level	V_{PORTN} = –54V, V_{NEG} = –53V I_{LIM_EN} Floating (Notes 18, 19)	●	700	750	800	mA
I_{LIM_LO}	Input Current Limit, Low Level	V_{PORTN} = –54V, V_{NEG} = –53V (Notes 18, 19)	●	250	300	350	mA
I_{LIM_DISA}	Safeguard Current Limit When I_{LIM} is Disabled	V_{PORTN} = –54V, V_{NEG} = –52.5V I_{LIM_EN} Tied to V_{PORTN} (Notes 18, 19, 20)		1.2	1.45	1.65	A
f_{OSC}	Oscillator Frequency	C_{OSC} = 100pF	●	84	100	110	kHz
C_{OSC}	Oscillator Capacitor Value	(Note 21)		33		200	pF
$t_{ON(MIN)}$	Minimum Switch on Time				200		ns
t_{ENDLY}	Flyback Enable Delay Time				265		ns
t_{PGDLY}	PG Turn-On Delay Time				200		ns
$DC_{ON(MAX)}$	Maximum Switch Duty Cycle		●	85	88		%
V_{SYNC}	SYNC Pin Threshold		●		1.53	2.1	V
R_{SYNC}	SYNC Pin Input Resistance				40		kΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 14V, SG open, V_{CMP} = 1.5V, V_{SENSE} = 0V, R_{CMP} = 1k, R_{tON} = 90k, R_{PGDLY} = 27.4k, R_{ENDLY} = 90k, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{LCOMP}	Feedback Pin Load Compensation Current	V_{RCMP} With V_{SENSE}^+ = 0V			20		µA
V_{LCOMP}	Load Comp to V_{SENSE} Offset Voltage	V_{SENSE+} = 20mV, V_{FB} = 1.23V			1		mV
V_{UVLO}	UVLO Pin Threshold		●	1.215	1.237	1.265	V
I_{UVLOL} I_{UVLOH}	UVLO Pin Bias Current	V_{UVLO} = 1.2V V_{UVLO} = 1.3V		–0.25 –4.50	0 –3.4	0.25 –2.5	µA µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltages are with respect to V_{PORTP} pin unless otherwise noted.

Note 3: Active High PWRGD internal clamp circuit self-regulates to 14V with respect to V_{NEG}. V_{CC} has internal 20V clamp with respect to GND.

Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 5: T_J is calculated from the ambient temperature T_A and power dissipation P_{DIS} according to the formula:

$$T_J = T_A + (P_{DIS} \bullet 49°C/W)$$

Note 6: The LTC4268-1 operates with a negative supply voltage in the range of –1.5V to –57V. To avoid confusion, voltages in this data sheet are referred to in terms of absolute magnitude. Terms such as "maximum negative voltage" refer to the largest negative voltage and a "rising negative voltage" refers to a voltage that is becoming more negative.

Note 7: In IEEE 802.3af systems, the maximum voltage at the PD jack is defined to be –57V.

Note 8: The LTC4268-1 is designed to work with two polarity protection diodes in series with the input. Parameter ranges specified in the Electrical Characteristics are with respect to LTC4268-1 pins and are designed to meet IEEE 802.3af specifications when the drop from the two diodes is included. See Applications Information.

Note 9: Signature resistance is measured via the two-point ΔV/ΔI method as defined by IEEE 802.3af. The LTC4268-1 signature resistance is offset from 25k to account for diode resistance. With two series diodes, the total PD resistance will be between 23.75k and 26.25k and meet IEEE 802.3af specifications. The minimum probe voltages measured at the LTC4268-1 pins are –1.5V and –2.5V. The maximum probe voltages are –9.1V and –10.1V.

Note 10: The LTC4268-1 includes hysteresis in the UVLO voltages to preclude any start-up oscillation. Per IEEE 802.3af requirements, the LTC4268-1 will power up from a voltage source with 20Ω series resistance on the first trial.

Note 11: Supply current does not include gate charge current to the MOSFETs. See Application Information.

Note 12: To disable the 25k signature, tie SHDN to V_{PORTP} (±0.1V) or hold SHDN high with respect to V_{IN}. See Applications Information.

Note13: I_{LIM_EN} pin is pulled high internally and for normal operation should be left floating. To disable current limit, tie I_{LIM_EN} to V_{IN}. See Applications Information.

Note 14: I_{IN_CLASS} does not include classification current programmed at Pin 3. Total supply current in classification mode will be I_{IN_CLASS} + I_{CLASS} (See Note 15).

Note 15: I_{CLASS} is the measured current flowing through R_{CLASS}. ΔI_{CLASS} accuracy is with respect to the ideal current defined as I_{CLASS} = 1.237/R_{CLASS}. $T_{CLASSRDY}$ is the time for I_{CLASS} to settle to within ±3.5% of ideal. The current accuracy specification does not include variations in R_{CLASS} resistance. The total classification current for a PD also includes the IC quiescent current (I_{IN_CLASS}). See Applications Information.

Note 16: This parameter is assured by design and wafer level testing.

Note 17: Active high power good is referenced to V_{NEG} and is valid for $V_{PORTP} - V_{NEG} \geq 4V$.

Note 18: The LTC4268-1 includes a dual current limit. At turn on, before C1 is charged, the LTC4268-1 current level is set to I_{LIMIT_LOW}. After C1 is charged and with I_{LIM_EN} floating, the LTC4268-1 switches to I_{LIMIT_HIGH}. With I_{LIM_EN} pin tied low, the LTC4268-1 switches to I_{LIMIT_DISA}. The LTC4268-1 stays in I_{LIMIT_HIGH} or I_{LIMIT_DISA} until the input voltage drops below the UVLO turn-off threshold or a thermal overload occurs.

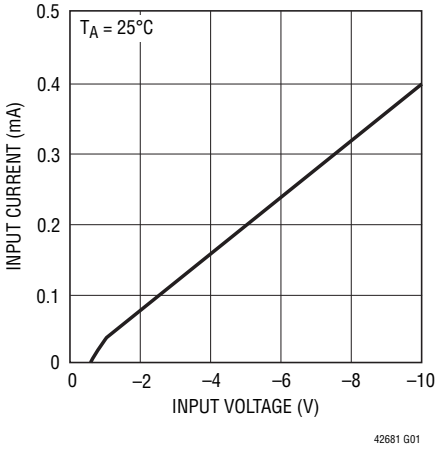
Note 19: The LTC4268-1 features thermal overload protection. In the event of an over temperature condition, the LTC4268-1 will turn off the power MOSFET, disable the classification load current, and present an invalid power good signal. Once the LTC4268-1 cools below the over temperature limit, the LTC4268-1 current limit switches to I_{LIMIT_LOW} and normal operation resumes.

Note 20: I_{LIMIT_DISA} is a safeguard current limit that is activated when the normal input current limit (I_{LIMIT_HIGH}) is defeated using the I_{LIM_EN} pin. Currents at or near I_{LIMIT_DISA} will cause significant package heating and may require a reduced maximum ambient operating temperature in order to avoid tripping the thermal overload protection.

Note 21: Component value range guaranteed by design.

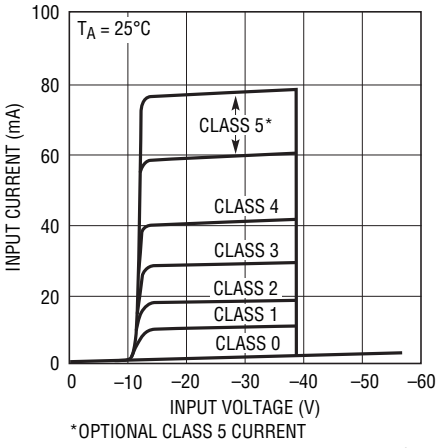
TYPICAL PERFORMANCE CHARACTERISTICS

Input Current vs Input Voltage 25k Detection Range



42681 G01

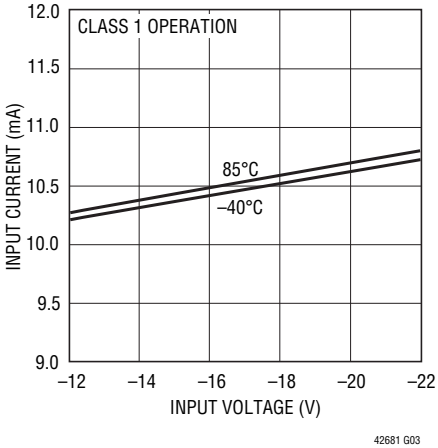
Input Current vs Input Voltage



*OPTIONAL CLASS 5 CURRENT

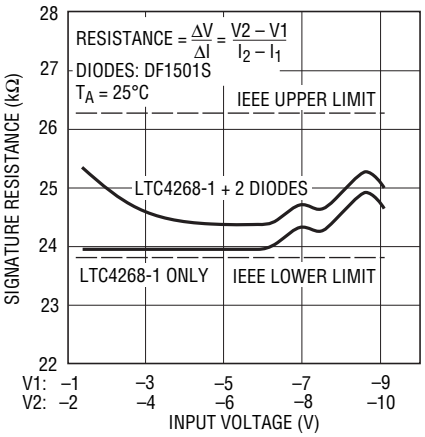
42681 G02

Input Current vs Input Voltage



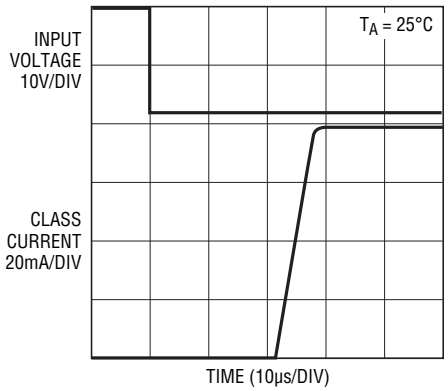
42681 G03

Signature Resistance vs Input Voltage



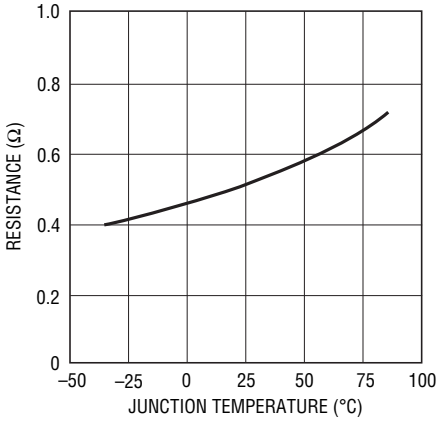
42681 G04

Class Operation vs Time



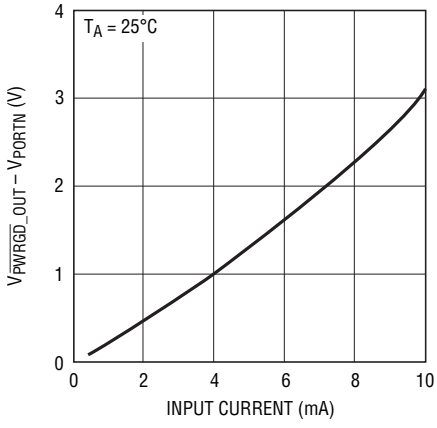
42681 G05

On Resistance vs Temperature



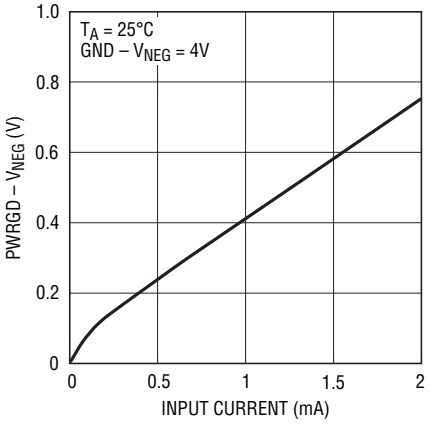
42681 G06

Active Low $\overline{\text{PWRGD}}$: Output Low Voltage vs Current



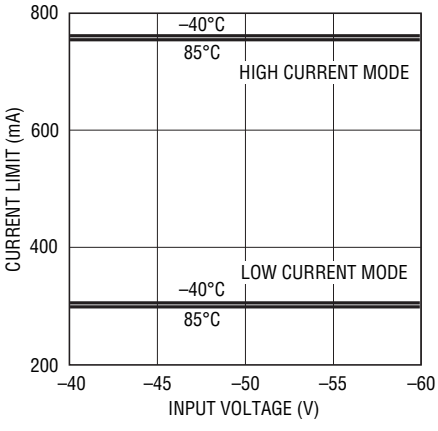
42681 G07

Active High PWRGD: Output Low Voltage vs Current



42681 G08

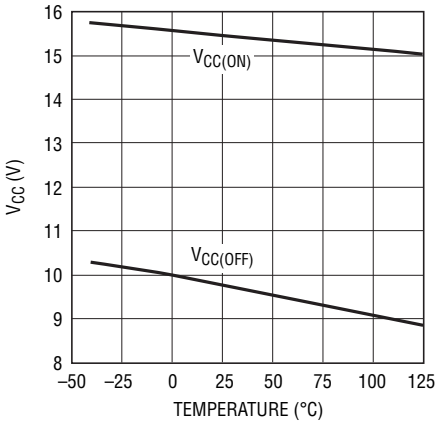
Current Limit vs Input Voltage



42681 G09

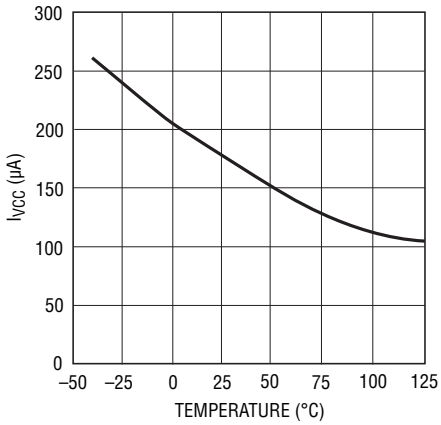
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{CC(ON)}$ and $V_{CC(OFF)}$ vs Temperature



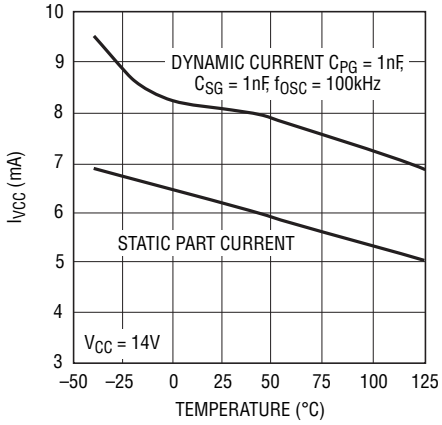
42681 G10

V_{CC} Start-Up Current vs Temperature



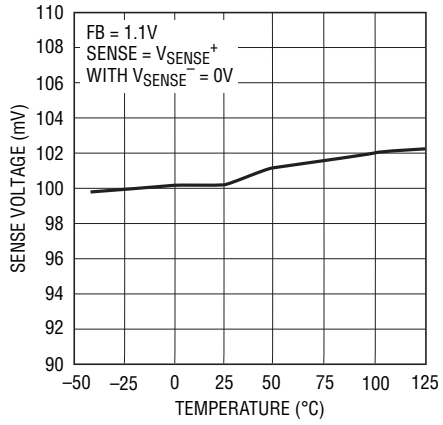
42681 G11

V_{CC} Current vs Temperature



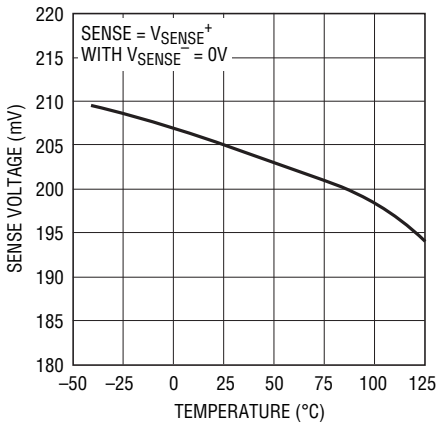
42681 G12

SENSE Voltage vs Temperature



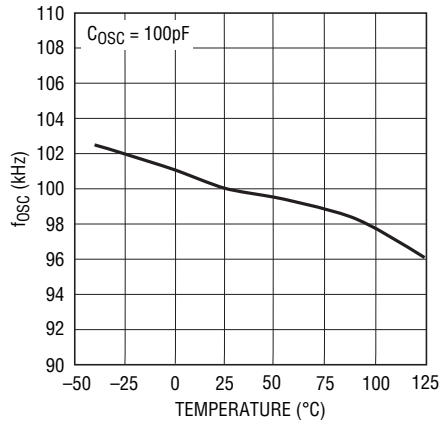
42681 G13

SENSE Fault Voltage vs Temperature



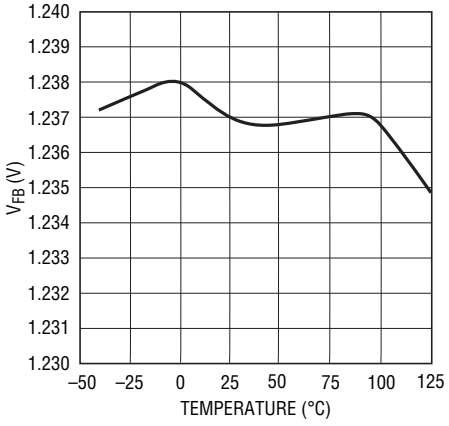
42681 G14

Oscillator Frequency vs Temperature



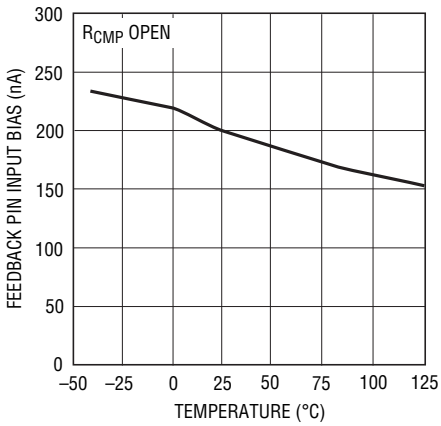
42681 G15

V_{FB} vs Temperature



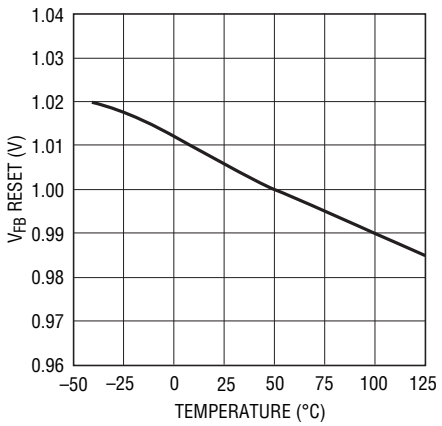
42681 G16

Feedback Pin Input Bias vs Temperature



42681 G17

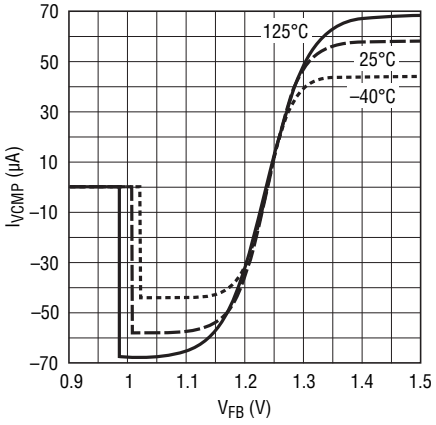
V_{FB} Reset vs Temperature



42681 G18

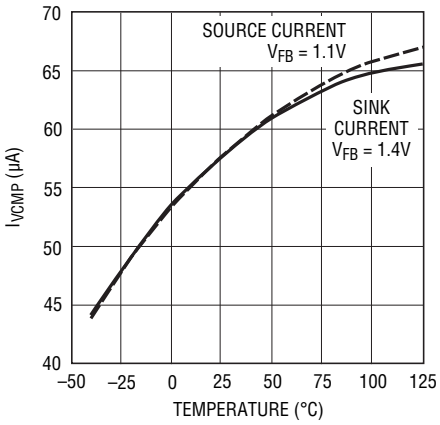
TYPICAL PERFORMANCE CHARACTERISTICS

Feedback Amplifier Output Current vs V_{FB}



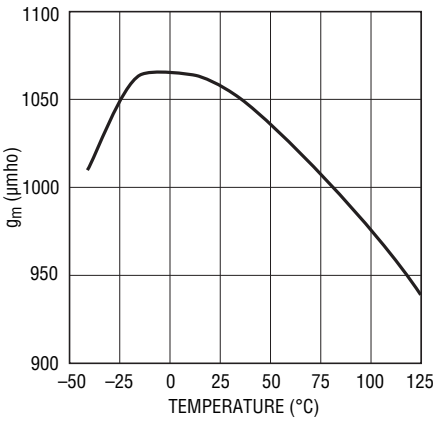
42681 G19

Feedback Amplifier Source and Sink Current vs Temperature



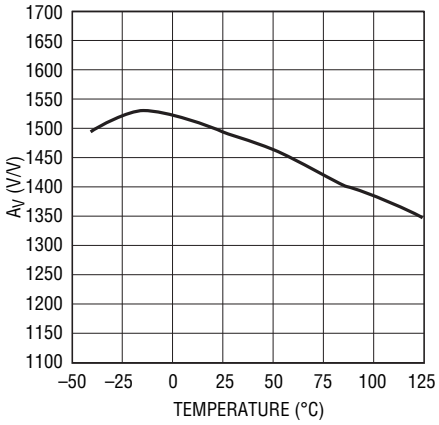
42681 G20

Feedback Amplifier g_m vs Temperature



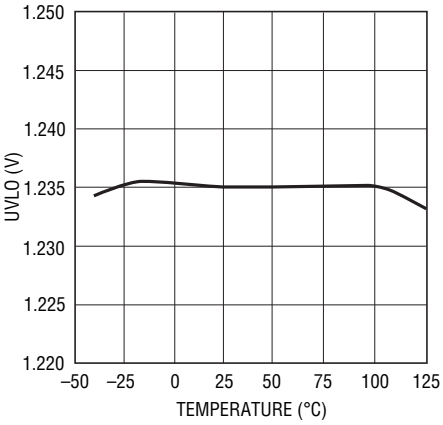
42681 G21

Feedback Amplifier Voltage Gain vs Temperature



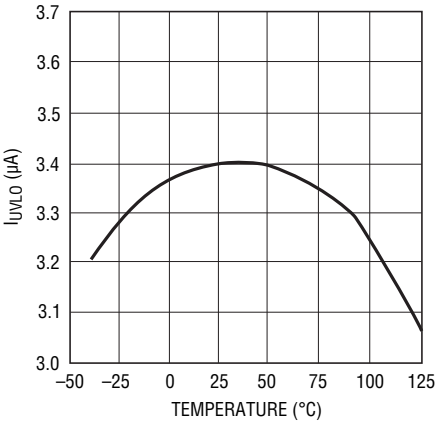
42681 G22

UVLO vs Temperature



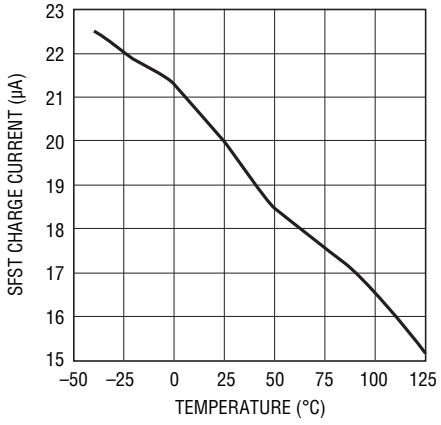
42681 G23

I_{UVLO} Hysteresis vs Temperature



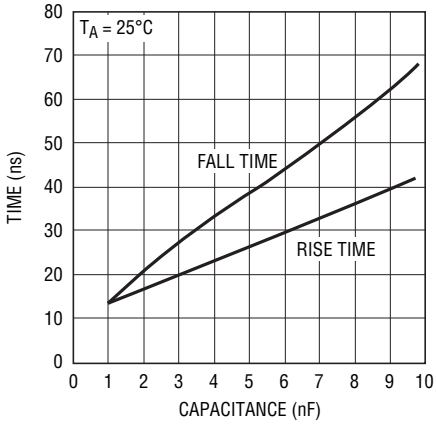
42681 G24

Soft-Start Charge Current vs Temperature



42681 G25

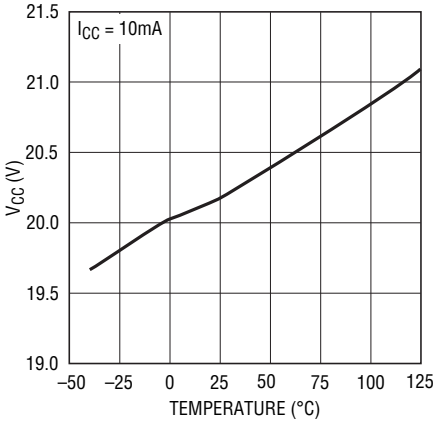
PG, SG Rise and Fall Times vs Load Capacitance



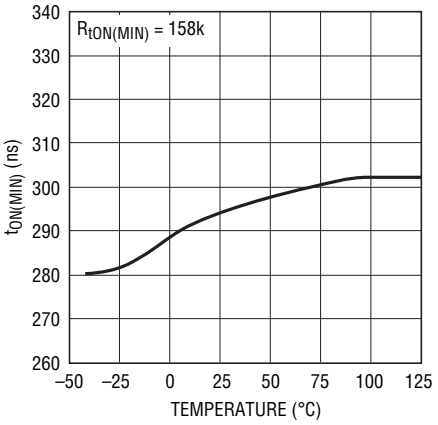
42681 G26

TYPICAL PERFORMANCE CHARACTERISTICS

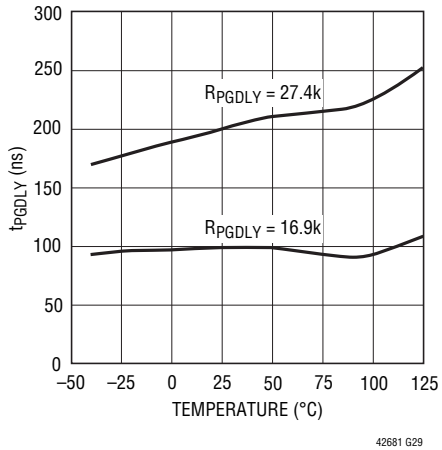
V_{CC} Clamp Voltage vs Temperature



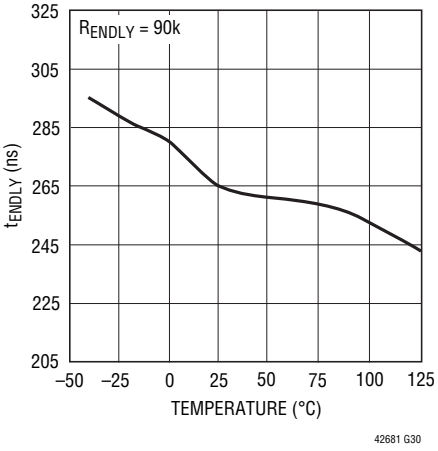
Minimum PG On Time vs Temperature



PG Delay Time vs Temperature



Enable Delay Time vs Temperature



PIN FUNCTIONS

SHDN (Pin 1): Shutdown Input. Used to command the LTC4268-1 to present an invalid signature and remain inactive. Connecting SHDN to V_{PORTP} lowers the signature resistance to an invalid value and disables the LTC4268-1 PD interface operations. If unused, tie SHDN to V_{PORTN}.

NC (Pin 2): No Internal Connection.

R_{CLASS} (Pin 3): Class Select Input. Used to set the current the LTC4268-1 maintains during classification. Connect a resistor between R_{CLASS} and V_{PORTN}. (See Table 2.)

I_{LIM_EN} (Pin 4): Input Current Limit Enable. Used for controlling the LTC4268-1 current limit behavior during powered operation. For normal operation, float I_{LIM_EN} to enable I_{LIMIT_HIGH} current. Tie I_{LIM_EN} to V_{PORTN} to disable input current limit. Note that the inrush current limit will always be active. See Applications Information.

V_{PORTN} (Pins 5, 6, 7): Power Input. Tie to the PD Input through the diode bridge. Pins 5, 6 and 7 must be electrically tied together.

NC (Pin 8): No Internal Connection.

SG (Pin 9): Secondary Gate Driver Output. This pin provides an output signal for a secondary-side synchronous switch. Large dynamic currents may flow during voltage transitions. See the Applications Information for details.

V_{CC} (Pin 10): Converter Voltage Supply. Bypass this pin to GND with 4.7µF or greater. This pin has a 20V clamp to ground. V_{CC} has an undervoltage lockout function that turns on when V_{CC} is approximately 15.3V and off at 9.7V. In a conventional "trickle-charge" bootstrapped configuration, the V_{CC} supply current increases significantly during turn-on causing a benign relaxation oscillation action on the V_{CC} pin if the part does not start normally.

t_{ON} (Pin 11): Primary Switch Minimum On Time Control. A programming resistor (R_{Ton}) to GND sets the minimum time for each cycle. See Applications Information for details.

ENDLY (Pin 12): Enable Delay Time Control. The enable delay time is set by a programming resistor (R_{ENDLY}) to GND and disables the feedback amplifier for a fixed time after the turn-off of the primary-side MOSFET. This allows the leakage inductance voltage spike to be ignored for flyback voltage sensing. See Applications Information for details.

SYNC (Pin 13): External Sync Input. This pin is used to synchronize the internal oscillator with an external clock. The positive edge of the clock causes the oscillator to discharge causing PG to go low (off) and SG high (on). The sync threshold is typically 1.5V. Tie to ground if unused. See Applications Information for details.

SFST (Pin 14): Soft-Start. This pin, in conjunction with a capacitor (C_{SFST}) to GND, controls the ramp-up of peak primary current through the sense resistor. It is also used to control converter inrush at start-up. The SFST clamps the V_{CMP} voltage and thus limits peak current until soft-start is complete. The ramp time is approximately 70ms per µF of capacitance. Leave SFST open if not using the soft-start function.

OSC (Pin 15): Oscillator. This pin in conjunction with an external capacitor (C_{OSC}) to GND defines the controller oscillator frequency. The frequency is approximately 100kHz • 100/C_{OSC} (pF).

FB (Pin 16): Feedback Amplifier Input. Feedback is usually sensed via a third winding and enabled during the flyback period. This pin also sinks additional current to compensate for load current variation as set by the R_{CMP} pin. Keep the Thevenin equivalent resistance of the feedback divider at roughly 3k.

V_{CMP} (Pin 17): Frequency Compensation Control. V_{CMP} is used for frequency compensation of the switcher control loop. It is the output of the feedback amplifier and the input to the current comparator. Switcher frequency compensation components are normally placed on this pin to GND. The voltage on this pin is proportional to the peak primary switch current. The feedback amplifier output is enabled during the synchronous switch on time.

UVLO (Pin 18): Undervoltage Lockout. A resistive divider from V_{IN} to this pin sets an undervoltage lockout based upon V_{IN} level (not V_{CC}). When the UVLO pin is below its threshold, the gate drives are disabled, but the part draws its normal quiescent current from V_{CC}. The V_{CC} undervoltage lockout supersedes this function so V_{CC} must be great enough to start the part. The bias current on this pin has hysteresis such that the bias current is sourced when UVLO threshold is exceeded. This introduces a hysteresis at the pin equivalent to the bias current change times the imped-

PIN FUNCTIONS

ance of the upper divider resistor. The user can control the amount of hysteresis by adjusting the impedance of the divider. Tie the UVLO pin to V_{CC} if you are not using this function. See the Applications Information for details. This pin is used for the UVLO function of the switching regulator. The PD interface section has an UVLO defined by the IEEE 802.3af specification.

SENSE–, SENSE+ (Pins 19, 20): Current Sense Inputs. These pins are used to measure primary side switch current through an external sense resistor. Peak primary side current is used in the converter control loop. Make Kelvin connections to the sense resistor R_{SENSE} to reduce noise problems. SENSE– connects to the GND side. At maximum current (V_{CMP} at its maximum voltage) SENSE pins have 100mV threshold. The signal is blanked (ignored) during the minimum turn-on time.

C_{CMP} (Pin 21): Load Compensation Capacitive Control. Connect a capacitor from C_{CMP} to GND in order to reduce the effects of parasitic resistances in the feedback sensing path. A 0.1µF ceramic capacitor suffices for most applications. Short this pin to GND in less demanding applications.

R_{CMP} (Pin 22): Load Compensation Resistive Control. Connect a resistor from R_{CMP} to GND in order to compensate for parasitic resistances in the feedback sensing path. In less demanding applications, this resistor is not needed and this pin can be left open. See Applications Information for details.

PGDLY (Pin 23): Primary Gate Delay Control. Connect an external programming resistor (R_{PGDLY}) to set delay from synchronous gate turn-off to primary gate turn-on. See Applications Information for details.

PG (Pin 24): Primary Gate Drive. PG is the gate drive pin for the primary side MOSFET Switch. Large dynamic currents flow during voltage transitions. See the Applications Information for details.

NC (Pin 25): No Internal Connection.

V_{NEG} (Pins 26, 27, 28): System Negative Rail. Tie to the GND pin to supply power to the flyback controller through the internal power MOSFET. V_{NEG} is high impedance until the input voltage rises above the UVLO turn-on threshold. The output is then connected to V_{PORTN} through a current-limited internal MOSFET switch. Pins 26, 27 and 28 must be electrically tied together.

PWRGD (Pin 29): Active High Power Good Output, Open-Collector. Signals to the flyback controller that the LTC4268-1 MOSFET is on and that the flyback controller can start operation. High impedance indicates power is good. PWRGD is referenced to V_{NEG} and is low impedance during inrush and in the event of a thermal overload. PWRGD is clamped to 14V above V_{NEG}.

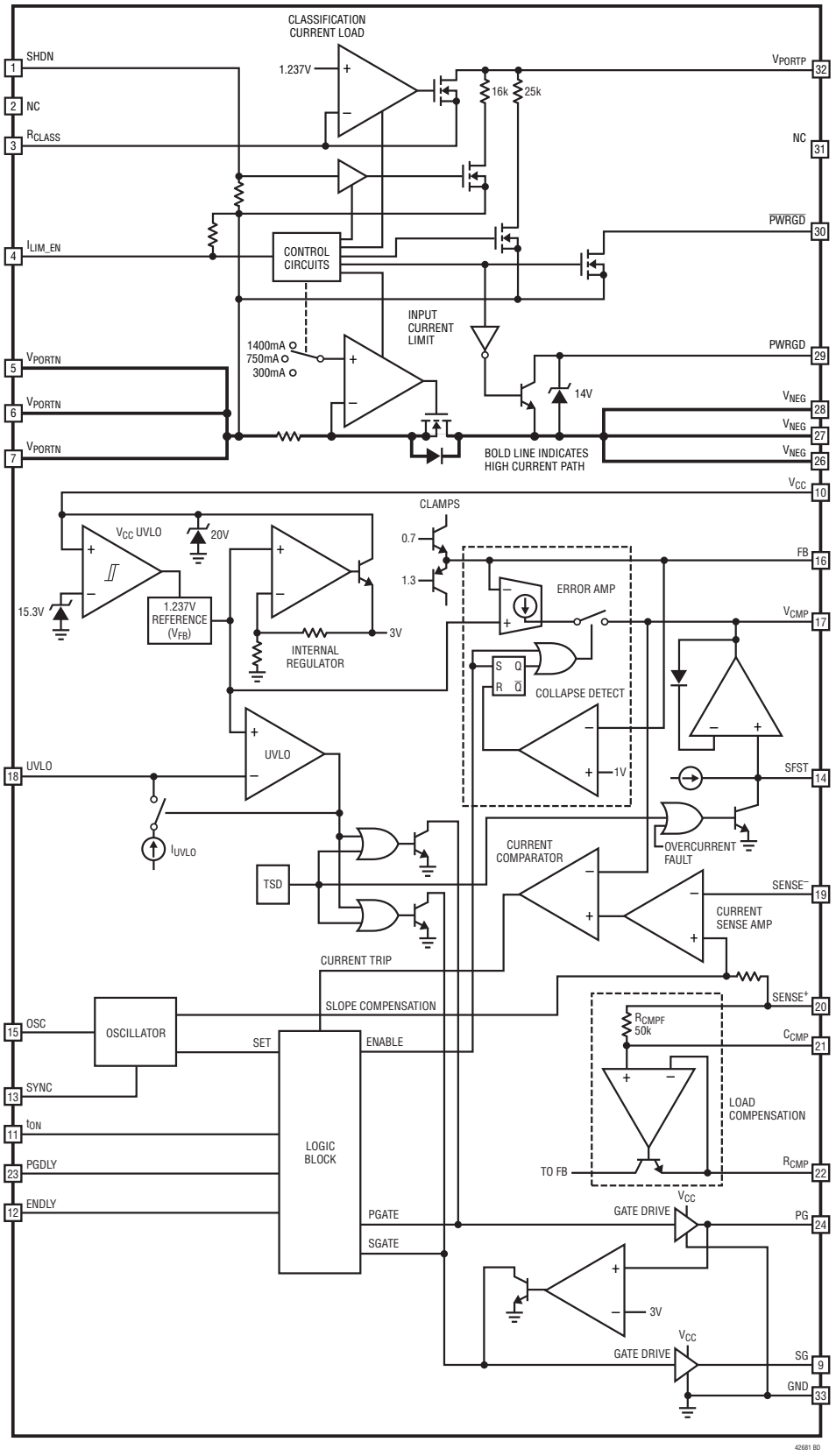
$\overline{\text{PWRGD}}$ (Pin 30): Active Low Power Good Output, Open-Drain. Signals to the DC/DC converter that the LTC4268-1 MOSFET is on and that the converter can start operation. Low impedance indicates power is good. $\overline{\text{PWRGD}}$ is referenced to V_{PORTN} and is high impedance during detection, classification and in the event of a thermal overload. $\overline{\text{PWRGD}}$ has no internal clamps.

NC (Pin 31): No Internal Connection.

V_{PORTP} (Pin 32): Positive Power Input. Tie to the input port power return through the input diode bridge.

GND (Pin 33): Ground. This is the negative rail connection for both signal ground and gate driver grounds. This pin should be connected to V_{NEG}. Careful attention must be paid to layout. See the Applications Information for details.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

OVERVIEW

Power over Ethernet (PoE) continues to gain popularity as an increasing number of products are taking advantage of having DC power and high speed data available from a single RJ45 connector. As PoE is becoming established in the marketplace, Powered Device (PD) equipment vendors are running into the 12.95W power limit established by the IEEE 802.3af standard. To solve this problem and expand the application of PoE, the LTC4268-1 breaks the power barrier by allowing custom PoE applications to deliver up to 35W for power hungry PoE applications such as dual band access points, RFID readers and PTZ security cameras.

The LTC4268-1 is designed to be a complete solution for PD applications with power requirements up to 35W. The LTC4268-1 interfaces with custom Power Sourcing Equipment (PSE) using a high efficiency flyback topology for maximum power delivery without the need for opto-isolator feedback. Off-the-shelf high power PSEs are available today from a variety of vendors for use with the LTC4268-1 to allow quick implementation of a custom system.

OPERATION

Note: Please refer to the simplified application circuit (Figure 1) for voltage naming conventions used in this data sheet.

The LTC4268-1 high power PD interface controller and switching regulator has several modes of operation depending on the applied V_{PORT} voltage as shown in Figure 2 and summarized in Table 1. These various modes satisfy the requirements defined in the IEEE 802.3af specification. The input voltage is applied to the V_{PORTN} pin with reference to the V_{PORTP} pin and is always negative.

SERIES DIODES

The IEEE 802.3af-defined operating modes for a PD reference the input voltage at the RJ45 connector on the PD. In this data sheet port voltage is normally referenced to the pins of the LTC4268-1. Note that the voltage ranges specified in the LTC4268-1 Electrical Specifications are referenced with respect to the IC pins.

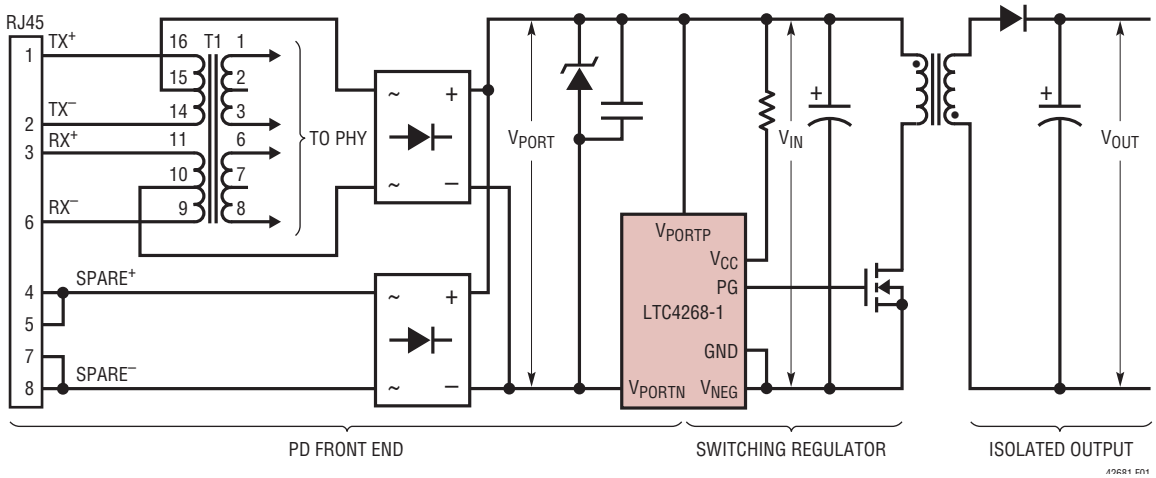


Figure 1. Simplified Application Circuit With Voltage Naming Conventions

APPLICATIONS INFORMATION

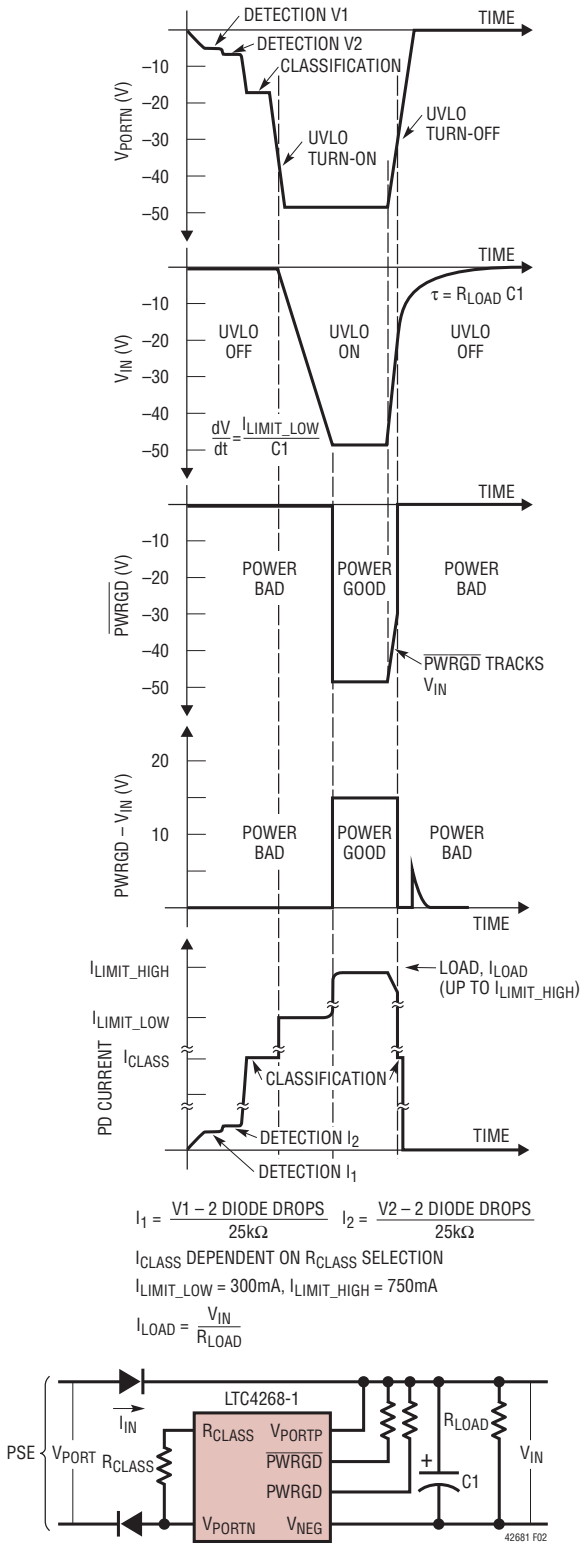


Figure 2. V_{IN} Voltage, $\overline{PWRGD}$, PWRGD and PD Current as a Function of Port Voltage

The PD must be able to handle power received in either polarity. For this reason, it is common to install diode bridges between the RJ45 connector and the LTC4268-1 (Figure 3). The diode bridges introduce an offset that affects the threshold points for each range of operation. The LTC4268-1 meets the IEEE 802.3af-defined operating modes by compensating for the diode drops in the threshold points. For the signature, classification, and the UVLO thresholds, the LTC4268-1 extends two diode drops below the IEEE 802.3af specifications. The LTC4268-1 threshold points support the use of either traditional or Schottky diode bridges.

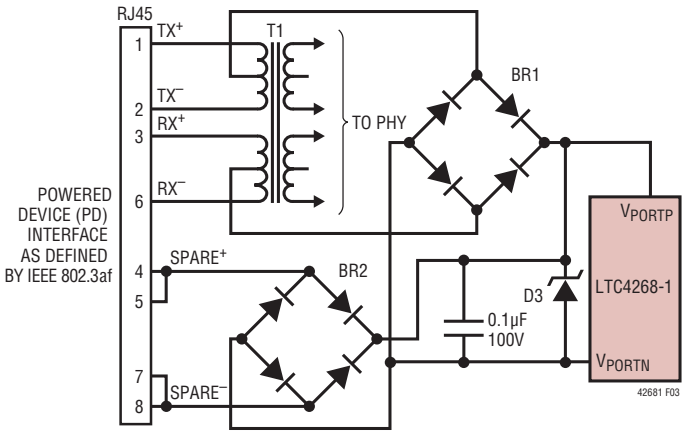


Figure 3. PD Front End Using Diode Bridges on Main and Spare Inputs

DETECTION

During detection, the PSE will apply a voltage in the range of –2.8V to –10V on the cable and look for a 25k signature resistor. This identifies the device at the end of the cable as a PD. With the PSE voltage in the detection range, the LTC4268-1 presents an internal 25k resistor between the V_{PORTP} and V_{PORTN} pins. This precision, temperature-compensated resistor provides the proper characteristics to alert the PSE that a PD is present and requests power to be applied.

APPLICATIONS INFORMATION

Table 1. LTC4268-1 Operational Mode as a Function of V_{PORT} Voltage

V_{PORT}	MODE OF OPERATION
0V to –1.4V	Inactive
–1.5V to –10.1V	25k Signature Resistor Detection
–10.3V to –12.4V	Classification Load Current Ramps Up from 0% to 100%
–12.5V to UVLO*	Classification Load Current Active
UVLO* to –57V	Power Applied to PD Load

*UVLO includes hysteresis.
Rising input threshold ≅ –38.9V
Falling input threshold ≅ –30.6V

The IEEE 802.3af specification requires the PSE to use a ΔV/ΔI measurement technique to keep the DC offset voltage of the diode bridge from affecting the signature resistance measurement. However, the diode resistance appears in series with the signature resistor and must be included in the overall signature resistance of the PD.

The LTC4268-1 compensates for the two series diodes in the signature path by offsetting the internal resistance so that a PD built with the LTC4268-1 meets the IEEE 802.3af specification.

In some designs that include an auxiliary power option, such as an external wall adapter, it is necessary to control whether or not the PD is detected by a PSE. With the LTC4268-1, the 25k signature resistor can be enabled or disabled with the SHDN pin (Figure 4). Taking the SHDN pin high will reduce the signature resistor to 10k which is an invalid signature per the IEEE 802.3af specifications. This will prevent a PSE from detecting and powering the PD. This invalid signature is present in the PSE probing range of –2.8V to –10V. When the input rises above –10V, the signature resistor reverts to 25k to minimize power dissipation in the LTC4268-1. To disable the signature, tie SHDN to V_{PORTP}. Alternately, the SHDN pin can be driven high with respect to V_{PORTN}. When SHDN is high, all functions are disabled. For normal operation tie SHDN to V_{PORTN}.

CLASSIFICATION

Once the PSE has detected a PD, the PSE may optionally classify the PD. Classification provides a method for more efficient allocation of power by allowing the PSE to identify lower-power PDs and assign the appropriate power level to these devices. For each class, there is an associated load current that the PD asserts onto the line during classification probing. The PSE measures the PD load current in order to assign the proper PD classification. Class 0 is included in the IEEE 802.3af specification to cover PDs that do not support classification. Class 1-3 partition PDs into three distinct power ranges as shown in Table 2.

Table 2. Summary of IEEE 802.3af Power Classifications and LTC4268-1 R_{CLASS} Resistor Selection

CLASS	USAGE	MAXIMUM POWER LEVELS AT INPUT OF PD (W)	NOMINAL CLASSIFICATION LOAD CURRENT (mA)	LTC4268-1 RCLASS RESISTOR (Ω, 1%)
0	Default	0.44 to 13.0	<5	Open
1	Optional	0.44 to 3.84	10.5	124
2	Optional	3.84 to 6.49	18.5	69.8
3	Optional	6.49 to 13.0	28	45.3
4	Reserved by IEEE. See Apps		40	30.9
5	Undefined by IEEE. See Apps		56	22.1

Class 4 was reserved by the IEEE 802.3af committee for future use and has been reassigned as a high power indicator by IEEE 802.3at. The new Class 5 defined here is available for system vendors to implement a unique

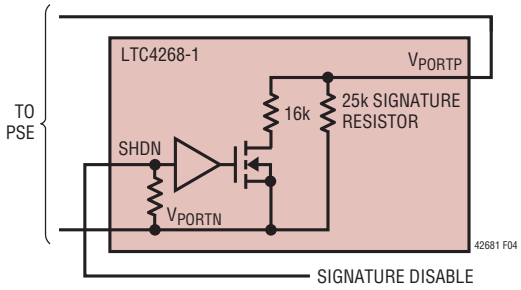


Figure 4. 25k Signature Resistor With Disable

APPLICATIONS INFORMATION

classification for use in closed systems and is not defined or supported by the IEEE 802.3af. With the extended classification range available in the LTC4268-1, it is possible for system designers to define multiple classes using load currents between 40mA and 75mA.

During classification, the PSE presents a fixed voltage between –15.5V and –20.5V to the PD (Figure 5). With the input voltage in this range, the LTC4268-1 asserts a load current from the V_{PORTP} pin through the R_{CLASS} resistor. The magnitude of the load current is set with the selection of the R_{CLASS} resistor. The resistor value associated with each class is shown in Table 2.

A substantial amount of power is dissipated in the LTC4268-1 during classification. The IEEE 802.3af specification limits the classification time to 75ms in order avoid excessive heating. The LTC4268-1 is designed to handle the power dissipation during the probe period. If the PSE probing exceeds 75ms, the LTC4268-1 may overheat. In this situation, the thermal protection circuit will engage and disable the classification current source, protecting the LTC4268-1 from damage. When the die cools, classification is automatically resumed.

Classification presents a challenging stability problem for the PSE due to the wide range of loads possible. The LTC4268-1 has been designed to avoid PSE interoperability problems by maintaining a positive I-V slope throughout the signature and classification ranges up to UVLO turn on as shown in Figure 6. The positive I-V slope avoids areas of negative resistance and helps prevent the PSE from power cycling or getting "stuck" during signature or classification probing. In the event a PSE overshoots beyond the classification voltage range, the available load current aids in returning the PD back into the classification voltage range. (The PD input may otherwise be "trapped" by a reverse-biased diode bridge and the voltage held by the 0.1µF capacitor.) By gently ramping the classification current on and maintaining a positive I-V slope until UVLO turn-on, the LTC4268-1 provides a well behaved load, assuring interoperability with any PSE.

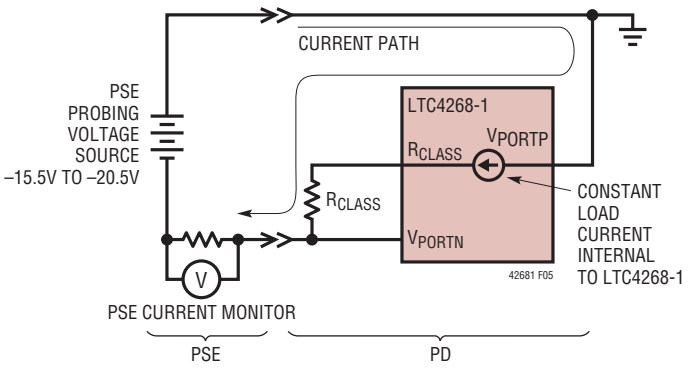


Figure 5. PSE Probing PD During Classification

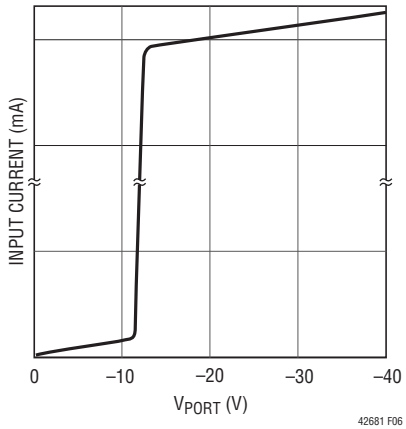


Figure 6. LTC4268-1 Positive I-V Slope

APPLICATIONS INFORMATION

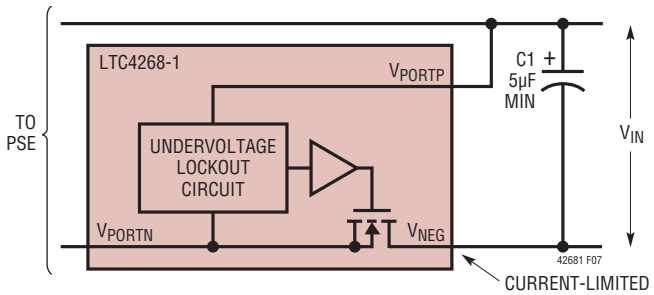
UNDERVOLTAGE LOCKOUT

The IEEE 802.3af specification dictates a maximum turn-on voltage of 42V and a minimum turn-off voltage of 30V for the PD. In addition, the PD must maintain large on-off hysteresis to prevent current-resistance (I-R) drops in the wiring between the PSE and the PD from causing start-up oscillation. The LTC4268-1 incorporates an undervoltage lockout (UVLO) circuit that monitors line voltage at V_{PORTN} to determine when to apply power to the PD load (Figure 7). Before power is applied to the load, the V_{NEG} pin is high impedance and there is no charge on capacitor C1. When the input voltage rises above the UVLO turn-on threshold, the LTC4268-1 removes the classification load current and turns on the internal power MOSFET. C1 charges up under LTC4268-1 inrush current limit control and the V_{NEG} pin transitions from 0V to V_{PORTN} as shown in Figure 2. The LTC4268-1 includes a hysteretic UVLO circuit on V_{PORTN} that keeps power applied to the load until the magnitude of the input voltage falls below the UVLO turn-off threshold. Once V_{PORTN} falls below UVLO turn-off, the internal power MOSFET disconnects V_{NEG} from V_{PORTN} and the classification current is re-enabled. C1 will discharge through the PD circuitry and the V_{NEG} pin will go to a high impedance state.

INPUT CURRENT LIMIT

IEEE 802.3af specifies a maximum inrush current and also specifies a minimum load capacitor between the V_{PORTP} and V_{NEG} pins. To control turn-on surge currents in the system the LTC4268-1 integrates a dual current limit circuit using an onboard power MOSFET and sense resistor to provide a complete inrush control circuit without additional external components. At turn-on, the LTC4268-1 will limit the inrush current to I_{LIMIT_LOW}, allowing the load capacitor to ramp up to the line voltage in a controlled manner without interference from the PSE current limit. By keeping the PD current limit below the PSE current limit, PD power up characteristics are well controlled and independent of PSE behavior. This ensures interoperability regardless of PSE output characteristics.

After load capacitor C1 is charged up, the LTC4268-1 switches to the high input current limit, I_{LIMIT_HIGH}. This allows the LTC4268-1 to deliver up to 35W to the PD load for high power applications. To maintain compatibility with IEEE 802.3af power levels, it is necessary for the PD designer to ensure the PD steady-state power consumption remains below the limits shown in Table 2. The LTC4268-1 maintains the high input current limit until the port voltage drops below the UVLO turn-off threshold.



V_{PORT} VOLTAGE	LTC4268-1 POWER MOSFET
0V TO UVLO*	OFF
>UVLO*	ON

*UVLO INCLUDES HYSTERESIS
RISING INPUT THRESHOLD ≅ –38.9V
FALLING INPUT THRESHOLD ≅ –30.6V

Figure 7. LTC4268-1 Undervoltage Lockout

APPLICATIONS INFORMATION

During the inrush event as C1 is being charged, a large amount of power is dissipated in the MOSFET. The LTC4268-1 is designed to accept this load and is thermally protected to avoid damage to the onboard power MOSFET. If a thermal overload does occur, the power MOSFET turns off, allowing the die to cool. Once the die has returned to a safe temperature, the LTC4268-1 automatically switches to I_{LIMIT_LOW}, and load capacitor C1 charging resumes.

The LTC4268-1 has the option of disabling the normal operating input current limit, I_{LIMIT_HIGH}, for custom high power PoE applications. To disable the current limit, connect I_{LIM_EN} to V_{PORTN}. To protect the LTC4268-1 from damage when the normal current limit is disabled, a safeguard current limit, I_{LIMIT_DISA} keeps the current below destructive levels, typically 1.4A. Note that continuous operation at or near the safeguard current limit will rapidly overheat the LTC4268-1, engaging the thermal protection circuit. For normal operations, float the I_{LIM_EN} pin. The LTC4268-1 maintains the I_{LIMIT_LOW} inrush current limit for charging the load capacitor regardless of the state of I_{LIM_EN}. The operation of the I_{LIM_EN} pin is summarized in Table 3.

Table 3. Summary of IEEE 802.3af Power Classifications and LTC4268-1 R_{CLASS} Resistor Selection

STATE OF I_{LIM_EN}	INRUSH CURRENT LIMIT	OPERATING INPUT CURRENT LIMIT
Floating	I_{LIMIT_LOW}	I_{LIMT_HIGH}
Tied to V_{PORTN}	I_{LIMIT_LOW}	I_{LIMIT_DISA}

POWER GOOD

The LTC4268-1 includes complementary power good outputs (Figure 8) to simplify connection to any DC/DC converter. Power Good is asserted at the end of the inrush event when load capacitor C1 is fully charged and the DC/DC converter can safely begin operation. The power good signal stays active during normal operation and is de-asserted at power off when the port drops below the UVLO threshold or in the case of a thermal overload event. For PD designs that use a large load capacitor and also

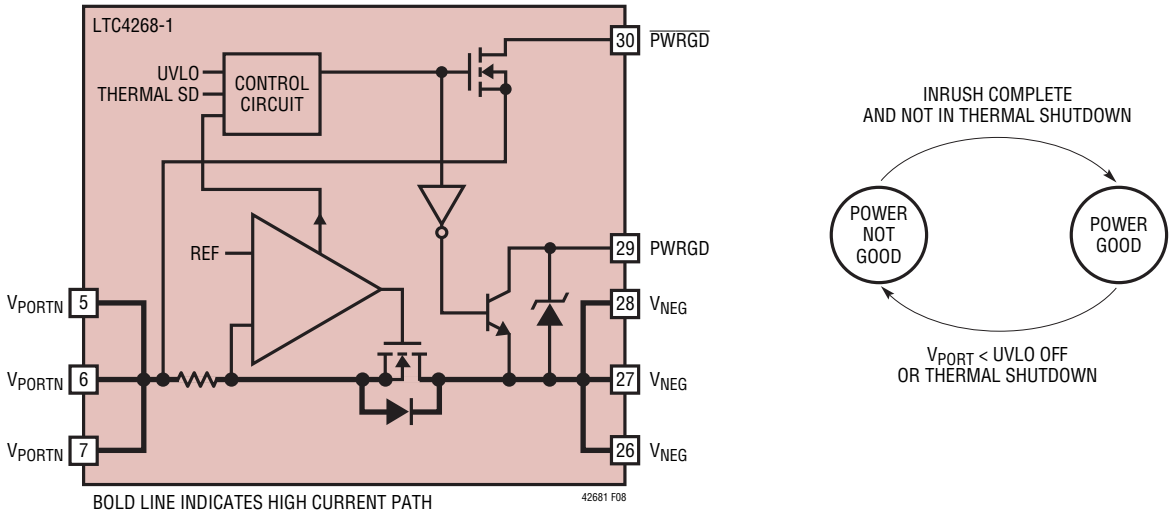


Figure 8. LTC4268-1 Power Good Functional and State Diagram

APPLICATIONS INFORMATION

consume a lot of power, it is important to delay activation of the DC/DC converter with the power good signal. If the converter is not disabled during the current-limited turn-on sequence, the DC/DC converter will rob current intended for charging up the load capacitor and create a slow rising input, possibly causing the LTC4268-1 to go into thermal shutdown.

The active high PWRGD pin features an internal, open-collector output referenced to V_{NEG}. During inrush, the active high PWRGD pin becomes valid when C1 reaches –4V and pulls low until the load capacitor is fully charged. At that point, PWRGD becomes high impedance, indicating the switching regulator may begin running. The active high PWRGD pin interfaces directly to the UVLO pin of the LTC4268-1 with the aid of an external pull-up resistor to Vcc. The PWRGD pin includes an internal 14V clamp to V_{NEG}. During a power supply ramp down event, PWRGD becomes low impedance when V_{PORT} drops below the 30V PD UVLO turn-off threshold, then goes high impedance when the V_{PORT} voltages fall to within the detection voltage range. Figure 11 shows a typical connection scheme for the active high PWRGD pin.

The LTC4268-1 also includes an active low $\overline{PWRGD}$ pin for system level use. $\overline{PWRGD}$ is referenced to the V_{PORTN} pin and when active will be near the V_{PORTN} potential. The negative rail (GND) of the internal switching regulator will typically be referenced to V_{NEG} and care must be taken to ensure that the difference in potential of the $\overline{PWRGD}$ pin does not cause a problem for the switcher.

THERMAL PROTECTION

The LTC4268-1 includes thermal overload protection in order to provide full device functionality in a miniature package while maintaining safe operating temperatures. At turn-on, before load capacitor C1 has charged up, the instantaneous power dissipated by the LTC4268-1 can be as high as 20W. As the load capacitor charges, the power dissipation in the LTC4268-1 will decrease until it reaches a steady-state value dependent on the DC load current. The LTC4268-1 can also experience device heating after turn-on if the PD experiences a fast input voltage rise. For example, if the PD input voltage steps from –37V to –57V, the instantaneous power dissipated by the LTC4268-1 can be as high as 16W. The LTC4268-1 protects itself from damage by monitoring die temperature. If the die exceeds the overtemperature trip point, the power MOSFET and classification transistors are disabled until the part cools down. Once the die cools below the overtemperature trip point, all functions are enabled automatically. During classification, excessive heating of the LTC4268-1 can occur if the PSE violates the 75ms probing time limit. In addition, the IEEE 802.3af specification requires a PD to withstand application of any voltage from 0V to 57V indefinitely. To protect the LTC4268-1 in these situations, the thermal protection circuitry disables the classification circuit and the input current if the die temperature exceeds the overtemperature trip point. When the die cools down, classification and input current are enabled.

Once the LTC4268-1 has charged up the load capacitor and the PD is powered and running, there will be some residual heating due to the DC load current of the PD flowing through the internal MOSFET. In some high current applications, the LTC4268-1 power dissipation may be significant. The LTC4268-1 uses a thermally enhanced DFN package that includes an exposed pad which should be soldered to the GND plane for heat sinking on the printed circuit board.

MAXIMUM AMBIENT TEMPERATURE

The LTC4268-1 I_{LIM_EN} pin allows the PD designer to disable the normal operating current limit. With the normal current limit disabled, it is possible to pass currents as high as 1.4A through the LTC4268-1. In this mode, significant package heating may occur. Depending on the current, voltage, ambient temperature, and waveform characteristics, the LTC4268-1 may shut down. To avoid nuisance trips of the thermal shutdown, it may be necessary to limit the maximum ambient temperature. Limiting the die temperature to 125°C will keep the LTC4268-1 from hitting thermal shutdown. For DC loads the maximum ambient temperature can be calculated as:

$$T_{MAX} = 125 – \theta_{JA} \bullet PWR\ (°C)$$

where T_{MAX} is the maximum ambient operating temperature, θ_{JA} is the junction-to-ambient thermal resistance (49°C/W), and PWR is the power dissipation for the LTC4268-1 in Watts ($I_{PD}^2 \bullet R_{ON}$).

APPLICATIONS INFORMATION

EXTERNAL INTERFACE AND COMPONENT SELECTION

Transformer

Nodes on an Ethernet network commonly interface to the outside world via an isolation transformer (Figure 9). For powered devices, the isolation transformer must include a center tap on the media (cable) side. Proper termination is required around the transformer to provide correct impedance matching and to avoid radiated and conducted emissions. For high power applications beyond IEEE 802.3af limits, the increased current levels increase the current imbalance in the magnetics. This imbalance reduces the perceived inductance and can interfere with data transmission. Transformers specifically designed for high current applications are required. Transformer vendors such as Bel Fuse, Coilcraft, Halo, Pulse, and Tyco (Table 4) can provide assistance with selection of an appropriate isolation transformer and proper termination methods. These vendors have transformers specifically designed for use in high power PD applications.

Table 4. Power over Ethernet Transformer Vendors

V_{PORT}	MODE OF OPERATION
Bel Fuse Inc.	206 Van Vorst Street Jersey City, NJ 07302 Tel: 201-432-0463 www.belfuse.com
Coilcraft Inc.	1102 Silver Lake Road Gary, IL 60013 Tel: 847-639-6400 www.coilcraft.com
Halo Electronics	1861 Landings Drive Mountain View, CA 94043 Tel: 650-903-3800 www.haloelectronics.com
Pulse Engineering	12220 World Trade Drive San Diego, CA 92128 Tel: 858-674-8100 www.pulseeng.com
Tyco Electronics	308 Constitution Drive Menlo Park, CA 94025-1164 Tel: 800-227-7040 www.circuitprotection.com

IEEE 802.3af allows power wiring in either of two configurations on the TX/RX wires, and power can be applied to the PD via the spare wire pair in the RJ45 connector. The

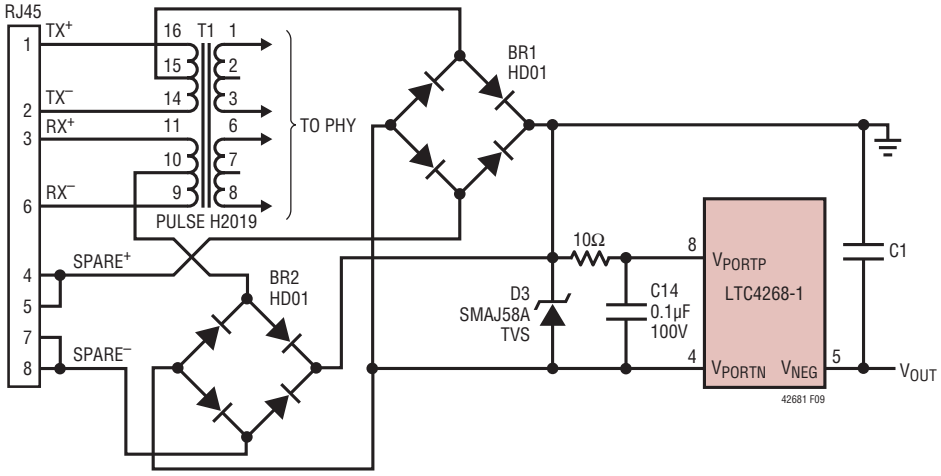


Figure 9. PD Front-End Isolation Transformer, Diode Bridges, Capacitors and TVS

APPLICATIONS INFORMATION

PD is required to accept power in either polarity on both the data and spare inputs; therefore it is common to install diode bridges on both inputs in order to accommodate the different wiring configurations. Figure 9 demonstrates an implementation of the diode bridges to minimize heating. The IEEE 802.3af specification also mandates that the leakage back through the unused bridge be less than 28µA when the PD is powered with 57V.

The LTC4268-1 has several different modes of operation based on the voltage present between the V_{PORTN} and V_{PORTP} pins. The forward voltage drop of the input diodes in a PD design subtracts from the input voltage and will affect the transition point between modes.

The input diode bridge of a PD can consume over 4% of the available power in some applications. Schottky diodes can be used in order to reduce power loss. The LTC4268-1 is designed to work with both standard and Schottky diode bridges while maintaining proper threshold points for IEEE 802.3af compliance.

Input Capacitor

The IEEE 802.3af/at standard includes an impedance requirement in order to implement the AC disconnect function. A 0.1µF capacitor (C14 in Figure 9) is used to meet the AC impedance requirement.

Input Series Resistance

Linear Technology has seen the customer community cable discharge requirements increase by nearly 500,000 times the original test levels. The PD must survive and operate reliably not only when an initially charged cable connects and dissipates the energy through the PD front end, but also when the electrical power system grounds are subject to very high energy events (e.g., lightning strikes).

In these high energy events, adding 10Ω series resistance into the V_{PORTP} pin greatly improves the robustness of the LTC4268-1 based PD (see Figure 9). The TVS limits the voltage across the port while the 10Ω and 0.1µF capacitance reduces the edge rate the LT4268-1 encounters across its pin. The added 10Ω series resistance does not operationally affect the LTC4268-1 PD Interface, nor does it affect its compliance with the IEEE 802.3 standard.

Transient Voltage Suppressor

The LTC4268-1 specifies and absolute maximum voltage of 100V and is designed to tolerate brief overvoltage events. However, the pins that interface to the outside world can routinely see excessive peak voltages. To protect the LTC4268-1, install a transient voltage suppressor (D3) between the input diode bridge and the LTC4268-1, as shown in Figure 9. An SMAJ58A is recommended for typical PD applications. However, an SMBJ58A may be preferred in applications where the PD front end must absorb higher energy discharge events.

Auxiliary Power Source

In some applications, it may be necessary to power the PD from an auxiliary power source such as a wall adapter. The auxiliary power can be injected into the PD at several locations and various trade-offs exist. Figure 10 demonstrates four methods of connecting external power to a PD.

Option 1 in Figure 10 inserts power before the LTC4268-1 interface controller. In this configuration, it is necessary for the wall adapter to exceed the LTC4268-1 UVLO turn-on requirement. This option provides input current limit for the adapter, provides a valid power good signal and simplifies power priority issues. As long as the adapter applies power to the PD before the PSE, it will take priority and the PSE will not power up the PD because the external power source will corrupt the 25k signature. If the PSE is already powering the PD, the adapter power will be in parallel with the PSE. In this case, priority will be given to the higher supply voltage. If the adapter voltage is higher, the PSE may remove the port voltage since no current will be drawn from the PSE. On the other hand, if the adapter voltage is lower, the PSE will continue to supply power to the PD and the adapter will not be used. Proper operation will occur in either scenario.

Option 2 applies power directly to the DC/DC converter. In this configuration the adapter voltage does not need to exceed the LTC4268-1 turn-on UVLO requirement and can be selected based solely on the PD load requirements. It is necessary to include diode D9 to prevent the adapter from applying power to the LTC4268-1. Power priority issues require more intervention. If the adapter voltage is below the PSE voltage, then the priority will be given

APPLICATIONS INFORMATION

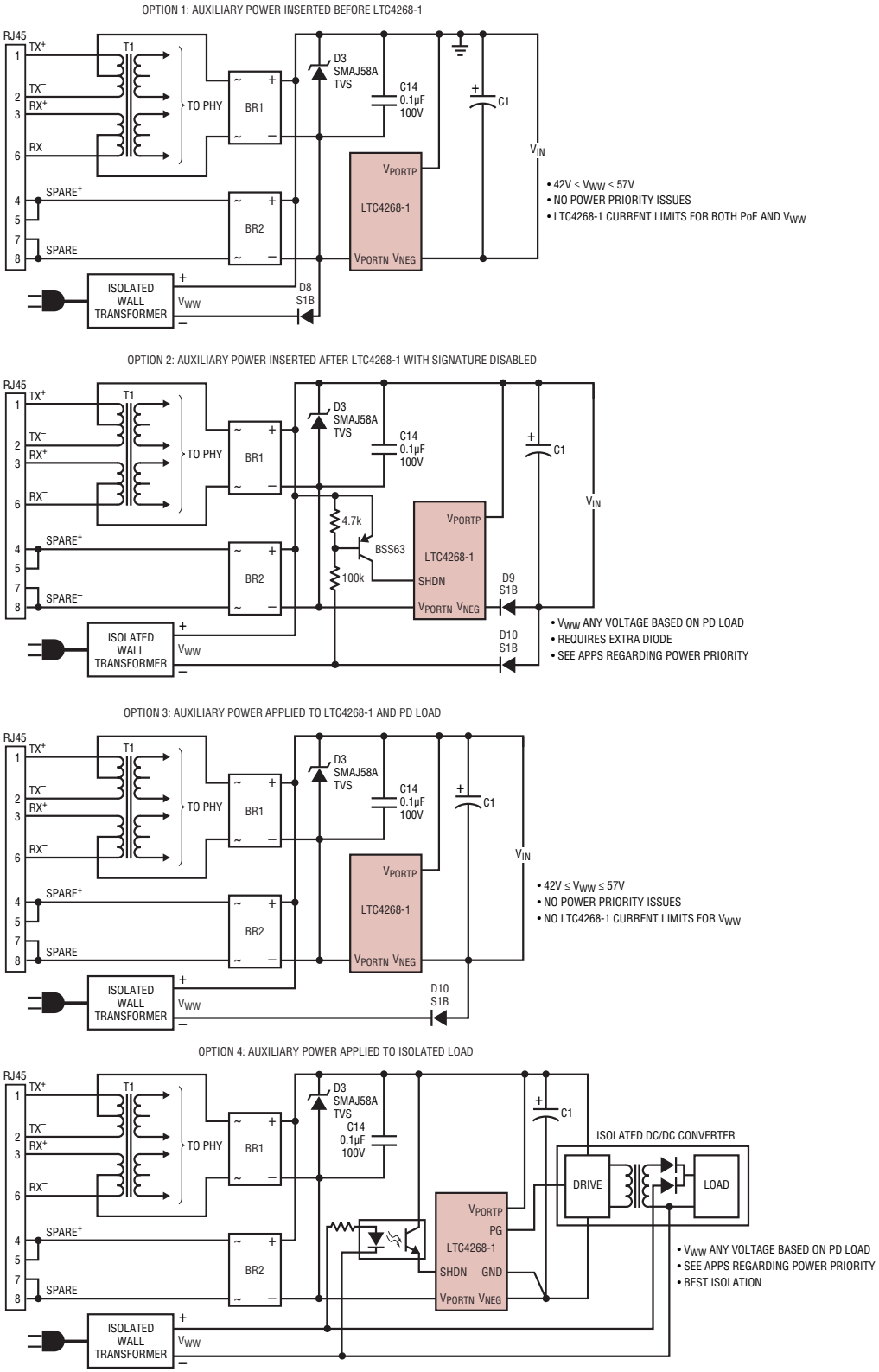


Figure 10. Interfacing Auxiliary Power Source to the PD

APPLICATIONS INFORMATION

to the PSE power. The PD will draw power from the PSE while the adapter will remain unused. This configuration is acceptable in a typical PoE system. However, if the adapter voltage is higher than the PSE voltage, the PD will draw power from the adapter. In this situation, it is necessary to address the issue of power cycling that may occur if a PSE is present. The PSE will detect the PD and apply power. If the PD is being powered by the adapter, then the PD will not meet the minimum load requirement and the PSE may subsequently remove power. The PSE will again detect the PD and power cycling will start. With an adapter voltage above the PSE voltage, it is necessary to either disable the signature as shown in option 2, or install a minimum load on the output of the LTC4268-1 to prevent power cycling. A 3k, 1W resistor connected between V_{PORTP} and V_{NEG} will present the required minimum load.

Option 3 applies power directly to the DC/DC converter bypassing the LTC4268-1 and omitting diode D9. With the diode omitted, the adapter voltage is applied to the LTC4268-1 in addition to the DC/DC converter. For this reason, it is necessary to ensure that the adapter maintain the voltage between 42V and 57V to keep the LTC4268-1 in its normal operating range. The third option has the advantage of corrupting the 25k signature resistance when the external voltage exceeds the PSE voltage and thereby solving the power priority issue.

Option 4 bypasses the entire PD interface and injects power at the output of the low voltage power supply. If the adapter output is below the low voltage output there are no power priority issues. However, if the adapter is above the internal supply, then option 4 suffers from the same power priority issues as option 2 and the signature should be disabled or a minimum load should be installed. Shown in option 4 is one method to disable to the signature while maintaining isolation.

If employing options 1 through 3, it is necessary to ensure that the end-user cannot access the terminals of the auxiliary power jack on the PD since this would compromise IEEE 802.3af isolation requirements and may violate local safety codes. Using option 4 along with an isolated power supply addresses the isolation issue and it is no longer necessary to protect the end-user from the power jack.

The above power cycling scenarios have assumed the PSE is using DC disconnect methods. For a PSE using AC disconnect, a PD with less than minimum load will continue to be powered.

Wall adapters have been known to generate voltage spikes outside their expected operating range. Care should be taken to ensure no damage occurs to the LTC4268-1 or any support circuitry from extraneous spikes at the auxiliary power interface.

Classification Resistor Selection (R_{CLASS})

The IEEE 802.3af specification allows classifying PDs into four distinct classes with class 4 being reserved for future use (Table 2). The LTC4268-1 supports all IEEE classes and implements an additional Class 5 for use in custom PoE applications. An external resistor connected from R_{CLASS} to V_{PORTN} (Figure 6) sets the value of the load current. The designer should determine which class the PD is to advertise and then select the appropriate value of R_{CLASS} from Table 2. If a unique load current is required, the value of R_{CLASS} can be calculated as:

$$R_{CLASS} = 1.237V/(I_{LOAD} – I_{IN\_CLASS})$$

I_{IN_CLASS} is the LTC4268-1 IC supply current during classification given in the electrical specifications. The R_{CLASS} resistor must be 1% or better to avoid degrading the overall accuracy of the classification circuit. Resistor power dissipation will be 100mW maximum and is transient so heating is typically not a concern. In order to maintain loop stability, the layout should minimize capacitance at the R_{CLASS} node. The classification circuit can be disabled by floating the R_{CLASS} pin. The R_{CLASS} pin should not be shorted to V_{PORTN} as this would force the LTC4268-1 classification circuit to attempt to source very large currents. In this case, the LTC4268-1 will quickly go into thermal shutdown.

APPLICATIONS INFORMATION

Power Good Interface

The LTC4268-1 provides complimentary power good signals to simplify the DC/DC converter interface. Using the power good signal to delay converter operation until the load capacitor is fully charged is recommended as this will help ensure trouble free start-up.

The active high PWRGD pin is controlled by an open collector transistor referenced to V_{NEG} while the active low $\overline{PWRGD}$ pin is controlled by a high voltage, open-drain MOSFET referenced to V_{PORTN}. The PWRGD pin is designed to interface directly to the UVLO pin with the aid of a pull-up resistor to Vcc. An example interface circuit is shown in Figure 11.

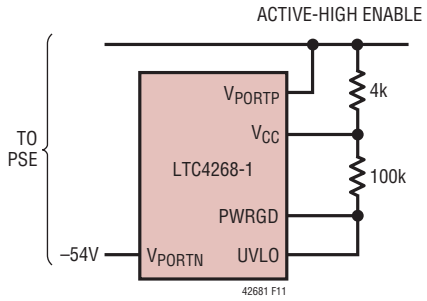


Figure 11. Power Good Interface Example

Port Voltage Lockout

PoE applications require the PD interface to turn on below 42V and turn off above 30V. The LTC4268-1 includes an internal port voltage lockout circuit to implement this basic chip on/off control. Additionally, the LTC4268-1 includes an enable/lockout function for the DC/DC converter that is controlled by the UVLO pin and is intended to be driven by PWRGD to ensure proper start-up. (Refer to Power Good Interface.) Users have the ability to implement higher turn-on voltages if necessary by connecting the UVLO pin to an external resistive divider between V_{PORTP} and V_{PORTN}. The UVLO pin also includes a bias current allowing implementation of hysteresis. When UVLO is below 1.24V, gate drivers are disabled and the converter sits idle. When the pin rises above the lockout threshold a small current is sourced out of the UVLO pin, increasing the pin voltage and thus creating hysteresis. As the pin voltage drops below this threshold, the current is disabled, further dropping the UVLO pin voltage. If not used, the UVLO pin can be disabled by tying to V_{CC}.

Shutdown Interface

To disable the 25k signature resistor, connect SHDN to the V_{PORTP} pin. Alternately, the SHDN pin can be driven high with respect to V_{PORTN}. Examples of interface circuits that disable the signature and all LTC4268-1 functions are shown in Figure 10, options 2 and 4. Note that the SHDN input resistance is relatively large and the threshold voltage is fairly low. Because of high voltages present on the printed circuit board, leakage currents from the V_{PORTP} pin could inadvertently pull SHDN high. To ensure trouble-free operation, use high voltage layout techniques in the vicinity of SHDN. If unused, connect SHDN directly to V_{PORTN}.

Load Capacitor

The IEEE 802.3af specification requires that the PD maintain a minimum load capacitance of 5µF. It is permissible to have a much larger load capacitor and the LTC4268-1 can charge very large load capacitors before thermal issues become a problem. However, the load capacitor must not be too large or the PD design may violate IEEE 802.3af requirements. If the load capacitor is too large, there can be a problem with inadvertent power shutdown by the PSE. For example, if the PSE is running at –57V (IEEE 802.3af maximum allowed) and the PD is detected and powered up, the load capacitor will be charged to nearly –57V. If for some reason the PSE voltage is suddenly reduced to –44V (IEEE 802.3af minimum allowed), the input bridge will reverse bias and the PD power will be supplied by the load capacitor. Depending on the size of the load capacitor and the DC load of the PD, the PD will not draw any power from the PSE for a period of time. If this period of time exceeds the IEEE 802.3af 300ms disconnect delay, the PSE will remove power from the PD. For this reason, it is necessary to evaluate the load current and capacitance to ensure that inadvertent shutdown cannot occur. Refer also to Thermal Protection in this data sheet for further discussion on load capacitor selection.

APPLICATIONS INFORMATION

MAINTAIN POWER SIGNATURE

In an IEEE 802.3af system, the PSE uses the maintain power signature (MPS) to determine if a PD continues to require power. The MPS requires the PD to periodically draw at least 10mA and also have an AC impedance less than 26.25k in parallel with 0.05µF. If either the DC current is less than 10mA or the AC impedance is above 26.25k, the PSE may disconnect power. The DC current must be less than 5mA and the AC impedance must be above 2M to guarantee power will be removed. The PD application circuits shown in this data sheet present the required AC impedance necessary to maintain power.

IEEE 802.3at Interoperability

In anticipation of the IEEE 802.3at standard release, the LTC4268-1 can be combined with a simple external circuit to be fully interoperable with an IEEE 802.3at-compliant PSE. For more information, please contact Linear Technology's Application Engineering.

SWITCHING REGULATOR OVERVIEW

The LTC4268-1 includes a current mode converter designed specifically for use in an isolated flyback topology employing synchronous rectification. The LTC4268-1 operation is similar to traditional current mode switchers. The major difference is that output voltage feedback is derived via sensing the output voltage through the transformer. This precludes the need of an opto-isolator in isolated designs greatly improving dynamic response and reliability. The LTC4268-1 has a unique feedback amplifier that samples a transformer winding voltage during the flyback period and uses that voltage to control output voltage. The internal blocks are similar to many current mode controllers. The differences lie in the feedback amplifier and load compensation circuitry. The logic block also contains circuitry to control the special dynamic requirements of flyback control. For more information on the basics of current mode switcher/controllers and isolated flyback converters see Application Note 19.

Feedback Amplifier—Pseudo DC Theory

For the following discussion refer to the simplified Flyback Amplifier diagram(Figure 12). When the primary side MOSFET switch MP turns off, its drain voltage rises above the V_{PORTP} rail. Flyback occurs when the primary MOSFET is off and the synchronous secondary MOSFET is on. During flyback the voltage on nondriven transformer pins is determined by the secondary voltage. The amplitude of this flyback pulse as seen on the third winding is given as:

$$V_{FLBK} = \frac{V_{OUT} + I_{SEC} \bullet \left(ESR + R_{DS(ON)}\right)}{N_{SF}}$$

$R_{DS(ON)}$ = on resistance of the synchronous MOSFET MS

I_{SEC} = transformer secondary current

ESR = impedance of secondary circuit capacitor, winding and traces

N_{SF} = transformer effective secondary-to-flyback winding turns ratio (i.e., N_S/N_{FLBK})

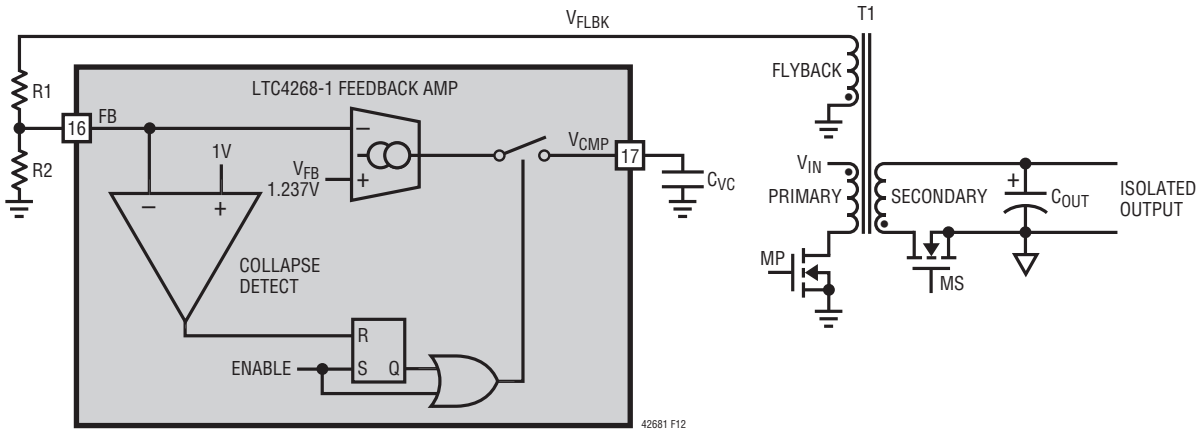


Figure 12. LTC4268-1 Switching Regulator Feedback Amplifier

APPLICATIONS INFORMATION

The flyback voltage is scaled by an external resistive divider R1/R2 and presented at the FB pin. The feedback amplifier compares the voltage to the internal bandgap reference. The feedback amp is actually a transconductance amplifier whose output is connected to V_{CMP} only during a period in the flyback time. An external capacitor on the V_{CMP} pin integrates the net feedback amp current to provide the control voltage to set the current mode trip point. The regulation voltage at the FB pin is nearly equal to the bandgap reference V_{FB} because of the high gain in the overall loop. The relationship between V_{FLBK} and V_{FB} is expressed as:

$$V_{FLBK} = \frac{R1+R2}{R2} \bullet V_{FB}$$

Combining this with the previous V_{FLBK} expression yields an expression for V_{OUT} in terms of the internal reference, programming resistors and secondary resistances:

$$V_{OUT} = \left(\frac{R1+R2}{R2} \bullet V_{FB} \bullet N_{SF} \right) - I_{SEC} \bullet \left(ESR + R_{DS(ON)} \right)$$

The effect of nonzero secondary output impedance is discussed in further detail; see Load Compensation Theory. The practical aspects of applying this equation for V_{OUT} are found in the Applications Information.

Feedback Amplifier Dynamic Theory

So far, this has been a pseudo-DC treatment of flyback feedback amplifier operation. But the flyback signal is a pulse, not a DC level. Provision is made to turn on the flyback amplifier only when the flyback pulse is present using the enable signal as shown in the timing diagram (Figure 13).

Minimum Output Switch On Time ($t_{ON(MIN)}$)

The LTC4268-1 affects output voltage regulation via flyback pulse action. If the output switch is not turned on, there is no flyback pulse and output voltage information is not available. This causes irregular loop response and start-up/latch-up problems. The solution is to require the primary switch to be on for an absolute minimum time per each oscillator cycle. To accomplish this the current limit feedback is blanked each cycle for $t_{ON(MIN)}$. If the output load is less than that developed under these conditions, forced continuous operation normally occurs. See Applications Information for further details.

Enable Delay Time (ENDLY)

The flyback pulse appears when the primary side switch shuts off. However, it takes a finite time until the transformer primary side voltage waveform represents the output voltage. This is partly due to rise time on the primary

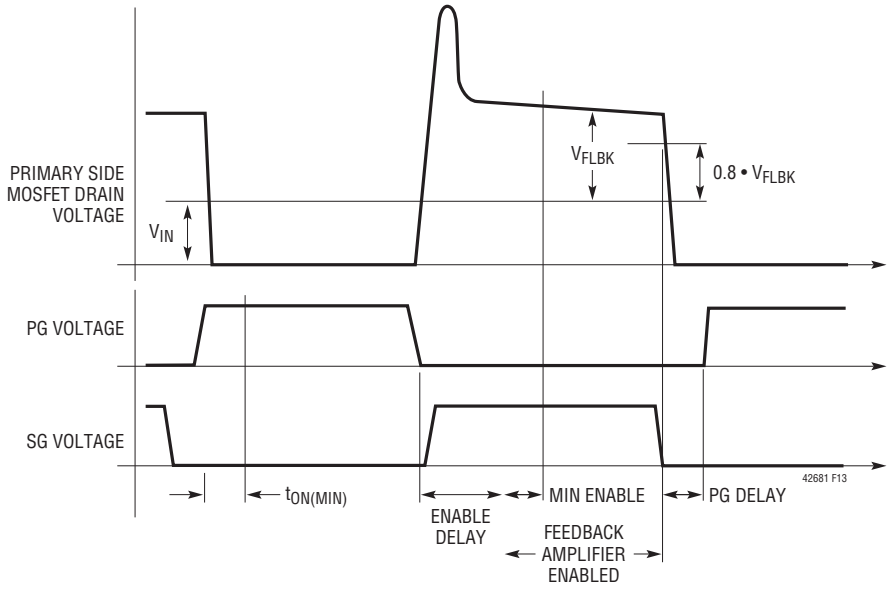


Figure 13. LTC4268-1 Switching Regulator Timing Diagram

APPLICATIONS INFORMATION

side MOSFET drain node but, more importantly, is due to transformer leakage inductance. The latter causes a voltage spike on the primary side, not directly related to output voltage. Some time is also required for internal settling of the feedback amplifier circuitry. In order to maintain immunity to these phenomena, a fixed delay is introduced between the switch turn-off command and the enabling of the feedback amplifier. This is termed "enable delay." In certain cases where the leakage spike is not sufficiently settled by the end of the enable delay period, regulation error may result. See Applications Information for further details.

Collapse Detect

Once the feedback amplifier is enabled, some mechanism is then required to disable it. This is accomplished by a collapse detect comparator, which compares the flyback voltage (FB) to a fixed reference, nominally 80% of V_{FB}. When the flyback waveform drops below this level, the feedback amplifier is disabled.

Minimum Enable Time

The feedback amplifier, once enabled, stays on for a fixed minimum time period termed "minimum enable time." This prevents lockup, especially when the output voltage is abnormally low; e.g., during start-up. The minimum enable time period ensures that the V_{CMP} node is able to "pump up" and increase the current mode trip point to the level where the collapse detect system exhibits proper operation. This time is set internally.

Effects of Variable Enable Period

The feedback amplifier is enabled during only a portion of the cycle time. This can vary from the fixed minimum enable time described to a maximum of roughly the "off" switch time minus the enable delay time. Certain parameters of feedback amp behavior are directly affected by the variable enable period. These include effective transconductance and V_{CMP} node slew rate.

Load Compensation Theory

The LTC4268-1 uses the flyback pulse to obtain information about the isolated output voltage. An error source is caused by transformer secondary current flow through the synchronous MOSFET $R_{DS(ON)}$ and real life nonzero impedances of the transformer secondary and output capacitor. This was represented previously by the expression "I_{SEC} • (ESR + $R_{DS(ON)}$)." However, it is generally more useful to convert this expression to effective output impedance. Because the secondary current only flows during the off portion of the duty cycle (DC), the effective output impedance equals the lumped secondary impedance divided by off time DC.

Since the off time duty cycle is equal to 1 – DC then:

$$R_{S(OUT)} = \frac{ESR + R_{DS(ON)}}{1 - DC}$$

where:

$R_{S(OUT)}$ = effective supply output impedance

DC = duty cycle

$R_{DS(ON)}$ and ESR are as defined previously

This impedance error may be judged acceptable in less critical applications, or if the output load current remains relatively constant. In these cases the external FB resistive divider is adjusted to compensate for nominal expected error. In more demanding applications, output impedance error is minimized by the use of the load compensation function. Figure 14 shows the block diagram of the load compensation function. Switch current is converted to a voltage by the external sense resistor, averaged and

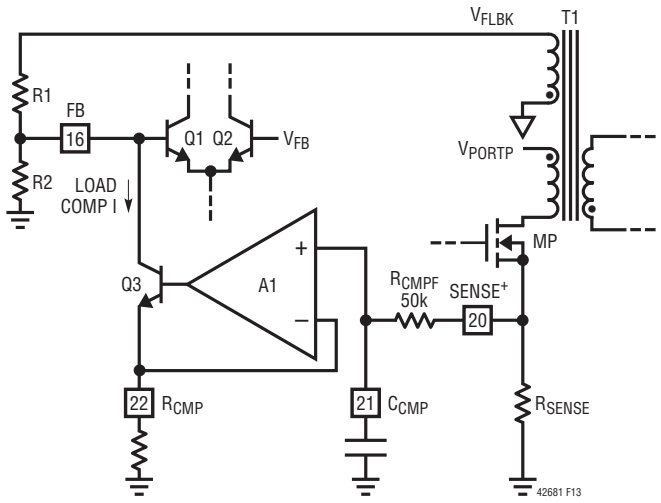


Figure 14. Load Compensation Diagram

APPLICATIONS INFORMATION

lowpass filtered by the internal 50k resistor R_{CMPF} and the external capacitor on C_{CMP}. This voltage is impressed across the external R_{CMP} resistor by op amp A1 and transistor Q3 producing a current at the collector of Q3 that is subtracted from the FB node. This effectively increases the voltage required at the top of the R1/R2 feedback divider to achieve equilibrium.

The average primary side switch current increases to maintain output voltage regulation as output loading increases. The increase in average current increases R_{CMP} resistor current which affects a corresponding increase in sensed output voltage, compensating for the IR drops. Assuming relatively fixed power supply efficiency, Eff, power balance gives:

$$P_{OUT} = Eff \bullet P_{IN}$$

$$V_{OUT} \bullet I_{OUT} = Eff \bullet V_{IN} \bullet I_{IN}$$

Average primary side current is expressed in terms of output current as follow:

$$I_{IN} = K1 \bullet I_{OUT}$$

where:

$$K1 = \frac{V_{OUT}}{V_{IN} \bullet Eff}$$

So the effective change in V_{OUT} target is:

$$\Delta V_{OUT} = K1 \bullet \frac{R_{SENSE}}{R_{CMP}} \bullet R1 \bullet N_{SF}$$

thus:

$$\frac{\Delta V_{OUT}}{\Delta I_{OUT}} = K1 \bullet \frac{R_{SENSE}}{R_{CMP}} \bullet R1 \bullet N_{SF}$$

where:

K1 = dimensionless variable related to V_{IN}, V_{OUT} and efficiency as explained above

R_{SENSE} = external sense resistor

Nominal output impedance cancellation is obtained by equating this expression with $R_{S(OUT)}$:

$$K1 \bullet \frac{R_{SENSE}}{R_{CMP}} \bullet R1 \bullet N_{SF} = \frac{ESR + R_{DS(ON)}}{1 - DC}$$

Solving for R_{CMP} gives:

$$R_{CMP} = K1 \bullet \frac{R_{SENSE} \bullet (1 - DC)}{ESR + R_{DS(ON)}} \bullet R1 \bullet N_{SF}$$

The practical aspects of applying this equation to determine an appropriate value for the R_{CMP} resistor are found in the Applications Information.

Transformer Design

Transformer design/specification is the most critical part of a successful application of the LTC4268-1. The following sections provide basic information about designing the transformer and potential trade-offs. If you need help, the LTC Applications group is available to assist in the choice and/or design of the transformer.

Turns Ratios

The design of the transformer starts with determining duty cycle (DC). DC impacts the current and voltage stress on the power switches, input and output capacitor RMS currents and transformer utilization (size vs power). The ideal turns ratio is:

$$N_{DEAL} = \frac{V_{OUT}}{V_{IN}} \bullet \frac{1 - DC}{DC}$$

Avoid extreme duty cycles as they, in general, increase current stresses. A reasonable target for duty cycle is 50% at nominal input voltage.

For instance, if we wanted a 48V to 5V converter at 50% DC then:

$$N_{DEAL} = \frac{5}{48} \bullet \frac{1 - 0.5}{0.5} = \frac{1}{9.6}$$

APPLICATIONS INFORMATION

In general, better performance is obtained with a lower turns ratio. A DC of 45.5% yields a 1:8 ratio. Note the use of the external feedback resistive divider ratio to set output voltage provides the user additional freedom in selecting a suitable transformer turns ratio. Turns ratios that are the simple ratios of small integers; e.g., 1:1, 2:1, 3:2 help facilitate transformer construction and improve performance. When building a supply with multiple outputs derived through a multiple winding transformer, lower duty cycle can improve cross regulation by keeping the synchronous rectifier on longer, and thus, keep secondary windings coupled longer. For a multiple output transformer, the turns ratio between output windings is critical and affects the accuracy of the voltages. The ratio between two output voltages is set with the formula $V_{OUT2} = V_{OUT1} \bullet N21$ where N21 is the turns ratio between the two windings. Also keep the secondary MOSFET $R_{DS(ON)}$ small to improve cross regulation. The feedback winding usually provides both the feedback voltage and power for the LTC4268-1. Set the turns ratio between the output and feedback winding to provide a rectified voltage that under worst-case conditions is greater than the 11V maximum V_{CC} turn-off voltage.

$$N_{SF} > \frac{V_{OUT}}{11 + V_F}$$

where:

V_F = Diode Forward Voltage

For our example: $N_{SF} > \frac{5}{11 + 0.7} = \frac{1}{2.34}$

We will choose $\frac{1}{3}$

Leakage Inductance

Transformer leakage inductance (on either the primary or secondary) causes a spike after the primary side switch turn-off. This is increasingly prominent at higher load currents, where more stored energy is dissipated. Higher flyback voltage may break down the MOSFET switch if it has too low a BV_{DSS} rating. One solution to reducing this spike is to use a snubber circuit to suppress the voltage excursion. However, suppressing the voltage extends the flyback pulse width. If the flyback pulse extends beyond the enable delay time, output voltage regulation is affected. The feedback system has a deliberately limited input range, roughly ±50mV referred to the FB node. This rejects higher voltage leakage spikes because once a leakage spike is several volts in amplitude; a further increase in amplitude has little effect on the feedback system. Therefore, it is advisable to arrange the snubber circuit to clamp at as high a voltage as possible, observing MOSFET breakdown, such that leakage spike duration is as short as possible. Application Note 19 provides a good reference on snubber design.

As a rough guide, leakage inductance of several percent (of mutual inductance) or less may require a snubber, but exhibit little to no regulation error due to leakage spike behavior. Inductances from several percent up to perhaps ten percent cause increasing regulation error.

Avoid double digit percentage leakage inductances. There is a potential for abrupt loss of control at high load current. This curious condition potentially occurs when the leakage spike becomes such a large portion of the flyback waveform that the processing circuitry is fooled into thinking that the leakage spike itself is the real flyback signal! It then reverts to a potentially stable state whereby the top of the leakage spike is the control point, and the trailing edge of the leakage spike triggers the collapse detect circuitry. This typically reduces the output voltage abruptly to a fraction, roughly one-third to two-thirds of its correct value. Once load current is reduced sufficiently, the system snaps back to normal operation. When using transformers with considerable leakage inductance, exercise this worst-case check for potential bistability:

1. Operate the prototype supply at maximum expected load current.
2. Temporarily short-circuit the output.
3. Observe that normal operation is restored.

If the output voltage is found to hang up at an abnormally low value, the system has a problem. This is usually evident by simultaneously viewing the primary side MOSFET drain voltage to observe firsthand the leakage spike behavior.

A final note—the susceptibility of the system to bistable behavior is somewhat a function of the load current/voltage characteristics. A load with resistive—i.e., I = V/R

APPLICATIONS INFORMATION

behavior—is the most apt to be bistable. Capacitive loads that exhibit $I = V^2/R$ behavior are less susceptible.

Secondary Leakage Inductance

Leakage inductance on the secondary forms an inductive divider on the transformer secondary, reducing the size of the flyback pulse. This increases the output voltage target by a similar percentage. Note that unlike leakage spike behavior; this phenomenon is independent of load. Since the secondary leakage inductance is a constant percentage of mutual inductance (within manufacturing variations), the solution is to adjust the feedback resistive divider ratio to compensate.

Winding Resistance Effects

Primary or secondary winding resistance acts to reduce overall efficiency (P_{OUT}/P_{IN}). Secondary winding resistance increases effective output impedance, degrading load regulation. Load compensation can mitigate this to some extent but a good design keeps parasitic resistances low.

Bifilar Winding

A bifilar or similar winding is a good way to minimize troublesome leakage inductances. Bifilar windings also improve coupling coefficients and thus improve cross regulation in multiple winding transformers. However, tight coupling usually increases primary-to-secondary capacitance and limits the primary-to-secondary breakdown voltage, so it isn't always practical.

Primary Inductance

The transformer primary inductance, L_P, is selected based on the peak-to-peak ripple current ratio (X) in the transformer relative to its maximum value.

As a general rule, keep X in the range of 20% to 40% (i.e., X = 0.2 to 0.4). Higher values of ripple will increase conduction losses, while lower values will require larger cores.

Ripple current and percentage ripple is largest at minimum duty cycle; in other words, at the highest input voltage. L_P is calculated from:

$$L_P = \frac{\left(V_{IN(MAX)} \bullet DC_{MIN}\right)^2}{f_{OSC} \bullet X_{MAX} \bullet P_{IN}} = \frac{\left(V_{IN(MAX)} \bullet DC_{MIN}\right)^2 \bullet Eff}{f_{OSC} \bullet X_{MAX} \bullet P_{OUT}}$$

where:

f_{OSC} is the oscillator frequency

DC_{MIN} is the DC at maximum input voltage

X_{MAX} is ripple current ratio at maximum input voltage

Using common high power PoE values a 48V (41V < V_{IN} < 57V) to 5V/5.3A Converter with 90% efficiency, P_{OUT}= 26.5W and P_{IN} = 29.5W Using X = 0.4 N = 1/8 and f_{OSC} = 200kHz:

$$DC_{MIN} = \frac{1}{1 + \frac{N \bullet V_{IN(MAX)}}{V_{OUT}}} = \frac{1}{1 + \frac{1}{8} \bullet \frac{57}{5}} = 41.2\%$$

$$L_P = \frac{(57V \bullet 0.412)^2}{200kHz \bullet 0.4 \bullet 26.5W} = 260\mu H$$

Optimization might show that a more efficient solution is obtained at higher peak current but lower inductance and the associated winding series resistance. A simple spreadsheet program is useful for looking at trade-offs.

APPLICATIONS INFORMATION

Transformer Core Selection

Once L_P is known, the type of transformer is selected. High efficiency converters use ferrite cores to minimize core loss. Actual core loss is independent of core size for a fixed inductance, but decreases as inductance increases. Since increased inductance is accomplished through more turns of wire, copper losses increase. Thus transformer design balances core and copper losses. Remember that increased winding resistance will degrade cross regulation and increase the amount of load compensation required.

The main design goals for core selection are reducing copper losses and preventing saturation. Ferrite core material saturates hard, rapidly reducing inductance when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and, consequently, output voltage ripple. Do not allow the core to saturate! The maximum peak primary current occurs at minimum V_{IN}:

$$I_{PK} = \frac{P_{IN}}{V_{IN(MIN)} \bullet DC_{MAX}} \bullet \left(1 + \frac{X_{MIN}}{2}\right)$$

now:

$$DC_{MAX} = \frac{1}{1 + \frac{N \bullet V_{IN(MIN)}}{V_{OUT}}} = \frac{1}{1 + \frac{1}{8} \bullet \frac{41}{5}} = 49.4\%$$

$$X_{MIN} = \frac{\left(V_{IN(MIN)} \bullet DC_{MAX}\right)^2}{f_{OSC} \bullet L_P \bullet P_{IN}} = \frac{(41 \bullet 49.4\%)^2}{200kHz \bullet 260\mu H \bullet 29.5W} = 0.267$$

Using the example numbers leads to:

$$I_{PK} = \frac{29.5W}{41 \bullet 0.494} \bullet \left(1 + \frac{0.267}{2}\right) = 1.65A$$

Multiple Outputs

One advantage that the flyback topology offers is that additional output voltages can be obtained simply by adding windings. Designing a transformer for such a situation is beyond the scope of this document. For multiple windings, realize that the flyback winding signal is a combination of activity on all the secondary windings. Thus load regulation is affected by each winding's load. Take care to minimize cross regulation effects.

Setting Feedback Resistive Divider

The expression for V_{OUT} developed in the Operation section is rearranged to yield the following expression for the feedback resistors:

$$R1 = R2\left(\frac{\left[V_{OUT} + I_{SEC} \bullet \left(ESR + R_{DS(ON)}\right)\right]}{V_{FB} \bullet N_{SF}} - 1\right)$$

Continuing the example, if ESR + $R_{DS(ON)}$ = 8mΩ, R2 = 3.32k, then:

$$R1 = 3.32k\left(\frac{5 + 5.3 \bullet 0.008}{1.237 \bullet 1/3} - 1\right) = 37.28k$$

choose 37.4k.

It is recommended that the Thevenin impedance of the resistive divider (R1||R2) is roughly 3k for bias current cancellation and other reasons.

Current Sense Resistor Considerations

The external current sense resistor is used to control peak primary switch current, which controls a number of key converter characteristics including maximum power and external component ratings. Use a noninductive current sense resistor (no wire-wound resistors). Mounting the resistor directly above an unbroken ground plane connected with wide and short traces keeps stray resistance and inductance low.

The dual sense pins allow for a full Kelvin connection. Make sure that SENSE+ and SENSE– are isolated and connect close to the sense resistor.

Peak current occurs at 100mV of sense voltage V_{SENSE}. So the nominal sense resistor is V_{SENSE}/I_{PK}. For example, a peak switch current of 10A requires a nominal sense resistor of 0.010Ω Note that the instantaneous peak power in the sense resistor is 1W, and that it is rated accordingly. The use of parallel resistors can help achieve low resistance, low parasitic inductance and increased power capability.

APPLICATIONS INFORMATION

Size R_{SENSE} using worst-case conditions, minimum L_P, V_{SENSE} and maximum V_{IN}. Continuing the example, let us assume that our worst-case conditions yield an I_{PK} of 40% above nominal so I_{PK} = 2.3A. If there is a 10% tolerance on R_{SENSE} and minimum V_{SENSE} = 88mV, then R_{SENSE} • 110% = 88mV/2.3A and nominal R_{SENSE} = 35mΩ. Round to the nearest available lower value, 33mΩ.

Selecting the Load Compensation Resistor

The expression for R_{CMP} was derived in the Operation section as:

$$R_{CMP} = K1 \bullet \frac{R_{SENSE} \bullet (1-DC)}{ESR + R_{DS(ON)}} \bullet R1 \bullet N_{SF}$$

Continuing the example:

$$K1 = \left(\frac{V_{OUT}}{V_{IN} \bullet Eff} \right) = \frac{5}{48 \bullet 90\%} = 0.116$$

$$DC = \frac{1}{1 + \frac{N \bullet V_{IN(NOM)}}{V_{OUT}}} = \frac{1}{1 + \frac{1}{8} \bullet \frac{48}{5}} = 45.5\%$$

If $ESR + R_{DS(ON)} = 8m\Omega$

$$R_{CMP} = 0.116 \bullet \frac{33m\Omega \bullet (1-0.455)}{8m\Omega} \bullet 37.4k\Omega \bullet \frac{1}{3}$$

$$= 3.25k$$

This value for R_{CMP} is a good starting point, but empirical methods are required for producing the best results. This is because several of the required input variables are difficult to estimate precisely. For instance, the ESR term above includes that of the transformer secondary, but its effective ESR value depends on high frequency behavior, not simply DC winding resistance. Similarly, K1 appears as a simple ratio of V_{IN} to V_{OUT} times efficiency, but theoretically estimating efficiency is not a simple calculation.

The suggested empirical method is as follows:

1. Build a prototype of the desired supply including the actual secondary components.
2. Temporarily ground the C_{CMP} pin to disable the load compensation function. Measure output voltage while sweeping output current over the expected range. Approximate the voltage variation as a straight line.

   $\Delta V_{OUT}/\Delta I_{OUT} = R_{S(OUT)}$.
3. Calculate a value for the K1 constant based on V_{IN}, V_{OUT} and the measured efficiency.
4. Compute:

$$R_{CMP} = K1 \bullet \frac{R_{SENSE}}{R_{S(OUT)}} \bullet R1 \bullet N_{SF}$$

5. Verify this result by connecting a resistor of this value from the R_{CMP} pin to ground.
6. Disconnect the ground short to C_{CMP} and connect a 0.1µF filter capacitor to ground. Measure the output impedance $R_{S(OUT)} = \Delta V_{OUT}/\Delta I_{OUT}$ with the new compensation in place. $R_{S(OUT)}$ should have decreased significantly. Fine tuning is accomplished experimentally by slightly altering R_{CMP}. A revised estimate for R_{CMP} is:

$$R'_{CMP} = R_{CMP} \bullet \left(1 + \frac{R_{S(OUT)CMP}}{R_{S(OUT)}} \right)$$

   where R'_{CMP} is the new value for the load compensation resistor. $R_{S(OUT)CMP}$ is the output impedance with R_{CMP} in place and $R_{S(OUT)}$ is the output impedance with no load compensation (from step 2).

APPLICATIONS INFORMATION

Setting Frequency

The switching frequency of the LTC4268-1 is set by an external capacitor connected between the OSC pin and ground. Recommended values are between 200pF and 33pF, yielding switching frequencies between 50kHz and 250kHz. Figure 15shows the nominal relationship between external capacitance and switching frequency. Place the capacitor as close as possible to the IC and minimize OSC trace length and area to minimize stray capacitance and potential noise pickup.

You can synchronize the oscillator frequency to an external frequency. This is done with a signal on the SYNC pin. Set the LTC4268-1 frequency 10% slower than the desired external frequency using the OSC pin capacitor, then use a pulse on the SYNC pin of amplitude greater than 2V and with the desired frequency. The rising edge of the SYNC signal initiates an OSC capacitor discharge forcing primary MOSFET off (PG voltage goes low). If the oscillator frequency is much different from the sync frequency, problems may occur with slope compensation and system stability. Keep the sync pulse width greater than 500ns.

Selecting Timing Resistors

There are three internal "one-shot" times that are programmed by external application resistors: minimum on time, enable delay time and primary MOSFET turn-on delay. These are all part of the isolated flyback control technique, and their functions are previously outlined in the Theory of Operation section. The following information should help in selecting and/or optimizing these timing values.

Minimum Output Switch On Time ($t_{ON(MIN)}$)

Minimum on time is the programmable period during which current limit is blanked (ignored) after the turn on of the primary side switch. This improves regulator performance by eliminating false tripping on the leading edge spike in the switch, especially at light loads. This spike is due to both the gate/source charging current and the discharge of drain capacitance. The isolated flyback sensing requires a pulse to sense the output. Minimum on time ensures that the output switch is always on a minimum time and that there is always a signal to close the loop. The LTC4268-1 does not employ cycle skipping at light loads. Therefore,

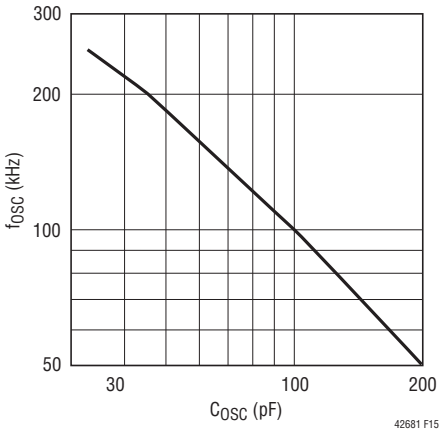


Figure 15. f_{OSC} vs OSC Capacitor Values

APPLICATIONS INFORMATION

minimum on time along with synchronous rectification sets the switch over to forced continuous mode operation.

The $t_{ON(MIN)}$ resistor is set with the following equation

$$R_{tON(MIN)}\,(k\Omega) = \frac{t_{ON(MIN)}\,(ns) - 104}{1.063}$$

Keep $R_{tON(MIN)}$ greater than 70k. A good starting value is 160k.

Enable Delay Time (ENDLY)

Enable delay time provides a programmable delay between turn-off of the primary gate drive node and the subsequent enabling of the feedback amplifier. As discussed earlier, this delay allows the feedback amplifier to ignore the leakage inductance voltage spike on the primary side. The worst-case leakage spike pulse width is at maximum load conditions. So set the enable delay time at these conditions.

While the typical applications for this part use forced continuous operation, it is conceivable that a secondary side controller might cause discontinuous operation at light loads. Under such conditions the amount of energy stored in the transformer is small. The flyback waveform becomes "lazy" and some time elapses before it indicates the actual secondary output voltage. The enable delay time should be made long enough to ignore the "irrelevant" portion of the flyback waveform at light loads.

Even though the LTC4268-1 has a robust gate drive, the gate transition time slows with very large MOSFETs. Increase delay time as required when using such MOSFETs.

The enable delay resistor is set with the following equation:

$$R_{ENDLY}\,(k\Omega) = \frac{t_{ENDLY}\,(ns) - 30}{2.616}$$

Keep R_{ENDLY} greater than 40k. A good starting point is 56k.

Primary Gate Delay Time (PGDLY)

Primary gate delay is the programmable time from the turn-off of the synchronous MOSFET to the turn-on of the primary side MOSFET. Correct setting eliminates overlap between the primary side switch and secondary side synchronous switch(es) and the subsequent current spike in the transformer. This spike will cause additional component stress and a loss in regulator efficiency.

The primary gate delay resistor is set with the following equation:

$$R_{PGDLY}\,(k\Omega) = \frac{t_{PGDLY}\,(ns) + 47}{9.01}$$

A good starting point is 27k.

Soft-Start Function

The LTC4268-1 contains an optional soft-start function that is enabled by connecting an external capacitor between the SFST pin and ground. Internal circuitry prevents the control voltage at the V_{CMP} pin from exceeding that on the SFST pin. There is an initial pull-up circuit to quickly bring the SFST voltage to approximately 0.8V. From there it charges to approximately 2.8V with a 20µA current source.

The SFST node is discharged to 0.8V when a fault occurs. A fault occurs when V_{CC} is too low (undervoltage lockout), current sense voltage is greater than 200mV or the IC's thermal (over temperature) shutdown is tripped. When SFST discharges, the V_{CMP} node voltage is also pulled low to below the minimum current voltage. Once discharged and the fault removed, the SFST charges up again. In this manner, switch currents are reduced and the stresses in the converter are reduced during fault conditions.

The time it takes to fully charge soft-start is:

$$t_{ss} = \frac{C_{SFST} \bullet 1.4V}{20\mu A} = 70k\Omega \bullet C_{SFST}\,(\mu F)$$

APPLICATIONS INFORMATION

Converter Start-Up

The standard topology for the LTC4268-1 utilizes a third transformer winding on the primary side that provides both feedback information and local V_{CC} power for the LTC4268-1 (see Figure 16). This power "bootstrapping" improves converter efficiency but is not inherently self-starting. Start-up is affected with an external "trickle charge" resistor and the LTC4268-1's internal V_{CC} undervoltage lockout circuit. The V_{CC} undervoltage lockout has wide hysteresis to facilitate start-up.

In operation, the "trickle charge" resistor R_{TR} is connected to V_{IN} and supplies a small current, typically on the order of 1mA to charge C_{TR}. Initially the LTC4268-1 is off and draws only its start-up current. When C_{TR} reaches the V_{CC} turn-on threshold voltage the LTC4268-1 turns on abruptly and draws its normal supply current.

Switching action commences and the converter begins to deliver power to the output. Initially the output voltage is low and the flyback voltage is also low, so C_{TR} supplies most of the LTC4268-1 current (only a fraction comes from R_{TR}.) V_{CC} voltage continues to drop until after some time, typically tens of milliseconds, the output voltage approaches its desired value. The flyback winding then provides the LTC4268-1 supply current and the V_{CC} voltage stabilizes.

If C_{TR} is undersized, V_{CC} reaches the V_{CC} turn-off threshold before stabilization and the LTC4268-1 turns off. The V_{CC} node then begins to charge back up via R_{TR} to the turn-on threshold, where the part again turns on. Depending upon the circuit, this may result in either several on-off cycles before proper operation is reached, or permanent relaxation oscillation at the V_{CC} node.

R_{TR} is selected to yield a worst-case minimum charging current greater than the maximum rated LTC4268-1 start-up current, and a worst-case maximum charging current less than the minimum rated LTC4268-1 supply current.

$$R_{TR(MAX)} < \frac{V_{IN(MIN)} - V_{CC(ON\_MAX)}}{I_{CC(ST\_MAX)}}$$

and

$$R_{TR(MIN)} > \frac{V_{IN(MAX)} - V_{CC(ON\_MIN)}}{I_{CC(MIN)}}$$

Make C_{TR} large enough to avoid the relaxation oscillatory behavior described above. This is complicated to determine theoretically as it depends on the particulars of the secondary circuit and load behavior. Empirical testing is recommended. Note that the use of the optional soft-start function lengthens the power-up timing and requires a correspondingly larger value for C_{TR}.

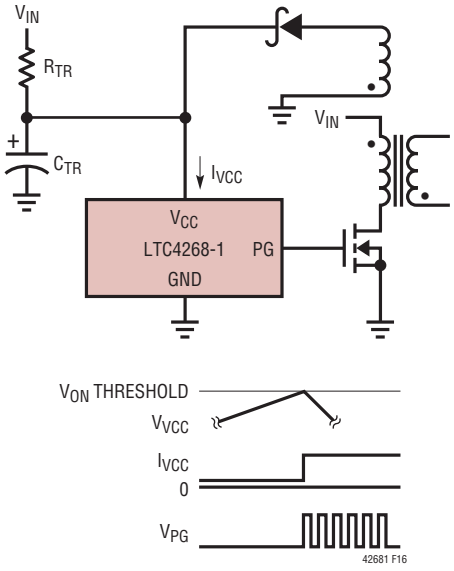


Figure 16. Typical Power Bootstrapping

APPLICATIONS INFORMATION

The LTC4268-1 has an internal clamp on V_{CC} of approximately 20V. This provides some protection for the part in the event that the switcher is off (UVLO low) and the V_{CC} node is pulled high. If R_{TR} is sized correctly the part should never attain this clamp voltage.

Control Loop Compensation

Loop frequency compensation is performed by connecting a capacitor network from the output of the feedback amplifier (V_{CMP} pin) to ground as shown in Figure 17. Because of the sampling behavior of the feedback amplifier, compensation is different from traditional current mode controllers. Normally only C_{VCMP} is required. R_{VCMP} can be used to add a "zero" but the phase margin improvement traditionally offered by this extra resistor is usually already accomplished by the nonzero secondary circuit impedance. C_{VCMP2} can be used to add an additional high frequency pole and is usually sized at 0.1 times C_{VCMP}.

In further contrast to traditional current mode switchers, V_{CMP} pin ripple is generally not an issue with the LTC4268-1. The dynamic nature of the clamped feedback amplifier forms an effective track/hold type response, whereby the V_{CMP} voltage changes during the flyback pulse, but is then "held" during the subsequent "switch on" portion of the next cycle. This action naturally holds the V_{CMP} voltage stable during the current comparator sense action (current mode switching).

Application Note 19 provides a method for empirically tweaking frequency compensation. Basically it involves introducing a load current step and monitoring the response.

Slope Compensation

The LTC4268-1 incorporates current slope compensation. Slope compensation is required to ensure current loop stability when the DC is greater than 50%. In some switching regulators, slope compensation reduces the maximum peak current at higher duty cycles. The LTC4268-1 eliminates this problem by having circuitry that compensates for the slope compensation so that maximum current sense voltage is constant across all duty cycles.

Minimum Load Considerations

At light loads, the LTC4268-1 derived regulator goes into forced continuous conduction mode. The primary side switch always turns on for a short time as set by the $t_{ON(MIN)}$ resistor. If this produces more power than the load requires, power will flow back into the primary during the "off" period when the synchronization switch is on. This does not produce any inherently adverse problems, although light load efficiency is reduced.

Maximum Load Considerations

The current mode control uses the V_{CMP} node voltage and amplified sense resistor voltage as inputs to the current comparator. When the amplified sense voltage exceeds the V_{CMP} node voltage, the primary side switch is turned off.

In normal use, the peak switch current increases while FB is below the internal reference. This continues until V_{CMP} reaches its 2.56V clamp. At clamp, the primary side MOSFET will turn off at the rated 100mV V_{SENSE} level. This repeats on the next cycle. It is possible for the peak primary switch currents as referred across R_{SENSE} to exceed the

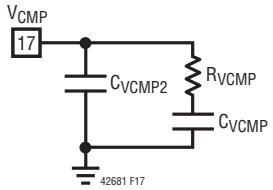


Figure 17. V_{CMP} Compensation Network

APPLICATIONS INFORMATION

max 100mV rating because of the minimum switch on time blanking. If the voltage on V_{SENSE} exceeds 205mV after the minimum turn-on time, the SFST capacitor is discharged, causing the discharge of the V_{CMP} capacitor. This then reduces the peak current on the next cycle and will reduce overall stress in the primary switch.

Short-Circuit Conditions

Loss of current limit is possible under certain conditions such as an output short circuit. If the duty cycle exhibited by the minimum on time is greater than the ratio of secondary winding voltage (referred-to-primary) divided by input voltage, then peak current is not controlled at the nominal value. It ratchets up cycle-by-cycle to some higher level. Expressed mathematically, the requirement to maintain short-circuit control is

$$DC_{MIN} = t_{ON(MIN)} \bullet f_{OSC} < \frac{I_{SC} \bullet \left(R_{SEC} + R_{DS(ON)}\right)}{V_{IN} \bullet N_{SP}}$$

where:

$t_{ON(MIN)}$ is the primary side switch minimum on-time

I_{SC} is the short-circuit output current

N_{SP} is the secondary-to-primary turns ratio (N_{SEC}/N_{PRI}) (Other variables as previously defined)

Trouble is typically encountered only in applications with a relatively high product of input voltage times secondary to primary turns ratio and/or a relatively long minimum switch on time. Additionally, several real world effects such as transformer leakage inductance, AC winding losses, and output switch voltage drop combine to make this simple theoretical calculation a conservative estimate. Prudent design evaluates the switcher for short-circuit protection and adds any additional circuitry to prevent destruction for these losses.

Output Voltage Error Sources

The LTC4268-1's feedback sensing introduces additional minor sources of errors. The following is a summary list.

- The internal bandgap voltage reference sets the reference voltage for the feedback amplifier. The specifications detail its variation.
- The external feedback resistive divider ratio directly affects regulated voltage. Use 1% components.
- Leakage inductance on the transformer secondary reduces the effective secondary-to-feedback winding turns ratio (NS/NF) from its ideal value. This increases the output voltage target by a similar percentage. Since secondary leakage inductance is constant from part to part (within a tolerance) adjust the feedback resistor ratio to compensate.
- The transformer secondary current flows through the impedances of the winding resistance, synchronous MOSFET $R_{DS(ON)}$ and output capacitor ESR. The DC equivalent current for these errors is higher than the load current because conduction occurs only during the converter's "off" time. So divide the load current by (1 – DC).

If the output load current is relatively constant, the feedback resistive divider is used to compensate for these losses. Otherwise, use the LTC4268-1 load compensation circuitry. (See Load Compensation.) If multiple output windings are used, the flyback winding will have a signal that represents an amalgamation of all these windings impedances. Take care that you examine worst-case loading conditions when tweaking the voltages.

APPLICATIONS INFORMATION

Power MOSFET Selection

The power MOSFETs are selected primarily on the criteria of "on" resistance $R_{DS(ON)}$, input capacitance, drain-to-source breakdown voltage (BV_{DSS}), maximum gate voltage (V_{GS}) and maximum drain current ($ID_{(MAX)}$).

For the primary-side power MOSFET, the peak current is:

$$I_{PK(PRI)} = \frac{P_{IN}}{V_{IN(MIN)} \bullet DC_{MAX}} \bullet \left(1 + \frac{X_{MIN}}{2}\right)$$

where X_{MIN} is peak-to-peak current ratio as defined earlier. For each secondary-side power MOSFET, the peak current is:

$$I_{PK(SEC)} = \frac{I_{OUT}}{1 - DC_{MAX}} \bullet \left(1 + \frac{X_{MIN}}{2}\right)$$

Select a primary-side power MOSFET with a BV_{DSS} greater than:

$$BV_{DSS} \geq I_{PK} \sqrt{\frac{L_{LKG}}{C_P}} + V_{IN(MAX)} + \frac{V_{OUT(MAX)}}{N_{SP}}$$

where N_{SP} reflects the turns ratio of that secondary-to primary winding. L_{LKG} is the primary-side leakage inductance and C_P is the primary-side capacitance (mostly from the drain capacitance (C_{OSS}) of the primary-side power MOSFET). A snubber may be added to reduce the leakage inductance as discussed.

For each secondary-side power MOSFET, the BV_{DSS} should be greater than:

$$BV_{DSS} \geq V_{OUT} + V_{IN(MAX)} \bullet N_{SP}$$

Choose the primary side MOSFET $R_{DS(ON)}$ at the nominal gate drive voltage (7.5V). The secondary side MOSFET gate drive voltage depends on the gate drive method.

Primary side power MOSFET RMS current is given by:

$$I_{RMS(PRI)} = \frac{P_{IN}}{V_{IN(MIN)} \sqrt{DC_{MAX}}}$$

For each secondary-side power MOSFET RMS current is given by:

$$I_{RMS(SEC)} = \frac{I_{OUT}}{\sqrt{1 - DC_{MAX}}}$$

Calculate MOSFET power dissipation next. Because the primary-side power MOSFET operates at high V_{DS}, a transition power loss term is included for accuracy. C_{MILLER} is the most critical parameter in determining the transition loss, but is not directly specified on the data sheets.

C_{MILLER} is calculated from the gate charge curve included on most MOSFET data sheets (Figure 17).

The flat portion of the curve is the result of the Miller (gate-to-drain) capacitance as the drain voltage drops. The Miller capacitance is computed as:

$$C_{MILLER} = \frac{Q_B - Q_A}{V_{DS}}$$

The curve is done for a given V_{DS}. The Miller capacitance for different V_{DS} voltages are estimated by multiplying the computed C_{MILLER} by the ratio of the application V_{DS} to the curve specified V_{DS}.

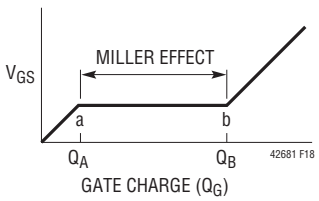


Figure 18. Gate Charge Curve

APPLICATIONS INFORMATION

With C_{MILLER} determined, calculate the primary-side power MOSFET power dissipation:

$$P_{D(PRI)} = I_{RMS(PRI)}^2 \bullet R_{DS(ON)}(1+\delta) + V_{IN(MAX)} \bullet \frac{P_{IN(MAX)}}{DC_{MIN}} \bullet R_{DR} \bullet \frac{C_{MILLER}}{V_{GATE(MAX)} - V_{TH}} \bullet f_{OSC}$$

where:

R_{DR} is the gate driver resistance (≈10Ω)

V_{TH} is the MOSFET gate threshold voltage

f_{OSC} is the operating frequency

$V_{GATE(MAX)}$ = 7.5V for this part

(1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve. If you don't have a curve, use δ = 0.005/°C • ΔT for low voltage MOSFETs.

The secondary-side power MOSFETs typically operate at substantially lower V_{DS}, so you can neglect transition losses. The dissipation is calculated using:

$$P_{DIS(SEC)} = I_{RMS(SEC)}^2 \bullet R_{DS(ON)}(1 + \delta)$$

With power dissipation known, the MOSFETs' junction temperatures are obtained from the equation:

$$T_J = T_A + P_{DIS} \bullet \theta_{JA}$$

where T_A is the ambient temperature and θ_{JA} is the MOSFET junction to ambient thermal resistance.

Once you have T_J iterate your calculations recomputing δ and power dissipations until convergence.

Gate Drive Node Consideration

The PG and SG gate drivers are strong drives to minimize gate drive rise and fall times. This improves efficiency but the high frequency components of these signals can cause problems. Keep the traces short and wide to reduce parasitic inductance.

The parasitic inductance creates an LC tank with the MOSFET gate capacitance. In less than ideal layouts, a series resistance of 5Ω or more may help to dampen the ringing at the expense of slightly slower rise and fall times and poorer efficiency.

The LTC4268-1 gate drives will clamp the max gate voltage to roughly 7.5V, so you can safely use MOSFETs with maximum V_{GS} of 10V and larger.

Synchronous Gate Drive

There are several different ways to drive the synchronous gate MOSFET. Full converter isolation requires the synchronous gate drive to be isolated. This is usually accomplished by way of a pulse transformer. Usually the pulse driver is used to drive a buffer on the secondary as shown in the application on the front page of this data sheet.

However, other schemes are possible. There are gate drivers and secondary side synchronous controllers available that provide the buffer function as well as additional features.

Capacitor Selection

In a flyback converter, the input and output current flows in pulses, placing severe demands on the input and output filter capacitors. The input and output filter capacitors are selected based on RMS current ratings and ripple voltage.

Select an input capacitor with a ripple current rating greater than:

$$I_{RMS(PRI)} = \frac{P_{IN}}{V_{IN(MIN)}} \sqrt{\frac{1 - DC_{MAX}}{DC_{MAX}}}$$

Continuing the example:

$$I_{RMS(PRI)} = \frac{29.5W}{41V} \sqrt{\frac{1 - 49.4\%}{49.4\%}} = 0.728A$$

Keep input capacitor series resistance (ESR) and inductance (ESL) small, as they affect electromagnetic interference suppression. In some instances, high ESR can also produce stability problems because flyback converters exhibit a negative input resistance characteristic. Refer to Application Note 19 for more information. The output capacitor is sized to handle the ripple current and to ensure acceptable output voltage ripple.

APPLICATIONS INFORMATION

The output capacitor should have an RMS current rating greater than:

$$I_{RMS(SEC)} = I_{OUT}\sqrt{\frac{DC_{MAX}}{1-DC_{MAX}}}$$

Continuing the example:

$$I_{RMS(SEC)} = 5.3A\sqrt{\frac{49.4\%}{1-49.4\%}} = 5.24A$$

This is calculated for each output in a multiple winding application.

ESR and ESL along with bulk capacitance directly affect the output voltage ripple. The waveforms for a typical flyback converter are illustrated in Figure 19.

The maximum acceptable ripple voltage (expressed as a percentage of the output voltage) is used to establish a starting point for the capacitor values. For the purpose of simplicity we will choose 2% for the maximum output ripple, divided equally between the ESR step and the charging/discharging ΔV. This percentage ripple changes, depending on the requirements of the application. You can modify the equations below. For a 1% contribution to the total ripple voltage, the ESR of the output capacitor is determined by:

$$ESR_{COUT} \le 1\% \bullet \frac{V_{OUT} \bullet (1-DC_{MAX})}{I_{OUT}}$$

The other 1% is due to the bulk C component, so use:

$$C_{OUT} \ge \frac{I_{OUT}}{1\% \bullet V_{OUT} \bullet f_{OSC}}$$

In many applications the output capacitor is created from multiple capacitors to achieve desired voltage ripple, reliability and cost goals. For example, a low ESR ceramic capacitor can minimize the ESR step, while an electrolytic capacitor satisfies the required bulk C.

Continuing our example, the output capacitor needs:

$$ESR_{COUT} \le 1\% \bullet \frac{5V \bullet (1-49.4\%)}{5.3A} = 4m\Omega$$

$$C_{OUT} \ge \frac{5.3A}{1\% \bullet 5 \bullet 200kHz} = 600\mu F$$

These electrical characteristics require paralleling several low ESR capacitors possibly of mixed type.

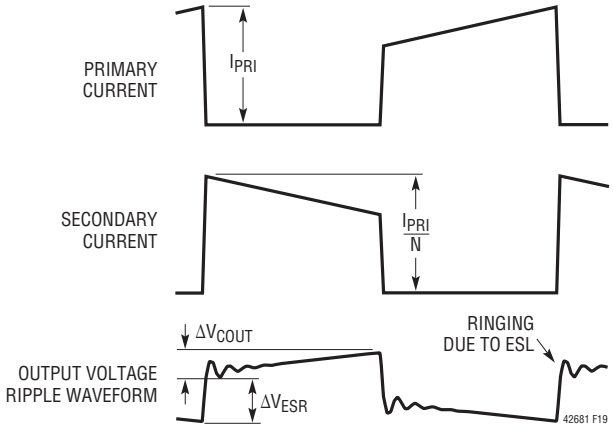


Figure 19. Typical Flyback Converter Waveforms

APPLICATIONS INFORMATION

Most capacitor ripple current ratings are based on 2000 hour life. This makes it advisable to derate the capacitor or to choose a capacitor rated at a higher temperature than required.

One way to reduce cost and improve output ripple is to use a simple LC filter. Figure 20 shows an example of the filter.

The design of the filter is beyond the scope of this data sheet. However, as a starting point, use these general guidelines. Start with a C_{OUT} 1/4 the size of the nonfilter solution. Make C1 1/4 of C_{OUT} to make the second filter pole independent of C_{OUT}. C1 may be best implemented with multiple ceramic capacitors. Make L1 smaller than the output inductance of the transformer. In general, a 0.1µH filter inductor is sufficient. Add a small ceramic capacitor (C_{OUT2}) for high frequency noise on V_{OUT}. For those interested in more details refer to "Second-Stage LC Filter Design," Ridley, Switching Power Magazine, July 2000 p8-10.

Circuit simulation is a way to optimize output capacitance and filters, just make sure to include the component parasitic. LTC SwitcherCAD® is a terrific free circuit simulation tool that is available at www.linear.com. Final optimization of output ripple must be done on a dedicated PC board. Parasitic inductance due to poor layout can significantly impact ripple. Refer to the PC Board Layout section for more details.

ISOLATION

The 802.3 standard requires Ethernet ports to be electrically isolated from all other conductors that are user accessible. This includes the metal chassis, other connectors and any auxiliary power connection. For PDs, there are two common methods to meet the isolation requirement. If there will be any user accessible connection to the PD, then an isolated DC/DC converter is necessary to meet the isolation requirements. If user connections can be avoided, then it is possible to meet the safety requirement by completely enclosing the PD in an insulated housing. In all PD applications, there should be no user accessible electrical connections to the LTC4268-1 or support circuitry other than the RJ-45 port.

LAYOUT CONSIDERATIONS FOR THE LTC4268-1

The LTC4268-1's PD front end is relatively immune to layout problems. Place C14 (Figure 9) as close as physically possible to the LTC4268-1. Place the series 10Ω resistor close to C14. Excessive parasitic capacitance on the R_{CLASS} pin should be avoided. Include a PCB heat sink to which the exposed pad on the bottom of the package can be soldered. This heat sink should be electrically connected to GND. For optimum thermal performance, make the heat sink as large as possible. Voltages in a PD can be as large as –57V for PoE applications, so high voltage layout techniques should be employed. The SHDN pin should be separated from other high voltage pins, like V_{PORTP}, V_{OUT}, to avoid the possibility of leakage shutting down the LTC4268-1. If not used, tie SHDN to V_{PORTN}. The load capacitor connected between V_{PORTP} and V_{OUT} of the LTC4268-1 can store significant energy when fully charged. The design of a PD must ensure that this energy is not inadvertently dissipated in the LTC4268-1. The polarity-protection diodes prevent an accidental short on the cable from causing damage. However if, V_{PORTN} is shorted to V_{PORTP} inside the PD while capacitor C1 is charged, current will flow through the parasitic body diode of the internal MOSFET and may cause permanent damage to the LTC4268-1.

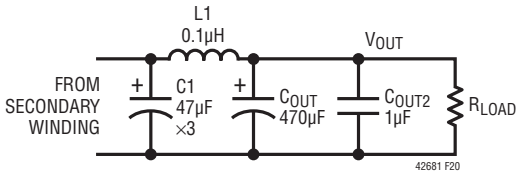


Figure 20. LC Filter

APPLICATIONS INFORMATION

In order to minimize switching noise and improve output load regulation, connect the GND pin of the LTC4268-1 directly to the ground terminal of the V_{CC} decoupling capacitor, the bottom terminal of the current sense resistor and the ground terminal of the input capacitor, using a ground plane with multiple vias. Place the V_{CC} capacitor immediately adjacent to the V_{CC} and GND pins on the IC package. This capacitor carries high di/dt MOSFET gate drive currents. Use a low ESR ceramic capacitor. Take care in PCB layout to keep the traces that conduct high switching currents short, wide and with minimal overall loop area. These are typically the traces associated with the switches. This reduces the parasitic inductance and also minimizes magnetic field radiation. Figure 21 outlines the critical paths. Keep electric field radiation low by minimizing the length and area of traces (keep stray capacitances low). The drain of the primary side MOSFET is the worst offender in this category. Always use a ground plane under the switcher circuitry to prevent coupling between PCB planes. Check that the maximum BV_{DSS} ratings of the MOSFETs are not exceeded due to inductive ringing. This is done by viewing the MOSFET node voltages with an oscilloscope. If it is breaking down either choose a higher voltage device, add a snubber or specify an avalanche-rated MOSFET.

Place the small-signal components away from high frequency switching nodes. This allows the use of a pseudo-Kelvin connection for the signal ground, where high di/dt gate driver currents flow out of the IC ground pin in one direction (to the bottom plate of the V_{CC} decoupling capacitor) and small-signal currents flow in the other direction. Keep the trace from the feedback divider tap to the FB pin short to preclude inadvertent pickup. For applications with multiple switching power converters connected to the same input supply, make sure that the input filter capacitor for the LTC4268-1 is not shared with other converters. AC input current from another converter could cause substantial input voltage ripple and this could interfere with the LTC4268-1 operation. A few inches of PC trace or wire ($L \cong 100nH$) between the C_{IN} of the LTC4268-1 and the actual source V_{IN} is sufficient to prevent current sharing problems.

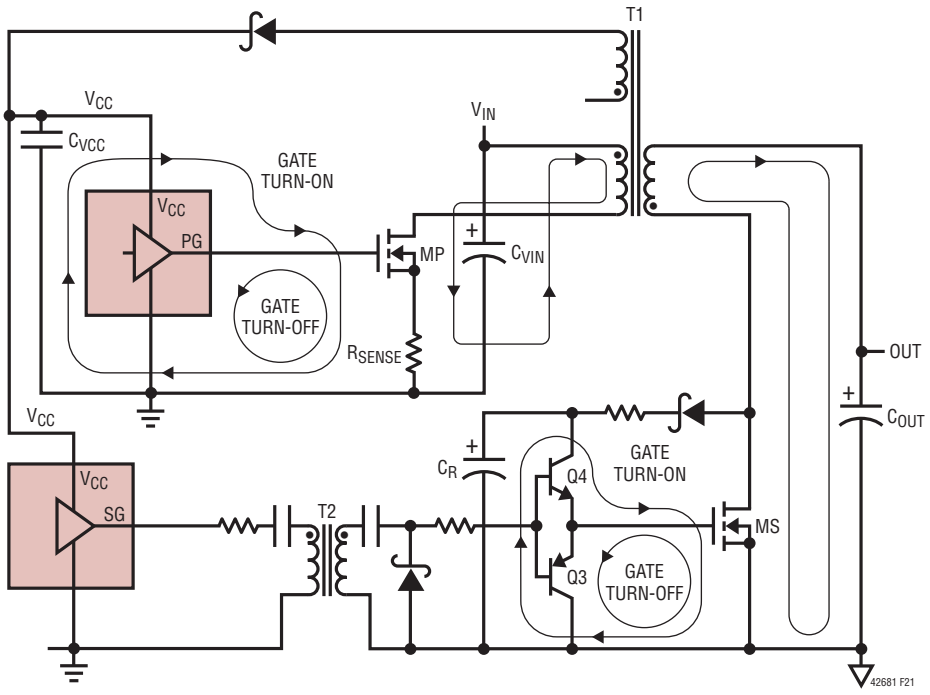
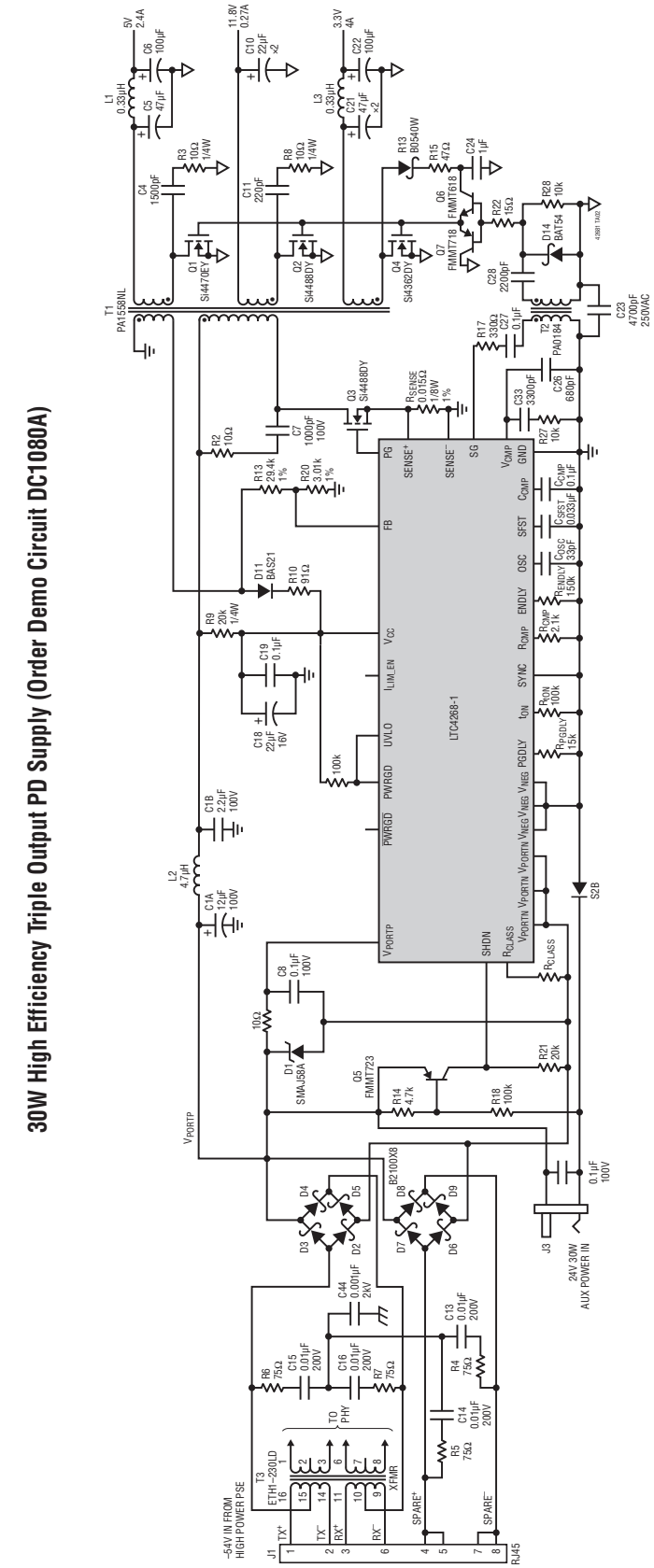


Figure 21. Layout Critical High Current Paths

TYPICAL APPLICATION

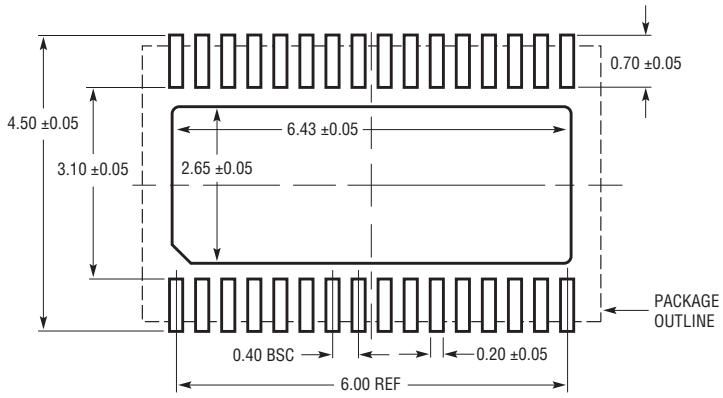
30W High Efficiency Triple Output PD Supply (Order Demo Circuit DC1080A)

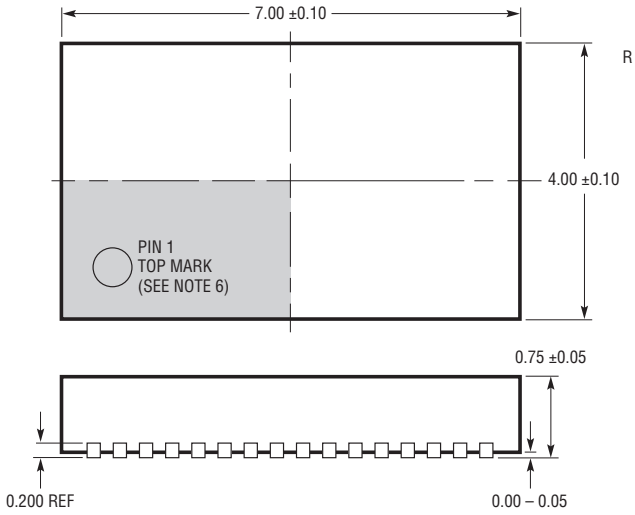


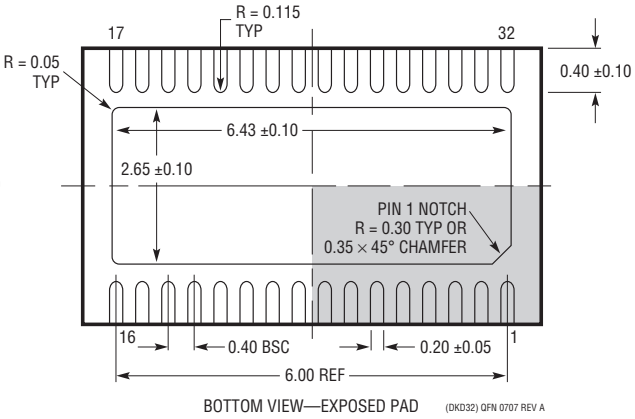
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DKD Package
32-Lead Plastic DFN (7mm × 4mm)
(Reference LTC DWG # 05-08-1734 Rev A)







NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WXXX) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	08/12	Simplified Overview section, including removal of Figure 1A and 1B which caused renumbering of all figures in data sheet	13, 14
		Changed maximum power levels for class 0 and class 3 to 13.0W	15
		Added 10Ω resistor to V_{PORTP} pin on schematic to make solution more robust to current surges	20, 43
		Added Input Capacitor, Input Series Resistance and Transient Voltage Supressor sections	21
		Added C14 and 10Ω resistor layout recommendation	41