

## FEATURES

- **Tiny 3mm × 3mm 8-Pin DFN Package**
- **Maximum 16-Bit INL Error:  $\pm 1$ LSB over Temperature**
- **Low 120 $\mu$ A Supply Current**
- **Guaranteed Monotonic over Temperature**
- **Low 0.5nV•sec Glitch Impulse**
- 2.7V to 5.5V Single Supply Operation
- Fast 1 $\mu$ s Settling Time to 16 Bits
- Unbuffered Voltage Output Directly Drives 60k Loads
- 50MHz SPI/QSPI/MICROWIRE Compatible Serial Interface
- Power-On Reset Clears DAC Output to Zero Scale (LTC2641) or Midscale (LTC2642)
- Schmitt-Trigger Inputs for Direct Optocoupler Interface
- Asynchronous  $\overline{\text{CLR}}$  Pin
- 8-Lead MSOP and 3mm × 3mm DFN Packages (LTC2641)
- 10-Lead MSOP and 3mm × 3mm DFN Packages (LTC2642)

## APPLICATIONS

- High Resolution Offset and Gain Adjustment
- Process Control and Industrial Automation
- Automatic Test Equipment
- Data Acquisition Systems

## DESCRIPTION

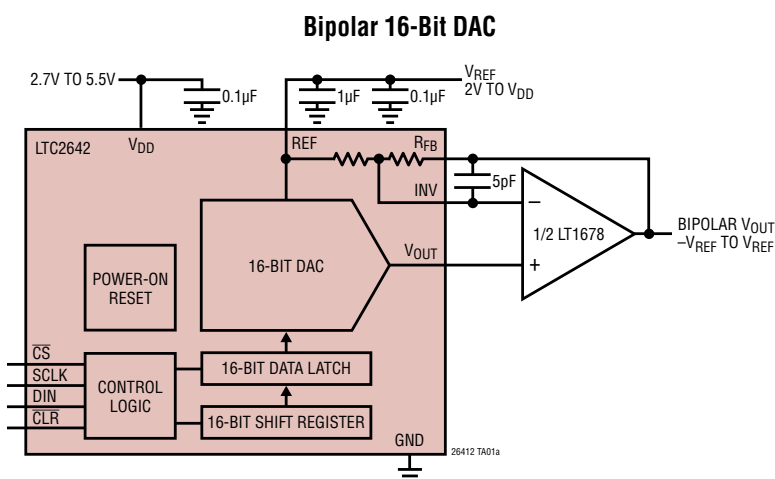
The **LTC<sup>®</sup>2641/LTC2642** are families of 16-, 14- and 12-bit unbuffered voltage output DACs. These DACs operate from a single 2.7V to 5.5V supply and are guaranteed monotonic over temperature. The LTC2641A-16/LTC2642A-16 provide 16-bit performance ( $\pm 1$ LSB INL and  $\pm 1$ LSB DNL) over temperature. Unbuffered DAC outputs result in low supply current of 120 $\mu$ A and a low offset error of  $\pm 1$ LSB.

Both the LTC2641 and LTC2642 feature a reference input range of 2V to  $V_{DD}$ .  $V_{OUT}$  swings from 0V to  $V_{REF}$ . For bipolar operation, the LTC2642 includes matched scaling resistors for use with an external precision op amp (such as the LT1678), generating a  $\pm V_{REF}$  output swing at  $R_{FB}$ .

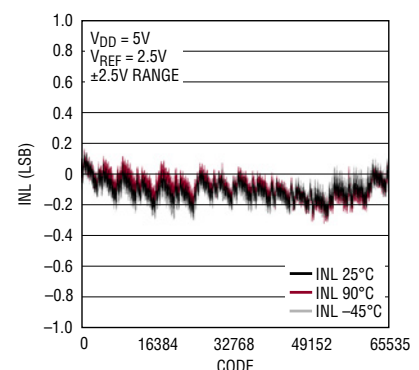
The LTC2641/LTC2642 use a simple SPI/MICROWIRE compatible 3-wire serial interface which can be operated at clock rates up to 50MHz and can interface directly with optocouplers for applications requiring isolation. A power-on reset circuit clears the LTC2641's DAC output to zero scale and the LTC2642's DAC output to midscale when power is initially applied. A logic low on the  $\overline{\text{CLR}}$  pin asynchronously clears the DAC to zero scale (LTC2641) or midscale (LTC2642). These DACs are all specified over the commercial and industrial ranges.

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## TYPICAL APPLICATION



**LTC2642-16 Integral Nonlinearity**



# LTC2641/LTC2642

## ABSOLUTE MAXIMUM RATINGS (Note 1)

$V_{DD}$ to GND .....	-0.3V to 6V	Operating Temperature Range	
$\overline{CS}$ , SCLK, DIN,		LTC2641C/LTC2642C .....	0°C to 70°C
$\overline{CLR}$ to GND .....	-0.3V to ( $V_{DD} + 0.3V$ ) or 6V	LTC2641I/LTC2642I .....	-40°C to 85°C
REF, $V_{OUT}$ , INV to GND .....	-0.3V to ( $V_{DD} + 0.3V$ ) or 6V	Maximum Junction Temperature (Note 2) .....	125°C
$R_{FB}$ to INV .....	-6V to 6V	Storage Temperature Range .....	-65°C to 150°C
$R_{FB}$ to GND .....	-6V to 6V	Lead Temperature (Soldering, 10 sec) .....	300°C
GND to GND (S8 Package) <b>OBSOLETE</b> ....	-0.3V to 0.3V		

## PIN CONFIGURATION

<p>LTC2641</p> <p>TOP VIEW</p> <p>DD PACKAGE 8-LEAD (3mm × 3mm) PLASTIC DFN</p> <p><math>T_{JMAX} = 125^{\circ}C</math> (NOTE 2), <math>\theta_{JA} = 43^{\circ}C/W</math> EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB</p>	<p>LTC2641</p> <p>TOP VIEW</p> <p>MS8 PACKAGE 8-LEAD PLASTIC MSOP</p> <p><math>T_{JMAX} = 125^{\circ}C</math> (NOTE 2), <math>\theta_{JA} = 120^{\circ}C/W</math></p>	<p>LTC2641</p> <p>TOP VIEW</p> <p>S8 PACKAGE 8-LEAD PLASTIC SO</p> <p><math>T_{JMAX} = 125^{\circ}C</math>, <math>\theta_{JA} = 110^{\circ}C/W</math> <b>OBSOLETE PACKAGE</b></p>
<p>LTC2642</p> <p>TOP VIEW</p> <p>DD PACKAGE 10-LEAD (3mm × 3mm) PLASTIC DFN</p> <p><math>T_{JMAX} = 125^{\circ}C</math> (NOTE 2), <math>\theta_{JA} = 43^{\circ}C/W</math> EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB</p>	<p>LTC2642</p> <p>TOP VIEW</p> <p>MS PACKAGE 10-LEAD PLASTIC MSOP</p> <p><math>T_{JMAX} = 125^{\circ}C</math> (NOTE 2), <math>\theta_{JA} = 120^{\circ}C/W</math></p>	

## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2641ACDD-16#PBF	LTC2641ACDD-16#TRPBF	LCZP	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2641CDD-16#PBF	LTC2641CDD-16#TRPBF	LCZP	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2641CDD-14#PBF	LTC2641CDD-14#TRPBF	LCZN	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2641CDD-12#PBF	LTC2641CDD-12#TRPBF	LCZM	8-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2641AIDD-16#PBF	LTC2641AIDD-16#TRPBF	LCZP	8-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LTC2641IDD-16#PBF	LTC2641IDD-16#TRPBF	LCZP	8-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LTC2641IDD-14#PBF	LTC2641IDD-14#TRPBF	LCZN	8-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LTC2641IDD-12#PBF	LTC2641IDD-12#TRPBF	LCZM	8-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LTC2641ACMS8-16#PBF	LTC2641ACMS8-16#TRPBF	LTCZS	8-Lead Plastic MSOP	0°C to 70°C
LTC2641CMS8-16#PBF	LTC2641CMS8-16#TRPBF	LTCZS	8-Lead Plastic MSOP	0°C to 70°C
LTC2641CMS8-14#PBF	LTC2641CMS8-14#TRPBF	LTCZR	8-Lead Plastic MSOP	0°C to 70°C
LTC2641CMS8-12#PBF	LTC2641CMS8-12#TRPBF	LTCZQ	8-Lead Plastic MSOP	0°C to 70°C
LTC2641AIMS8-16#PBF	LTC2641AIMS8-16#TRPBF	LTCZS	8-Lead Plastic MSOP	-40°C to 85°C
LTC2641IMS8-16#PBF	LTC2641IMS8-16#TRPBF	LTCZS	8-Lead Plastic MSOP	-40°C to 85°C
LTC2641IMS8-14#PBF	LTC2641IMS8-14#TRPBF	LTCZR	8-Lead Plastic MSOP	-40°C to 85°C
LTC2641IMS8-12#PBF	LTC2641IMS8-12#TRPBF	LTCZQ	8-Lead Plastic MSOP	-40°C to 85°C
LTC2642ACDD-16#PBF	LTC2642ACDD-16#TRPBF	LCZW	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2642CDD-16#PBF	LTC2642CDD-16#TRPBF	LCZW	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2642CDD-14#PBF	LTC2642CDD-14#TRPBF	LCZV	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2642CDD-12#PBF	LTC2642CDD-12#TRPBF	LCZT	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC2642AIDD-16#PBF	LTC2642AIDD-16#TRPBF	LCZW	10-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LTC2642IDD-16#PBF	LTC2642IDD-16#TRPBF	LCZW	10-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LTC2642IDD-14#PBF	LTC2642IDD-14#TRPBF	LCZV	10-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LTC2642IDD-12#PBF	LTC2642IDD-12#TRPBF	LCZT	10-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LTC2642ACMS-16#PBF	LTC2642ACMS-16#TRPBF	LTCZZ	10-Lead Plastic MSOP	0°C to 70°C
LTC2642CMS-16#PBF	LTC2642CMS-16#TRPBF	LTCZZ	10-Lead Plastic MSOP	0°C to 70°C
LTC2642CMS-14#PBF	LTC2642CMS-14#TRPBF	LTCZY	10-Lead Plastic MSOP	0°C to 70°C
LTC2642CMS-12#PBF	LTC2642CMS-12#TRPBF	LTCZX	10-Lead Plastic MSOP	0°C to 70°C
LTC2642AIMS-16#PBF	LTC2642AIMS-16#TRPBF	LTCZZ	10-Lead Plastic MSOP	-40°C to 85°C
LTC2642IMS-16#PBF	LTC2642IMS-16#TRPBF	LTCZZ	10-Lead Plastic MSOP	-40°C to 85°C
LTC2642IMS-14#PBF	LTC2642IMS-14#TRPBF	LTCZY	10-Lead Plastic MSOP	-40°C to 85°C
LTC2642IMS-12#PBF	LTC2642IMS-12#TRPBF	LTCZX	10-Lead Plastic MSOP	-40°C to 85°C
<b>OBSOLETE</b>				
LTC2641CS8-16#PBF	LTC2641CS8-16#TRPBF	264116	8-Lead Plastic SO	0°C to 70°C
LTC2641IS8-16#PBF	LTC2641IS8-16#TRPBF	264116	8-Lead Plastic SO	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

# LTC2641/LTC2642

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{DD} = 3\text{V}$  or  $5\text{V}$ ,  $V_{REF} = 2.5\text{V}$ ,  $C_L = 10\text{pF}$ ,  $\text{GND} = 0$ ,  $R_L = \infty$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	LTC2641-12 LTC2642-12			LTC2641-14 LTC2642-14			LTC2641-16 LTC2642-16			LTC2641A-16 LTC2642A-16			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
<b>Static Performance</b>															
N	Resolution		●	12		14		16		16				Bits	
	Monotonicity		●	12		14		16		16				Bits	
DNL	Differential Nonlinearity	(Note 3)	●		±0.5	±0.5	±1	±0.5	±1	±0.5	±1			LSB	
INL	Integral Nonlinearity	(Note 3)	●		±0.5	±0.5	±1	±0.5	±2	±0.5	±1			LSB	
ZSE	Zero Code Offset Error	Code = 0	●		1		2		2				2	LSB	
ZSTC	Zero Code Tempco				±0.05		±0.05		±0.05				±0.05	ppm/°C	
GE	Gain Error		●		±0.5	±2	±1	±4	±2	±5			±2	±5	LSB
GETC	Gain Error Tempco				±0.1		±0.1		±0.1				±0.1	ppm/°C	
ROUT	DAC Output Resistance	(Note 4)			6.2		6.2		6.2				6.2	kΩ	
	Bipolar Resistor Matching	(LTC2642) $R_{FB}/R_{INV}$			1		1		1				1		
		Ratio Error (Note 7)	●		±0.1		±0.03		±0.015				±0.015	%	
BZE	Bipolar Zero Offset Error	(LTC2642)	●		±0.5	±2	±0.5	±4	±2	±5			±2	±5	LSB
BZSTC	Bipolar Zero Tempco	(LTC2642)			±0.1		±0.1		±0.1				±0.1	ppm/°C	
PSR	Power Supply Rejection	$\Delta V_{DD} = \pm 10\%$	●		±0.5		±0.5		±1				±1	LSB	

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Reference Input</b>						
$V_{REF}$	Reference Input Range		●	2.0	$V_{DD}$	V
$R_{REF}$	Reference Input Resistance (Note 5)	Unipolar Mode (LTC2641)	●	11	14.8	kΩ
		Bipolar Mode (LTC2642)	●	8.5	11.4	kΩ

### Dynamic Performance— $V_{OUT}$

SR	Voltage Output Slew Rate	Measured from 10% to 90%		15		V/μs
	Output Settling Time	To ±0.5LSB of FS		1		μs
	DAC Glitch Impulse	Major Carry Transition		0.5		nV•s
	Digital Feedthrough	Code = 0000hex; NCS = $V_{DD}$ ; SCLK, DIN OV to $V_{DD}$ Levels		0.2		nV•s
	Output Voltage Noise Density			10		nV/√Hz

### Dynamic Performance—Reference Input

BW	Reference -3dB Bandwidth	Code = FFFFhex		1.3		MHz
	Reference Feedthrough	Code = 0000hex, $V_{REF} = 1V_{P-P}$ at 100kHz		1		mV <sub>P-P</sub>
SNR	Signal-to-Noise Ratio			92		dB
$C_{IN(REF)}$	Reference Input Capacitance	Code = 0000hex Code = FFFFhex		75 120		pF pF

### Digital Inputs

$V_{IH}$	Digital Input High Voltage	$V_{CC} = 3.6\text{V}$ to $5.5\text{V}$ $V_{CC} = 2.7\text{V}$ to $3.6\text{V}$	●	2.4		V
			●	2.0		V

26412fd

## ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IL}$	Digital Input Low Voltage	$V_{CC} = 4.5\text{V}$ to $5.5\text{V}$	●		0.8	V
		$V_{CC} = 2.7\text{V}$ to $4.5\text{V}$	●		0.6	V
$I_{IN}$	Digital Input Current	$V_{IN} = \text{GND}$ to $V_{DD}$	●		$\pm 1$	$\mu\text{A}$
$C_{IN}$	Digital Input Capacitance	(Note 6)	●	3	10	pF
$V_H$	Hysteresis Voltage			0.15		V
<b>Power Supply</b>						
$V_{DD}$	Supply Voltage		●	2.7	5.5	V
$I_{DD}$	Supply Current, $V_{DD}$	Digital Inputs = $0\text{V}$ or $V_{DD}$	●	120	200	$\mu\text{A}$
$P_D$	Power Dissipation	Digital Inputs = $0\text{V}$ or $V_{DD}$ , $V_{DD} = 5\text{V}$		0.60		mW
		Digital Inputs = $0\text{V}$ or $V_{DD}$ , $V_{DD} = 3\text{V}$		0.36		mW

## TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{DD} = 3\text{V}$  or  $5\text{V}$ ,  $V_{REF} = 2.5\text{V}$ ,  $C_L = 10\text{pF}$ ,  $\text{GND} = 0$ ,  $R_L = \infty$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_1$	DIN Valid to SCLK Setup Time		●	10		ns
$t_2$	DIN Valid to SCLK Hold Time		●	0		ns
$t_3$	SCLK Pulse Width High		●	9		ns
$t_4$	SCLK Pulse Width Low		●	9		ns
$t_5$	$\overline{\text{CS}}$ Pulse High Width		●	10		ns
$t_6$	LSB SCLK High to $\overline{\text{CS}}$ High		●	8		ns
$t_7$	$\overline{\text{CS}}$ Low to SCLK High		●	8		ns
$t_8$	$\overline{\text{CS}}$ High to SCLK Positive Edge		●	8		ns
$t_9$	$\overline{\text{CLR}}$ Pulse Width Low		●	15		ns
$f_{\text{SCLK}}$	SCLK Frequency	50% Duty Cycle	●		50	MHz
		$V_{DD}$ High to $\overline{\text{CS}}$ Low (Power-Up Delay)			30	$\mu\text{s}$

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** Continuous operation above the specified maximum operating junction temperature may impair device reliability.

**Note 3:** LTC2641-16/LTC2642-16  $\pm 1\text{LSB} = \pm 0.0015\% = \pm 15.3\text{ppm}$  of full scale. LTC2641-14/LTC2642-14  $\pm 1\text{LSB} = \pm 0.006\% = \pm 61\text{ppm}$  of full scale. LTC2641-12/LTC2642-12  $\pm 1\text{LSB} = \pm 0.024\% = \pm 244\text{ppm}$  of full scale.

**Note 4:**  $R_{OUT}$  tolerance is typically  $\pm 20\%$ .

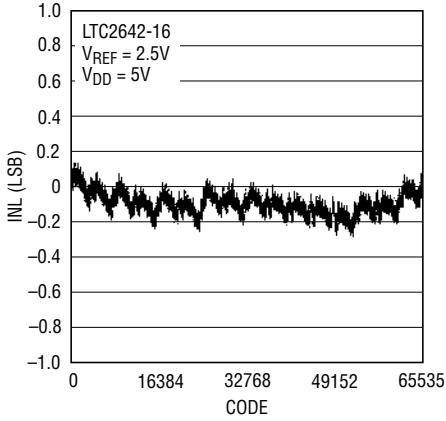
**Note 5:** Reference input resistance is code dependent. Minimum is at 871Chex (34,588) in unipolar mode and at 671Chex (26,396) in bipolar mode.

**Note 6:** Guaranteed by design and not production tested.

**Note 7:** Guaranteed by gain error and offset error testing, not production tested.

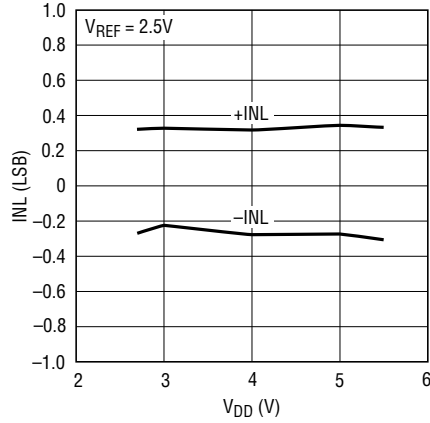
## TYPICAL PERFORMANCE CHARACTERISTICS

**Integral Nonlinearity (INL)**



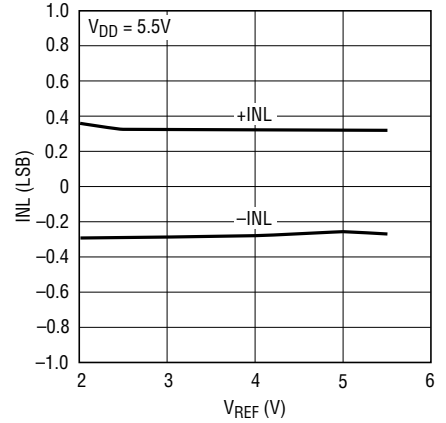
26412 G01

**Integral Nonlinearity (INL) vs Supply (V<sub>DD</sub>)**



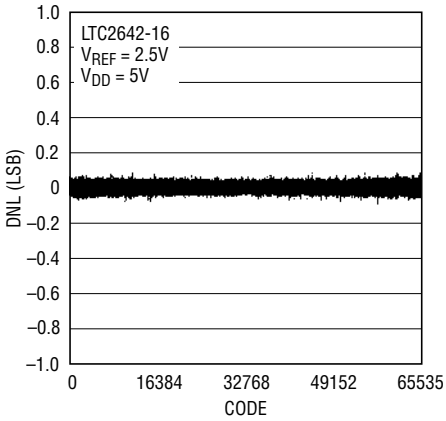
26412 G02

**INL vs V<sub>REF</sub>**



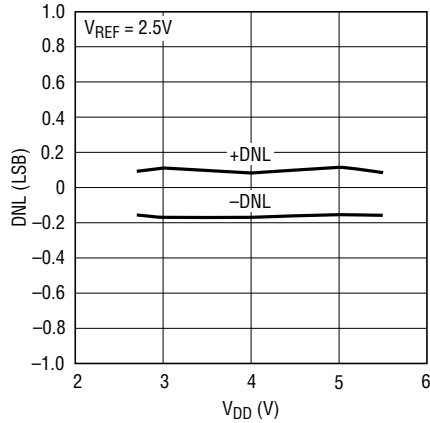
26412 G03

**Differential Nonlinearity (DNL)**



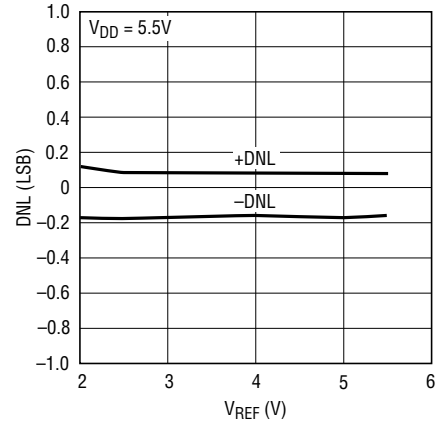
26412 G04

**Differential Nonlinearity (DNL) vs Supply (V<sub>DD</sub>)**



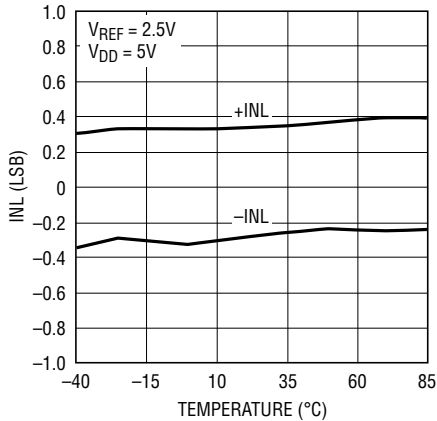
26412 G05

**DNL vs V<sub>REF</sub>**



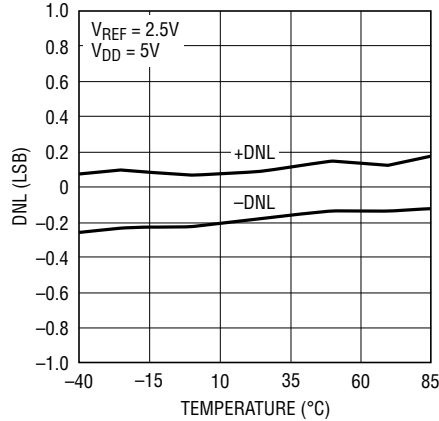
26412 G06

**INL vs Temperature**



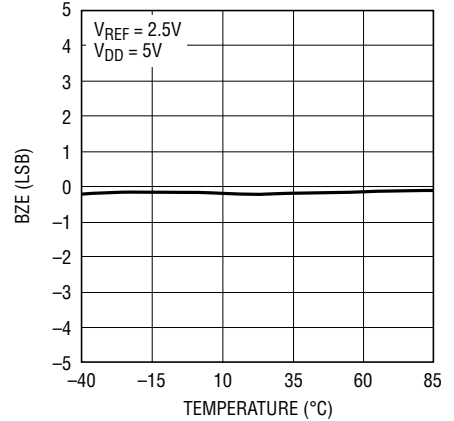
26412 G07

**DNL vs Temperature**



26412 G08

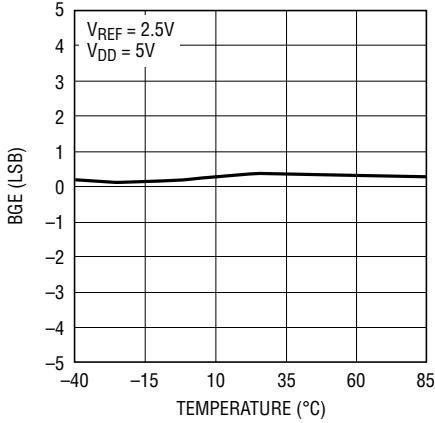
**Bipolar Zero Error vs Temperature**



26412 G09

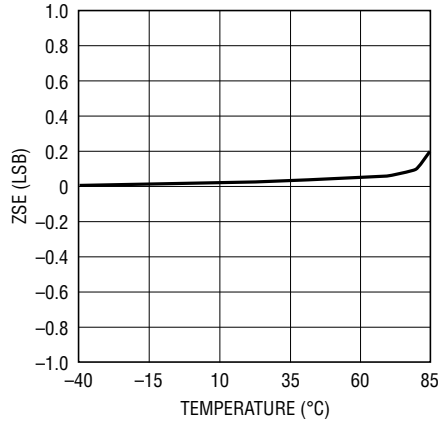
# TYPICAL PERFORMANCE CHARACTERISTICS

**Bipolar Gain Error vs Temperature**



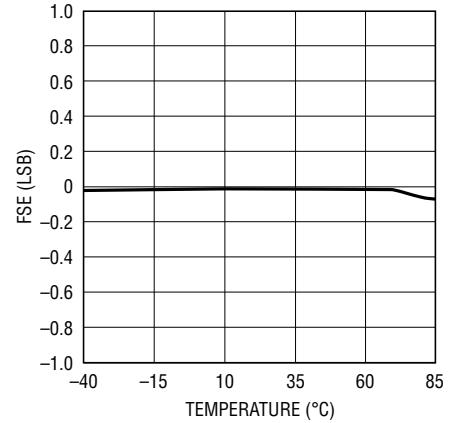
26412 G10

**Unbuffered Zero Scale Error vs Temperature (LTC2641-16)**



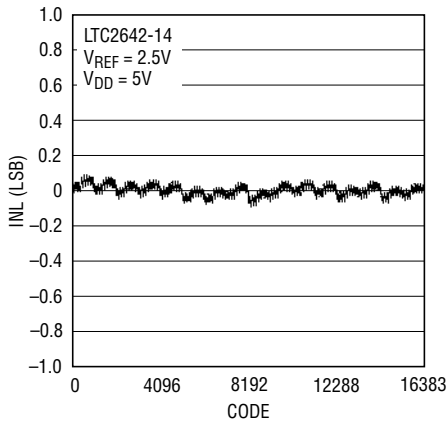
26412 G11

**Unbuffered Full-Scale Error vs Temperature (LTC2641-16)**



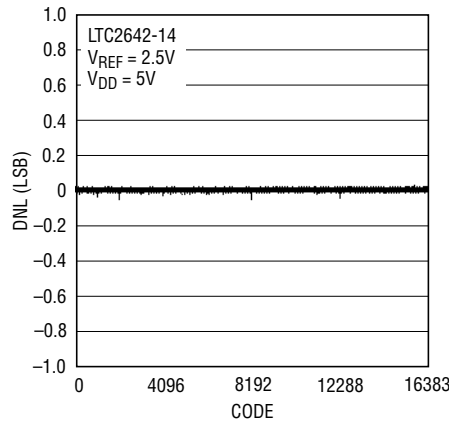
26412 G12

**14-Bit Integral Nonlinearity (INL) (LTC2642-14)**



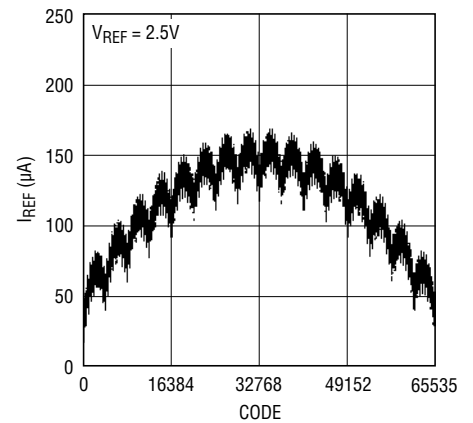
26412 G13

**14-Bit Differential Nonlinearity (DNL) (LTC2642-14)**



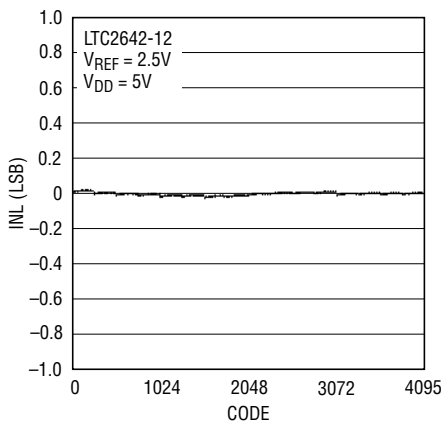
26412 G14

**I<sub>REF</sub> vs Code (Unipolar LTC2641)**



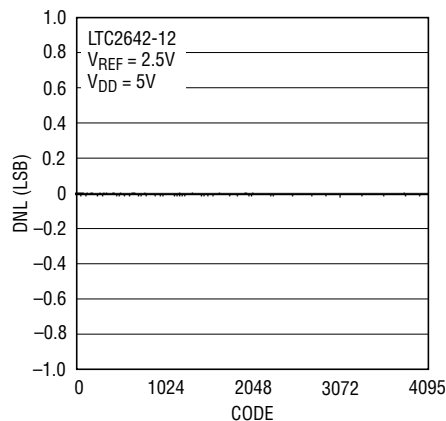
26412 G15

**12-Bit Integral Nonlinearity (INL) (LTC2642-12)**



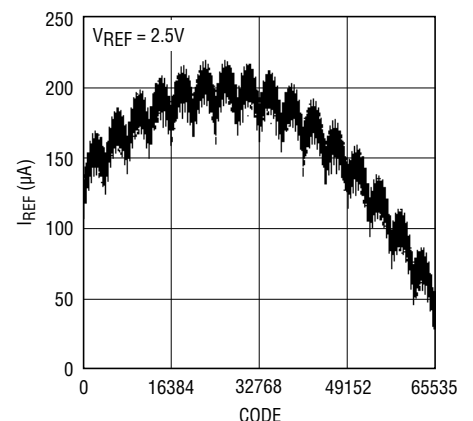
26412 G16

**12-Bit Differential Nonlinearity (DNL) (LTC2642-12)**



26412 G17

**I<sub>REF</sub> vs Code (Bipolar LTC2642)**

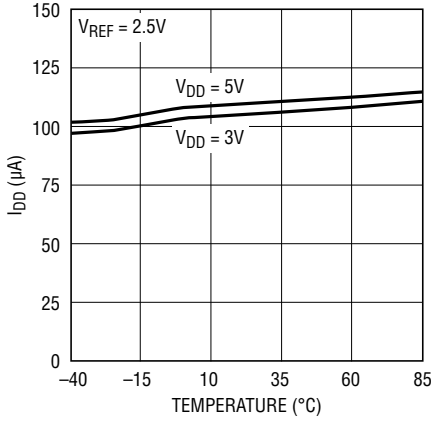


26412 G18

26412fd

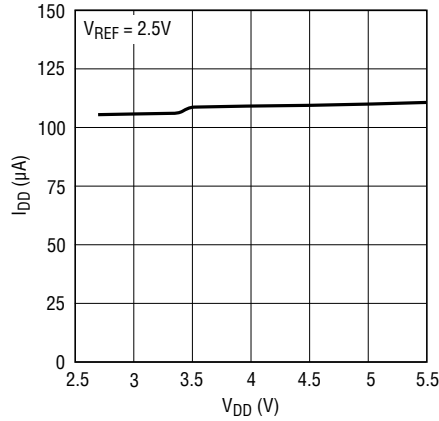
## TYPICAL PERFORMANCE CHARACTERISTICS

**Supply Current ( $I_{DD}$ ) vs Temperature**



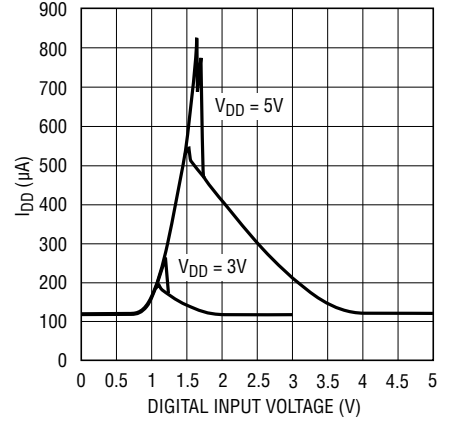
26412 G19

**Supply Current ( $I_{DD}$ ) vs Supply Voltage ( $V_{DD}$ )**



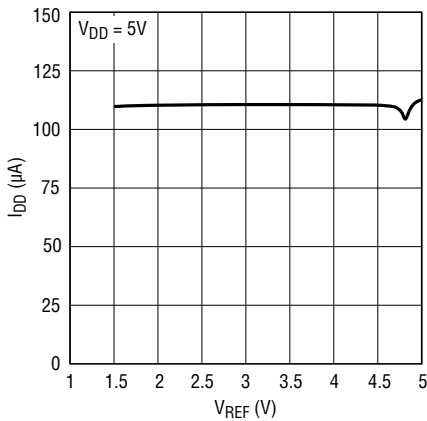
26412 G20

**Supply Current ( $I_{DD}$ ) vs Digital Input Voltage**



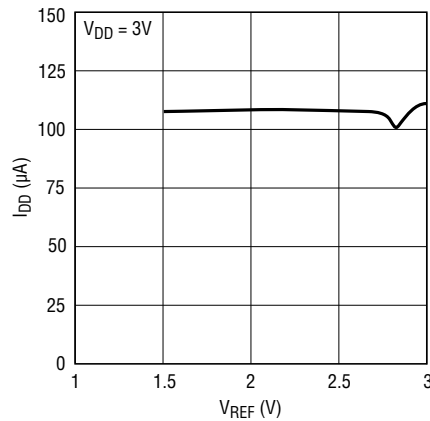
26412 G21

**Supply Current ( $I_{DD}$ ) vs  $V_{REF}$ ,  $V_{DD} = 5V$**



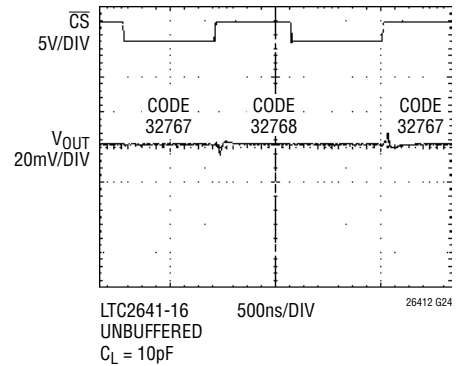
26412 G22

**Supply Current ( $I_{DD}$ ) vs  $V_{REF}$ ,  $V_{DD} = 3V$**



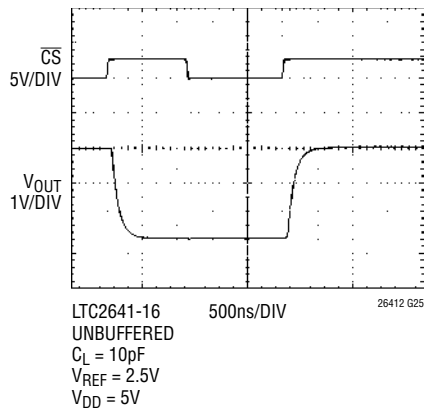
26412 G23

**Midscale Glitch Impulse**



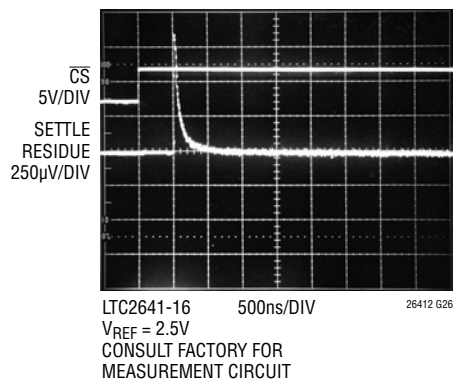
LTC2641-16 UNBUFFERED  
 $C_L = 10pF$   
500ns/DIV  
26412 G24

**Full-Scale Transition**



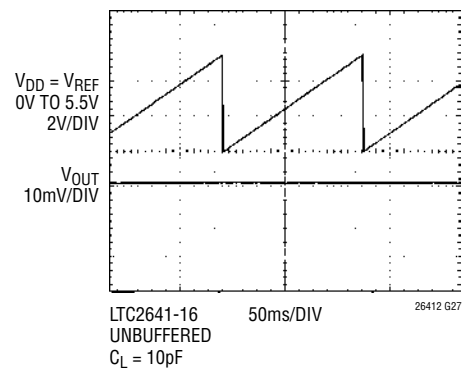
LTC2641-16 UNBUFFERED  
 $C_L = 10pF$   
 $V_{REF} = 2.5V$   
 $V_{DD} = 5V$   
500ns/DIV  
26412 G25

**Full-Scale Settling (Zoomed In)**



LTC2641-16 UNBUFFERED  
 $V_{REF} = 2.5V$   
CONSULT FACTORY FOR MEASUREMENT CIRCUIT  
500ns/DIV  
26412 G26

**$V_{OUT}$  vs  $V_{DD} = 0V$  to  $5.5V$  (POR Function) LTC2641**



LTC2641-16 UNBUFFERED  
 $C_L = 10pF$   
50ms/DIV  
26412 G27



## PIN FUNCTIONS

### LTC2641 – MSOP, DFN Packages

**REF (Pin 1):** Reference Voltage Input. Apply an external reference at REF between 2V and  $V_{DD}$ .

**$\overline{CS}$  (Pin 2):** Serial Interface Chip Select/Load Input. When  $\overline{CS}$  is low, SCLK is enabled for shifting in data on DIN. When  $\overline{CS}$  is taken high, SCLK is disabled, the 16-bit input word is latched and the DAC is updated.

**SCLK (Pin 3):** Serial Interface Clock Input. CMOS and TTL compatible.

**DIN (Pin 4):** Serial Interface Data Input. Data is applied to DIN for transfer to the device at the rising edge of SCLK.

**$\overline{CLR}$  (Pin 5):** Asynchronous Clear Input. A logic low clears the DAC to code 0.

**$V_{OUT}$  (Pin 6):** DAC Output Voltage. The output range is 0V to  $V_{REF}$ .

**$V_{DD}$  (Pin 7):** Supply Voltage. Set between 2.7V and 5.5V.

**GND (Pin 8):** Circuit Ground.

**Exposed Pad (DFN Pin 9):** Circuit Ground. Must be soldered to PCB ground.

### LTC2641 – SO Package OBSOLETE

**$V_{OUT}$  (Pin 1):** DAC Output Voltage. The output range is 0V to  $V_{REF}$ .

**GND (Pin 2):** Circuit Ground.

**REF (Pin 3):** Reference Voltage Input. Apply an external reference at REF between 2V and  $V_{DD}$ .

**$\overline{CS}$  (Pin 4):** Serial Interface Chip Select/Load Input. When  $\overline{CS}$  is low, SCLK is enabled for shifting in data on DIN. When  $\overline{CS}$  is taken high, SCLK is disabled, the 16-bit input word is latched and the DAC is updated.

**SCLK (Pin 5):** Serial Interface Clock Input. CMOS and TTL compatible.

**DIN (Pin 6):** Serial Interface Data Input. Data is applied to DIN for transfer to the device at the rising edge of SCLK.

**GND (Pin 7):** Circuit Ground Pin. Must be connected to Pin 2 (GND).

**$V_{DD}$  (Pin 8):** Supply Voltage. Set between 2.7V and 5.5V.

### LTC2642 – MSOP, DFN Packages

**REF (Pin 1):** Reference Voltage Input. Apply an external reference at REF between 2V and  $V_{DD}$ .

**$\overline{CS}$  (Pin 2):** Serial Interface Chip Select/Load Input. When  $\overline{CS}$  is low, SCLK is enabled for shifting in data on DIN. When  $\overline{CS}$  is taken high, SCLK is disabled, the 16-bit input word is latched and the DAC is updated.

**SCLK (Pin 3):** Serial Interface Clock Input. CMOS and TTL compatible.

**DIN (Pin 4):** Serial Interface Data Input. Data is applied to DIN for transfer to the device at the rising edge of SCLK.

**$\overline{CLR}$  (Pin 5):** Asynchronous Clear Input. A logic low clears the DAC to midscale.

**$V_{OUT}$  (Pin 6):** DAC Output Voltage. The output range is 0V to  $V_{REF}$ .

**INV (Pin 7):** Center Tap of Internal Scaling Resistors. Connect to an external amplifier's inverting input in bipolar mode.

**$R_{FB}$  (Pin 8):** Feedback Resistor. Connect to an external amplifier's output in bipolar mode. The bipolar output range is  $-V_{REF}$  to  $V_{REF}$ .

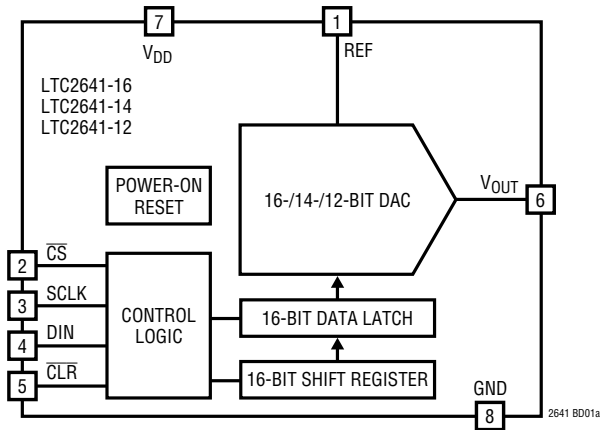
**$V_{DD}$  (Pin 9):** Supply Voltage. Set between 2.7V and 5.5V.

**GND (Pin 10):** Circuit Ground.

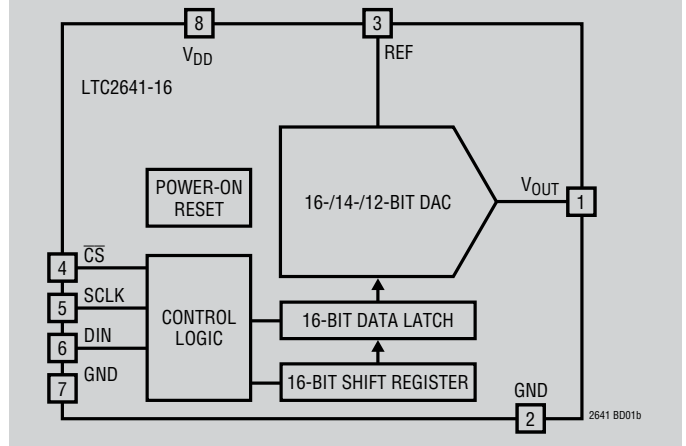
**Exposed Pad (DFN Pin 11):** Circuit Ground. Must be soldered to PCB ground.

## BLOCK DIAGRAMS

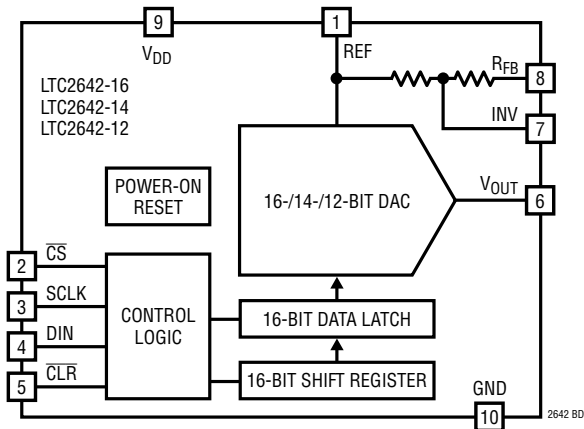
LTC2641 - MSOP, DFN



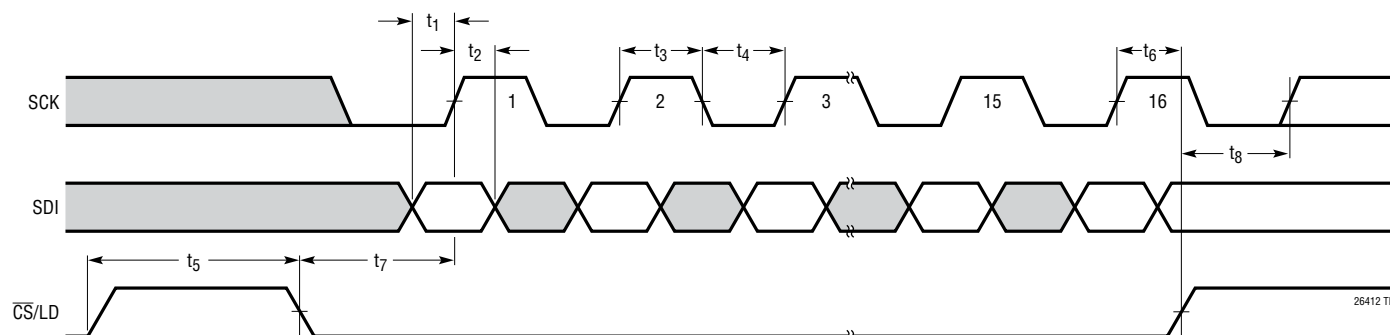
LTC2641 - SO  
OBSOLETE PACKAGE



LTC2642



## TIMING DIAGRAM



## OPERATION

### General Description

The LTC2641/LTC2642 family of 16-/14-/12-bit voltage output DACs offer full 16-bit performance with less than  $\pm 1$ LSB integral linearity error and less than  $\pm 1$ LSB differential linearity error, guaranteeing monotonic operation. They operate from a single supply ranging from 2.7V to 5.5V, consuming 120 $\mu$ A (typical). An external voltage reference of 2V to  $V_{DD}$  determines the DAC's full-scale output voltage. A 3-wire serial interface allows the LTC2641/LTC2642 to fit into a small 8-/10-pin MSOP or DFN 3mm  $\times$  3mm package.

### Digital-to-Analog Architecture

The DAC architecture is a voltage switching mode resistor ladder using precision thin-film resistors and CMOS switches. The LTC2641/LTC2642 DAC resistor ladders are composed of a proprietary arrangement of matched DAC sections. The four MSBs are decoded to drive 15 equally weighted segments, and the remaining lower bits drive successively lower weighted sections. Major carry glitch impulse is very low at 500pV $\cdot$ sec,  $C_L = 10$ pF, ten times lower than previous DACs of this type.

The digital-to-analog transfer function at the  $V_{OUT}$  pin is:

$$V_{OUT(IDEAL)} = \left( \frac{k}{2^N} \right) V_{REF}$$

where  $k$  is the decimal equivalent of the binary DAC input code,  $N$  is the resolution, and  $V_{REF}$  is between 2.0V and  $V_{DD}$  (see Tables 1a, 1b and 1c).

The LTC2642 includes matched resistors that are tied to an external amplifier to provide bipolar output swing (Figure 2). The bipolar transfer function at the RFB pin is:

$$V_{OUT\_BIPOLAR(IDEAL)} = V_{REF} \left( \frac{k}{2^{N-1}} - 1 \right)$$

(see Tables 2a, 2b and 2c).

### Serial Interface

The LTC2641/LTC2642 communicates via a standard 3-wire SPI/QSPI/MICROWIRE compatible interface. The chip select input ( $\overline{CS}$ ) controls and frames the loading of serial data from the data input (DIN). Following a  $\overline{CS}$  high-to-low transition, the data on DIN is loaded, MSB first, into the shift register on each rising edge of the serial clock

## OPERATION

input (SCLK). After 16 data bits have been loaded into the serial input register, a low-to-high transition on  $\overline{CS}$  transfers the data to the 16-bit DAC latch, updating the DAC output (see Figures 1a, 1b, 1c). While  $\overline{CS}$  remains high, the serial input shift register is disabled. If there are less than 16 low-to-high transitions on SCLK while  $\overline{CS}$  remains low, the data will be corrupted, and must be reloaded. Also, if there are more than 16 low-to-high transitions on SCLK while  $\overline{CS}$  remains low, only the last 16 data bits loaded from DIN will be transferred to the DAC latch. For the 14-bit DACs, (LTC2641-14/LTC2642-14), the MSB remains in the same (left-justified) position in the input 16-bit data word. Therefore, two “don’t-care” bits must be loaded after the LSB, to make up the required 16 data bits (Figure 1b). Similarly, for the 12-bit family members (LTC2641-12/LTC2642-12) four “don’t-care” bits must follow the LSB (Figure 1c).

### Power-On Reset

The LTC2641/LTC2642 include a power-on reset circuit to ensure that the DAC output comes up in a known state. When  $V_{DD}$  is first applied, the power-on reset circuit sets the output of the LTC2641 to zero-scale (code 0). The LTC2642 powers up to midscale (bipolar zero). Depending on the DAC number of bits, the midscale code is: 32,768 (LTC2642-16); 8,192 (LTC2642-14); or 2,048 (LTC2642-12).

### Clearing the DAC

A low pulse meeting the  $t_9$  (minimum) specification on the  $\overline{CLR}$  pin asynchronously clears the DAC latch to code zero (LTC2641) or to midscale (LTC2642).

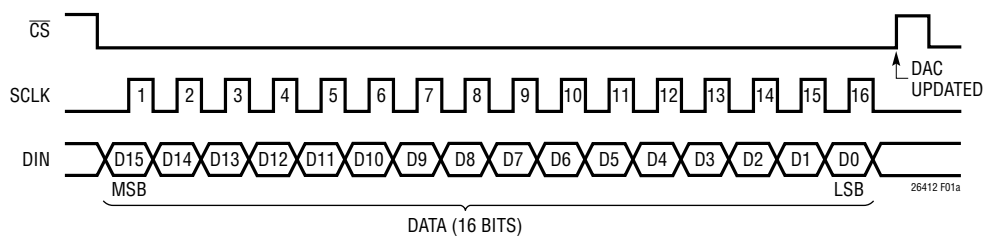


Figure 1a. 16-Bit Timing Diagram (LTC2641-16/LTC2642-16)

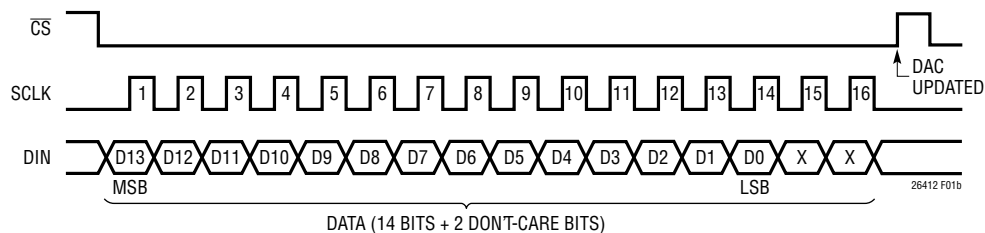


Figure 1b. 14-Bit Timing Diagram (LTC2641-14/LTC2642-14)

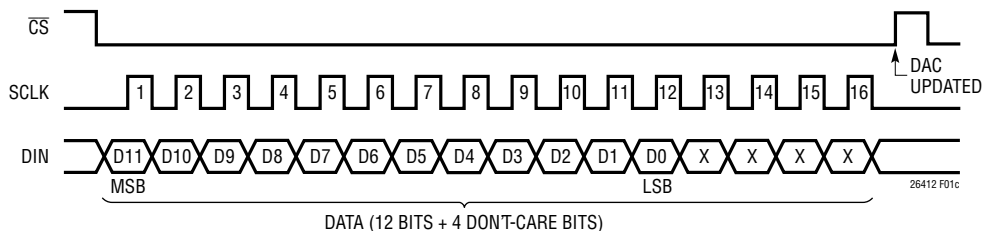


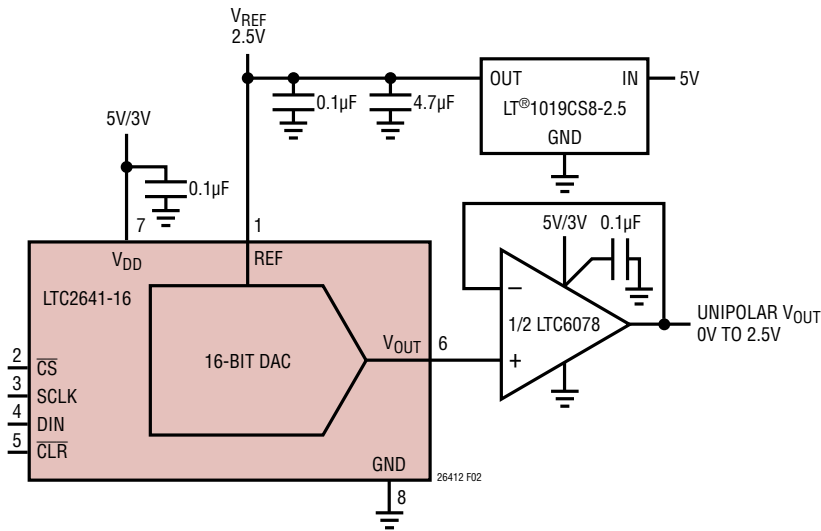
Figure 1c. 12-Bit Timing Diagram (LTC2641-12/LTC2642-12)

## APPLICATIONS INFORMATION

### Unipolar Configuration

Figure 2 shows a typical unipolar DAC application for the LTC2641. Tables 1a, 1b and 1c show the unipolar binary code tables for 16-bit, 14-bit and 12-bit operation.

The external amplifier provides a unity-gain buffer. The LTC2642 can also be used in unipolar configuration by tying  $R_{FB}$  and  $INV$  to  $REF$ . This provides power-up and clear to midscale.



**Table 1a. 16-Bit Unipolar Binary Code Table (LTC2641-16)**

DIGITAL INPUT BINARY NUMBER IN DAC LATCH		ANALOG OUTPUT ( $V_{OUT}$ )
MSB	LSB	
1111	1111 1111	$V_{REF}$ (65,535/65,536)
1000	0000 0000	$V_{REF}$ (32,768/65,536) = $V_{REF}/2$
0000	0000 0001	$V_{REF}$ (1/65,536)
0000	0000 0000	0V

**Figure 2. 16-Bit Unipolar Output (LTC2641-16) Unipolar  $V_{OUT}$  = 0V to  $V_{REF}$**

**Table 1b. 14-Bit Unipolar Binary Code Table (LTC2641-14)**

DIGITAL INPUT BINARY NUMBER IN DAC LATCH		ANALOG OUTPUT ( $V_{OUT}$ )
MSB	LSB	
1111	1111 11xx	$V_{REF}$ (16,383/16,384)
1000	0000 00xx	$V_{REF}$ (8,192/16,384) = $V_{REF}/2$
0000	0000 01xx	$V_{REF}$ (1/16,384)
0000	0000 00xx	0V

**Table 1c. 12-Bit Unipolar Binary Code Table (LTC2641-12)**

DIGITAL INPUT BINARY NUMBER IN DAC LATCH		ANALOG OUTPUT ( $V_{OUT}$ )
MSB	LSB	
1111	1111 xxxx	$V_{REF}$ (4,095/4,096)
1000	0000 xxxx	$V_{REF}$ (2,048/4,096) = $V_{REF}/2$
0000	0001 xxxx	$V_{REF}$ (1/4,096)
0000	0000 xxxx	0V

## APPLICATIONS INFORMATION

### Bipolar Configuration

Figure 3 shows a typical bipolar DAC application for the LTC2642. The on-chip bipolar offset/gain resistors,  $R_{FB}$  and  $R_{INV}$ , are connected to an external amplifier to produce a bipolar output swing from  $-V_{REF}$  to  $V_{REF}$  at the  $R_{FB}$  pin.

The amplifier circuit provides a gain of +2 from the  $V_{OUT}$  pin, and gain of  $-1$  from  $V_{REF}$ . Tables 2a, 2b and 2c show the bipolar offset binary code tables for 16-bit, 14-bit and 12-bit operation.

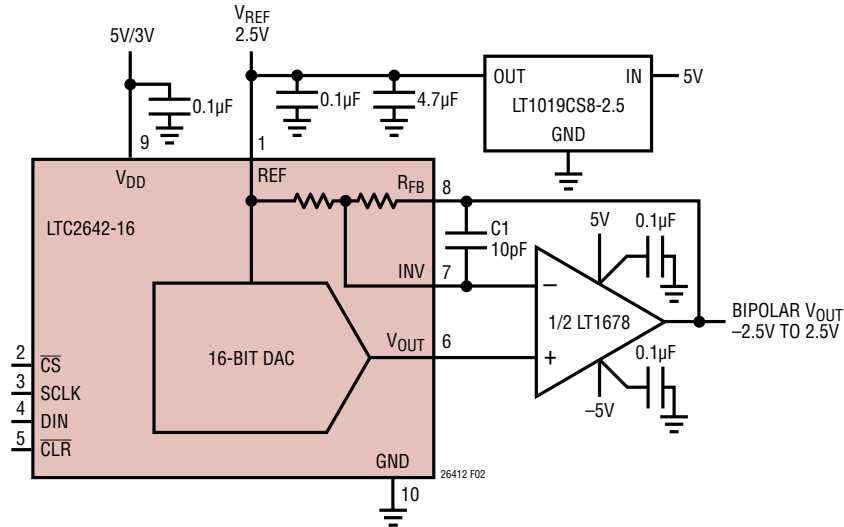


Figure 3. 16-Bit Bipolar Output (LTC2642-16)  $V_{OUT} = -V_{REF}$  to  $V_{REF}$

Table 2a. 16-Bit Bipolar Offset Binary Code Table (LTC2642-16)

DIGITAL INPUT BINARY NUMBER IN DAC LATCH		ANALOG OUTPUT ( $V_{OUT}$ )
MSB	LSB	
1111 1111 1111 1111		$V_{REF}$ (32,767/32,768)
1000 0000 0000 0001		$V_{REF}$ (1/32,768)
1000 0000 0000 0000		0V
0111 1111 1111 1111		$-V_{REF}$ (1/32,768)
0000 0000 0000 0000		$-V_{REF}$

Table 2b. 14-Bit Bipolar Offset Binary Code Table (LTC2642-14)

DIGITAL INPUT BINARY NUMBER IN DAC LATCH		ANALOG OUTPUT ( $V_{OUT}$ )
MSB	LSB	
1111 1111 1111 11xx		$V_{REF}$ (8,191/8,192)
1000 0000 0000 01xx		$V_{REF}$ (1/8,192)
1000 0000 0000 00xx		0V
0111 1111 1111 11xx		$-V_{REF}$ (1/8,192)
0000 0000 0000 00xx		$-V_{REF}$

Table 2c. 12-Bit Bipolar Offset Binary Code Table (LTC2642-12)

DIGITAL INPUT BINARY NUMBER IN DAC LATCH		ANALOG OUTPUT ( $V_{OUT}$ )
MSB	LSB	
1111 1111 1111 xxxx		$V_{REF}$ (2,047/2,048)
1000 0000 0001 xxxx		$V_{REF}$ (1/2,048)
1000 0000 0000 xxxx		0V
0111 1111 1111 xxxx		$-V_{REF}$ (1/2048)
0000 0000 0000 xxxx		$-V_{REF}$

## APPLICATIONS INFORMATION

### Unbuffered Operation and $V_{OUT}$ Loading

The DAC output is available directly at the  $V_{OUT}$  pin, which swings from GND to  $V_{REF}$ . Unbuffered operation provides the lowest possible offset, full-scale and linearity errors, the fastest settling time and minimum power consumption.

However, unbuffered operation requires that appropriate loading be maintained on the  $V_{OUT}$  pin. The LTC2641/LTC2642  $V_{OUT}$  can be modeled as an ideal voltage source in series with a source resistance of  $R_{OUT}$ , typically 6.2k (Figure 4). The DAC's linear output impedance allows it to drive medium loads ( $R_L > 60k$ ) without degrading INL or DNL; only the gain error is increased. The gain error (GE) caused by a load resistance,  $R_L$ , (relative to full scale) is:

$$GE = \frac{-1}{1 + \left(\frac{R_{OUT}}{R_L}\right)}$$

In 16-bit LSBs:

$$GE = \frac{-65536}{1 + \left(\frac{R_{OUT}}{R_L}\right)} \text{ [LSB]}$$

$R_{OUT}$  has a low tempco (typically  $< \pm 50\text{ppm}/^\circ\text{C}$ ), and is independent of DAC code. The variation of  $R_{OUT}$ , part-to-part, is typically less than  $\pm 20\%$ .

Note on LSB units:

For the following error descriptions, "LSB" means 16-bit LSB and 65,536 is rounded to 66k.

To convert to 14-bit LSBs (LTC2641-14/LTC2642-14) divide by 4.

To convert to 12-bit LSBs (LTC2641-12/LTC2642-12) divide by 16.

A constant current,  $I_L$ , loading  $V_{OUT}$  will produce an offset of:

$$V_{OFFSET} = -I_L \cdot R_{OUT}$$

For  $V_{REF} = 2.5\text{V}$ , a 16-bit LSB equals  $2.5\text{V}/65,536$ , or  $38\mu\text{V}$ . Since  $R_{OUT}$  is 6.2k, an  $I_L$  of 6nA produces an offset of 1LSB. Therefore, to avoid degrading DAC performance, it is critical to protect the  $V_{OUT}$  pin from any sources of leakage current.

### Unbuffered $V_{OUT}$ Settling Time

The settling time at the  $V_{OUT}$  pin can be closely approximated by a single-pole response where:

$$\tau = R_{OUT} \cdot (C_{OUT} + C_L)$$

(Figure 4). Settling to 1/2LSB at 16-bits requires about 12 time constants ( $\ln(2 \cdot 65,536)$ ). The typical settling time of  $1\mu\text{s}$  corresponds to a time constant of 83ns, and a total ( $C_{OUT} + C_L$ ) of about  $83\text{ns}/6.2\text{k} = 13\text{pF}$ . The internal capacitance,  $C_{OUT}$  is typically 10pF, so an external  $C_L$  of 3pF corresponds to  $1\mu\text{s}$  settling to 1/2LSB.

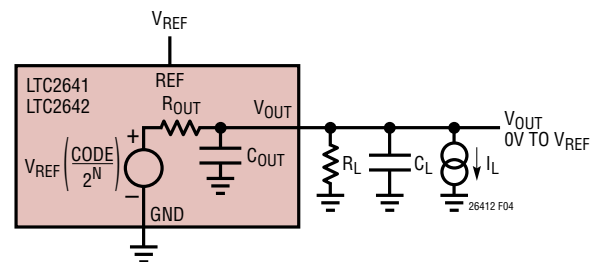


Figure 4.  $V_{OUT}$  Pin Equivalent Circuit

### Op Amp Selection

The optimal choice for an external buffer op amp depends on whether the DAC is used in the unipolar or bipolar mode of operation, and also depends on the accuracy, speed, power dissipation and board area requirements of the application. The LTC2641/LTC2642's combination of tiny package size, rail-to-rail single supply operation, low power dissipation, fast settling and nearly ideal accuracy specifications makes it impractical for one op amp type to fit every application.

In bipolar mode (LTC2642 only), the amplifier operates with the internal resistors to provide bipolar offset and scaling. In this case, a precision amplifier operating from dual power supplies, such as the the LT1678 provides the  $\pm V_{REF}$  output range (Figure 3).

In unipolar mode, the output amplifier operates as a unity gain voltage follower. For unipolar, single supply applications a precision, rail-to-rail input, single supply op amp

## APPLICATIONS INFORMATION

such as the LTC6078 is suitable, if the application does not require linear operation very near to GND, or zero scale (Figure 2). The LTC6078 typically swings to within 1mV of GND if it is not required to sink any load current. For an LSB size of 38 $\mu$ V, 1mV represents 26 missing codes near zero scale. Linearity will be degraded over a somewhat larger range of codes above GND. It is also unavoidable that settling time and transient performance will degrade whenever a single supply amplifier is operated very close to GND, or to the positive supply rail.

The small LSB size of a 16-bit DAC, coupled with the tight accuracy specifications on the LTC2641/LTC2642, means that the accuracy and input specifications for the external op amp are critical for overall DAC performance.

### Op Amp Specifications and Unipolar DAC Accuracy

Most op amp accuracy specifications convert easily to DAC accuracy.

Op amp input bias current on the noninverting (+) input is equivalent to an  $I_L$  loading the DAC  $V_{OUT}$  pin and therefore produces a DAC zero-scale error (ZSE) (see Unbuffered Operation):

$$ZSE = -I_B(IN+) \cdot R_{OUT} \text{ [Volts]}$$

In 16-bit LSBs:

$$ZSE = -I_B(IN+) \cdot 6.2k \cdot \left( \frac{66k}{V_{REF}} \right) \text{ [LSB]}$$

Op amp input impedance,  $R_{IN}$ , is equivalent to an  $R_L$  loading the LTC2641/LTC2642  $V_{OUT}$  pin, and produces a gain error of:

$$GE = \frac{-66k}{1 + \left( \frac{6.2k}{R_{IN}} \right)} \text{ [LSB]}$$

Op amp offset voltage,  $V_{OS}$ , corresponds directly to DAC zero code offset error, ZSE:

$$ZSE = V_{OS} \cdot \frac{66k}{V_{REF}} \text{ [LSB]}$$

Temperature effects also must be considered. Over the  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  industrial temperature range, an offset

voltage temperature coefficient (referenced to  $25^\circ\text{C}$ ) of  $0.6\mu\text{V}/^\circ\text{C}$  will add 1LSB of zero-scale error. Also,  $I_{BIAS}$  and the  $V_{OFFSET}$  error it causes, will typically show significant relative variation over temperature.

Op amp open-loop gain,  $A_{VOL}$ , contributes to DAC gain error (GE):

$$GE = \frac{66k}{A_{VOL}} \text{ [LSB]}$$

Op amp input common mode rejection ratio (CMRR) is an input-referred error that corresponds to a combination of gain error (GE) and INL, depending on the op amp architecture and operating conditions. A conservative estimate of total CMRR error is:

$$\text{Error} = \left( 10^{\left( \frac{CMRR}{20} \right)} \right) \cdot \left( \frac{V_{CMRR\_RANGE}}{V_{REF}} \right) \cdot 66k \text{ [LSB]}$$

where  $V_{CMRR\_RANGE}$  is the voltage range that CMRR (in dB) is specified over. Op amp Typical Performance Characteristics graphs are useful to predict the impact of CMRR errors on DAC performance. Typically, a precision op amp will exhibit a fairly linear CMRR behavior (corresponding to DAC gain error only) over most of the common mode input range (CMR), and become nonlinear and produce significant errors near the edge of the CMR.

Rail-to-rail input op amps are a special case, because they have 2 distinct input stages, one with CMR to GND and the other with CMR to  $V^+$ . This results in a "crossover" CM input region where operation switches between the two input stages.

The LTC6078 rail-to-rail input op amp typically exhibits remarkably low crossover linearity error, as shown in the  $V_{OS}$  vs  $V_{CM}$  Typical Performance Characteristics graphs (see the LTC6078 data sheet). Crossover occurs at CM inputs about 1V below  $V^+$ , and an LTC6078 operating as a unipolar DAC buffer with  $V_{REF} = 2.5\text{V}$  and  $V^+ = 5\text{V}$  will typically add only about 1LSB of GE and almost no INL error due to CMRR. Even in a full rail-to-rail application, with  $V_{REF} = V^+ = 5\text{V}$ , a typical LTC6078 will add only about 1LSB of INL at 16-bits.



## APPLICATIONS INFORMATION

### Op Amp Specifications and Bipolar DAC Accuracy

The op amp contributions to unipolar DAC error discussed above apply equally to bipolar operation. The bipolar application circuit gains up the DAC span, and all errors, by a factor of 2. Since the LSB size also doubles, the errors in LSBs are identical in unipolar and bipolar modes.

One added error in bipolar mode comes from  $I_B$  ( $IN^-$ ), which flows through  $R_{FB}$  to generate an offset. The full bias current offset error becomes:

$$V_{\text{OFFSET}} = (I_B (IN^-) \cdot R_{FB} - I_B (IN^+) \cdot R_{\text{OUT}} \cdot 2) \text{ [Volts]}$$

So:

$$V_{\text{OFFSET}} = (I_B (IN^-) \cdot 28k - I_B (IN^+) \cdot 12.4k) \cdot \frac{33k}{V_{\text{REF}}} \text{ [LSB]}$$

### Settling Time with Op Amp Buffer

When using an external op amp, the output settling time will still include the single pole settling on the LTC2641/LTC2642  $V_{\text{OUT}}$  node, with time constant  $R_{\text{OUT}} \cdot (C_{\text{OUT}} + C_L)$  (see Unbuffered  $V_{\text{OUT}}$  Settling Time).  $C_L$  will include the buffer input capacitance and PC board interconnect capacitance.

The external buffer amplifier adds another pole to the output response, with a time constant equal to  $(f_{\text{bandwidth}}/2\pi)$ . For example, assume that  $C_L$  is maintained at the same value as above, so that the  $V_{\text{OUT}}$  node time constant is  $83\text{ns} = 1\mu\text{s}/12$ . The output amplifier pole will also have a time constant of  $83\text{ns}$  if the closed-loop bandwidth equals  $(1/2\pi \cdot 83\text{ns}) = 1.9\text{MHz}$ . The effective time constant of two cascaded single-pole sections is approximately the root square sum of the individual time constants, or  $\sqrt{2} \cdot 83\text{ns} = 117\text{ns}$ , and  $1/2$  LSB settling time will be  $\sim 12 \cdot 117\text{ns} = 1.4\mu\text{s}$ . This represents an ideal case, with no slew limiting and ideal op amp phase margin. In practice, it will take a considerably faster amplifier, as well as careful attention to maintaining good phase margin, to approach the unbuffered settling time of  $1\mu\text{s}$ .

The output settling time for bipolar applications (Figure 3) will be somewhat increased due to the feedback resistor network  $R_{FB}$  and  $R_{\text{INV}}$  (each  $28k$  nominal). The parasitic capacitance,  $C_P$ , on the op amp ( $-$ ) input node

will introduce a feedback loop pole with a time constant of  $(C_P \cdot 28k/2)$ . A small feedback capacitor,  $C_1$ , should be included, to introduce a zero that will partially cancel this pole.  $C_1$  should nominally be  $< C_P$ , typically in the range of  $5\text{pF}$  to  $10\text{pF}$ . This will restore the phase margin and improve coarse settling time, but a pole-zero doublet will unavoidably leave a slower settling tail, with a time constant of roughly  $(C_P + C_1) \cdot 28k/2$ , which will limit 16-bit settling time to be greater than  $2\mu\text{s}$ .

### Reference and GND Input

The LTC2641/LTC2642 operates with external voltage references from  $2V$  to  $V_{DD}$ , and linearity, offset and gain errors are virtually unchanged vs  $V_{\text{REF}}$ . Full 16-bit performance can be maintained if appropriate guidelines are followed when selecting and applying the reference. The LTC2641/LTC2642's very low gain error tempco of  $0.1\text{ppm}/^\circ\text{C}$ , typical, corresponds to less than  $0.5\text{LSB}$  variation over the  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  temperature range. In practice, this means that the overall gain error tempco will be determined almost entirely by the external reference tempco.

The DAC voltage-switching mode "inverted" resistor ladder architecture used in the LTC2641/LTC2642 exhibits a reference input resistance ( $R_{\text{REF}}$ ) that is code dependent (see the Typical Performance curves  $I_{\text{REF}}$  vs Input Code).

In unipolar mode, the minimum  $R_{\text{REF}}$  is  $14.8k$  (at code  $871\text{Chex}$ ,  $34,588$  decimal) and the the maximum  $R_{\text{REF}}$  is  $300k$  at code  $0000\text{hex}$  (zero scale). The maximum change in  $I_{\text{REF}}$  for a  $2.5V$  reference is  $160\mu\text{A}$ . Since the maximum occurs near midscale, the INL error is about one half of the change on  $V_{\text{REF}}$ , so maintaining an INL error of  $< 0.1\text{LSB}$  requires a reference load regulation of  $(1.53\text{ppm} \cdot 2/160\mu\text{A}) = 19 \text{ [ppm/mA]}$ . This implies a reference output impedance of  $48\text{m}\Omega$ , including series wiring resistance.

To prevent output glitches from occurring when resistor ladder branches switch from GND to  $V_{\text{REF}}$ , the reference input must maintain low impedance at higher frequencies. A  $0.1\mu\text{F}$  ceramic capacitor with short leads between REF and GND provides high frequency bypassing. A surface mount ceramic chip capacitor is preferred because it has the lowest inductance. An additional  $1\mu\text{F}$  between REF and GND provides low frequency bypassing. The circuit

## APPLICATIONS INFORMATION

will benefit from even higher bypass capacitance, as long as the external reference remains stable with the added capacitive loading.

### Digital Inputs and Interface Logic

All of the digital inputs include Schmitt-trigger buffers to accept slow transition interfaces. This means that optocouplers can interface directly to the LTC2641/LTC2642 without additional external logic. Digital input hysteresis is typically 150mV.

The digital inputs are compatible with TTL/CMOS-logic levels. However, rail-to-rail (CMOS) logic swings are preferred, because operating the logic inputs away from the supply rails generates additional  $I_{DD}$  and GND current, (see Typical Performance Characteristic graph Supply Current vs Logic Input Voltage).

Digital feedthrough is only 0.2nV•s typical, but it is always preferred to keep all logic inputs static except when loading a new code into the DAC.

### Board Layout for Precision

Even a small amount of board leakage can degrade accuracy. The 6nA leakage current into  $V_{OUT}$  needed to generate 1LSB offset error corresponds to 833M $\Omega$  leakage resistance from a 5V supply.

The  $V_{OUT}$  node is relatively sensitive to capacitive noise coupling, so minimum trace length, appropriate shielding and clean board layout are imperative here.

Temperature differences at the DAC, op amp or reference pins can easily generate tens of microvolts of thermocouple voltages. Analog signal traces should be short, close together and away from heat dissipating components. Air currents across the board can also generate thermocouples.

The PC board should have separate areas for the analog and digital sections of the circuit. A single, solid ground plane

should be used, with analog and digital signals carefully routed over separate areas of the plane. This keeps digital signals away from sensitive analog signals and minimizes the interaction between digital ground currents and the analog section of the ground plane.

A “star ground” area should be established by attaching the LTC2641/LTC2642 GND pin,  $V_{REF}$  GND and the DAC  $V_{OUT}$  GND reference terminal to the same area on the GND plane. Care should be taken to ensure that no large GND return current paths flow through the “star GND” area. In particular, the resistance from the LTC2641 GND pin to the point where the  $V_{REF}$  input source connects to the ground plane should be as low as possible. Excessive resistance here will be multiplied by the code dependent  $I_{REF}$  current to produce an INL error similar to the error produced by  $V_{REF}$  source resistance. For the LTC2641 in the S8 package both GND pins, Pin 2 and Pin 7 should be tied to the same GND plane.

Sources of ground return current in the analog area include op amp power supply bypass capacitors and the GND connection for single supply amps. A useful technique for minimizing errors is to use a separate board layer for power ground return connections, and reserve one ground plane layer for low current “signal” GND connections. The “signal”, or “star” GND plane must be connected to the “power” GND plane at a single point, which should be located near the LTC2641/LTC2642 GND pin.

If separate analog and digital ground areas exist it is necessary to connect them at a single location, which should be fairly close to the DAC for digital signal integrity. In some systems, large GND return currents can flow between the digital and analog GNDs, especially if different PC boards are involved. In such cases the digital and analog ground connection point should not be made right at the “star” GND area, so the highly sensitive analog signals are not corrupted. If forced to choose, always place analog ground quality ahead of digital signal ground. (A few mV of noise

## APPLICATIONS INFORMATION

on the digital inputs is imperceptible, thanks to the digital input hysteresis)

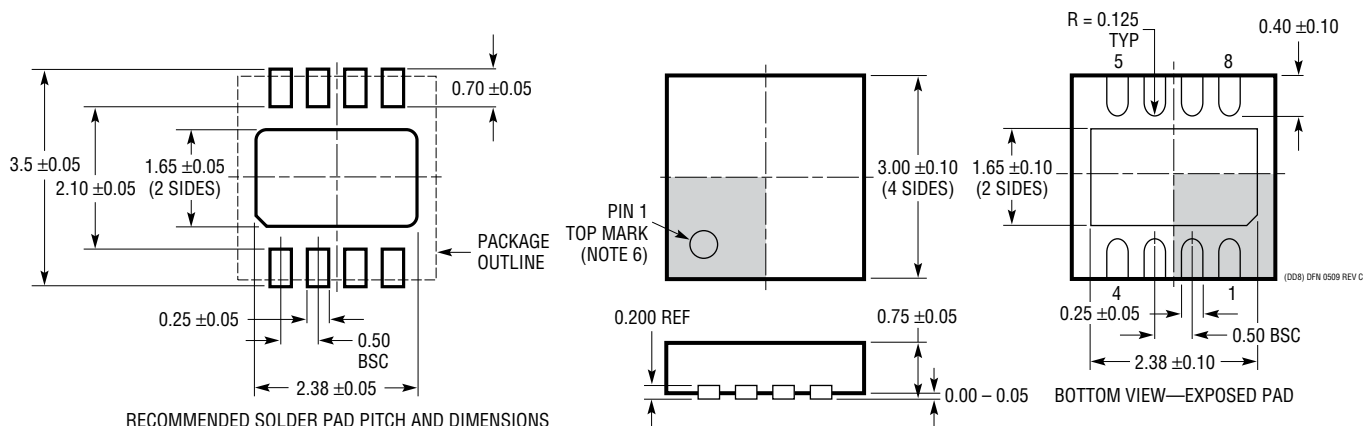
Just by maintaining separate areas on the GND plane where analog and digital return currents naturally flow, good results are generally achieved. Only after this has been done, it is sometimes useful to interrupt the ground plane with strategically placed “slots”, to prevent the digital ground currents from fringing into the analog portion of the plane. When doing this, the gap in the plane should be only as long as it needs to be to serve its purpose.

Caution: if a GND plane gap is improperly placed, so that it interrupts a significant GND return path, or if a signal traces crosses over the gap, then adding the gap may greatly degrade performance! In this case, the GND and signal return currents are forced to flow the long way around the gap, and then are typically channeled directly into the most sensitive area of the analog GND plane.

## PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

**DD Package**  
**8-Lead Plastic DFN (3mm × 3mm)**  
 (Reference LTC DWG # 05-08-1698 Rev C)



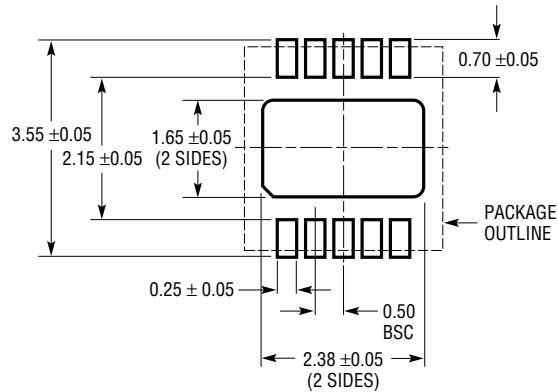
**NOTE:**

1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

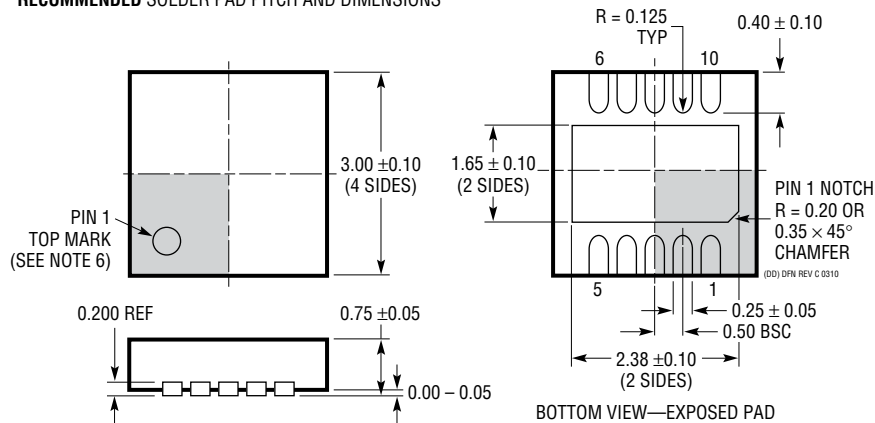
## PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

### DD Package 10-Lead Plastic DFN (3mm × 3mm) (Reference LTC DWG # 05-08-1699 Rev C)



#### RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



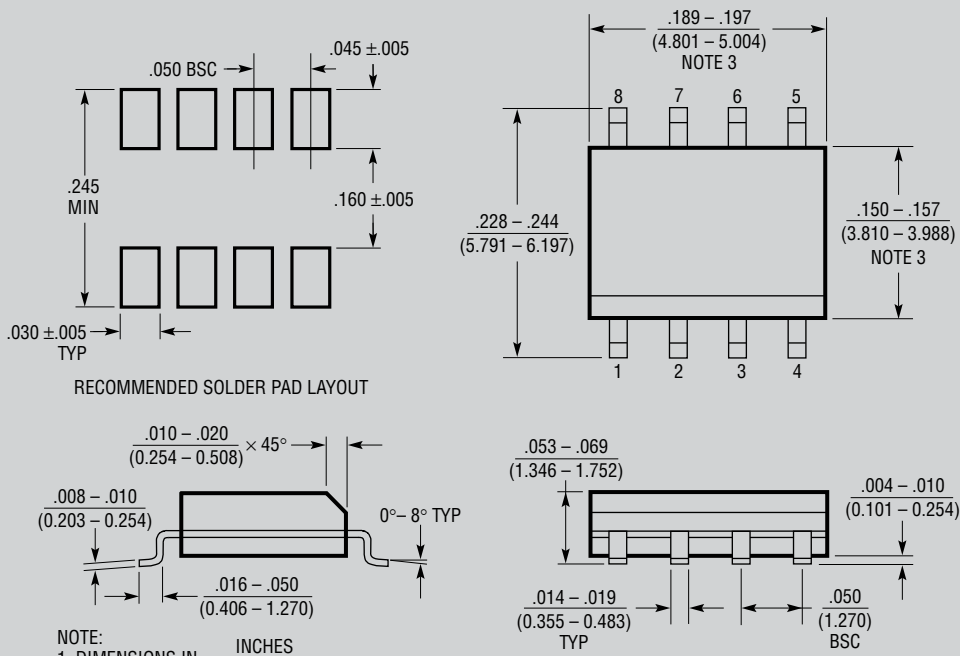
#### NOTE:

1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2).  
CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

# PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

## S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610 Rev G)



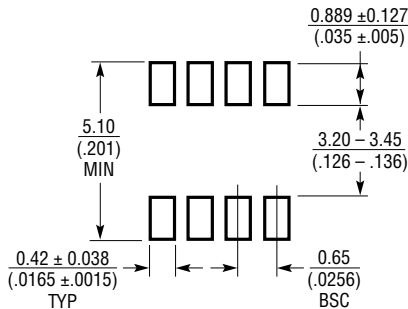
- NOTE:
1. DIMENSIONS IN INCHES (MILLIMETERS)
  2. DRAWING NOT TO SCALE
  3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED  $.006^\circ$  (0.15mm)
  4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

S08 REV G 0212

**OBsolete PACKAGE**

## PACKAGE DESCRIPTION

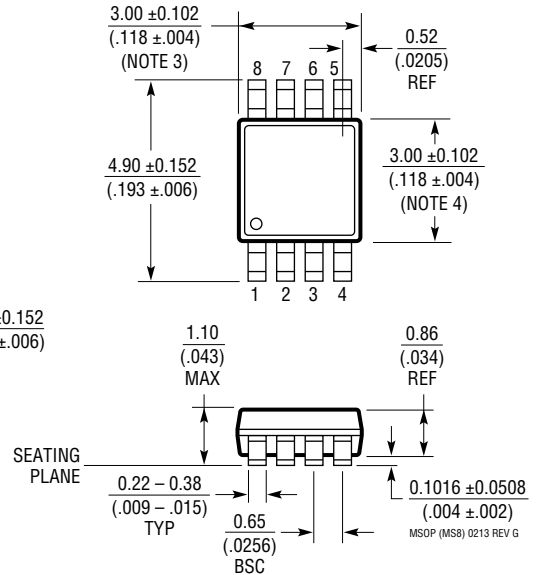
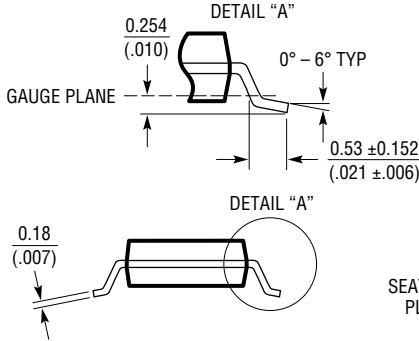
**MS8 Package**  
**8-Lead Plastic MSOP**  
 (Reference LTC DWG # 05-08-1660 Rev G)



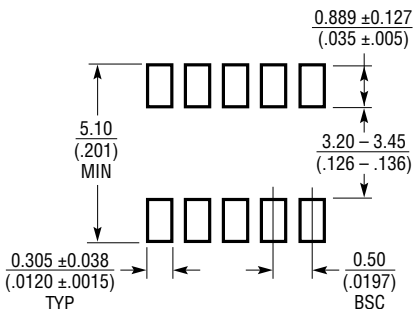
RECOMMENDED SOLDER PAD LAYOUT

NOTE:

1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.  
 MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.  
 INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX



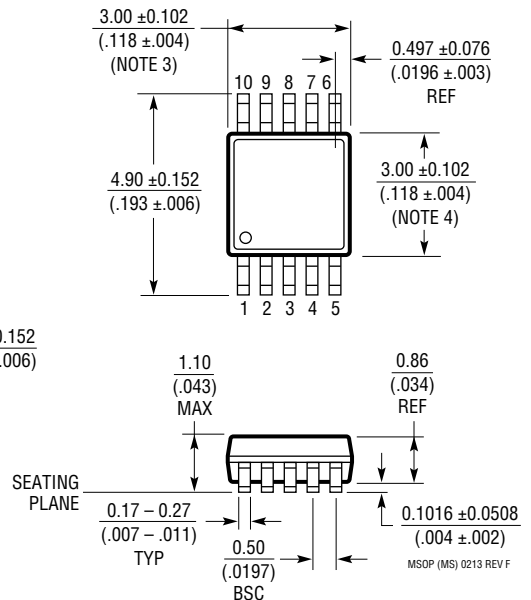
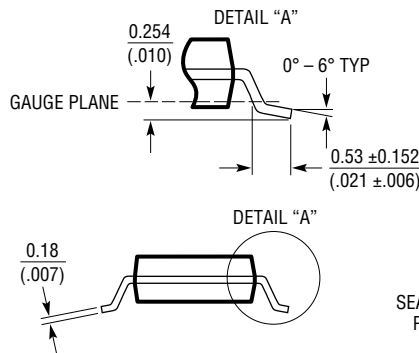
**MS Package**  
**10-Lead Plastic MSOP**  
 (Reference LTC DWG # 05-08-1661 Rev F)



RECOMMENDED SOLDER PAD LAYOUT

NOTE:

1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.  
 MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.  
 INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX



**REVISION HISTORY** (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	12/13	Marked S8 package as Obsolete	2, 3, 9, 10, 18, 21
D	10/14	Added output voltage noise density specifications Updated text under Clearing the DAC section	4 12