



**ABSOLUTE MAXIMUM RATINGS**

(Note 1,7)

$V_{DCIN}, V_{USBIN}$	
$t < 1ms$ and Duty Cycle $< 1\%$ .....	-0.3V to 7V
Steady State .....	-0.3V to 6V
BAT, CHRG, NTC, HPWR, SUSP .....	-0.3V to 6V
IDC, IUSB, ITERM .....	-0.3V to $V_{CC} + 0.3V$
BAT Short-Circuit Duration .....	Continuous
VNTC Short-Circuit Duration .....	Continuous
DCIN, BAT Pin Current (Note 6) .....	1.25A
USBIN Pin Current (Note 6) .....	1.1A
IDC, IUSB, ITERM Pin Current .....	1.25mA
Junction Temperature .....	125°C
Operating Temperature Range (Note 2) ...	-40°C to 85°C
Storage Temperature Range .....	-65°C to 125°C

**PACKAGE/ORDER INFORMATION**

TOP VIEW

DDB PACKAGE  
12-LEAD (3mm x 2mm) PLASTIC DFN  
 $T_{JMAX} = 125^{\circ}C, \theta_{JA} = 60^{\circ}C/W$  (Note 3)  
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB

ORDER PART NUMBER	DDB PART MARKING
LTC4097EDDB	LCRM

**Order Options** Tape and Reel: Add #TR  
Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF  
Lead Free Part Marking: <http://www.linear.com/leadfree/>

Consult LTC Marketing for parts specified with wider operating temperature ranges.

**ELECTRICAL CHARACTERISTICS**

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^{\circ}C$ .  $V_{DCIN} = 5V, V_{USBIN} = 5V, HPWR = 5V, NTC = 0V, R_{IDC} = 1k\Omega, R_{IUSB} = 2k\Omega, R_{ITERM} = 2k\Omega$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{DCIN}$	Adapter Supply Voltage		● 4.25		5.5	V
$V_{USBIN}$	USB Supply Voltage		● 4.25		5.5	V
$I_{DCIN}$	DCIN Supply Current	Charge Mode (Note 4), $R_{IDC} = 10k$ Standby Mode; Charge Terminated Shutdown Mode (SUSP = 5V)	●	250	800	$\mu A$
			●	50	100	$\mu A$
				20	40	$\mu A$
$I_{USBIN}$	USBIN Supply Current	Charge Mode (Note 5), $R_{IUSB} = 10k, V_{DCIN} = 0V$ Standby Mode; Charge Terminated, $V_{DCIN} = 0V$ Shutdown ( $V_{DCIN} = 0V, SUSP = 5V$ ) $V_{DCIN} > V_{USBIN}$	●	250	800	$\mu A$
			●	50	100	$\mu A$
				20	40	$\mu A$
				10	20	$\mu A$
$V_{FLOAT}$	Regulated Output (Float) Voltage	$I_{BAT} = 1mA$ $I_{BAT} = 1mA, 0^{\circ}C < T_A < 85^{\circ}C$	4.179	4.2	4.221	V
			4.158	4.2	4.242	V
$I_{BAT}$	BAT Pin Current	$R_{IDC} = 1.25k$ , Constant-Current Mode $R_{IUSB} = 2.1k$ , Constant-Current Mode $R_{IUSB} = 2.1k$ , Constant-Current Mode, HPWR = 0V $R_{IDC} = 10k$ or $R_{IUSB} = 10k$ Standby Mode, Charge Terminated Shutdown Mode (Charger Disabled) Sleep Mode ( $V_{DCIN} = 0V, V_{USBIN} = 0V$ )	750	800	850	mA
			450	476	500	mA
			90	95	100	mA
			88	100	112	mA
				-5	-8	$\mu A$
				-2	-4	$\mu A$
				-5	-8	$\mu A$
$V_{IDC}$	IDC Pin Regulated Voltage	Constant-Current Mode, $R_{IDC} = 1.25k$		1		V
$V_{IUSB}$	IUSB Pin Regulated Voltage	Constant-Current Mode, $R_{IUSB} = 2k$ Constant-Current Mode, $R_{IUSB} = 2k, HPWR = 0$		1		V
				0.2		V
$I_{TERMINATE}$	Charge Current Termination Threshold	$R_{ITERM} = 1k$ $R_{ITERM} = 2k$ $R_{ITERM} = 10k$	88	100	112	mA
			42	50	58	mA
			6	9.5	13	mA
$I_{TRIKL}$	Trickle Charge Current	$V_{BAT} < V_{TRIKL}; R_{IDC} = 1k$ $V_{BAT} < V_{TRIKL}; R_{IUSB} = 2k$	85	100	115	mA
			42	50	58	mA

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{\text{DCIN}} = 5\text{V}$ ,  $V_{\text{USBIN}} = 5\text{V}$ ,  $\text{HPWR} = 5\text{V}$ ,  $\text{NTC} = 0\text{V}$ ,  $R_{\text{IDC}} = 1\text{k}\Omega$ ,  $R_{\text{IUSB}} = 2\text{k}\Omega$ ,  $R_{\text{ITERM}} = 2\text{k}\Omega$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{\text{TRIKL}}$	Trickle Charge Threshold Voltage	$V_{\text{BAT}}$ Rising Hysteresis	● 2.8	2.9 135	3	V mV
$V_{\text{UVDC}}$	DCIN Undervoltage Lockout Voltage	From Low to High Hysteresis	4	4.22 200	4.4	V mV
$V_{\text{UVUSB}}$	USBIN Undervoltage Lockout Voltage	From Low to High Hysteresis	3.8	4 200	4.2	V mV
$V_{\text{ASD-DC}}$	$V_{\text{DCIN}} - V_{\text{BAT}}$ Lockout Threshold Voltage	$V_{\text{DCIN}}$ from High to Low, $V_{\text{BAT}} = 4.3\text{V}$ $V_{\text{DCIN}}$ from Low to High, $V_{\text{BAT}} = 4.3\text{V}$	5	30 100	55	mV mV
$V_{\text{ASD-USB}}$	$V_{\text{USBIN}} - V_{\text{BAT}}$ Lockout Threshold Voltage	$V_{\text{USBIN}}$ from High to Low, $V_{\text{BAT}} = 4.3\text{V}$ $V_{\text{USBIN}}$ from Low to High, $V_{\text{BAT}} = 4.3\text{V}$	5	30 150	55	mV mV
$V_{\text{SUSP}}, V_{\text{HPWR}}$	$V_{\text{IL}}$ , Logic Low Voltage				0.5	V
	$V_{\text{IH}}$ , Logic High Voltage		1.2			V
$R_{\text{SUSP}}$	SUSP Pulldown Resistance		●	3.4		$\text{M}\Omega$
$R_{\text{HPWR}}$	HPWR Pulldown Resistance		●	3.4		$\text{M}\Omega$
$V_{\text{CHRG}}$	CHRG Output Low Voltage	$I_{\text{CHRG}} = 5\text{mA}$	●	62	150	mV
$\Delta V_{\text{RECHRG}}$	Recharge Battery Threshold Voltage	$V_{\text{FLOAT}} - V_{\text{RECHRG}}$	70	100	130	mV
$t_{\text{RECHRG}}$	Recharge Comparator Filter Time	$V_{\text{BAT}}$ from High to Low		1.6		ms
$t_{\text{TERM}}$	Termination Comparator Filter Time	$I_{\text{BAT}}$ Drops Below Termination Threshold		3		ms
$R_{\text{ON-DC}}$	Power FET "ON" Resistance (Between DCIN and BAT)			420		$\text{m}\Omega$
$R_{\text{ON-USB}}$	Power FET "ON" Resistance (Between USBIN and BAT)			470		$\text{m}\Omega$
$T_{\text{LIM}}$	Junction Temperature in Constant-Temperature Mode			115		$^\circ\text{C}$
$I_{\text{VNTC}}$	VNTC Pin Current	$V_{\text{VNTC}} = 4.55\text{V}$ DCIN Powered $V_{\text{VNTC}} = 4.8\text{V}$ USBIN Powered		30 30		$\text{mA}$ $\text{mA}$
$V_{\text{VNTC}}$	VNTC Bias Voltage	$I_{\text{VNTC}} = 250\mu\text{A}$	4.25		5.5	V
$I_{\text{NTC}}$	NTC Input Leakage Current	$V_{\text{NTC}} = 1\text{V}$		0	$\pm 1$	$\mu\text{A}$
$V_{\text{NTC-COLD}}$	Cold Temperature Fault Threshold Voltage	Rising Threshold Hysteresis		$0.765 \cdot V_{\text{VNTC}}$ $0.016 \cdot V_{\text{VNTC}}$		V V
$V_{\text{NTC-HOT}}$	Hot Temperature Fault Threshold Voltage	Falling Threshold Hysteresis		$0.349 \cdot V_{\text{VNTC}}$ $0.016 \cdot V_{\text{VNTC}}$		V V
$V_{\text{NTC-DIS}}$	NTC Disable Threshold Voltage	NTC Input Voltage to GND (Falling) Hysteresis		$0.017 \cdot V_{\text{VNTC}}$ $0.01 \cdot V_{\text{VNTC}}$		V V

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC4097 is guaranteed to meet the performance specifications from  $0^\circ\text{C}$  to  $85^\circ\text{C}$ . Specifications over the  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  operating temperature range are assured by design, characterization and correlation with statistical process controls.

**Note 3:** Failure to correctly solder the Exposed Pad of the package to the PC board will result in a thermal resistance much higher than  $60^\circ\text{C}/\text{W}$ . See

Thermal Considerations.

**Note 4:** Supply current includes IDC and ITERM pin current (approximately  $100\mu\text{A}$  each) but does not include any current delivered to the battery through the BAT pin.

**Note 5:** Supply current includes IUSB and ITERM pin current (approximately  $100\mu\text{A}$  each) but does not include any current delivered to the battery through the BAT pin.

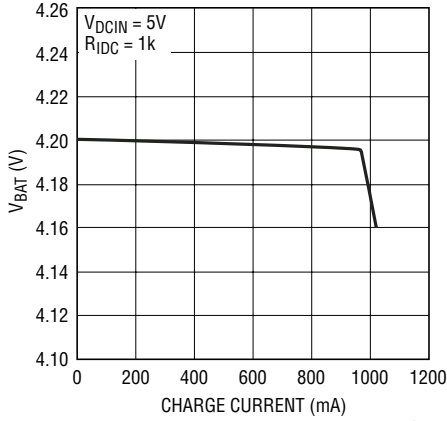
**Note 6:** Guaranteed by long term current density limitations.

**Note 7:**  $V_{\text{CC}}$  is greater of DCIN or USBIN

## TYPICAL PERFORMANCE CHARACTERISTICS

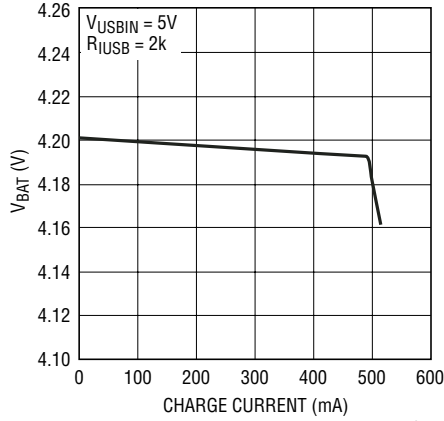
NTC = 0V, HPWR = 5V,  $T_A = 25^\circ\text{C}$ ,  
unless otherwise noted.

**Battery Regulated Output (Float)  
Voltage vs Charge Current**



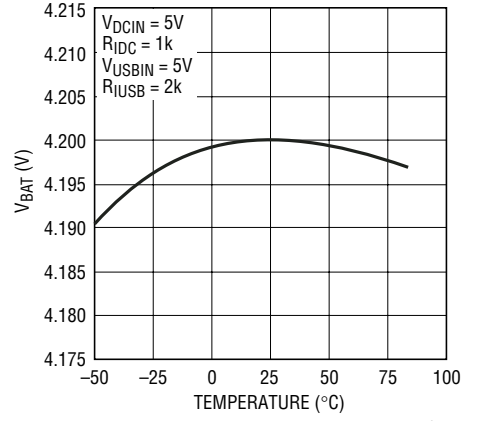
4097 G01

**Battery Regulated Output (Float)  
Voltage vs Charge Current**



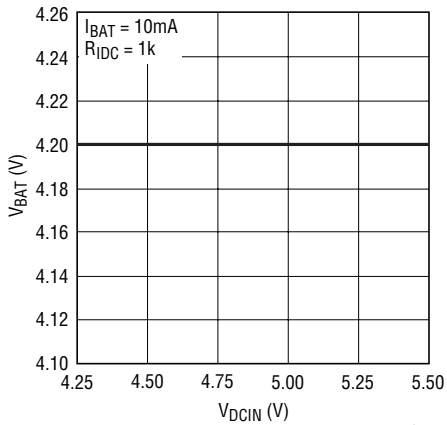
4097 G02

**Battery Regulated Output (Float)  
Voltage vs Temperature**



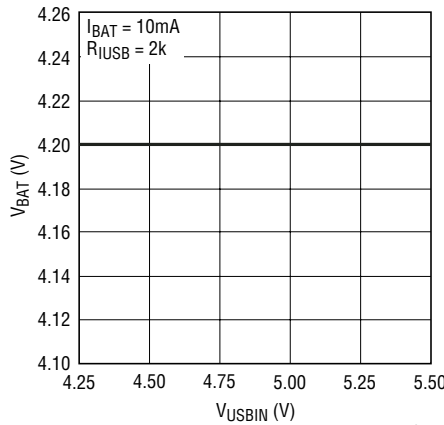
4097 G03

**Battery Regulated Output (Float)  
Voltage vs DCIN Voltage**



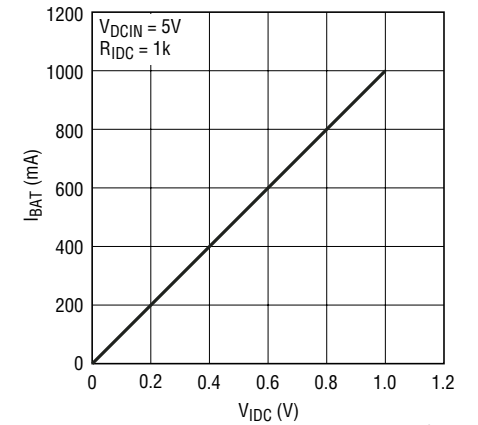
4097 G04

**Battery Regulated Output (Float)  
Voltage vs USBIN Voltage**



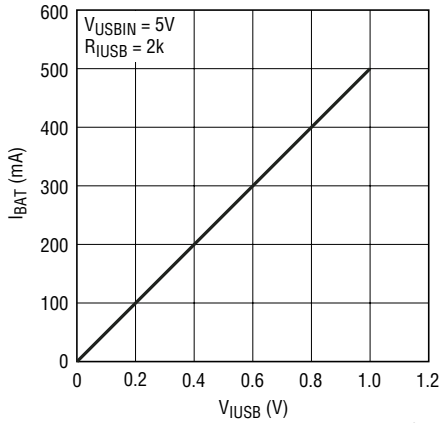
4097 G05

**Charge Current vs IDC Pin  
Voltage**



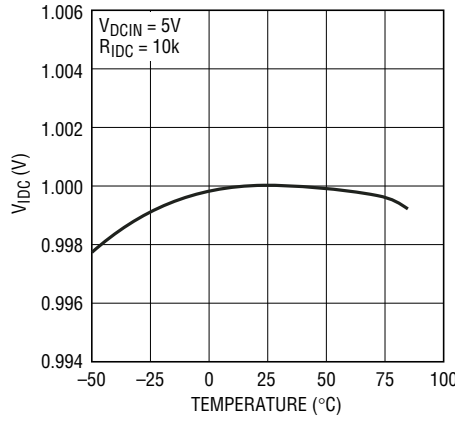
4097 G06

**Charge Current vs IUSB Pin  
Voltage**



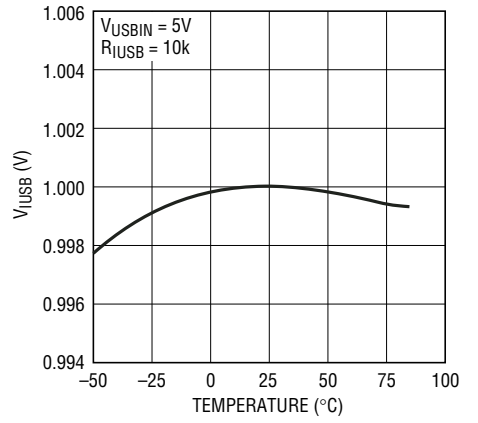
4097 G07

**IDC Pin Voltage vs Temperature  
(Constant-Current Mode)**



4097 G08

**IUSB Pin Voltage vs Temperature  
(Constant-Current Mode)**

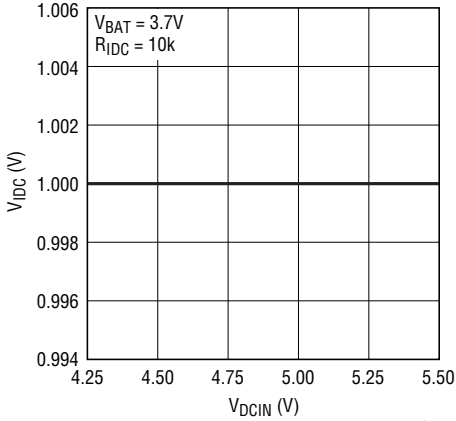


4097 G09

**TYPICAL PERFORMANCE CHARACTERISTICS**

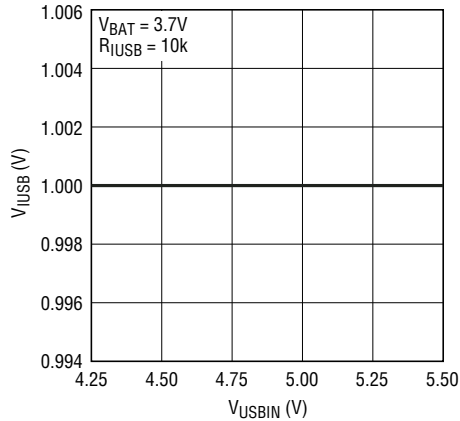
NTC = 0V, HPWR = 5V,  $T_A = 25^\circ\text{C}$ ,  
unless otherwise noted.

**IDC Pin Voltage vs  $V_{\text{DCIN}}$   
(Constant-Current Mode)**



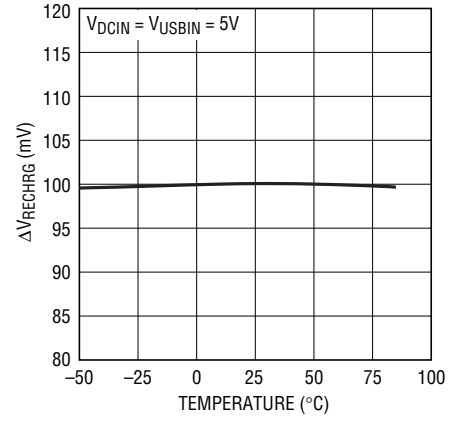
4097 G10

**IUSB Pin Voltage vs  $V_{\text{USBIN}}$   
(Constant-Current Mode)**



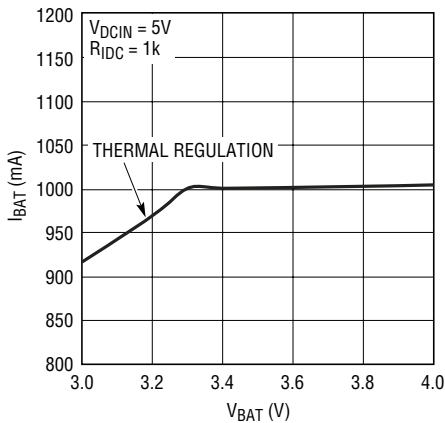
4097 G11

**Recharge Threshold Voltage  
vs Temperature**



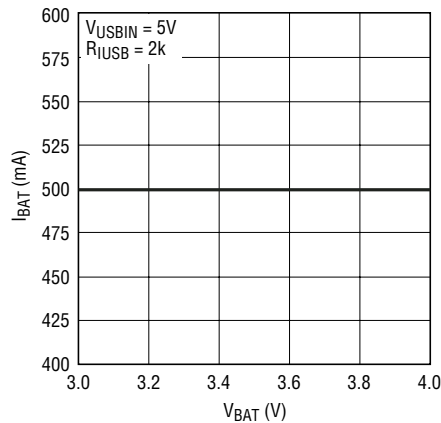
4097 G12

**Charge Current vs Battery Voltage**



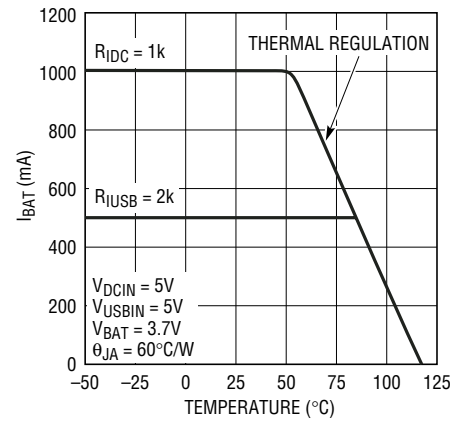
4097 G13

**Charge Current vs Battery Voltage**



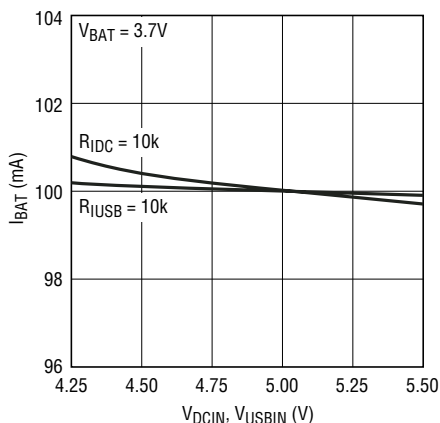
4097 G14

**Charge Current vs Ambient  
Temperature with Thermal  
Regulation**



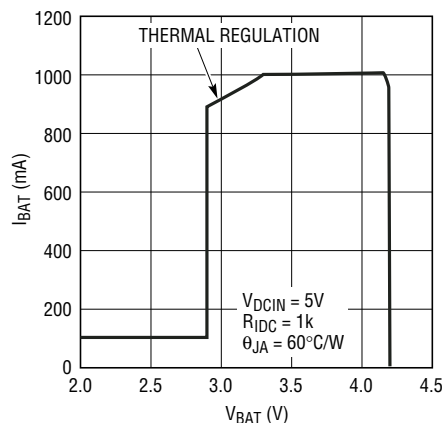
4097 G15

**Charge Current vs Supply Voltage**



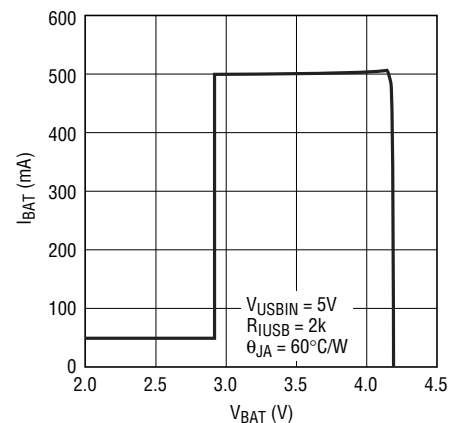
4097 G16

**Charge Current vs Battery Voltage**



4097 G17

**Charge Current vs Battery Voltage**

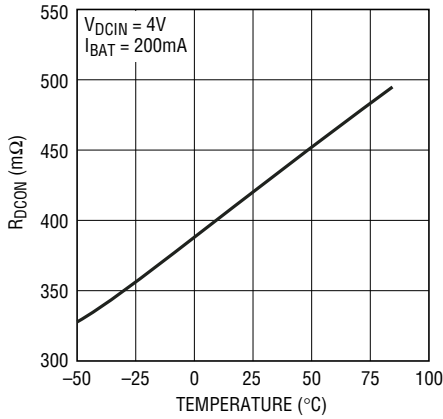


4097 G18

## TYPICAL PERFORMANCE CHARACTERISTICS

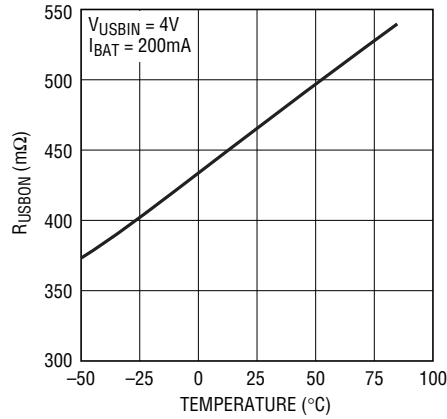
NTC = 0V, HPWR = 5V,  $T_A = 25^\circ\text{C}$ ,  
unless otherwise noted.

**DCIN Power FET On-Resistance vs Temperature**



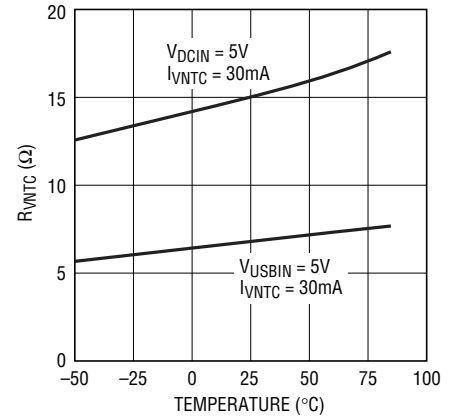
4097 G19

**USBIN Power FET On-Resistance vs Temperature**



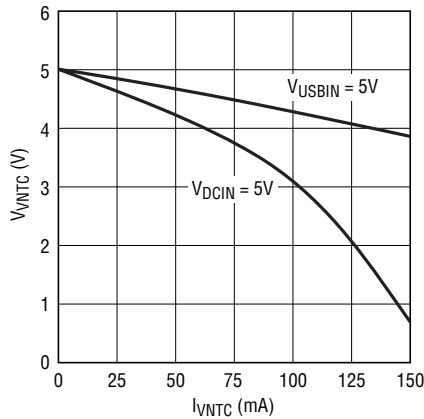
4097 G20

**VNTC-DCIN and VNTC-USBIN Power FET On-Resistance vs Temperature**



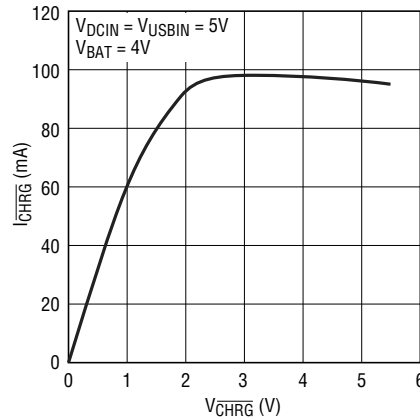
4097 G21

**V\_VNTC vs I\_VNTC**



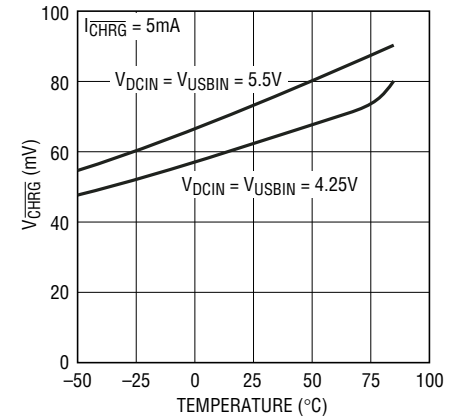
4097 G22

**CHRG Pin I-V Curve**



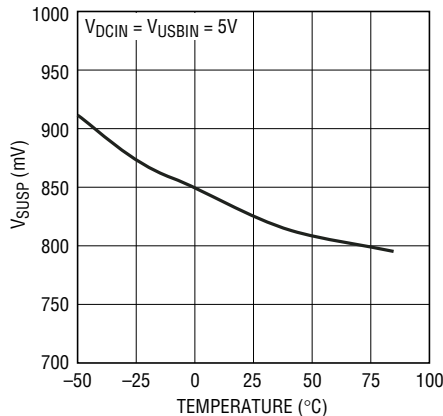
4097 G23

**CHRG Pin Output Low Voltage vs Temperature**



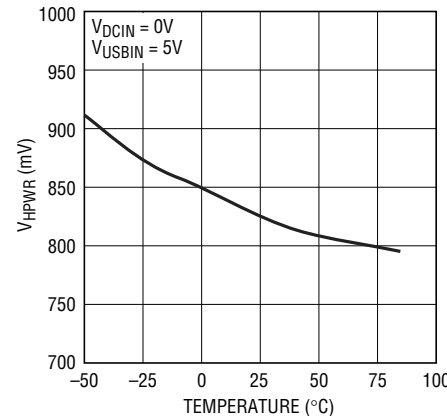
4097 G24

**SUSP Pin Threshold Voltage (On-to-Off) vs Temperature**



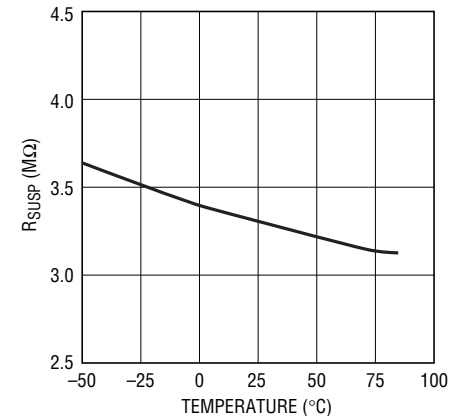
4097 G25

**HPWR Pin Threshold Voltage (On-to-Off) vs Temperature**



4097 G26

**SUSP Pin Pulldown Resistance vs Temperature**

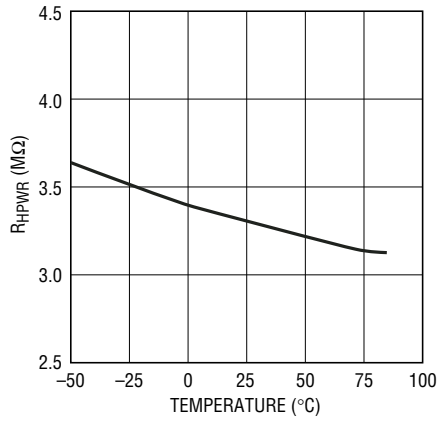


4097 G27

**TYPICAL PERFORMANCE CHARACTERISTICS**

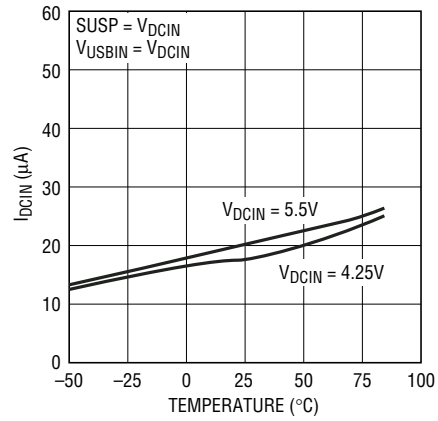
NTC = 0V, HPWR = 5V,  $T_A = 25^\circ\text{C}$ ,  
unless otherwise noted.

**HPWR Pin Pulldown Resistance vs Temperature**



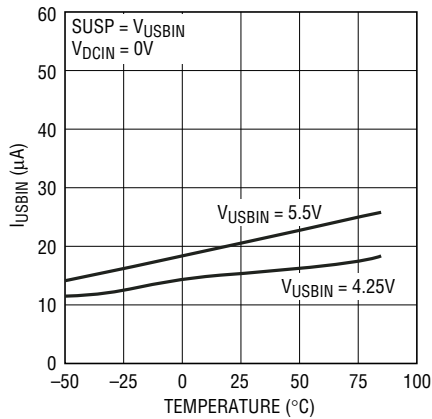
4097 G28

**Shutdown Supply Current vs Temperature and V<sub>DCIN</sub>**



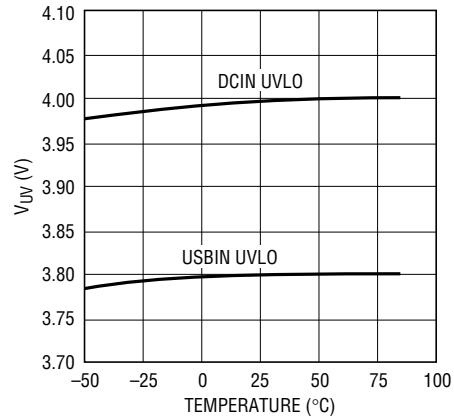
4097 G29

**Shutdown Supply Current vs Temperature and V<sub>USBIN</sub>**



4097 G30

**Undervoltage Lockout Voltage (Falling) vs Temperature**



4097 G31

## PIN FUNCTIONS

**DCIN (Pin 1):** Wall Adapter Input Supply Pin. Provides power to the battery charger. The maximum supply current is 1.2A. This pin should be bypassed with a 1 $\mu$ F capacitor.

**USBIN (Pin 2):** USB Input Supply Pin. Provides power to the battery charger. The maximum supply current is 1A. This pin should be bypassed with a 1 $\mu$ F capacitor.

**VNTC (Pin 3):** Output Bias Voltage for NTC. A resistor from this pin to the NTC pin sets up the bias for an NTC thermistor. When the DCIN or USBIN pin voltage is sufficient to begin charging (i.e. when the DCIN or USBIN supply is greater than the undervoltage lockout thresholds and at least 100mV or 150mV, respectively, above the battery terminal), the VNTC pin is connected to the appropriate input through an internal P-channel MOSFET. If sufficient voltage to charge is not present on DCIN or USBIN the VNTC pin is high impedance. This output can source up to 120mA.

**CHRG (Pin 4):** Open-Drain Charge Status Output. When the LTC4097 is charging, the  $\overline{\text{CHRG}}$  pin is pulled low by an internal N-channel MOSFET. When the charge cycle is completed,  $\overline{\text{CHRG}}$  becomes high impedance. This output can sink up to 10mA, making it suitable for driving a LED.

**SUSP (Pin 5):** Charge Enable Input. A logic low on this pin enables the charger. If left floating, an internal 3.4M $\Omega$  pull-down resistor defaults the LTC4097 to charge mode. Pull this pin high for shutdown.

**NTC (Pin 6):** Input to the NTC (Negative Temperature Coefficient) Thermistor Temperature Monitoring Circuit. For normal operation, connect a thermistor from the NTC pin to ground and a resistor of equal value from the NTC pin to VNTC. When the voltage at this pin drops below  $0.349 \cdot \text{VNTC}$  at hot temperatures or rises above  $0.765 \cdot \text{VNTC}$  at cold, charging is suspended and the  $\overline{\text{CHRG}}$  pin output will keep the state in which it was before the event (low-Z or high-Z). Pulling this pin below  $0.017 \cdot \text{VNTC}$  disables the NTC feature. There is approximately 2°C of temperature hysteresis associated with each of the input comparator's thresholds.

**HPWR (Pin 7):** HPWR Enable Input. Used to control the amount of current drawn from the USB port. A logic high on the HPWR pin sets the charge current to 100% of the current programmed by the IUSB pin. A logic low on the HPWR pin sets the charge current to 20% of the current programmed by the IUSB pin. An internal 3.4M $\Omega$  pull-down resistor defaults the HPWR pin to its low current state.

**ITERM (Pin 8):** Charge Termination Current Threshold Program. The termination current threshold,  $I_{\text{TERMINATE}}$ , is set by connecting a resistor,  $R_{\text{ITERM}}$ , to ground.  $I_{\text{TERMINATE}}$  is set by the following formula:

$$I_{\text{TERMINATE}} = \frac{100\text{V}}{R_{\text{ITERM}}}$$

When the battery current,  $I_{\text{BAT}}$ , falls below the termination threshold, charging stops and the  $\overline{\text{CHRG}}$  output becomes high impedance.



## PIN FUNCTIONS

**IUSB (Pin 9):** Charge Current Program for USB Power. The charge current is set by connecting a resistor,  $R_{IUSB}$ , to ground. When charging in constant current mode, this pin serves to 1V. The voltage on this pin can be used to measure the battery current delivered from the USBIN input using the following formula:

$$I_{BAT} = \frac{V_{IUSB}}{R_{IUSB}} \cdot 1000$$

**IDC (Pin 10):** Charge Current Program for Wall Adapter Power. The charge current is set by connecting a resistor,  $R_{IDC}$ , to ground. When charging in constant current mode, this pin serves to 1V. The voltage on this pin can be used

to measure the battery current delivered from the DCIN input using the following formula:

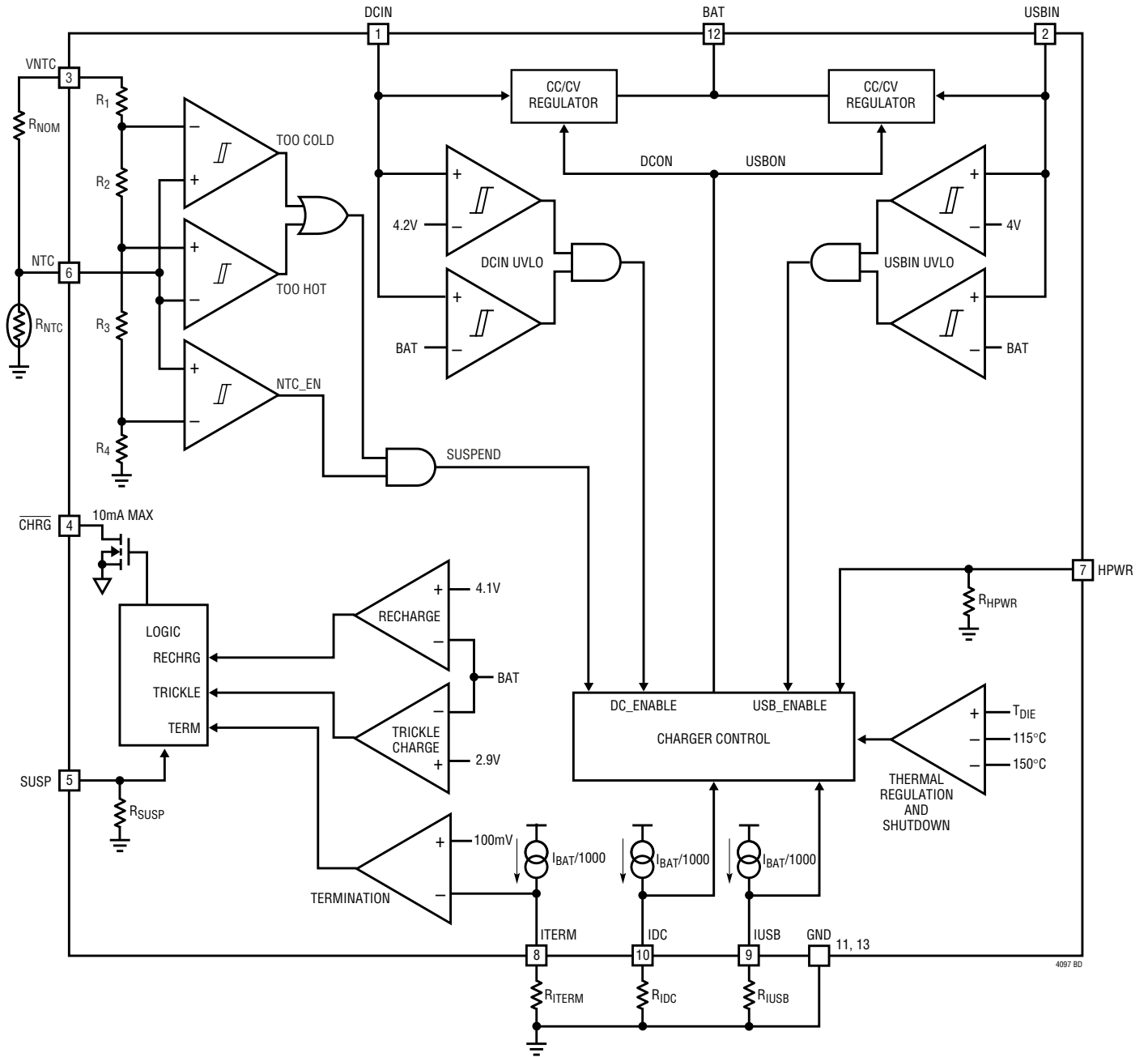
$$I_{BAT} = \frac{V_{IDC}}{R_{IDC}} \cdot 1000$$

**GND (Pin 11):** Ground.

**BAT (Pin 12):** Charger Output. This pin provides charge current to the battery and regulates the final float voltage to 4.2V.

**Exposed Pad (Pin 13):** Ground. The exposed backside of the package is ground and must be soldered to the PC board ground for electrical connection and maximum heat transfer.

**BLOCK DIAGRAM**



## OPERATION

The LTC4097 is designed to efficiently manage charging a single-cell lithium-ion battery from two separate power sources: a wall adapter and USB power bus. Using the constant-current/constant-voltage algorithm, the charger can deliver up to 1.2A of charge current from the wall adapter supply or up to 1A of charge current from the USB supply with a final float voltage accuracy of  $\pm 0.6\%$ . The LTC4097 has two internal P-channel power MOSFETs, thermal regulation and shut down circuitry. No blocking diodes or external sense resistors are required.

### Power Source Selection

The LTC4097 can charge a battery from either the wall adapter input or the USB port input. The LTC4097 automatically senses the presence of voltage at each input. If both power sources are present, the LTC4097 defaults to the wall adapter source provided sufficient power is present at the DCIN input. "Sufficient power" is defined as:

- Supply voltage is greater than the UVLO threshold.
- Supply voltage is greater than the battery voltage by 30mV (100mV or 150mV rising, 30mV falling).

The VNTC output pin indicates that sufficient input voltage is available. Table 1 describes the behavior of the power source selection.

**Table 1. Power Source Selection**

	$V_{USBIN} > 4V$ and $V_{USBIN} > BAT + 30mV$	$V_{USBIN} < 4V$ or $V_{USBIN} < BAT + 30mV$
$V_{DCIN} > 4.2V$ and $V_{DCIN} > BAT + 30mV$	Charger powered from wall adapter source; USBIN current $< 25\mu A$	Charger powered from wall adapter source
$V_{DCIN} < 4.2V$ or $V_{DCIN} < BAT + 30mV$	Charger powered from USB source	No charging

### Programming and Monitoring Charge Current

The charge current delivered to the battery from the wall adapter supply is programmed using a single resistor from the IDC pin to ground.

$$R_{IDC} = \frac{1000V}{I_{CHRG(DC)}}, I_{CHRG(DC)} = \frac{1000V}{R_{IDC}}$$

Similarly, the charge current from the USB supply is programmed using a single resistor from the IUSB pin to ground. Setting HPWR pin to its high state will select 100% of the programmed charge current, while setting HPWR to its low state will select 20% of the programmed charge current.

$$R_{IUSB} = \frac{1000V}{I_{CHRG(USB)}} \quad (\text{HPWR} = \text{HIGH})$$

$$I_{CHRG(USB)} = \frac{1000V}{R_{IUSB}} \quad (\text{HPWR} = \text{HIGH})$$

$$I_{CHRG(USB)} = \frac{200V}{R_{IUSB}} \quad (\text{HPWR} = \text{LOW})$$

Charge current out of the BAT pin can be determined at any time by monitoring the IDC or IUSB pin voltage and applying the following equations:

$$I_{BAT} = \frac{V_{IDC}}{R_{IDC}} \cdot 1000, \quad (\text{charging from wall adapter})$$

$$I_{BAT} = \frac{V_{IUSB}}{R_{IUSB}} \cdot 1000,$$

(charging from USB supply, HPWR = HIGH)

$$I_{BAT} = \frac{V_{IUSB}}{R_{IUSB}} \cdot 200,$$

(charging from USB supply, HPWR = LOW)

## OPERATION

### Programming Charge Termination

The charge cycle terminates when the charge current falls below the programmed termination threshold during constant-voltage mode. This threshold is set by connecting an external resistor,  $R_{\text{ITERM}}$ , from the  $\text{ITERM}$  pin to ground.

The charge termination current threshold ( $I_{\text{TERMINATE}}$ ) is set by the following equation:

$$R_{\text{ITERM}} = \frac{100\text{V}}{I_{\text{TERMINATE}}}, I_{\text{TERMINATE}} = \frac{100\text{V}}{R_{\text{ITERM}}}$$

The termination condition is detected by using an internal filtered comparator to monitor the  $\text{ITERM}$  pin. When the  $\text{ITERM}$  pin voltage drops below  $100\text{mV}^*$  for longer than  $t_{\text{TERMINATE}}$  (typically  $3\text{ms}$ ), the charge cycle terminates, charge current latches off and the LTC4097 enters standby mode. When charging, transient loads on the  $\text{BAT}$  pin can cause the  $\text{ITERM}$  pin to fall below  $100\text{mV}$  for short periods of time before the DC charge current has dropped below the programmed termination current. The  $3\text{ms}$  filter time ( $t_{\text{TERMINATE}}$ ) on the termination comparator ensures that transient loads of this nature do not result in premature charge cycle termination. Once the average charge current drops below the programmed termination threshold, the LTC4097 terminates the charge cycle and ceases to provide any current out of the  $\text{BAT}$  pin. In this state, any load on the  $\text{BAT}$  pin must be supplied by the battery.

### Low-Battery Charge Conditioning (Trickle Charge)

This feature ensures that deeply discharged batteries are gradually charged before applying full charge current. If the  $\text{BAT}$  pin voltage is below  $2.9\text{V}$ , the LTC4097 supplies  $1/10\text{th}$  of the full charge current to the battery until the  $\text{BAT}$  pin rises above  $2.9\text{V}$ . For example, if the charger is

programmed to charge at  $800\text{mA}$  from the wall adapter input and  $500\text{mA}$  from the USB input, the charge current during trickle charge mode would be  $80\text{mA}$  and  $50\text{mA}$ , respectively.

### Automatic Recharge

In standby mode, the charger sits idle and monitors the battery voltage using a comparator with a  $1.6\text{ms}$  filter time ( $t_{\text{RECHRG}}$ ). A charge cycle automatically restarts when the battery voltage falls below  $4.1\text{V}$  (which corresponds to approximately  $80\%$ - $90\%$  battery capacity). This ensures that the battery is kept at, or near, a fully charged condition and eliminates the need for periodic charge cycle initiations. If the battery is removed from the charger, a sawtooth waveform appears at the battery output. This is caused by the repeated cycling between termination and recharge events. This cycling results in pulsing at the  $\overline{\text{CHRG}}$  output; an LED connected to this pin will exhibit a blinking pattern, indicating to the user that a battery is not present. The frequency of the sawtooth is dependent on the amount of output capacitance.

### Status Indicators

The charge status output ( $\overline{\text{CHRG}}$ ) has two states: pull-down and high impedance. The pull-down state indicates that the LTC4097 is in a charge cycle. Once the charge cycle has terminated or the LTC4097 is disabled, the pin state becomes high impedance. The pull-down state is capable of sinking up to  $10\text{mA}$ .

The power present output ( $\text{VNTC}$ ) has two states:  $\text{DCIN}/\text{USBIN}$  voltages and high impedance. The high impedance state indicates that sufficient voltage is not present at either  $\text{DCIN}$  or  $\text{USBIN}$ , therefore no charging will occur. The  $\text{VNTC}$  output is capable of sourcing up to  $120\text{mA}$  steady state and includes short circuit protection.

\*Any external sources that hold the  $\text{ITERM}$  pin above  $100\text{mV}$  will prevent the LTC4097 from terminating a charge cycle.

## OPERATION

### Manual Shutdown

The SUSP pin has a  $3.4\text{M}\Omega$  pulldown resistor to GND. A logic low enables the charger and a logic high disables it (the pulldown defaults the charger to the charging state). The DCIN input draws  $20\mu\text{A}$  when the charger is in shutdown. The USBIN input draws  $20\mu\text{A}$  during shutdown if no power is applied to DCIN, but draws only  $10\mu\text{A}$  when  $V_{\text{DCIN}} > V_{\text{USBIN}}$ .

### NTC Thermistor

The battery temperature is measured by placing a negative temperature coefficient (NTC) thermistor close to the battery pack. The NTC circuitry is shown in the Block Diagram of Figure 4. To use this feature, connect the NTC thermistor,  $R_{\text{NTC}}$ , between the NTC pin and ground and a bias resistor,  $R_{\text{NOM}}$ , from VNTC to NTC.  $R_{\text{NOM}}$  should be a 1% resistor with a value equal to the value of the chosen NTC thermistor at  $25^\circ\text{C}$  ( $R_{25}$ ).

The LTC4097 will pause charging when the resistance of the  $100\text{k}$  NTC thermistor drops to 0.54 times the value of  $R_{25}$  or approximately  $54\text{k}$  (for a Vishay “Curve 1” thermistor, this corresponds to approximately  $40^\circ\text{C}$ ). As the temperature drops, the resistance of the NTC thermistor

rises. The LTC4097 is also designed to pause charging when the value of the NTC thermistor increases to 3.25 times the value of  $R_{25}$ . For a Vishay “Curve 1” thermistor this resistance,  $325\text{k}$ , corresponds to approximately  $0^\circ\text{C}$ . The hot and cold comparators each have approximately  $3^\circ\text{C}$  of hysteresis to prevent oscillation about the trip point. Grounding the NTC pin disables all NTC functionality.

### Thermal Limiting

An internal thermal feedback loop reduces the programmed charge current if the die temperature attempts to rise above a preset value of approximately  $115^\circ\text{C}$ . This feature protects the LTC4097 from excessive temperature and allows the user to push the limits of the power handling capability of a given circuit board without risk of damaging the device. The charge current can be set according to typical (not worst case) ambient temperature with the assurance that the charger will automatically reduce the current in worst case conditions. A safety thermal shut down circuit will turn off the charger if the die temperature rises above a value of approximately  $150^\circ\text{C}$ . DFN power considerations are discussed further in the Applications Information section.

OPERATION

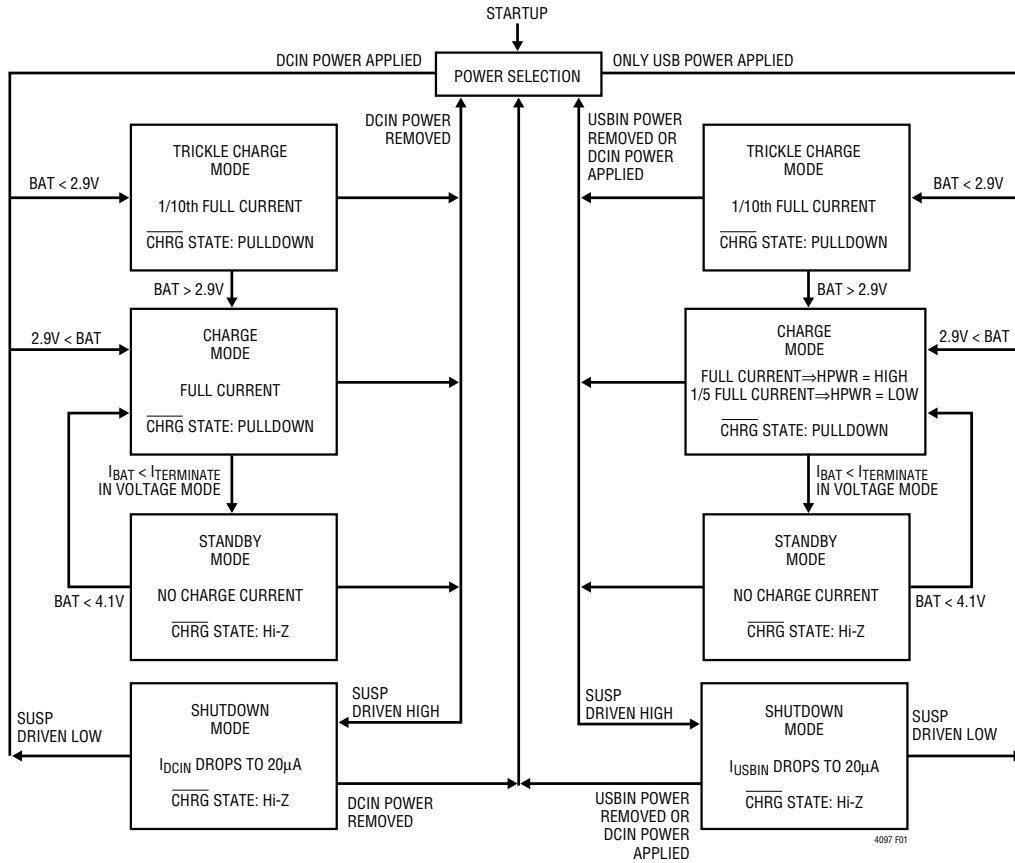


Figure 1. LTC4097 State Diagram of a Charge Cycle

## APPLICATIONS INFORMATION

### Using a Single Charge Current Program Resistor

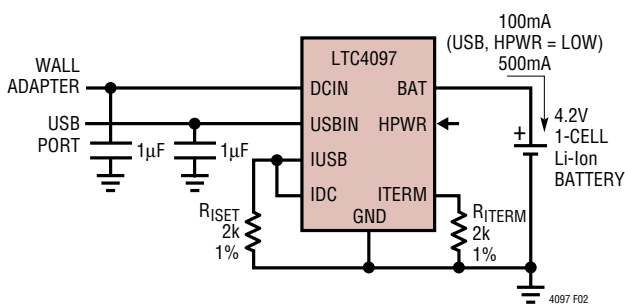
In applications where the programmed wall adapter charge current and USB charge current are the same, a single program resistor can be used to set both charge currents. Figure 2 shows a charger circuit that uses one charge current program resistor. In this circuit, one resistor programs the same charge current for each input supply.

$$I_{\text{CHRG(DC)}} = I_{\text{CHRG(USB)}} = \frac{1000V}{R_{\text{SET}}}$$

The LTC4097 can also program the wall adapter charge current and USB charge current independently using two program resistors,  $R_{\text{IDC}}$  and  $R_{\text{IUSB}}$ . Figure 3 shows a charger circuit that sets the wall adapter charge current to 800mA and the USB charge current to 500mA.

### Stability Considerations

The constant-voltage mode feedback loop is stable without any compensation provided a battery is connected to the charger output. However, a 4.7 $\mu\text{F}$  capacitor with a 1 $\Omega$  series resistor is recommended at the BAT pin to keep the ripple voltage low when the battery is disconnected. When the charger is in constant-current mode, the charge current program pin (IDC or IUSB) is in the feedback loop, not the battery. The constant-current mode stability is affected by the impedance at the charge current program pin. With no additional capacitance on this pin, the charger is stable with program resistor values as high as 20K $\Omega$  ( $I_{\text{CHRG}} = 50\text{mA}$ ); however, additional capacitance on these nodes reduces the maximum allowed program resistor.



**Figure 2. Dual Input Charger Circuit. The Wall Adapter Charge Current and USB Charge Current are Both Programmed to be 500mA**

### Power Dissipation

When designing the battery charger circuit, it is not necessary to design for worst-case power dissipation scenarios because the LTC4097 automatically reduces the charge current during high power conditions. The conditions that cause the LTC4097 to reduce charge current through thermal feedback can be approximated by considering the power dissipated in the IC. Most of the power dissipation is generated from the internal MOSFET pass device. Thus, the power dissipation is calculated to be:

$$P_D = (V_{\text{CC}} - V_{\text{BAT}}) \cdot I_{\text{BAT}}$$

$P_D$  is the power dissipated,  $V_{\text{CC}}$  is the input supply voltage (either DCIN or USBIN),  $V_{\text{BAT}}$  is the battery voltage and  $I_{\text{BAT}}$  is the charge current. The approximate ambient temperature at which the thermal feedback begins to protect the IC is:

$$T_A = 115^\circ\text{C} - P_D \cdot \theta_{\text{JA}}$$

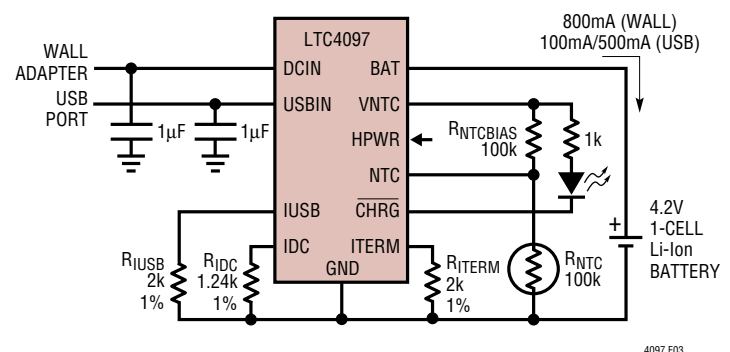
$$T_A = 115^\circ\text{C} - (V_{\text{CC}} - V_{\text{BAT}}) \cdot I_{\text{BAT}} \cdot \theta_{\text{JA}}$$

Example: An LTC4097 operating from a 5V USB adapter (on the USBIN input) is programmed to supply 500mA full-scale current to a discharged Li-Ion battery with a voltage of 3.3V. Assuming  $\theta_{\text{JA}}$  is 60 $^\circ\text{C}/\text{W}$  (see Thermal Considerations), the ambient temperature at which the LTC4097 will begin to reduce the charge current is approximately:

$$T_A = 115^\circ\text{C} - (5\text{V} - 3.3\text{V}) \cdot (500\text{mA}) \cdot 60^\circ\text{C}/\text{W}$$

$$T_A = 115^\circ\text{C} - 0.85\text{W} \cdot 60^\circ\text{C}/\text{W} = 115^\circ\text{C} - 51^\circ\text{C}$$

$$T_A = 64^\circ\text{C}$$



**Figure 3. Full Featured Dual Input Charger Circuit**

## APPLICATIONS INFORMATION

The LTC4097 can be used above 64°C ambient, but the charge current will be reduced from 500mA. The approximate current at a given ambient temperature can be approximated by:

$$I_{\text{BAT}} = \frac{115^{\circ}\text{C} - T_{\text{A}}}{(V_{\text{IN}} - V_{\text{BAT}}) \cdot \theta_{\text{JA}}}$$

Using the previous example with an ambient temperature of 75°C, the charge current will be reduced to approximately:

$$I_{\text{BAT}} = \frac{115^{\circ}\text{C} - 75^{\circ}\text{C}}{(5\text{V} - 3.3\text{V}) \cdot 60^{\circ}\text{C} / \text{W}} = \frac{40^{\circ}\text{C}}{102^{\circ}\text{C} / \text{A}}$$

$$I_{\text{BAT}} = 392\text{mA}$$

It is important to remember that LTC4097 applications do not need to be designed for worst-case thermal conditions, since the IC will automatically reduce power dissipation when the junction temperature reaches approximately 115°C. Moreover a thermal shut down protection circuit around 150°C safely prevents any damage by forcing the LTC4097 into shut down mode.

### Thermal Considerations

In order to deliver maximum charge current under all conditions, it is critical that the exposed metal pad on the backside of the LTC4097 package is properly soldered to the PC board ground. When correctly soldered to a 2500mm<sup>2</sup> double sided 1oz copper board, the LTC4097 has a thermal resistance of approximately 60°C/W. Failure to make thermal contact between the exposed pad on the backside of the package and the copper board will result in thermal resistances far greater than 60°C/W. As an example, a correctly soldered LTC4097 can deliver over 500mA to a battery from a 5V supply at room temperature. Without a good backside thermal connection, this number would drop to much less than 300mA.

### Alternate NTC Thermistors and Biasing

The LTC4097 provides temperature qualified charging if a grounded thermistor and a bias resistor are connected to NTC. By using a bias resistor whose value is equal to the room temperature resistance of the thermistor (R25)

the upper and lower temperatures are pre-programmed to approximately 40°C and 0°C, respectively (assuming a Vishay “Curve 1” thermistor).

The upper and lower temperature thresholds can be adjusted by either a modification of the bias resistor value or by adding a second adjustment resistor to the circuit. If only the bias resistor is adjusted, then either the upper or the lower threshold can be modified but not both. The other trip point will be determined by the characteristics of the thermistor. Using the bias resistor in addition to an adjustment resistor, both the upper and the lower temperature trip points can be independently programmed with the constraint that the difference between the upper and lower temperature thresholds cannot decrease. Examples of each technique are given below.

NTC thermistors have temperature characteristics which are indicated on resistance-temperature conversion tables. The Vishay-Dale thermistor NTHS0603N011-N1003F, used in the following examples, has a nominal value of 100k and follows the Vishay “Curve 1” resistance-temperature characteristic.

In the explanation below, the following notation is used.

R25 = Value of the Thermistor at 25°C

R<sub>NTC|COLD</sub> = Value of thermistor at the cold trip point

R<sub>NTC|HOT</sub> = Value of the thermistor at the hot trip point

r<sub>COLD</sub> = Ratio of R<sub>NTC|COLD</sub> to R25

r<sub>HOT</sub> = Ratio of R<sub>NTC|HOT</sub> to R25

R<sub>NOM</sub> = Primary thermistor bias resistor (see Figure 4)

R1 = Optional temperature range adjustment resistor (see Figure 5)

The trip points for the LTC4097’s temperature qualification are internally programmed at 0.349 • VNTC for the hot threshold and 0.765 • VNTC for the cold threshold.

Therefore, the hot trip point is set when:

$$\frac{R_{\text{NTC|HOT}}}{R_{\text{NOM}} + R_{\text{NTC|HOT}}} \cdot \text{VNTC} = 0.349 \cdot \text{VNTC}$$



## APPLICATIONS INFORMATION

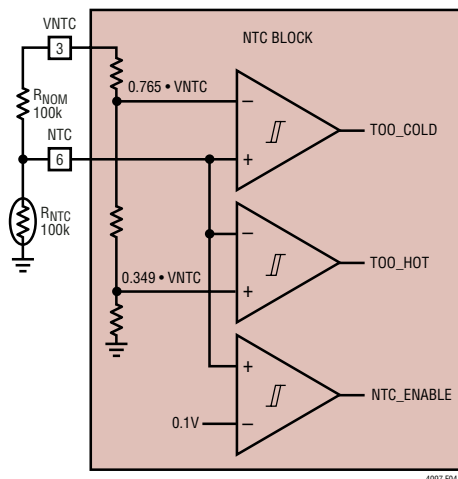


Figure 4. Typical NTC Thermistor Circuit

and the cold trip point is set when:

$$\frac{R_{NTC|COLD}}{R_{NOM} + R_{NTC|COLD}} \cdot V_{NTC} = 0.765 \cdot V_{NTC}$$

Solving these equations for  $R_{NTC|COLD}$  and  $R_{NTC|HOT}$  results in the following:

$$R_{NTC|COLD} = 0.536 \cdot R_{NOM}$$

and

$$R_{NTC|HOT} = 3.25 \cdot R_{NOM}$$

By setting  $R_{NOM}$  equal to  $R_{25}$ , the above equations result in  $r_{HOT} = 0.536$  and  $r_{COLD} = 3.25$ . Referencing these ratios to the Vishay Resistance-Temperature Curve 1 chart gives a hot trip point of about 40°C and a cold trip point of about 0°C. The difference between the hot and cold trip points is approximately 40°C.

By using a bias resistor,  $R_{NOM}$ , different in value from  $R_{25}$ , the hot and cold trip points can be moved in either direction. The temperature span will change somewhat due to the non-linear behavior of the thermistor. The following equations can be used to easily calculate a new value for the bias resistor:

$$R_{NOM} = \frac{r_{HOT}}{0.536} \cdot R_{25}$$

$$R_{NOM} = \frac{r_{COLD}}{3.25} \cdot R_{25}$$

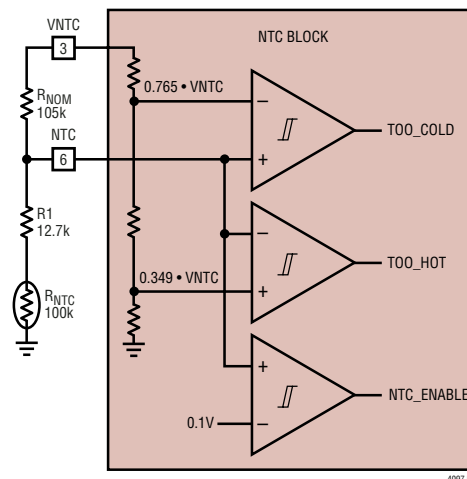


Figure 5. NTC Thermistor Circuit with Additional Bias Resistor

where  $r_{HOT}$  and  $r_{COLD}$  are the resistance ratios at the *desired* hot and cold trip points. Note that these equations are linked. Therefore, only one of the two trip points can be chosen, the other is determined by the default ratios designed in the IC. Consider an example where a 60°C hot trip point is desired.

From the Vishay Curve 1 R-T characteristics,  $r_{HOT}$  is 0.2488 at 60°C. Using the above equation,  $R_{NOM}$  should be set to 46.4k. With this value of  $R_{NOM}$ , the cold trip point is about 16°C. Notice that the span is now 44°C rather than the previous 40°C. This is due to the decrease in “temperature gain” of the thermistor as absolute temperature increases.

The upper and lower temperature trip points can be independently programmed by using an additional bias resistor as shown in Figure 5. The following formulas can be used to compute the values of  $R_{NOM}$  and  $R1$ :

$$R_{NOM} = \frac{r_{COLD} - r_{HOT}}{2.714} \cdot R_{25}$$

$$R1 = 0.536 \cdot R_{NOM} - r_{HOT} \cdot R_{25}$$

For example, to set the trip points to 0°C and 45°C with a Vishay Curve 1 thermistor choose

$$R_{NOM} = \frac{3.266 - 0.4368}{2.714} \cdot 100k = 104.2k$$

## APPLICATIONS INFORMATION

the nearest 1% value is 105k.

$$R1 = 0.536 \cdot 105k - 0.4368 \cdot 100k = 12.6k$$

the nearest 1% value is 12.7k. The final solution is shown in Figure 5 and results in an upper trip point of 45°C and a lower trip point of 0°C.

### Protecting the USB Pin and Wall Adapter Input from Overvoltage Transients

Caution must be exercised when using ceramic capacitors to bypass the USBIN or the wall adapter inputs. High voltage transients can be generated when the USB or wall adapter is hot plugged. When power is supplied via the USB bus or wall adapter, the cable inductance along with the self resonant and high Q characteristics of ceramic capacitors can cause substantial ringing which could exceed the maximum voltage ratings and damage the LTC4097. Refer to Linear Technology Application Note 88, entitled “Ceramic Input Capacitors Can Cause Overvoltage Transients” for a detailed discussion of this problem.

**Always use an oscilloscope to check the voltage waveforms at the USBIN and DCIN pins during USB and wall adapter hot-plug events to ensure that overvoltage transients have been adequately removed.**

### Reverse Polarity Input Voltage Protection

In some applications, protection from reverse polarity voltage on the input supply pins is desired. If the supply voltage is high enough, a series blocking diode can be used. In other cases where the voltage drop must be kept low, a P-channel MOSFET can be used (as shown in Figure 6).

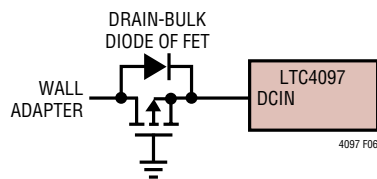
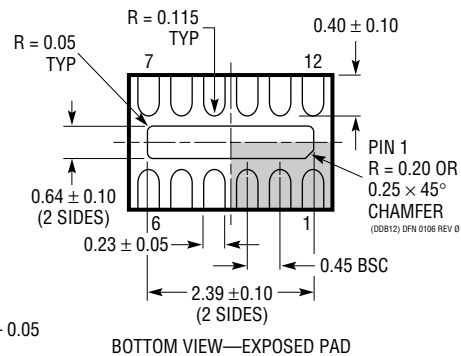
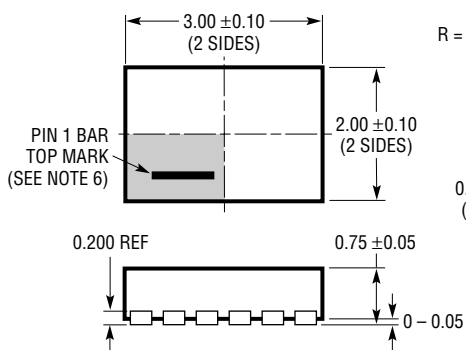
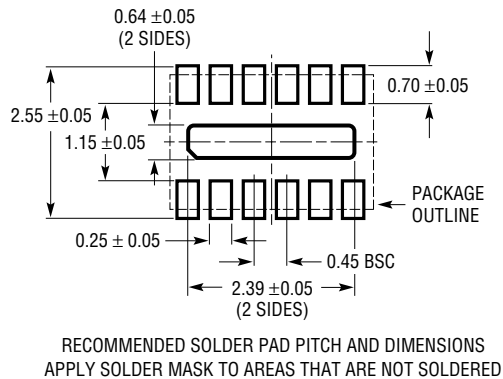


Figure 6. Low Loss Input Reverse Polarity Protection

## PACKAGE DESCRIPTION

**DDB Package**  
**12-Lead Plastic DFN (3mm × 2mm)**  
 (Reference LTC DWG # 05-08-1723 Rev 0)



**NOTE:**

1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE