Broadband Ultra Low Distortion 7-Bit Digitally Controlled VGA

FEATURES

- 1GHz Bandwidth at all Gains
- 48dBm OIP3 at 200MHz, $2V_{P-P}$ into 50Ω, R_{OUT} = 100Ω
- –88dBc IMD3 at 200MHz, $2V_{P-P}$ into 50Ω, R_{OUT} = 100Ω
- 1.4nV/√Hz Input-Referred-Noise (RTI)
- 20dBm Output P1dB at 70MHz, R_{OUT} = 130Ω
- 2dB to 18dB Gain Range (R_{OUT} = 50Ω)
- 0.125dB Gain Step Size
- 30ps Group Delay Variation
- 5ns Fast Gain Settling Time
- 5ns Fast Overdrive Recovery
- –80dB Reverse Isolation

APPLICATIONS

- Differential ADC Driver
- IF Sampling Receivers
- VGA IF Power Amplifier
- 50Ω Driver
- Instrumentation

DESCRIPTION

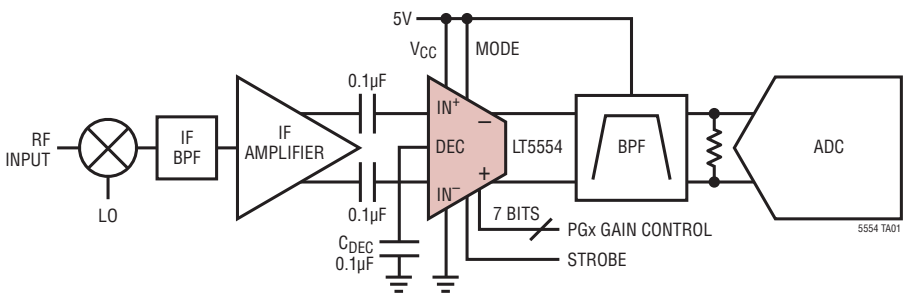
The LT®5554 is a 7-bit digitally controlled programmable gain (PG) amplifier with 16dB gain control range. It consists of a 50Ω input variable attenuator, followed by a high linearity variable transconductance amplifier. The coarse 4dB input attenuator step is implemented via 2-bits of digital control (PG5, PG6). The fine transconductance amplifier 0.125dB step within 3.875dB gain control range is set via 5-bits digital control (PG0 to PG4). The LT5554 gain control inputs (PGx) and the STROBE input can be directly coupled to TTL or ECL drivers. The seven parallel gain control inputs time skew can be eliminated by using the STROBE input positive transition.

The internal output resistor R_O = 400Ω limits the maximum overall gain to 36dB for open outputs. The internal circuitry of open output collectors enables the LT5554 to be unconditionally stable over any loading conditions (including external SAW filters) and provides –80dB reverse isolation at 300MHz.

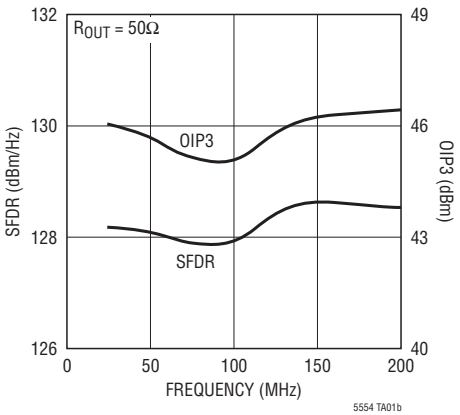
The LT5554 is internally protected during overdrive and has an on-chip power supply regulator.

With 0.125dB step resolution and 5ns settling time, the LT5554 is suitable in applications where continuous gain control is required.

TYPICAL APPLICATION



OIP3 and SFDR vs Frequency



ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage
- V_{CC} 6V

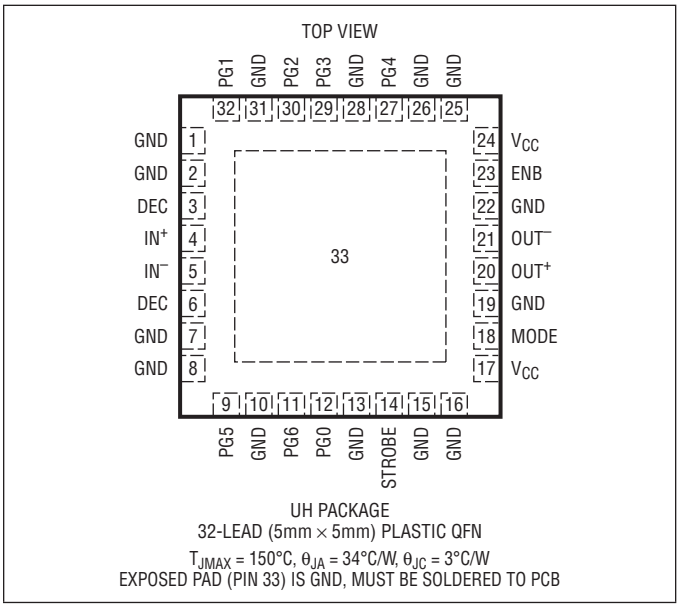
Pin Voltages and Currents
- OUT^+, OUT^- 7V
- STROBE, PGx ..... –0.5V to V_{CC}
- ENB, MODE ..... –0.5V to V_{CC}
- IN^+, IN^-, DEC ..... –0.5V to 4V

Operating Ambient Temperature Range
- LT5554 ..... –40°C to +85°C

Junction Temperature ..... 125°C

Storage Temperature Range ..... –65°C to +150°C

PIN CONFIGURATION



UH PACKAGE
32-LEAD (5mm × 5mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 34°C/W, θ_{JC} = 3°C/W
EXPOSED PAD (PIN 33) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT5554IUH#PBF	LT5554IUH#TRPBF	5554	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

AC ELECTRICAL CHARACTERISTICS

(R_{OUT} = 50Ω) Specifications are at T_A = 25°C. V_{CC} = 5V, V_{CCO} = 5V, ENB = 3V, MODE = 5V, STROBE = 2.2V, V_{IH} = 2.2V, V_{IL} = 0.6V, maximum gain (Notes 3, 6), (Test circuits shown in Figure 16), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Dynamic Performance						
BW	Large Signal –3dB Bandwidth	All Gain Settings (Note 7)		LF – 1000		MHz
OP1dB	Output 1dB Compression Point	All Gain Settings, R_{OUT} = 130Ω, 70MHz		20		dBm
G_M	Amplifier Transconductance at G_{MAX}	F_{IN} = 100MHz		0.15		S
CMRR	Common Mode Gain to Single-Ended Output	F_{IN} = 100MHz, Figure 19		–6		dB
S12	Reverse Isolation	F_{IN} = 100MHz F_{IN} = 400MHz		–86 –78		dB dB
	Overdrive Recovery Time	5ns Input Pulse, V_{OUT} within ±10%		5		ns
Noise/Linearity Performance Two Tones, P_{OUT} = 4dBm/Tone ($2V_{P-P}$ into 50Ω), Δf = 200kHz						
IIP3	Input Third Order Intercept Point	G_{MAX}, F_{IN} = 200MHz G_{MAX} –3.875dB, F_{IN} = 200MHz		27 30		dBm dBm
OIP3	Output Third Order Intercept Point for Max-Gain	F_{IN} = 100MHz F_{IN} = 200MHz		45 46		dBm dBm
IMD3	Intermodulation Product for Max-Gain	F_{IN} = 100MHz F_{IN} = 200MHz		–82 –84		dBc dBc
OIP3	Output Third Order Intercept Point for –3.875dB STEP	F_{IN} = 100MHz F_{IN} = 200MHz		44 40		dBm dBm
OIP3	Output Third Order Intercept Point	G_{MAX}, F1 = 88MHz, F2 = 112MHz G_{MAX} –3.875dB, F1 = 88MHz, F2 = 112MHz	40.5 38	47 44		dBm dBm
HD3	Third Harmonic Distortion	Pout = 10dBm, F_{IN} = 100MHz, G_{MAX}		–62		dBc
V_{ONOISE}	Output Noise Noise Spectral Density	G_{MAX}, F_{IN} = 200MHz G_{MAX} –3.875dB, F_{IN} = 200MHz		10.7 7.3		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
NF	Noise Figure	G_{MAX}, F_{IN} = 200MHz G_{MAX} –3.875dB, F_{IN} = 200MHz		10 10.5		dB dB
RTI	Input Referred Noise Spectral Density (RMS) (Note 5)	G_{MAX}, F_{IN} = 200MHz G_{MAX} –3.875dB, F_{IN} = 200MHz		1.34 1.42		$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
SFDR	Spurious Free Dynamic Range in 1Hz BW.	G_{MAX}, F_{IN} = 200MHz G_{MAX} –3.875dB, F_{IN} = 200MHz		128 129		dBm/Hz dBm/Hz
Amplifier Voltage Gain and Gain Step						
G_{MAX}	Maximum Voltage and Power Gain	F_{IN} = 112MHz	15.3	17.6	19.7	dB
G_{MIN}	Minimum Voltage and Power Gain	F_{IN} = 100MHz		1.725		dB
G_{STEP}	Gain Step Size (Note 9)	Except For –4dB, –8dB, –12dB Steps For –4dB, –8dB, –12dB Steps		0.125	0.25 0.35	dB dB
GD_{ERROR}	Group Delay Step Accuracy	F_{IN} = 100MHz		10		ps
AMPLIFIER I/O Differential IMPEDANCE						
R_{IN}	Input Resistance	F_{IN} = 100MHz, G_{MAX} to G_{MAX} –3.875dB F_{IN} = 100MHz, G_{MAX} –4dB to G_{MIN}		43 47		Ω Ω
C_{IN}	Input Capacitance	F_{IN} = 100MHz		2.8		pF
R_O	Output Resistance	F_{IN} = 100MHz		400		Ω
C_O	Output Capacitance	F_{IN} = 100MHz		1.9		pF

AC ELECTRICAL CHARACTERISTICS

(R_{OUT} = 100Ω) Specifications are at T_A = 25°C. V_{CC} = 5V, V_{CCO} = 5V, ENB = 3V, MODE = 5V, STROBE = 2.2V, V_{IH} = 2.2V, V_{IL} = 0.6V, maximum gain (Notes 3, 8), (Test circuits shown in Figure 16), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Noise/Linearity Performance Two Tones, P_{OUT} = 4dBm/Tone ($2V_{P-P}$ into 50Ω), Δf = 200kHz						
IIP3	Input Third Order Intercept Point	G_{MAX}, F_{IN} = 200MHz G_{MAX} –3.875dB, F_{IN} = 200MHz		27 27		dBm dBm
OIP3	Output Third Order Intercept Point for Max-Gain	F_{IN} = 100MHz F_{IN} = 200MHz		48 48		dBm dBm
IMD3	Intermodulation Product for Max-Gain	F_{IN} = 100MHz F_{IN} = 200MHz		–88 –88		dBc dBc
V_{ONOISE}	Output Noise Noise Spectral Density	G_{MAX}, F_{IN} = 200MHz G_{MAX} –3.875dB, F_{IN} = 200MHz		21.4 14.5		nV/√Hz nV/√Hz
NF	Noise Figure	G_{MAX}, F_{IN} = 200MHz G_{MAX} –3.875dB, F_{IN} = 200MHz		10 10.5		dB dB
RTI	Input Referred Noise Spectral Density (RMS) (Note 5)	G_{MAX}, F_{IN} = 200MHz G_{MAX} –3.875dB, F_{IN} = 200MHz		1.34 1.42		nV/√Hz nV/√Hz
SFDR	Spurious Free Dynamic Range in 1Hz BW.	G_{MAX}, F_{IN} = 200MHz		128		dBm/Hz
G_{VMAX}	Maximum Voltage Gain	F_{IN} = 100MHz		23.6		dB
G_{PMAX}	Maximum Power Gain	F_{IN} = 100MHz		20.6		dB

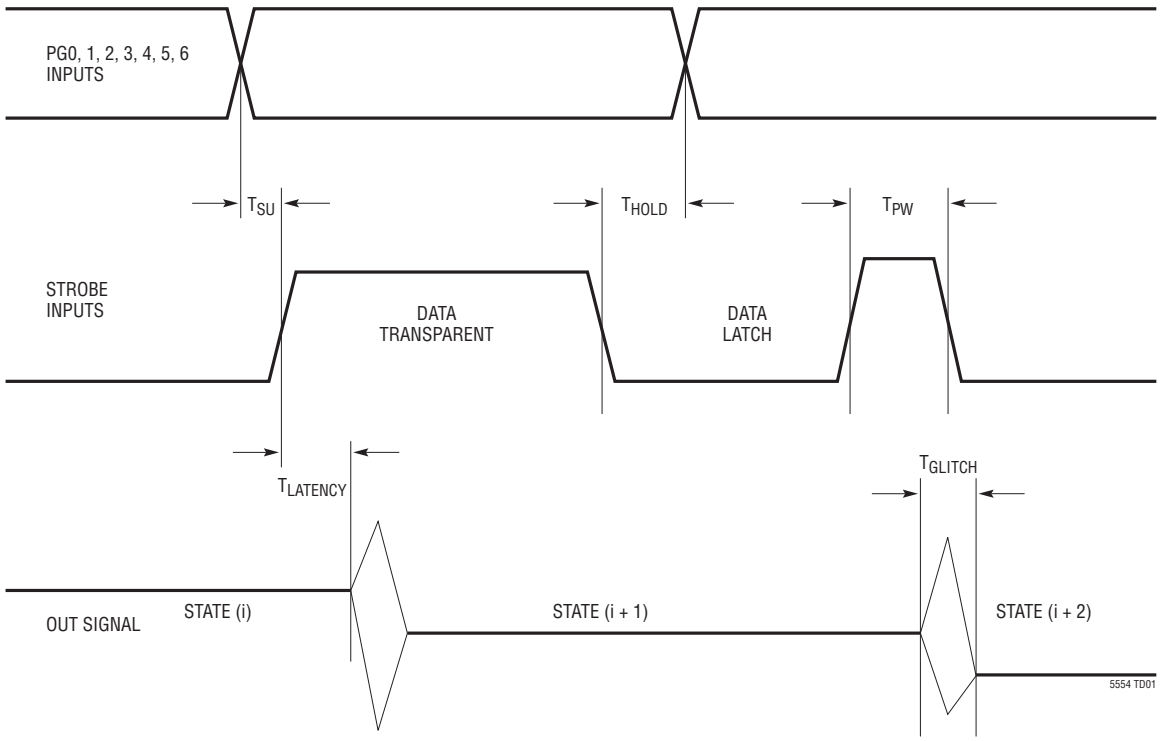
AC ELECTRICAL CHARACTERISTICS (Timing Diagram)

(R_{OUT} = 50Ω) Specifications are at T_A = 25°C. V_{CC} = 5V, V_{CCO} = 5V, ENB = 3V, MODE = 5V, STROBE = 3V, V_{IH} = 2.2V, V_{IL} = 0.6V, maximum gain (Test circuit shown in Figure 16), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
PGx and Strobe Timing Characteristics						
T_{SU}	Setup Time PGx vs STROBE			0		ns
T_{HOLD}	Hold Time PGx vs STROBE			1		ns
T_{PW}	STROBE Pulse Width			2		ns
T_R	STROBE Period			4		ns
$T_{LATENCY}$	Latency Time of the Previous Gain State	Output Settles within 1%		4		ns
T_{GLITCH}	Time Between Previous Stable Gain State to Next Stable State	Output Settles within 1%		5		ns
A_{GLITCH}	Max Glitch Amplitude	V_{IN} = 0 (No Signal or STROBE Transition During Output Signal Zero Crossing)		1		mV
		STROBE Transition when Output Power is at Peak + 10dBm Power		3		dB

AC ELECTRICAL CHARACTERISTICS (Timing Diagram)

Timing Diagram



DC ELECTRICAL CHARACTERISTICS

Specifications are at T_A = 25°C. V_{CC} = 5V, V_{CCO} = 5V, ENB = 3V, MODE = 5V, unless otherwise noted. (Note 3) (Test circuit shown in Figure 16), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Normal Operating Conditions						
V_{CC}	Supply Voltage		4.75	5	5.25	V
V_{CCO}	OUT^+, OUT^- Output Pin DC Common Mode Voltage	(Note 4)		5	6	V
Shutdown DC Characteristics, ENB = 0.6V						
$V_{IN(BIAS)}$	DEC, IN^+, IN^- Bias Voltage			2	2.15	V
$I_{IL(PG)}$	PGx, STR Input Current	V_{IN} = 0.6V		0		µA
$I_{IH(PG)}$	PGx, STR Input Current	V_{IN} = 5V		210		µA
I_{OUT}	OUT^+, OUT^- Current				20	µA
I_{CC}	V_{CC} Supply Current			4	5.1	mA
Enable Input DC Characteristics						
$V_{IL(EN)}$	ENB Input LOW Voltage	Disable			0.6	V
$V_{IH(EN)}$	ENB Input HIGH Voltage	Enable	3		V_{CC}	V
$I_{IL(EN)}$	ENB Input Current	V_{IN} = 0.6V			20	µA
$I_{IH(EN)}$	ENB Input Current	V_{IN} = 3V		70		µA
$I_{IH(EN)}$	ENB Input Current	V_{IN} = 5V		220	300	µA

DC ELECTRICAL CHARACTERISTICS

Specifications are at T_A = 25°C. V_{CC} = 5V, V_{CCO} = 5V, ENB = 3V, MODE = 5V, unless otherwise noted. (Note 3) (Test circuit shown in Figure 16), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
DEC External Capacitor Charge/Discharge CURRENT						
$I_{IH(DEC)}$	DEC Pin Source Current	V_{DEC} = 4V	27	50	70	mA
$I_{IL(DEC)}$	DEC Pin Sink Current	V_{DEC} = 1.8V	–70	–38	–14	mA
Mode Input Three-State DC Characteristics						
$V_{IL(MODE)}$	MODE Input LOW Voltage for AC-Couple	PGx AC-Coupled, STROBE AC-Coupled	0		0.6	V
$V_{OPEN(MODE)}$	MODE Input OPEN	PGx AC-Coupled, STROBE DC-Coupled	1.7	OPEN	2.3	V
$V_{IH(MODE)}$	MODE Input HIGH Voltage	PGx DC-Coupled, STROBE DC-Coupled	V_{CC} – 0.4	V_{CC}		V
$I_{IL(MODE)}$	MODE Input Current	V_{MODE} = 0V	–42	–31	–23	µA
$I_{IH(MODE)}$	MODE Input Current	V_{MODE} = 5V	43	72	100	µA
PGx (MODE = V_{CC}) and STROBE (MODE = OPEN or MODE = V_{CC}) INPUTS for DC-Coupled						
V_{IL}	Input LOW Voltage				0.6	V
V_{IH}	Input HIGH Voltage		2.2			V
$I_{IL(DC)}$	Input Current	V_{IN} = 0.6V			30	µA
$I_{IH(DC)}$	Input Current	V_{IN} = 5V	125	170	220	µA
PGx (MODE = 0V or MODE = OPEN) and STROBE (MODE = 0V) INPUTS for AC-Coupled						
$V_{IN(AC)}$	Input Pulse Range	Instantaneous Input Voltage	0		4.6	V
$V_{IN(AC)P-P}$	Input Pulse Amplitude	Rise and Fall Time <5ns Rise and Fall Time >80ns		600 300		mV_{P-P} mV_{P-P}
$V_{IN(AC)MAX}$	Maximum Input Noise Amplitude	No LT5554 Gain Update		100		mV_{P-P}
$I_{IL(AC)}$	Input Current	V_{IN} = 0V	–210	–155	–100	µA
$I_{IH(AC)}$	Input Current	V_{IN} = 5V	310	420	530	µA
Amplifier DC Characteristics						
$V_{IN(DEC)}$	DEC	G_{MAX}	1.85	2	2.25	V
$V_{IN(BIAS)}$	IN^+, IN^- Bias Voltage	G_{MAX}	1.8	2.04	2.2	V
R_{IN}	INPUT Differential Resistance	G_{MAX} G_{MIN}		48 50		Ω Ω
G_M	Amplifier Transconductance	G_{MAX}		0.15		S
I_{ODC}	OUT^+, OUT^- Quiescent Current	V_{OUT} = 5V	33	47	57	mA
$I_{OUT(OFFSET)}$	Output Current Mismatch	IN^+, IN^- Open		200		µA
I_{CC}	V_{CC} Supply Current	G_{MAX}, MODE = 0V G_{MIN}, MODE = 0V G_{MAX}, MODE = 5V G_{MIN}, MODE = 5V	78 77 75 75	110 109 106 106	132 131 127 127	mA mA mA mA
$I_{CC(TOTAL)}$	Total Supply Current	I_{CC} + 2 • I_{ODC} (G_{MAX})		200		mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND ground.

Note 3: $R_S = R_{IN}$ = 50Ω Input matching is assumed. P_{IN} is the available input power. P_{OUT} is the power into R_{OUT}. $R_{OUT} = R_O \,||\, R_{LOAD}$ is the total output resistance at amplifier open-collectors outputs (used in G_V, G_P gain calculation). R_O = 400Ω is LT5554 internal output impedance. R_{LOAD} is load resistance as seen at OUT^+, OUT^- pins.

All dBm figures are with respect to 50Ω. Specifications refer to differential inputs and differential outputs.

Note 4: An external power supply equal to V_{CCO} is used for choke inductors or center-tap transformer output interfaces. Whenever OUT^+, OUT^- pins are biased via resistors, the voltage drop produced by the DC-output current (I_{ODC} = 45mA typical) may require a larger output external power supply. However, care must be taken not to exceed the OUT^+, OUT^- absolute maximum rating when the LT5554 is disabled.

ELECTRICAL CHARACTERISTICS

Note 5: RTI (Referred-To-Input) stands for the total input-referred noise voltage source. RTI is close to output noise voltage divided by voltage gain (the exact equation is given in Definition of Specification section). The equivalent noise source e_N is twice the RTI value.

Note 6: The external loading at LT5554 OUT^+/OUT^- pins is $R_{LOAD} = 57\Omega$. $R_{OUT} = R_{LOAD} \,||\, R_O = 50\Omega$.

Note 7: The IN^+, IN^-, DEC pins are internally biased. The time-constant of input coupling capacitor sets the low frequency corner (LF) at input. The output coupling capacitors or the transformer sets the low frequency corner (LF) at the output. The LT5554 operates internally down to DC.

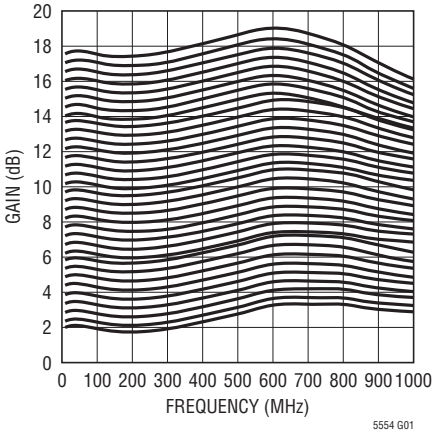
Note 8: The external loading at OUT^+/OUT^- pins is $R_{LOAD} = 133\Omega$. $R_{OUT} = R_{LOAD} \,||\, R_O = 100\Omega$.

Note 9: Depending on the actual input matching conditions and frequency of operation, the LT5554 steps involving the input attenuator tap change may show less than 0.125dB change. These steps are G_{MAX} –4dB, G_{MAX} –8dB, G_{MAX} –12dB, and the code is given in the Programmable Gain Table. The LT5554 monotonic operation for 0.125dB step resolution can still be obtained by skipping any such code with a gain error excedding 0.125dB.

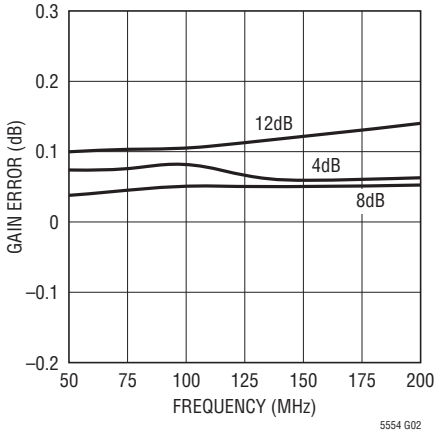
TYPICAL PERFORMANCE CHARACTERISTICS

($R_{OUT} = 50\Omega$) $T_A = 25°C$. $V_{CC} = 5V$, $V_{CCO} = 5V$, ENB = 3V, MODE = 5V, STROBE = 3V, $V_{IH} = 2.2V$, $V_{IL} = 0.6V$ (Test circuit shown in Figure 16), unless otherwise noted.

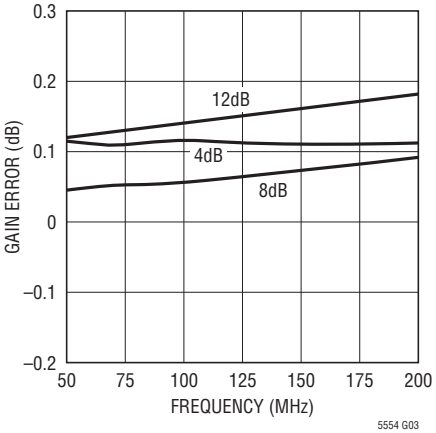
Gain vs Frequency for 0.5dB Steps, Figure 17



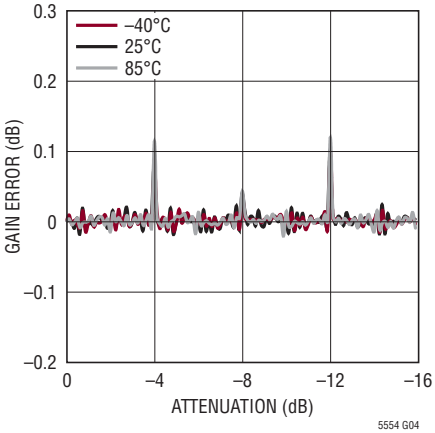
Differential Gain Error vs Frequency at –40°C



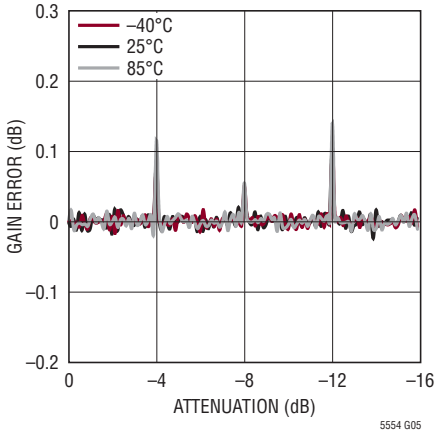
Differential Gain Error vs Frequency at 85°C



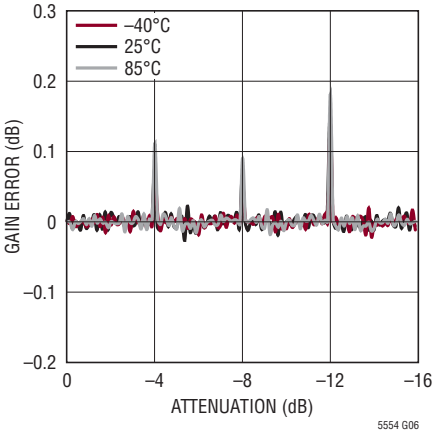
Differential Gain Error vs Attenuation at 50MHz



Differential Gain Error vs Attenuation at 100MHz



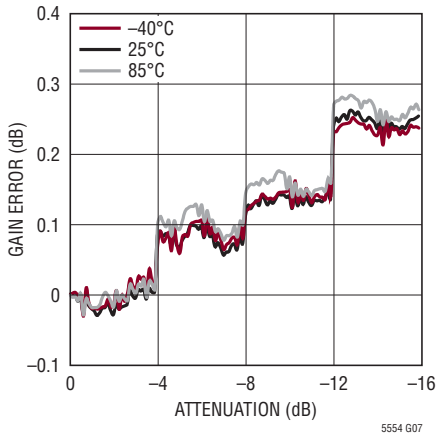
Differential Gain Error vs Attenuation at 200MHz



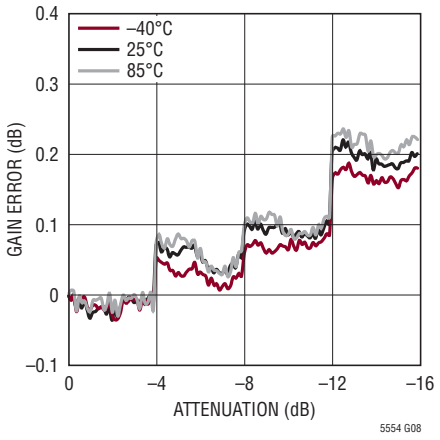
TYPICAL PERFORMANCE CHARACTERISTICS

(R_{OUT} = 50Ω) T_A = 25°C. V_{CC} = 5V, V_{CCO} = 5V, ENB = 3V, MODE = 5V, STROBE = 3V, V_{IH} = 2.2V, V_{IL} = 0.6V (Test circuit shown in Figure 16), unless otherwise noted.

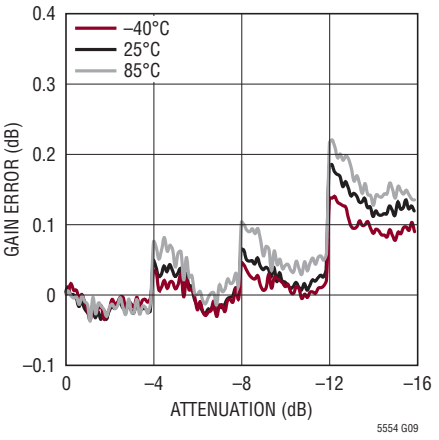
Integral Gain Error vs Attenuation at 50MHz



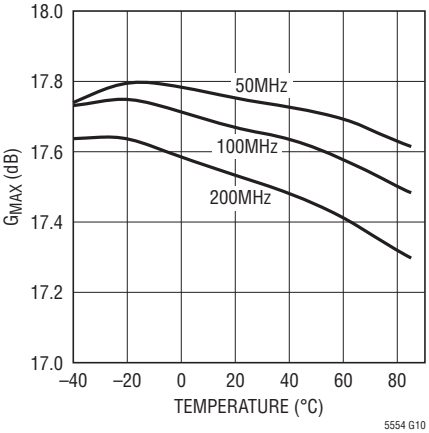
Integral Gain Error vs Attenuation at 100MHz



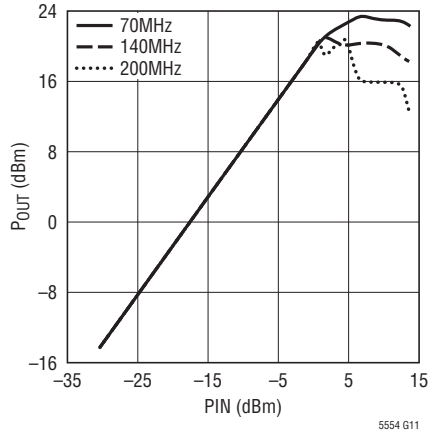
Integral Gain Error vs Attenuation at 200MHz



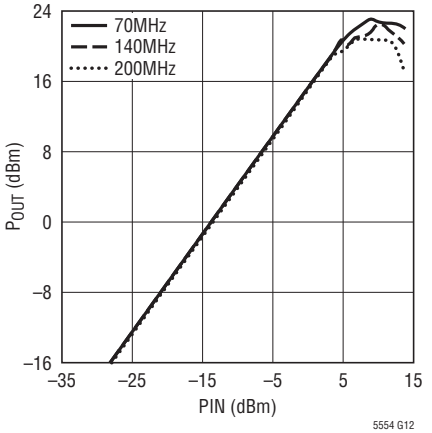
Maximum Gain vs Temperature



P_{OUT} vs P_{IN} at Maximum Gain

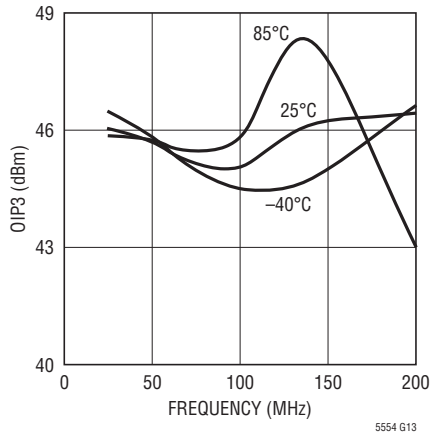


P_{OUT} vs P_{IN} at G_{MAX} – 3.875dB

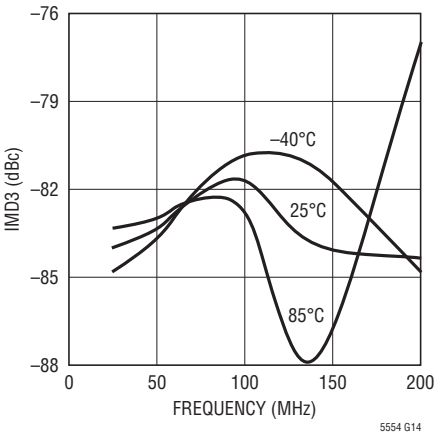


(R_{OUT} = 50Ω) T_A = 25°C. V_{CC} = 5V, V_{CCO} = 5V, ENB = 3V, MODE = 5V, STROBE = 3V, V_{IH} = 2.2V, V_{IL} = 0.6V (Test circuit shown in Figure 16) P_{OUT} = 4dBm/tone ($2V_{P-P}$ into 50Ω), Δf = 200kHz, unless otherwise noted.

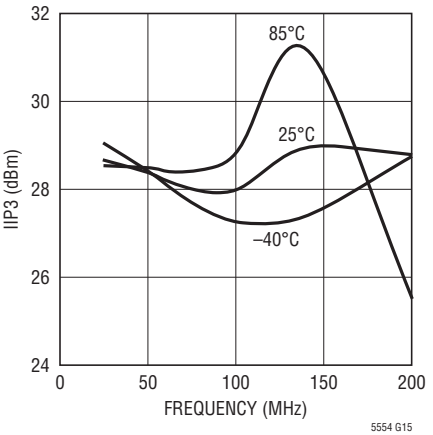
Two-Tone OIP3 vs Frequency at Max Gain, Three Temperatures



Two-Tone IMD3 vs Frequency at Max Gain, Three Temperatures



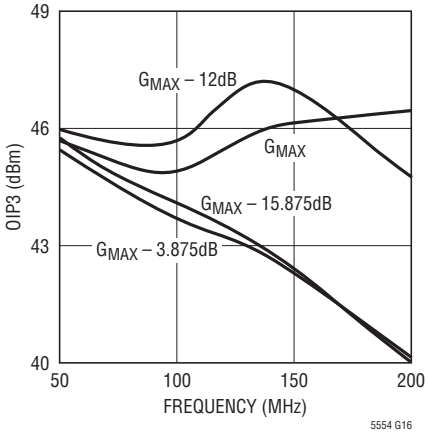
IIP3 vs Frequency at Max Gain, Three Temperatures



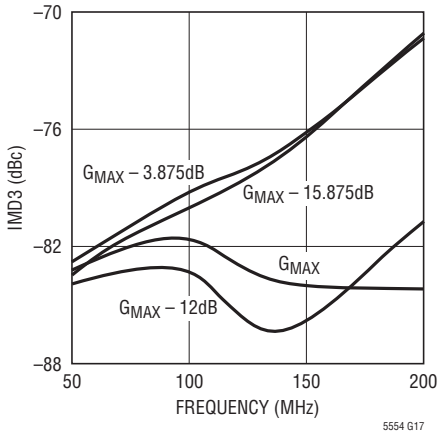
TYPICAL PERFORMANCE CHARACTERISTICS

(R_{OUT} = 50Ω) T_A = 25°C. V_{CC} = 5V, V_{CCO} = 5V, ENB = 3V, MODE = 5V, STROBE = 3V, V_{IH} = 2.2V, V_{IL} = 0.6V (Test circuit shown in Figure 16) P_{OUT} = 4dBm/tone ($2V_{P-P}$ into 50Ω), Δf = 200kHz, unless otherwise noted.

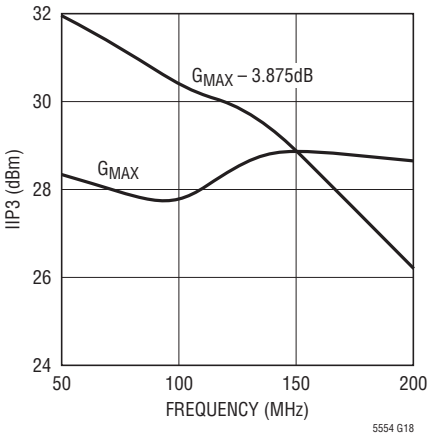
Two-Tone OIP3 vs Frequency for G_{MAX} and Critical Gain Steps



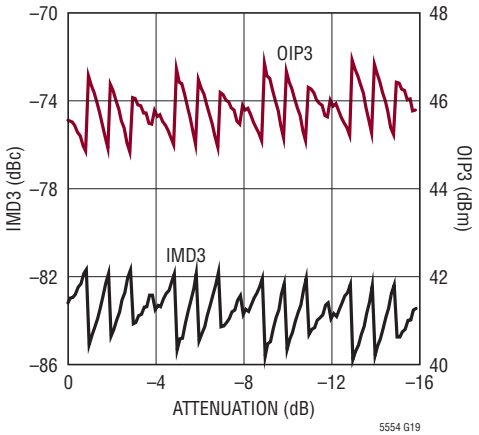
Two-Tone IMD3 vs Frequency for G_{MAX} and Critical Gain Steps



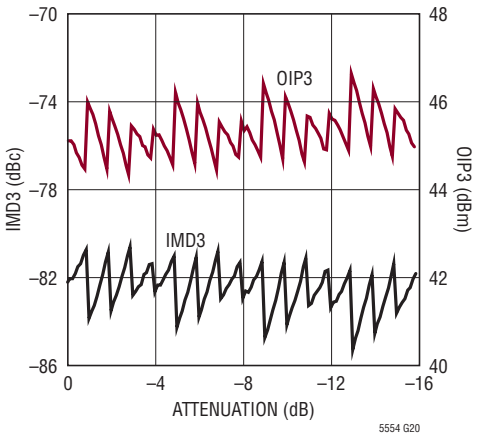
IIP3 vs Frequency for G_{MAX} and G_{MAX} –3.875dB



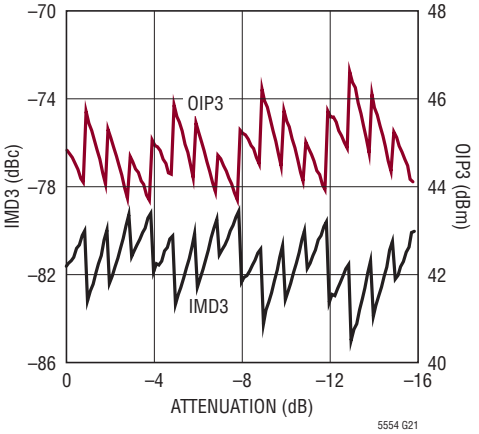
Two-Tone IMD3 and OIP3 vs Attenuation at 50MHz



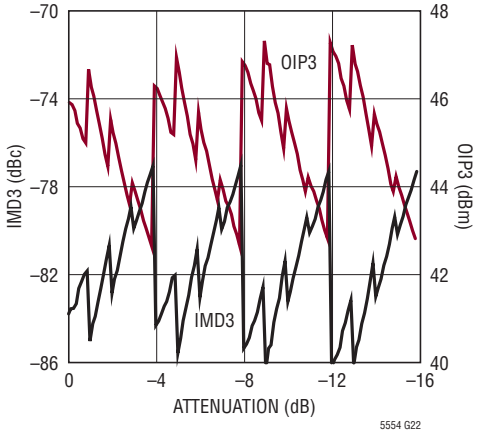
Two-Tone IMD3 and OIP3 vs Attenuation at 70MHz



Two-Tone IMD3 and OIP3 vs Attenuation at 100MHz



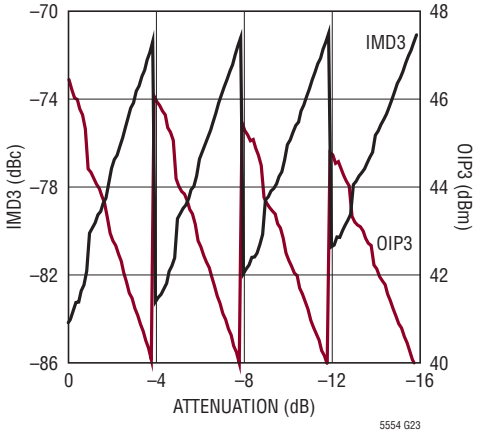
Two-Tone IMD3 and OIP3 vs Attenuation at 140MHz



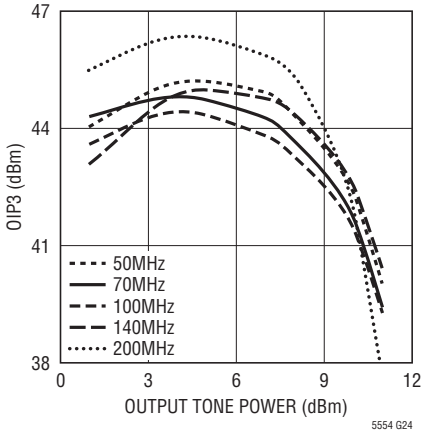
TYPICAL PERFORMANCE CHARACTERISTICS

(R_{OUT} = 50Ω) T_A = 25°C. V_{CC} = 5V, V_{CCO} = 5V, ENB = 3V, MODE = 5V, STROBE = 3V, V_{IH} = 2.2V, V_{IL} = 0.6V (Test circuit shown in Figure 16) P_{OUT} = 4dBm/tone ($2V_{P-P}$ into 50Ω), Δf = 200kHz, unless otherwise noted.

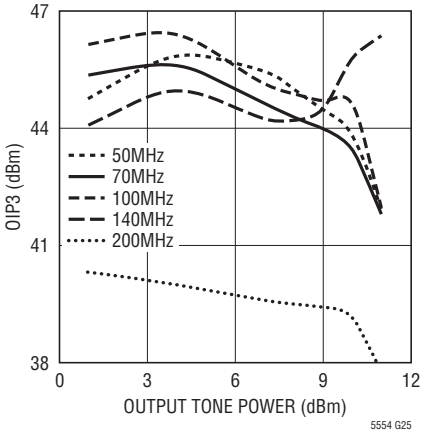
Two-Tone IMD3 and OIP3 vs Attenuation at 200MHz



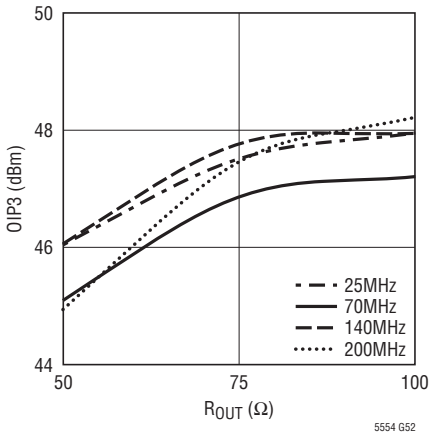
Two-Tone OIP3 vs Tone Power at Max-Gain



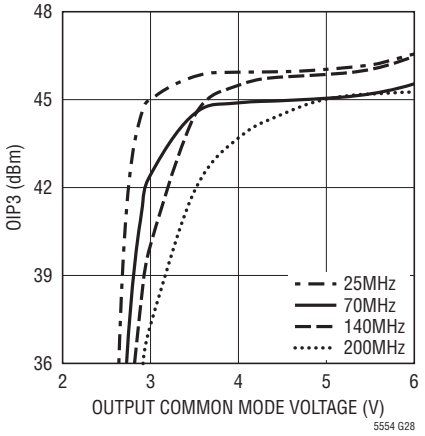
Two-Tone OIP3 vs Tone Power at Min-Gain



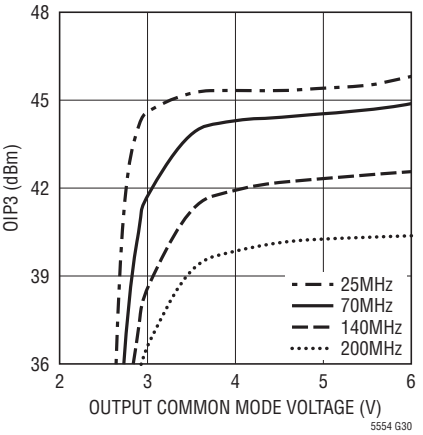
Two-Tone OIP3 vs R_{OUT}, for G_{MAX}



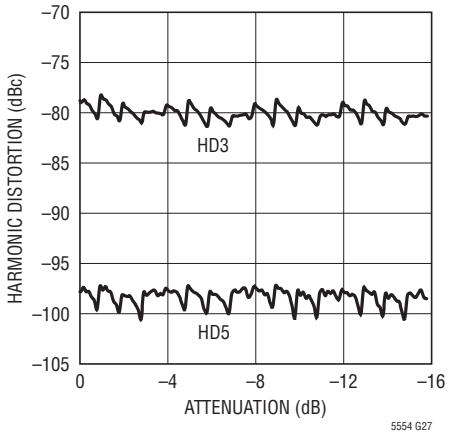
Two-Tone OIP3 vs V_{CCO}, for G_{MAX}



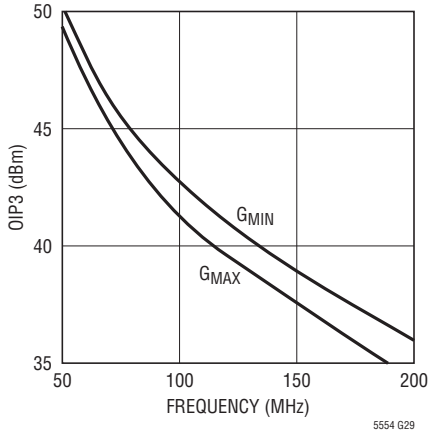
Two-Tone OIP3 vs V_{CCO}, for G_{MAX} –3.875dB



Harmonic Distortion vs Attenuation, 50MHz, P_{OUT} = 10dBm, Figure 17



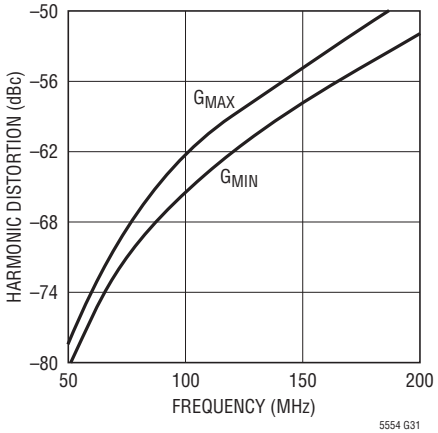
OIP3 vs Frequency for G_{MAX} and G_{MIN}, P_{OUT} = 10dBm



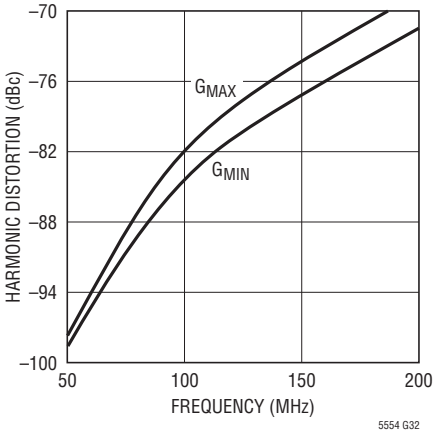
TYPICAL PERFORMANCE CHARACTERISTICS

(R_{OUT} = 50Ω) T_A = 25°C. V_{CC} = 5V, V_{CCO} = 5V, ENB = 3V, MODE = 5V, STROBE = 3V, V_{IH} = 2.2V, V_{IL} = 0.6V (Test circuit shown in Figure 16) P_{OUT} = 4dBm/tone ($2V_{P-P}$ into 50Ω), Δf = 200kHz, unless otherwise noted.

HD3 vs Frequency for G_{MAX} and G_{MIN}, P_{OUT} = 10dBm, Figure 17

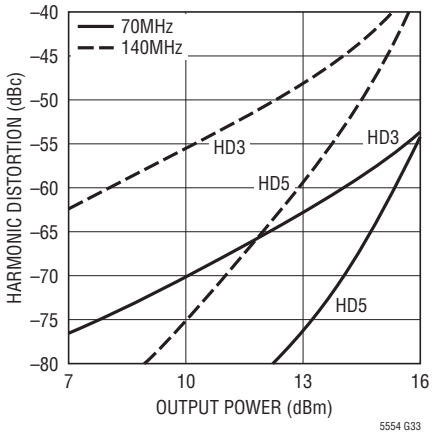


HD5 vs Frequency for G_{MAX} and G_{MIN}, P_{OUT} = 10dBm, Figure 17

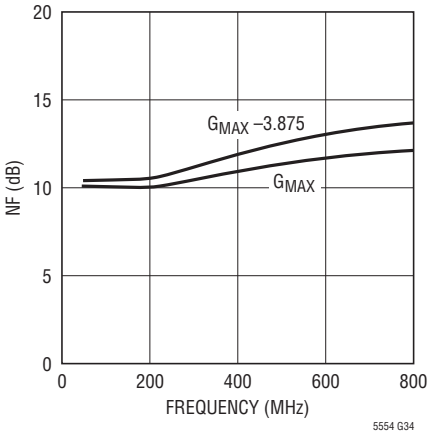


(R_{OUT} = 50Ω) T_A = 25°C. V_{CC} = 5V, V_{CCO} = 5V, ENB = 3V, MODE = 5V, STROBE = 3V, V_{IH} = 2.2V, V_{IL} = 0.6V (Test circuit shown in Figure 16), maximum gain, unless otherwise noted.

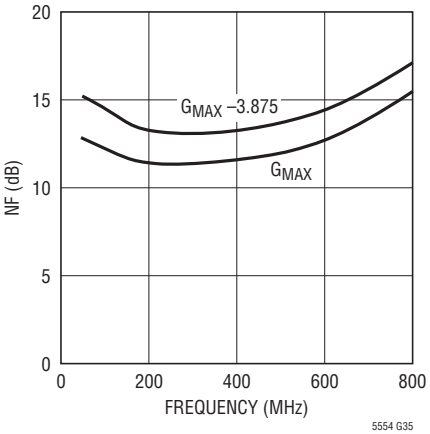
HD3 and HD5 vs P_{OUT} for G_{MAX}, Figure 17



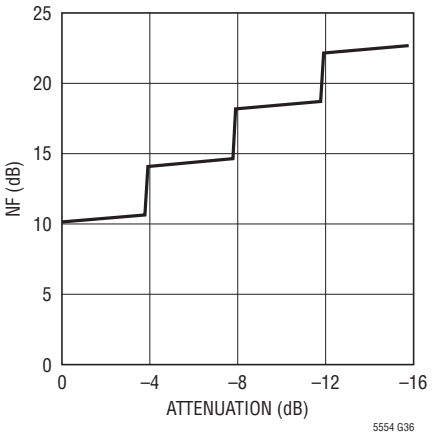
Noise Figure vs Frequency



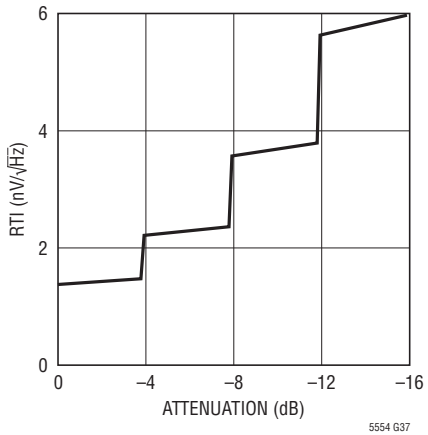
Single-Ended Output NF vs Frequency, Figure 18



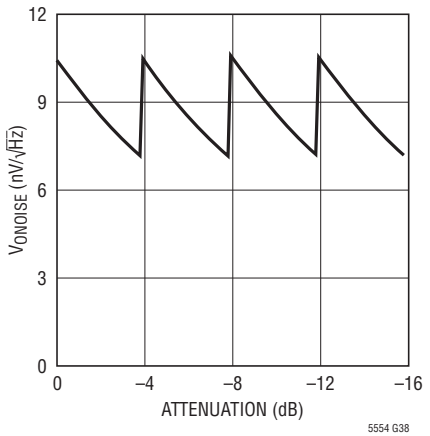
Noise Figure vs Attenuation, 140MHz



Input Referred Noise vs Attenuation, 140MHz



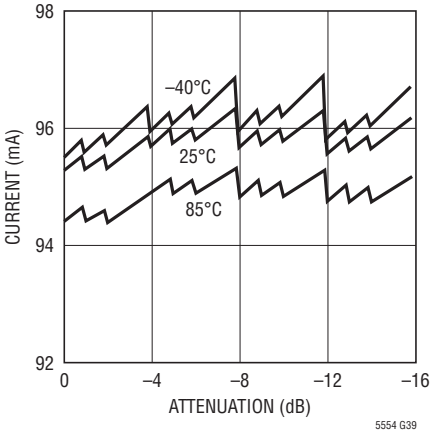
Output Noise Density vs Attenuation, 140MHz



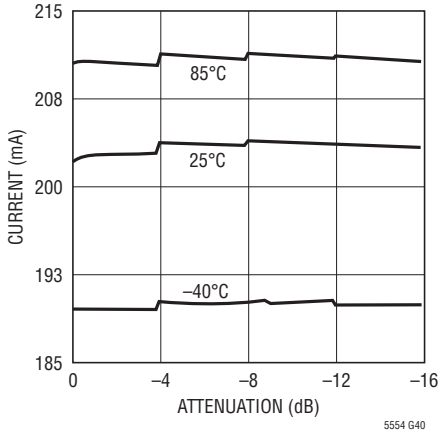
TYPICAL PERFORMANCE CHARACTERISTICS

(R_{OUT} = 50Ω) T_A = 25°C. V_{CC} = 5V, V_{CCO} = 5V, ENB = 3V, MODE = 5V, STROBE = 3V, V_{IH} = 2.2V, V_{IL} = 0.6V (Test circuit shown in Figure 16), maximum gain, unless otherwise noted.

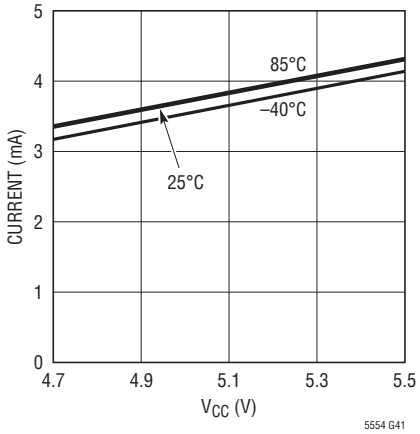
Single-Ended Output Current vs Attenuation



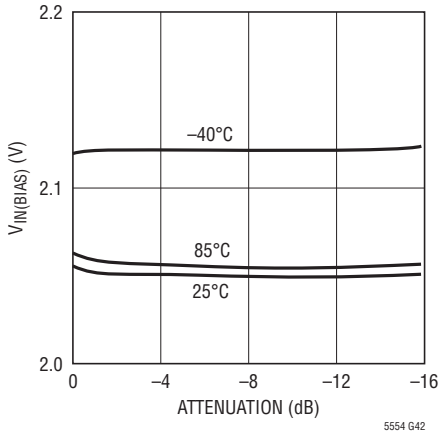
Total I_{CC} Current vs Attenuation



I_{CC} Shutdown Current vs V_{CC}, ENB = 0.6V



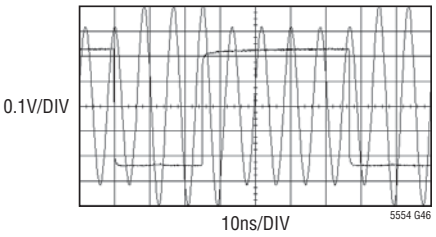
$V_{IN(BIAS)}$ vs Attenuation



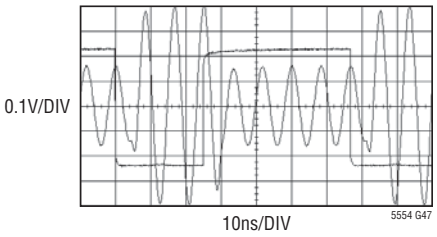
TYPICAL PERFORMANCE CHARACTERISTICS

(R_{OUT} = 50Ω) T_A = 25°C. V_{CC} = 5V, V_{CCO} = 5V, ENB = 3V, MODE = 5V, STROBE = 3V, V_{IH} = 2.2V, V_{IL} = 0.6V (Test circuit shown in Figure 16), maximum gain, unless otherwise noted.

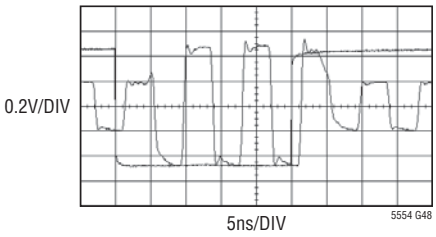
2dB-Step Response (PG4) 120MHz Signal



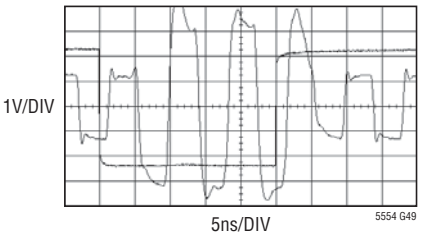
8dB-Step Response (PG6) 120MHz Signal



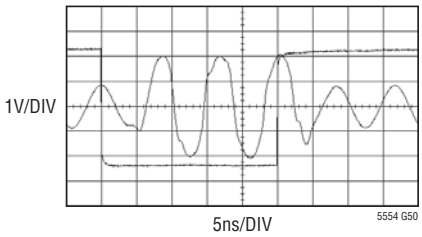
8dB-Step Response (PG6) 120MHz Pulse Signal



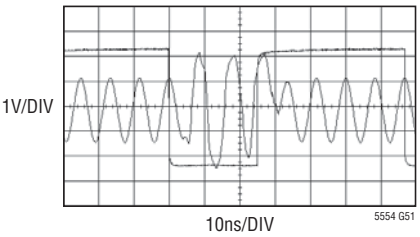
8dB-Step (PG6) 120MHz Pulse Signal for 8dB Overdrive



8dB-Step (PG6) 120MHz Sinusoidal Signal for 2dB Overdrive



8dB-Step (PG6) 120MHz Sinusoidal Signal for 8dB Overdrive



PIN FUNCTIONS

GND (Pins 1, 2, 7, 8, 10, 13, 15, 16, 19, 22, 25, 26, 28, 31): Ground Pins.

DEC (Pins 3, 6): Decoupling Pin for the Internal DC Bias Voltage for the Differential Inputs, IN^+ and IN^-. It is also connected to the 'virtual ground' of the input resistive attenuator. Capacitive de-coupling to ground is recommended in order to preserve linearity performance when IN^+, IN^- inputs are driven with up to 3dB imbalance.

IN^+ (Pin 4): Positive Signal Input Pin with Internal DC Bias to 2V.

IN^- (Pin 5): Negative Signal Input Pin with Internal DC Bias to 2V.

PG5 (Pin 9): 4dB Step Amplifier Programmable Gain Control Input Pin. Input levels are controlled by MODE pin.

PG6 (Pin 11): 8dB Step Amplifier Programmable Gain Control Input Pin. Input levels are controlled by the MODE pin.

PG0 (Pin 12): 0.125dB Step Amplifier Programmable Gain Control Input Pin. Input levels are controlled by MODE pin.

STROBE (Pin 14): Strobe Pin for the Programmable Gain Control Inputs (PGx). With STROBE in Low-state, the Amplifier Gain is not changed by PGx state changes (latch mode). With STROBE in High-state, the Amplifier Gain is asynchronously set by PGx inputs transitions (transparent-mode). A positive STROBE transition updates the PGx state. Low-state and High-state depends on MODE pin level (Table1).

V_{CC} (Pins 17, 24): Power Supply Pins. These pins are internally connected together.

MODE (Pin 18): PGx and STROBE Functionality and Level Control Pin. When MODE is higher than V_{CC} – 0.4V, the PGx and STROBE are DC-coupled. When the MODE pin is lower than 0.6V, the PGx and STROBE are AC-coupled.

PIN FUNCTIONS

When the MODE pin is left open, the PGx inputs are AC-couple and the STROBE input is DC-coupled.

In DC-coupled mode, the PGx and STROBE inputs levels are 0.6V and 2.2V. In AC-coupled mode, the PGx and STROBE inputs are driven with $0.6V_{P-P}$ minimum amplitude (with rise and fall time <5ns) regardless the DC voltage level. A positive transition sets a High-state. A negative transition sets a Low-state (for PGx and STROBE inputs).

OUT^+ (Pin 20): Positive Amplifier Output Pin. A transformer with a center tap tied to V_{CC} or a choke inductor is recommended to conduct the DC quiescent current.

OUT^- (Pin 21): Negative Amplifier Output Pin. A transformer with a center tap tied to V_{CC} or a choke inductor is recommended to conduct the DC quiescent current.

ENB (Pin 23): Enable Pin for Amplifier. When the ENB input voltage is higher than 3V, the amplifier is turned on. When the ENB input voltage is less than or equal to 0.6V, the amplifier is turned off.

PG4 (Pin 27): 2dB Step Amplifier Programmable Gain Control Input Pin. Input levels are controlled by MODE pin.

PG3 (Pin 29): 1dB Step Amplifier Programmable Gain Control Input Pin. Input levels are controlled by MODE pin.

PG2 (Pin 30): 0.5dB Step Amplifier Programmable Gain Control Input Pin. Input levels are controlled by MODE pin.

PG1 (Pin 32): 0.25dB Step Amplifier Programmable Gain Control Input Pin. Input levels are controlled by MODE pin.

EXPOSED PAD (Pin 33): Ground. This pin must be soldered to the printed circuit board ground plane for good heat dissipation.

BLOCK DIAGRAM

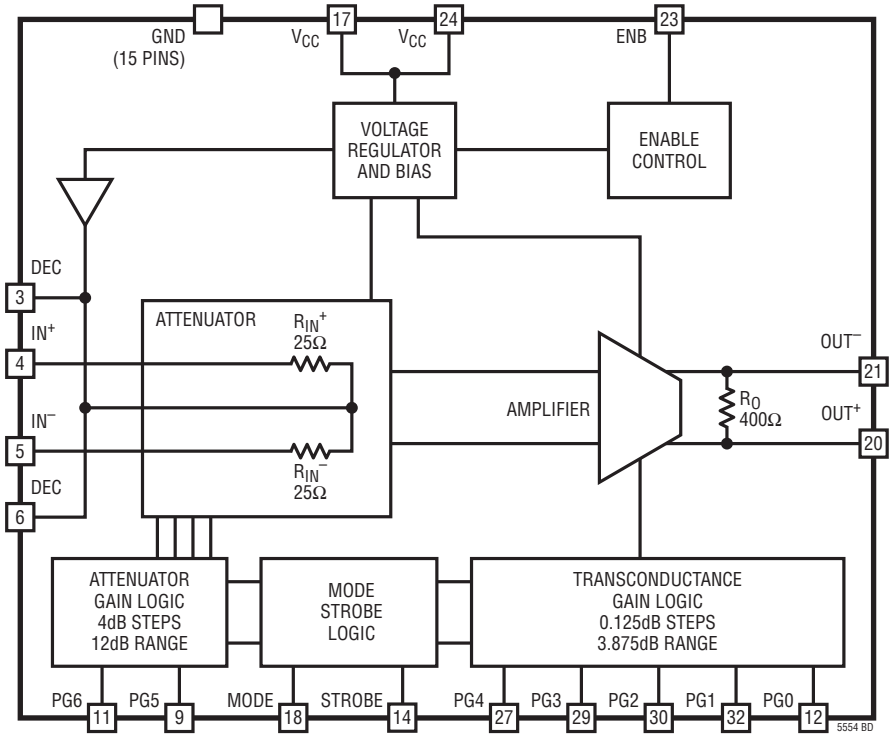


Figure 1. Functional Block Diagram

FUNCTIONAL CHARACTERISTICS

Programmable Gain Table

STATE	PG0	PG1	PG2	PG3	PG4	PG5	PG6	ATTENUATION Step Relative to Max Gain	GAIN STATE NAME
N	Step Size in dB							dB	
	0.125	0.25	0.5	1	2	4	8	(N – 127) • 0.125dB	
127	H	H	H	H	H	H	H	0.00dB	G_{MAX} (Max Gain)
126	L	H	H	H	H	H	H	–0.125dB	G_{MAX} –0.125dB
125	H	L	H	H	H	H	H	–0.250dB	G_{MAX} –0.25dB
124	L	L	H	H	H	H	H	–0.375dB	G_{MAX} –0.375dB
123	H	H	L	H	H	H	H	–0.500dB	G_{MAX} –0.5dB
122	L	H	L	H	H	H	H	–0.625dB	G_{MAX} –0.625dB
121	H	L	L	H	H	H	H	–0.750dB	G_{MAX} –0.75dB
120	L	L	L	H	H	H	H	–0.875dB	
119	H	H	H	L	H	H	H	–1.00dB	G_{MAX} –1dB
118	L	H	H	L	H	H	H	–1.125dB	G_{MAX} –1.125dB
…									
112	L	L	L	L	H	H	H	–1.875dB	G_{MAX} –1.875dB
111	H	H	H	H	L	H	H	–2.00dB	G_{MAX} –2dB
…									
104	L	L	L	H	L	H	H	–2.875dB	G_{MAX} –2.875dB
103	H	H	H	L	L	H	H	–3.00dB	G_{MAX} –3dB
…									
96	L	L	L	L	L	H	H	–3.875dB	G_{MAX} –3.875dB
95	H	H	H	H	H	L	H	–4.00dB	G_{MAX} –4dB
…									
64	L	L	L	L	L	L	H	–7.875dB	G_{MAX} –7.875dB
63	H	H	H	H	H	H	L	–8.00dB	G_{MAX} –8dB
…									
32	L	L	L	L	L	H	L	–11.875dB	G_{MAX} –11.875dB
31	H	H	H	H	H	L	L	–12.000dB	G_{MAX} –12dB
…									
8	L	L	L	H	L	L	L	–14.875dB	G_{MAX} –14.875dB
7	H	H	H	L	L	L	L	–15.000dB	G_{MAX} –15dB
6	L	H	H	L	L	L	L	–15.125dB	G_{MAX} –15.125dB
5	H	L	H	L	L	L	L	–15.250dB	G_{MAX} –15.25dB
4	L	L	H	L	L	L	L	–15.375dB	G_{MAX} –15.375dB
3	H	H	L	L	L	L	L	–15.500dB	G_{MAX} –15.5dB
2	L	H	L	L	L	L	L	–15.625dB	G_{MAX} –15.625dB
1	H	L	L	L	L	L	L	–15.750dB	G_{MAX} –15.75dB
0	L	L	L	L	L	L	L	–15.875dB	G_{MIN} (Min Gain)

DEFINITION OF SPECIFICATIONS

Amplifier Impedance and Gain Definitions (Differential)

R_S Input source resistor. Input matching is assumed:

$R_S = R_{IN}$

R_{IN} LT5554 input resistance (internal, 50Ω)

C_{IN} LT5554 input capacitance (internal)

R_O LT5554 output resistance (internal, 400Ω)

C_O LT5554 output capacitance (internal)

R_{LOAD} Load resistance as seen by LT5554 output pins

C_{LOAD} Load capacitance as seen by LT5554 output pins

R_{OUT} Total output resistance at LT5554 open-collectors outputs (used in G_V, G_P gain calculation):

$R_{OUT} = R_O \,||\, R_{LOAD}$

C_{OUT} Total output capacitance at LT5554 output (used in gain calculation):

$C_{OUT} = C_{LOAD} + C_O$

G_M LT5554 differential transconductance:

$$G_M = \frac{I_{OUT}}{V_{IN}}$$

G_V LT5554 differential voltage gain:

$$G_V = 20\log\left(\frac{V_{OUT}}{V_{IN}}\right) = 20\log\left(G_M \bullet R_{OUT}\right) \text{ in dB}$$

G_P LT5554 differential power gain:

$G_P = 10\log(R_{IN} \bullet G_M{}^2 \bullet R_{OUT})$ in dB

P_{IN} Power available at LT5554 input, $R_S = R_{IN} = 50\Omega$ input matching:

$$P_{IN} = 10\log\left(\frac{\left(\frac{V_{IN}{}^2}{2}\right)}{\left(R_{IN} \bullet 1\text{mW}\right)}\right) \text{ in dBm,}$$

V_{IN} is peak-value

P_{OUT} Total power delivered by LT5554 open-collector outputs:

$$P_{OUT} = 10\log\left(\frac{\left(\frac{V_{OUT}{}^2}{2}\right)}{\left(R_{OUT} \bullet 1\text{mW}\right)}\right) \text{ in dBm,}$$

V_{OUT} is peak-value

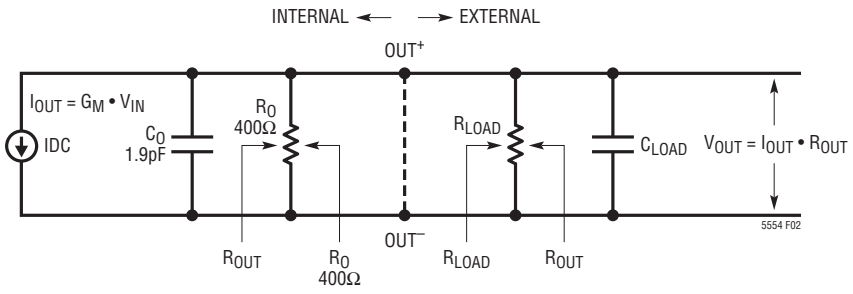


Figure 2. Output Equivalent Circuit and Impedance Definitions

DEFINITION OF SPECIFICATIONS

Noise Definitions for 50Ω Matched Input

e_{RS} Source resistor RMS noise voltage:

$$e_{RS}^2 = 4 \bullet k \bullet T \bullet R_S;\ \text{for } R_S = 50\Omega,$$

$$e_{RS} = \frac{0.9nV}{\sqrt{Hz}}$$

e_N Equivalent short-circuit input RMS noise voltage source

i_N Equivalent open-circuit input RMS noise current source

v_N Equivalent total input RMS noise voltage source:

$$v_N^2 = e_N^2 + i_N^2 \bullet R_S^2\ (R_S = 50\Omega)$$

RTI Referred-to-input LT5554 noise voltage:

$$RTI = \frac{\sqrt{(e_{RS}^2 + e_N^2 + i_N^2 \bullet R_S^2)}}{2} = \frac{v_N}{2}$$

V_{ONOISE} LT5554 output noise voltage:

$$V_{ONOISE} = \sqrt{\left(RTI^2 + \left(\frac{e_{RS}}{2}\right)^2\right) \bullet 10^{\left(\frac{GV}{20}\right)}}$$

NF Noise figure in dB according to any of the following equations:

$$NF = 10\log\left(1 + \frac{\left(e_N^2 + i_N^2 \bullet R_S^2\right)}{e_{RS}^2}\right) =$$

$$10\log\left(\frac{1 + V_N^2}{e_{RS}^2}\right) = 10\log\left(\frac{1 + RTI^2}{\left(\frac{e_{RS}}{2}\right)^2}\right)$$

Linearity Definitions for 50Ω Matched Input

IMD3[dBc] Third-order intermodulation product (negative value)

IIP3[dBm] $IIP3 = P_{IN}\ (\text{per-tone}) - \frac{IMD3}{2}$

SFDR[dBm/Hz] $SFDR = \left(\frac{2}{3}\right) \bullet (174 + IIP3 - NF)$

OIP3[dBm] $OIP3 = P_{OUT} - \frac{IMD3}{2} = IIP3 + G_P$

APPLICATIONS INFORMATION

Circuit Operation

The LT5554 is a high dynamic range programmable-gain amplifier. It consists of the following sections:

- An input variable attenuator with 50Ω input impedance (four 4dB steps, controlled by PG5, PG6 inputs)
- A differential programmable transconductance amplifier (32 steps, 0.125dB each controlled by PG0, PG1, PG2, PG3, PG4 inputs)
- Programmable logic blocks
- Internal bias (voltage regulators)
- Enable/disable circuit
- Overdrive protection circuit

Since no internal feedback network is used between amplifier outputs and inputs, the LT5554 is able to offer:

- Unconditional stability for I/O reactive loading such as filters (no isolation output resistors required)
- High reverse isolation

The LT5554 is a class-A transconductance amplifier. An input signal voltage is first converted to an output current via the LT5554 internal G_M. And then, the output load (R_{OUT}) converts the output current into an output voltage. R_{OUT} sets the LT5554 gain and output noise floor. However, the SFDR performance is almost independent of R_{OUT} for values of 25Ω to 100Ω.

APPLICATIONS INFORMATION

The PGx gain control inputs and STROBE input can be configured to be either DC coupled or AC coupled depending on MODE pin level. The LT5554 gain control inputs can be connected without external components to a wide range of user control interfaces.

The LT5554 has internal overdrive protection circuitry. The recovery time from a short duration (less than 5ns) overdrive pulse is 5ns.

Input Interface

The DC voltage level at the IN+, IN– inputs are internally biased to about 2V when the part is either enabled or disabled. The best linearity performance is achieved when an input imbalance is less than 2dB.

Two typical Input connection circuits are shown in Figures 3 and 4.

An input source with 50Ω (5%) is required for best gain error performance.

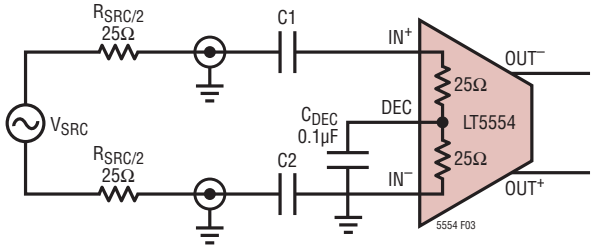


Figure 3. Input Capacitively-Coupled to a Differential Source

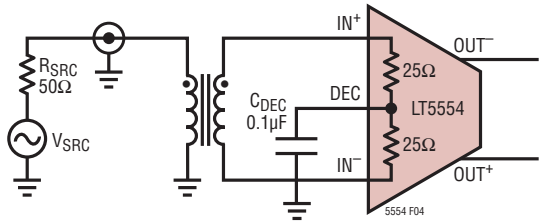


Figure 4. Input Transformer-Coupled to Single-Ended Source

Decouple (DEC) Input

The DEC pin provides the DC voltage level for differential inputs IN+, IN– via an internal buffer, which is able to fast charge/discharge the LT5554 input coupling capacitors with about 30mA sourcing or sinking current capability.

This buffer is also connected to the input resistive attenuator network. The DEC pin is a 'virtual ground' and typically connected to an external capacitor C_{DEC} (Figures 3 and 4). When C_{DEC} is used, the LT5554 will have same input attenuation for both differential mode and common mode signals. The DEC pin de-coupling capacitor improves the common mode AC performance even when the differential IN+, IN– inputs are imbalanced by 3dB.

The DEC pin can be used as a voltage reference for external circuitry when DC input coupling is desired.

Output Interface

The output interface must conduct the DC current of about 45mA to the amplifier outputs (OUT+ OUT–). Two interface examples are shown in Figures 5 and 6.

A wide band ADC voltage interface is shown in Figure 5 where L1 and L2 are choke inductors. For a narrow band application, a band pass filter can be placed at the LT5554's outputs.

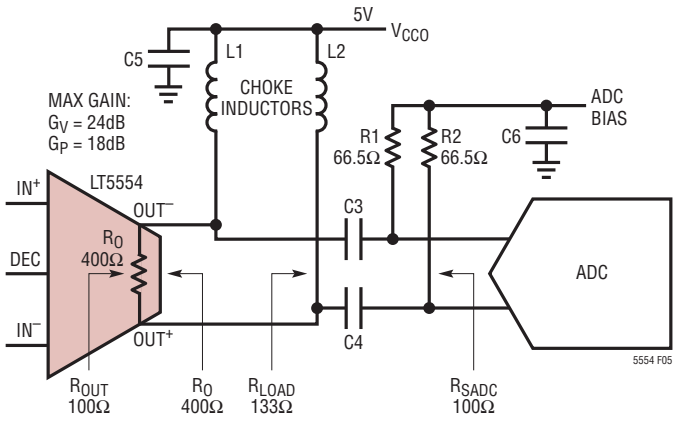


Figure 5. Differential Output Interface

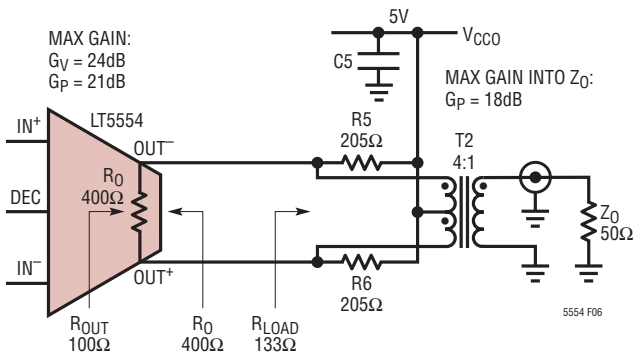


Figure 6. Single-Ended Matched Output Interface

APPLICATIONS INFORMATION

The differential outputs can also be converted to single-ended 50Ω load using a center-tap transformer interface shown in Figure 6 and Figure 16.

The internal 400Ω differential resistor (R_O) sets the output impedance and the maximum voltage gain (G_{MAX}) to 36dB when outputs OUT+, OUT– are open.

Figure 7 shows the Voltage and Power Gains as a function of R_{OUT}, which is the total output loading at the open collector amplifier output including the internal resistor R_O = 400Ω.

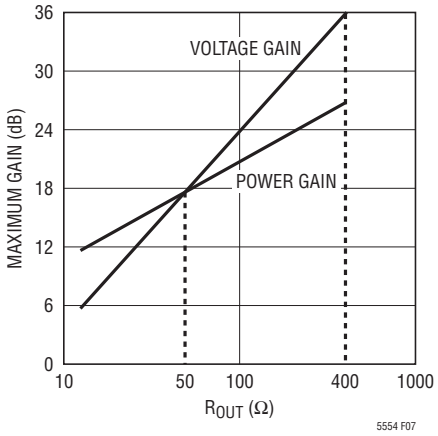


Figure 7. Maximum Voltage and Power Gain vs R_{OUT}

The gain vs R_{OUT} relationship is given by the following equations:

$$G_V = 20\log(G_M \bullet R_{OUT}) \text{ in dB}$$

$$G_P = 10\log(R_{IN} \bullet G_{M2} \bullet R_{OUT}) \text{ in dB}$$

Where R_{IN} = 50Ω and G_M = 0.15 siemens at G_{MAX}

For wide band applications, the amplifier bandwidth can be extended by inductive peaking technique. The inductor in series with the LT5554 outputs (OUT+ OUT–) can have a value up to some tens of nH depending on R_{OUT} value and board capacitance.

The current limiting will occur with R_{OUT} <140Ω, in which case the instantaneous signal current at the output exceeds I_{ODC} = 45mA.

Voltage clipping will occur with R_{OUT} >140Ω, in which case the instantaneous voltage at each OUT+ and OUT– outputs is either <2V or >8V.

The output OP1dB = 20dBm can be achieved when R_{OUT} = 130Ω. In this case, the LT5554 outputs reach both current and voltage limiting for maximum output power.

Gain Control Interface

The MODE pin selects the interface to the LT5554 gain control pins.

The PGx and STROBE control inputs can be configured to be either DC-coupled (for TTL interface) or AC-coupled (for ECL or low-voltage CMOS interfaces).

In addition, the STROBE input can be driven such that the LT5554 gain state is updated asynchronously (PGx latch control in transparent-mode) or controlled by positive STROBE transition (PGx latch control in strobed-mode).

There are several options available for coupling type and latch control which are given in the following tables:

Table1. MODE Input Options

MODE (State)	COUPLING TYPE		PGx (Latch Control)
	STROBE	PGx	
LOW	AC Positive Transition	AC	Strobe
OPEN	DC >2.2V	AC	Transparent
OPEN	0.6 to 2.2V	AC	Strobe
HIGH	DC >2.2V	DC	Transparent
HIGH	0.6 to 2.2V	DC	Strobe

Table2. MODE Input Levels

MODE (State)	MODE (Min Level)	MODE (Max Level)
LOW	0	0.6V
OPEN	1.5V	2.5V
HIGH	V_{CC} – 0.4V	V_{CC}

Alternatively, the MODE pin can be left open (2V internal).

APPLICATIONS INFORMATION

All seven PGx gain control inputs and STROBE input can be configured as DC-coupled or ac-coupled. Accordingly, there are two basic equivalent schematics (shown in Figures 8 and 9) depending on MODE input choice (Table1).

Each PGx input circuit shown in Figures 8 and 9 is followed by a transparent latch controlled by the STROBE input level (Table 1).

The DC-coupled interface is shown in Figure 8. DC levels for PGx inputs and STROBE input are V_{IL} <0.6V, V_{IH} >2.2V.

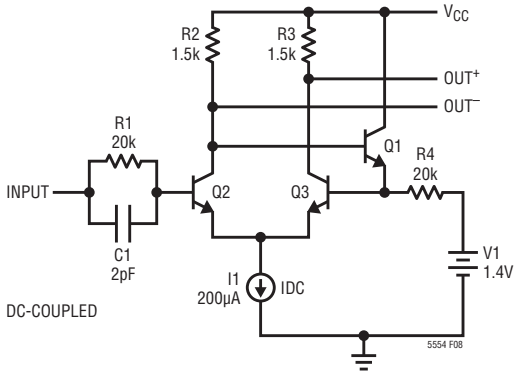


Figure 8. DC-Coupled PGx and STROBE Equivalent Inputs (Simplified Schematic)

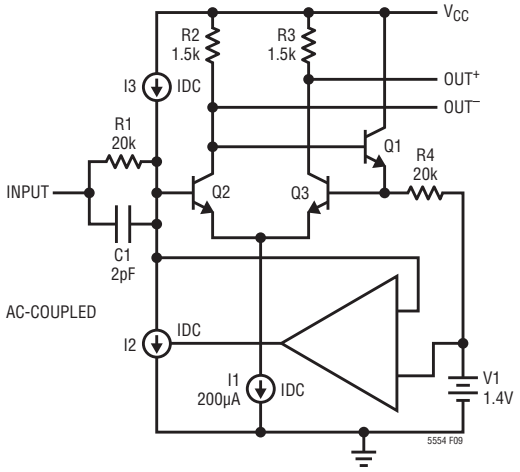


Figure 9. AC-Coupled PGx and STROBE Equivalent Inputs (Simplified Schematic)

The AC-coupled interface is shown in Figure 9. The PGx inputs and STROBE input state is decided by a signal transition rather than signal level.

A HIGH-state is set by positive transitions. A LOW-state is set by negative transitions. The PGx and STROBE inputs appear as capacitive coupled inputs. The DC voltage (0V to V_{CC} range) presented on any PGx or STROBE input is shifted to the internal 1.4V level by the additional circuit shown in Figure 9. Each PGx and STROBE input has an independent shift circuit such that each input can have a different DC voltage.

Each PGx input has a parallel R-C (R1 = 20k, C1 = 2pF) with a 40ns time constant. The STROBE input circuit has R1 = 20k C1 = 3pF and 60ns time constant. An minimum amplitude of $0.6V_{P-P}$ is required to trip the PGx and STROBE inputs to an appropriate state when the signal period is less than input time constant. The circuit shown in Figure 8 converts the single-ended external signal to an internal differential signal. Consequently, when the input is idle for more than the input time constant, a $0.3V_{P-P}$ transition will still trigger the gain control state change. All control inputs have 200mV hysteresis to insure stable logic levels when the input noise level is less than $100mV_{P-P}$.

For transparent latch control, the amplifier gain will be updated directly with any PGx input state changes. If different PGx inputs have an (external) time skew greater than 1ns, then a noticeable amplifier output glitch can occur. The strobe latch control is recommended to avoid this amplifier output glitch.

It is not necessary to double buffer the PGx inputs since the LT5554 has good internal isolation from the PGx inputs to the amplifier output to any type of external gain control circuit without external components.

If LT5554 is powered up or enabled in latch mode, the LT5554 gain initial gain is indeterminate. If the minimum gain state is desired at power up, it is recommended to set the transparent-mode with all PGx inputs low.

APPLICATIONS INFORMATION

Gain Step Accuracy

LT5554 internal input signal coupling to the transconductance amplifier inputs across the 4dB step attenuator increases with frequency. The gain step error is higher when the LT5554 gain update changes the input attenuator tap (PG5, PG6 transitions) and this error is frequency dependent.

Gain error is 'compressive', effectively reducing LT5554 gain range. Therefore, it is possible to skip one gain code whenever PG5, PG6 transitions are involved in order to preserve high-frequency monotonic behavior for 0.125dB steps.

Linearity and Noise Performance Throughout the Gain Range

The LT5554's Noise and Linearity performance across the 16dB gain range at 100MHz with R_{OUT} = 100 and R_{SADC} = 50Ω is shown in Figures 10 through 13.

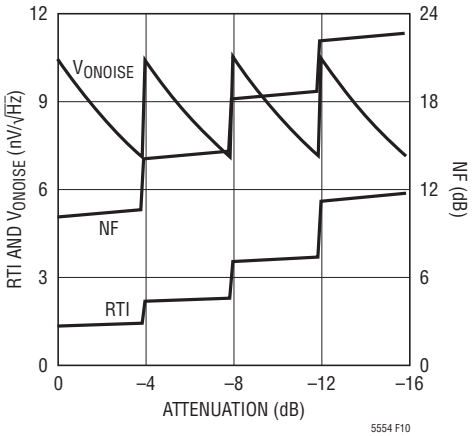


Figure 10. Noise, 140MHz, R_{OUT} = 50Ω

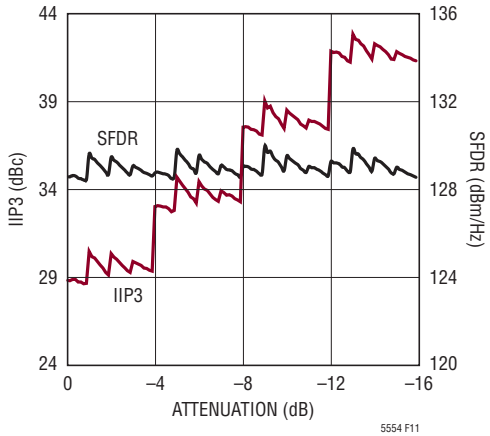


Figure 11. Noise, 140MHz, R_{OUT} = 50Ω

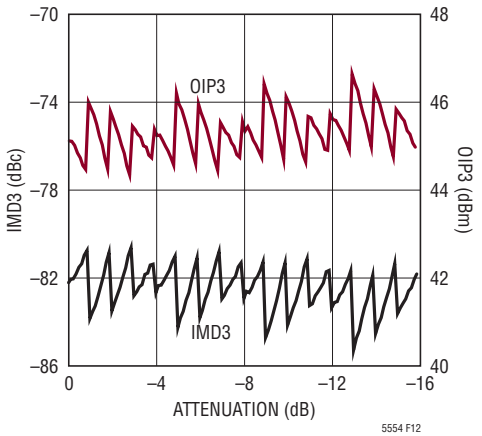


Figure 12. Linearity, 70MHz, R_{OUT} = 50Ω, 4dBm/Tone

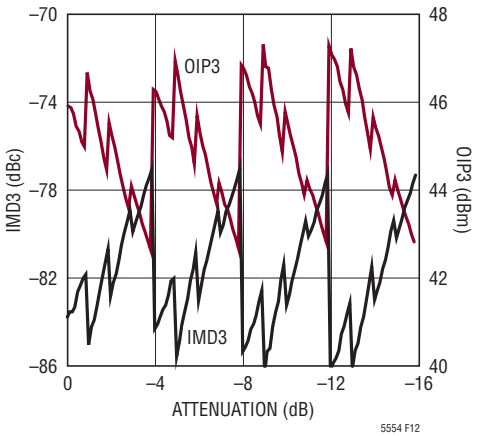


Figure 13. Linearity, 140MHz, R_{OUT} = 50Ω, 4dBm/Tone

APPLICATIONS INFORMATION

The LT5554 Noise and Linearity performance throughout the 16dB gain range has an obvious discontinuity at every 4dB gain step. The noise figure is fairly constant from 0dB (Maximum Gain) to –3.875dB attenuation when the gain is decreased by lowering the amplifier transconductance. And then, the NF increases by 4dB when the input attenuator is switched to –4dB attenuation while the amplifier gain is switched back to maximum transconductance. This pattern repeats for each 4dB gain step change.

SECOND ORDER HARMONIC DISTORTION

Balanced differential inputs and outputs are important for achieving excellent second order harmonic distortion (HD2) of the LT5554. When configured in single-ended input and output interfaces, therefore, the single-ended to differential conversion at the input and differential to single-ended conversion at the output will have significant impact on the HD2 performance.

Figure 14, for example, shows the desirable singe-ended input and output configuration using external transformers for the single-ended to differential conversion and differential to single-ended conversion. To assure a good HD2 performance, R5 and R6 should also be matched to better

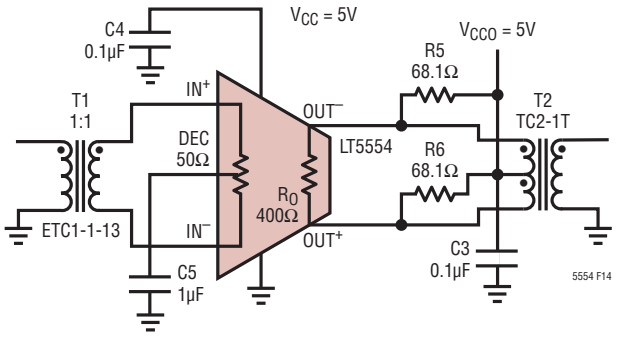


Figure 14. Recommended Single-Ended Input and Output Configuration, HD2 = –80dBc at 10dBm, 140MHz

than 1% or use these two resistors with 1% component tolerance. In this case, the HD2 can be as good as -80dBc when the output power is 10dBm at 140MHz.

When the single-ended input is not converted into well balanced inputs to LT5554, the HD2 performance will be degraded. For instance, when the T1 transformer is improperly rotated by 90 degrees as shown in Figure 15, the imbalance of the differential input signals will result in 14dB degradation in HD2. It is also important to split the differential R7 resistor into two single-ended R5 and R6 resistors at the outputs to reduce the imbalance of the T2 transformer. If not, 3dB degradation in HD2 performance can also be observed.

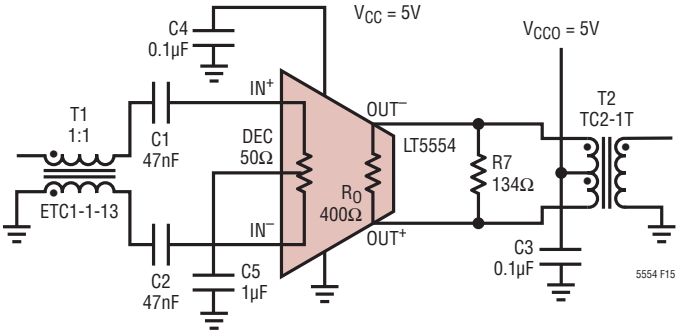


Figure 15. Not Recommended Single-Ended Input and Output Configuration, HD2 = –63dBc at 10dBm, 140MHz

The HD2 performance can be further improved by mounting a capacitor from IN+ to ground (a few pF) and a capacitor from OUT– to ground. For narrow band applications, these capacitors cancels to some degree the T1 and T2 imbalance as shown in Figure 15.

For optimum HD2 performance, fully differential input and output interfaces to the LT5554 part are recommended.

APPLICATIONS INFORMATION

Layout Considerations

Attention must be paid to the printed circuit board layout to avoid output pin to input pin signal coupling (external feedback). The evaluation board layout is a good example. The exposed backside pad on the LT5554 package must be soldered to PCB ground plane for thermal considerations.

Characterization Test Circuits

The LT5554's typical performance data are on the test circuits shown in Figures 16, 17 and 18 which are simplified schematics of the evaluation board schematic from Figure 21.

The transformer board from Figure 16 was used for characterization as a function of R_{OUT}. For each R_{OUT} option, The T2 transformer model and the matching resistors R5, R6 values are given in Table 3. The T2 transformer total matching resistance is $R_{MATCH} = R_O \,||\, (R5 + R6)$ (part LT5554 internal, and part on board R5 and R6).

Table 3. Transformer Board R_{OUT} Options

R_{OUT} (Ω)	50	75	100
T2 (Mini-Circuits)	TC2-1T	TC3-1T	TC4-1W
N_{LOAD} Ratio	2	3	4
R_{LOAD} (Ω)	57.1	92.3	133.3
R5, R6 (Ω)	68.1	124	205
G_{P_BOARD} (dB)	13.2	16	17.2
IL(T2) at 200MHz (dB)	–0.6	–0.65	–1

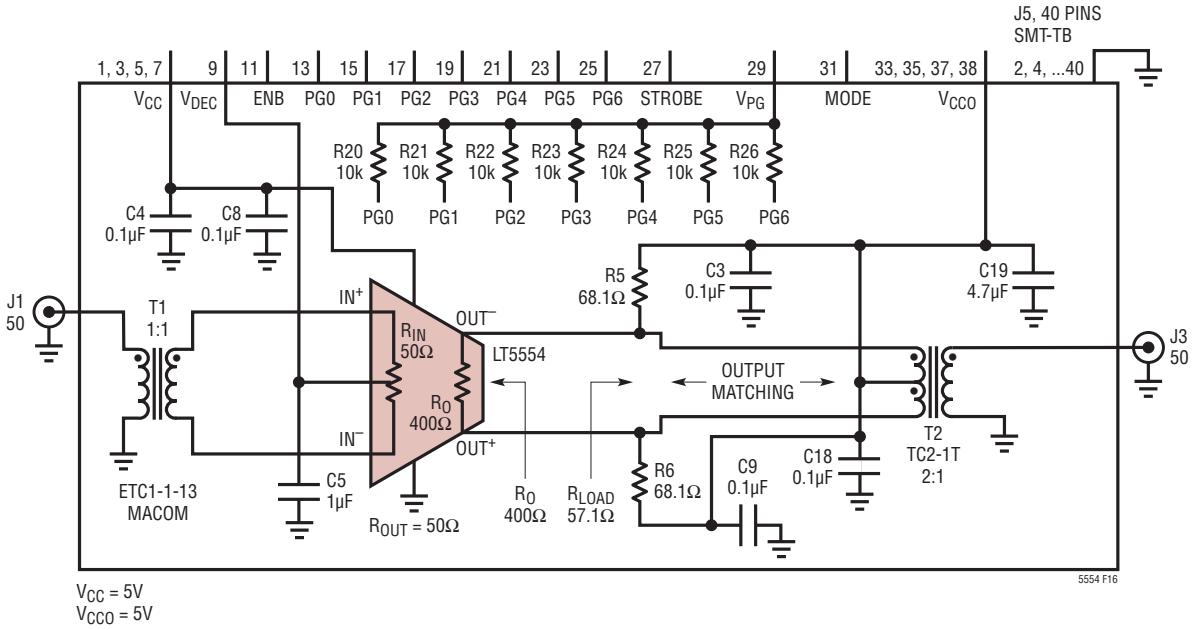


Figure 16. Single-Ended Transformer Test Board (Simplified Schematic)

APPLICATIONS INFORMATION

The LT5554 output power P_{OUT} was obtained by adding 3dB for matching-loss and the transformer loss IL(T2) in Table 3 to the board output power at J3 connector. The transformer insertion loss (frequency and temperature dependent) has been included in characterization.

The output power matching is required when LT5554 drives a 50Ω transmission line as shown on the evaluation board.

When LT5554 drives local (on-board) loads such that an ADC part, output power matching is not required and OIP3 is defined based on P_{OUT}, total power at LT5554 open collector outputs.

Figure 17 shows the evaluation board for wide-band characterization at R_{OUT} = 50Ω, where the insertion loss of the output balun is about –1dB at 1GHz. Several R_{OUT} options are given in Table 4 as well as the output padding insertion-loss and required V_{CCO} for 5V on LT5554 outputs. The LT5554 output power at open collector outputs is:

$$P_{OUT} = P_{WR}(J3) + IL(T2) + 3dB + IL_{PAD}$$

Table 4. Balun Board R_{OUT} Options

R_{OUT} (Ω)	25	36	50	71	100
R3, R4 (Ω)	0	6.49	15.4	30.1	53.6
R5, R6 (Ω)	28.7	28.7	28	28	28
IL_{PAD}	0	1.88	3.66	5.76	8.08
V_{CCO} (V)	6.29	6.57	6.96	7.61	8.66

The differential-output board from Figure 18 was used for R_{OUT} = 50Ω wide-band characterization of the LT5554 single-ended outputs.

Both Figure 17 and Figure 18 boards V_{CCO} was shifted up with the voltage drop on R5, R6 produced by 45mA output DC current such that OUT+, OUT– DC bias voltage is still 5V. The LT5554 part should be always enabled when V_{CCO} >6V. If disabled, the V_{CCO} will be applied at OUT+, OUT– exceeding the absolute maximum 6V limit with possible LT5554 failure.

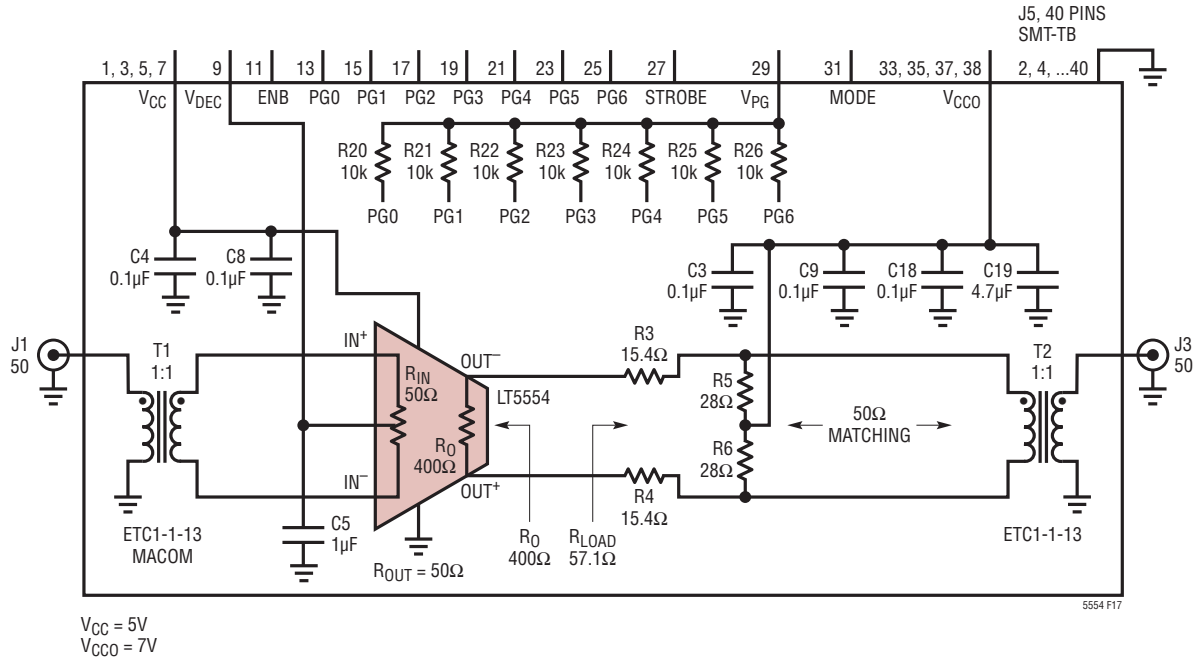


Figure 17. Single Ended Test Board (Simplified Schematic)

APPLICATIONS INFORMATION

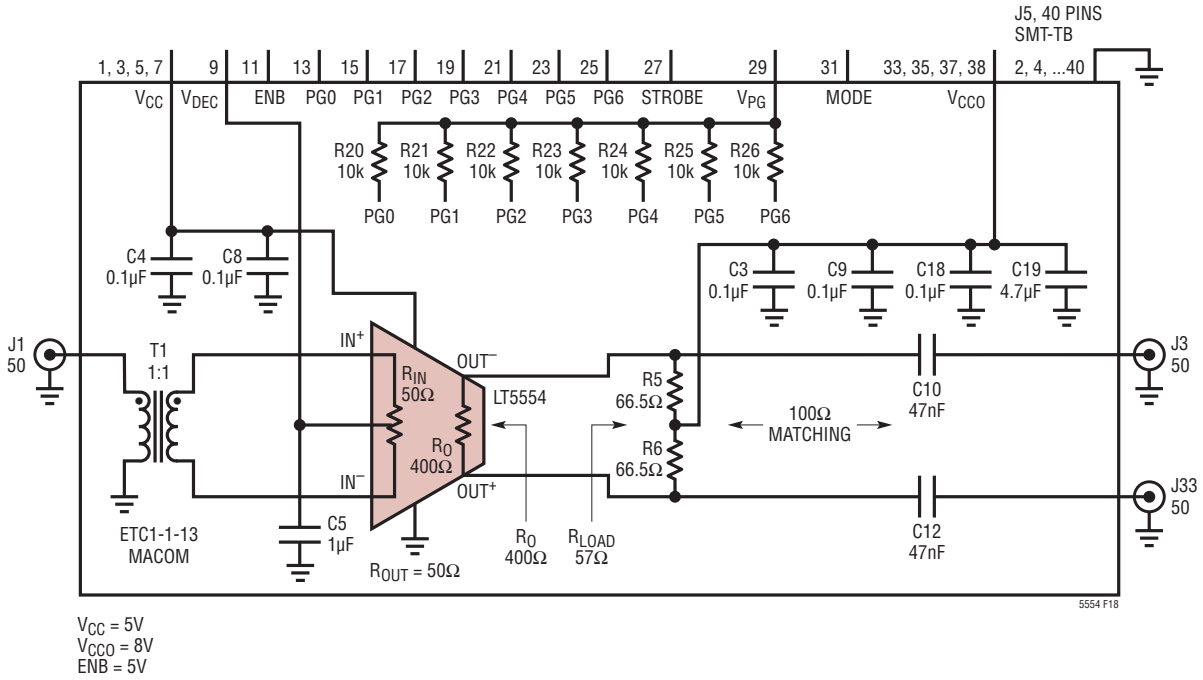


Figure 18. Wideband Differential Output Test Board (Simplified Schematic)

Common mode characterization for the LT5554 was performed with input circuit shown in Figure 19.

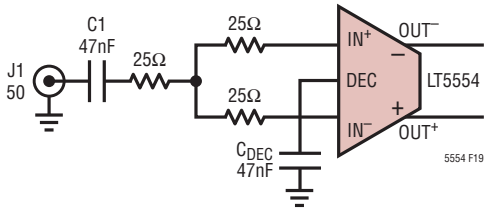


Figure 19. Common Mode Input Interface

Timing characterization and AC-coupled gain control inputs are tested on evaluation board. The required circuit modifications are shown in the Figure 20 simplified schematic and detailed below for PG6 (8dB step). The PG6 pulse source is applied at J6 connector and 50Ω terminated by R16 and R33 resistors. C66 decouple R33 to ground while C16 provides DC-decoupling between referenced to ground pulse source and the PG6 DC-voltage. A supply connected to PG6 turret will set the PG6 DC-voltage in 0V to 5V range. All other (untested) PGx DC-voltage can be independently be applied at V_{PG} turret decoupled by C88.

Strobe-mode operation is tested with a pulse source applied at J7 connector as shown in Figure 20.

Applying similar modifications around J2 and J4 connectors shown in Figure 21, other PGx inputs can be evaluated. As described in Table 1 and Table 2, the MODE pin will select the desired state.

APPLICATIONS INFORMATION

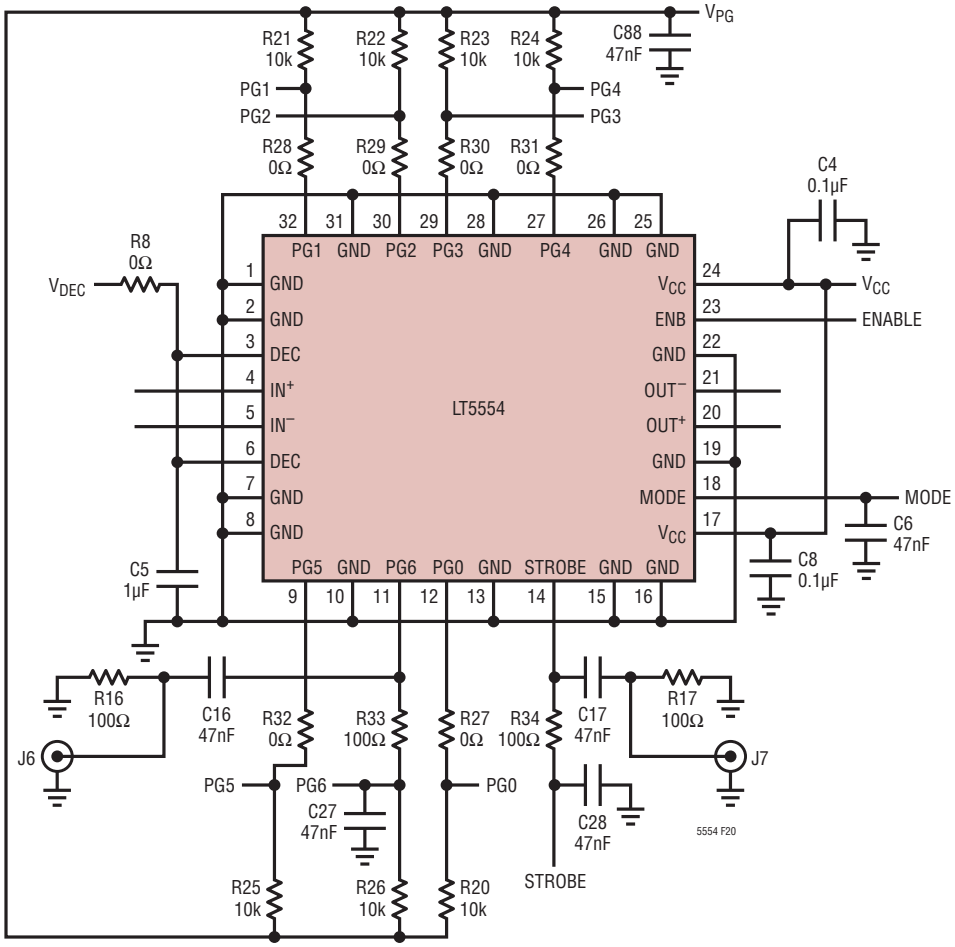


Figure 20. Timing Test for PG6 and STROBE (Simplified Schematic)

Evaluation Board

Figure 21 shows the schematic of the LT5554 evaluation board. Transformer T2 is TC2-1T and resistor R5 + R6 = 134Ω (R_{OUT} = 50Ω G_P(J3) = 13.2dB). The silkscreen and layout are shown in Figures 22 through Figure 27. The board control J5 edge connector (40PINS SMT-TB) allows easy access to LT5554 component pins. Alternatively or combined with J5, 14 test points (turrets) for signals and two for GND are also available. The board is powered with a single supply in 4.75V to 5.25V at V_{CC} and V_{CCO} (either J5 connector or turrets). Connecting the ENABLE pin to V_{CC} supply enables the LT5554 part. PGx gain control and STROBE inputs will have TTL levels (DC-coupled) when MODE = 5V (same power supply). To set LT5554 for maximum gain (G_{MAX}) in transparent-mode, all seven PGx and STROBE can be connected to 5V supply. Alternatively, a 2.2V power supply at V_{PG} pin and STROBE turret will set same G_{MAX} state.

J1 (input) and J3 (output) are the default board signal ports for evaluation with 50Ω single ended test system. For differential evaluation, the board J11 and J33 connectors must be reconfigured.

APPLICATIONS INFORMATION

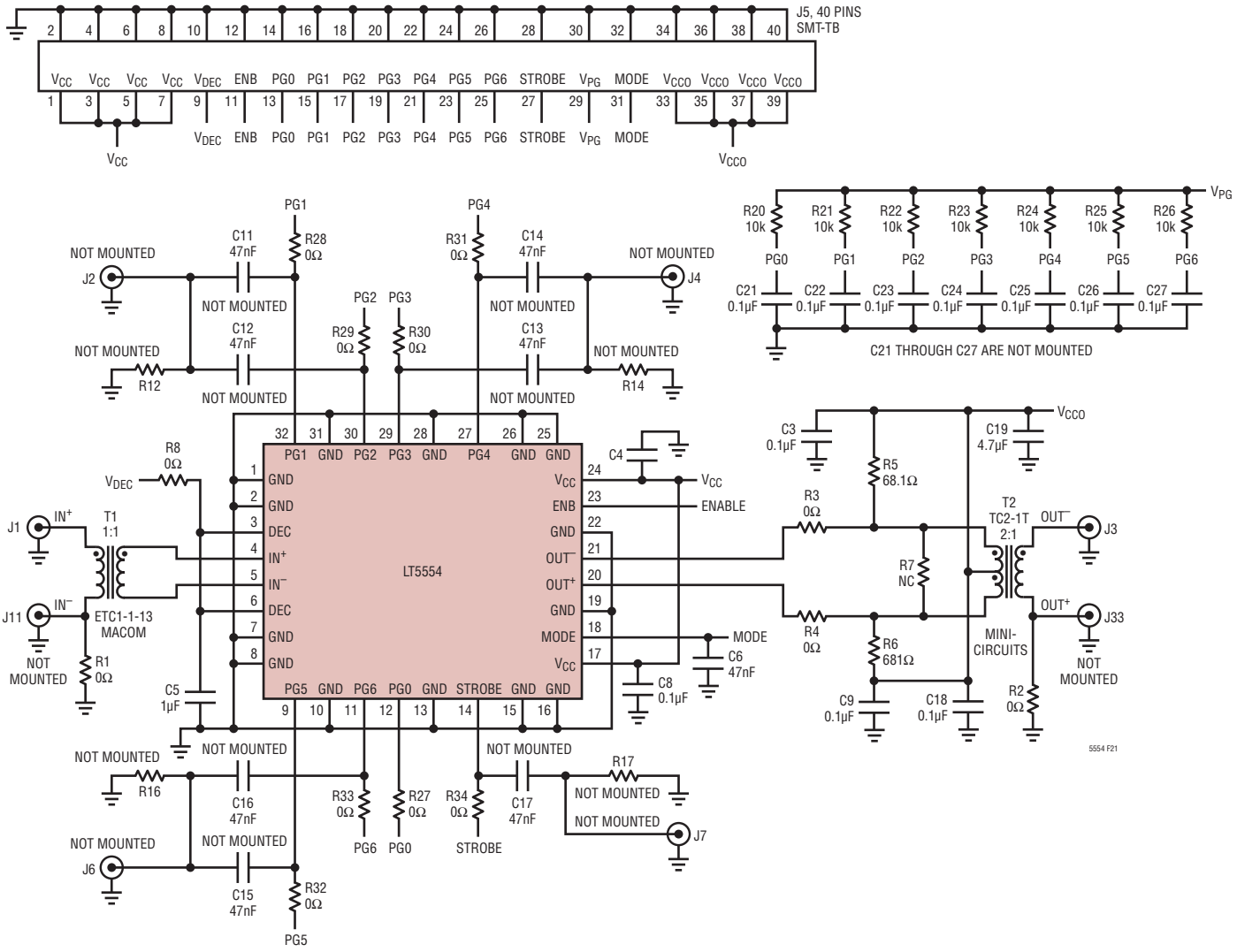


Figure 21. Evaluation Circuit Schematic

APPLICATIONS INFORMATION

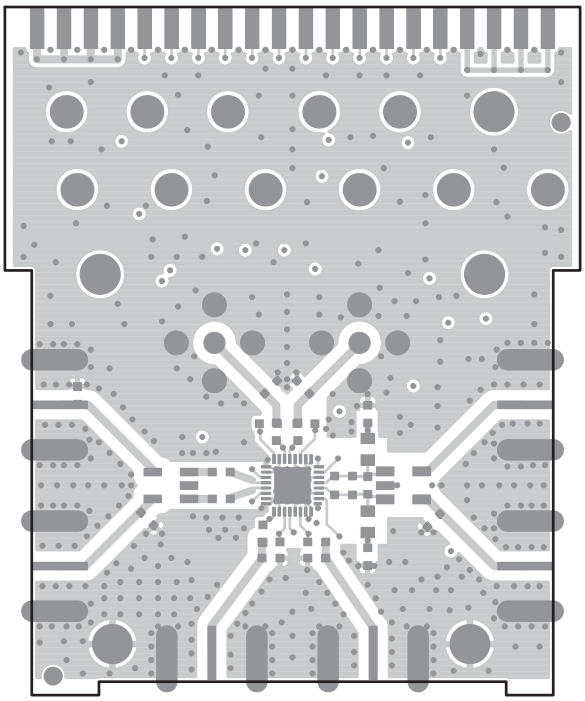


Figure 22. Top Side

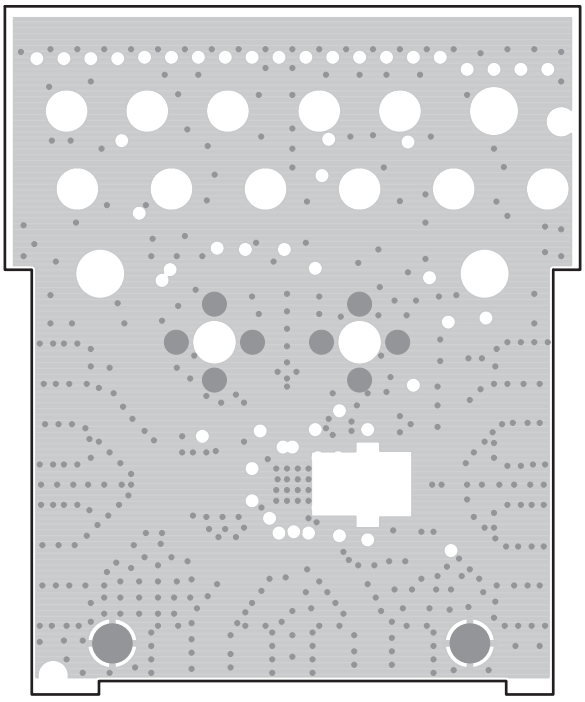


Figure 23. Inner Layer 2 GND

APPLICATIONS INFORMATION

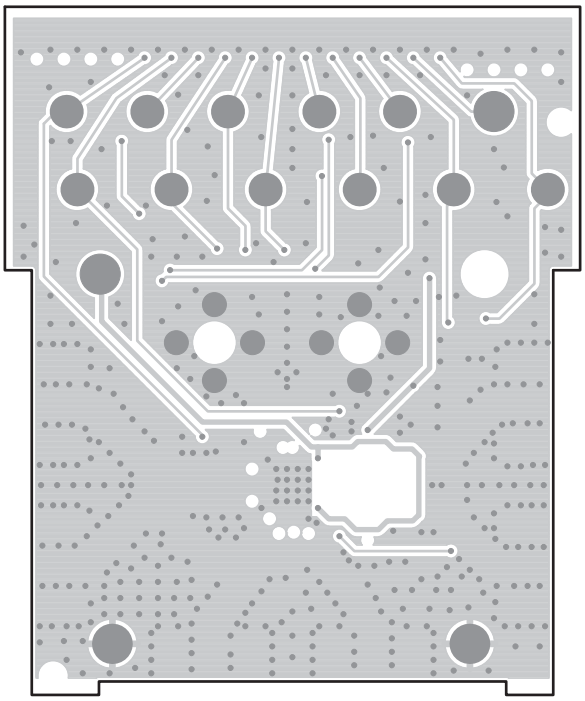


Figure 24. Inner Layer 3 Power

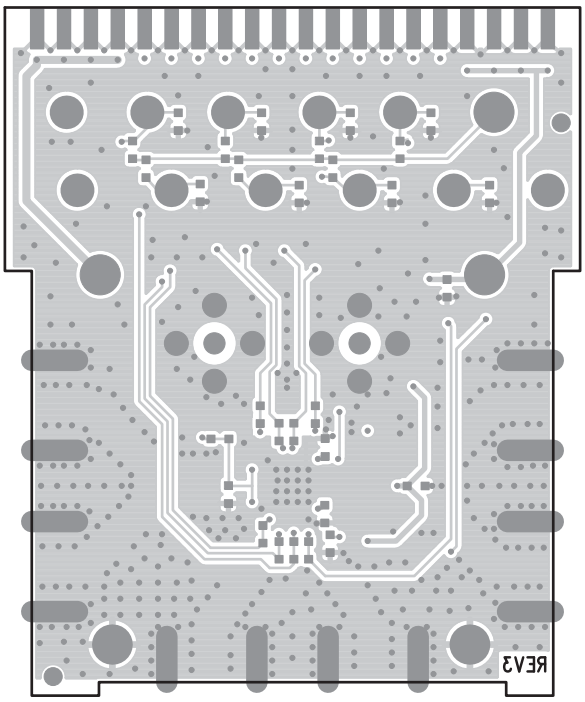


Figure 25. Bottom Side

APPLICATIONS INFORMATION

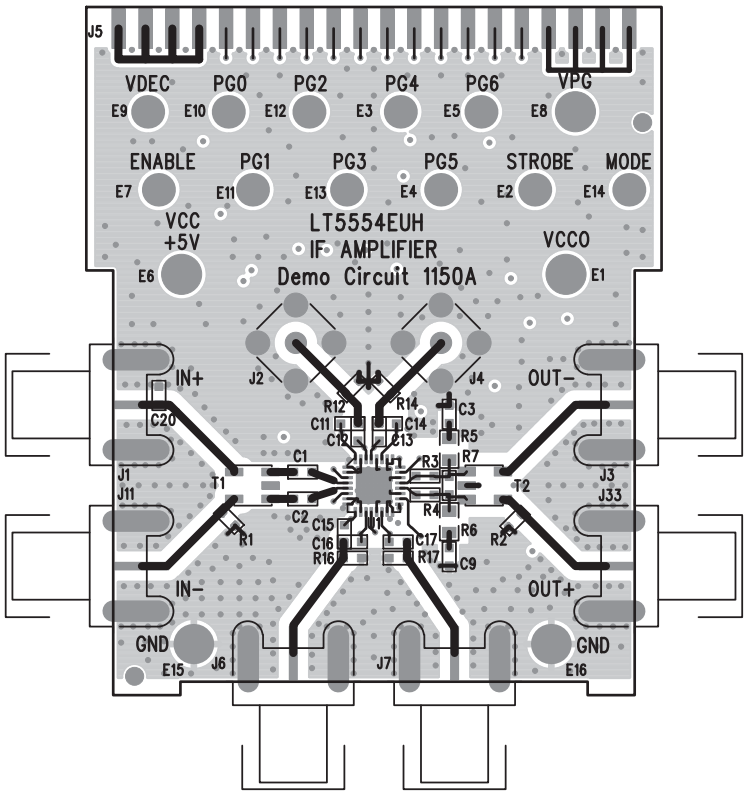


Figure 26. Silkscreen Top

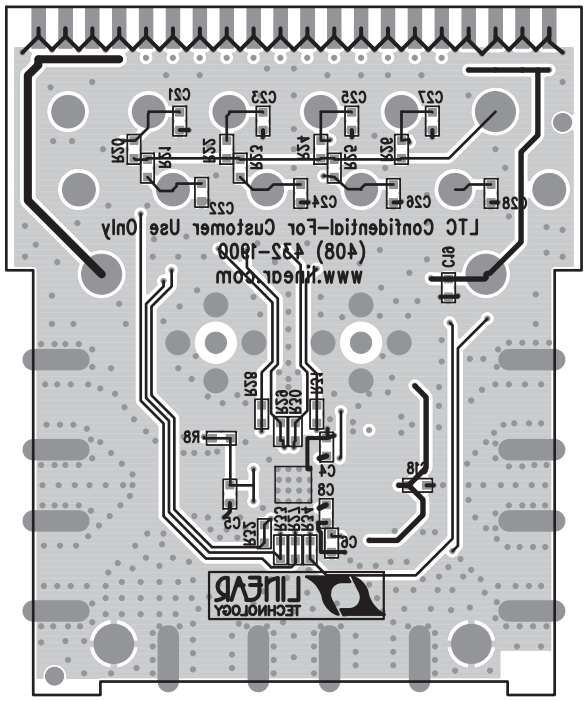
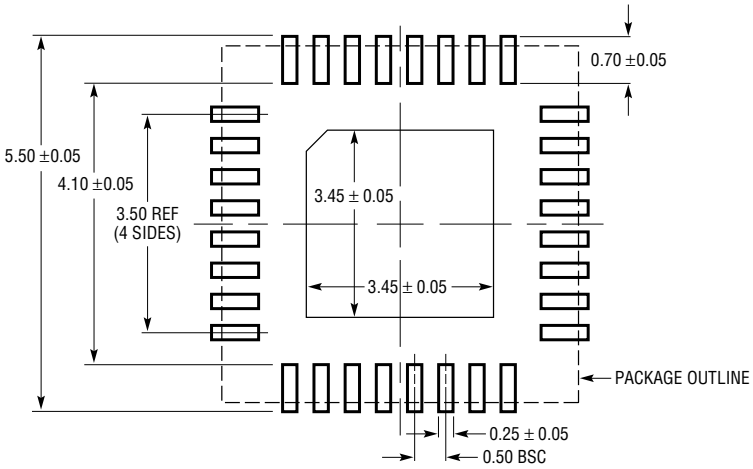


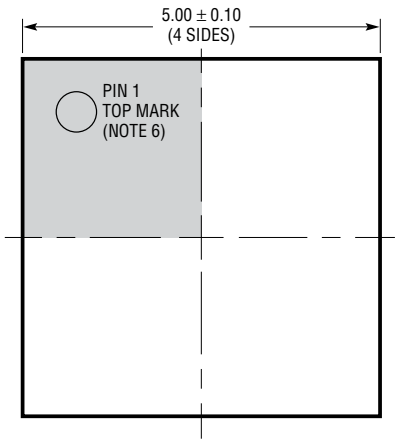
Figure 27. Silkscreen Bottom

PACKAGE DESCRIPTION

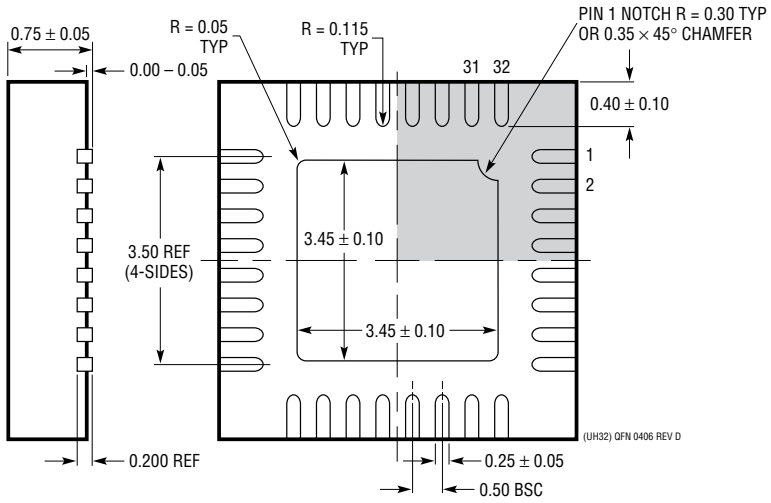
UH Package
32-Lead Plastic QFN (5mm × 5mm)
(Reference LTC DWG # 05-08-1693 Rev D)



RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD



NOTE:
1. DRAWING PROPOSED TO BE A JEDEC PACKAGE OUTLINE
   M0-220 VARIATION WHHD-(X) (TO BE APPROVED)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION
   ON THE TOP AND BOTTOM OF PACKAGE