# 1.8A, 4MHz, Synchronous Step-Down DC/DC Converter

## FEATURES

- **Uses Tiny Capacitors and Inductor**
- **High Frequency Operation: Up to 4MHz**
- **Low $R_{DS(ON)}$ Internal Switches: 0.110Ω**
- High Efficiency: Up to 96%
- Stable with Ceramic Capacitors
- Current Mode Operation for Excellent Line and Load Transient Response
- Short-Circuit Protected
- Low Dropout Operation: 100% Duty Cycle
- Low Shutdown Current: $I_Q \leq 1\mu A$
- Low Quiescent Current: 60µA
- Output Voltages from 0.8V to 5V
- Selectable Burst Mode® Operation
- Sychronizable to External Clock
- Small 3mm × 3mm, 10-Lead DFN Package

## APPLICATIONS

- Notebook Computers
- Digital Cameras
- Cellular Phones
- Handheld Instruments
- Board Mounted Power Supplies

## DESCRIPTION

The LTC®3568 is a constant frequency, synchronous step- down DC/DC converter. Intended for medium power applications, it operates from a 2.5V to 5.5V input voltage range and has a user configurable operating frequency up to 4MHz, allowing the use of tiny, low cost capacitors and inductors 2mm or less in height. The output voltage is adjustable from 0.8V to 5V. Internal sychronous 0.11Ω power switches with 2.4A peak current ratings provide high efficiency. The LTC3568's current mode architecture and external compensation allow the transient response to be optimized over a wide range of loads and output capacitors.

The LTC3568 can be configured for automatic power saving Burst Mode operation to reduce gate charge losses when the load current drops below the level required for continuous operation. For reduced noise and RF interference, the SYNC/MODE pin can be configured to skip pulses or provide forced continuous operation.

To further maximize battery life, the P-channel MOSFET is turned on continuously in dropout (100% duty cycle) with a low quiescent current of 60µA. In shutdown, the device draws <1µA.



## TYPICAL APPLICATION

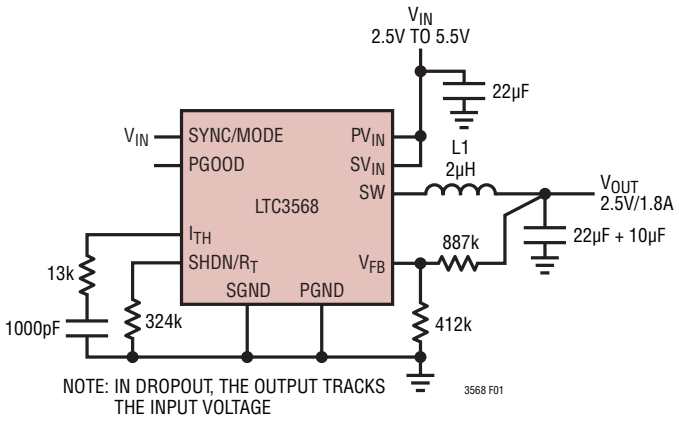
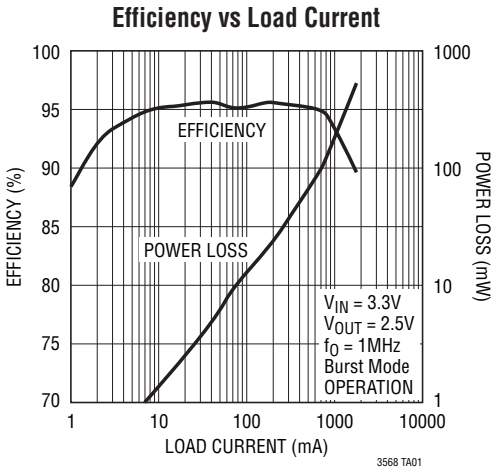



**Figure 1. Step-Down 1.8A Regulator**

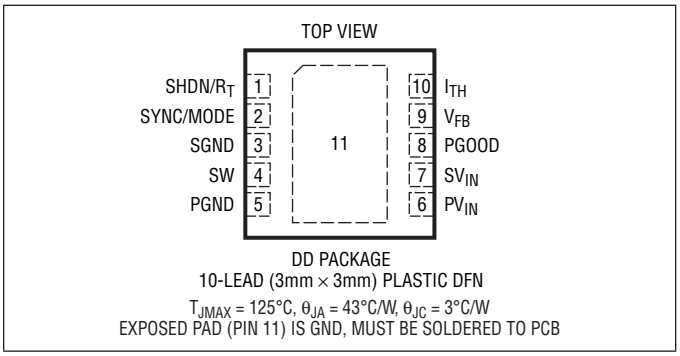


## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

$PV_{IN}$, $SV_{IN}$ Voltages ..... –0.3V to 6V
$V_{FB}$, $I_{TH}$, $SHDN/R_T$ Voltages..... –0.3V to ($V_{IN}$ + 0.3V)
SYNC/MODE Voltage ..... –0.3V to ($V_{IN}$ + 0.3V)
SW Voltage ..... –0.3V to ($V_{IN}$ + 0.3V)
PGOOD Voltage..... –0.3V to 6V
Operating Junction Temperature Range
(Note 2) ..... –40°C to 125°C
Junction Temperature (Notes 5, 8)..... 125°C
Storage Temperature Range ..... –65°C to 125°C

## PIN CONFIGURATION




DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 43°C/W, $\theta_{JC}$ = 3°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC3568EDD#PBF | LTC3568EDD#TRPBF | LCSG | 10-Lead (3mm × 3mm) Plastic DFN | –40°C to 125°C |
| LTC3568IDD#PBF | LTC3568IDD#TRPBF | LCSG | 10-Lead (3mm × 3mm) Plastic DFN | –40°C to 125°C |
| **LEAD BASED FINISH** | **TAPE AND REEL** | **PART MARKING*** | **PACKAGE DESCRIPTION** | **TEMPERATURE RANGE** |
| LTC3568EDD | LTC3568EDD#TR | LCSG | 10-Lead (3mm × 3mm) Plastic DFN | –40°C to 125°C |
| LTC3568IDD | LTC3568IDD#TR | LCSG | 10-Lead (3mm × 3mm) Plastic DFN | –40°C to 125°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{IN}$ = 3.3V, $R_T$ = 324k unless otherwise specified. (Note 2)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Operating Voltage Range | | | 2.25 | | 5.5 | V |
| $I_{FB}$ | Feedback Pin Input Current | (Note 3) | | | | ±0.1 | µA |
| $V_{FB}$ | Feedback Voltage | LTC3568E (Note 3)<br>LTC3568I (Note 3) | ●<br>● | 0.784<br>0.780 | 0.8<br>0.8 | 0.816<br>0.816 | V<br>V |
| $\Delta V_{LINEREG}$ | Reference Voltage Line Regulation | $V_{IN}$ = 2.25V to 5V | | | 0.04 | 0.2 | %/V |
| $\Delta V_{LOADREG}$ | Output Voltage Load Regulation | $I_{TH}$ = 0.36, (Note 3)<br>$I_{TH}$ = 0.84, (Note 3) | ●<br>● | | 0.02<br>–0.02 | 0.2<br>–0.2 | %<br>% |
| $g_{m(EA)}$ | Error Amplifier Transconductance | $I_{TH}$ Pin Load = ±5µA (Note 3) | | | 800 | | µS |
| $I_S$ | Input DC Supply Current (Note 4)<br>Active Mode<br>Sleep Mode<br>Shutdown | <br>$V_{FB}$ = 0.75V, SYNC/MODE = 3.3V<br>$V_{SYNC/MODE}$ = 3.3V, $V_{FB}$ = 1V<br>$V_{SHDN/RT}$ = 3.3V | | | <br>240<br>62<br>0.1 | <br>350<br>100<br>1 | <br>µA<br>µA<br>µA |
| $V_{SHDN/RT}$ | Shutdown Threshold High<br>Active Oscillator Resistor | | | | $V_{IN}$ – 0.6<br>324k | $V_{IN}$ – 0.4<br>1M | V<br>Ω |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. $V_{IN}$ = 3.3V, $R_T$ = 324k unless otherwise specified. (Note 2)**

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $f_{OSC}$ | Oscillator Frequency | $R_T$ = 324k<br>(Note 7) | | 0.85 | 1 | 1.15<br>4 | MHz<br>MHz |
| $f_{SYNC}$ | Synchronization Frequency | (Note 7) | | 0.4 | | 4 | MHz |
| $I_{LIM}$ | Peak Switch Current Limit | $I_{TH}$ = 1.3 | | 2.4 | 3 | 4 | A |
| $R_{DS(ON)}$ | Top Switch On-Resistance (Note 6) | $V_{IN}$ = 3.3V | | | 0.11 | 0.15 | Ω |
| | Bottom Switch On-Resistance (Note 6) | $V_{IN}$ = 3.3V | | | 0.11 | 0.15 | Ω |
| $I_{SW(LKG)}$ | Switch Leakage Current | $V_{IN}$ = 6V, $V_{ITH/RUN}$ = 0V, $V_{FB}$ = 0V | | | 0.01 | 1 | µA |
| $V_{UVLO}$ | Undervoltage Lockout Threshold | $V_{IN}$ Ramping Down | | | 2 | 2.25 | V |
| PGOOD | Power Good Threshold | $V_{FB}$ Ramping Up, SHDN/$R_T$ = 1V<br>$V_{FB}$ Ramping Down, SHDN/$R_T$ = 1V | | | 6.8<br>–7.6 | | %<br>% |
| RPGOOD | Power Good Pull-Down On-Resistance | | | | 118 | 200 | Ω |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC3568 is tested under pulsed load conditions such that $T_J$ = $T_A$. The LTC3568E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3568I is guaranteed over the full –40°C to 125°C operating junction temperature range. The maximum ambient temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistors and other environmental factors.

**Note 3:** The LTC3568 is tested in a feedback loop which servos $V_{FB}$ to the midpoint for the error amplifier ($V_{ITH}$ = 0.6V).

**Note 4:** Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

**Note 5:** $T_J$ is calculated from the ambient $T_A$ and power dissipation $P_D$ according to the following formula:

$$T_J = T_A + (P_D \bullet 43°C/W)$$

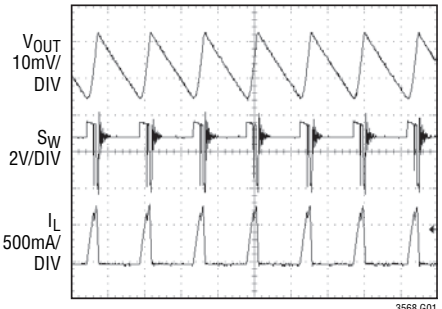
**Note 6:** Switch on-resistance is guaranteed by correlation to wafer level measurements.

**Note 7:** 4MHz operation is guaranteed by design but not production tested and is subject to duty cycle limitations (see Applications Information).

**Note 8:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

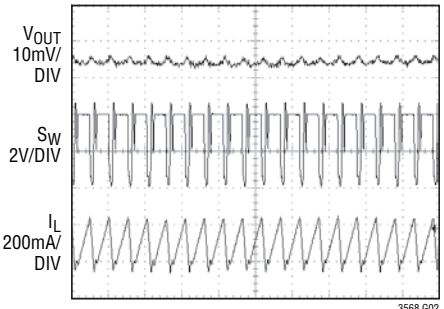
# TYPICAL PERFORMANCE CHARACTERISTICS

### Burst Mode Operation



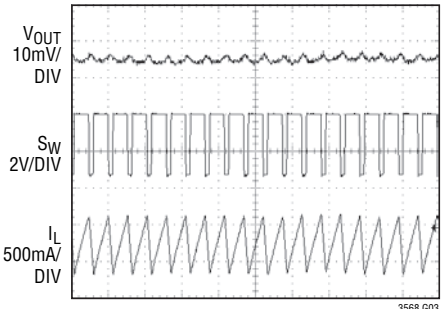

$V_{IN}$ = 3.3V 10µs/DIV
$V_{OUT}$ = 2.5V
$I_{LOAD}$ = 100mA

### Pulse Skipping Mode



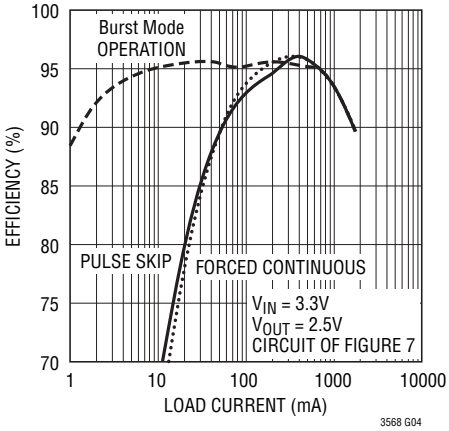

$V_{IN}$ = 3.3V 2µs/DIV
$V_{OUT}$ = 2.5V
$I_{LOAD}$ = 100mA

### Forced Continuous Mode

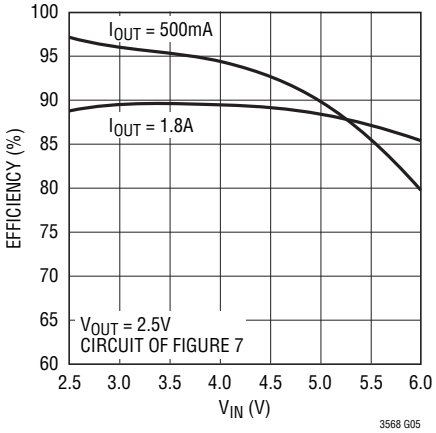



$V_{IN}$ = 3.3V 2µs/DIV
$V_{OUT}$ = 2.5V
$I_{LOAD}$ = 100mA

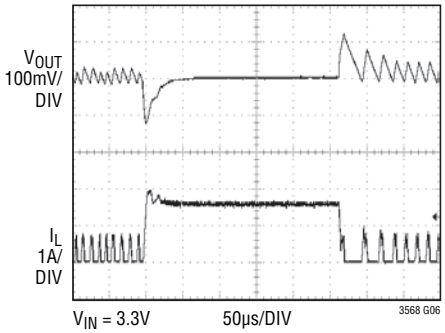
### Efficiency vs Load Current




### Efficiency vs $V_{IN}$

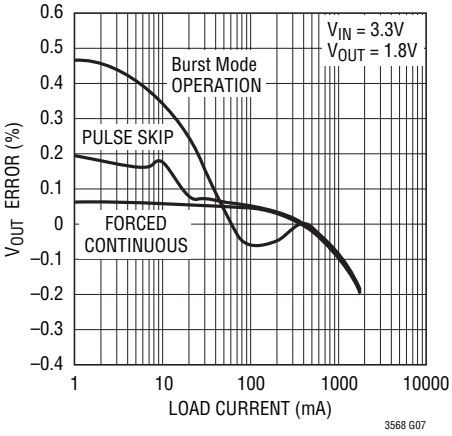



### Load Step

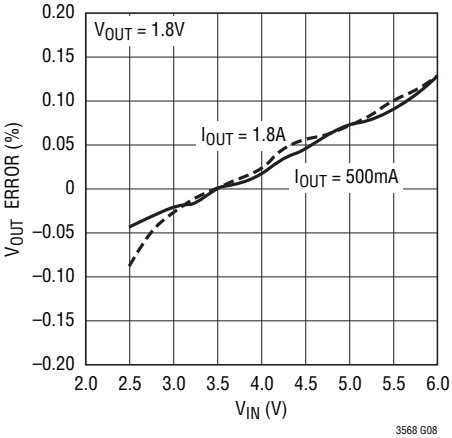



$V_{IN}$ = 3.3V 50µs/DIV
$V_{OUT}$ = 2.5V
$I_{LOAD}$ = 180mA TO 1.8A

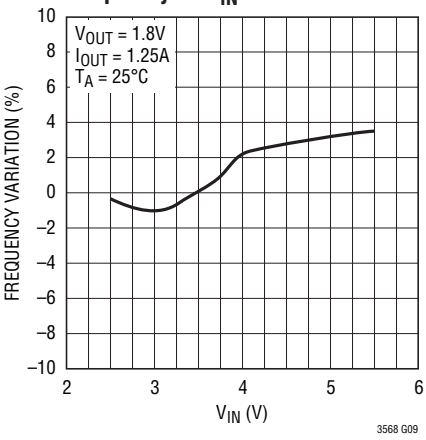
### Load Regulation




### Line Regulation

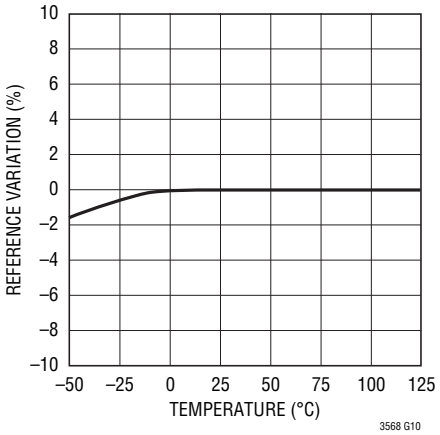



### Frequency vs $V_{IN}$

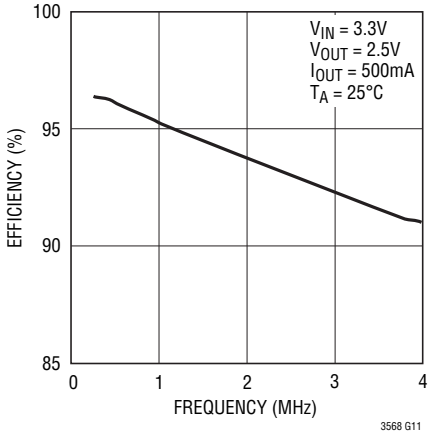


# TYPICAL PERFORMANCE CHARACTERISTICS

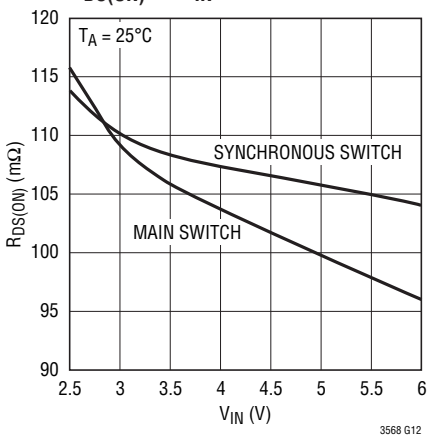
**Frequency Variation vs Temperature**



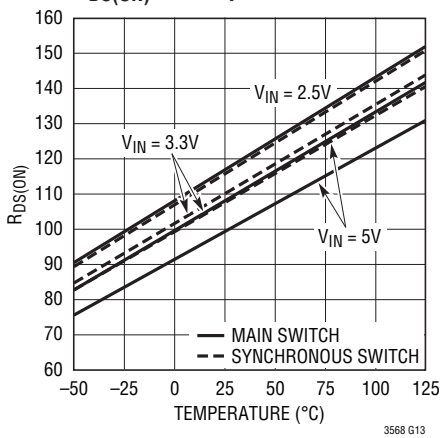

**Efficiency vs Frequency**




**$R_{DS(ON)}$ vs $V_{IN}$**




**$R_{DS(ON)}$ vs Temperature**



## PIN FUNCTIONS

**SHDN/$R_T$ (Pin 1):** Combination Shutdown and Timing Resistor Pin. The oscillator frequency is programmed by connecting a resistor from this pin to ground. Forcing this pin to $SV_{IN}$ causes the device to be shut down. In shutdown all functions are disabled.

**SYNC/MODE (Pin 2):** Combination Mode Selection and Oscillator Synchronization Pin. This pin controls the operation of the device. When tied to $SV_{IN}$ or SGND, Burst Mode operation or pulse skipping mode is selected, respectively. If this pin is held at half of $SV_{IN}$, the forced continuous mode is selected. The oscillation frequency can be syncronized to an external oscillator applied to this pin. When synchronized to an external clock pulse skip mode is selected.

**SGND (Pin 3):** The Signal Ground Pin. All small signal components and compensation components should be connected to this ground (see Board Layout Considerations).

**SW (Pin 4):** The Switch Node Connection to the Inductor. This pin swings from $PV_{IN}$ to PGND.

**PGND (Pin 5):** Main Power Ground Pin. Connect to the (–) terminal of $C_{OUT}$, and (–) terminal of $C_{IN}$.

**$PV_{IN}$ (Pin 6):** Main Supply Pin. Must be closely decoupled to PGND.

**$SV_{IN}$ (Pin 7):** The Signal Power Pin. All active circuitry is powered from this pin. Must be closely decoupled to SGND. $SV_{IN}$ must be greater than or equal to $PV_{IN}$.

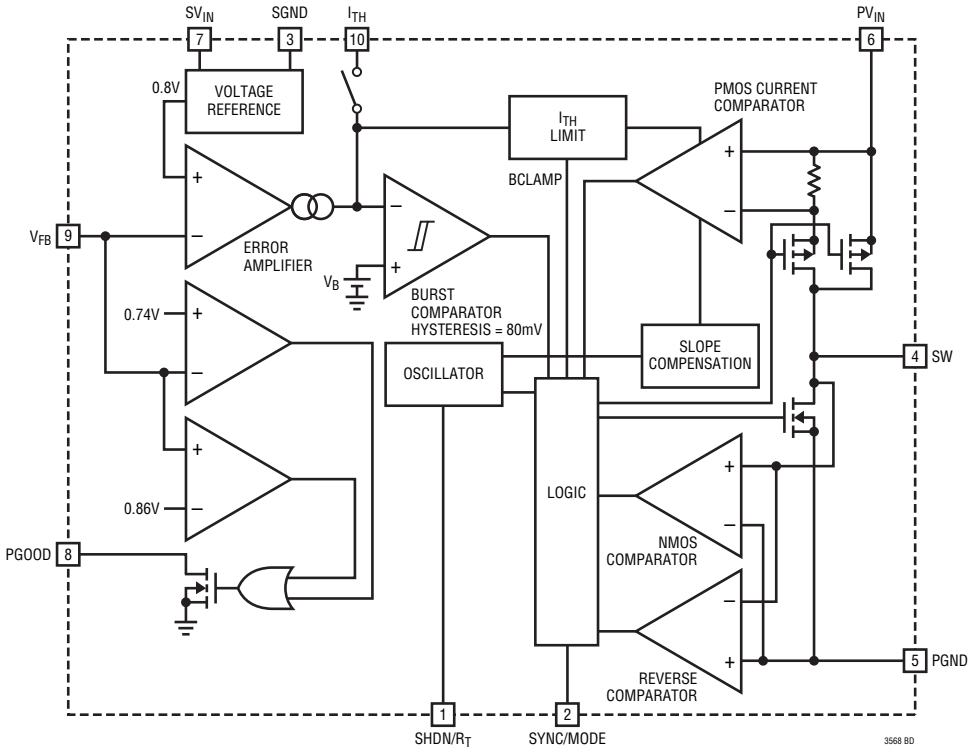
**PGOOD (Pin 8):** The Power Good Pin. This common drain logic output is pulled to SGND when the output voltage is not within ±7.5% of regulation.

**$V_{FB}$ (Pin 9):** Receives the feedback voltage from the external resistive divider across the output. Nominal voltage for this pin is 0.8V.

**$I_{TH}$ (Pin 10):** Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Nominal voltage range for this pin is 0V to 1.5V.

**GND (Exposed Pad Pin 11):** Thermal Ground. Connect to SGND and solder to the PCB for rated thermal performance.

## BLOCK DIAGRAM



## OPERATION

The LTC3568 uses a constant frequency, current mode architecture. The operating frequency is determined by the value of the $R_T$ resistor or can be synchronized to an external oscillator. To suit a variety of applications, the selectable Mode pin, allows the user to trade-off noise for efficiency.

The output voltage is set by an external divider returned to the $V_{FB}$ pin. An error amplfier compares the divided output voltage with a reference voltage of 0.8V and adjusts the peak inductor current accordingly. Overvoltage and undervoltage comparators will pull the PGOOD output low if the output voltage is not within ±7.5%.

### Main Control Loop

During normal operation, the top power switch (P-channel MOSFET) is turned on at the beginning of a clock cycle when the $V_{FB}$ voltage is below the the reference voltage. The current into the inductor and the load increases until the current limit is reached. The switch turns off and energy stored in the inductor flows through the bottom switch (N-channel MOSFET) into the load until the next clock cycle.

The peak inductor current is controlled by the voltage on the $I_{TH}$ pin, which is the output of the error amplifier.This amplifier compares the $V_{FB}$ pin to the 0.8V reference. When the load current increases, the $V_{FB}$ voltage decreases slightly below the reference. This decrease causes the error amplifier to increase the $I_{TH}$ voltage until the average inductor current matches the new load current.

The main control loop is shut down by pulling the SHDN/$R_T$ pin to $SV_{IN}$. A digital soft-start is enabled after shutdown, which will slowly ramp the peak inductor current up over 1024 clock cycles or until the output reaches regulation, whichever is first. Soft-start can be lengthened by ramping the voltage on the $I_{TH}$ pin (see Applications Information section).

### Low Current Operation

Three modes are available to control the operation of the LTC3568 at low currents. All three modes automatically switch from continuous operation to to the selected mode when the load current is low.

To optimize efficiency, the Burst Mode operation can be selected. When the load is relatively light, the LTC3568 automatically switches into Burst Mode operation in which the PMOS switch operates intermittently based on load demand. By running cycles periodically, the switching losses which are dominated by the gate charge losses of the power MOSFETs are minimized. The main control loop is interrupted when the output voltage reaches the desired regulated value. The hysteretic voltage comparator B trips when $I_{TH}$ is below 0.24V, shutting off the switch and reducing the power. The output capacitor and the inductor supply the power to the load until $I_{TH}$/RUN exceeds 0.31V, turning on the switch and the main control loop which starts another cycle.

For lower output voltage ripple at low currents, pulse skipping mode can be used. In this mode, the LTC3568 continues to switch at a constant frequency down to very low currents, where it will eventually begin skipping pulses.

Finally, in forced continuous mode, the inductor current is constantly cycled which creates a fixed output voltage ripple at all output current levels. This feature is desirable in telecommunications since the noise is at a constant frequency and is thus easy to filter out. Another advantage of this mode is that the regulator is capable of both sourcing current into a load and sinking some current from the output.

### Dropout Operation

When the input supply voltage decreases toward the output voltage, the duty cycle increases to 100% which is the dropout condition. In dropout, the PMOS switch is turned on continuously with the output voltage being equal to the input voltage minus the voltage drops across the internal P-channel MOSFET and the inductor.

### Low Supply Operation

The LTC3568 incorporates an undervoltage lockout circuit which shuts down the part when the input voltage drops below about 2V.

## APPLICATIONS INFORMATION

A general LTC3568 application circuit is shown in Figure 5. External component selection is driven by the load requirement, and begins with the selection of the inductor L1. Once L1 is chosen, $C_{IN}$ and $C_{OUT}$ can be selected.

### Operating Frequency

Selection of the operating frequency is a tradeoff between efficiency and component size. High frequency operation allows the use of smaller inductor and capacitor values. Operation at lower frequencies improves efficiency by reducing internal gate charge losses but requires larger inductance values and/or capacitance to maintain low output ripple voltage.

The operating frequency, $f_O$, of the LTC3568 is determined by an external resistor that is connected between the $R_T$ pin and ground. The value of the resistor sets the ramp current that is used to charge and discharge an internal timing capacitor within the oscillator and can be calculated by using the following equation:

$$R_T = 9.78 \bullet 10^{11} (f_O)^{-1.08} (\Omega)$$

or can be selected using Figure 2.

The maximum usable operating frequency is limited by the minimum on-time and the duty cycle. This can be calculated as:

$$f_{O(MAX)} \approx 6.67 \bullet (V_{OUT} / V_{IN(MAX)}) \text{ (MHz)}$$

The minimum frequency is limited by leakage and noise coupling due to the large resistance of $R_T$.

### Inductor Selection

Although the inductor does not influence the operating frequency, the inductor value has a direct effect on ripple current. The inductor ripple current $\Delta I_L$ decreases with higher inductance and increases with higher $V_{IN}$ or $V_{OUT}$:

$$\Delta I_L = \frac{V_{OUT}}{f_O \bullet L} \bullet \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of $\Delta I_L$ allows the use of low inductances, but results in higher output voltage ripple, greater core losses, and lower output current capability.

A reasonable starting point for setting ripple current is $\Delta I_L = 0.4 \bullet I_{OUT}$, where $I_{OUT}$ is the maximum output current. The largest ripple current $\Delta I_L$ occurs at the maximum input voltage. To guarantee that the ripple current stays below a specified maximum, the inductor value should be chosen according to the following equation:

$$L = \frac{V_{OUT}}{f_O \bullet \Delta I_L} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

The inductor value will also have an effect on Burst Mode operation. The transition from low current operation begins when the peak inductor current falls below a level set by the burst clamp. Lower inductor values result in higher ripple current which causes this to occur at lower load currents. This causes a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to increase.

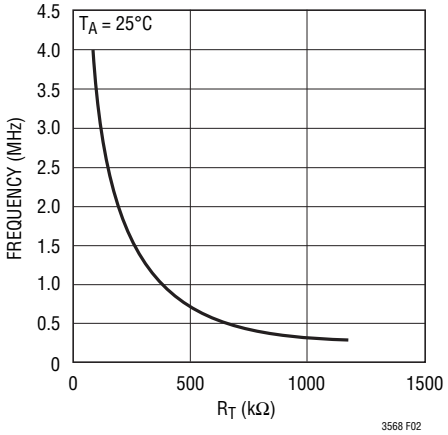



**Figure 2. Frequency vs $R_T$**

### Inductor Core Selection

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and don't radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price vs size requirements and any radiated field/EMI requirements than on what the LTC3568 requires to operate. Table 1 shows some typical surface mount inductors that work well in LTC3568 applications.

## APPLICATIONS INFORMATION

**Table 1. Representative Surface Mount Inductors**

| MANU-FACTURER | PART NUMBER | VALUE | MAX DC CURRENT | DCR | HEIGHT |
|---|---|---|---|---|---|
| Toko | A914BYW-2R2M (D52LC) | 2.2µH | 2.05A | 49mΩ | 2mm |
| Toko | A915Y-2R0M (D53LC-A) | 2µH | 3.3A | 22mΩ | 3mm |
| Toko | A918CY-2R0M (D62LCB) | 2µH | 2.33A | 24mΩ | 2mm |
| Coilcraft | D01608C-222 | 2.2µH | 2.3A | 70mΩ | 3mm |
| Sumida | CDRH2D18/HP1R7 | 1.7µH | 1.8A | 35mΩ | 2mm |
| Sumida | CDRH4D282R2 | 2.2µH | 2.04A | 23mΩ | 3mm |
| Sumida | CDC5D232R2 | 2.2µH | 2.16A | 30mΩ | 2.5mm |
| TDK | VLCF4020T-1R8N1R9 | 1.8µH | 1.97A | 46mΩ | 2mm |
| Taiyo Yuden | N06DB2R2M | 2.2µH | 3.2A | 29mΩ | 3.2mm |
| Taiyo Yuden | N05DB2R2M | 2.2µH | 2.9A | 32mΩ | 2.8mm |
| Cooper | SD14-2R0 | 2µH | 2.37A | 45mΩ | 1.45mm |

### Catch Diode Selection

A catch diode is not necessary.

### Input Capacitor ($C_{IN}$) Selection

In continuous mode, the input current of the converter is a square wave with a duty cycle of approximately $V_{OUT}/V_{IN}$. To prevent large voltage transients, a low equivalent series resistance (ESR) input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} \approx I_{MAX} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

where the maximum average output current $I_{MAX}$ equals the peak current minus half the peak-to-peak ripple current, $I_{MAX} = I_{LIM} - \Delta I_L/2$.

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst case is commonly used to design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours lifetime. This makes it advisable to further derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet the size or height requirements of the design. An additional 0.1µF to 1µF ceramic capacitor is also recommended on $V_{IN}$ for high frequency decoupling, when not using an all ceramic capacitor solution.

### Output Capacitor ($C_{OUT}$) Selection

The selection of $C_{OUT}$ is driven by the required ESR to minimize voltage ripple and load step transients. Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple ($\Delta V_{OUT}$) is determined by:

$$\Delta V_{OUT} \approx \Delta I_L \left( ESR + \frac{1}{8 f_O C_{OUT}} \right)$$

where f = operating frequency, $C_{OUT}$ = output capacitance and $\Delta I_L$ = ripple current in the inductor. The output ripple is highest at maximum input voltage since $\Delta I_L$ increases with input voltage. With $\Delta I_L = 0.4 \bullet I_{OUT}$ the output ripple will be less than 100mV at maximum $V_{IN}$ and $f_O$ = 1MHz with:

$$ESR C_{OUT} < 130m\Omega$$

Once the ESR requirements for $C_{OUT}$ have been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement, except for an all ceramic solution.

In surface mount applications, multiple capacitors may have to be paralleled to meet the capacitance, ESR or RMS current handling requirement of the application. Aluminum electrolytic, special polymer, ceramic and dry tantulum capacitors are all available in surface mount packages. The OS-CON semiconductor dielectric capacitor available from Sanyo has the lowest ESR(size) product of any aluminum electrolytic at a somewhat higher price. Special polymer capacitors, such as Sanyo POSCAP, offer very low ESR, but have a lower capacitance density than other types. Tantalum capacitors have the highest capacitance density, but it has a larger ESR and it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalums, avalable in case heights ranging from 2mm to 4mm. Aluminum electrolytic capacitors have a significantly larger ESR, and is often used in extremely cost-sensitive applications provided that consideration is given to ripple current ratings and long term reliability.

## APPLICATIONS INFORMATION

Ceramic capacitors have the lowest ESR and cost but also have the lowest capacitance density, a high voltage and temperature coefficient and exhibit audible piezoelectric effects. In addition, the high Q of ceramic capacitors along with trace inductance can lead to significant ringing. Other capacitor types include the Panasonic specialty polymer (SP) capacitors.

In most cases, 0.1µF to 1µF of ceramic capacitors should also be placed close to the LTC3568 in parallel with the main capacitors for high frequency decoupling.

### Ceramic Input and Output Capacitors

Higher value, lower cost ceramic capacitors are now becoming available in smaller case sizes. These are tempting for switching regulator use because of their very low ESR. Unfortunately, the ESR is so low that it can cause loop stability problems. Solid tantalum capacitor ESR generates a loop "zero" at 5kHz to 50kHz that is instrumental in giving acceptable loop phase margin. Ceramic capacitors remain capacitive to beyond 300kHz and ususally resonate with their ESL before ESR becomes effective. Also, ceramic caps are prone to temperature effects which requires the designer to check loop stability over the operating temperature range. To minimize their large temperature and voltage coefficients, only X5R or X7R ceramic capacitors should be used. A good selection of ceramic capacitors is available from Taiyo Yuden, TDK and Murata.

Great care must be taken when using only ceramic input and output capacitors. When a ceramic capacitor is used at the input and the power is being supplied through long wires, such as from a wall adapter, a load step at the output can induce ringing at the $V_{IN}$ pin. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, the ringing at the input can be large enough to damage the part.

Since the ESR of a ceramic capacitor is so low, the input and output capacitor must instead fulfill a charge storage requirement. During a load step, the output capacitor must instantaneously supply the current to support the load until the feedback loop raises the switch current enough to support the load. The time required for the feedback loop to respond is dependent on the compensation components and the output capacitor size. Typically, 3 to 4 cycles are required to respond to a load step, but only in the first cycle does the output drop linearly. The output droop, $V_{DROOP}$ is usually about 2 to 3 times the linear drop of the first cycle. Thus, a good place to start is with the output capacitor size of approximately:

$$C_{OUT} \approx 2.5 \frac{\Delta I_{OUT}}{f_O \bullet V_{DROOP}}$$

More capacitance may be required depending on the duty cycle and load step requirements.

In most applications, the input capacitor is merely required to supply high frequency bypassing, since the impedance to the supply is very low. A 22µF ceramic capacitor is usually enough for these conditions.

### Setting the Output Voltage

The LTC3568 develops a 0.8V reference voltage between the feedback pin, $V_{FB}$, and the signal ground as shown in Figure 5. The output voltage is set by a resistive divider according to the following formula:

$$V_{OUT} \approx 0.8V \left(1 + \frac{R2}{R1}\right)$$

Keeping the current small (<5µA) in these resistors maximizes efficiency, but making them too small may allow stray capacitance to cause noise problems and reduce the phase margin of the error amp loop.

To improve the frequency response, a feed-forward capacitor $C_F$ may also be used. Great care should be taken to route the $V_{FB}$ line away from noise sources, such as the inductor or the SW line.

### Shutdown and Soft-Start

The SHDN/$R_T$ pin is a dual purpose pin that sets the oscillator frequency and provides a means to shut down the LTC3568. This pin can be interfaced with control logic in several ways, as shown in Figure 3(a) and Figure 3(b).

The $I_{TH}$ pin is primarily for loop compensation, but it can also be used to increase the soft-start time. Soft start reduces surge currents from $V_{IN}$ by gradually increasing the peak inductor current. Power supply sequencing can also be accomplished using this pin. The LTC3568 has an

## APPLICATIONS INFORMATION

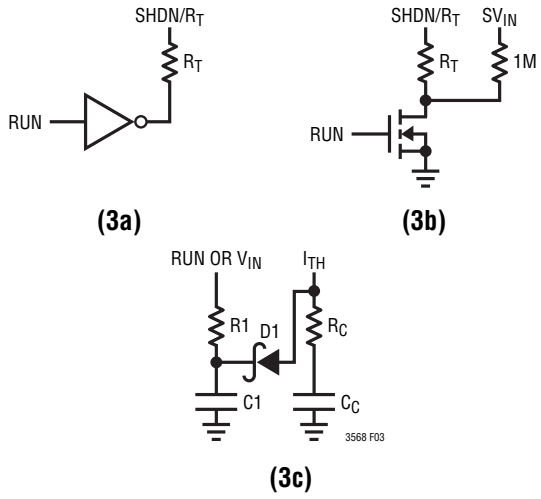



**Figure 3. SHDN/$R_T$ Pin Interfacing and External Soft-Start**

internal digital soft-start which steps up a clamp on $I_{TH}$ over 1024 clock cycles, as can be seen in Figure 4.

The soft-start time can be increased by ramping the voltage on $I_{TH}$ during start-up as shown in Figure 3(c). As the voltage on $I_{TH}$ ramps through its operating range the internal peak current limit is also ramped at a proportional linear rate.

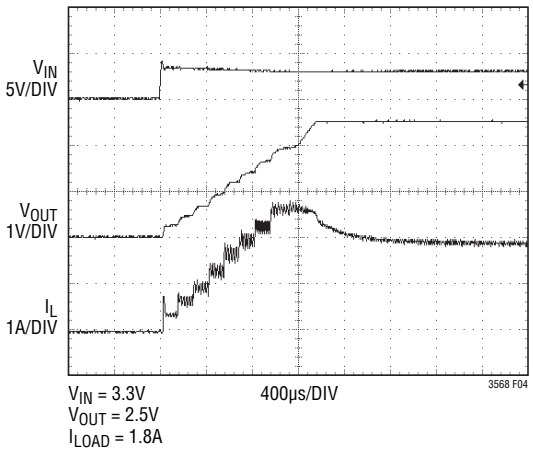



**Figure 4. Digital Soft-Start**

### Mode Selection and Frequency Synchronization

The SYNC/MODE pin is a multipurpose pin which provides mode selection and frequency synchronization. Connecting this pin to $V_{IN}$ enables Burst Mode operation, which provides the best low current efficiency at the cost of a higher output voltage ripple. When this pin is connected to ground, pulse skipping operation is selected which provides the lowest output voltage and current ripple at the cost of low current efficiency. Applying a voltage between $SV_{IN}$ – 1V and 1V, results in forced continuous mode, which creates a fixed output ripple and is capable of sinking some current (about $1/2\Delta I_L$). Since the switching noise is constant in this mode, it is also the easiest to filter out. In many cases, the output voltage can be simply connected to the SYNC/MODE pin, giving the forced continuous mode, except at startup.

The LTC3568 can also be synchronized to an external clock signal by the SYNC/MODE pin. The internal oscillator frequency should be set to 20% lower than the external clock frequency to ensure adequate slope compensation, since slope compensation is derived from the internal oscillator. During synchronization, the mode is set to pulse skipping and the top switch turn on is synchronized to the rising edge of the external clock.

### Checking Transient Response

The OPTI-LOOP® compensation allows the transient response to be optimized for a wide range of loads and output capacitors. The availability of the $I_{TH}$ pin not only allows optimization of the control loop behavior but also provides a DC-coupled and AC filtered closed loop response test point. The DC step, rise time and settling at this test point truly reflects the closed loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin.

The $I_{TH}$ external components shown in the Figure 1 circuit will provide an adequate starting point for most applications. The series R-C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop feedback factor gain and phase. An output current pulse of 20% to 100% of full load current having a rise time of 1µs to 10µs will produce output voltage and $I_{TH}$ pin waveforms

## APPLICATIONS INFORMATION

that will give a sense of the overall loop stability without breaking the feedback loop.

Switching regulators take several cycles to respond to a step in load current. When a load step occurs, $V_{OUT}$ immediately shifts by an amount equal to $\Delta I_{LOAD} \bullet ESR$, where ESR is the effective series resistance of $C_{OUT}$. $\Delta I_{LOAD}$ also begins to charge or discharge $C_{OUT}$ generating a feedback error signal used by the regulator to return $V_{OUT}$ to its steady-state value. During this recovery time, $V_{OUT}$ can be monitored for overshoot or ringing that would indicate a stability problem.

The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine phase margin. The gain of the loop increases with R and the bandwidth of the loop increases with decreasing C. If R is increased by the same factor that C is decreased, the zero frequency will be kept the same, thereby keeping the phase the same in the most critical frequency range of the feedback loop. In addition, a feedforward capacitor $C_F$ can be added to improve the high frequency response, as shown in Figure 5. Capacitor $C_F$ provides phase lead by creating a high frequency zero with R2 which improves the phase margin.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Linear Technology Application Note 76.

Although a buck regulator is capable of providing the full output current in dropout, it should be noted that as the input voltage $V_{IN}$ drops toward $V_{OUT}$, the load step capability does decrease due to the decreasing voltage across the inductor. Applications that require large load step capability near dropout should use a different topology such as SEPIC, Zeta or single inductor, positive buck/boost.

In some applications, a more severe transient can be caused by switching in loads with large (>1uF) input capacitors. The discharged input capacitors are effectively put in parallel with $C_{OUT}$, causing a rapid drop in $V_{OUT}$. No regulator can deliver enough current to prevent this problem, if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A hot swap controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection, and soft-starting.

### Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%Efficiency = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of

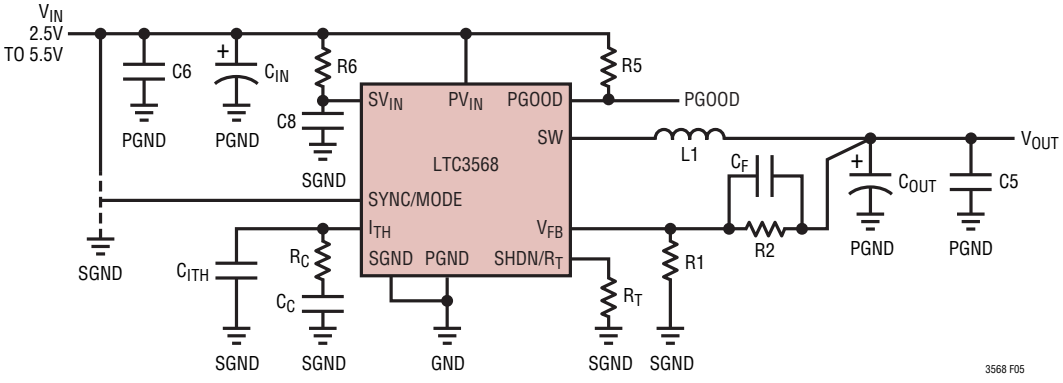



**Figure 5. LTC3568 General Schematic**

## APPLICATIONS INFORMATION

the losses in LTC3568 circuits: 1) LTC3568 $V_{IN}$ current, 2) switching losses, 3) $I^2R$ losses, 4) other losses.

1. The $V_{IN}$ current is the DC supply current given in the electrical characteristics which excludes MOSFET driver and control currents. $V_{IN}$ current results in a small loss that increases with $V_{IN}$, even at no load.

2. The switching current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $V_{IN}$ to ground. The resulting dQ/dt is a current out of $V_{IN}$ that is typically much larger than the DC bias current. In continuous mode, $I_{GATECHG} = f_O(QT + QB)$, where QT and QB are the gate charges of the internal top and bottom MOSFET switches. The gate charge losses are proportional to $V_{IN}$ and thus their effects will be more pronounced at higher supply voltages.

3. $I^2R$ Losses are calculated from the DC resistances of the internal switches, $R_{SW}$, and external inductor, RL. In continuous mode, the average output current flowing through inductor L is "chopped" between the internal top and bottom switches. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

   $$R_{SW} = (R_{DS(ON)}TOP)(DC) + (R_{DS(ON)}BOT)(1 – DC)$$

   The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain $I^2R$ losses:

   $$I^2R \text{ losses} = I_{OUT}2(R_{SW} + RL)$$

4. Other "hidden" losses such as copper trace and internal battery resistances can account for additional efficiency degradations in portable systems. It is very important to include these "system" level losses in the design of a system. The internal battery and fuse resistance losses can be minimized by making sure that $C_{IN}$ has adequate charge storage and very low ESR at the switching frequency. Other losses including diode conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

### Thermal Considerations

In a majority of applications, the LTC3568 does not dissipate much heat due to its high efficiency. However, in applications where the LTC3568 is running at high ambient temperature with low supply voltage and high duty cycles, such as in dropout, the heat dissipated may exceed the maximum junction temperature of the part. If the junction temperature reaches approximately 150°C, both power switches will be turned off and the SW node will become high impedance.

To avoid the LTC3568 from exceeding the maximum junction temperature, the user will need to do some thermal analysis. The goal of the thermal analysis is to determine whether the power dissipated exceeds the maximum junction temperature of the part. The temperature rise is given by:

$$T_{RISE} = P_D \bullet \theta_{JA}$$

where $P_D$ is the power dissipated by the regulator and $\theta_{JA}$ is the thermal resistance from the junction of the die to the ambient temperature.

The junction temperature, $T_J$, is given by:

$$T_J = T_{RISE} + T_{AMBIENT}$$

As an example, consider the case when the LTC3568 is in dropout at an input voltage of 3.3V with a load current of 1.8A with a 70°C ambient temperature. From the Typical Performance Characteristics graph of Switch Resistance, the $R_{DS(ON)}$ resistance of the P-channel switch is 0.125Ω. Therefore, power dissipated by the part is:

$$P_D = I^2 \bullet R_{DS(ON)} = 405mW$$

The DFN package junction-to-ambient thermal resistance, $\theta_{JA}$ is 43°C/W. Therefore, the junction temperature of the regulator operating in a 70°C ambient temperature is approximately:

$$T_J = 0.405 \bullet 43 + 70 = 87.4°C$$

Remembering that the above junction temperature is obtained from an $R_{DS(ON)}$ at 70°C, we might recalculate the junction temperature based on a higher $R_{DS(ON)}$ since it increases with temperature. However, we can safely assume that the actual junction temperature will not exceed the absolute maximum junction temperature of 125°C.

## APPLICATIONS INFORMATION

### Design Example

As a design example, consider using the LTC3568 in a typical application with $V_{IN}$ = 5V. The load requires a maximum of 1.8A in active mode and 10mA in standby mode. The output voltage is $V_{OUT}$ = 2.5V. Since the load still needs power in standby, Burst Mode operation is selected for good low load efficiency.

First, calculate the timing resistor:

$$R_T = 9.78 \bullet 10^{11} (1MHz)^{-1.08} = 323.8k$$

Use a standard value of 324k. Next, calculate the inductor value for about 40% ripple current at maximum $V_{IN}$:

$$L = \frac{2.5V}{1MHz \bullet 720mA} \bullet \left(1 - \frac{2.5V}{5V}\right) = 1.7\mu H$$

Choosing the closest inductor from a vendor of 2µH, results in a maximum ripple current of:

$$\Delta I_L = \frac{2.5V}{1MHz \bullet 2\mu} \bullet \left(1 - \frac{2.5V}{5V}\right) = 625mA$$

For cost reasons, a ceramic capacitor will be used. $C_{OUT}$ selection is then based on load step droop instead of ESR requirements. For a 5% output droop:

$$C_{OUT} \approx 2.5 \frac{1.8A}{1MHz \bullet (5\% \bullet 2.5V)} = 36\mu F$$

The closest standard value is 22µF plus 10µF. Since the supply's output impedance is very low, $C_{IN}$ is typically a 22µF. In noisy environments, decoupling $SV_{IN}$ from $PV_{IN}$ with an R6/C8 filter of 1Ω/0.1µF may help, but is typically not needed.

The output voltage can now be programmed by choosing the values of R1 and R2. To maintain high efficiency, the current in these resistors should be kept small. Choosing 2µA with the 0.8V feedback voltage makes R1~400k. A close standard 1% resistor is 412k and R2 is then 887k.

The compensation should be optimized for these components by examining the load step response but a good place to start for the LTC3568 is with a 13kΩ and 1000pF filter. The output capacitor may need to be increased depending on the actual undershoot during a load step.

The PGOOD pin is a common drain output and requires a pull-up resistor. A 100k resistor is used for adequate speed.

Figure 1 shows the complete schematic for this design example.

### Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3568. These items are also illustrated graphically in the layout diagram of Figure 6. Check the following in your layout:

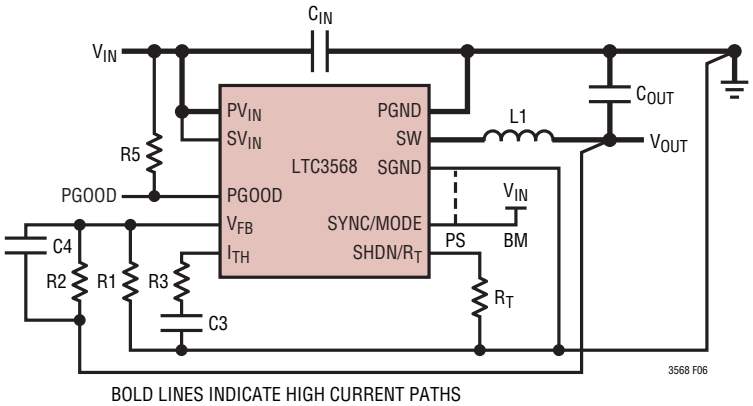
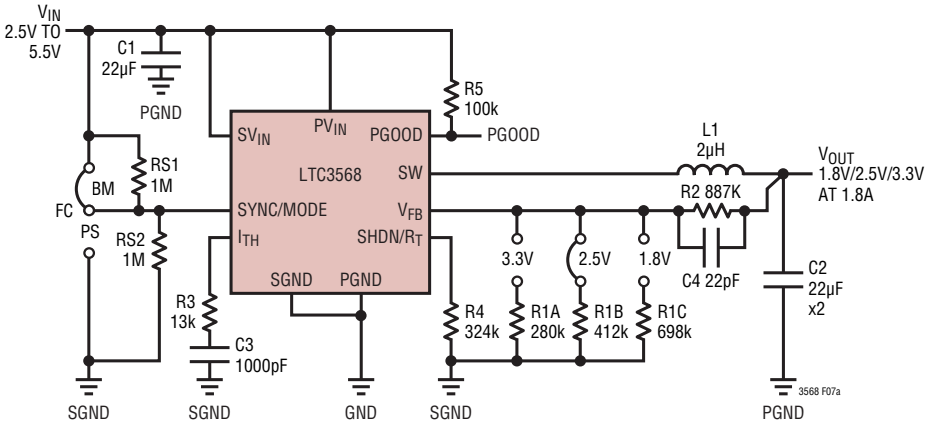



**Figure 6. LTC3568 Layout Diagram (See Board Layout Checklist)**

## APPLICATIONS INFORMATION

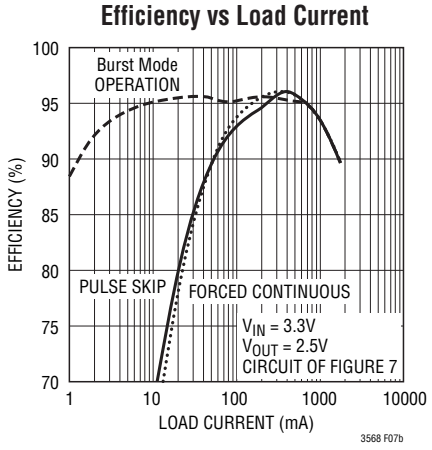
1. Does the capacitor $C_{IN}$ connect to the power $V_{IN}$ (Pin 6) and power GND (Pin 5) as close as possible? This capacitor provides the AC current to the internal power MOSFETs and their drivers.
2. Are the $C_{OUT}$ and L1 closely connected? The (–) plate of $C_{OUT}$ returns current to PGND and the (–) plate of $C_{IN}$.
3. The resistor divider, R1 and R2, must be connected between the (+) plate of $C_{OUT}$ and a ground line terminated near SGND (Pin 3). The feedback signal $V_{FB}$ should be routed away from noisy components and traces, such as the SW line (Pin 4), and its trace should be minimized.
4. Keep sensitive components away from the SW pin. The input capacitor $C_{IN}$, the compensation capacitor $C_C$ and $C_{ITH}$ and all the resistors R1, R2, $R_T$, and $R_C$ should be routed away from the SW trace and the inductor L1.
5. A ground plane is preferred, but if not available, keep the signal and power grounds segregated with small signal components returning to the SGND pin at one point which is then connected to the PGND pin.
6. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. These copper areas should be connected to one of the input supplies: $PV_{IN}$, PGND, $SV_{IN}$ or SGND.

## TYPICAL APPLICATIONS



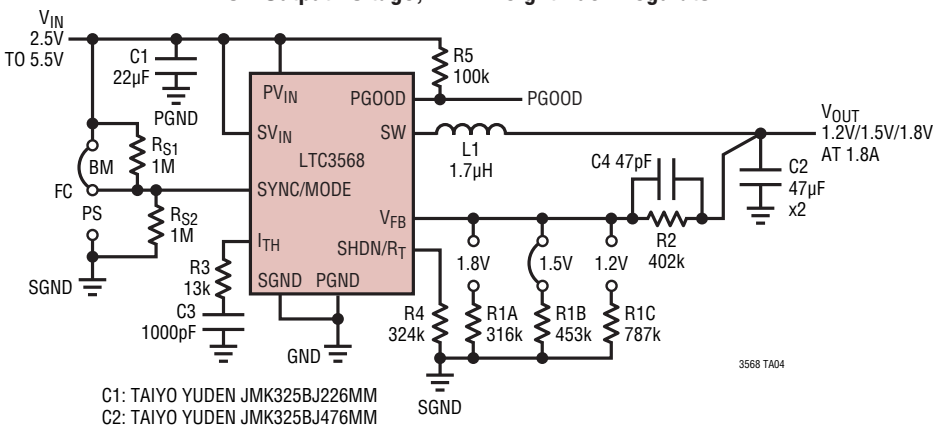

NOTE: IN DROPOUT, THE OUTPUT TRACKS THE INPUT VOLTAGE
C1, C2: TAIYO YUDEN JMK325BJ226MM
L1: TOKO A915AY-2ROM (D53LC SERIES)

**Figure 7. General Purpose Buck Regulator Using Ceramic Capacitors**



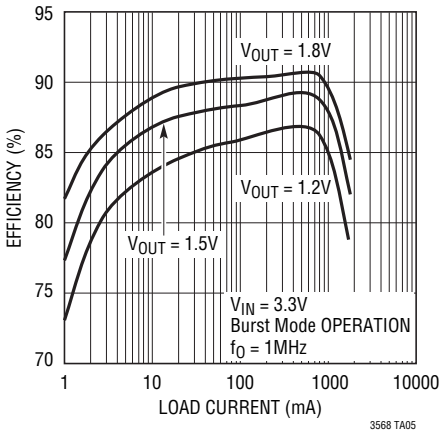
# TYPICAL APPLICATIONS

### Low Output Voltage, 2mm Height Buck Regulator



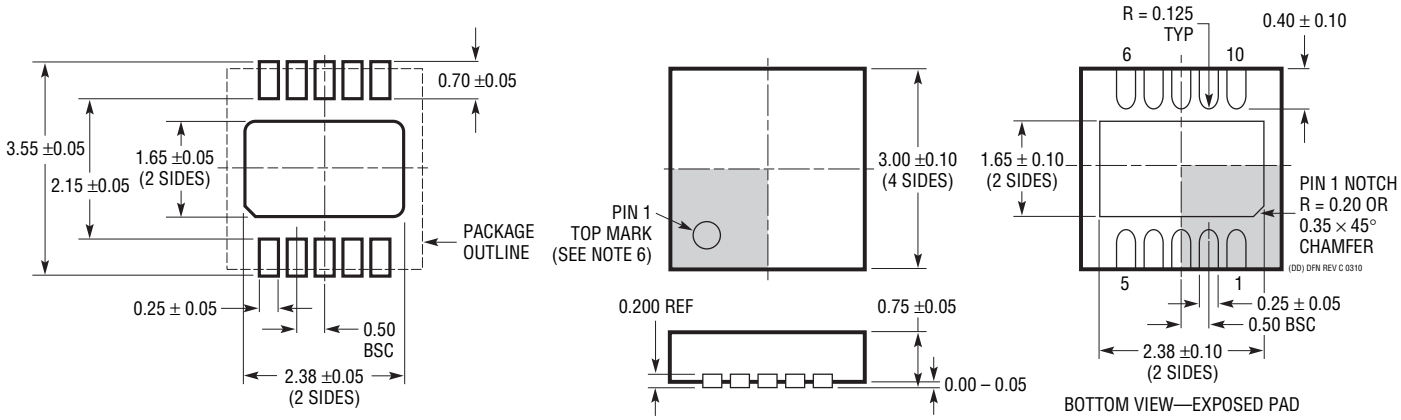

C1: TAIYO YUDEN JMK325BJ226MM
C2: TAIYO YUDEN JMK325BJ476MM
L1: SUMIDA CDRH2D18/HP1R7

### Efficiency vs Load Current




# PACKAGE DESCRIPTION

**DD Package**
**10-Lead Plastic DFN (3mm × 3mm)**
(Reference LTC DWG # 05-08-1699 Rev C)




**RECOMMENDED** SOLDER PAD PITCH AND DIMENSIONS

BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

## REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 9/10 | I-Grade added. Reflected throughout the data sheet | 1 to 18 |