Monolithic 400mA Buck Regulator with Dual 150mA LDOs in 3mm × 2mm DFN

FEATURES

- **Triple Output Supply from a Single 2.5V to 5.5V Input**
- **400mA Buck DC/DC Plus Dual 150mA LDOs in One IC**
- **Outputs Regulate Down to 0.8V**
- **±2.5% Reference Accuracy**
- **Constant-Frequency 2.25MHz Operation**
- **Burst Mode® Operation for High Efficiency at Light Loads; I_Q = 70µA, All Outputs Enabled**
- **Independent Enable Pin for Each Output**
- Current Mode Operation for Excellent Line and Load Transient Response
- Internal Soft-Start for Each Output
- Tiny 12-Lead 3mm × 2mm × 0.75mm DFN Package

APPLICATIONS

- Handheld Products
- Portable Instruments
- Single-Cell Li-Ion/Li-Polymer Powered Devices
- DMB/DVB-H Multimedia Cell Phones
- Multivoltage Power for Digital Logic, I/O, FPGAs, CPLDs, ASICs, SoCs, CPUs and RF Chipsets

DESCRIPTION

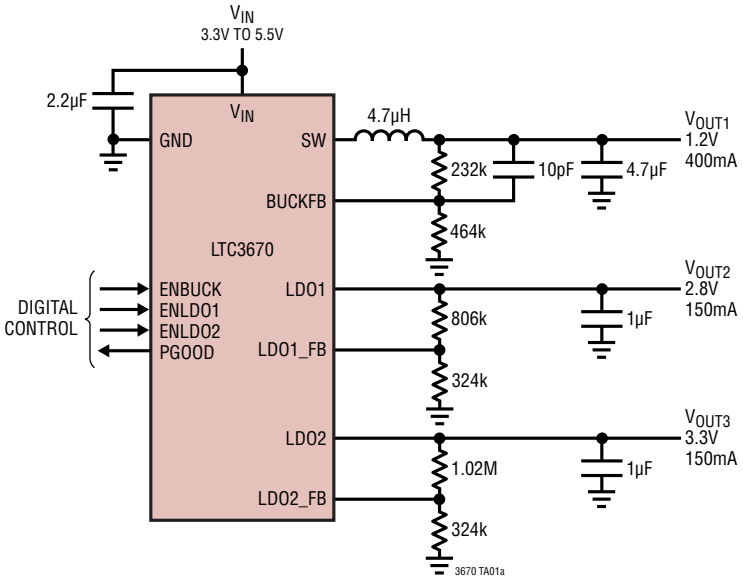
The LTC®3670 is a triple power supply composed of a 400mA synchronous buck regulator and two 150mA low dropout linear regulators (LDOs). The input supply range of 2.5V to 5.5V is especially well-suited for single-cell Lithium-Ion and Lithium-Ion/Polymer applications, and for powering low voltage ASICs and SoCs from 3V, 3.3V or 5V rails. Regulated output voltages are programmed via external resistors. Each output has its own enable pin for maximum flexibility.

The 400mA buck regulator features constant-frequency 2.25MHz operation, allowing small surface mount inductors and capacitors to be used. Burst Mode operation maintains high efficiency in light-load and no-load conditions. Internal control-loop compensation simplifies application design.

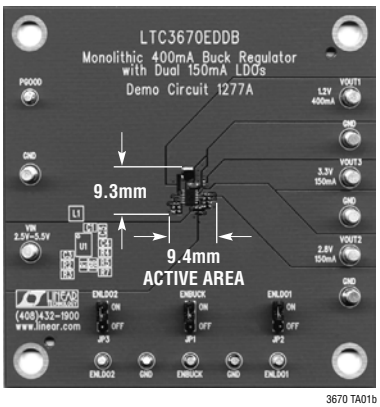
The LTC3670 is available in a 0.75mm profile, 3mm × 2mm 12-lead DFN package.

TYPICAL APPLICATION

Triple Power Supply with Independent Enables



Demoboard



3670 TA01b

Rev A

ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2, 3)

V_{IN}, ENBUCK, ENLDO1, ENLDO2, PGOOD ..... –0.3V to 6V

SW, BUCKFB, LDO1_FB, LDO2_FB, LDO1, LDO2.....–0.3V to (V_{IN} + 0.3V)

I_{SW} 600mA

I_{LDO1}, I_{LDO2} 250mA

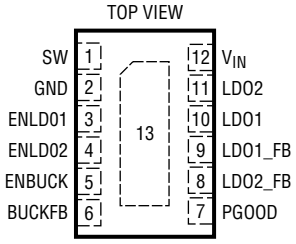
I_{PGOOD}.....40mA

Junction Temperature .....125°C

Operating Temperature Range.....–40°C to 85°C

Storage Temperature Range.....–65°C to 125°C

PIN CONFIGURATION



DDB PACKAGE
12-LEAD (3mm × 2mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 76°C/W, θ_{JC} = 13.5°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3670EDDB#PBF	LTC3670EDDB#TRPBF	LDBY	12-Lead (3mm × 2mm) Plastic DFN	–40°C to 85°C

Consult ADI Marketing for parts specified with wider operating temperature ranges.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range		●	2.5		5.5	V
V_{UVLO}	Undervoltage Lockout Threshold	V_{IN} Rising			2.2	2.45	V
	Undervoltage Lockout Hysteresis				18	100	mV
I_Q	V_{IN} Quiescent Current, No Load All Outputs Enabled Buck Enabled Only Buck Enabled Only, in Dropout One LDO Enabled Only Shutdown	(Note 4) V_{BUCKFB} = 0.9V V_{BUCKFB} = 0.9V V_{BUCKFB} = 0V V_{ENBUCK} = V_{ENLDO1} = V_{ENLDO2} = 0V			 70 38 700 22	 110 60 1100 35 1	 µA µA µA µA µA
V_{IL} V_{IH}	ENBUCK, ENLDO1, ENLDO2 Pin Thresholds Logic Low Voltage Logic High Voltage		 ● ●	 1.2		 0.4	 V V
	ENBUCK, ENLDO1, ENLDO2 Pin Pull-Down Resistance				4		MΩ
R_{PGOOD}	PGOOD Pin Logic Low Output Resistance				30		Ω
	PGOOD Pin Hi-Z Leakage	V_{PGOOD} = 6V				1	µA
	PGOOD Threshold on Feedback Voltages of Enabled Regulators	(Note 5)			92		%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Synchronous Buck Regulator							
f_{OSC}	Oscillator Frequency			1.91	2.25	2.59	MHz
V_{BUCKFB}	Buck Regulated Feedback Voltage		●	0.78	0.8	0.82	V
I_{BUCKFB}	Feedback Pin Input Bias Current		●			±20	nA
I_{MAXP}	PMOS Switch Maximum Peak Current (Note 6)			600	800	1100	mA
$R_{P(BUCK)}$	PMOS Switch On-Resistance				0.6		Ω
$R_{N(BUCK)}$	NMOS Switch On-Resistance				0.7		Ω
$R_{PD(BUCK)}$	SW Pin Pull-Down Resistance in Shutdown				10		kΩ
$t_{SS(BUCK)}$	Soft-Start Time				0.6		ms
Each LDO Regulator							
V_{LDO}	LDO Regulated Feedback Voltage	LDO Output, I_{LDO} = 1mA to 150mA	●	0.78	0.8	0.82	V
	LDO Line Regulation (Note 7)	I_{LDO} = 1mA, V_{IN} = 2.5V to 5.5V			0.25		mV/V
	LDO Load Regulation (Note 7)	I_{LDO} = 1mA to 150mA			–5		µV/mA
I_{LDO_FB}	Feedback Pin Input Bias Current		●			±20	nA
	Short-Circuit Output Current (Note 6)				420		mA
V_{DROP}	Dropout Voltage (Note 8)	I_{LDO} = 150mA V_{IN} = 3.6V V_{IN} = 2.5V			 150 200	 200 300	 mV mV
$t_{SS(LDO)}$	Soft-Start Time				0.1		ms
$R_{PD(LDO)}$	Output Pull-Down Resistance in Shutdown				10		kΩ

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperatures will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may result in device degradation or failure.

Note 3: The LTC3670 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 4: Dynamic supply current is higher due to the gate charge delivered to the buck regulator's internal MOSFET switches at the switching frequency.

Note 5: PGOOD threshold is expressed as a percentage of the feedback regulation voltage. The threshold is measured for the feedback pin voltage rising.

Note 6: The current limit features are intended to protect the IC from short term or intermittent fault conditions. Prolonged operation above the specified Absolute Maximum pin current rating may result in device degradation or failure.

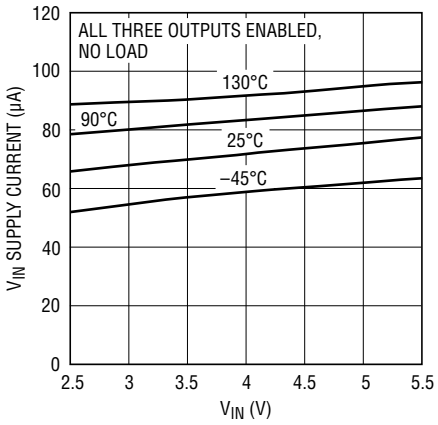
Note 7: Measured with the LDO running unity gain, with output tied to feedback pin.

Note 8: Dropout voltage is the minimum input to output voltage differential needed for an LDO to maintain regulation at a specified output current. When an LDO is in dropout, its output voltage will be equal to:

$V_{IN} – V_{DROP}$

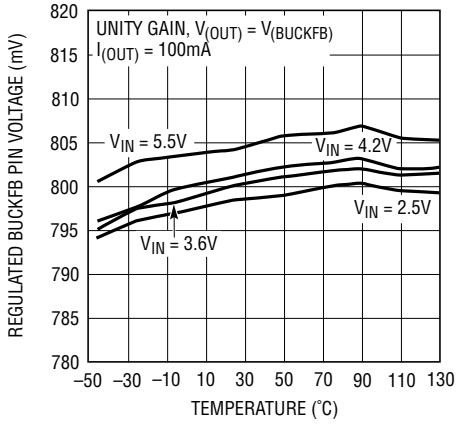
TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise noted)

V_{IN} Supply Current vs V_{IN}



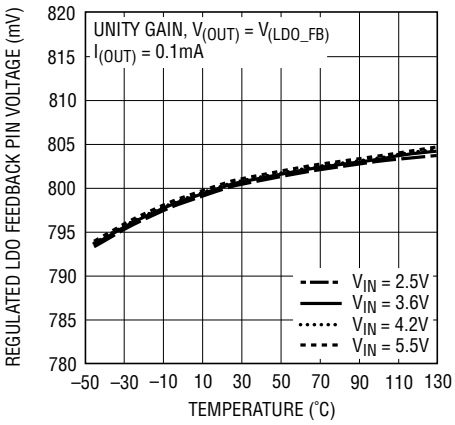
3670 G01

Buck Regulated Feedback Voltage vs Temperature



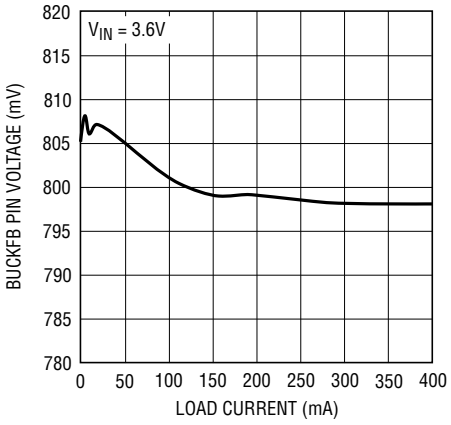
3670 G02

Regulated LDO Feedback Pin Voltage vs Temperature



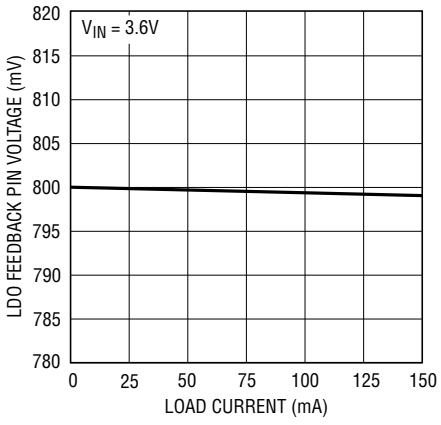
3670 G03

Buck Load Regulation



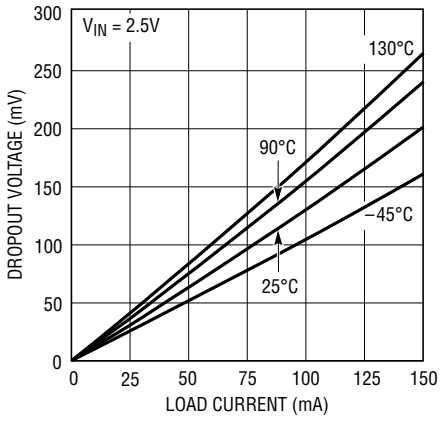
3670 G04

LDO Load Regulation



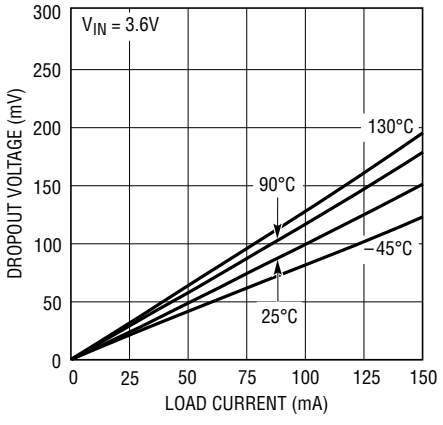
3670 G05

LDO Dropout vs Load Current at V_{IN} = 2.5V



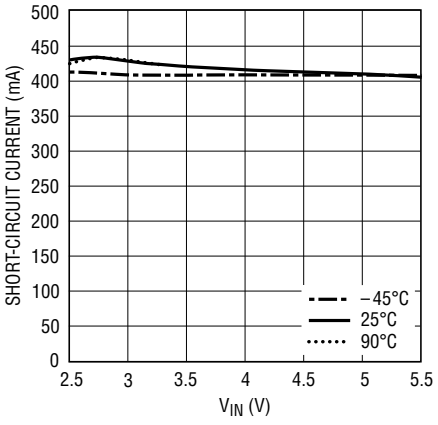
3670 G06

LDO Dropout vs Load Current at V_{IN} = 3.6V



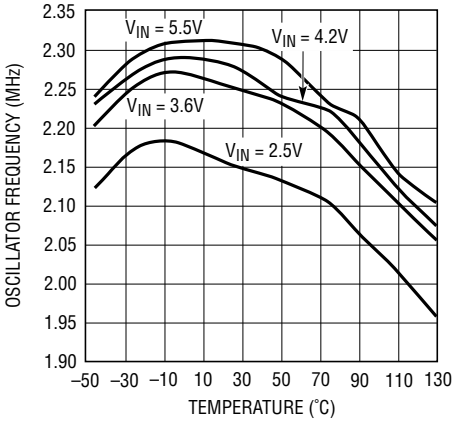
3670 G07

LDO Short-Circuit Current vs V_{IN}



3670 G08

Buck Oscillator Frequency vs Temperature

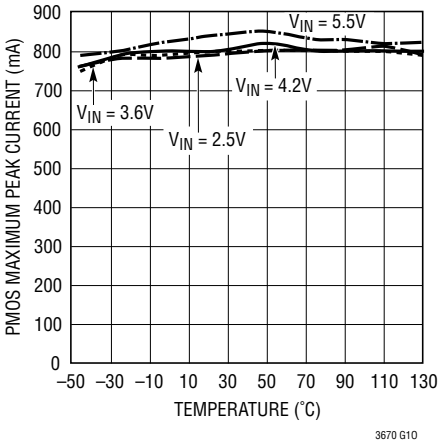


3670 G09

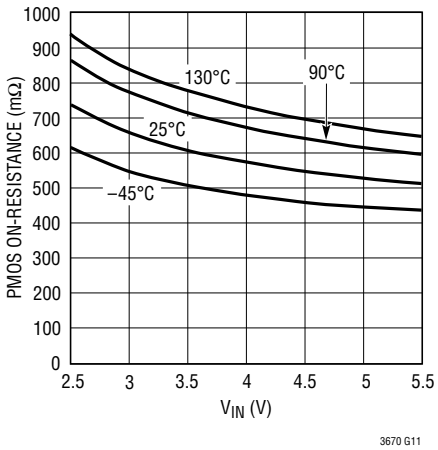
Rev A

TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C unless otherwise noted)

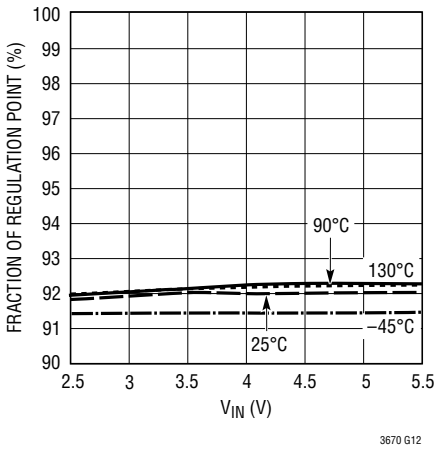
PMOS Switch Maximum Peak Current vs Temperature



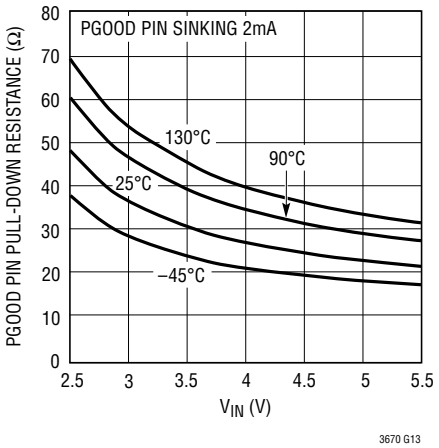
Buck PMOS On-Resistance



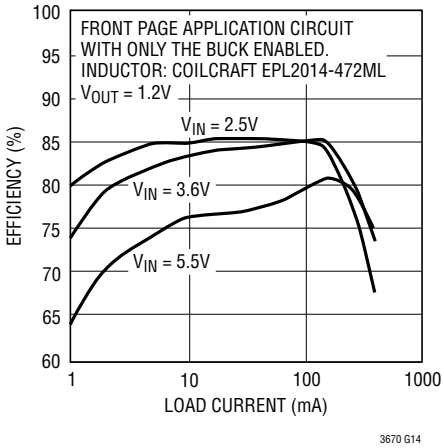
PGOOD Threshold at Any Feedback Pin



PGOOD Pin Pull-Down Resistance



Front Page Application Efficiency



PIN FUNCTIONS

SW (Pin 1): Buck Regulator Switch Node Connection to Inductor. This pin connects to the drains of the buck regulator's main PMOS and synchronous NMOS switches.

GND (Pin 2): Ground.

ENLDO1 (Pin 3): Enables the First Low Dropout Linear Regulator (LDO1) When High. This is a MOS gate input. There is an internal 4MΩ pull-down.

ENLDO2 (Pin 4): Enables the Second Low Dropout Linear Regulator (LDO2) When High. This is a MOS gate input. There is an internal 4MΩ pull-down.

ENBUCK (Pin 5): Enables the Buck Converter When High. This is a MOS gate input. There is an internal 4MΩ pull-down.

BUCKFB (Pin 6): Feedback Voltage Input for the Buck Regulator. Typically, an external resistor divider feeds a fraction of the buck output voltage to this pin.

PGOOD (Pin 7): Power Good Open-Drain NMOS Output. The PGOOD pin goes Hi-Z when all enabled outputs are within 8% of final value.

LDO2_FB (Pin 8): Feedback Voltage Input for the Second Low Dropout Linear Regulator (LDO2). Typically, an external resistor divider feeds a fraction of the LDO2 output voltage to this pin.

LDO1_FB (Pin 9): Feedback Voltage Input for the First Low Dropout Linear Regulator (LDO1). Typically, an external resistor divider feeds a fraction of the LDO1 output voltage to this pin.

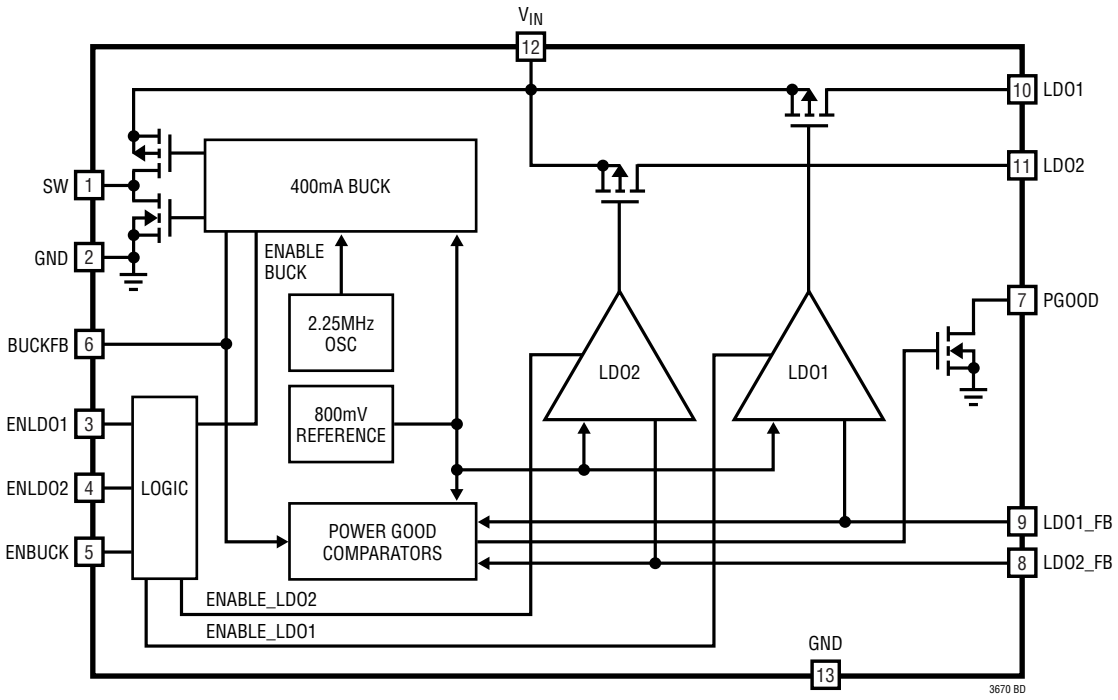
LDO1 (Pin 10): Output of the First Low Dropout Linear Regulator. This pin must be bypassed to ground with a 1µF or greater ceramic capacitor.

LDO2 (Pin 11): Output of the Second Low Dropout Linear Regulator. This pin must be bypassed to ground with a 1µF or greater ceramic capacitor.

V_{IN} (Pin 12): Input Supply. This pin should be bypassed to ground with a 2.2µF or greater ceramic capacitor.

Exposed Pad (Pin 13): Ground. This pin must be soldered to the PCB.

BLOCK DIAGRAM



OPERATION

INTRODUCTION

The LTC3670 combines a synchronous buck converter with two low dropout linear regulators (LDOs) to provide three low voltage outputs from a higher voltage input source. The input supply range of 2.5V to 5.5V spans the single-cell Li-Ion operating range. Each output can be independently enabled or shut down via the three enable pins. The output regulation voltages are programmed by external resistor dividers.

SYNCHRONOUS BUCK REGULATOR

The synchronous buck includes many features: It uses a Constant-frequency current mode architecture, switching at 2.25MHz down to light loads. Automatic Burst Mode operation maintains efficiency in light load and no-load situations. Should the input voltage ever fall below the target output voltage, the buck enters 100% duty cycle operation. Also known as operating in *dropout*, this can extend operating life in battery-powered systems. Soft-start circuitry limits inrush current when powering on. Output current is limited in the event of an output short circuit. The switch node is slew-rate limited to reduce EMI radiation. The buck regulation control-loop compensation is internal to the IC and requires no external components.

Main Control Loop

An error amplifier monitors the difference between an internal reference voltage and the voltage on the BUCKFB pin. When the BUCKFB voltage is below the reference, the error amplifier output voltage increases. When the BUCKFB voltage exceeds the reference, the error amplifier output voltage decreases.

The error amplifier output controls the peak inductor current through the following mechanism: Paced by a free-running 2.25MHz oscillator, the main P-channel MOSFET switch is turned on at the start of the oscillator cycle. Current flows from the V_{IN} supply through this PMOS switch, through the inductor via the SW pin, and into the output capacitor and load. When the current reaches the level programmed by the output of the error amplifier, the PMOS is shut off, and the N-channel MOSFET synchronous rectifier turns on. Energy stored in the inductor discharges into the load through this NMOS. The NMOS turns off at the end of the 2.25MHz cycle, or sooner, if the current through it drops to zero before the end of the cycle.

Through these mechanisms, the error amplifier adjusts the peak inductor current to deliver the required output power to regulate the output voltage as sensed by the BUCKFB pin. All necessary control-loop compensation is internal to the step-down switching regulator requiring only a single ceramic output capacitor for stability.

At light loads, the inductor current may reach zero before the end of the oscillator cycle, which will turn off the NMOS synchronous rectifier. In this case, the SW pin goes high impedance and will show damped "ringing." This is known as discontinuous operation and is normal behavior for a switching regulator.

Burst Mode Operation

At light load and no-load conditions, the buck automatically switches to a power-saving hysteretic control algorithm that operates the switches intermittently to minimize switching losses. Known as Burst Mode operation, the buck cycles the power switches enough times to charge the output capacitor to a voltage slightly higher than the regulation point. The buck then goes into a reduced quiescent current sleep mode. In this state, power loss is minimized while the load current is supplied by the output capacitor. Whenever the output voltage drops below a pre-determined value, the buck wakes from sleep and cycles the switches again until the output capacitor voltage is once again slightly above the regulation point. Sleep time thus depends on load current, because the load current determines the discharge rate of the output capacitor. Should load current increase above roughly 1/4 of the rated output load current, the buck resumes constant-frequency operation.

Soft-Start

Soft-start in the buck regulator is accomplished by gradually increasing the maximum allowed peak inductor current over a 600µs period. This allows the output to rise slowly, controlling the inrush current required to charge up the output capacitor. A soft-start cycle occurs whenever the LTC3670 is enabled, or after a fault condition has occurred (thermal shutdown or UVLO).

OPERATION

Switch Slew-Rate Control

The buck regulator contains new patent-pending circuitry to limit the slew rate of the switch node (SW pin). This new circuitry is designed to transition the switch node over a period of a couple nanoseconds, significantly reducing radiated EMI and conducted supply noise while maintaining high efficiency.

LOW DROPOUT LINEAR REGULATORS (LDOs)

The LTC3670 contains two independent LDO regulators, each supporting a load of up to 150mA. Each LDO takes power from the V_{IN} pin and drives its output pin with the goal of bringing its feedback pin voltage to 0.8V. In the usual case, a resistor divider is connected between the LDO's output pin, feedback pin and ground, in order to close the control loop and program the output voltage. For stability, each LDO output must be bypassed to ground with a minimum 1µF ceramic capacitor.

Each LDO can be enabled or disabled via its own enable pin. When disabled with V_{IN} still applied, an internal pull-down resistor is switched in to help bring the output to ground. When an LDO is enabled, a soft-start circuit ramps its regulation point from zero to final value over a period of roughly 0.1ms, reducing the required V_{IN} inrush current.

LOW V_{IN} SUPPLY UNDERVOLTAGE LOCKOUT

An undervoltage lockout (UVLO) circuit shuts down the LTC3670 when V_{IN} drops below about 2.2V.

POWER GOOD DETECTION

The LTC3670 has a built-in supply monitor. If the feedback voltage of every enabled regulator is above 92% of its regulation value, the PGOOD pin becomes high impedance. Otherwise, or if no regulators are enabled, the PGOOD pin is driven to ground by an internal open-drain NMOS.

The PGOOD pin may be connected through a pull-up resistor to a supply voltage of up to 5.5V, independent of the V_{IN} pin voltage.

APPLICATIONS INFORMATION

Buck Regulator Inductor Selection

Many different sizes and shapes of inductors are available from numerous manufacturers. Choosing the right inductor from such a large selection of devices can be overwhelming, but following a few basic guidelines will make the selection process much simpler.

The buck regulator is designed to work with inductors in the range of 2.2µH to 10µH. A 4.7µH inductor is a good starting point. Larger value inductors reduce ripple current which improves output ripple voltage. Lower value inductors result in higher ripple current and improved transient response time. To maximize efficiency, choose an inductor with a low DC resistance. Choose an inductor with a DC current rating at least 1.5 times larger than the maximum load current to ensure that the inductor does not saturate during normal operation. If output short-circuit is a possible condition, the inductor should be rated to handle the maximum peak current specified for the buck regulator.

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or Permalloy materials are small and do not radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. Inductors that are very thin or have a very small volume typically have much higher core and DCR losses, and will not give the best efficiency. The choice of which style inductor to use often depends more on the price vs size, performance, and any radiated EMI requirements than on what the buck regulator needs to operate.

Table 1 shows several inductors that work well with the buck regulator. These inductors offer a good compromise in current rating, DCR and physical size. Consult each manufacturer for detailed information on their entire selection of inductors.

Table 1. Recommended Inductors for the Buck Regulator

INDUCTOR TYPE	L (µH)	MAXIMUM I_{DC} (A)	MAXIMUM DCR (Ω)	SIZE in mm (L × W × H)	MANUFACTURER
EPL2014-472ML	4.7	1.3	0.254	1.8 × 2.0 × 1.4	Coilcraft www.coilcraft.com
LPS3015	4.7 3.3	1.1 1.3	0.2 0.13	3.0 × 3.0 × 1.5 3.0 × 3.0 × 1.5	
DE2818C	4.7 3.3	1.25 1.45	0.072 0.053	3.0 × 2.8 × 1.8 3.0 × 2.8 × 1.8	Toko www.toko.com
DE2812C	4.7 3.3	1.15 1.37	0.13* 0.105*	3.0 × 2.8 × 1.2 3.0 × 2.8 × 1.2	
CDRH3D16	4.7	0.9	0.11	4.0 × 4.0 × 1.8	Sumida www.sumida.com
CDRH2D11	4.7 3.3	0.5 0.6	0.17 0.123	3.2 × 3.2 × 1.2 3.2 × 3.2 × 1.2	
SD3118	4.7 3.3	1.3 1.59	0.162 0.113	3.1 × 3.1 × 1.8 3.1 × 3.1 × 1.8	Cooper www.cooperet.com

*Typical DCR

APPLICATIONS INFORMATION

Input/Output Capacitor Selection

Low ESR (equivalent series resistance) ceramic capacitors should be used to bypass the following pins to ground: V_{IN}, the buck output, LDO1 and LDO2. Only X5R or X7R ceramic capacitors should be used because they retain their capacitance over wider voltage and temperature ranges than other ceramic types. A 10µF output capacitor is sufficient for the buck regulator output. For good transient response and stability the output capacitor for the buck regulator should retain at least 4µF of capacitance over operating temperature and bias voltage. The V_{IN} pin should be bypassed with a 2.2µF capacitor. The LDO1 and LDO2 output pins should each be bypassed with a 1µF capacitor or greater. Larger values yield improved transient response.

Consult with capacitor manufacturers for detailed information and specifications on their selection of ceramic capacitors. Many manufacturers now offer very thin (<1mm tall) ceramic capacitors ideal for use in height-restricted designs. Table 2 shows a list of several ceramic capacitor manufacturers.

Table 2. Ceramic Capacitor Manufacturers

AVX	www.avxcorp.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
Vishay Siliconix	www.vishay.com
TDK	www.tdk.com

Output Voltage Programming

Figure 1 shows how feedback resistor dividers are connected to the LTC3670 to set the output voltages of the buck and an LDO.

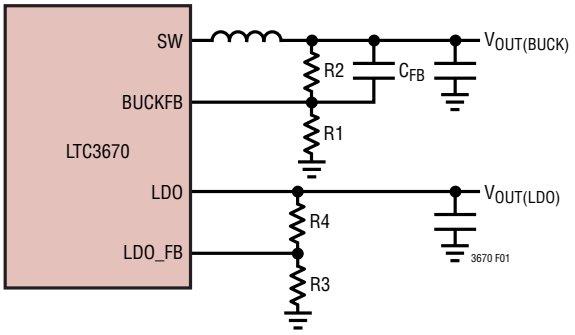


Figure 1. Setting the Output Voltages of the LTC3670

The output voltage of the buck regulator is determined by R1 and R2, following the equation:

$$V_{OUT(BUCK)} = 1+\frac{R2}{R1} \bullet 0.8V$$

An LDO's output voltage is similarly determined by R3 and R4, following:

$$V_{OUT(LDO)} = 1+\frac{R4}{R3} \bullet 0.8V$$

Typical values for R2 and R4 are in the range from 40k to 1M.

For improved buck regulator transient response, the capacitor C_{FB} cancels the pole created by the feedback resistors and the input capacitance of the BUCKFB pin. A variety of capacitor sizes can be used for C_{FB}, but a value of 10pF is recommended for most applications. Experimentation with capacitor sizes between 2pF and 22pF may yield improved transient response.

Printed Circuit Board Layout Considerations

When laying out the printed circuit board, the following list should be followed to ensure proper operation of the LTC3670:

1) The Exposed Pad of the package should connect directly to a large ground plane to minimize thermal and electrical impedance.

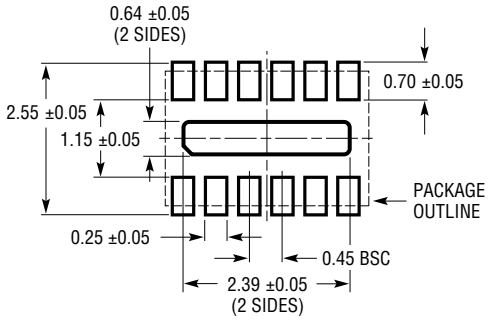
2) The connection from the input supply pin (V_{IN}) to its decoupling capacitor should be kept as short as possible. The GND side of this capacitor should connect directly to the ground plane of the part. The V_{IN} capacitor provides the AC current to the buck regulator's power MOSFETs and their drivers. It is especially important to minimize PCB trace inductance from this capacitor to the V_{IN} and GND pins of the LTC3670.

3) The switching power trace connecting the SW pin to the inductor should be kept as short as possible to reduce radiated EMI and parasitic coupling.

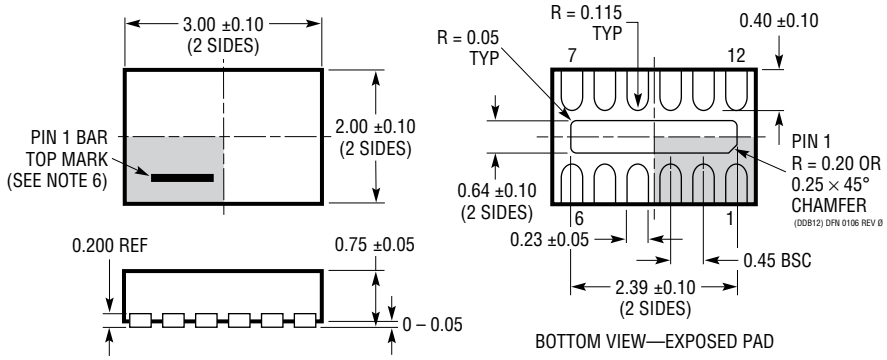
4) The LDO output capacitors should be placed as close to the IC as possible, and connected to the LDO outputs and the GND pin as directly as possible.

PACKAGE DESCRIPTION

DDB Package
12-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1723 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	06/18	Clarified V_{UVLO} in Electrical Characteristic table	2