Dual Adjustable Lowpass Filter

FEATURES

- **Guaranteed Phase and Gain Matching Specs**
- **Programmable BW Up to 2.5MHz**
- **Programmable Gain (0dB/6dB/12dB/24dB)**
- **9th Order Linear Phase Response**
- Differential, Rail-to-Rail Inputs and Outputs
- Low Noise: –145dBm/Hz (Input Referred)
- Low Distortion: –75dBc at 200kHz
- Simple Pin Programming or SPI Interface
- Set the Max Speed/Power with an External R
- Operates from 2.7V to 3.6V
- Input Range from 0V to 5.5V
- 4mm × 4mm QFN Package

APPLICATIONS

- Small/Low Cost Basestations:
  IDEN, PHS, TD-SCDMA, CDMA2000, WCDMA, UMTS
- Low Cost Repeaters, Radio Links, and Modems
- 802.11x Receivers
- JTRS

DESCRIPTION

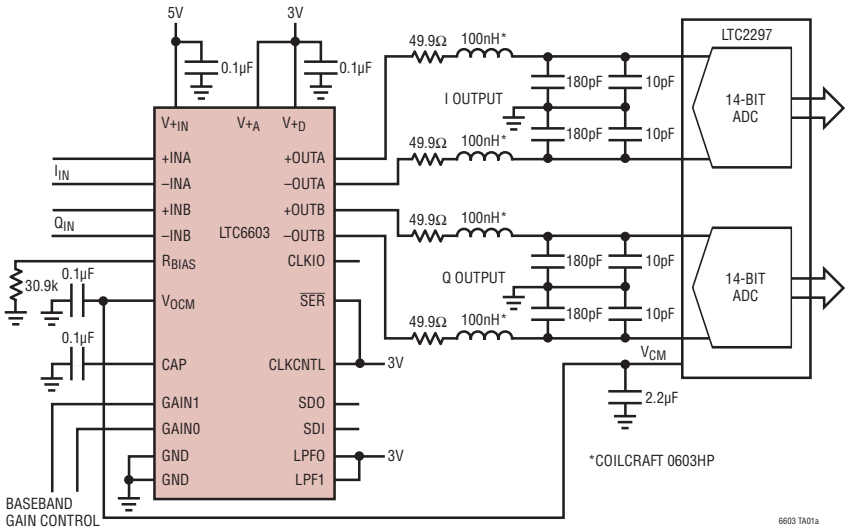
The LTC®6603 is a dual, matched, programmable lowpass filter for communications receivers and transmitters. The selectivity of the LTC6603, combined with its linear phase, phase matching and dynamic range, make it suitable for filtering in many communications systems. With 1.5° phase matching between channels, the LTC6603 can be used in applications requiring pairs of matched filters, such as transceiver I and Q channels. Furthermore, the differential inputs and outputs provide a simple interface for most communications systems.

The sampled data filter does not require an external clock yet its cutoff frequency can be set with a single external resistor with an accuracy of 3.5% or better. The external resistor programs an internal oscillator whose frequency is divided prior to being applied to the filter networks. This allows up to three cutoff frequencies that can be obtained for each external resistor value, allowing the cutoff frequency to be programmed over a range of more than six octaves. Alternatively, the cutoff frequency can be set with an external clock. The filter gain can also be programmed to 1, 2, 4 or 16.

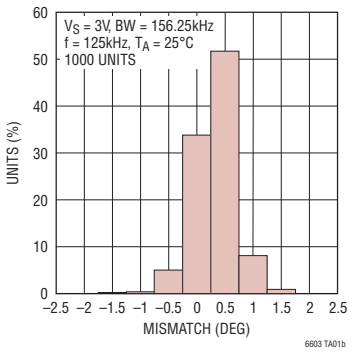
The LTC6603 features a low power shutdown mode that can be programmed through the serial interface and is available in a 24-pin 4mm × 4mm QFN package.

TYPICAL APPLICATION

2.5MHz I and Q Lowpass Filter and Dual ADC



Phase Matching

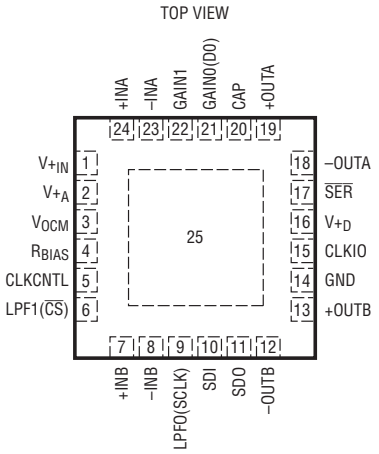


ABSOLUTE MAXIMUM RATINGS

(Note 1)

$V+_{IN}$ to GND 6V
$V+_A$, $V+_D$ to GND 4V
$V+_A$ to $V+_D$ ..... –0.3V to +0.3V
Filter Inputs to GND ..... –0.3V to $V+_{IN}$ + 0.3V
Pins 3, 4 to GND ..... –0.3V to $V+_A$ + 0.3V
Pins 5, 6, 9-11,
15, 17, 21, 22 to GND ..... –0.3V to $V+_D$ + 0.3V
Output Short-Circuit Duration ..... Indefinite
Operating Temperature Range (Note 2)
LTC6603CUF ..... –40°C TO 85°C
LTC6603IUF ..... –40°C TO 85°C
Specified Temperature Range (Note 3)
LTC6603CUF ..... 0°C TO 70°C
LTC6603IUF ..... –40°C TO 85°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 150°C, θ_{JA} = 37°C/W, θ_{JC} = 4.3°C/W
EXPOSED PAD (PIN 25) IS GND. MUST BE SOLDERED TO THE PCB.

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6603CUF#PBF	LTC6603CUF#TRPBF	6603	24-Lead (4mm × 4mm) Plastic QFN	0°C to 70°C
LTC6603IUF#PBF	LTC6603IUF#TRPBF	6603	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. $V+_A$ = $V+_D$ = $V+_{IN}$ = 3V, V_{ICM} = V_{OCM} = 1.5V, Gain = 0dB, lowpass cutoff = 2.5MHz, internal clocking with R_{BIAS} = 30.9k unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Filter Gain Either Channel	External Clock = 80MHz, Filter Cutoff (f_C)= 156.25kHz, V_{IN} = 3.6V_{P-P}, Pin 3 Open DC Gain, Gain Set = 0dB					
	f_{IN} = 62.5kHz (0.4 • f_C), Relative to DC Gain	●	0.25	0.4	0.55	dB
	f_{IN} = 125kHz (0.8 • f_C), Relative to DC Gain	●	–0.5	–0.3	–0.1	dB
	f_{IN} = 156.25kHz (f_C), Relative to DC Gain	●	0.4	0.6	0.8	dB
	f_{IN} = 234.375kHz (1.5 • f_C), Relative to DC Gain	●	–0.6	–0.4	–0.2	dB
		●		–32	–29.5	dB
Matching of Filter Gain	External Clock = 80MHz, Filter Cutoff (f_C)= 156.25kHz, V_{IN} = 3.6V_{P-P}, Pin 3 Open DC Gain, Gain Set = 0dB	●		±0.03	±0.1	dB
	f_{IN} = 62.5kHz (0.4 • f_C)	●		±0.03	±0.1	dB
	f_{IN} = 125kHz (0.8 • f_C)	●		±0.03	±0.1	dB
	f_{IN} = 156.25kHz (f_C)	●		±0.03	±0.15	dB

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Filter Phase Either Channel	External Clock = 80MHz, Filter Cutoff (f_C) = 156.25kHz, V_{IN} = 3.6V_{P-P}, Pin 3 Open					
	f_{IN} = 62.5kHz (0.4 • f_C)	●	158	161	163	deg
	f_{IN} = 125kHz (0.8 • f_C)	●	–44	–39	–36	deg
	f_{IN} = 156.25kHz (f_C)	●	–152	–146	–142	deg
Matching of Filter Phase	External Clock = 80MHz, Filter Cutoff (f_C) = 156.25kHz, V_{IN} = 3.6V_{P-P}, Pin 3 Open					
	f_{IN} = 62.5kHz (0.4 • f_C)	●		±0.2	±1.5	deg
	f_{IN} = 125kHz (0.8 • f_C)	●		±0.4	±3	deg
	f_{IN} = 156.25kHz (f_C)	●		±0.5	±4	deg
Filter Gain Either Channel	External Clock = 80MHz, Filter Cutoff (f_C) = 2.5MHz, V_{IN} = 3.6V_{P-P}, Pin 3 Open					
	DC Gain, Gain Set = 0dB	●	0	0.5	1.2	dB
	f_{IN} = 1MHz (0.4 • f_C), Relative to DC Gain	●	–2	–0.8	–0.1	dB
	f_{IN} = 2MHz (0.8 • f_C), Relative to DC Gain	●	–0.7	0.4	1.5	dB
	f_{IN} = 2.5MHz (f_C), Relative to DC Gain	●	–1.1	0.1	1	dB
	f_{IN} = 4MHz (1.5 • f_C), Relative to DC Gain	●		–43	–32.6	dB
Matching of Filter Gain	External Clock = 80MHz, Filter Cutoff (f_C) = 2.5MHz, V_{IN} = 3.6V_{P-P}, Pin 3 Open					
	f_{IN} = 2MHz (0.8 • f_C)	●		±0.05	±0.2	dB
	f_{IN} = 2.5MHz (f_C)	●		±0.2	±0.4	dB
Filter Phase Either Channel	External Clock = 80MHz, Filter Cutoff (f_C) = 2.5MHz, V_{IN} = 3.6V_{P-P}, Pin 3 Open					
	f_{IN} = 1MHz (0.4 • f_C)	●	150	155	159	deg
	f_{IN} = 2MHz (0.8 • f_C)	●	–45	–39	–28	deg
	f_{IN} = 2.5MHz (f_C)	●	–152	–141	–126	deg
Matching of Filter Phase	External Clock = 80MHz, Filter Cutoff (f_C) = 2.5MHz, V_{IN} = 3.6V_{P-P}, Pin 3 Open					
	f_{IN} = 1MHz (0.4 • f_C)	●			±2.5	deg
	f_{IN} = 2MHz (0.8 • f_C)	●			±4	deg
	f_{IN} = 2.5MHz (f_C)	●			±4	deg
Filter Cutoff Accuracy when Self Clocked	CLKCNTL = 3V (Note 4)					
	R_{BIAS} = 200k	●			±3	%
	R_{BIAS} = 54.9k	●			±3	%
	R_{BIAS} = 30.9k	●			±3.5	%
DC Gain	Filter Cutoff (f_C) = 2.5MHz, 0.6V to 2.4V Each Output, Pin 3 Open					
	Gain Setting = 0dB	●	0	0.5	1.2	dB
	Gain Setting = 6dB	●	5.6	6	6.6	dB
	Gain Setting = 12dB	●	11.2	11.8	12.5	dB
	Gain Setting = 24dB	●	22.5	23.2	24	dB
DC Gain Matching	Filter Cutoff (f_C) = 2.5MHz, 0.6V to 2.4V Each Output, Pin 3 Open					
	Gain Setting = 0dB	●		±0.1	±0.2	dB
	Gain Setting = 6dB	●		±0.05	±0.1	dB
	Gain Setting = 12dB	●		±0.05	±0.15	dB
	Gain Setting = 24dB	●		±0.1	±0.2	dB
Noise At 200kHz	Voltage Noise Referred to the Input					
	Gain = 0dB			–124		dBm/Hz
	Gain = 6dB			–129		dBm/Hz
	Gain = 12dB			–135		dBm/Hz
	Gain = 24dB			–145		dBm/Hz
Integrated Noise	Noise Bandwidth = 5MHz, Referred to the Input					
	Gain = 0dB			–53		dBm
	Gain = 6dB			–59		dBm
	Gain = 12dB			–65		dBm
	Gain = 24dB			–76		dBm
THD	V_{IN} = 2V_{P-P}, f_{IN} = 200kHz, Gain Setting = 24dB			–75		dB
Input Impedance	Gain = 24dB, R_{BIAS} = 30.9k, Filter Cutoff (f_C) = 2.5MHz					
	Differential			1.6		kΩ
	Common Mode			5		kΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. $V+_A$ = $V+_D$ = $V+_{IN}$ = 3V, V_{ICM} = V_{OCM} = 1.5V, Gain = 0dB, lowpass cutoff = 2.5MHz, internal clocking with R_{BIAS} = 30.9k unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS} Differential	Input Referred Differential Offset Voltage at Either Output					
	Lowest Cutoff Frequency, Gain Setting = 24dB	●			±8	mV
	Highest Cutoff Frequency, Gain Setting = 24dB	●			±14	mV
	Lowest Cutoff Frequency, Gain Setting = 0dB	●			±40	mV
	Highest Cutoff Frequency, Gain Setting = 0dB	●			±60	mV
CMRR Differential	f_C = 625kHz					
	Common Mode Input from 0V to 3V, $V+_{IN}$ = 3V	●	60	90		dB
	Common Mode Input from 0V to 5V, $V+_{IN}$ = 5V	●	60	90		dB
V_{OCM} Pin Voltage	$V+_A$ = $V+_D$ = 3V, Pin 3 Open, f_C = 156.25kHz	●	1.3	1.45	1.5	V
V_{OCM} Pin Input Impedance	$V+_A$ = $V+_D$ = 3V, Pin 3 Open, f_C = 156.25kHz	●	2.5	3.4	4.5	kΩ
V_{OSCM}	Common Mode Offset Voltage, V_{OCM} = 1.5V, Supplies = 3V V_{OSCM} = V_{OUT-CM} – V_{OCM}	●		100	185	mV
Output Swing	f_C = 156.25kHz					
	Source 1mA, Relative to $V+_A$	●		200	500	mV
	Sink 1mA, Relative to GND	●		150	400	mV
Short-Circuit Current	f_C = 156.25kHz					
	Sourcing	●	7	25		mA
	Sinking	●	11	30		mA
Supply Current	Internal Clock (R_{BIAS} = 30.9k); Sum of the Currents into $V+_D$, $V+_A$, and $V+_{IN}$ All Supplies Set to 3V					
	f_C = 156.25kHz	●		88	96	mA
	f_C = 625kHz	●		121	130	mA
	f_C = 2.5MHz	●		162	175	mA
Supply Current, Shutdown Mode	Sum of the Currents into $V+_D$, $V+_A$, and $V+_{IN}$; All Supplies Set to 3V Shutdown Via Serial Interface	●		170	235	µA
Supply Voltage	$V+_D$, $V+_A$ Relative to GND	●	2.7		3.6	V
	$V+_{IN}$ Relative to GND	●	2.7		5.5	V
PSRR	$V+_D$ = $V+_A$ = $V+_{IN}$, All from 2.7V to 3.6V	●	40	50		dB
	$V+_D$ = $V+_A$ = 3V, $V+_{IN}$ from 4.5V to 5.5V	●	65	85		dB
R_{BIAS} Resistor Range	CLKCNTL = 3V					
	Clock Frequency Error < ±3.5%	●	30.9		54.9	kΩ
	Clock Frequency Error < ±3%	●	54.9		200	kΩ
R_{BIAS} Pin Voltage	30.9k < R_{BIAS} < 200k			1.17		V
Clock Frequency Drift Over Temperature	R_{BIAS} = 30.9k CLKCNTL Pin Open			40		ppm/°C
Clock Frequency Drift Over Supply	$V+_A$, $V+_D$ from 2.7V to 3.6V, R_{BIAS} = 30.9k CLKCNTL Pin Open	●		0.2	0.5	%/V
Output Clock Duty Cycle	R_{BIAS} = 30.9k	●	45	50	55	%
CLKIO Pin High Level Input Voltage	CLKCNTL = 0V (Note 5)	●	$V+_D$ – 0.3			V
CLKIO Pin Low Level Input Voltage	CLKCNTL = 0V (Note 5)	●			0.3	V
CLKIO Pin Input Current	CLKCNTL = 0V					
	CLKIO = 0V (Note 6)	●	–1			µA
	CLKIO = $V+_D$	●			10	µA
CLKIO Pin High Level Output Voltage	$V+_A$ = $V+_D$ = 3V, CLKCNTL = 3V					
	I_{OH} = –1mA			2.95		V
	I_{OH} = –4mA			2.9		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. $V+_A$ = $V+_D$ = $V+_{IN}$ = 3V, V_{ICM} = V_{OCM} = 1.5V, Gain = 0dB, lowpass cutoff = 2.5MHz, internal clocking with R_{BIAS} = 30.9k unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CLKIO Pin Low Level Output Voltage	$V+_A$ = $V+_D$ = 3V, CLKCNTL = 3V I_{OL} = 1mA I_{OL} = 4mA			 0.05 0.1		 V V
CLKIO Pin Rise Time	$V+_A$ = $V+_D$ = CLKCNTL = 3V, C_{LOAD} = 5pF			0.3		ns
CLKIO Pin Fall Time	$V+_A$ = $V+_D$ = CLKCNTL = 3V, C_{LOAD} = 5pF			0.3		ns
$\overline{SER}$ High Level Input Voltage	Pin 17	●	$V+_D$ – 0.3			V
$\overline{SER}$ Low Level Input Voltage	Pin 17	●			0.3	V
$\overline{SER}$ Input Current	Pin 17 = 0V (Note 6) Pin 17 = $V+_D$	● ●	–10		 2	µA µA
CLKCNTL High Level Input Voltage	Pin 5	●	$V+_D$ – 0.5			V
CLKCNTL Low Level Input Voltage	Pin 5				0.5	V
CLKCNTL Input Current	CLKCNTL = 0V (Note 6) CLKCNTL = $V+_D$	● ●	–25	–15 15	 25	µA µA

Pin Programmable Control Mode Specifications. Specifications apply to Pins 6, 9, 21 and 22 in pin programmable control mode.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V+_D$ = 2.7V to 3.6V							
V_{IH}	Digital Input High Voltage	Pins 6, 9, 21, 22	●	2			V
V_{IL}	Digital Input Low Voltage	Pins 6, 9, 21, 22	●			0.8	V
I_{IN}	Digital Input Current	Pins 6, 9, 21, 22 (Note 6)	●	–1		1	µA

Serial Port DC and Timing Specifications. Specifications apply to Pins 6, 9-11, and 21 in serial programming mode.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V+_D$ = 2.7V to 3.6V							
V_{IH}	Digital Input High Voltage	Pins 6, 9, 10	●	2			V
V_{IL}	Digital Input Low Voltage	Pins 6, 9, 10	●			0.8	V
I_{IN}	Digital Input Current	Pins 6, 9, 10 (Note 6)	●	–1		1	µA
V_{OH}	Digital Output High Voltage	Pins 11, 21 Sourcing 500µA	●	V_{SUPPLY} – 0.3			V
V_{OL}	Digital Output Low Voltage	Pins 11, 21 Sinking 500µA	●			0.3	V
t_1 (Note 5)	SDI Valid to SCLK Setup		●	60			ns
t_2 (Note 5)	SDI Valid to SCLK Hold		●	0			ns
t_3	SCLK Low		●	100			ns
t_4	SCLK High		●	100			ns
t_5	$\overline{CS}$ Pulse Width		●	60			ns
t_6 (Note 5)	LSB SCLK to $\overline{CS}$		●	60			ns
t_7 (Note 5)	$\overline{CS}$ Low to SCLK		●	30			ns
t_8	SDO Output Delay	C_L = 15pF	●			125	ns
t_9 (Note 5)	SCLK Low to $\overline{CS}$ Low		●	0			ns

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: LTC6603C and LTC6603I are guaranteed functional over the operating temperature range of –40°C to 85°C.

Note 3: LTC6603C is guaranteed to meet specified performance from 0°C to 70°C. The LTC6603C is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LTC6603I is guaranteed to meet the specified performance limits from –40°C to 85°C.

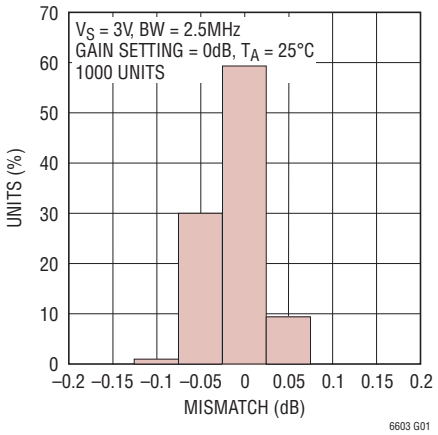
Note 4: This test measures the internal oscillator accuracy (deviation from the f_{CLK} equation). Variations in the internal oscillator cause variations in the filter cutoff frequency. See the "Applications Information" section.

Note 5: Guaranteed by design, not subject to test.

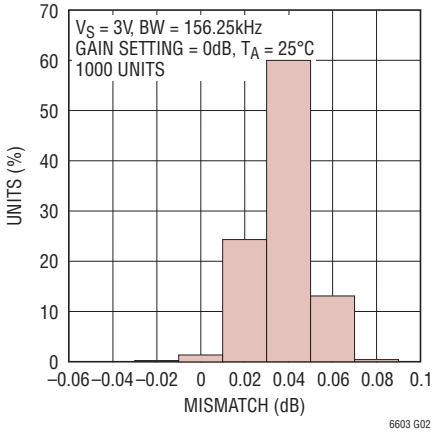
Note 6: To conform to the logic IC standard, current out of a pin is arbitrarily given a negative value.

TYPICAL PERFORMANCE CHARACTERISTICS

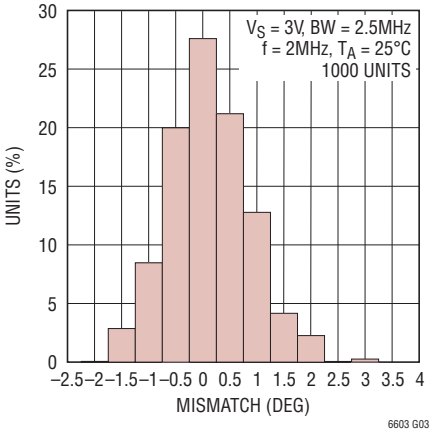
DC Gain Matching



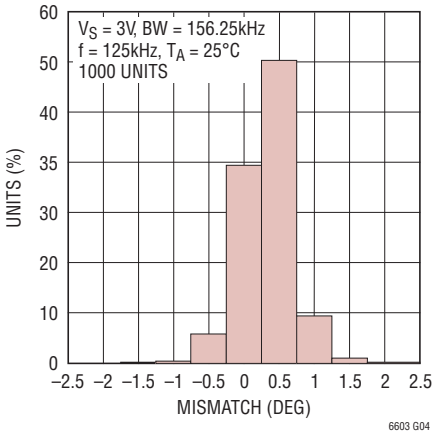
DC Gain Matching



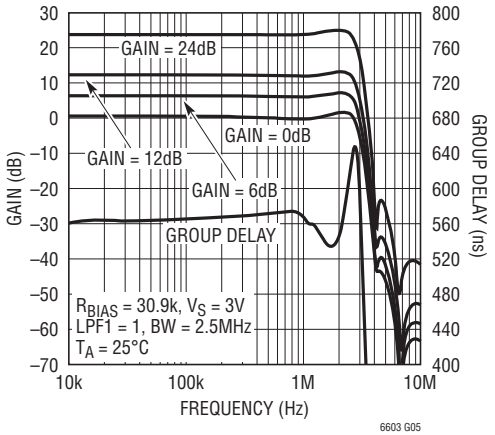
Phase Matching



Phase Matching

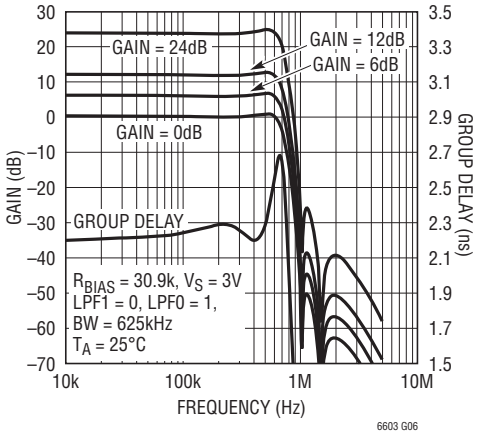


Gain and Group Delay vs Frequency

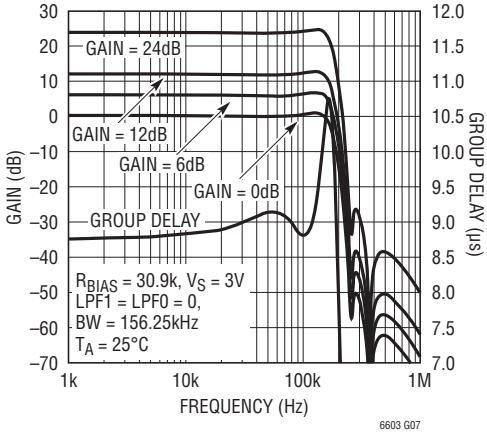


TYPICAL PERFORMANCE CHARACTERISTICS

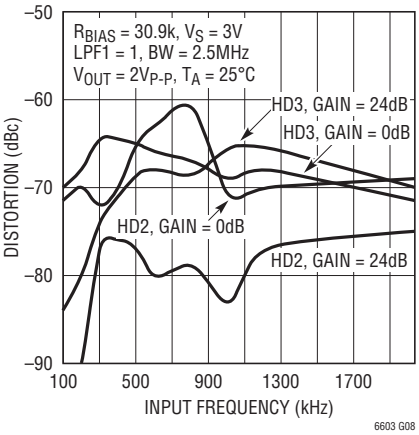
Gain and Group Delay vs Frequency



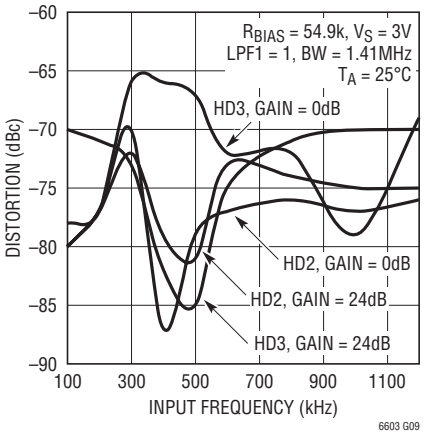
Gain and Group Delay vs Frequency



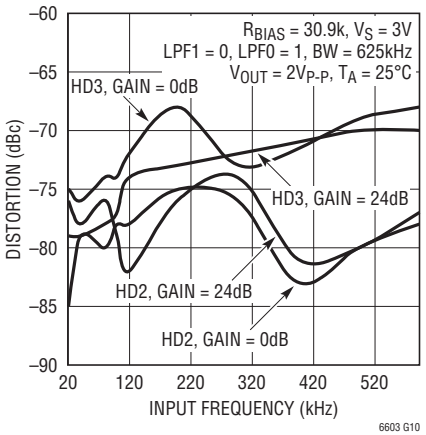
Distortion vs Input Frequency



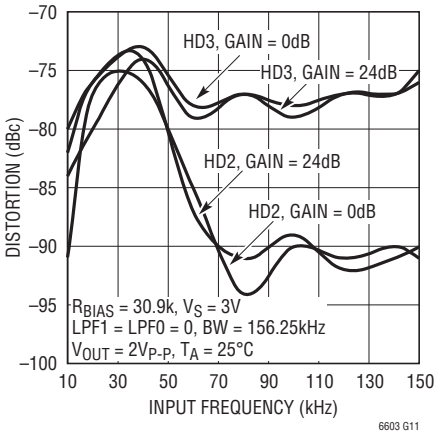
Distortion vs Input Frequency



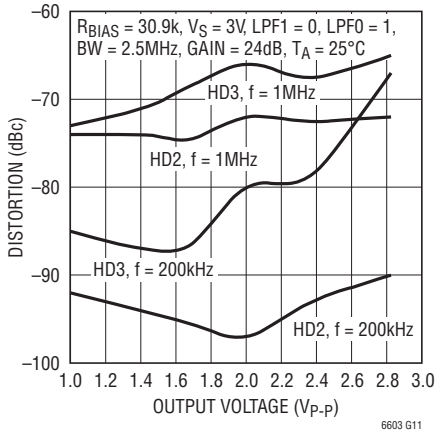
Distortion vs Input Frequency



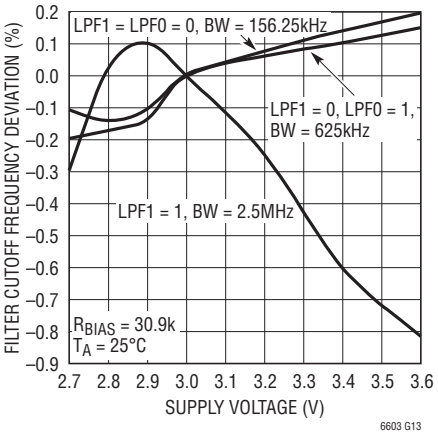
Distortion vs Input Frequency



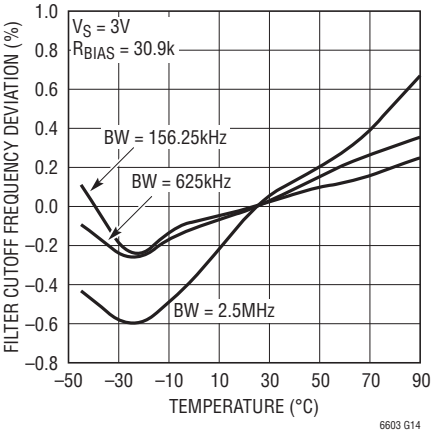
Distortion vs Output Voltage



Filter Cutoff Accuracy vs Supply Voltage

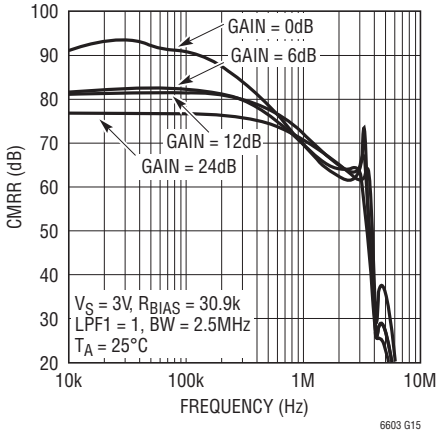


Filter Cutoff Accuracy vs Temperature

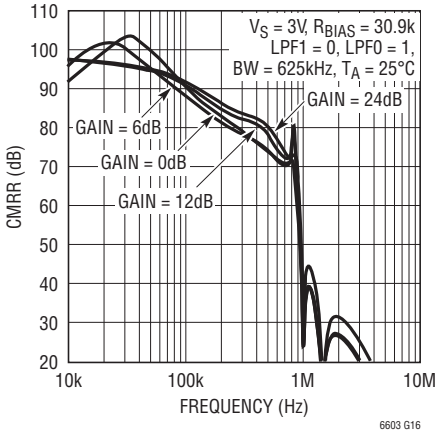


TYPICAL PERFORMANCE CHARACTERISTICS

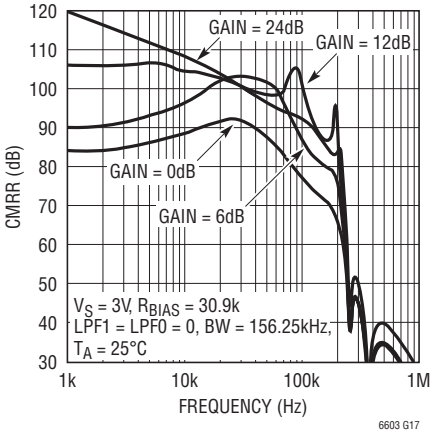
Common Mode Rejection Ratio



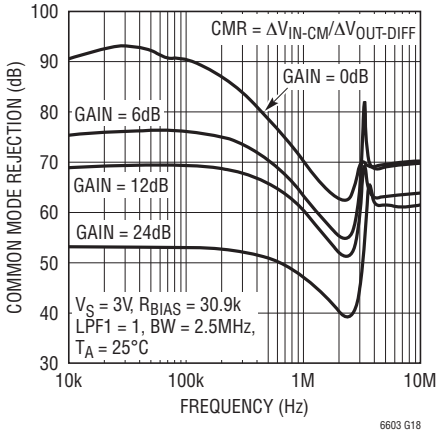
Common Mode Rejection Ratio



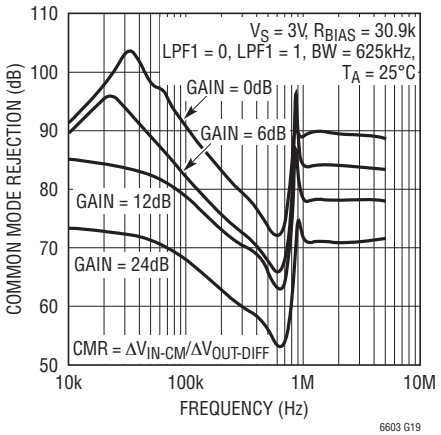
Common Mode Rejection Ratio



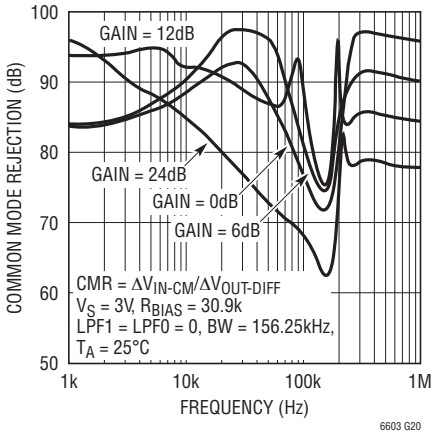
Common Mode Rejection



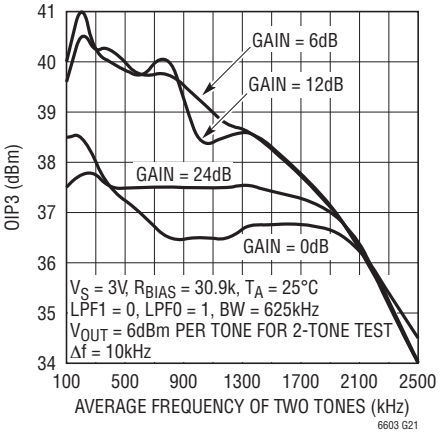
Common Mode Rejection



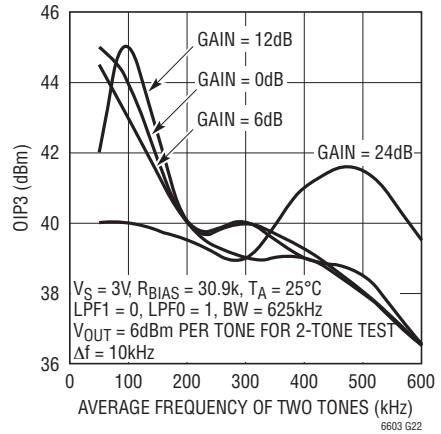
Common Mode Rejection



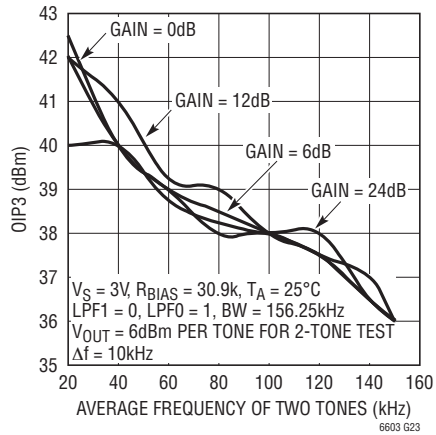
OIP3 vs Average Signal Frequency



OIP3 vs Average Signal Frequency

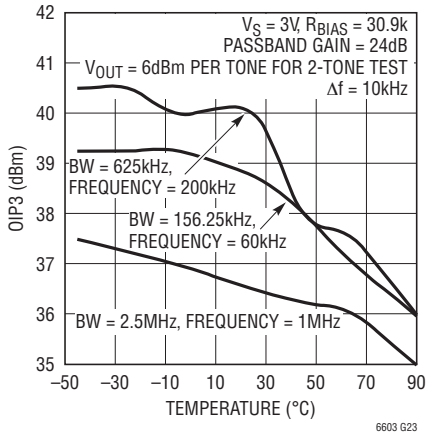


OIP3 vs Average Signal Frequency

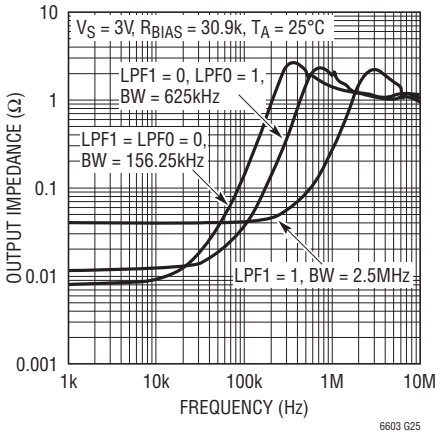


TYPICAL PERFORMANCE CHARACTERISTICS

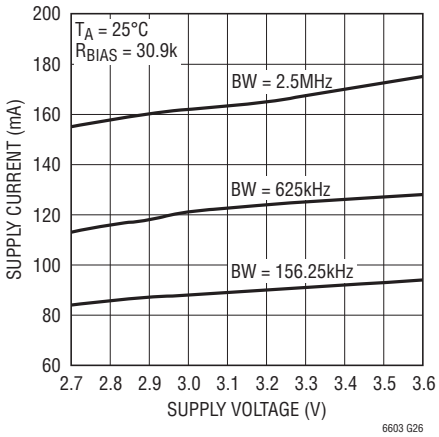
OIP3 vs Temperature



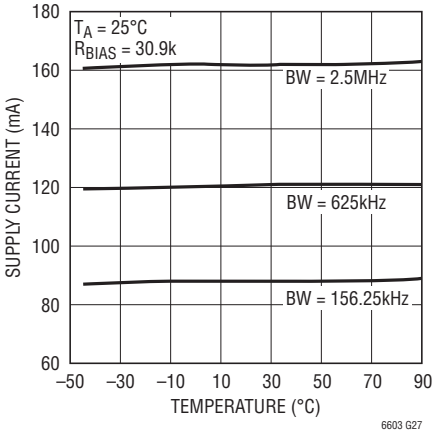
Output Impedance vs Frequency



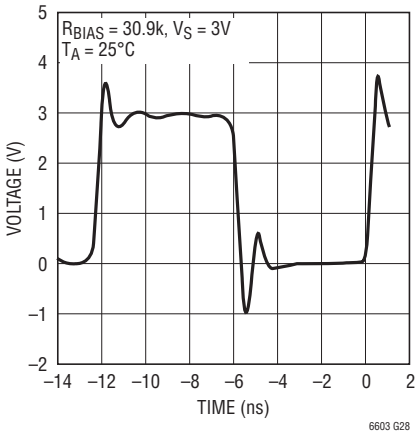
Supply Current vs Supply Voltage



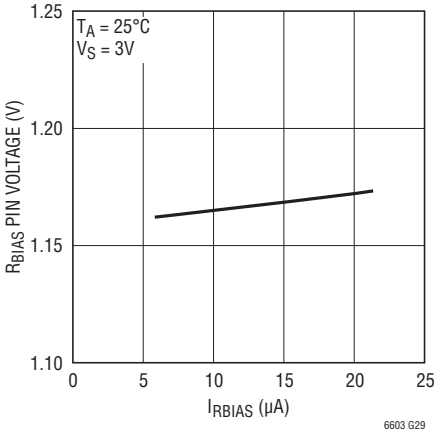
Supply Current vs Temperature



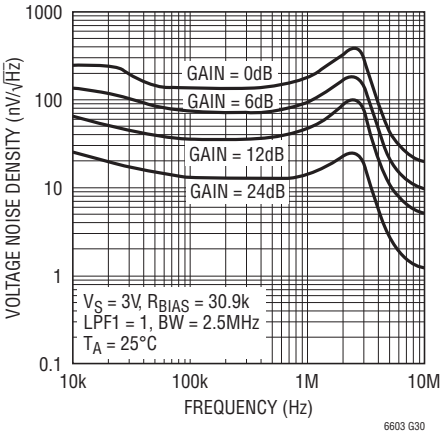
Clock Output Operating at 80MHz



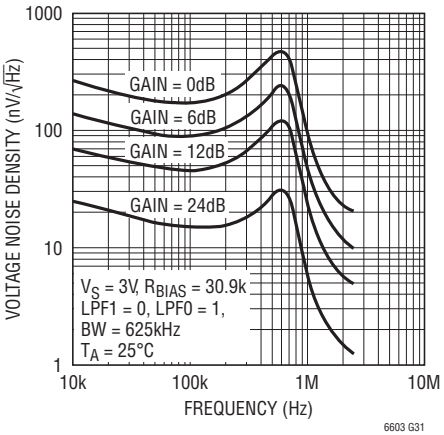
R_{BIAS} Pin Voltage vs I_{RBIAS}



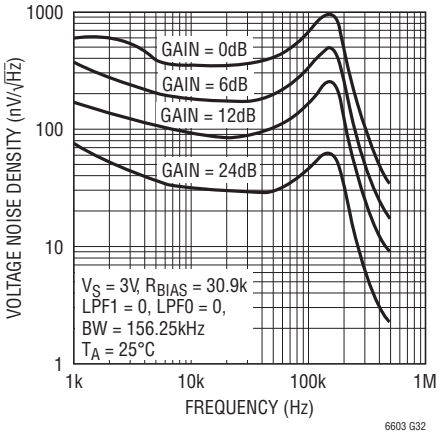
Input Referred Noise Density



Input Referred Noise Density

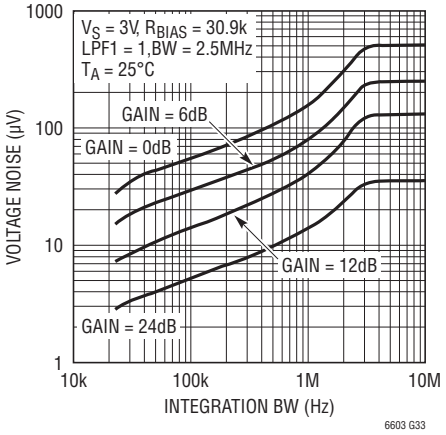


Input Referred Noise Density

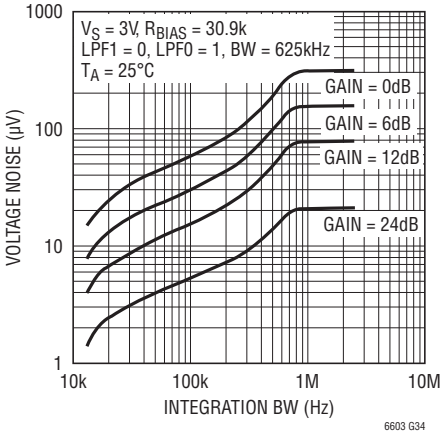


TYPICAL PERFORMANCE CHARACTERISTICS

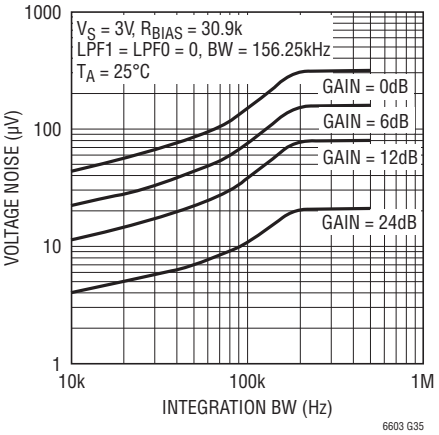
Integral Input Referred Noise



Integral Input Referred Noise



Integral Input Referred Noise



PIN FUNCTIONS

$V+_{IN}$ (Pin 1): Input Voltage Supply (2.7V ≤ V ≤ 5.5V). This supply must be kept free from noise and ripple. It should be bypassed directly to a ground plane with a 0.1µF capacitor unless it is tied to $V+_A$ (Pin 2). The bypass should be as close as possible to the IC, but is not as critical as the bypassing of $V+_A$ and $V+_D$ (Pin16).

$V+_A$ (Pin 2): Analog Voltage Supply (2.7V ≤ V ≤ 3.6V). This supply must be kept free from noise and ripple. It should be bypassed directly to a ground plane with a 0.1µF capacitor. The bypass should be as close as possible to the IC.

V_{OCM} (Pin 3): Output Common Mode Voltage Reference. If floated, an internal resistive divider sets the voltage on this pin to half the supply voltage (typically 1.5V), maximizing the dynamic range of the filter. If this pin is floated, it must be bypassed with a quality 1µF capacitor to ground. This pin has a typical input impedance of 3.4k and may be overdriven. Driving this pin to a voltage other than the default value will reduce the signal range the filter can handle before clipping.

R_{BIAS} (Pin 4): Oscillator Frequency-Setting Resistor Input. The value of the resistor connected between this pin and ground determines the frequency of the master oscillator, and sets the bias currents for the filter networks. The voltage on this pin is held by the LTC6603 to approximately 1.17V. For best performance, use a precision metal film resistor with a value between 30.9k and 200k and limit the capacitance on this pin to less than 10pF. This resistor is necessary even if an external clock is used.

CLKCNTL (Pin 5): Clock Control Input. This three-state input selects the function of CLKIO (Pin 15). Tying the CLKCNTL pin to ground allows the CLKIO pin to be driven by an external clock (CLKIO is the master clock input). If the CLKCNTL pin is floated, the internal oscillator is enabled, but the master clock is not present at the CLKIO pin (CLKIO is a no-connect). If the CLKCNTL pin is tied to $V+_D$ (Pin 16), the internal oscillator is enabled and the master clock is present at the CLKIO pin (CLKIO is the master clock output). To detect a floating CLKCNTL pin, the LTC6603 attempts to pull the pin toward mid-supply. This is realized with two internal 15µA current sources, one tied to $V+_D$ and CLKCNTL and the other one tied to ground and CLKCNTL. Therefore, driving the CLKCNTL pin high requires sourcing approximately 15µA. Likewise, driving the CLKCNTL pin low requires sinking 15µA. When the CLKCNTL pin is floated, it should be bypassed by a 1nF capacitor to ground or be surrounded by a ground shield to prevent excessive coupling from other PCB traces.

PIN FUNCTIONS

LPF1($\overline{CS}$) (Pin 6): TTL Level Input. When in pin programmable control mode, this pin is the MSB of the lowpass cutoff frequency control code; in serial control mode, this pin is the chip select input (active low).

+INB, –INB (Pins 7, 8): Channel B Differential Inputs. The input range and input resistance are described in the Applications Information section. Input voltages which exceed $V+_{IN}$ (Pin 1) should be avoided.

LPF0 (SCLK) (Pin 9): TTL Level Input. When in pin programmable control mode, this pin is the LSB of the lowpass cutoff frequency control code; in serial control mode, this pin is the clock of the serial interface.

SDI (Pin 10): TTL Level Input. When in pin programmable control mode, this pin is left floating; in serial control mode, this pin is the serial data input.

SDO (Pin 11): TTL Level Input. When in pin programmable control mode, this pin is left floating; in serial control mode, this pin is the serial data output.

–OUTB, +OUTB (Pins 12, 13): Channel B Differential Filter Outputs. These pins can drive 1k and/or 50pF loads. For larger capacitive loads, an external 100Ω series resistor is recommended for each output. The common mode voltage of the filter outputs is the same as the voltage at V_{OCM} (Pin 3).

GND (Pin 14): Ground. Should be tied to a ground plane for best performance.

CLKIO (Pin 15): When CLKCNTL (Pin 5) is tied to ground, CLKIO is the master clock input. When CLKCNTL is floated, CLKIO is pulled to ground by a weak pulldown. When CLKCNTL is tied to $V+_D$ (Pin 16), CLKIO is the master clock output. When configured as a clock output, this pin can drive 1k and/or 5pF loads (heavier loads will cause inaccuracies).

$V+_D$ (Pin 16): Digital Voltage Supply (2.7V ≤ V ≤ 3.6V). This supply must be kept free from noise and ripple. It should be bypassed directly to a ground plane with a 0.1µF capacitor. The bypass should be as close as possible to the IC.

$\overline{SER}$ (Pin 17): Interface Selection Input. When tied to $V+_D$ (Pin 16) or floated, the interface is in pin programmable control mode, i.e. the filter gain and cutoff frequencies are programmed by the GAIN1, GAIN0, LPF1 and LPF0 pins. When $\overline{SER}$ is tied to ground, the filter gain, the filter cutoff frequency and shutdown mode are programmed by the serial interface.

–OUTA, +OUTA (Pins 18, 19): Channel A Differential Filter Outputs. These pins can drive 1k and/or 50pF loads. For larger capacitive loads, an external 100Ω series resistor is recommended for each output. The common mode voltage of the filter outputs is the same as the voltage at V_{OCM} (Pin 3).

CAP (Pin 20): Connect a 0.1µF bypass capacitor to this pin. Pin 20 is a buffered version of Pin 3.

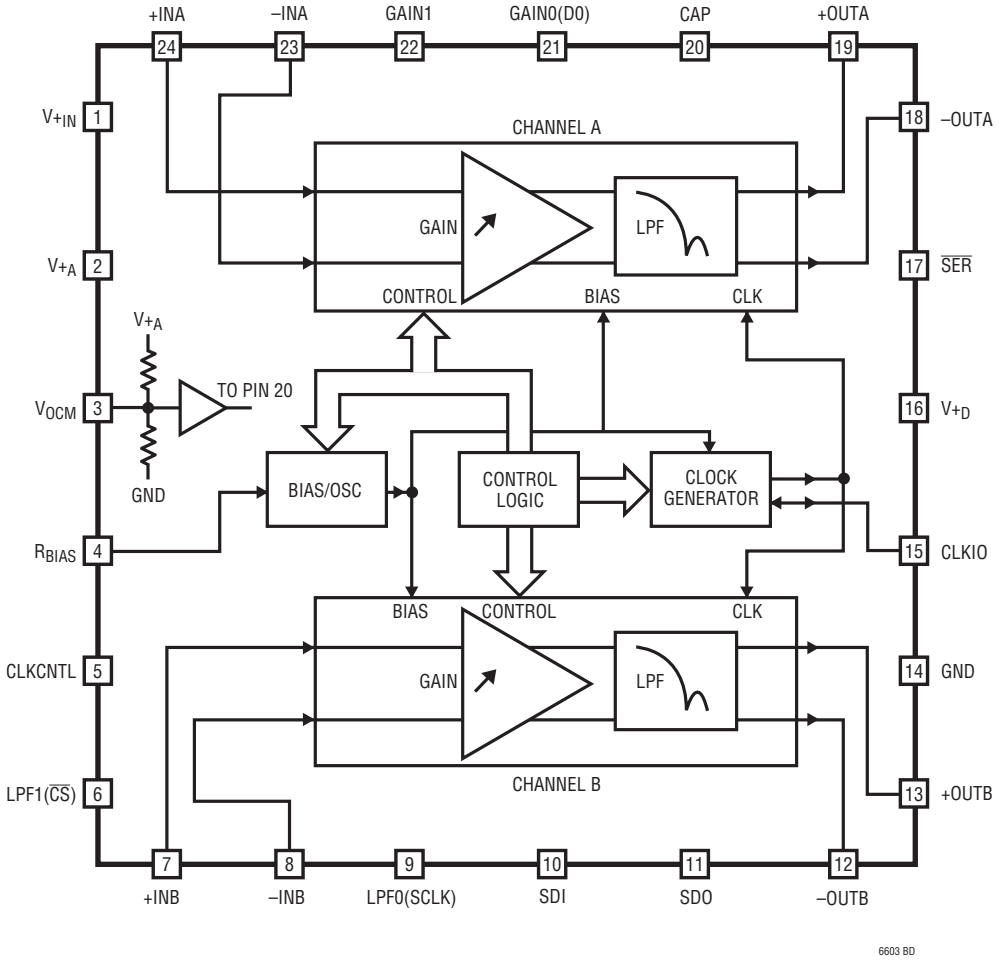
GAIN0(D0) (Pin 21): TTL Level Input. When in pin programmable control mode, this pin is the LSB of the gain control code; in serial control mode, this pin is the LSB of the serial control register, an output.

GAIN1 (Pin 22): TTL Level Input. When in pin programmable control mode, this pin is the MSB of the gain control code; in serial control mode, this pin is a no-connect.

–INA, +INA (Pins 23, 24): Channel A Differential Inputs. The input range and input resistance are described in the Applications Information section. Input voltages which exceed $V+_{IN}$ (Pin 1) should be avoided.

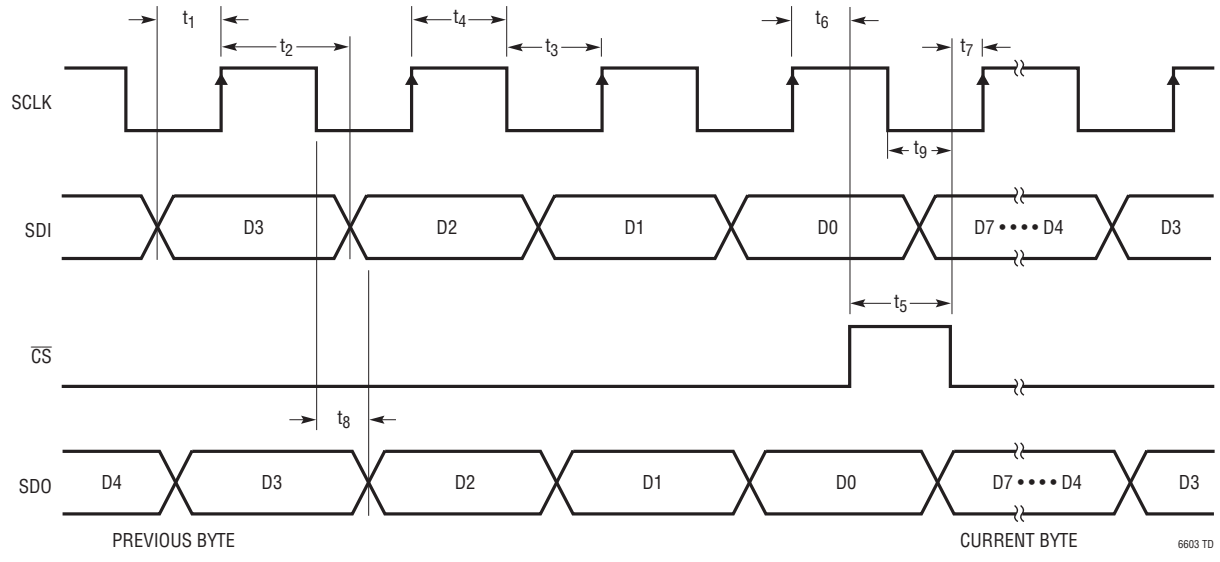
Exposed Pad (Pin 25): Ground. The Exposed Pad must be soldered to PCB.

BLOCK DIAGRAM



TIMING DIAGRAM

Timing Diagram of the Serial Interface



APPLICATIONS INFORMATION

Theory of Operation (Refer to Block Diagram)

The LTC6603 features two matched filter channels, each containing gain control and lowpass filter networks that are controlled by a single control block and clocked by a single clock generator. The gain and cutoff frequency can be separately programmed. The two channels are not independent, i.e. if the gain is set to 24dB then both channels have a gain of 24dB. The filter can be clocked with an external clock source, or using the internal oscillator. A resistor connected to the R_{BIAS} pin sets the bias currents for the filter networks and the internal oscillator frequency (unless driven by an external clock). Altering the clock frequency changes the filter bandwidth. This allows the filters to be "tuned" to many different bandwidths.

Pin Programmable Interface

As shown in Figure 1, connecting $\overline{SER}$ to $V+_D$ allows the filter to be directly controlled through the pin programmable control lines GAIN1, GAIN0, LPF1 and LPF0. The GAIN0(D0) pin is bidirectional (input in pin programmable control mode, output in serial mode). In pin programmable control mode, the voltage at GAIN0(D0) cannot exceed $V+_D$; otherwise, large currents can be injected to $V+_D$ through the parasitic diodes (see Figure 2). Connecting a 10k resistor at the GAIN0(D0) pin (see Figure 1) is recommended for current limiting, to less than 10mA. $\overline{SER}$ has an internal pull-up to $V+_D$. None of the logic inputs have an internal pull-up or pull-down.

Serial Interface

Connecting $\overline{SER}$ to ground allows the filter to be controlled through the SPI serial interface. When $\overline{CS}$ is low, the serial data on SDI is shifted into an 8-bit shift register on the rising edge of the clock (SCLK), with the MSB transferred first (see Figure 3). Serial data on SDO is shifted out on the clock's falling edge. A high $\overline{CS}$ will load the 8 bits of the shift register into an 8-bit D-latch, which is the serial control register. The clock is disabled internally when $\overline{CS}$ is pulled high. Note: SCLK must be low before $\overline{CS}$ is pulled low to avoid an extra internal clock pulse. SDO is always active in serial mode (never tri-stated) and cannot be "wire-ORed" to other SPI outputs. In addition, SDO is not forced to zero when $\overline{CS}$ is pulled high.

An LTC6603 may be daisy-chained with other LTC6603s or other devices having serial interfaces. Daisy chaining is accomplished by connecting the SDO of the lead chip to the SDI of the next chip, while SCLK and $\overline{CS}$ remain common to all chips in the daisy chain. The serial data is clocked to all the chips then the $\overline{CS}$ signal is pulled high to update all of them simultaneously. Figure 4 shows an example of two LTC6603s in a daisy-chained SPI configuration.

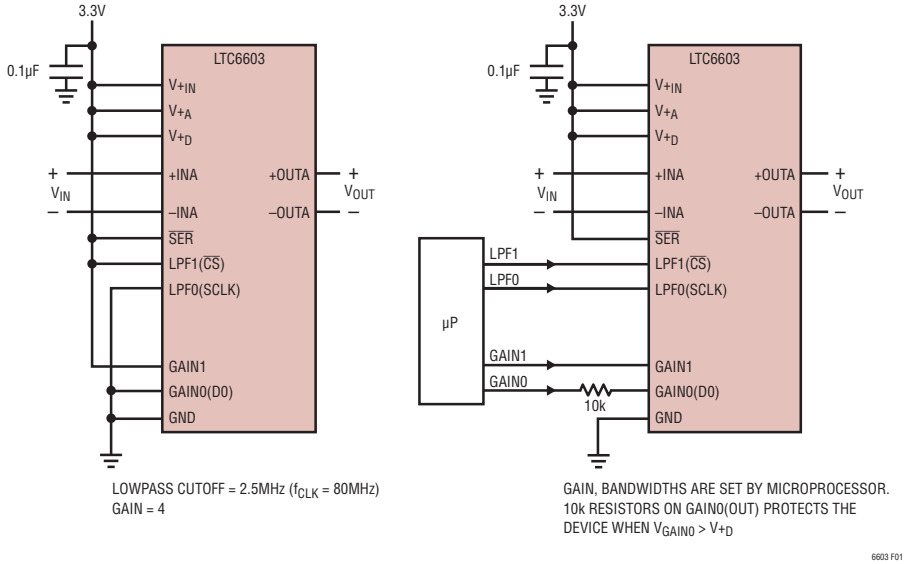


Figure 1. Filter in Pin Programmable Control Mode

APPLICATIONS INFORMATION

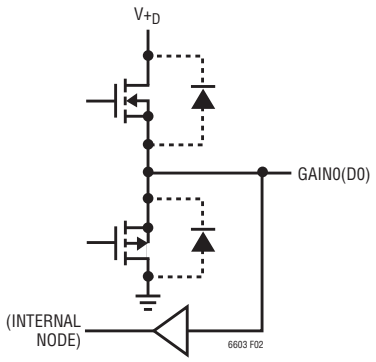


Figure 2. Bidirectional Design of GAIN0(OUT) Pin

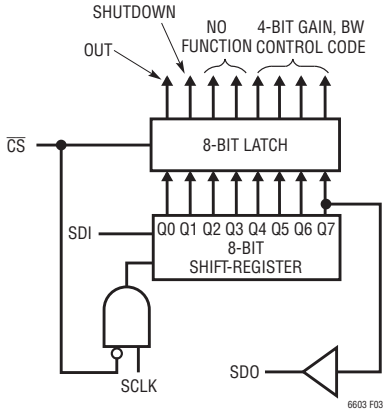


Figure 3. Diagram of Serial Interface (MSB First Out)

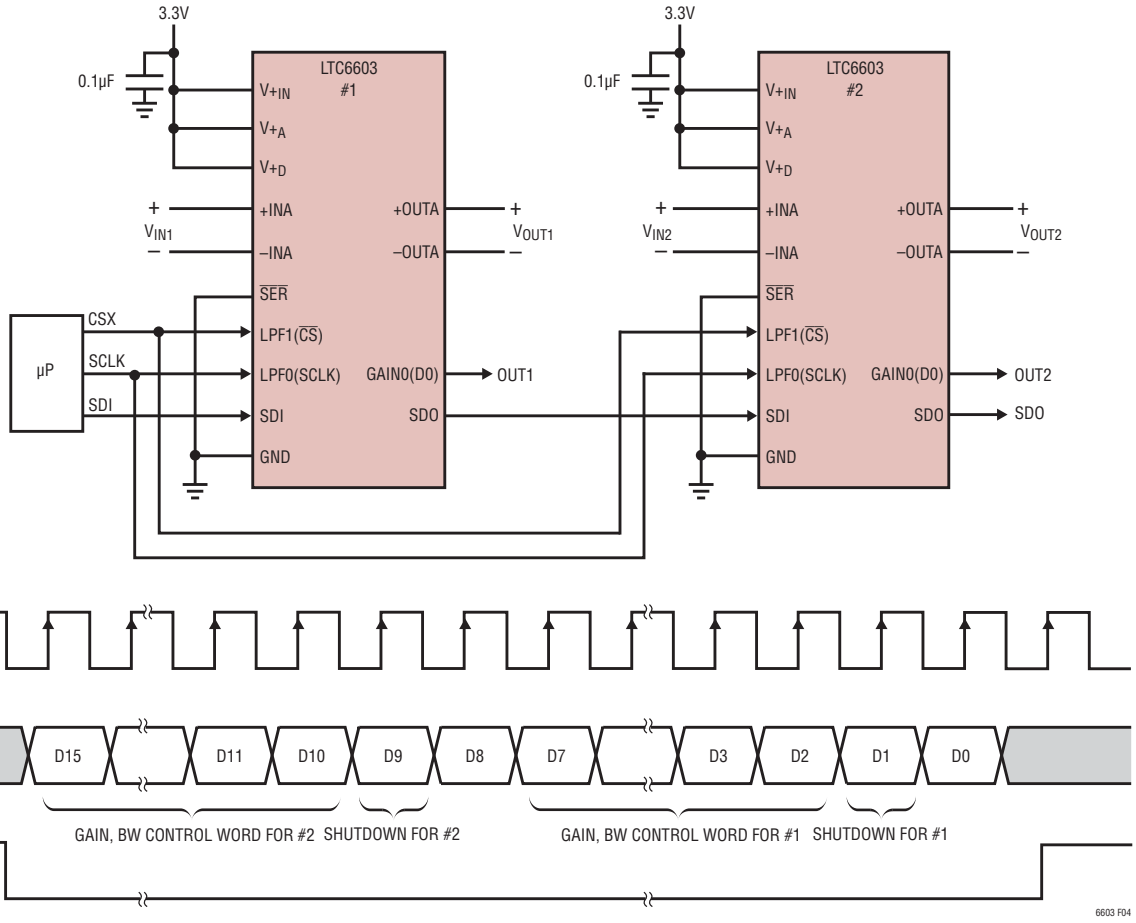


Figure 4. Two Devices in a Daisy Chain

Serial Control Register Definition

D7	D6	D5	D4	D3	D2	D1	D0
GAIN0	GAIN1	LPF0	LPF1	NO FUNCTION	NO FUNCTION	SHDN	OUT

APPLICATIONS INFORMATION

GAIN1 and GAIN0 are the gain control bits (register bits D6 and D7 when in serial mode). Their function is shown in Table 1. In serial mode, register bit D1 can be set to 1 to put the device into a low power shutdown mode. Register bit D0 is a general purpose output (Pin 21) when in serial mode.

Table 1. Gain Control

GAIN 1	GAIN 0	PASSBAND GAIN (dB)
0	0	0
0	1	6
1	0	12
1	1	24

Self-Clocking Operation

The LTC6603 features a unique internal oscillator which sets the filter cutoff frequency using a single external resistor connected to the R_{BIAS} pin. The clock frequency is determined by the following simple formula (see Figure 5):

$$f_{CLK} = 247.2MHz \bullet 10k/R_{BIAS}$$

Note: $R_{BIAS} \leq 200k$

The design is optimized for $V+_A$, $V+_D$ = 3V, f_{CLK} = 45MHz, where the filter cutoff frequency error is typically <3% when a 0.1% external 54.9k resistor is used (any resistor (R_{BIAS}) tolerance, will shift the clock frequency). With different resistor values and cutoff frequency control settings (LPF1 and LPF0), the lowpass cutoff frequency can be accurately varied from 24.14kHz to 2.5MHz. Table 2 summarizes the cutoff frequencies that can be obtained with an external resistor (R_{BIAS}) value of 30.9k. Note that the cutoff frequencies scale with the clock frequency. For example, if LPF1 and LPF0 are both equal to zero, and R_{BIAS} is increased from 30.9k to 200k, f_{CLK} will decrease from 80MHz to 12.36MHz and the cutoff frequency will be reduced from 156.25kHz to 24.14kHz. The cutoff frequencies that can be obtained with external resistor values of 54.9k and 200k are shown in Table 3 and Table 4, respectively. When the LTC6603 is programmed for the cutoff frequencies lower than the maximum, the power is automatically reduced. The power savings at the middle bandwidth setting (LPF1 = 0, LPF0 = 1), is about 23%, while the power savings at the lowest bandwidth setting (LPF1 = 0, LPF0 = 0) is about 60%.

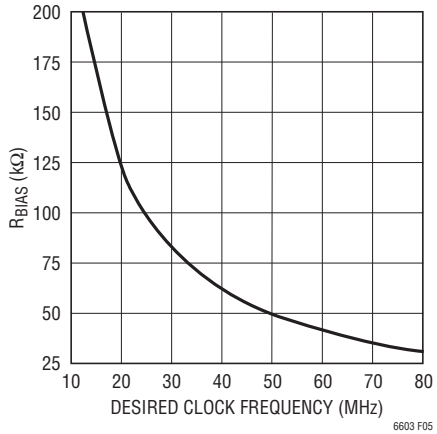


Figure 5. R_{BIAS} vs Desired Clock Frequency

Table 2. Cutoff Frequency Control, R_{BIAS} = 30.9k, f_{CLK} = 80MHz

LPF1	LPF0	LOWPASS BW(kHz)
0	0	156.25
0	1	625
1	0	2500
1	1	2500

Table 3. Cutoff Frequency Control, R_{BIAS} = 54.9k, f_{CLK} = 45MHz

LPF1	LPF0	LOWPASS BW(kHz)
0	0	87.94
0	1	351.78
1	0	1407
1	1	1407

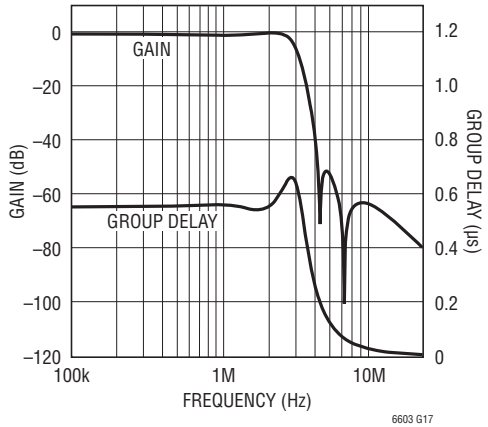
Table 4. Cutoff Frequency Control, R_{BIAS} = 200k, f_{CLK} = 12.36MHz

LPF1	LPF0	LOWPASS BW(kHz)
0	0	24.14
0	1	96.56
1	0	386.25
1	1	386.25

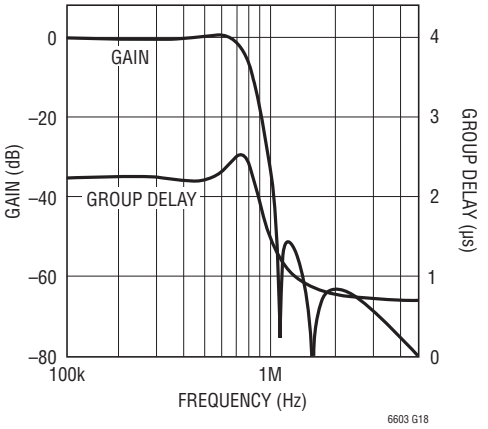
APPLICATIONS INFORMATION

The following graphs show a few of the possible lowpass filters.

Gain and Group Delay vs Frequency (2.5MHz Lowpass Response)



Gain and Group Delay vs Frequency (650kHz Lowpass Response)



The oscillator is sensitive to transients on the positive supply. The IC should be soldered to the PC board and the PCB layout should include a 0.1µF ceramic capacitor between $V+_A$ (Pin 2) and ground, as close as possible to the IC to minimize inductance. The PCB layout should also include an additional 0.1µF ceramic capacitor between $V+_D$ (Pin 16) and ground. Avoid parasitic capacitance on R_{BIAS} (Pin 4) and avoid routing noisy signals near R_{BIAS}. Use a ground plane connected to Pin 14 and the Exposed Pad (Pin 25).

Alternative Methods of Setting the Clock Frequency of the LTC6603

The oscillator may be programmed by any method that sinks a current out of the R_{BIAS} pin. The circuit in Figure 6 sets the clock frequency by using a programmable current source and in the expression for f_{CLK}, the resistor R_{BIAS} is replaced by the ratio of $1.17V/I_{CONTROL}$. Because the voltage of the R_{BIAS} pin is approximately 1.17V ±5%, the Figure 6 circuit is less accurate than if a resistor controls the clock frequency.

In this circuit, the LTC2621 (a 12-bit DAC) is daisy-chained with the LTC6603. Because the sinking current from the R_{BIAS} pin is:

$$\frac{V_{RBIAS} \bullet k}{2^N \bullet R1}$$

the equivalent R_{BIAS} is:

$$\frac{2^N \bullet R1}{k},$$

where k is the binary DAC input code and N is the resolution. Figure 7 shows some of the frequency responses that can be obtained using this circuit.

Figure 8 shows the LTC6603's oscillator configured as a VCO. A voltage source is connected in series with the R_{BIAS} resistor. The clock frequency, f_{CLK}, will vary with $V_{CONTROL}$. Again, this circuit decouples the relationship between the current out of the R_{BIAS} pin and the voltage of the R_{BIAS} pin; the frequency accuracy will be degraded. The clock frequency, however, will increase monotonically with decreasing $V_{CONTROL}$.

Operation Using an External Clock

The LTC6603 may be clocked by an external oscillator for tighter bandwidth control by pulling CLKCNTL (Pin 5) to ground and driving a clock into CLKIO (Pin 15). If an external clock is used, the R_{BIAS} resistor is still necessary. The value of R_{BIAS} must be no larger than the value that would be required for using the internal oscillator. For example, a 100k resistor would program the internal oscillator for 24.705MHz, so an external oscillator frequency of 24.705MHz would require an R_{BIAS} resistance of no more

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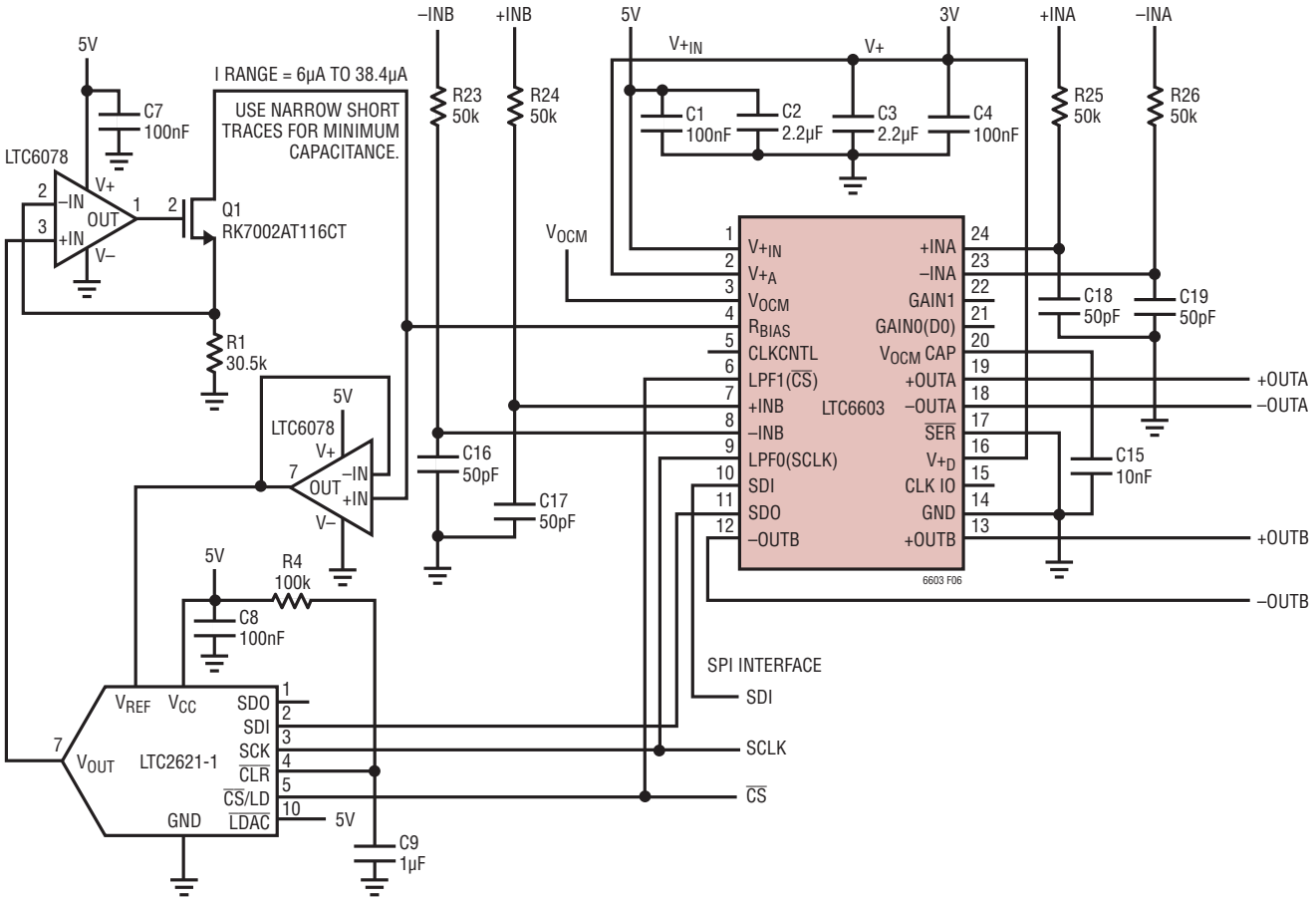

CLR LOW WILL SET DAC TO MID-SCALE (WITH A LTC6603-1 VERSION). HAS ~100ms TC AT START-UP TO RESET TO ZERO-SCALE.

DATA FORMAT
DATA IS SHIFTED FROM MOSI (MASTER OUT, SLAVE IN) THRU LTC6603 INTO THE LTC2621.
THE TOTAL PACKET IS 32 BITS. IT STARTS WITH A CONTROL BYTE (0011 XXXX) THEN MSB OF THE DAC, WITH DUMMY BITS AT THE END, 16 BITS (24 BITS TOTAL). THEN 8 BITS TO THE FILTER.
D6 AND D7 = GAIN, D4 AND D5 = LPF, D1 = SHDN. D0 = GEN. PURPOSE OUTPUT.

Figure 6. Current Controlled Clock Frequency

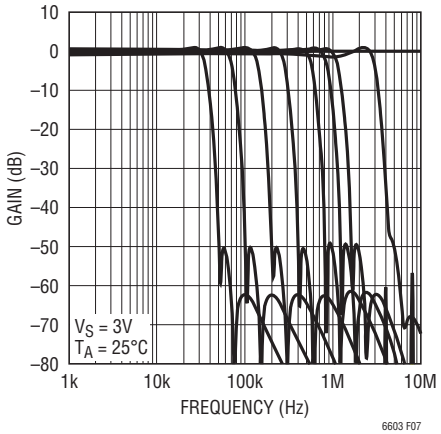

Figure 7. Frequency Response Controlled by LTC2621-1

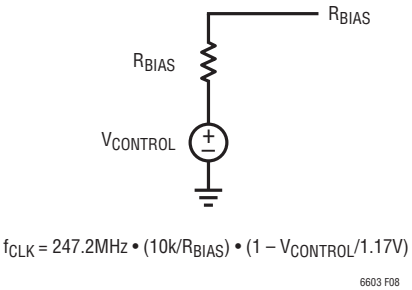

Figure 8. Voltage Controlled Clock Frequency

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than 100k. If the value of R_{BIAS} is too large, the filters will not receive a large enough bias current, possibly causing errors due to insufficient settling. Be sure to obey the absolute maximum specifications when driving a clock into CLKIO (Pin 15).

Input Common Mode and Differential Voltage Range

The input signal range extends from zero to the $V+_{IN}$ supply voltage. This input supply can be tied to $V+_A$ and $V+_D$, or driven up to 5.5V for increased input signal range. Figure 9 shows the distortion of the filter versus common mode input voltage with a $2V_{P-P}$ differential input signal ($V+_{IN}$ = 5V).

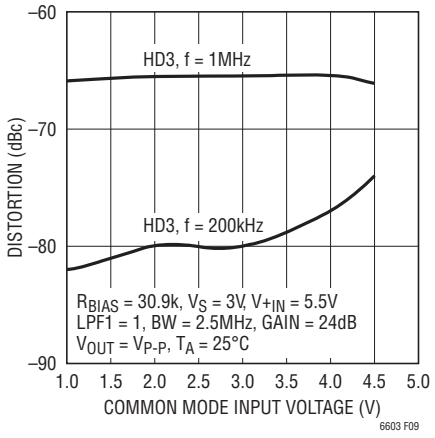

Figure 9. Distortion vs Common Mode Input Voltage (5V)

For best performance, the inputs should be driven differentially. For single-ended signals, connect the unused input to V_{OCM} (Pin 3) or to a quiet DC reference voltage. To achieve the best distortion performance, the input signal should be centered around the DC voltage of the unused input.

Refer to the Typical Performance Characteristics section to estimate the distortion for a given input level.

Dynamic Input Impedance

The unique input sampling structure of the LTC6603 has a dynamic input impedance which depends on the configuration and the clock frequency. This dynamic input impedance has both a differential component and a common mode component. The common mode input impedance is a function of the clock frequency and the control bits LPF1 and LPF0. The differential input impedance is a function of the clock frequency and the control bits LPF1, LPF0, GAIN1 and GAIN0. Table 5 shows the typical input impedances for a clock frequency of 80MHz. These input impedances are all proportional to $1/f_{CLK}$, so if the clock frequency were reduced by half to 40MHz, the impedances would be doubled. The typical variation in dynamic input impedance for a given clock frequency is –20% to +35%.

Table 5. Differential, Common Mode Input Impedances, f_{CLK} = 80MHz

GAIN1	GAIN0	LPF1	LPF0	DIFFERENTIAL INPUT IMPEDANCE (kΩ)	COMMON MODE INPUT IMPEDANCE (kΩ)
0	0	0	0	38	40
0	0	0	1	16	20
0	0	1	0	2.5	5
0	0	1	1	2.5	5
0	1	0	0	20	40
0	1	0	1	9.5	20
0	1	1	0	2.5	5
0	1	1	1	2.5	5
1	0	0	0	10	40
1	0	0	1	5.4	20
1	0	1	0	1.9	5
1	0	1	1	1.9	5
1	1	0	0	5.2	40
1	1	0	1	2.8	20
1	1	1	0	1.6	5
1	1	1	1	1.6	5

Output Common Mode and Differential Voltage Range

The output voltage is a fully differential signal with a common mode level equal to the voltage at V_{OCM}. Any of the filter outputs may be used as single-ended outputs, although this will degrade the performance. The output voltage range is typically 0.5V to $V+_A$ – 0.5V ($V+_A$ = 2.7V to 3.6V).

The common mode output voltage can be adjusted by overdriving the voltage present on V_{OCM}. To maximize the undistorted peak-to-peak signal swing of the filter, the V_{OCM} voltage should be set to $V+_A/2$. Note that the output common mode voltages of the two channels are

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not independent as they are both set by the V_{OCM} pin. Figure 10 illustrates the distortion versus output common mode voltage for a $2V_{P-P}$ differential input voltage and a common mode input voltage that is equal to mid-supply.

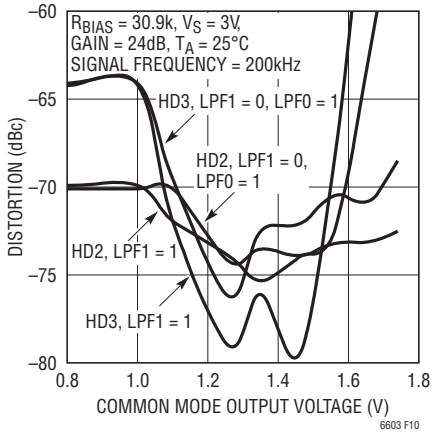

Figure 10. Distortion vs Common Mode Output Voltage

Interfacing to the LTC6603

The input and output common mode voltages of the LTC6603 are independent. The input common mode voltage is set by the signal source if DC-coupled, as shown in Figure 11. If the inputs are AC-coupled, as shown in Figure 12 (Circuit A), the input common mode voltage will be pulled to ground by an equivalent resistance of R_{CM}, shown in Table 5. This does not affect the filter's performance as long as the input amplitude is less than $0.5V_{P-P}$. At low filter gain settings, a larger input voltage swing may be desired.

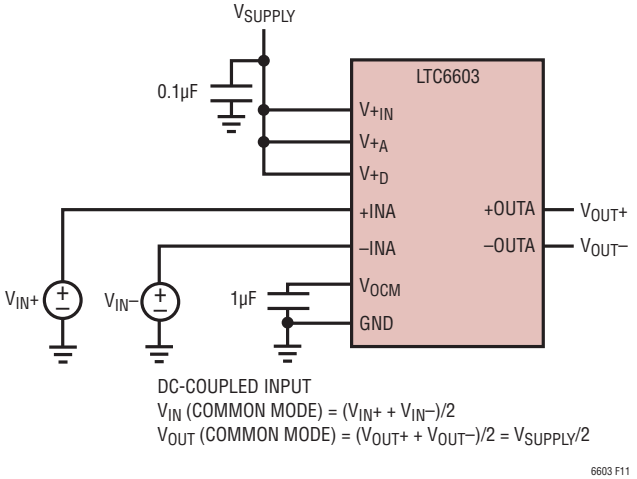

Figure 11. DC-Coupled Inputs

Connecting resistors between each input and $V+_{IN}$ will pull the input common mode voltage up, increasing the input signal swing. The resistance, $R_{PULL-UP}$, necessary to set the input common mode voltage, V_{ICM}, to any desired level can be calculated by

$$R_{PULL-UP} = R_{CM}\left(\frac{V_{SUPPLY}}{V_{ICM}} - 1\right)$$

where

$R_{CM} = 40k \bullet 80MHz/f_{CLK}$ for LPF1=0, LPF0=0

$R_{CM} = 20k \bullet 80MHz/f_{CLK}$ for LPF1=0, LPF0=1

$R_{CM} = 5k \bullet 80MHz/f_{CLK}$ for LPF1=1

For example, if the lowpass cutoff frequency is set to 2.5MHz, 5k resistors connected between each input and $V+_{IN}$ will set the input common mode voltage to mid-supply.

Circuit A of Figure 12 is for a fixed CLK and LPF0, LPF1 setting. If the clock varies or the LPF0, LPF1 setting changes then Circuit B of Figure 12 should be used.

Due to the sampled data nature of the filter, an anti-aliasing filter at the inputs is recommended.

The output common mode voltage is equal to the voltage of the V_{OCM} pin. The V_{OCM} pin is biased to one-half of the supply voltage by an internal resistive divider (see Block Diagram). To alter the common mode output voltage, V_{OCM} can be driven with an external voltage source or resistor network. If external resistors are used, it is important to note that the internal 2k resistors can vary ±30% (their ratio varies only ±1%). The filter outputs can also be AC-coupled.

The LTC6603 can be interfaced to an A/D converter by pulling CLKCNTL (Pin 5) to $V+_D$. This configures CLKIO (Pin 15) as a clock output, which can be used to drive the clock input of the A/D converter. This allows the A/D converter to be synchronized with the filter sampling clock, avoiding "beat frequencies" and simplifying the board layout. Any routing attached to the CLKIO pin should be as short as possible, in order to minimize reflections.

Similarly, the LTC6603 can be interfaced to another LTC6603 in a master/slave configuration as shown in Figure 13. This

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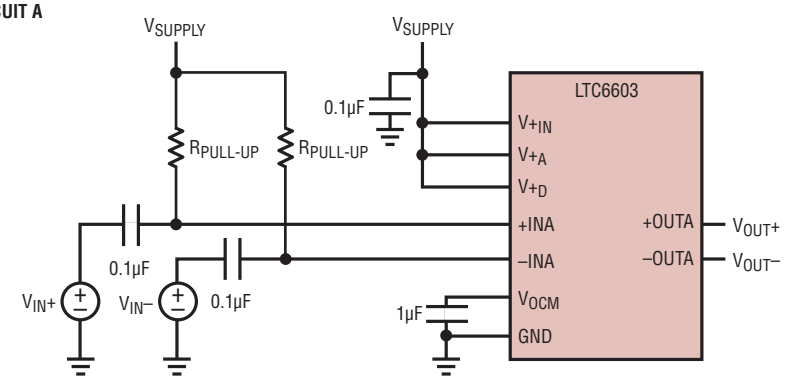
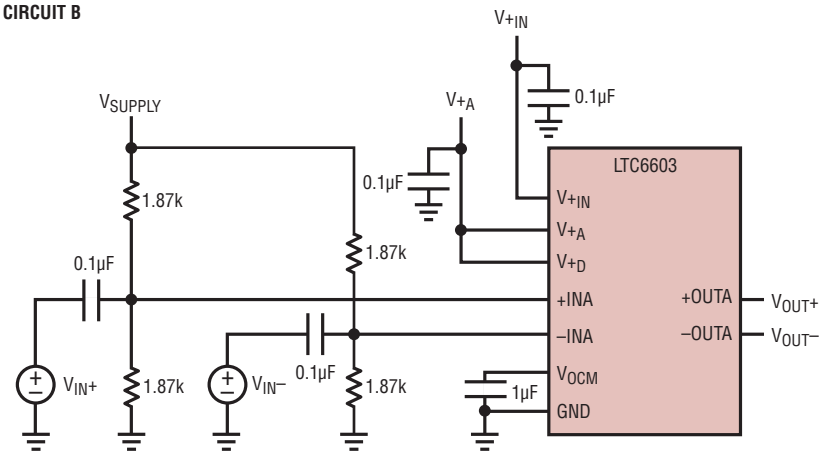
CIRCUIT A



AC-COUPLED INPUT
V_{IN} (COMMON MODE) = V_{OUT} (COMMON MODE) = $V_{SUPPLY}/2$

CIRCUIT B



AC-COUPLED INPUT

$$V_{IN}\ (\text{COMMON MODE}) = \frac{R_{CM} \bullet V_{+IN}}{2 \bullet R_{CM} + 1.87k}$$

Figure 12. AC-Coupled Inputs

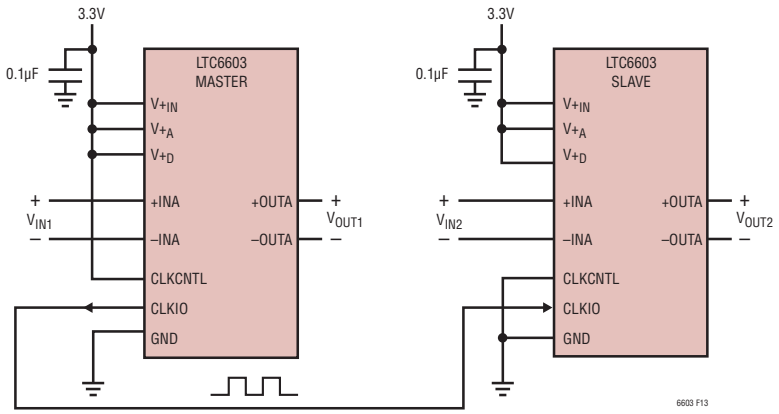


Figure 13. Two Devices in a Master/Slave Clocking Configuration

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results in four matched filter channels, all synchronized to the same clock. The master has its CLKCNTL pin pulled to $V+_D$, configuring its CLKIO pin as an output, while the slave has its CLKCNTL pin pulled to ground, configuring its CLKIO pin as an input. Note that in order to synchronize the two filters, the clock frequency must not be buffered. This requires that the filters be close together on the PC board. If the clock is buffered, the filters would have matching bandwidths, but would not be synchronized.

Output Drive

The filter outputs can drive 1k and/or 50pF loads connected to AC ground with a 0.5V to 2.5V signal (corresponding to a $4V_{P-P}$ differential signal). For differential loads (loads connected between +OUTA and –OUTA or +OUTB and –OUTB) the outputs can produce a $4V_{P-P}$ signal across 2k and/or 25pF. For smaller signal amplitudes, the outputs can drive correspondingly larger loads. For larger capacitive loads, an external 50Ω series resistor is recommended for each output.

Clock Feedthrough

Clock feedthrough is defined as the RMS value of the clock frequency and its harmonics that are present at the filter's output. The clock feedthrough is measured with +INA and –INA (or +INB, –INB) tied to V_{OCM} and depends on the PC board layout and the power supply decoupling. The clock feedthrough can be reduced with a simple RC post filter.

Decoupling Capacitors

The LTC6603 uses sampling techniques, therefore its performance is sensitive to supply noise. 0.1µF ceramic decoupling capacitors must be connected from $V+_A$ (Pin 2) and $V+_D$ (Pin 16) to ground with leads as short as possible. A ground plane should be used. Noisy signals should be isolated from the filter's input pins. In addition, a 0.1µF decoupling capacitor at Pin 20 is recommended since this pin receives clocked current injection.

Aliasing

Aliasing is an inherent phenomenon of sampled data filters. Significant aliasing only occurs when the frequency of the input signal approaches the sampling frequency or multiples of the sampling frequency. The ratio of the LTC6603 input sampling frequency to the clock frequency, f_{CLK}, is determined by the state of control bits LPF1 and LPF0. Table 6 shows the possible input sampling frequencies for a clock frequency of 80MHz. The input sampling frequency is proportional to the clock frequency. For example, if the clock frequency is lowered from 80MHz to 40MHz, the input sampling frequency will be lowered by half. Input signals with frequencies near the input sampling frequency will be aliased to the passband of the filter and appear at the output unattenuated.

Table 6. Input Sampling Frequency (f_{CLK} = 80MHz)

LPF1	LPF0	Input Sampling Frequency (MHz)
0	0	20
0	1	40
1	0	160
1	1	160

A simple LC anti-aliasing filter is recommended at the filter inputs to attenuate frequencies near the input sampling frequency that will be aliased to the passband. For example, if the clock frequency is set to 80MHz and the cutoff frequency of the filter is set to its maximum (LPF1 = 1), the lowest frequency that would be aliased to the passband would be $f_{CLK} – f_{CUTOFF}$, i.e., 160MHz – 2.5MHz = 157.5MHz. The LTC6603 filter inputs should be driven by a low impedance output (<100Ω).

Wideband Noise

The wideband noise of the filter is the RMS value of the device's output noise spectral density. The wideband noise is nearly independent of the value of the clock frequency and excludes the clock feedthrough. Most of the wideband noise is concentrated in the filter passband and cannot be removed with post filtering.

Power Supply Current

The power supply current depends on the state of the lowpass cutoff frequency controls (LPF1, LPF0) and the value of R_{BIAS}. When the LTC6603 is programmed for the middle cutoff frequency (LPF1 = 0, LPF0 = 1), the supply current is reduced by about 23% relative to the supply current for the higher bandwidth setting. Programming

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the LTC6603 for the lowest cutoff frequency (LPF1 = 0, LFP0 = 0) reduces the supply current by about 60%. Power supply current vs. cutoff frequency for various bandwidth settings is shown in the Typical Performance Characteristicst section. The LTC6603 can be programmed through the serial interface to enter into a low power shutdown mode. The power supply current during shutdown is less than 235µA.

Supply Current vs Noise Trade-Off

The passband of the LTC6603 is determined by the master clock frequency (which is set by R_{BIAS} when the internal oscillator is used), LPF1 and LPF0. The LTC6603 is optimized for use with R_{BIAS} having a value between 200k and 30.9k to set the internal oscillation frequency from 12.36MHz to 80MHz. The lowpass corner frequency is proportional to the clock frequency (internal or external).

To extend the filter's operational frequency range, the master clock is divided down before reaching the filter. LPF1 and LPF0 set the division ratio of the lowpass clock. Figure 14 shows the possible cutoff frequencies versus f_{CLK}, LPF1 and LPF0. Overlapping frequency ranges allow more than one possible choice of bandwidth settings for some cutoff frequencies. Figure 15 shows supply current as a function of the filter cutoff frequency, LPF1 and LPF0. Note that the higher bandwidth setting always gives the minimum supply current for a given cutoff frequency. The input referred integrated noise voltage for a passband gain of 24dB is shown in Table 7. Note that the noise is higher for the higher bandwidth settings. This creates a tradeoff between supply current and noise. For a given cutoff frequency, using the highest possible bandwidth setting gives the minimum supply current at the expense of higher noise.

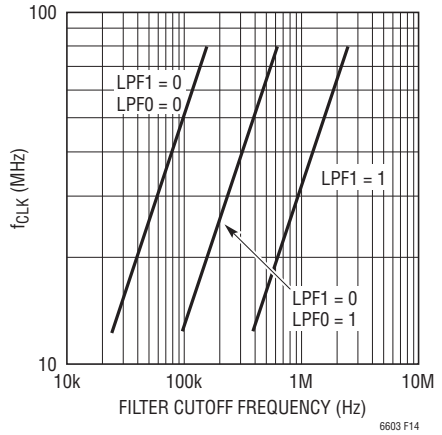


Figure 14. f_{CLK} vs Filter Cutoff Frequencies

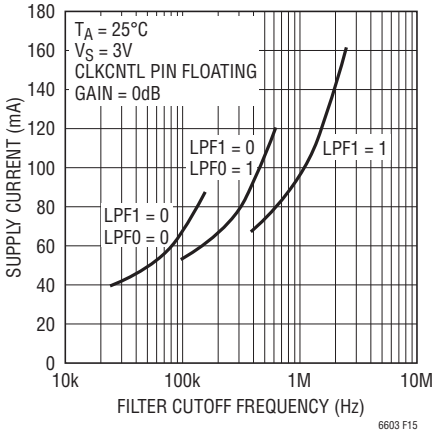


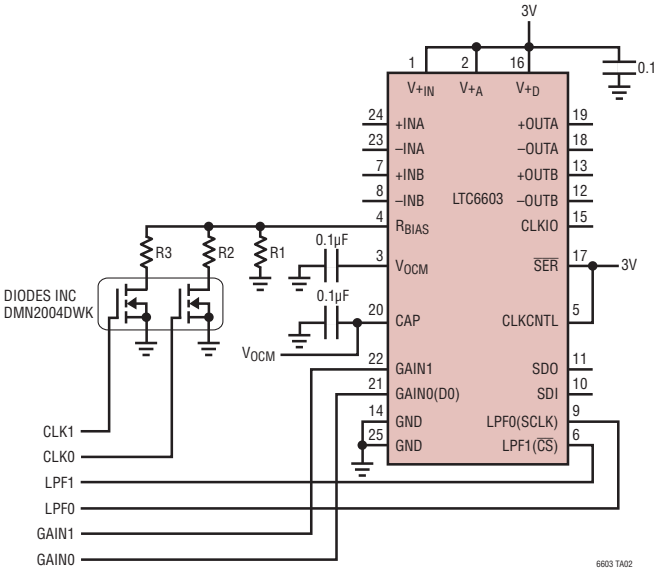
Figure 15. Supply Current vs Filter Cutoff Frequency

Table 7. Total Input Referred Integrated Noise Voltage (Passband Gain = 24dB)

LPF1	LPF0	NOISE VOLTAGE
0	0	–81dBm
0	1	–80dBm
1	X	–76dBm

TYPICAL APPLICATIONS

LTC6603 Parallel Clock Control



CLK1	CLK0		
0	0	R_{BIAS1}	f_{CLK1}
0	1	R_{BIAS2}	f_{CLK2}
1	0	R_{BIAS3}	f_{CLK3}
1	1	R_{BIAS4}	f_{CLK4}

$R_{BIAS1} > R_{BIAS2}$ OR R_{BIAS3}

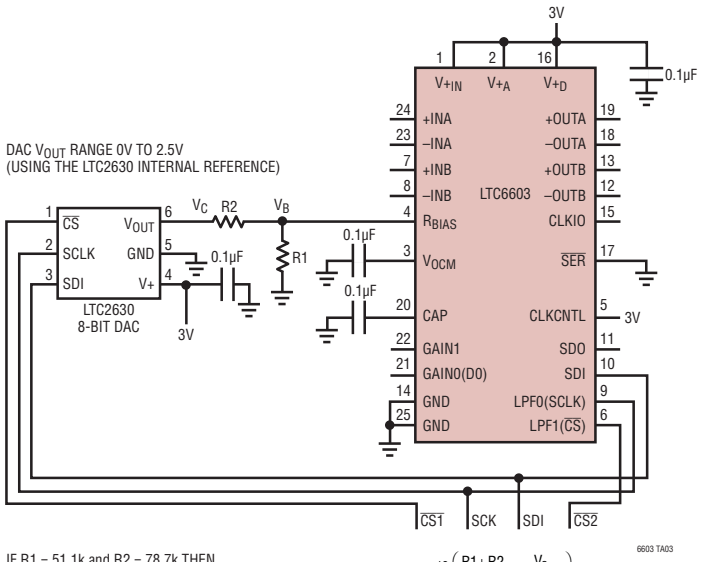
$$R_{BIAS} = \frac{2472}{f_{CLK}}$$

R_{BIAS} IN k
f_{CLK} in MHz

$$R1 = R_{BIAS1}\ R2 = \frac{R_{BIAS1} \bullet R_{BIAS2}}{R_{BIAS1} - R_{BIAS2}} \qquad R3 = \frac{R_{BIAS1} \bullet R_{BIAS3}}{R_{BIAS1} - R_{BIAS3}} \qquad R_{BIAS4} = \frac{R1 \bullet R2 \bullet R3}{R1 \bullet (R2 + R3) + R2 \bullet R3}$$

DESIGN PROCEDURE
1. CHOOSE f_{CLK1}, f_{CLK2} AND f_{CLK3}
2. CALCULATE R_{BIAS1}, R_{BIAS2} AND R_{BIAS3}
3. CALCULATE R2, R3 AND R_{BIAS4}

LTC6603 SPI Clock Control



IF R1 = 51.1k and R2 = 78.7k THEN
THE f_{CLK} RANGE IS 12.36MHz to 80MHz

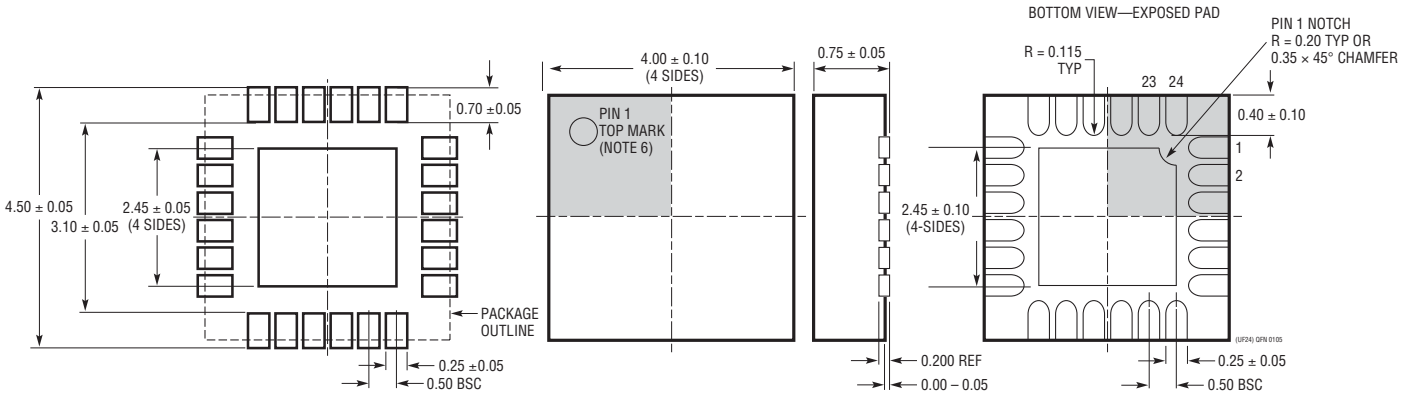
$$R1 = \frac{5.282 \bullet 10^{12}}{1.137 f_{CLKHI} + f_{CLKLO}}, \quad R2 = \frac{5.282 \bullet 10^{12}}{f_{CLKHI} - f_{CLKLO}}$$

$$f_{CLK} = 2.472 \bullet 10^{12} \left(\frac{R1+R2}{R1 \bullet R2} - \frac{V_C}{V_B \bullet R2} \right)$$

V_C RANGE 0V to 2.5V, V_B = 1.17V
IF V_C = 0V THEN $f_{CLK} = f_{CLKHI}$
IF V_C = 2.5V THEN $f_{CLK} = f_{CLKLO}$

PACKAGE DESCRIPTION

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE