14-Bit, 125/105/80Msps Ultralow Power 1.8V ADCs

FEATURES

- 73.4dB SNR
- 85dB SFDR
- Low Power: 127mW/106mW/89mW
- Single 1.8V Supply
- CMOS, DDR CMOS or DDR LVDS Outputs
- Selectable Input Ranges: $1V_{P-P}$ to $2V_{P-P}$
- 800MHz Full-Power Bandwidth S/H
- Optional Data Output Randomizer
- Optional Clock Duty Cycle Stabilizer
- Shutdown and Nap Modes
- Serial SPI Port for Configuration
- Pin Compatible 14-Bit and 12-Bit Versions
- 40-Pin (6mm × 6mm) QFN Package

APPLICATIONS

- Communications
- Cellular Base Stations
- Software Defined Radios
- Portable Medical Imaging
- Multi-Channel Data Acquisition
- Nondestructive Testing

DESCRIPTION

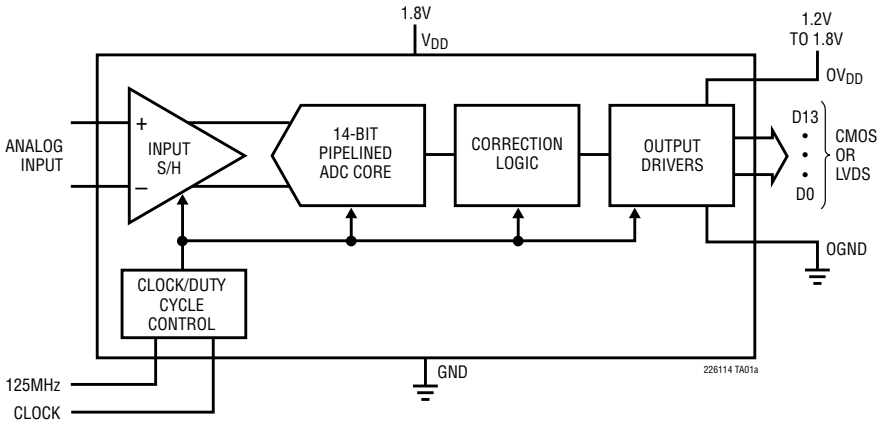
The LTC®2261-14/LTC2260-14/LTC2259-14 are sampling 14-bit A/D converters designed for digitizing high frequency, wide dynamic range signals. They are perfect for demanding communications applications with AC performance that includes 73.4dB SNR and 85dB spurious free dynamic range (SFDR). Ultralow jitter of $0.17ps_{RMS}$ allows undersampling of IF frequencies with excellent noise performance.

DC specs include ±1LSB INL (typical), ±0.3LSB DNL (typical) and no missing codes over temperature. The transition noise is a low $1.2LSB_{RMS}$.

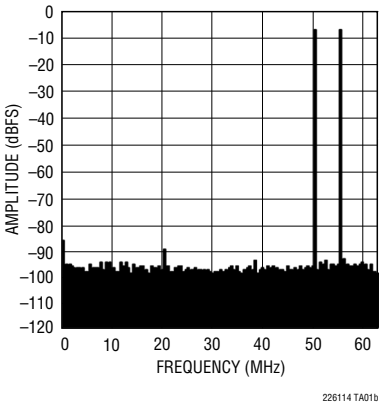
The digital outputs can be either full-rate CMOS, double-data rate CMOS, or double-data rate LVDS. A separate output power supply allows the CMOS output swing to range from 1.2V to 1.8V.

The ENC+ and ENC– inputs may be driven differentially or single ended with a sine wave, PECL, LVDS, TTL or CMOS inputs. An optional clock duty cycle stabilizer allows high performance at full speed for a wide range of clock duty cycles.

TYPICAL APPLICATION



2-Tone FFT, f_{IN} = 70MHz and 75MHz

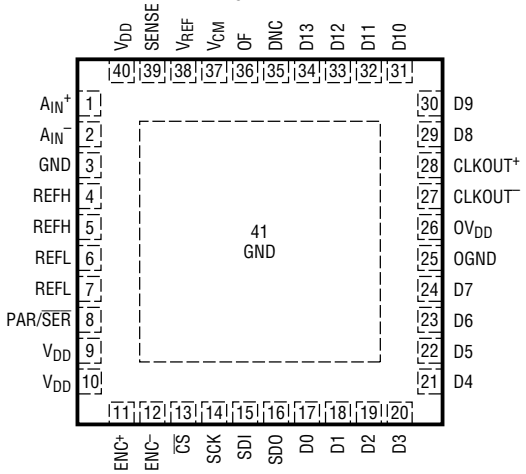


ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltages (V_{DD}, OV_{DD}) ..... –0.3V to 2V
Analog Input Voltage (A_{IN}^+, A_{IN}^-, PAR/$\overline{SER}$, SENSE) (Note 3) ..... –0.3V to (V_{DD} + 0.2V)
Digital Input Voltage (ENC+, ENC–, $\overline{CS}$, SDI, SCK) (Note 4) ..... –0.3V to 3.9V
SDO (Note 4) ..... –0.3V to 3.9V
Digital Output Voltage ..... –0.3V to (OV_{DD} + 0.3V)
Operating Temperature Range:
LTC2261C, LTC2260C, LTC2259C ..... 0°C to 70°C
LTC2261I, LTC2260I, LTC2259I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATIONS

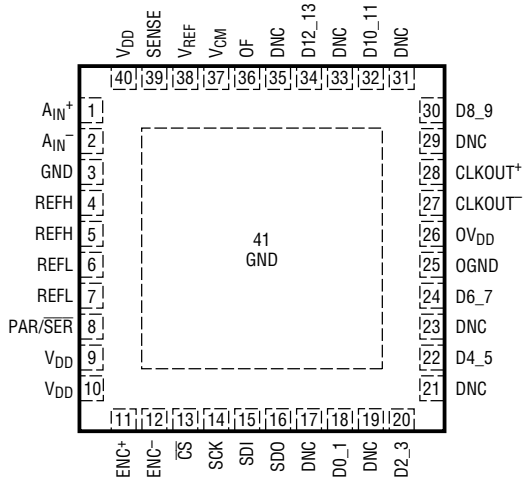
FULL-RATE CMOS OUTPUT MODE
TOP VIEW



UJ PACKAGE
40-LEAD (6mm × 6mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 32°C/W
EXPOSED PAD (PIN 41) IS GND, MUST BE SOLDERED TO PCB

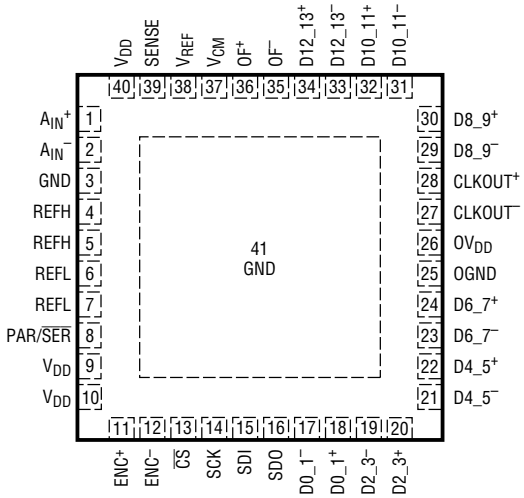
DOUBLE DATA RATE CMOS OUTPUT MODE
TOP VIEW



UJ PACKAGE
40-LEAD (6mm × 6mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 32°C/W
EXPOSED PAD (PIN 41) IS GND, MUST BE SOLDERED TO PCB

DOUBLE DATA RATE LVDS OUTPUT MODE
TOP VIEW



UJ PACKAGE
40-LEAD (6mm × 6mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 32°C/W
EXPOSED PAD (PIN 41) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2261CUJ-14#PBF	LTC2261CUJ-14#TRPBF	LTC2261UJ-14	40-Lead (6mm × 6mm) Plastic QFN	0°C to 70°C
LTC2261IUJ-14#PBF	LTC2261IUJ-14#TRPBF	LTC2261UJ-14	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 85°C
LTC2260CUJ-14#PBF	LTC2260CUJ-14#TRPBF	LTC2260UJ-14	40-Lead (6mm × 6mm) Plastic QFN	0°C to 70°C
LTC2260IUJ-14#PBF	LTC2260IUJ-14#TRPBF	LTC2260UJ-14	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 85°C
LTC2259CUJ-14#PBF	LTC2259CUJ-14#TRPBF	LTC2259UJ-14	40-Lead (6mm × 6mm) Plastic QFN	0°C to 70°C
LTC2259IUJ-14#PBF	LTC2259IUJ-14#TRPBF	LTC2259UJ-14	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

PARAMETER	CONDITIONS		LTC2261-14 MIN	LTC2261-14 TYP	LTC2261-14 MAX	LTC2260-14 MIN	LTC2260-14 TYP	LTC2260-14 MAX	LTC2259-14 MIN	LTC2259-14 TYP	LTC2259-14 MAX	UNITS
Resolution (No Missing Codes)		●	14			14			14			Bits
Integral Linearity Error	Differential Analog Input (Note 6)	●	–3.75	±1	3.75	–3.75	±1	3.75	–3.5	±1	3.5	LSB
Differential Linearity Error	Differential Analog Input	●	–0.9	±0.3	0.9	–0.9	±0.3	0.9	–0.9	±0.3	0.9	LSB
Offset Error	(Note 7)	●	–9	±1.5	9	–9	±1.5	9	–9	±1.5	9	mV
Gain Error	Internal Reference External Reference	 ●	 –1.5	±1.5 ±0.4	 1.5	 –1.5	±1.5 ±0.4	 1.5	 –1.5	±1.5 ±0.4	 1.5	%FS %FS
Offset Drift				±20			±20			±20		µV/°C
Full-Scale Drift	Internal Reference External Reference			±30 ±10			±30 ±10			±30 ±10		ppm/°C ppm/°C
Transition Noise	External Reference			1.2			1.2			1.2		LSB_{RMS}

ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Analog Input Range ($A_{IN}^+ - A_{IN}^-$)	1.7V < V_{DD} < 1.9V	●		1 to 2		V_{P-P}
$V_{IN(CM)}$	Analog Input Common Mode ($A_{IN}^+ + A_{IN}^-$)/2	Differential Analog Input (Note 8)	●	V_{CM} – 100mV	V_{CM}	V_{CM} + 100mV	V
V_{SENSE}	External Voltage Reference Applied to SENSE	External Reference Mode	●	0.625	1.250	1.300	V
I_{INCM}	Analog Input Common Mode Current	Per Pin, 125Msps Per Pin, 105Msps Per Pin, 80Msps			155 130 100		µA µA µA
I_{IN1}	Analog Input Leakage Current	0 < A_{IN}^+, A_{IN}^- < V_{DD}, No Encode	●	–1		1	µA
I_{IN2}	PAR/$\overline{SER}$ Input Leakage Current	0 < PAR/$\overline{SER}$ < V_{DD}	●	–3		3	µA
I_{IN3}	SENSE Input Leakage Current	0.625 < SENSE < 1.3V	●	–6		6	µA
t_{AP}	Sample-and-Hold Acquisition Delay Time				0		ns
t_{JITTER}	Sample-and-Hold Acquisition Delay Jitter				0.17		ps_{RMS}
CMRR	Analog Input Common Mode Rejection Ratio				80		dB
BW-3B	Full-Power Bandwidth	Figure 6 Test Circuit			800		MHz

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. A_{IN} = –1dBFS. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC2261-14 MIN	LTC2261-14 TYP	LTC2261-14 MAX	LTC2260-14 MIN	LTC2260-14 TYP	LTC2260-14 MAX	LTC2259-14 MIN	LTC2259-14 TYP	LTC2259-14 MAX	UNITS
SNR	Signal-to-Noise Ratio	5MHz Input			73.4			73.4			73.1		dB
		70MHz Input	●	71.3	73.2		71.3	73.2		70.9	72.9		dB
		140MHz Input			72.7			72.7			72.4		dB
SFDR	Spurious Free Dynamic Range 2nd or 3rd Harmonic	5MHz Input			88			88			88		dB
		70MHz Input	●	76	85		76	85		79	85		dB
		140MHz Input			82			82			82		dB
	Spurious Free Dynamic Range 4th Harmonic or Higher	5MHz Input			90			90			90		dB
		70MHz Input	●	85	90		83	90		85	90		dB
		140MHz Input			90			90			90		dB
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	5MHz Input			73			73			72.9		dB
		70MHz Input	●	70.2	72.6		70.2	72.6		70.4	72.6		dB
		140MHz Input			72			72			72		dB

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CM} Output Voltage	I_{OUT} = 0		0.5 • V_{DD} – 25mV	0.5 • V_{DD}	0.5 • V_{DD} + 25mV	V
V_{CM} Output Temperature Drift				±25		ppm/°C
V_{CM} Output Resistance	–600µA < I_{OUT} < 1mA			4		Ω
V_{REF} Output Voltage	I_{OUT} = 0		1.225	1.250	1.275	V
V_{REF} Output Temperature Drift				±25		ppm/°C
V_{REF} Output Resistance	–400µA < I_{OUT} < 1mA			7		Ω
V_{REF} Line Regulation	1.7V < V_{DD} < 1.9V			0.6		mV/V

DIGITAL INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ENCODE INPUTS (ENC⁺, ENC⁻)							
Differential Encode Mode (ENC⁻ Not Tied to GND)							
V_{ID}	Differential Input Voltage	(Note 8)	●	0.2			V
V_{ICM}	Common Mode Input Voltage	Internally Set Externally Set (Note 8)	 ●	 1.1	1.2	 1.6	V V
V_{IN}	Input Voltage Range	ENC⁺, ENC⁻ to GND	●	0.2		3.6	V
R_{IN}	Input Resistance	(See Figure 10)			10		kΩ
C_{IN}	Input Capacitance	(Note 8)			3.5		pF
Single-Ended Encode Mode (ENC⁻ Tied to GND)							
V_{IH}	High Level Input Voltage	V_{DD} = 1.8V	●	1.2			V
V_{IL}	Low Level Input Voltage	V_{DD} = 1.8V	●			0.6	V
V_{IN}	Input Voltage Range	ENC⁺ to GND	●	0		3.6	V
R_{IN}	Input Resistance	(See Figure 11)			30		kΩ
C_{IN}	Input Capacitance	(Note 8)			3.5		pF
DIGITAL INPUTS ($\overline{CS}$, SDI, SCK)							
V_{IH}	High Level Input Voltage	V_{DD} = 1.8V	●	1.3			V
V_{IL}	Low Level Input Voltage	V_{DD} = 1.8V	●			0.6	V
I_{IN}	Input Current	V_{IN} = 0V to 3.6V	●	–10		10	µA
C_{IN}	Input Capacitance	(Note 8)			3		pF
SDO OUTPUT (Open-Drain Output. Requires 2k Pull-Up Resistor if SDO is Used)							
R_{OL}	Logic Low Output Resistance to GND	V_{DD} = 1.8V, SDO = 0V			200		Ω
I_{OH}	Logic High Output Leakage Current	SDO = 0V to 3.6V	●	–10		10	µA
C_{OUT}	Output Capacitance	(Note 8)			4		pF
DIGITAL DATA OUTPUTS (CMOS MODES: FULL DATA RATE AND DOUBLE-DATA RATE)							
OV_{DD} = 1.8V							
V_{OH}	High Level Output Voltage	I_O = –500µA	●	1.750	1.790		V
V_{OL}	Low Level Output Voltage	I_O = 500µA	●		0.010	0.050	V
OV_{DD} = 1.5V							
V_{OH}	High Level Output Voltage	I_O = –500µA			1.488		V
V_{OL}	Low Level Output Voltage	I_O = 500µA			0.010		V
OV_{DD} = 1.2V							
V_{OH}	High Level Output Voltage	I_O = –500µA			1.185		V
V_{OL}	Low Level Output Voltage	I_O = 500µA			0.010		V
DIGITAL DATA OUTPUTS (LVDS MODE)							
V_{OD}	Differential Output Voltage	100Ω Differential Load, 3.5mA Mode 100Ω Differential Load, 1.75mA Mode	●	247	350 175	454	mV mV
V_{OS}	Common Mode Output Voltage	100Ω Differential Load, 3.5mA Mode 100Ω Differential Load, 1.75mA Mode	●	1.125	1.250 1.250	1.375	V V
R_{TERM}	On-Chip Termination Resistance	Termination Enabled, OV_{DD} = 1.8V			100		Ω

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 9)

SYMBOL	PARAMETER	CONDITIONS		LTC2261-14 MIN	LTC2261-14 TYP	LTC2261-14 MAX	LTC2260-14 MIN	LTC2260-14 TYP	LTC2260-14 MAX	LTC2259-14 MIN	LTC2259-14 TYP	LTC2259-14 MAX	UNITS
CMOS Output Modes: Full Data Rate and Double-Data Rate													
V_{DD}	Analog Supply Voltage	(Note 10)	●	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
OV_{DD}	Output Supply Voltage	(Note 10)	●	1.1		1.9	1.1		1.9	1.1		1.9	V
I_{VDD}	Analog Supply Current	DC Input Sine Wave Input	● ●		70.5 71.8	83.2		58.6 59.8	69.1		49.2 50.2	58.1	mA mA
I_{OVDD}	Digital Supply Current	Sine Wave Input, OV_{DD}=1.2V			3.9			3.3			2.5		mA
P_{DISS}	Power Dissipation	DC Input Sine Wave Input, OV_{DD}=1.2V	● ●		127 134	150		106 112	125		89 93	105	mW mW
LVDS Output Mode													
V_{DD}	Analog Supply Voltage	(Note 10)	●	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
OV_{DD}	Output Supply Voltage	(Note 10)	●	1.7		1.9	1.7		1.9	1.7		1.9	V
I_{VDD}	Analog Supply Current	Sine Wave Input	●		75.4	89		63.4	74.8		53.8	63.5	mA
I_{OVDD}	Digital Supply Current ($0V_{DD}$ = 1.8V)	Sine Input, 1.75mA Mode Sine Input, 3.5mA Mode	● ●		20.7 40.5	26 47.8		20.7 40.5	26 47.8		20.7 40.5	26 47.8	mA mA
P_{DISS}	Power Dissipation	Sine Input, 1.75mA Mode Sine Input, 3.5mA Mode	● ●		173 209	207 246		151 187	182 221		134 170	161 201	mW mW
All Output Modes													
P_{SLEEP}	Sleep Mode Power				0.5			0.5			0.5		mW
P_{NAP}	Nap Mode Power				9			9			9		mW
$P_{DIFFCLK}$	Power Increase with Differential Encode Mode Enabled (No increase for Nap or Sleep Modes)				10			10			10		mW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		LTC2261-14 MIN	LTC2261-14 TYP	LTC2261-14 MAX	LTC2260-14 MIN	LTC2260-14 TYP	LTC2260-14 MAX	LTC2259-14 MIN	LTC2259-14 TYP	LTC2259-14 MAX	UNITS
f_S	Sampling Frequency	(Note 10)	●	1		125	1		105	1		80	MHz
t_L	ENC Low Time (Note 8)	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	3.8 2.0	4 4	500 500	4.52 2.00	4.76 4.76	500 500	5.93 2.00	6.25 6.25	500 500	ns ns
t_H	ENC High Time (Note 8)	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	3.8 2.0	4 4	500 500	4.52 2.00	4.76 4.76	500 500	5.93 2.00	6.25 6.25	500 500	ns ns
t_{AP}	Sample-and-Hold Acquisition Delay Time				0			0			0		ns

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Data Outputs (CMOS Modes: Full Data Rate and Double-Data Rate)							
t_D	ENC to Data Delay	C_L = 5pF (Note 8)	●	1.1	1.7	3.1	ns
t_C	ENC to CLKOUT Delay	C_L = 5pF (Note 8)	●	1	1.4	2.6	ns
t_{SKEW}	DATA to CLKOUT Skew	$t_D - t_C$ (Note 8)	●	0	0.3	0.6	ns
	Pipeline Latency	Full Data Rate Mode Double-Data Rate Mode			5.0 5.5		Cycles Cycles

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Digital Data Outputs (LVDS Mode)							
t_D	ENC to Data Delay	C_L = 5pF (Note 8)	●	1.1	1.8	3.2	ns
t_C	ENC to CLKOUT Delay	C_L = 5pF (Note 8)	●	1	1.5	2.7	ns
t_{SKEW}	DATA to CLKOUT Skew	$t_D - t_C$ (Note 8)	●	0	0.3	0.6	ns
	Pipeline Latency				5.5		Cycles
SPI Port Timing (Note 8)							
t_{SCK}	SCK Period	Write Mode Readback Mode, C_{SDO} = 20pF, R_{PULLUP} = 2k	● ●	40 250			ns ns
t_S	$\overline{CS}$ to SCK Setup Time		●	5			ns
t_H	SCK to $\overline{CS}$ Setup Time		●	5			ns
t_{DS}	SDI Setup Time		●	5			ns
t_{DH}	SDI Hold Time		●	5			ns
t_{DO}	SCK Falling to SDO Valid	Readback Mode, C_{SDO} = 20pF, R_{PULLUP} = 2k	●			125	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND with GND and OGND shorted (unless otherwise noted).

Note 3: When these pin voltages are taken below GND or above V_{DD}, they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND or above V_{DD} without latchup.

Note 4: When these pin voltages are taken below GND they will be clamped by internal diodes. When these pin voltages are taken above V_{DD} they will not be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND without latchup.

Note 5: V_{DD} = OV_{DD} = 1.8V, f_{SAMPLE} = 125MHz (LTC2261), 105MHz (LTC2260), or 80MHz (LTC2259), LVDS outputs with internal termination disabled, differential ENC^+/ENC^- = $2V_{P-P}$ sine wave, input range = $2V_{P-P}$ with differential drive, unless otherwise noted.

Note 6: Integral nonlinearity is defined as the deviation of a code from a best fit straight line to the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: Offset error is the offset voltage measured from –0.5 LSB when the output code flickers between 00 0000 0000 0000 and 11 1111 1111 1111 in 2's complement output mode.

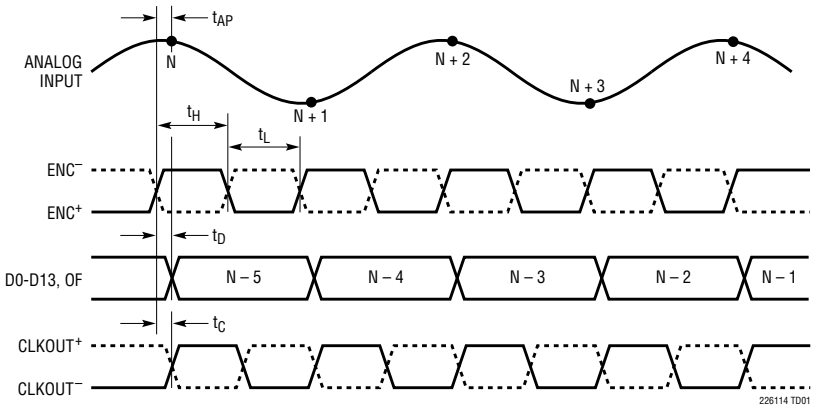
Note 8: Guaranteed by design, not subject to test.

Note 9: V_{DD} = 1.8V, f_{SAMPLE} = 125MHz (LTC2261), 105MHz (LTC2260), or 80MHz (LTC2259), ENC^+ = single-ended 1.8V square wave, ENC^- = 0V, input range = $2V_{P-P}$ with differential drive, 5pF load on each digital output unless otherwise noted.

Note 10: Recommended operating conditions.

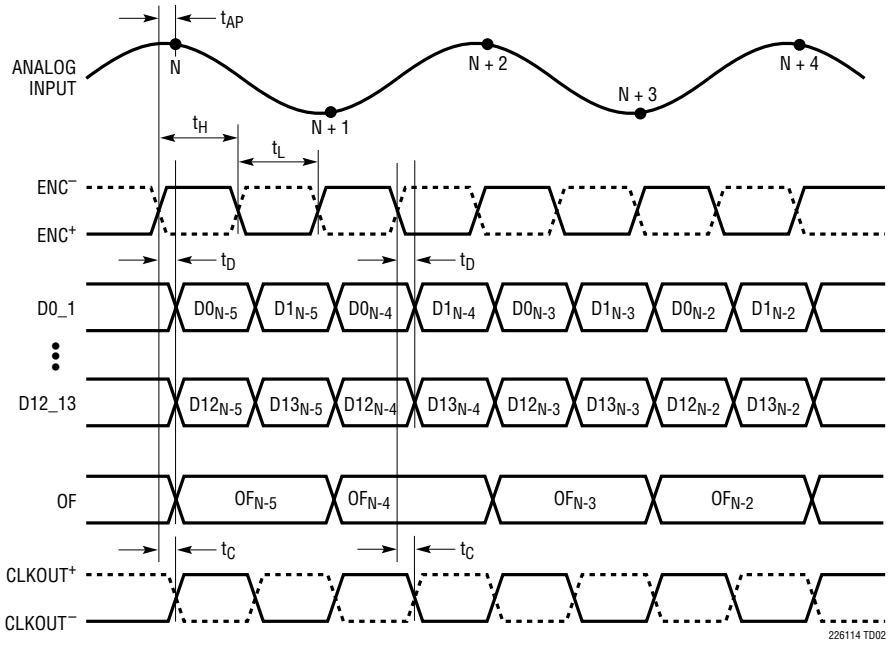
TIMING DIAGRAMS

Full-Rate CMOS Output Mode Timing
All Outputs Are Single Ended and Have CMOS Levels

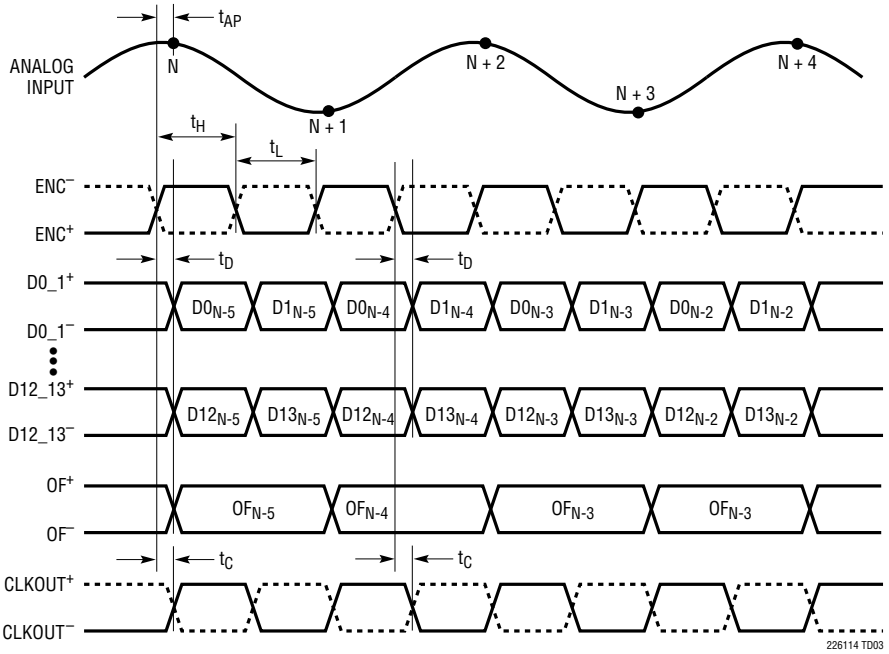


TIMING DIAGRAMS

Double-Data Rate CMOS Output Mode Timing
All Outputs Are Single Ended and Have CMOS Levels

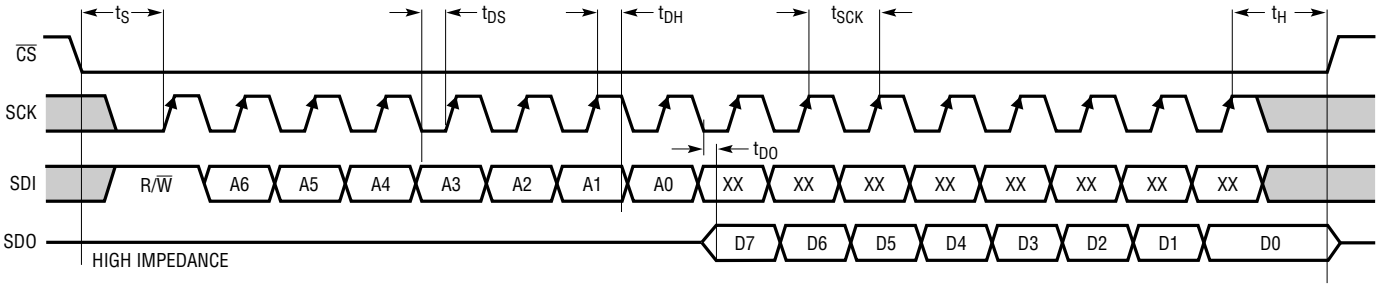


Double-Data Rate LVDS Output Mode Timing
All Outputs Are Differential and Have LVDS Levels

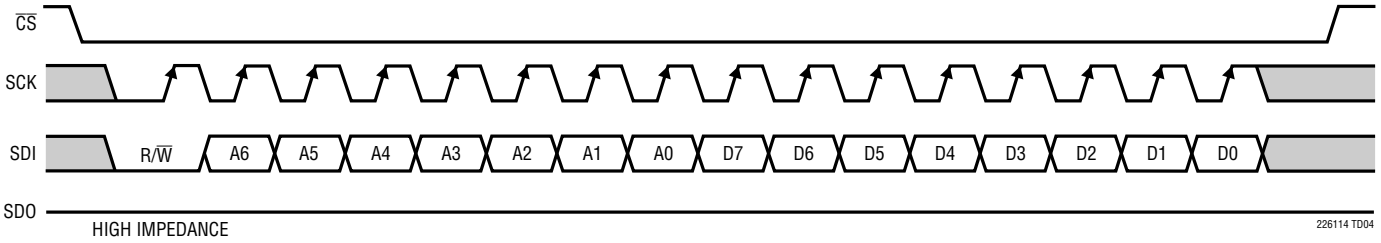


TIMING DIAGRAMS

SPI Port Timing (Readback Mode)



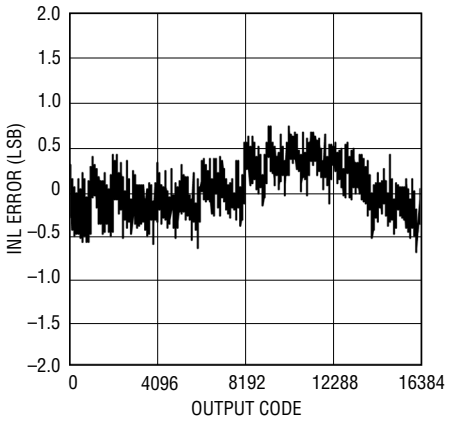
SPI Port Timing (Write Mode)



226114 TD04

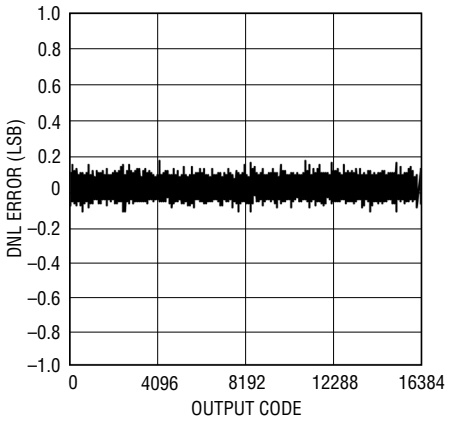
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2261-14: Integral Non-Linearity (INL)



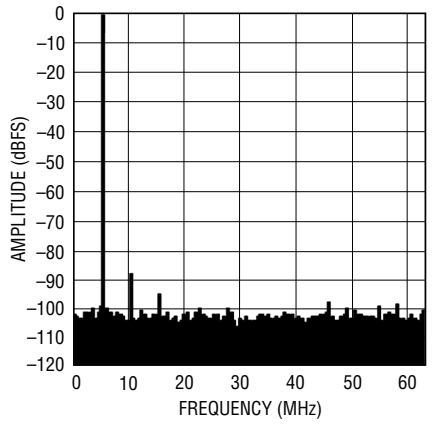
226114 G01

LTC2261-14: Differential Non-Linearity (DNL)



226114 G02

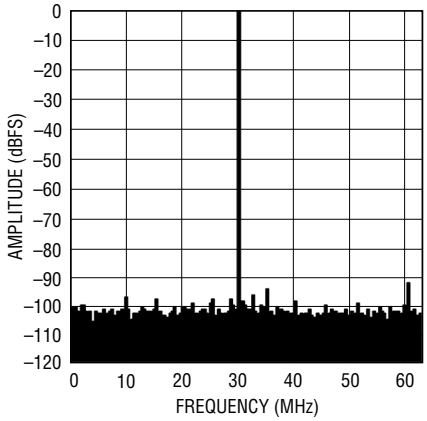
LTC2261-14: 8k Point FFT, f_{IN} = 5MHz –1dBFS, 125Msps



226114 G03

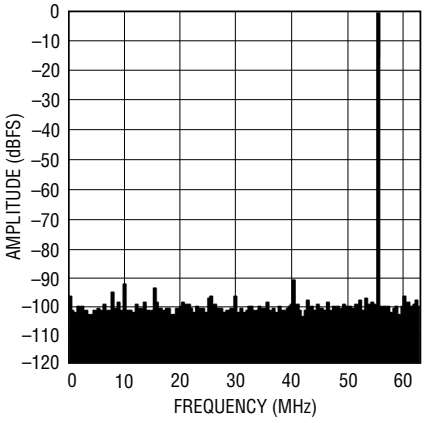
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2261-14: 8k Point FFT, f_{IN} = 30MHz –1dBFS, 125Msps



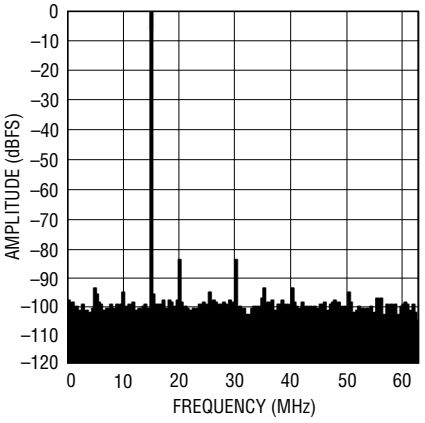
226114 G04

LTC2261-14: 8k Point FFT, f_{IN} = 70MHz –1dBFS, 125Msps



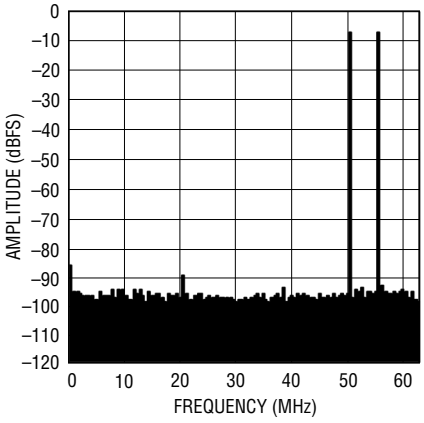
226114 G05

LTC2261-14: 8k Point FFT, f_{IN} = 140MHz –1dBFS, 125Msps



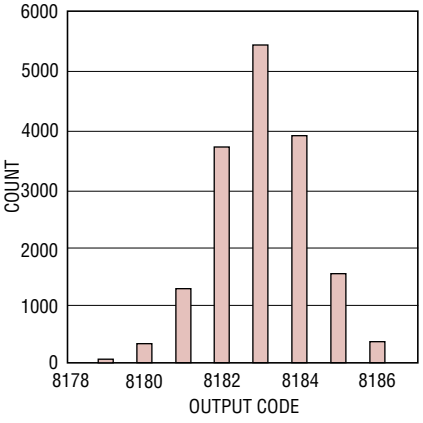
226114 G06

LTC2261-14: 8k Point 2-Tone FFT, f_{IN} = 70MHz, 75MHz, –1dBFS, 125Msps



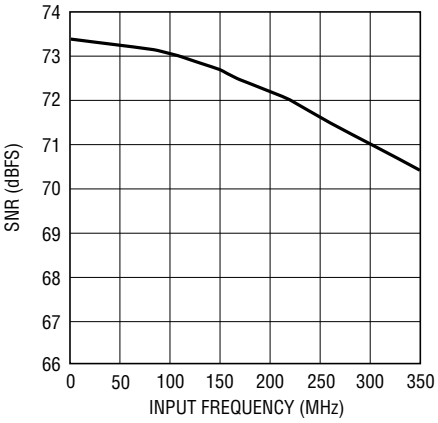
226114 G07

LTC2261-14: Shorted Input Histogram



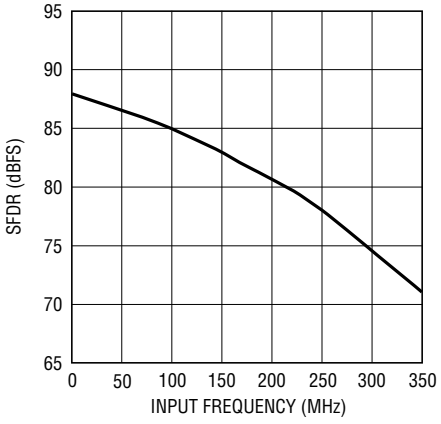
226114 G08

LTC2261-14: SNR vs Input Frequency, –1dB, 2V Range, 125Msps



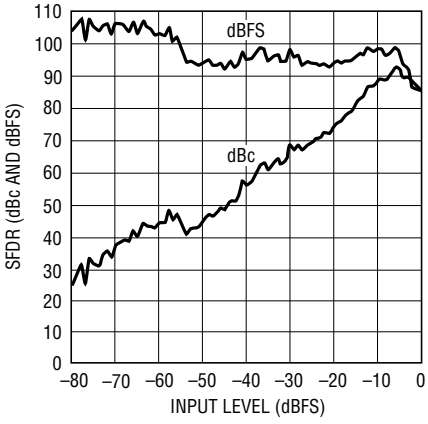
226114 G09

LTC2261-14: SFDR vs Input Frequency, –1dB, 2V Range, 125Msps



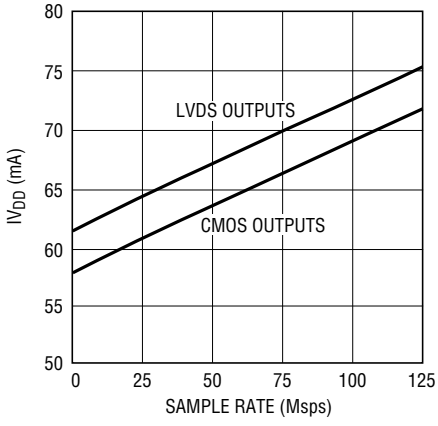
226114 G10

LTC2261-14: SFDR vs Input Level, f_{IN} = 70MHz, 2V Range, 125Msps



226114 G12

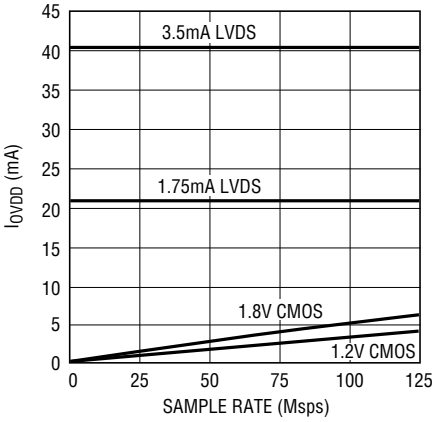
LTC2261-14: I_{VDD} vs Sample Rate, 5MHz Sine Wave Input, –1dB



226114 G13

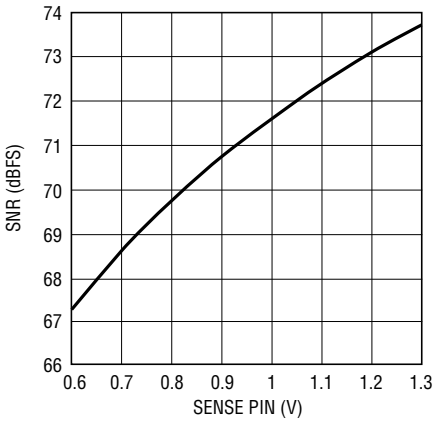
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2261-14: I_{OVDD} vs Sample Rate, 5MHz Sine Wave Input, –1dB, 5pF on Each Data Output



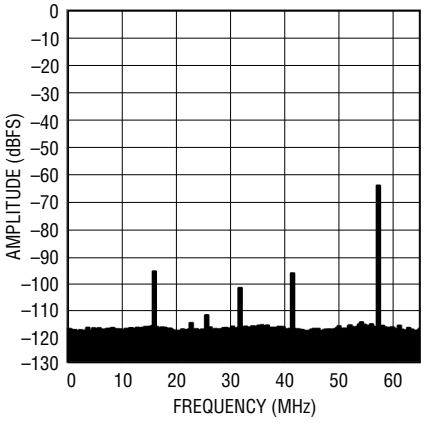
226114 G14

LTC2261-14: SNR vs SENSE, f_{IN} = 5MHz, –1dB



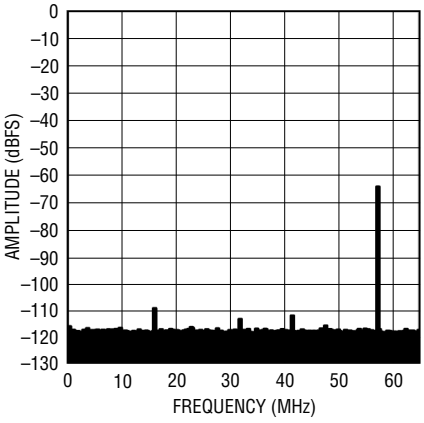
226114 G15

LTC2261-14: 128k Point Averaged FFT, f_{IN} = 70MHz, –65dBFS, 125Msps, RAND OFF, ABP OFF



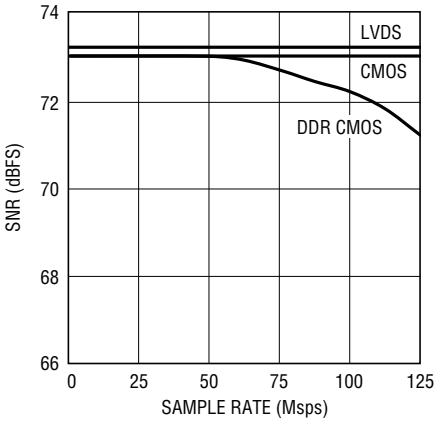
226114 G16

LTC2261-14: 128k Point Averaged FFT, f_{IN} = 70MHz, –65dBFS, 125Msps, RAND ON, ABP ON



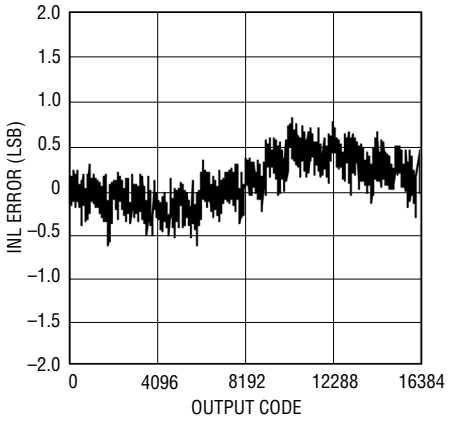
226114 G17

LTC2261-14: SNR vs Sample Rate and Digital Output Mode, 30MHz Sine Wave Input, –1dB



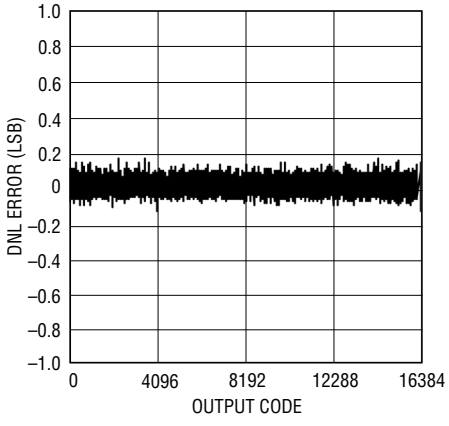
226114 G18

LTC2260-14: Integral Non-Linearity (INL)



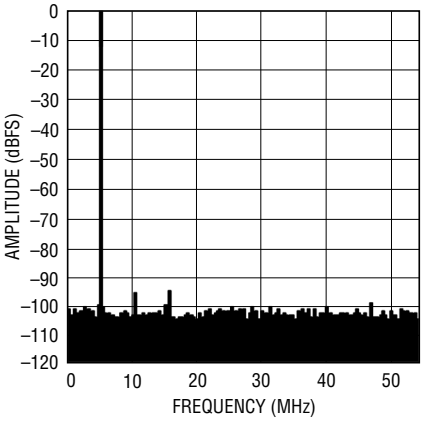
226114 G21

LTC2260-14: Differential Non-Linearity (DNL)



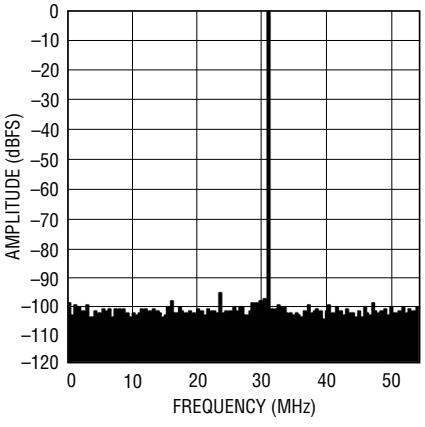
226114 G22

LTC2260-14: 8k Point FFT, f_{IN} = 5MHz –1dBFS, 105Msps



226114 G23

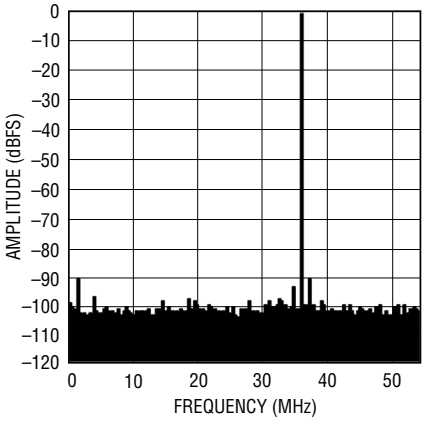
LTC2260-14: 8k Point FFT, f_{IN} = 30MHz –1dBFS, 105Msps



226114 G24

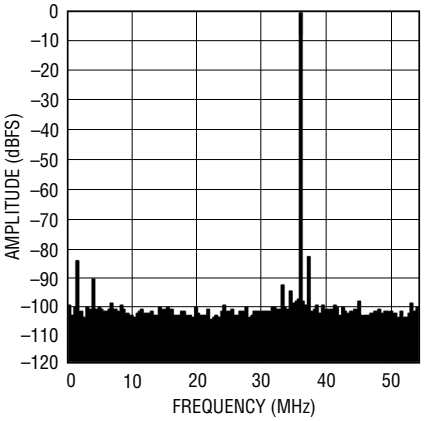
TYPICAL PERFORMANCE CHARACTERISTICS

LTC2260-14: 8k Point FFT, f_{IN} = 70MHz –1dBFS, 105Msps



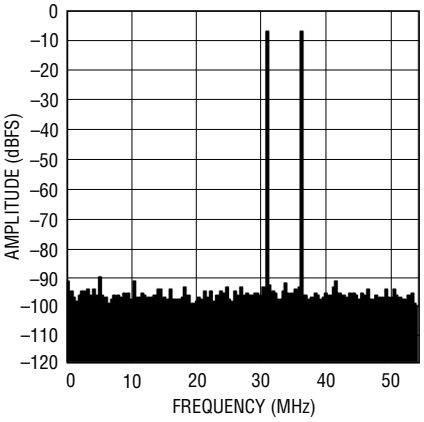
226114 G25

LTC2260-14: 8k Point FFT, f_{IN} = 140MHz –1dBFS, 105Msps



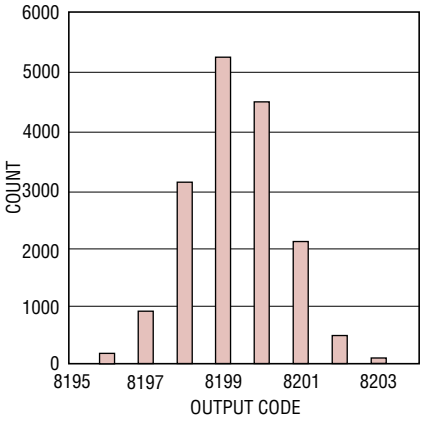
226114 G26

LTC2260-14: 8k Point 2-Tone FFT, f_{IN} = 70MHz, 75MHz, –1dBFS, 105Msps



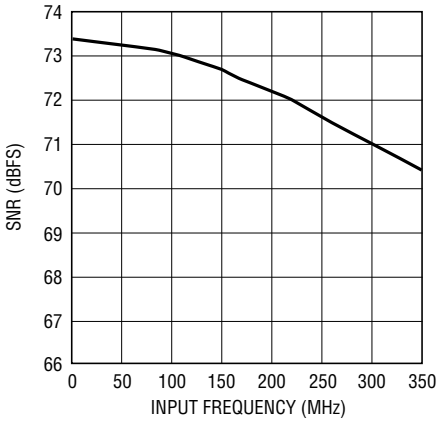
226114 G27

LTC2260-14: Shorted Input Histogram



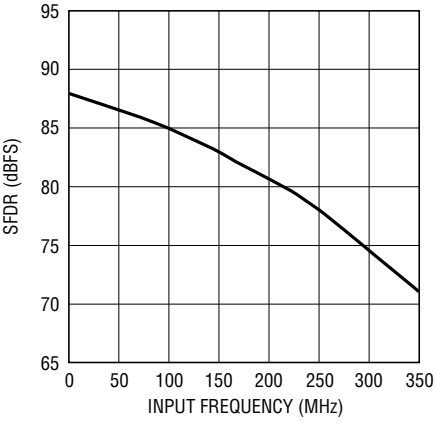
226114 G28

LTC2260-14: SNR vs Input Frequency, –1dB, 2V Range, 105Msps



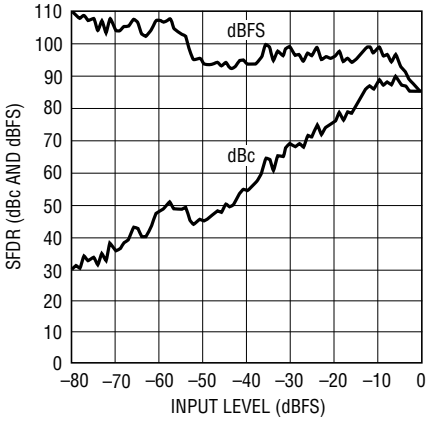
226114 G29

LTC2260-14: SFDR vs Input Frequency, –1dB, 2V Range, 105Msps



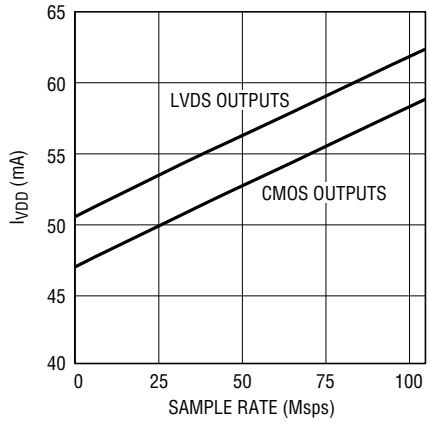
226114 G30

LTC2260-14: SFDR vs Input Level, f_{IN} = 70MHz, 2V Range, 105Msps



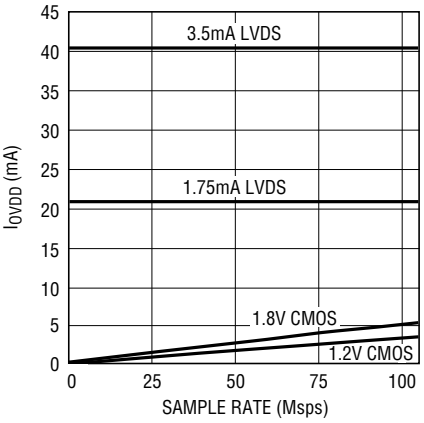
226114 G32

LTC2260-14: I_{VDD} vs Sample Rate, 5MHz Sine Wave Input, –1dB



226114 G33

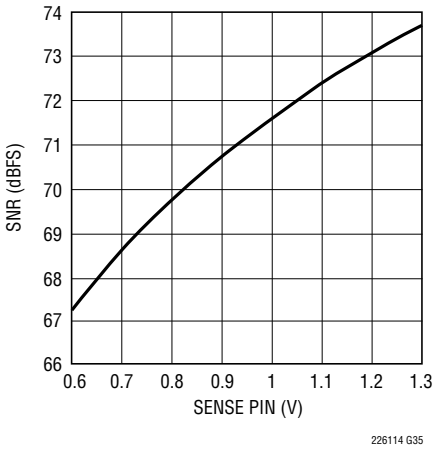
LTC2260-14: I_{OVDD} vs Sample Rate, 5MHz Sine Wave Input, –1dB, 5pF on Each Data Output



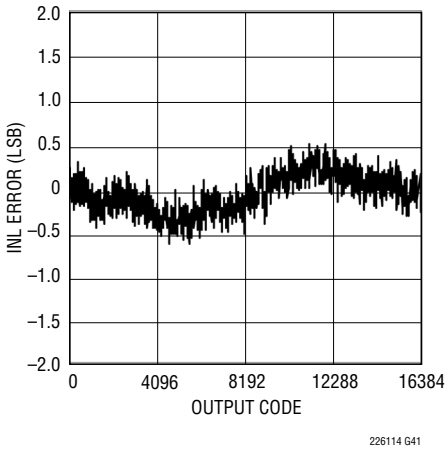
226114 G34

TYPICAL PERFORMANCE CHARACTERISTICS

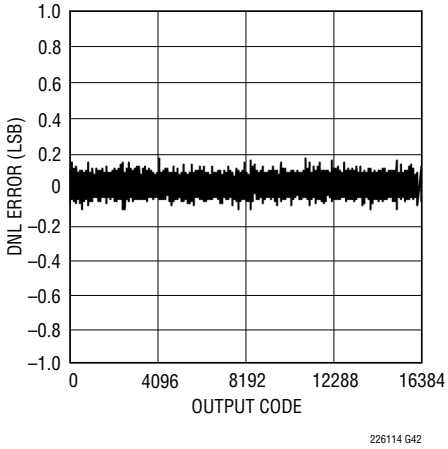
LTC2260-14: SNR vs SENSE, f_{IN} = 5MHz, –1dB



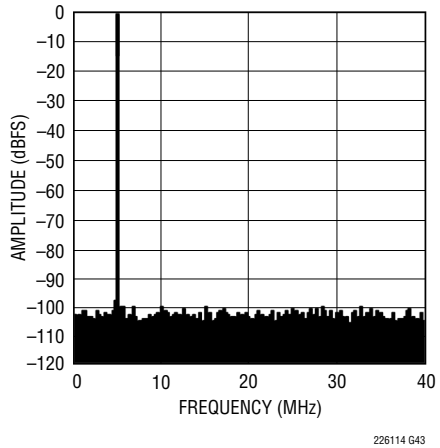
LTC2259-14: Integral Non-Linearity (INL)



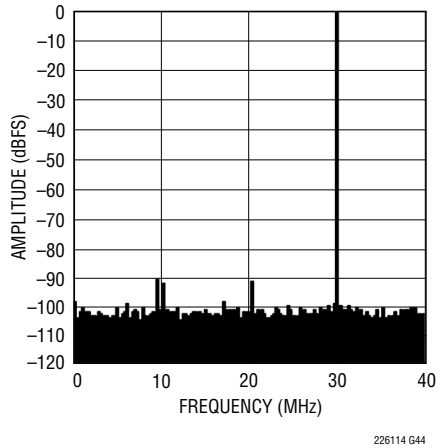
LTC2259-14: Differential Non-Linearity (DNL)



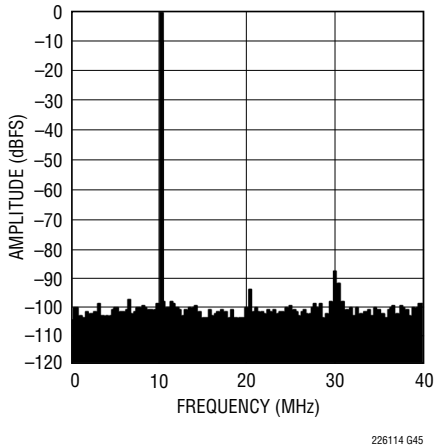
LTC2259-14: 8k Point FFT, f_{IN} = 5MHz –1dBFS, 80Msps



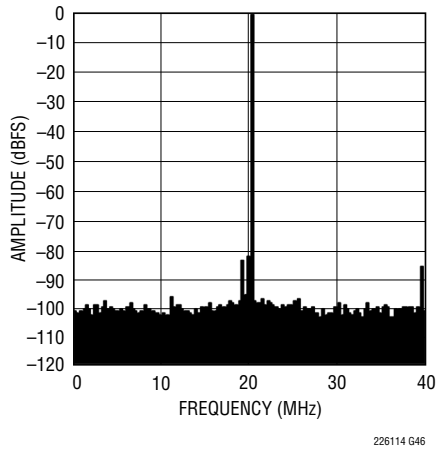
LTC2259-14: 8k Point FFT, f_{IN} = 30MHz –1dBFS, 80Msps



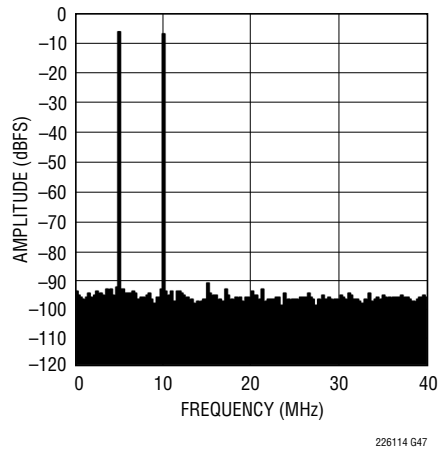
LTC2259-14: 8k Point FFT, f_{IN} = 70MHz –1dBFS, 80Msps



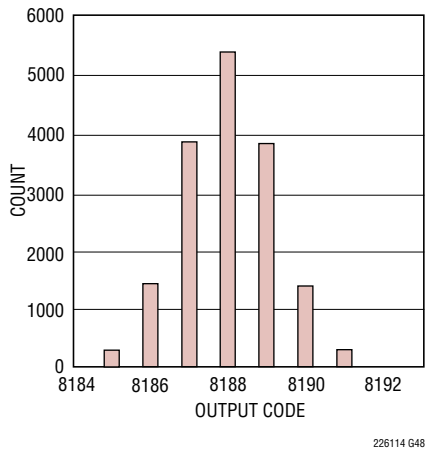
LTC2259-14: 8k Point FFT, f_{IN} = 140MHz –1dBFS, 80Msps



LTC2259-14: 8k Point 2-Tone FFT, f_{IN} = 70MHz, 75MHz, –1dBFS, 80Msps

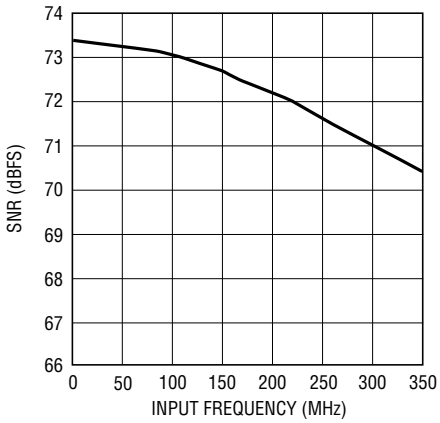


LTC2259-14: Shorted Input Histogram

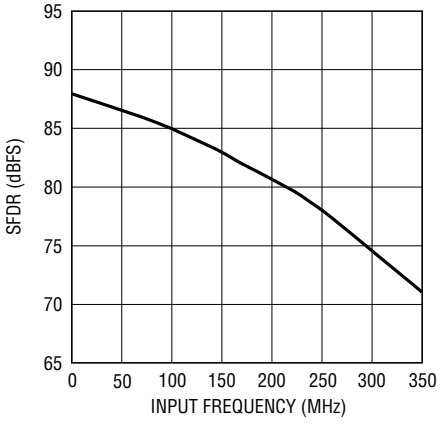


TYPICAL PERFORMANCE CHARACTERISTICS

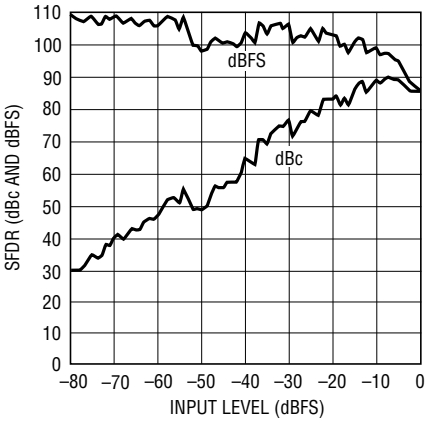
LTC2259-14: SNR vs Input Frequency, –1dB, 2V Range, 80Msps



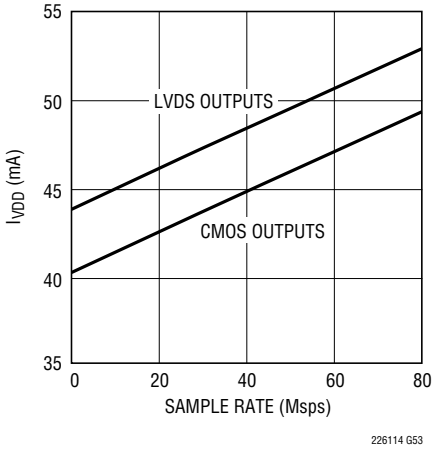
LTC2259-14: SFDR vs Input Frequency, –1dB, 2V Range, 80Msps



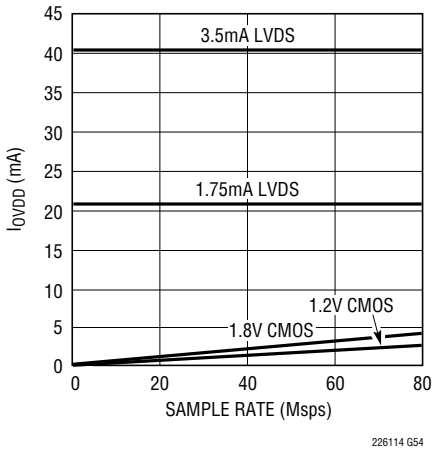
LTC2259-14: SFDR vs Input Level, f_{IN} = 70MHz, 2V Range, 80Msps



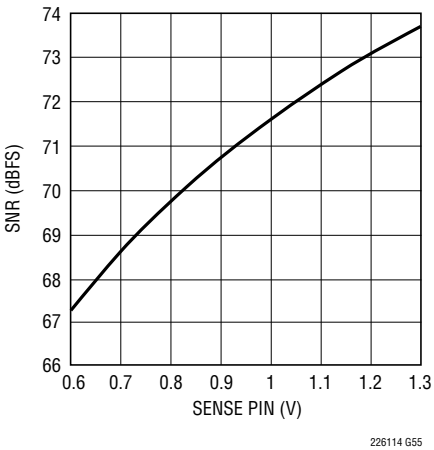
LTC2259-14: I_{VDD} vs Sample Rate, 5MHz Sine Wave Input, –1dB



LTC2259-14: I_{OVDD} vs Sample Rate, 5MHz Sine Wave Input, –1dB, 5pF on Each Data Output



LTC2259-14: SNR vs SENSE, f_{IN} = 5MHz, –1dB



PIN FUNCTIONS

PINS THAT ARE THE SAME FOR ALL DIGITAL OUTPUT MODES

A_{IN}^+ (Pin 1): Positive Differential Analog Input.

A_{IN}^- (Pin 2): Negative Differential Analog Input.

GND (Pin 3): ADC Power Ground.

REFH (Pins 4, 5): ADC High Reference. Bypass to Pins 6, 7 with a 2.2µF ceramic capacitor and to ground with a 0.1µF ceramic capacitor.

REFL (Pins 6, 7): ADC Low Reference. Bypass to Pins 4, 5 with a 2.2µF ceramic capacitor and to ground with a 0.1µF ceramic capacitor.

PAR/$\overline{SER}$ (Pin 8): Programming Mode Selection Pin. Connect to ground to enable the serial programming mode. $\overline{CS}$, SCK, SDI, SDO become a serial interface that control the A/D operating modes. Connect to V_{DD} to enable the parallel programming mode where $\overline{CS}$, SCK, SDI become parallel logic inputs that control a reduced set of the A/D operating modes. PAR/$\overline{SER}$ should be connected directly to ground or the V_{DD} of the part and not be driven by a logic signal.

V_{DD} (Pins 9, 10, 40): 1.8V Analog Power Supply. Bypass to ground with 0.1µF ceramic capacitors. Pins 9 and 10 can share a bypass capacitor.

ENC^+ (Pin 11): Encode Input. Conversion starts on the rising edge.

ENC^- (Pin 12): Encode Complement Input. Conversion starts on the falling edge.

$\overline{CS}$ (Pin 13): In serial programming mode, (PAR/$\overline{SER}$ = 0V), $\overline{CS}$ is the serial interface chip select input. When $\overline{CS}$ is low, SCK is enabled for shifting data on SDI into the mode control registers. In the parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), $\overline{CS}$ controls the clock duty cycle stabilizer. When $\overline{CS}$ is low, the clock duty cycle stabilizer is turned off. When $\overline{CS}$ is high, the clock duty cycle stabilizer is turned on. $\overline{CS}$ can be driven with 1.8V to 3.3V logic.

SCK (Pin 14): In serial programming mode, (PAR/$\overline{SER}$ = 0V), SCK is the serial interface clock input. In the parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), SCK controls the digital output mode. When SCK is low, the full-rate CMOS output mode is enabled. When SCK is high, the double-data rate LVDS output mode (with 3.5mA output current) is enabled. SCK can be driven with 1.8V to 3.3V logic.

SDI (Pin 15): In serial programming mode, (PAR/$\overline{SER}$ = 0V), SDI is the serial interface data input. Data on SDI is clocked into the mode control registers on the rising edge of SCK. In the parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), SDI can be used to power down the part. When SDI is low, the part operates normally. When SDI is high, the part enters sleep mode. SDI can be driven with 1.8V to 3.3V logic.

SDO (Pin 16): In serial programming mode, (PAR/$\overline{SER}$ = 0V), SDO is the optional serial interface data output. Data on SDO is read back from the mode control registers and can be latched on the falling edge of SCK. SDO is an open-drain NMOS output that requires an external 2k pull-up resistor to 1.8V-3.3V. If read back from the mode control registers is not needed, the pull-up resistor is not necessary and SDO can be left unconnected. In the parallel programming mode (PAR/$\overline{SER}$ = V_{DD}), SDO is not used and should not be connected.

OGND (Pin 25): Output Driver Ground.

OV_{DD} (Pin 26): Output Driver Supply. Bypass to ground with a 0.1µF ceramic capacitor.

V_{CM} (Pin 37): Common Mode Bias Output, Nominally Equal to $V_{DD}/2$. V_{CM} should be used to bias the common mode of the analog inputs. Bypass to ground with a 0.1µF ceramic capacitor.

V_{REF} (Pin 38): Reference Voltage Output. Bypass to ground with a 1µF ceramic capacitor, nominally 1.25V.

SENSE (Pin 39): Reference Programming Pin. Connecting SENSE to V_{DD} selects the internal reference and a ±1V input range. Connecting SENSE to ground selects the internal reference and a ±0.5V input range. An external reference between 0.625V and 1.3V applied to SENSE selects an input range of ±0.8 • V_{SENSE}.

PIN FUNCTIONS

FULL-RATE CMOS OUTPUT MODE

All Pins Below Have CMOS Output Levels (OGND to OV_{DD})

D0 to D13 (Pins 17-24, 29-34): Digital Outputs. D13 is the MSB.

CLKOUT⁻ (Pin 27): Inverted Version of CLKOUT⁺.

CLKOUT⁺ (Pin 28): Data Output Clock. The digital outputs normally transition at the same time as the falling edge of CLKOUT⁺. The phase of CLKOUT⁺ can also be delayed relative to the digital outputs by programming the mode control registers.

DNC (Pin 35): Do not connect this pin.

OF (Pin 36): Over/Under Flow Digital Output. OF is high when an overflow or underflow has occurred.

DOUBLE-DATA RATE CMOS OUTPUT MODE

All Pins Below Have CMOS Output Levels (OGND to OV_{DD})

D0_1 to D12_13 (Pins 18, 20, 22, 24, 30, 32, 34): Double-Data Rate Digital Outputs. Two data bits are multiplexed onto each output pin. The even data bits (D0, D2, D4, D6, D8, D10, D12) appear when CLKOUT⁺ is low. The odd data bits (D1, D3, D5, D7, D9, D11, D13) appear when CLKOUT⁺ is high.

CLKOUT⁻ (Pin 27): Inverted Version of CLKOUT⁺.

CLKOUT⁺ (Pin 28): Data Output Clock. The digital outputs normally transition at the same time as the falling and rising edges of CLKOUT⁺. The phase of CLKOUT⁺ can also be delayed relative to the digital outputs by programming the mode control registers.

DNC (Pins 17, 19, 21, 23, 29, 31, 33, 35): Do not connect these pins.

OF (Pin 36): Over/Under Flow Digital Output. OF is high when an overflow or underflow has occurred.

DOUBLE-DATA RATE LVDS OUTPUT MODE

All Pins Below Have LVDS Output Levels. The Output Current Level is Programmable. There is an Optional Internal 100Ω Termination Resistor Between the Pins of Each LVDS Output Pair.

D0_1⁻/D0_1⁺ to D12_13⁻/D12_13⁺ (Pins 17/18, 19/20, 21/22, 23/24, 29/30, 31/32, 33/34): Double-Data Rate Digital Outputs. Two data bits are multiplexed onto each differential output pair. The even data bits (D0, D2, D4, D6, D8, D10, D12) appear when CLKOUT⁺ is low. The odd data bits (D1, D3, D5, D7, D9, D11, D13) appear when CLKOUT⁺ is high.

CLKOUT⁻/CLKOUT⁺ (Pins 27/28): Data Output Clock. The digital outputs normally transition at the same time as the falling and rising edges of CLKOUT⁺. The phase of CLKOUT⁺ can also be delayed relative to the digital outputs by programming the mode control registers.

OF⁻/OF⁺ (Pins 35/36): Over/Under Flow Digital Output. OF⁺ is high when an overflow or underflow has occurred.

FUNCTIONAL BLOCK DIAGRAM

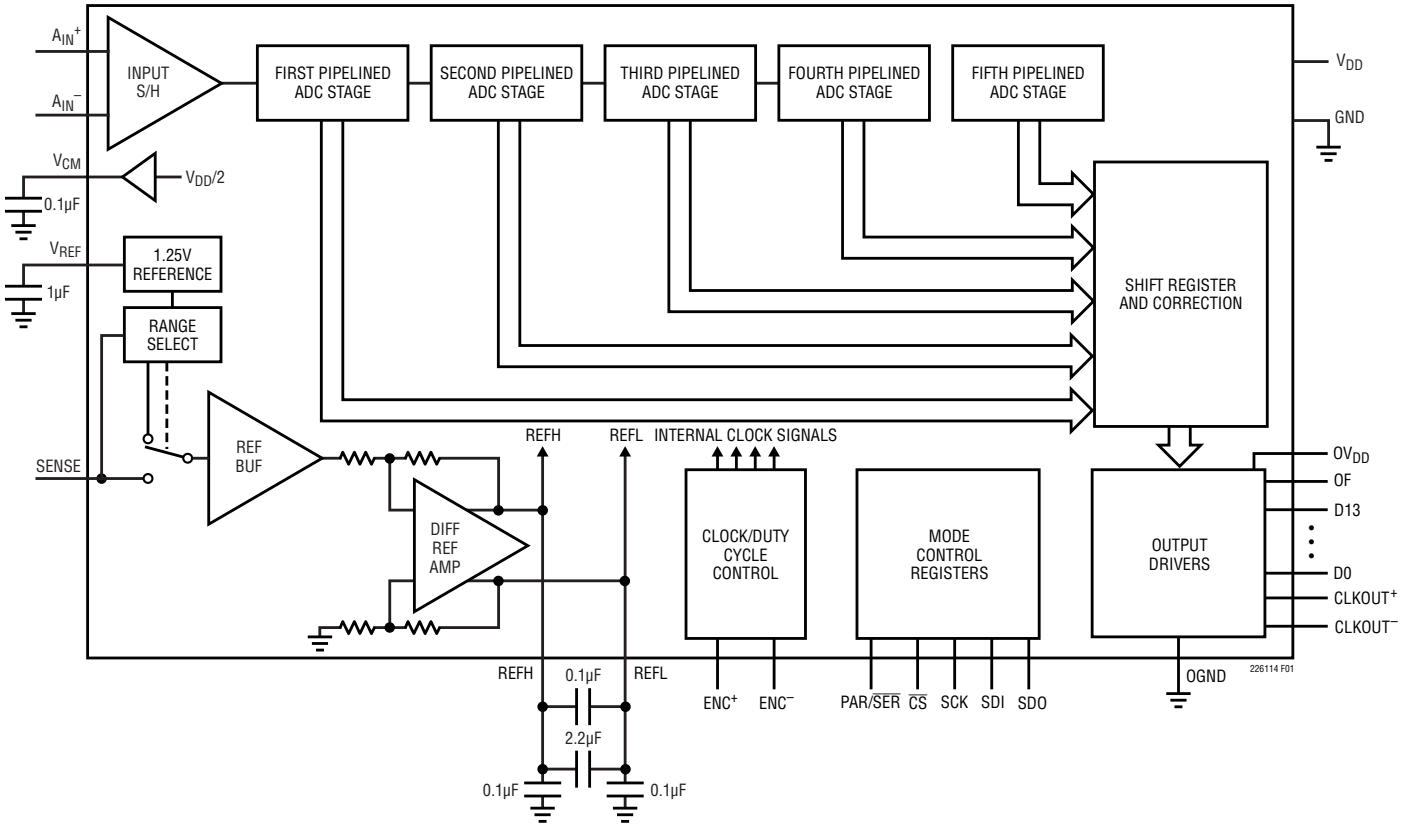


Figure 1. Functional Block Diagram

APPLICATIONS INFORMATION

CONVERTER OPERATION

The LTC2261-14/LTC2260-14/LTC2259-14 are low power 14-bit 125Msps/105Msps/80Msps A/D converters that are powered by a single 1.8V supply. The analog inputs should be driven differentially. The encode input can be driven differentially, or single ended for lower power consumption. The digital outputs can be CMOS, double-data rate CMOS (to halve the number of output lines), or double-data rate LVDS (to reduce digital noise in the system.) Many additional features can be chosen by programming the mode control registers through a serial SPI port. See the Serial Programming Mode section.

ANALOG INPUT

The analog input is a differential CMOS sample-and-hold circuit (Figure 2). The inputs should be driven differentially around a common mode voltage set by the V_{CM} output pin, which is nominally $V_{DD}/2$. For the 2V input range, the inputs should swing from V_{CM} – 0.5V to V_{CM} + 0.5V. There should be 180° phase difference between the inputs.

INPUT DRIVE CIRCUITS

Input Filtering

If possible, there should be an RC lowpass filter right at the analog inputs. This lowpass filter isolates the drive circuitry from the A/D sample-and-hold switching, and also limits wideband noise from the drive circuitry. Figure 3 shows an example of an input RC filter. The RC component values should be chosen based on the application's input frequency.

Transformer-Coupled Circuits

Figure 3 shows the analog input being driven by an RF transformer with a center-tapped secondary. The center tap is biased with V_{CM}, setting the A/D input at its optimal

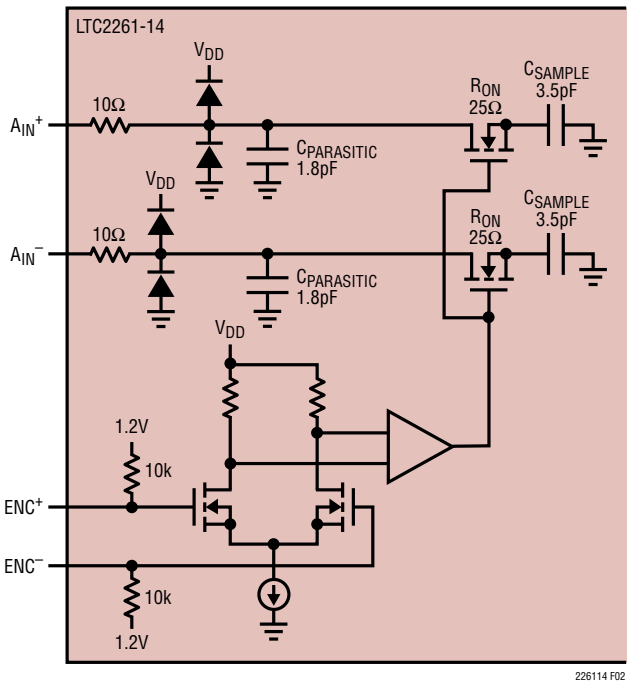


Figure 2. Equivalent Input Circuit

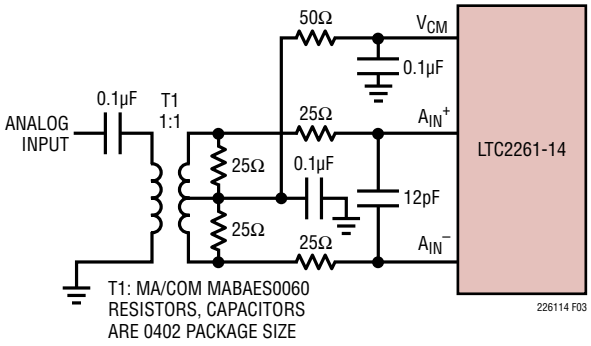


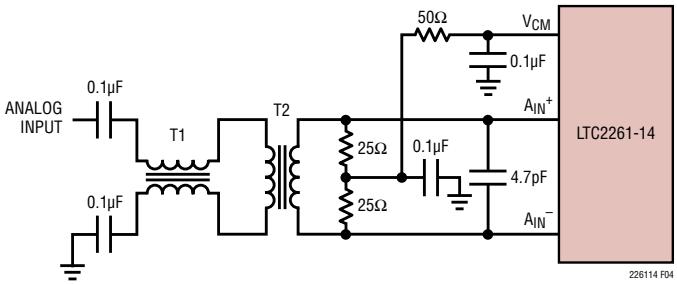
Figure 3. Analog Input Circuit Using a Transformer. Recommended for Input Frequencies from 5MHz to 70MHz

APPLICATIONS INFORMATION

DC level. At higher input frequencies a transmission line balun transformer (Figures 4 to 6) has better balance, resulting in lower A/D distortion.

Amplifier Circuits

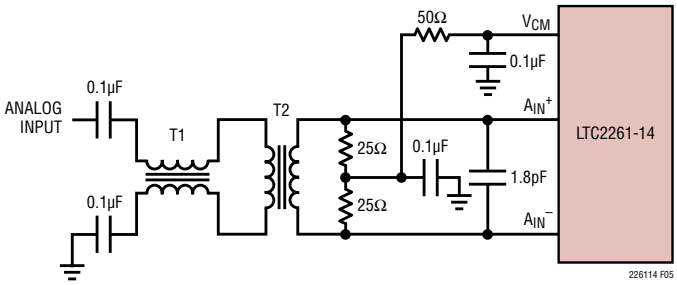
Figure 7 shows the analog input being driven by a high speed differential amplifier. The output of the amplifier is AC-coupled to the A/D so the amplifier's output common mode voltage can be optimally set to minimize distortion.



T1: MA/COM MABA-007159-000000
T2: MA/COM MABAES0060
RESISTORS, CAPACITORS ARE 0402 PACKAGE SIZE

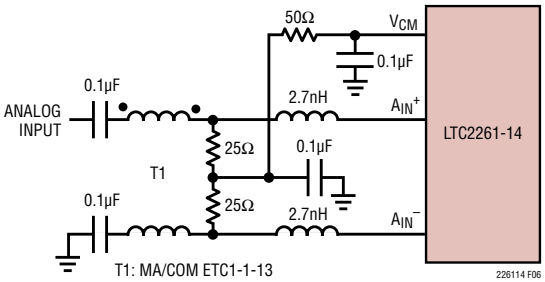
Figure 4. Recommended Front-End Circuit for Input Frequencies from 70MHz to 170MHz

At very high frequencies an RF gain block will often have lower distortion than a differential amplifier. If the gain block is single-ended, then a transformer circuit (Figures 4 to 6) should convert the signal to differential before driving the A/D.



T1: MA/COM MABA-007159-000000
T2: COILCRAFT WBC1-1LB
RESISTORS, CAPACITORS ARE 0402 PACKAGE SIZE

Figure 5. Recommended Front-End Circuit for Input Frequencies from 170MHz to 270MHz



T1: MA/COM ETC1-1-13
RESISTORS, CAPACITORS
ARE 0402 PACKAGE SIZE

Figure 6. Recommended Front-End Circuit for Input Frequencies Above 270MHz

APPLICATIONS INFORMATION

Reference

The LTC2261-14/LTC2260-14/LTC2259-14 have an internal 1.25V voltage reference. For a 2V input range using the internal reference, connect SENSE to V_{DD}. For a 1V input range using the internal reference, connect SENSE to ground. For a 2V input range with an external reference, apply a 1.25V reference voltage to SENSE (Figure 9.)

The input range can be adjusted by applying a voltage to SENSE that is between 0.625V and 1.30V. The input range will then be 1.6 • V_{SENSE}.

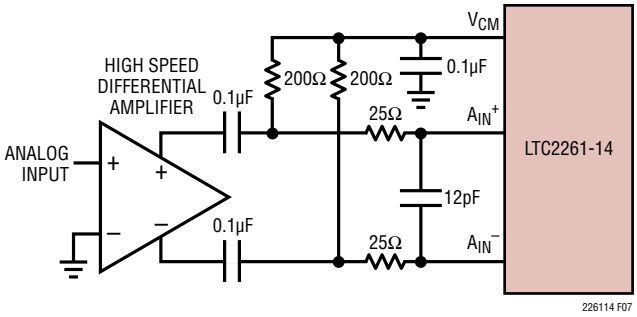


Figure 7. Front-End Circuit Using a High Speed Differential Amplifier

The V_{REF}, REFH and REFL pins should be bypassed as shown in Figure 8. The 0.1µF capacitor between REFH and REFL should be as close to the pins as possible (not on the back side of the circuit board).

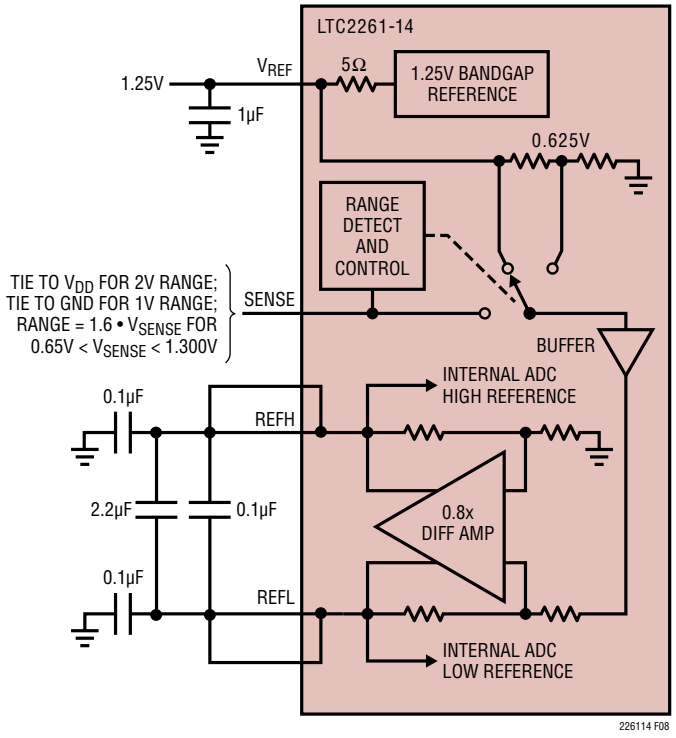


Figure 8. Reference Circuit

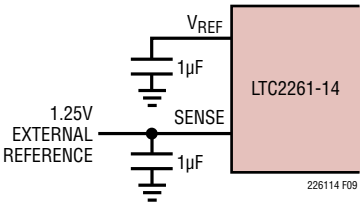


Figure 9. Using an External 1.25V Reference

APPLICATIONS INFORMATION

Encode Input

The signal quality of the encode inputs strongly affects the A/D noise performance. The encode inputs should be treated as analog signals—do not route them next to digital traces on the circuit board. There are two modes of operation for the encode inputs: the differential encode mode (Figure 10) and the single-ended encode mode (Figure 11).

The differential encode mode is recommended for sinusoidal, PECL or LVDS encode inputs (Figures 12, 13). The encode inputs are internally biased to 1.2V through 10k equivalent resistance. The encode inputs can be taken above V_{DD} (up to 3.6V), and the common mode range is from 1.1V to 1.6V. In the differential encode mode, ENC^- should stay at least 200mV above ground to avoid falsely triggering the single-ended encode mode. For good jitter performance ENC^+ and ENC^- should have fast rise and fall times.

The single-ended encode mode should be used with CMOS encode inputs. To select this mode, ENC^- is connected to ground and ENC^+ is driven with a square wave encode input. ENC^+ can be taken above V_{DD} (up to 3.6V) so 1.8V to 3.3V CMOS logic levels can be used. The ENC^+ threshold is 0.9V. For good jitter performance ENC^+ should have fast rise and fall times.

Clock Duty Cycle Stabilizer

For good performance the encode signal should have a 50%(±5%) duty cycle. If the optional clock duty cycle stabilizer circuit is enabled, the encode duty cycle can vary from 30% to 70% and the duty cycle stabilizer will maintain a constant 50% internal duty cycle. If the encode signal changes frequency or is turned off, the duty cycle stabilizer circuit requires one hundred clock cycles to lock onto the input clock. The duty cycle stabilizer is enabled by mode control register A2 (serial programming mode), or by $\overline{CS}$ (parallel programming mode).

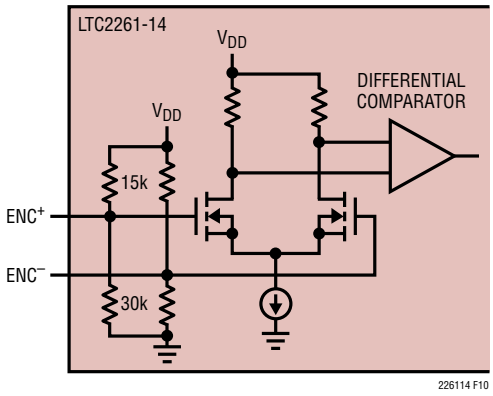


Figure 10. Equivalent Encode Input Circuit for Differential Encode Mode

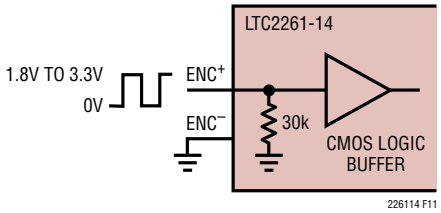
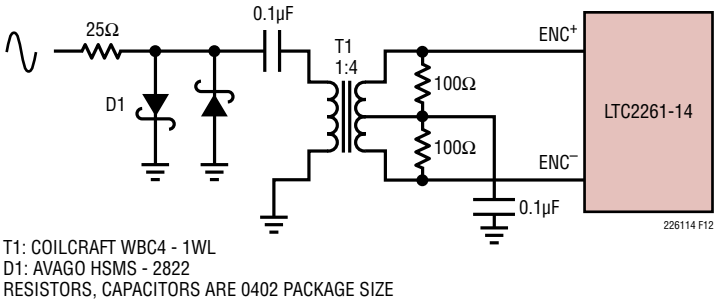


Figure 11. Equivalent Encode Input Circuit for Single-Ended Encode Mode



T1: COILCRAFT WBC4 - 1WL
D1: AVAGO HSMS - 2822
RESISTORS, CAPACITORS ARE 0402 PACKAGE SIZE

Figure 12. Sinusoidal Encode Drive

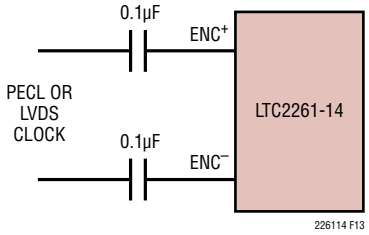


Figure 13. PECL or LVDS Encode Drive

APPLICATIONS INFORMATION

For applications where the sample rate needs to be changed quickly, the clock duty cycle stabilizer can be disabled. If the duty cycle stabilizer is disabled, care should be taken to make the sampling clock have a 50%(±5%) duty cycle. The duty cycle stabilizer should not be used below 5Msps.

DIGITAL OUTPUTS

Digital Output Modes

The LTC2261-14/LTC2260-14/LTC2259-14 can operate in three digital output modes: full-rate CMOS, double-data rate CMOS (to halve the number of output lines), or double-data rate LVDS (to reduce digital noise in the system). The output mode is set by mode control register A3 (serial programming mode), or by SCK (parallel programming mode). Note that double-data rate CMOS cannot be selected in the parallel programming mode.

Full-Rate CMOS Mode

In full-rate CMOS mode the 14 digital outputs (D0-D13), overflow (OF), and the data output clocks ($CLKOUT^+$, $CLKOUT^-$) have CMOS output levels. The outputs are powered by OV_{DD} and OGND which are isolated from the A/D core power and ground. OV_{DD} can range from 1.1V to 1.9V, allowing 1.2V through 1.8V CMOS logic outputs.

For good performance, the digital outputs should drive minimal capacitive loads. If the load capacitance is larger than 10pF a digital buffer should be used.

Double-Data Rate CMOS Mode

In double-data rate CMOS mode, two data bits are multiplexed and output on each data pin. This reduces the number of data lines by seven, simplifying board routing and reducing the number of input pins needed to receive the data. The 7 digital outputs (D0_1, D2_3, D4_5, D6_7, D8_9, D10_11, D12_13), overflow (OF), and the data output clocks ($CLKOUT^+$, $CLKOUT^-$) have CMOS output levels. The outputs are powered by OV_{DD} and OGND which are isolated from the A/D core power and ground. OV_{DD} can range from 1.1V to 1.9V, allowing 1.2V through 1.8V CMOS logic outputs.

For good performance the digital outputs should drive minimal capacitive loads. If the load capacitance is larger than 10pF a digital buffer should be used.

When using double-data rate CMOS at high sample rates the SNR will degrade slightly (see Typical Performance Characteristics section). DDR CMOS is not recommended for sample frequencies above 100MHz.

Double-Data Rate LVDS Mode

In double-data rate LVDS mode, two data bits are multiplexed and output on each differential output pair. There are 7 LVDS output pairs ($D0\_1^+/D0\_1^-$ through $D12\_13^+/D12\_13^-$) for the digital output data. Overflow (OF^+/OF^-) and the data output clock ($CLKOUT^+/CLKOUT^-$) each have an LVDS output pair.

By default the outputs are standard LVDS levels: 3.5mA output current and a 1.25V output common mode voltage. An external 100Ω differential termination resistor is required for each LVDS output pair. The termination resistors should be located as close as possible to the LVDS receiver.

The outputs are powered by OV_{DD} and OGND which are isolated from the A/D core power and ground. In LVDS mode, OV_{DD} must be 1.8V.

Programmable LVDS Output Current

In LVDS mode, the default output driver current is 3.5mA. This current can be adjusted by serially programming mode control register A3. Available current levels are 1.75mA, 2.1mA, 2.5mA, 3mA, 3.5mA, 4mA and 4.5mA.

Optional LVDS Driver Internal Termination

In most cases using just an external 100Ω termination resistor will give excellent LVDS signal integrity. In addition, an optional internal 100Ω termination resistor can be enabled by serially programming mode control register A3. The internal termination helps absorb any reflections caused by imperfect termination at the receiver. When the internal termination is enabled, the output driver current is increased by 1.6x to maintain about the same output voltage swing.

Overflow Bit

The overflow output bit (OF) outputs a logic high when the analog input is either overranged or underranged. The overflow bit has the same pipeline latency as the data bits.

APPLICATIONS INFORMATION

Phase Shifting the Output Clock

In full-rate CMOS mode the data output bits normally change at the same time as the falling edge of CLKOUT+, so the rising edge of CLKOUT+ can be used to latch the output data. In double-data rate CMOS and LVDS modes the data output bits normally change at the same time as the falling and rising edges of CLKOUT+. To allow adequate setup-and-hold time when latching the data, the CLKOUT+ signal may need to be phase shifted relative to the data output bits. Most FPGAs have this feature; this is generally the best place to adjust the timing.

The LTC2261-14/LTC2260-14/LTC2259-14 can also phase shift the CLKOUT+/CLKOUT– signals by serially programming mode control register A2. The output clock can be shifted by 0°, 45°, 90° or 135°. To use the phase shifting feature the clock duty cycle stabilizer must be turned on. Another control register bit can invert the polarity of CLKOUT+ and CLKOUT–, independently of the phase shift. The combination of these two features enables phase shifts of 45° up to 315° (Figure 14).

DATA FORMAT

Table 1 shows the relationship between the analog input voltage, the digital data output bits and the overflow bit. By default the output data format is offset binary. The 2's complement format can be selected by serially programming mode control register A4.

Table 1. Output Codes vs Input Voltage

$A_{IN}^+ - A_{IN}^-$ (2V Range)	OF	D13-D0 (OFFSET BINARY)	D13-D0 (2's COMPLEMENT)
>1.000000V	1	11 1111 1111 1111	01 1111 1111 1111
+0.999878V	0	11 1111 1111 1111	01 1111 1111 1111
+0.999756V	0	11 1111 1111 1110	01 1111 1111 1110
+0.000122V	0	10 0000 0000 0001	00 0000 0000 0001
+0.000000V	0	10 0000 0000 0000	00 0000 0000 0000
–0.000122V	0	01 1111 1111 1111	11 1111 1111 1111
–0.000244V	0	01 1111 1111 1110	11 1111 1111 1110
–0.999878V	0	00 0000 0000 0001	10 0000 0000 0001
–1.000000V	0	00 0000 0000 0000	10 0000 0000 0000
≤–1.000000V	1	00 0000 0000 0000	10 0000 0000 0000

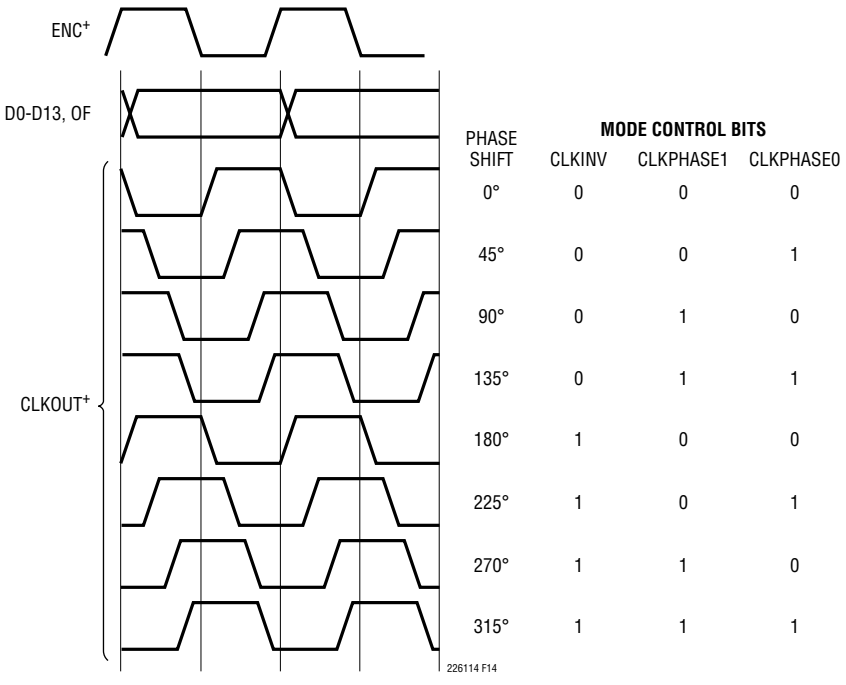


Figure 14. Phase Shifting CLKOUT

APPLICATIONS INFORMATION

Digital Output Randomizer

Interference from the A/D digital outputs is sometimes unavoidable. Digital interference may be from capacitive or inductive coupling or coupling through the ground plane. Even a tiny coupling factor can cause unwanted tones in the ADC output spectrum. By randomizing the digital output before it is transmitted off chip, these unwanted tones can be randomized which reduces the unwanted tone amplitude.

The digital output is *randomized* by applying an exclusive-OR logic operation between the LSB and all other data output bits. To decode, the reverse operation is applied—an exclusive-OR operation is applied between the LSB and all other bits. The LSB, OF and CLKOUT outputs are not affected. The output randomizer is enabled by serially programming mode control register A4.

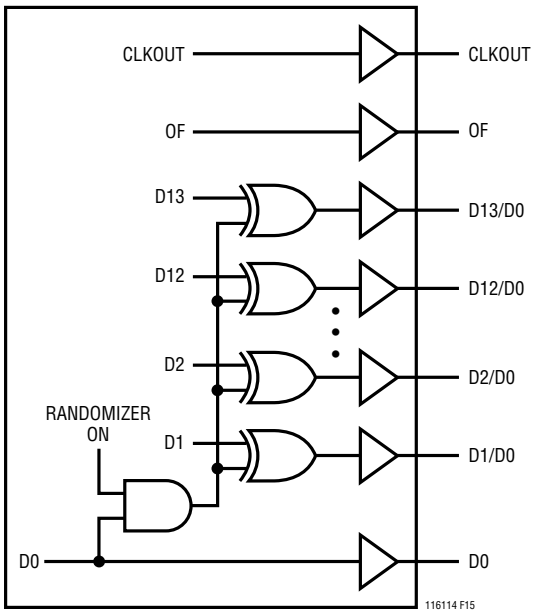


Figure 15. Functional Equivalent of Digital Output Randomizer

Alternate Bit Polarity

Another feature that reduces digital feedback on the circuit board is the alternate bit polarity mode. When this mode is enabled, all of the odd bits (D1, D3, D5, D7, D9, D11, D13) are inverted before the output buffers. The even bits (D0, D2, D4, D6, D8, D10, D12), OF and CLKOUT are not affected. This can reduce digital currents in the circuit board ground plane and reduce digital noise, particularly for very small analog input signals.

When there is a very small signal at the input of the A/D that is centered around mid-scale, the digital outputs toggle between mostly 1s and mostly 0s. This simultaneous switching of most of the bits will cause large currents in the ground plane. By inverting every other bit, the alternate bit polarity mode makes half of the bits transition high while half of the bits transition low. To first order, this cancels current flow in the ground plane, reducing the digital noise.

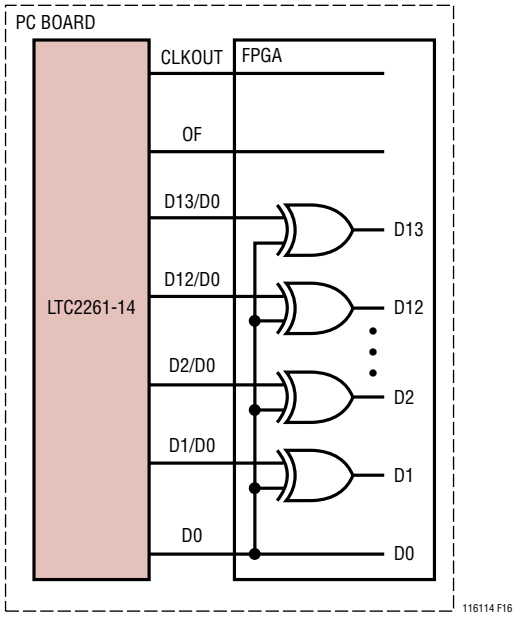


Figure 16. Unrandomizing a Randomized Digital Output Signal

APPLICATIONS INFORMATION

The digital output is decoded at the receiver by inverting the odd bits (D1, D3, D5, D7, D9, D11, D13.) The alternate bit polarity mode is independent of the digital output randomizer—either, both or neither function can be on at the same time. When alternate bit polarity mode is on, the data format is offset binary and the 2's complement control bit has no effect. The alternate bit polarity mode is enabled by serially programming mode control register A4.

Digital Output Test Patterns

To allow in-circuit testing of the digital interface to the A/D, there are several test modes that force the A/D data outputs (OF, D13-D0) to known values:

All 1s: All outputs are 1

All 0s: All outputs are 0

Alternating: Outputs change from all 1s to all 0s on alternating samples

Checkerboard: Outputs change from 101010101010101 to 010101010101010 on alternating samples

The digital output test patterns are enabled by serially programming mode control register A4. When enabled, the test patterns override all other formatting modes: 2's complement, randomizer, alternate-bit-polarity.

Output Disable

The digital outputs may be disabled by serially programming mode control register A3. All digital outputs including OF and CLKOUT are disabled. The high impedance disabled state is intended for long periods of inactivity—it is too slow to multiplex a data bus between multiple converters at full speed.

Sleep and Nap Modes

The A/D may be placed in sleep or nap modes to conserve power. In sleep mode the entire A/D converter is powered down, resulting in 0.5mW power consumption. Sleep mode is enabled by mode control register A1 (serial programming mode), or by SDI (parallel programming mode). The amount of time required to recover from sleep mode depends on the size of the bypass capacitors on V_{REF}, REFH, and REFL. For the suggested values in Figure 8, the A/D will stabilize after 2ms.

In nap mode the A/D core is powered down while the internal reference circuits stay active, allowing faster wake-up than from sleep mode. Recovering from nap mode requires at least 100 clock cycles. If the application demands very accurate DC settling then an additional 50µs should be allowed so the on-chip references can settle from the slight temperature shift caused by the change in supply current as the A/D leaves nap mode. Nap mode is enabled by mode control register A1 in the serial programming mode.

DEVICE PROGRAMMING MODES

The operating modes of the LTC2261-14 can be programmed by either a parallel interface or a simple serial interface. The serial interface has more flexibility and can program all available modes. The parallel interface is more limited and can only program some of the more commonly used modes.

Parallel Programming Mode

To use the parallel programming mode, PAR/$\overline{SER}$ should be tied to V_{DD}. The $\overline{CS}$, SCK and SDI pins are binary logic inputs that set certain operating modes. These pins can be tied to V_{DD} or ground, or driven by 1.8V, 2.5V or 3.3V CMOS logic. Table 2 shows the modes set by $\overline{CS}$, SCK and SDI.

Table 2. Parallel Programming Mode Control Bits (PAR/$\overline{SER}$ = V_{DD})

PIN	DESCRIPTION
$\overline{CS}$	Clock Duty Cycle Stabilizer Control Bit 0 = Clock Duty Cycle Stabilizer Off 1 = Clock Duty Cycle Stabilizer On
SCK	Digital Output Mode Control Bit 0 = Full-Rate CMOS Output Mode 1 = Double-Data Rate LVDS Output Mode (3.5mA LVDS Current, Internal Termination Off)
SDI	Power Down Control Bit 0 = Normal Operation 1 = Sleep Mode

APPLICATIONS INFORMATION

Serial Programming Mode

To use the serial programming mode, PAR/$\overline{SER}$ should be tied to ground. The $\overline{CS}$, SCK, SDI and SDO pins become a serial interface that program the A/D mode control registers. Data is written to a register with a 16-bit serial word. Data can also be read back from a register to verify its contents.

Serial data transfer starts when $\overline{CS}$ is taken low. The data on the SDI pin is latched at the first 16 rising edges of SCK. Any SCK rising edges after the first 16 are ignored. The data transfer ends when $\overline{CS}$ is taken high again.

The first bit of the 16-bit input word is the R/$\overline{W}$ bit. The next seven bits are the address of the register (A6:A0). The final eight bits are the register data (D7:D0).

If the R/$\overline{W}$ bit is low, the serial data (D7:D0) will be written to the register set by the address bits (A6:A0). If the R/$\overline{W}$ bit is high, data in the register set by the address bits (A6:A0) will be read back on the SDO pin (see the timing diagrams). During a read back command the register is not updated and data on SDI is ignored.

The SDO pin is an open-drain output that pulls to ground with a 200Ω impedance. If register data is read back through SDO, an external 2k pull-up resistor is required. If serial data is only written and read back is not needed, then SDO can be left floating and no pull-up resistor is needed.

Table 3 shows a map of the mode control registers.

Software Reset

If serial programming is used, the mode control registers should be programmed as soon as possible after the power supplies turn on and are stable. The first serial command must be a software reset which will reset all register data bits to logic 0. To perform a software reset, bit D7 in the reset register is written with a logic 1. After the reset SPI write command is complete, bit D7 is automatically set back to zero.

Table 3. Serial Programming Mode Register Map

REGISTER A0: RESET REGISTER (ADDRESS 00h)

D7	D6	D5	D4	D3	D2	D1	D0
RESET	X	X	X	X	X	X	X

Bit 7	**RESET**	Software Reset Bit
	0 = Not Used 1 = Software Reset. All Mode Control Registers are Reset to 00h. This Bit is Automatically Set Back to Zero at the End of the SPI Write Command. The Reset Register Is Write Only.	
Bits 6-0	Unused, Don't Care Bits.	

REGISTER A1: POWER-DOWN REGISTER (ADDRESS 01h)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	PWROFF1	PWROFF0

Bits 7-2	Unused, Don't Care Bits.	
Bits 1-0	**PWROFF1:PWROFF0** 00 = Normal Operation 01 = Nap Mode 10 = Not Used 11 = Sleep Mode	Power Down Control Bits

APPLICATIONS INFORMATION

REGISTER A2: TIMING REGISTER (ADDRESS 02h)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	CLKINV	CLKPHASE1	CLKPHASE0	DCS

Bits 7-4 Unused, Don't Care Bits.

Bit 3 **CLKINV** Output Clock Invert Bit
0 = Normal CLKOUT Polarity (As Shown in the Timing Diagrams)
1 = Inverted CLKOUT Polarity

Bits 2-1 **CLKPHASE1:CLKPHASE0** Output Clock Phase Delay Bits
00 = No CLKOUT Delay (As Shown in the Timing Diagrams)
01 = $CLKOUT^+/CLKOUT^-$ Delayed by 45° (Clock Period • 1/8)
10 = $CLKOUT^+/CLKOUT^-$ Delayed by 90° (Clock Period • 1/4)
11 = $CLKOUT^+/CLKOUT^-$ Delayed by 135° (Clock Period • 3/8)
Note: If the CLKOUT Phase Delay Feature is Used, the Clock Duty Cycle Stabilizer Must Also be Turned On

Bit 0 **DCS** Clock Duty Cycle Stabilizer Bit
0 = Clock Duty Cycle Stabilizer Off
1 = Clock Duty Cycle Stabilizer On

REGISTER A3: OUTPUT MODE REGISTER (ADDRESS 03h)

D7	D6	D5	D4	D3	D2	D1	D0
X	ILVDS2	ILVDS1	ILVDS0	TERMON	OUTOFF	OUTMODE1	OUTMODE0

Bit 7 Unused, Don't Care Bit.

Bits 6-4 **ILVDS2:ILVDS0** LVDS Output Current Bits
000 = 3.5mA LVDS Output Driver Current
001 = 4.0mA LVDS Output Driver Current
010 = 4.5mA LVDS Output Driver Current
011 = Not Used
100 = 3.0mA LVDS Output Driver Current
101 = 2.5mA LVDS Output Driver Current
110 = 2.1mA LVDS Output Driver Current
111 = 1.75mA LVDS Output Driver Current

Bit 3 **TERMON** LVDS Internal Termination Bit
0 = Internal Termination Off
1 = Internal Termination On. LVDS Output Driver Current is 1.6× the Current Set by ILVDS2:ILVDS0

Bit 2 **OUTOFF** Output Disable Bit
0 = Digital Outputs are Enabled
1 = Digital Outputs are Disabled and Have High Output Impedance

Bits 1-0 **OUTMODE1:OUTMODE0** Digital Output Mode Control Bits
00 = Full-Rate CMOS Output Mode
01 = Double-Data Rate LVDS Output Mode
10 = Double-Data Rate CMOS Output Mode
11 = Not Used

APPLICATIONS INFORMATION

REGISTER A4: DATA FORMAT REGISTER (ADDRESS 04h)

D7	D6	D5	D4	D3	D2	D1	D0
X	X	OUTTEST2	OUTTEST1	OUTTEST0	ABP	RAND	TWOSCOMP

Bit 7-6 Unused, Don't Care Bits.

Bits 5-3 **OUTTEST2:OUTTEST0** Digital Output Test Pattern Bits
000 = Digital Output Test Patterns Off
001 = All Digital Outputs = 0
011 = All Digital Outputs = 1
101 = Checkerboard Output Pattern. OF, D13-D0 Alternate Between 101 0101 0101 0101 and 010 1010 1010 1010
111 = Alternating Output Pattern. OF, D13-D0 Alternate Between 000 0000 0000 0000 and 111 1111 1111 1111
Note: Other Bit Combinations are not Used

Bit 2 **ABP** Alternate Bit Polarity Mode Control Bit
0 = Alternate Bit Polarity Mode Off
1 = Alternate Bit Polarity Mode On

Bit 1 **RAND** Data Output Randomizer Mode Control Bit
0 = Data Output Randomizer Mode Off
1 = Data Output Randomizer Mode On

Bit 0 **TWOSCOMP** Two's Complement Mode Control Bit
0 = Offset Binary Data Format
1 = Two's Complement Data Format
Note: ABP = 1 Forces the Output Format to be Offset Binary

GROUNDING AND BYPASSING

The LTC2261-14 requires a printed circuit board with a clean unbroken ground plane. A multilayer board with an internal ground plane is recommended. Layout for the printed circuit board should ensure that digital and analog signal lines are separated as much as possible. In particular, care should be taken not to run any digital track alongside an analog signal track or underneath the ADC.

High quality ceramic bypass capacitors should be used at the V_{DD}, OV_{DD}, V_{CM}, V_{REF}, REFH and REFL pins. Bypass capacitors must be located as close to the pins as possible. Of particular importance is the 0.1µF capacitor between REFH and REFL. This capacitor should be on the same side of the circuit board as the A/D, and as close to the device as possible (1.5mm or less). Size 0402 ceramic capacitors are recommended. The larger 2.2µF capacitor between REFH and REFL can be somewhat further away.

The V_{CM} capacitor should be located as close to the pin as possible. To make space for this the capacitor on V_{REF} can be further away or on the back of the PC board. The traces connecting the pins and bypass capacitors must be kept short and should be made as wide as possible.

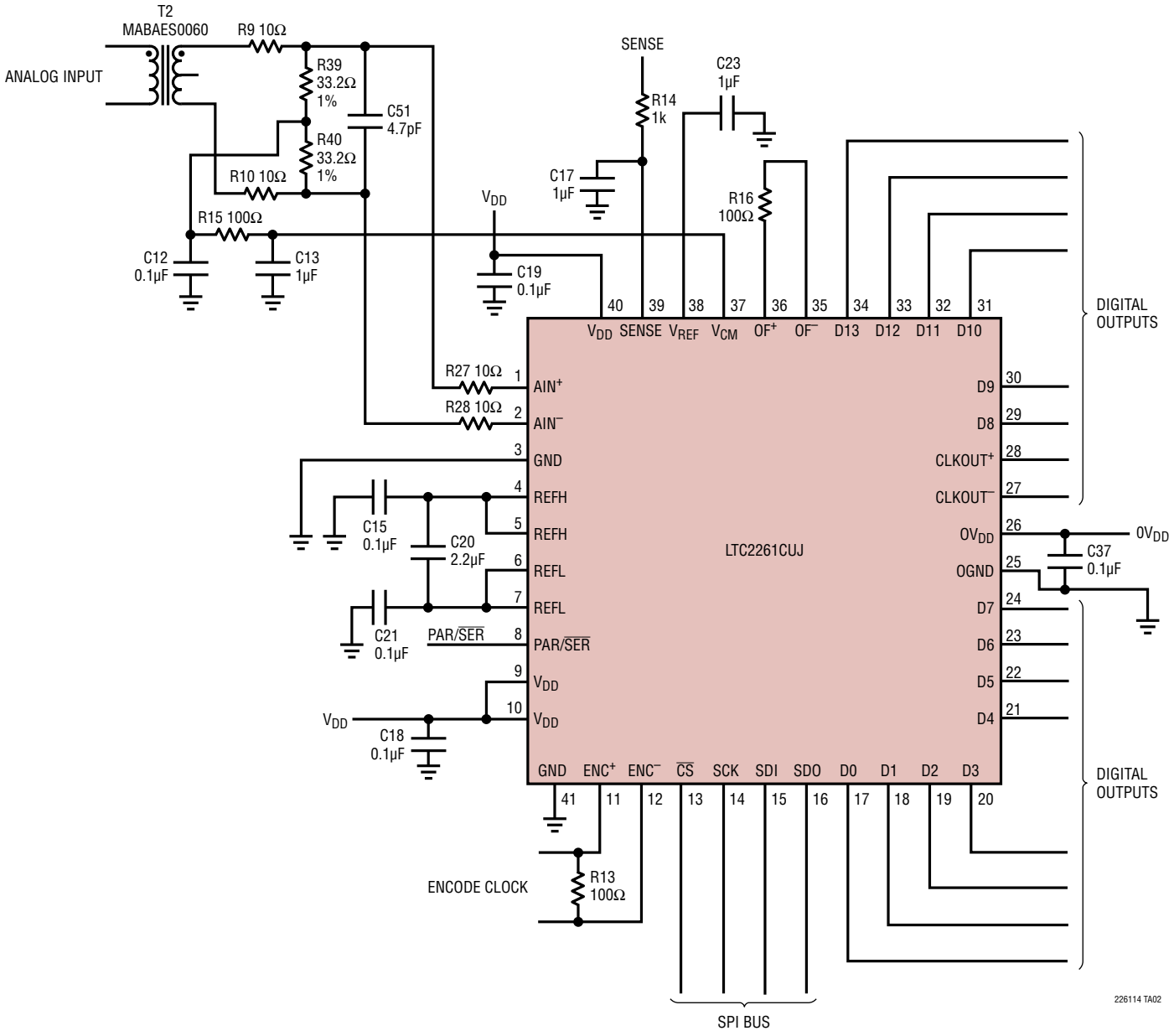
The analog inputs, encode signals, and digital outputs should not be routed next to each other. Ground fill and grounded vias should be used as barriers to isolate these signals from each other.

HEAT TRANSFER

Most of the heat generated by the LTC2261-14 is transferred from the die through the bottom-side exposed pad and package leads onto the printed circuit board. For good electrical and thermal performance, the exposed pad must be soldered to a large grounded pad on the PC board.

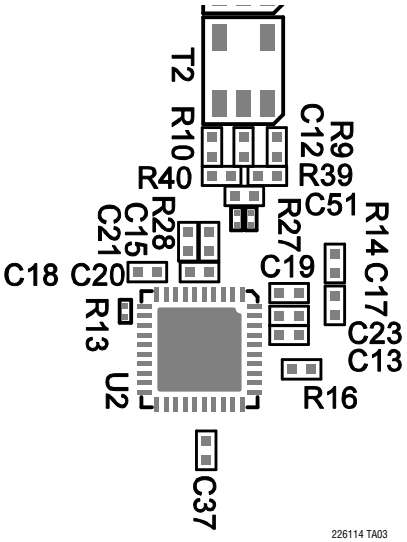
TYPICAL APPLICATIONS

LTC2261 Schematic



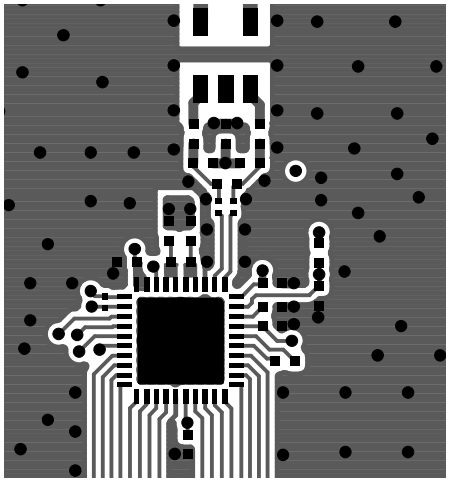
TYPICAL APPLICATIONS

Silkscreen Top



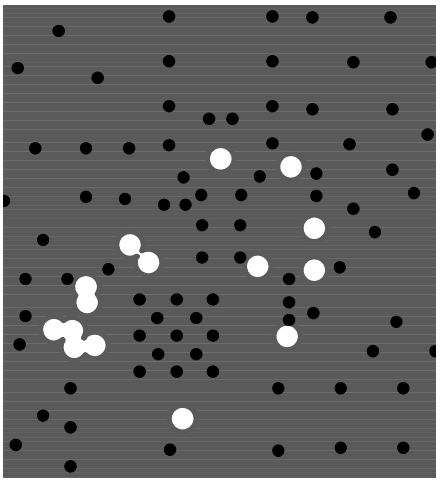
226114 TA03

Top Side



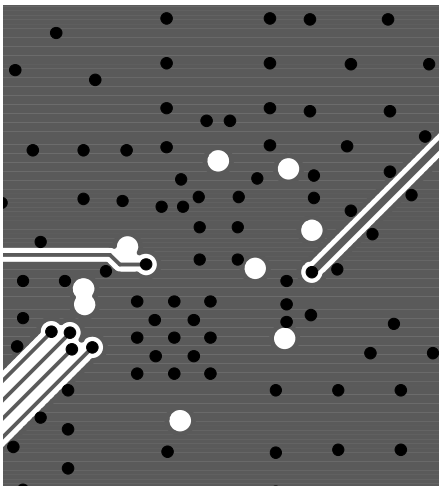
226114 TA04

Inner Layer 2 GND



226114 TA04

Inner Layer 3



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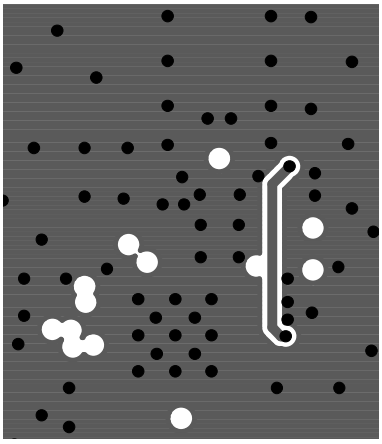
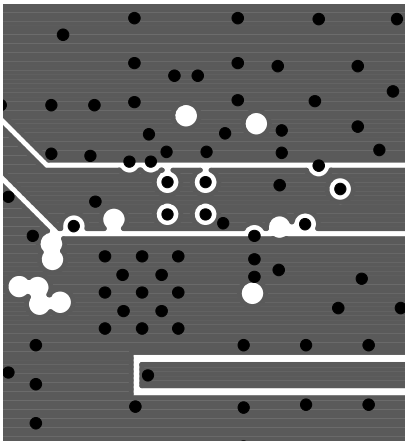
TYPICAL APPLICATIONS

Inner Layer 4



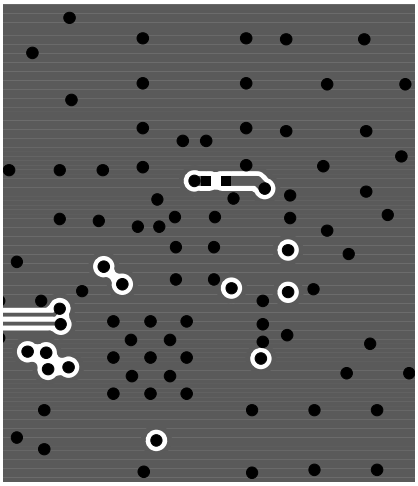
226114 TA07

Inner Layer 5 Power



226114 TA08

Bottom Side

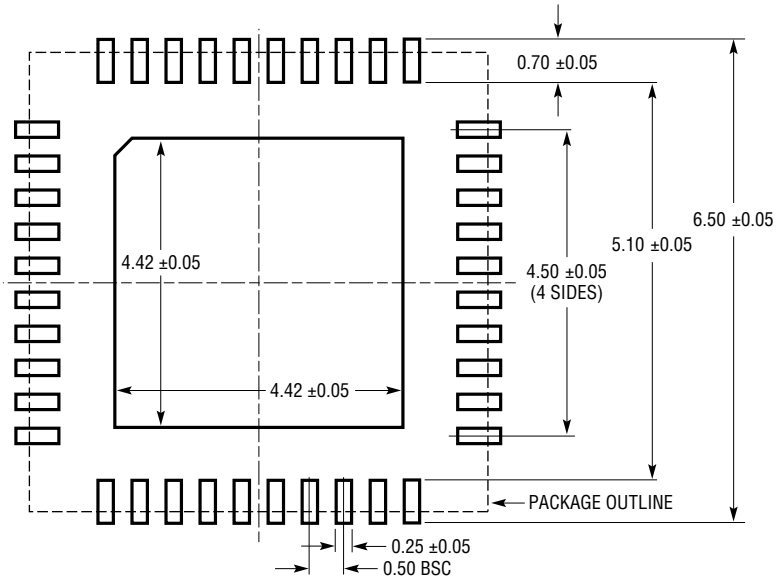


226114 TA09

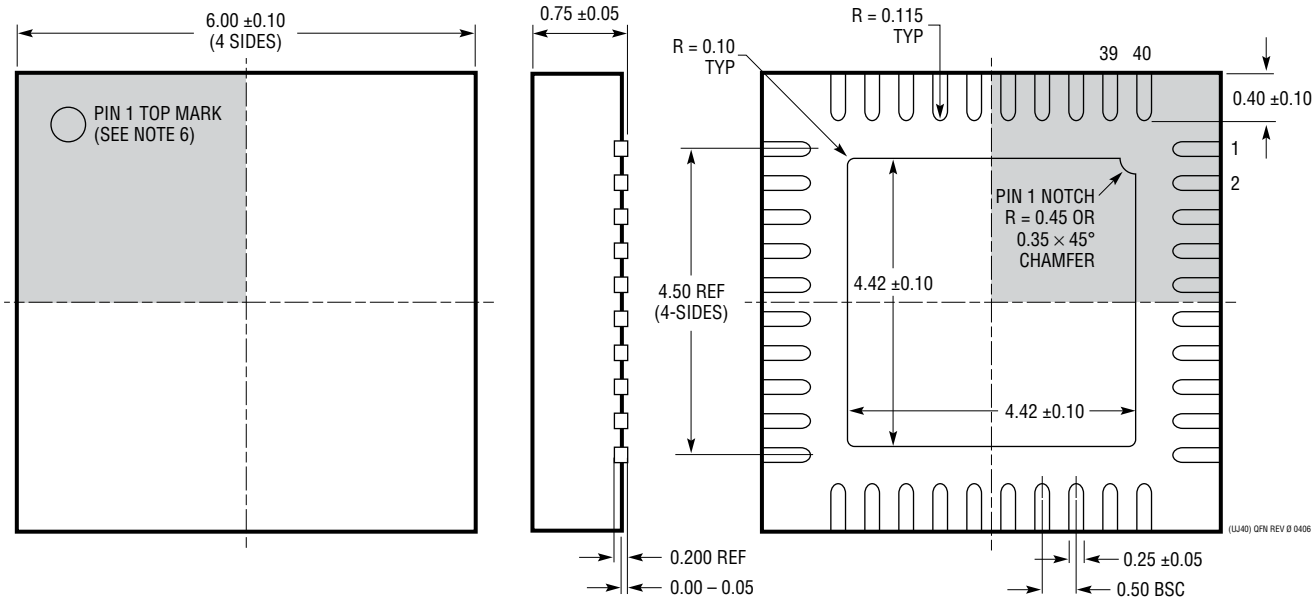
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

UJ Package
40-Lead Plastic QFN (6mm × 6mm)
(Reference LTC DWG # 05-08-1728 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS A JEDEC PACKAGE OUTLINE VARIATION OF (WJJD-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	08/12	Corrected IO_{VDD} to I_{OVDD}.	14
		Corrected RESET REGISTER A0, D7 description.	26
		Attached V_{DD} to pins 9,10 and 40 on schematic.	29
C	01/14	Corrected “external reference” to “internal reference” for 1V input range.	20