Dual 8A per Channel Low V_{IN} DC/DC µModule Regulator

FEATURES

- **Complete Dual DC/DC Regulator System**
- **Input Voltage Range: 2.7V to 5.5V**
- **Dual 8A Outputs, or Single 16A Output with a 0.6V to 5V Range**
- **Output Voltage Tracking and Margining**
- **±1.75% Total DC Output Error (–55°C to 125°C)**
- **Current Mode Control/Fast Transient Response**
- **Power Good Tracking and Margining**
- **Overcurrent/Thermal Shutdown Protection**
- **Onboard Frequency Synchronization**
- **Spread Spectrum Frequency Modulation**
- **Multiphase Operation**
- Selectable Burst Mode® Operation
- Output Overvoltage Protection
- SnPb (BGA) or RoHS Compliant (LGA and BGA) Finish
- Small Surface Mount Footprint, Low Profile (15mm × 15mm × 2.82mm) LGA and (15mm × 15mm × 3.42mm) BGA Packages

APPLICATIONS

- Telecom, Networking and Industrial Equipment
- Storage and ATCA, PCI Express Cards
- Battery Operated Equipment

DESCRIPTION

The LTM®4616 is a complete dual 2-phase 8A per channel switch mode DC/DC power regulator system in a 15mm × 15mm surface mount LGA or BGA package. Included in the package are the switching controller, power FETs, inductor and all support components. Operating from an input voltage range of 2.7V to 5.5V, the LTM4616 supports two outputs within a voltage range of 0.6V to 5V, each set by a single external resistor. This high efficiency design delivers up to 8A continuous current (10A peak) for each output. Only bulk input and output capacitors are needed, depending on ripple requirement. The part can also be configured for a 2-phase single output at up to 16A.

The low profile package enables utilization of unused space on the back side of PC boards for high density point-of-load regulation.

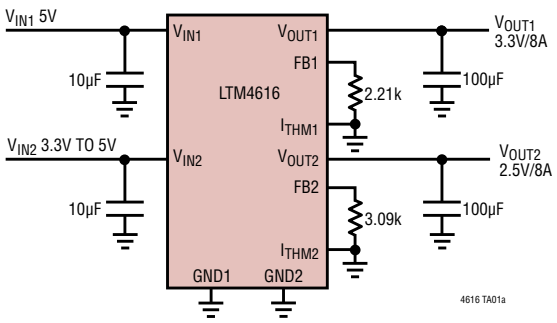
Fault protection features include overvoltage protection, overcurrent protection and thermal shutdown. The power module is offered in space saving and thermally enhanced 15mm × 15mm × 2.82mm LGA and 15mm × 15mm × 3.42mm BGA packages. The LTM4616 is available with SnPb (BGA) or RoHS compliant terminal finish.

Different Combinations of Input and Output

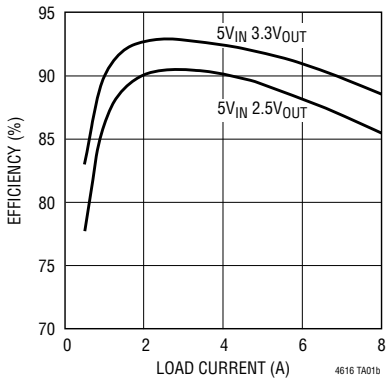
Number of Inputs	Number of Outputs	I_{OUT} (MAX)
2	2	8A, 8A
2	1	16A
1	2	8A, 8A
1	1	16A

TYPICAL APPLICATION

Dual Output DC/DC µModule® Regulator



Efficiency vs Load Current

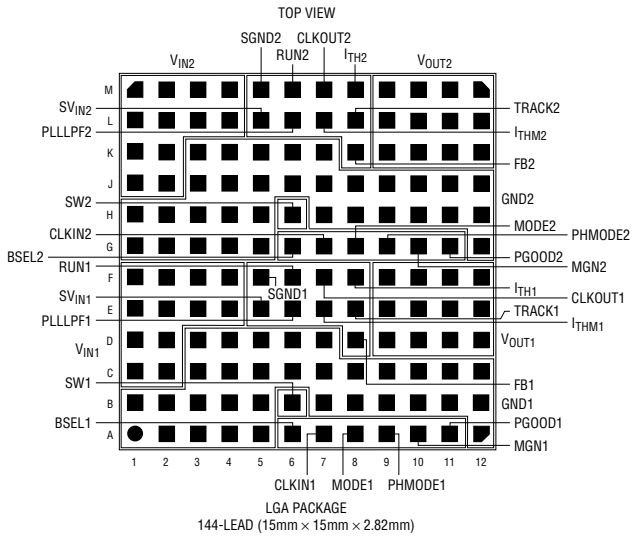


ABSOLUTE MAXIMUM RATINGS

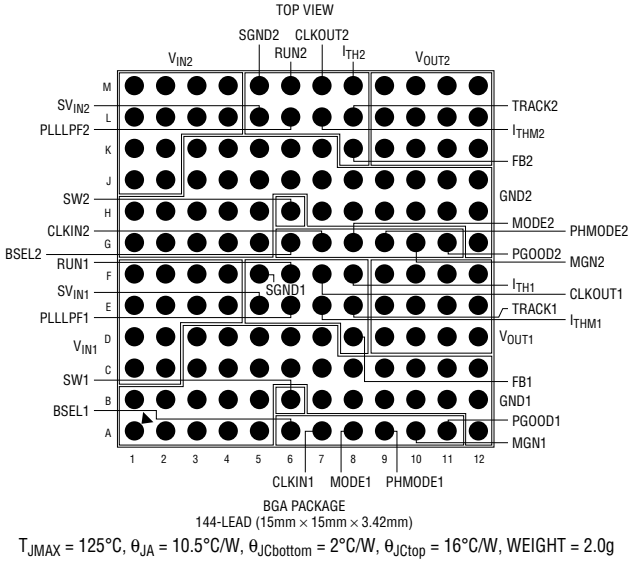
(Note 1)

V_{IN1}, SV_{IN1}, V_{IN2}, SV_{IN2} ..... –0.3V to 6V
CLKOUT1, CLKOUT2 ..... –0.3V to 2V
PGOOD1, PLLLPF1, CLKIN1, PHMODE1, MODE1, PGOOD2, PLLLPF2, CLKIN2, PHMODE2, MODE2 ..... –0.3V to V_{IN}
I_{TH1}, I_{THM1}, RUN1, FB1, TRACK1, MGN1, BSEL1, I_{TH2}, I_{THM2}, RUN2, FB2, TRACK2, MGN2, BSEL2 ..... –0.3V to V_{IN}
V_{OUT1}, V_{OUT2}, SW1, SW2 ..... –0.3V to V_{IN}
Internal Operating Temperature Range (Note 2)
E- and I-Grades ..... –40°C to 125°C
MP-Grade ..... –55°C to 125°C
Junction Temperature ..... 125°C
Storage Temperature Range ..... –55°C to 125°C

PIN CONFIGURATION



T_{JMAX} = 125°C, θ_{JA} = 10.5°C/W, $\theta_{JCbottom}$ = 2°C/W, θ_{JCtop} = 16°C/W, WEIGHT = 1.8g
θ_{JA} DERIVED FROM 95mm × 76mm PCB WITH 4 LAYERS



T_{JMAX} = 125°C, θ_{JA} = 10.5°C/W, $\theta_{JCbottom}$ = 2°C/W, θ_{JCtop} = 16°C/W, WEIGHT = 2.0g
θ_{JA} DERIVED FROM 95mm × 76mm PCB WITH 4 LAYERS

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING*		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (Note 2)
		DEVICE	FINISH CODE			
LTM4616EV#PBF	Au (RoHS)	LTM4616V	e4	LGA	3	–40°C to 125°C
LTM4616IV#PBF	Au (RoHS)	LTM4616V	e4	LGA	3	–40°C to 125°C
LTM4616MPV#PBF	Au (RoHS)	LTM4616V	e4	LGA	3	–55°C to 125°C
LTM4616EY#PBF	SAC305 (RoHS)	LTM4616Y	e1	BGA	3	–40°C to 125°C
LTM4616IY#PBF	SAC305 (RoHS)	LTM4616Y	e1	BGA	3	–40°C to 125°C
LTM4616IY	SnPb (63/37)	LTM4616Y	e0	BGA	3	–40°C to 125°C
LTM4616MPY#PBF	SAC305 (RoHS)	LTM4616Y	e1	BGA	3	–55°C to 125°C
LTM4616MPY	SnPb (63/37)	LTM4616Y	e0	BGA	3	–55°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Pb-free and Non-Pb-free Part Markings: www.linear.com/leadfree
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures: www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings: www.linear.com/packaging

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). T_A = 25°C, V_{IN} = 5V unless otherwise noted. Per the typical application in Figure 18. Specified as each channel (Note 3).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN1(DC)}$, $V_{IN2(DC)}$	Input DC Voltage		●	2.7		5.5	V
$V_{OUT1(DC)}$, $V_{OUT2(DC)}$	Output Voltage, Total Variation with Line and Load	C_{IN} = 10µF × 1, C_{OUT} = 100µF Ceramic, 100µF POSCAP, R_{FB} = 6.65k, MODE = 0V		1.472	1.49	1.508	V
		V_{IN} = 2.7V to 5.5V, I_{OUT} = $I_{OUT(DC)MIN}$ to $I_{OUT(DC)MAX}$ (Note 4)	●	1.464	1.49	1.516	V
Input Specifications							
$V_{IN1(UVLO)}$, $V_{IN2(UVLO)}$	Undervoltage Lockout Threshold	SV_{IN} Rising		2.05	2.2	2.35	V
		SV_{IN} Falling		1.85	2.0	2.15	V
$I_{Q(VIN1, VIN2)}$	Input Supply Bias Current	V_{IN} = 3.3V, V_{OUT} = 1.5V, No Switching, MODE = V_{IN}			400		µA
		V_{IN} = 3.3V, V_{OUT} = 1.5V, No Switching, MODE = 0V			1.15		mA
		V_{IN} = 3.3V, V_{OUT} = 1.5V, Switching Continuous			55		mA
		V_{IN} = 5V, V_{OUT} = 1.5V, No Switching, MODE = V_{IN}			450		µA
		V_{IN} = 5V, V_{OUT} = 1.5V, No Switching, MODE = 0V			1.3		mA
		V_{IN} = 5V, V_{OUT} = 1.5V, Switching Continuous			75		mA
		Shutdown, RUN = 0, V_{IN} = 5V			1		µA
$I_{S(VIN1, VIN2)}$	Input Supply Current	V_{IN} = 3.3V, V_{OUT} = 1.5V, I_{OUT} = 8A			4.5		A
		V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 8A			2.93		A
Output Specifications							
$I_{OUT1(DC)}$, $I_{OUT2(DC)}$	Output Continuous Current Range	V_{OUT} = 1.5V (Note 4)					
		V_{IN} = 3.3V, 5.5V		0		8	A
		V_{IN} = 2.7V		0		5	A
$\Delta V_{OUT1(LINE)}/V_{OUT1}$ $\Delta V_{OUT2(LINE)}/V_{OUT2}$	Line Regulation Accuracy	V_{OUT} = 1.5V, V_{IN} from 2.7V to 5.5V, I_{OUT} = 0A	●		0.1	0.25	%/V
$\Delta V_{OUT1(LOAD)}/V_{OUT1}$ $\Delta V_{OUT2(LOAD)}/V_{OUT2}$	Load Regulation Accuracy	V_{OUT} = 1.5V (Note 4)					
		V_{IN} = 3.3V, 5.5V, I_{LOAD} = 0A to 8A	●		0.3	0.5	%
		V_{IN} = 2.7V, I_{LOAD} = 0A to 5A	●		0.3	0.5	%
$V_{OUT1(AC)}$, $V_{OUT2(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 100µF X5R Ceramic, V_{IN} = 5V, V_{OUT} = 1.5V			10		mV_{P-P}
f_{S1}, f_{S2}	Switching Frequency	I_{OUT} = 8A, V_{IN} = 5V, V_{OUT} = 1.5V		1.25	1.5	1.75	MHz
f_{SYNC1}, f_{SYNC2}	SYNC Capture Range			0.75		2.25	MHz
$\Delta V_{OUT1(START)}$, $\Delta V_{OUT2(START)}$	Turn-On Overshoot	C_{OUT} = 100µF, V_{OUT} = 1.5V, I_{OUT} = 0A					
		V_{IN} = 3.3V			10		mV
		V_{IN} = 5V			10		mV
t_{START1}, t_{START2}	Turn-On Time	C_{OUT} = 100µF, V_{OUT} = 1.5V, V_{IN} = 5V, I_{OUT} = 1A Resistive Load, Track = V_{IN}			100		µs
$\Delta V_{OUT1(LS)}$, $\Delta V_{OUT2(LS)}$	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 100µF Ceramic x2, 470µF POSCAP, V_{IN} = 5V, V_{OUT} = 1.5V			20		mV
$t_{SETTLE1}$, $t_{SETTLE2}$	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load, V_{IN} = 5V, V_{OUT} = 1.5V, C_{OUT} = 100µF			10		µs
$I_{OUT1(PK)}$, $I_{OUT2(PK)}$	Output Current Limit	C_{OUT} = 100µF					
		V_{IN} = 2.7V, V_{OUT} = 1.5V			8		A
		V_{IN} = 3.3V, V_{OUT} = 1.5V			11		A
		V_{IN} = 5V, V_{OUT} = 1.5V			13		A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range (Note 2). T_A = 25°C, V_{IN} = 5V unless otherwise noted. Per the typical application in Figure 18. Specified as each channel (Note 3).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Control Section							
FB1, FB2	Voltage at FB Pin	I_{OUT} = 0A, V_{OUT} = 1.5V, V_{IN} = 2.7V to 5.5V	 ●	0.590 0.587	0.596 0.596	0.602 0.606	V V
SS Delay	Internal Soft-Start Delay				90		µs
I_{FB1}, I_{FB2}					0.2		µA
V_{RUN1}, V_{RUN2}	RUN Pin On/Off Threshold	RUN Rising RUN Falling		1.4 1.3	1.55 1.4	1.7 1.5	V V
TRACK1, TRACK2	Tracking Threshold (Rising) Tracking Threshold (Falling) Tracking Disable Threshold	RUN = V_{IN} RUN = 0V			0.57 0.18 V_{IN} – 0.5		V V V
R_{FBHI1}, R_{FBHI2}	Resistor Between V_{OUT} and FB Pins			9.95	10	10.05	kΩ
ΔV_{PGOOD1}, ΔV_{PGOOD2}	PGOOD Range				±10		%
I_{PGOOD1}, I_{PGOOD2}	PGOOD Leakage Current	V_{PGOOD} = V_{IN} = 2.7V to 5.5V, I_{OUT} = $I_{OUT(DC)MAX}$ (Note 4)	●		20	30	µA
V_{PGL1}, V_{PGL2}	PGOOD Voltage Low	I_{PGOOD} = 5mA			0.2	0.4	V
%Margining	Output Voltage Margining Percentage	MGN = V_{IN}, BSEL = 0V MGN = V_{IN}, BSEL = V_{IN} MGN = V_{IN}, BSEL = Float MGN = 0V, BSEL = 0V MGN = 0V, BSEL = V_{IN} MGN = 0V, BSEL = Float		4 9 14 –4 –9 –14	5 10 15 –5 –10 –15	6 11 16 –6 –11 –16	% % % % % %

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

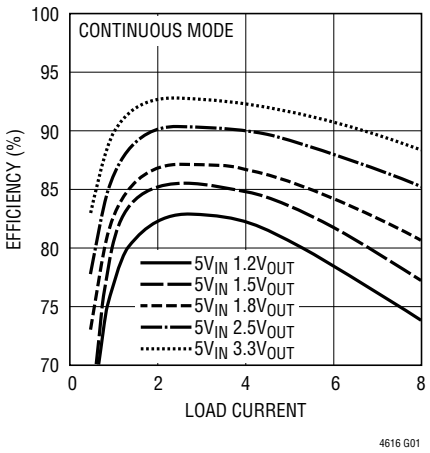
Note 2: The LTM4616 is tested under pulsed load conditions, such that $T_J \approx T_A$. The LTM4616E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4616I is guaranteed to meet specifications over the –40°C to 125°C internal operating temperature range. The LTM4616MP is guaranteed and tested over the –55°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: Two channels are tested separately and the same testing conditions are applied to each channel.

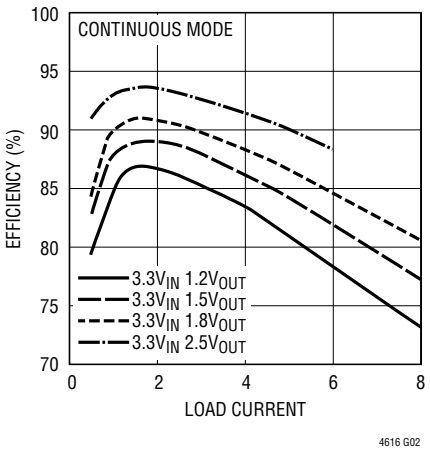
Note 4: See Output Current Derating curves for different V_{IN}, V_{OUT} and T_A.

TYPICAL PERFORMANCE CHARACTERISTICS Specified as Each Channel

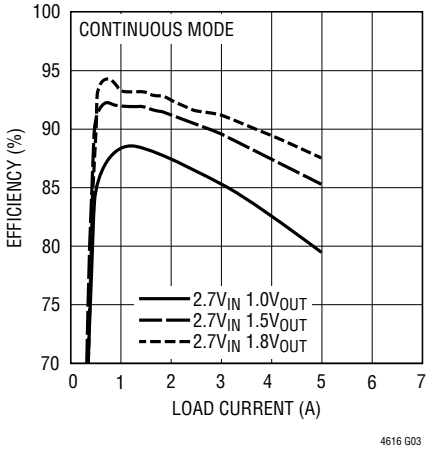
Efficiency vs Load Current



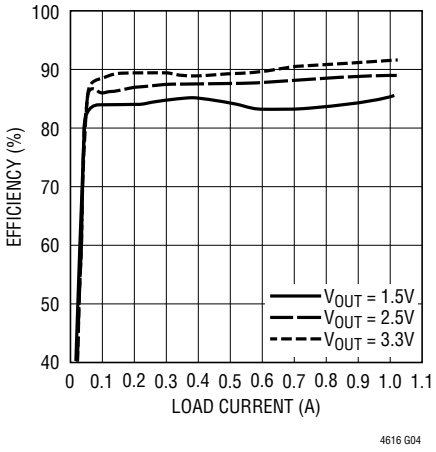
Efficiency vs Load Current



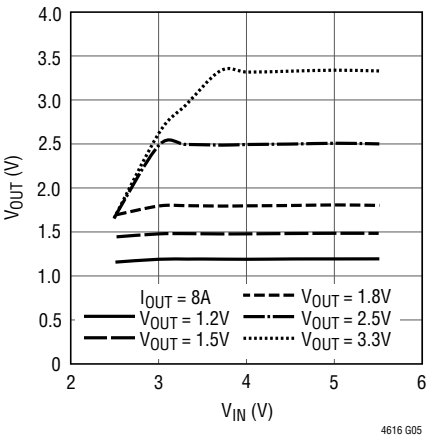
Efficiency vs Load Current



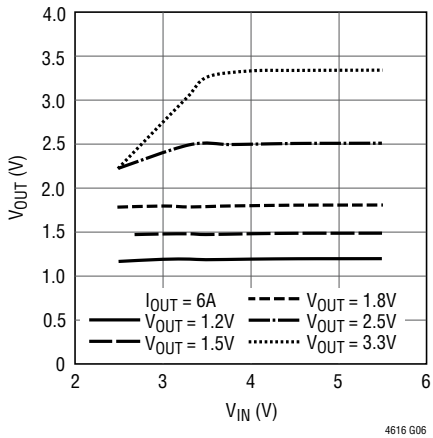
Burst Mode Efficiency with 5V Input



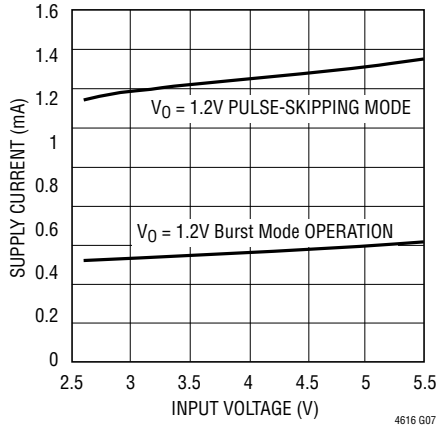
V_{IN} to V_{OUT} Step-Down Ratio



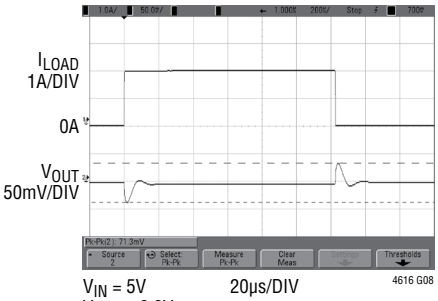
V_{IN} to V_{OUT} Step-Down Ratio



Supply Current vs V_{IN}

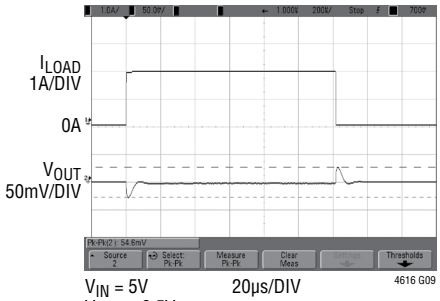


Load Transient Response



V_{IN} = 5V 20µs/DIV
V_{OUT} = 3.3V
2A/µs STEP
C_{OUT} = 2 × 100µF X5R, 470µF 4V POSCAP

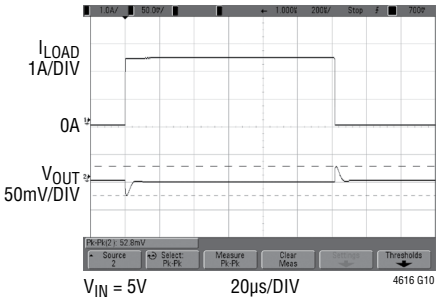
Load Transient Response



V_{IN} = 5V 20µs/DIV
V_{OUT} = 2.5V
2A/µs STEP
C_{OUT} = 2 × 100µF X5R, 470µF 4V POSCAP

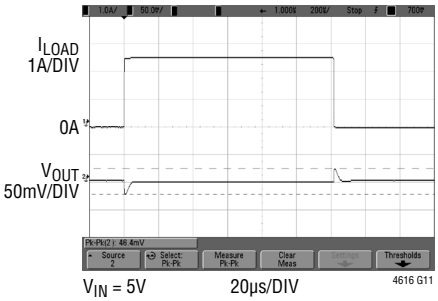
TYPICAL PERFORMANCE CHARACTERISTICS Specified as Each Channel

Load Transient Response



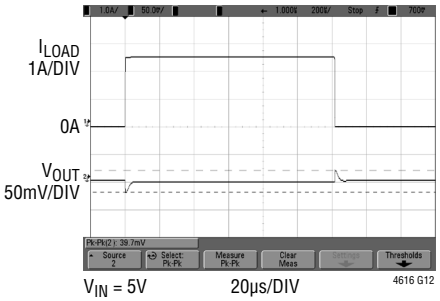
V_{IN} = 5V 20µs/DIV
V_{OUT} = 1.8V
2.5A/µs STEP
C_{OUT} = 2 × 100µF X5R, 470µF 4V POSCAP

Load Transient Response



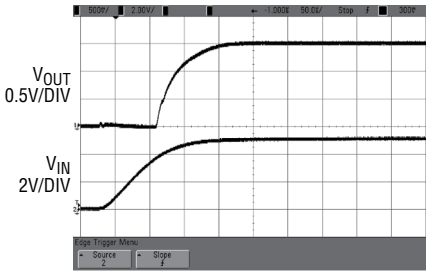
V_{IN} = 5V 20µs/DIV
V_{OUT} = 1.5V
2.5A/µs STEP
C_{OUT} = 2 × 100µF X5R, 470µF 4V POSCAP

Load Transient Response



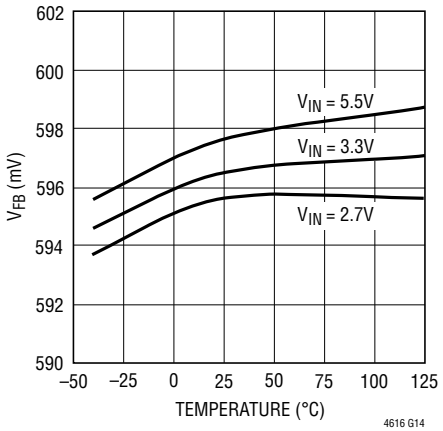
V_{IN} = 5V 20µs/DIV
V_{OUT} = 1.2V
2.5A/µs STEP
C_{OUT} = 2 × 100µF X5R, 470µF POSCAP

Start-Up

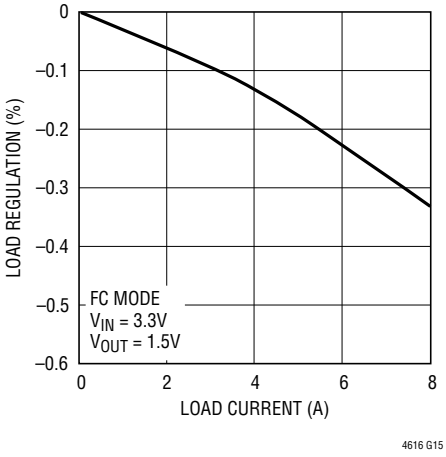


V_{IN} = 5V 50µs/DIV
V_{OUT} = 1.5V
C_{OUT} = 100µF NO LOAD AND 8A LOAD
(DEFAULT 100µs SOFT-START)

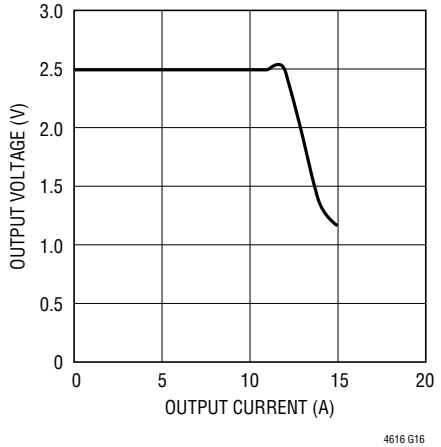
V_{FB} vs Temperature



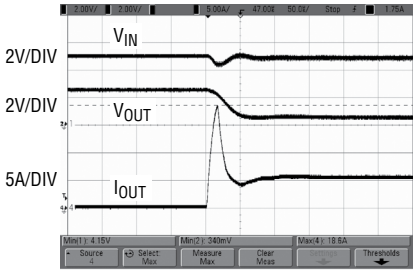
Load Regulation vs Current



2.5V Output Current

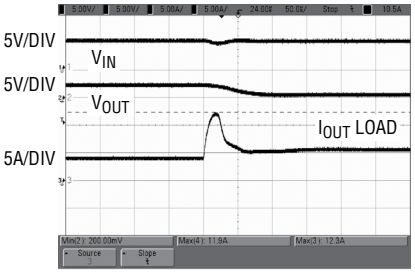


Short-Circuit Protection (2.5V Short, No Load)



V_{IN} = 5V 50µs/DIV
V_{OUT} = 2.5V

Short-Circuit Protection (2.5V Short, 4A Load)



V_{IN} = 5V 50µs/DIV
V_{OUT} = 2.5V

PIN FUNCTIONS

V_{IN1}, V_{IN2}, (BANK1 and BANK2); (F1-F4, E1-E4, C1-C2, D1-D2) and (J1-J2, K1-K2, L1-L4, M1-M4): Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and GND pins.

V_{OUT1}, V_{OUT2} (BANK3 and BANK6); (D9-D12, E9-E12, F9-F12) and (K9-K12, L9-L12, M9-M12): Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. See Table 1.

GND1 and GND2 (BANK2 and BANK5); (A1-A5, A12, B1-B5, B7-B12, C3-C12, D3-D7) and (G1-G5, G12, H1-H5, H7-H12, J3-J12, K3-K7): Power Ground Pins for Both Input and Output Returns.

SV_{IN1} and SV_{IN2} (E5 and L5): Signal Input Voltage for Each Channel. This pin is internally connected to V_{IN} through a lowpass filter.

SGND1 and SGND2 (F5 and M5): Signal Ground Pin for Each Channel. Return ground path for all analog and low power circuitry. Tie a single connection to the output capacitor GND in the application. See layout guidelines in Figure 17.

MODE1 and MODE2 (A8 and G8): Mode Select Input for Each Channel. Tying this pin high enables Burst Mode operation. Tying this pin low enables forced continuous operation. Floating this pin or tying it to $V_{IN}/2$ enables pulse-skipping operation.

CLKIN1 and CLKIN2 (A7 and G7): External Synchronization Input to Phase Detector for Each Channel. This pin is internally terminated to SGND with a 50k resistor. The phase-locked loop will force the internal top power PMOS turn on to be synchronized with the rising edge of the CLKIN signal. Connect this pin to SV_{IN} to enable spread spectrum modulation. During external synchronization, make sure the PLLLPF pin is not tied to V_{IN} or GND.

PLLLPF1 and PLLLPF2 (E6 and L6): Phase-Locked Loop Lowpass Filter for Each Channel. An internal lowpass filter is tied to this pin. In spread spectrum mode, placing a capacitor here to SGND controls the slew rate from one frequency to the next. Alternatively, floating this pin allows normal running frequency at 1.5MHz, tying this pin to SV_{IN} forces the part to run at 1.33 times its normal frequency (2MHz), tying it to ground forces the frequency to run at 0.67 times its normal frequency (1MHz).

PHMODE1 and PHMODE2 (A9 and G9): Phase Selector Input for Each Channel. This pin determines the phase relationship between the internal oscillator and CLKOUT. Tie it high for 2-phase operation, tie it low for 3-phase operation, and float or tie it to $V_{IN}/2$ for 4-phase operation.

MGN1 and MGN2 (A10 and G10): Voltage Margining Pin for Each Channel. Increases or decreases the output voltage by the amount specified by the BSEL pin. To disable margining, tie the MGN pin to a voltage divider with 50k resistors from V_{IN} to ground (see Figure 5). For margining, connect a voltage divider from V_{IN} to GND with the center point connected to the MGN pin for the specific channel. Each resistor should be close to 50k. Margin High is within 0.3V of V_{IN}, and Margin Low is within 0.3V of GND. See the Applications Information section and Figure 18 for margining control. The specified tri-state drivers are capable of the high and low requirements for margining.

BSEL1 and BSEL2 (A6 and G6): Margining Bit Select Pin for Each Channel. Tying BSEL low selects ±5% margin value, tying it high selects 10% margin value. Floating it or tying it to $V_{IN}/2$ selects 15% margin value.

TRACK1 and TRACK2 (E8 and L8): Output Voltage Tracking Pin for Each Channel. Voltage tracking is enabled when the TRACK voltage is below 0.57V. If tracking is not desired, then connect the TRACK pin to SV_{IN}. If TRACK is not tied to SV_{IN}, then the TRACK pin's voltage needs to be below 0.18V before the chip shuts down even though RUN is

PIN FUNCTIONS

already low. Do not float this pin. A resistor and capacitor can be applied to the TRACK pin to increase the soft-start time of the regulator. TRACK1 and TRACK2 can be tied together for parallel operation and tracking. See the Applications Information section.

FB1 and FB2 (D8 and K8): The Negative Input of the Error Amplifier for Each Channel. Internally, this pin is connected to V_{OUT} with a 10k precision resistor. Different output voltages can be programmed with an additional resistor between FB and GND pins. In PolyPhase® operation, tying the FB pins together allows for parallel operation. See the Applications Information section for details.

I_{TH1} and I_{TH2} (F8 and M8): Current Control Threshold and Error Amplifier Compensation Point for Each Channel. The current comparator threshold increases with this control voltage. Tie together in parallel operation.

I_{THM1} and I_{THM2} (E7 and L7): Negative Input to the Internal I_{TH} Differential Amplifier for Each Channel. Tie this pin to SGND for single phase operation on each channel. For PolyPhase operation, tie the master's I_{THM} to SGND while connecting all of the I_{THM} pins together at the master.

PGOOD1 and PGOOD2 (A11 and G11): Output Voltage Power Good Indicator for Each Channel. Open-drain logic output that is pulled to ground when the output voltage is not within ±10% of the regulation point. Power good is disabled during margining.

RUN1 and RUN2 (F6 and M6): Run Control Pin. A voltage above 1.7V will turn on the module.

SW1 and SW2 (B6 and H6): Switching Node of Each Channel That is Used for Testing Purposes. This can be connected to an electronically open circuit copper pad on the board for improved thermal performance.

CLKOUT1 and CLKOUT2 (F7 and M7): Output Clock Signal for PolyPhase Operation. The phase of CLKOUT is determined by the state of the PHMODE pin.

SIMPLIFIED BLOCK DIAGRAM

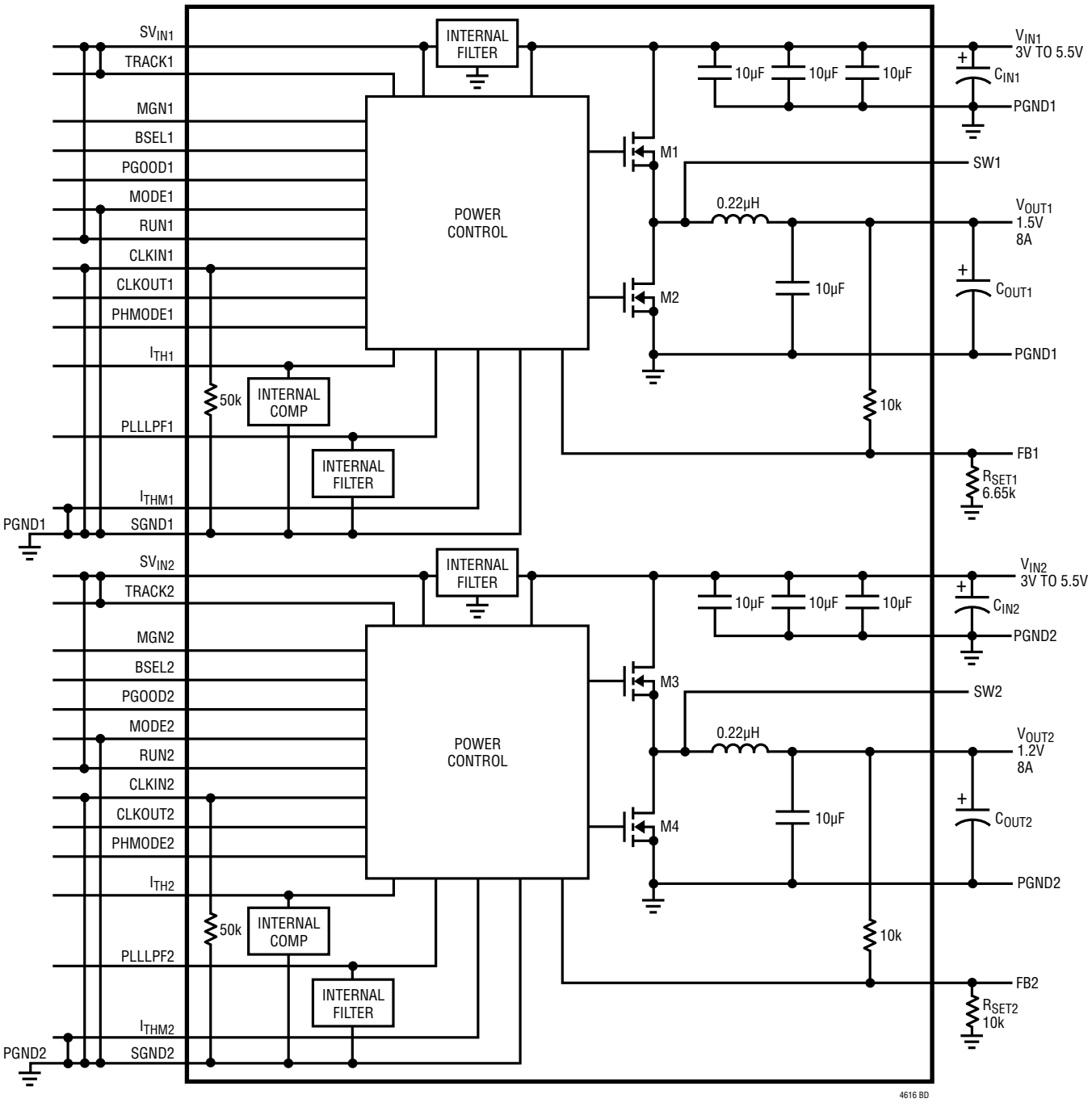


Figure 1. Simplified LTM4616 Block Diagram

SIMPLIFIED BLOCK DIAGRAM

Table 1. Decoupling Requirements. T_A = 25°C, Block Diagram Configuration.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN1} C_{IN2}	External Input Capacitor Requirement (V_{IN1} = 2.7V to 5.5V, V_{OUT1} = 1.5V) (V_{IN2} = 2.7V to 5.5V, V_{OUT2} = 2.5V)	 I_{OUT1} = 8A I_{OUT2} = 8A		 22 22		 µF µF
C_{OUT1} C_{OUT2}	External Output Capacitor Requirement (V_{IN1} = 2.7V to 5.5V, V_{OUT1} = 1.5V) (V_{IN2} = 2.7V to 5.5V, V_{OUT2} = 2.5V)	 I_{OUT1} = 8A I_{OUT2} = 8A		 100 100		 µF µF

OPERATION

The LTM4616 is a dual-output standalone nonisolated switching mode DC/DC power supply. It can provide two 8A outputs with few external input and output capacitors. This module provides precisely regulated output voltages programmable via external resistors from $0.6V_{DC}$ to $5V_{DC}$ over 2.7V to 5.5V input voltages. The typical application schematic is shown in Figure 18.

The LTM4616 has integrated constant frequency current mode regulators and built-in power MOSFET devices with fast switching speed. The typical switching frequency is 1.5MHz. For switching noise sensitive applications, it can be externally synchronized from 0.75MHz to 2.25MHz. Even spread spectrum switching can be implemented in the design to reduce noise.

With current mode control and internal feedback loop compensation, the LTM4616 module has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limit and thermal shutdown in an overcurrent condition. Internal overvoltage and undervoltage comparators pull the open-drain PGOOD output low if the output feedback voltage exits a ±10% window around the regulation point. The power good pins are disabled during margining.

Pulling the RUN pins below 1.3V forces the regulators into a shutdown state, by turning off both MOSFETs. The TRACK pin is used for programming the output voltage ramp and voltage tracking during start-up. See the Applications Information section.

The LTM4616 is internally compensated to be stable over all operating conditions. Table 3 provides a guideline for input and output capacitances for several operating conditions. LTpowerCAD™ design tool is available for fine tuning transient and stability performance. The FB pin is used to program the output voltage with a single external resistor to ground.

Multiphase operation can be easily employed with the synchronization and phase mode controls. The LTM4616 has clock in and clock out for poly phasing multiple devices or frequency synchronization.

High efficiency at light loads can be accomplished with selectable Burst Mode operation using the MODE pin. These light load features will accommodate battery operation. Efficiency graphs are provided for light load operation in the Typical Performance Characteristics section.

Output voltage margining is supported, and can be programed from ±5% to ±15% using the MGN and BSEL pins.

APPLICATIONS INFORMATION

The typical LTM4616 application circuit is shown in Figure 18. External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 3 for specific external capacitor requirements for a particular application.

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the maximum V_{IN} to V_{OUT} step-down ratio that can be achieved for a given input voltage. Each output of the LTM4616 is capable of 100% duty cycle, but the V_{IN} to V_{OUT} minimum drop out is still shown as a function of its load current. For a 5V input voltage, both outputs can deliver 8A for any output voltage. For a 3.3V input, all outputs can deliver 8A, except 2.5V_{OUT} and above which is limited to 6A. All outputs derived from a 2.7V input voltage are limited to 5A.

Output Voltage Programming

Each PWM controller has an internal 0.596V reference voltage. As shown in the Block Diagram, a 10k internal feedback resistor connects V_{OUT} and FB pins together. The output voltage will default to 0.596V with no feedback resistor. Adding a resistor R_{FB} from FB pin to GND programs the output voltage:

$$V_{OUT} = 0.596V \bullet \frac{10k + R_{FB}}{R_{FB}}$$

Table 2. FB Resistor vs Various Output Voltages

V_{OUT}	0.596V	1.2V	1.5V	1.8V	2.5V	3.3V
R_{FB}	Open	10k	6.65k	4.87k	3.09k	2.21k

For parallel operation of N number of outputs, the below equation can be used to solve for R_{FB}. Tie the FB pins together for each paralleled output with a single resistor to ground as determined by:

$$R_{FB} = \frac{10k / N}{\frac{V_{OUT}}{0.596} - 1}$$

Input Capacitors

The LTM4616 module should be connected to a low AC impedance DC source. For each regulator, three 10µF ceramic capacitors are included inside the module. Additional input capacitors are only needed if a large load step is required up to the 4A level. A 47µF to 100µF surface mount aluminum electrolytic bulk capacitor can be used for more input bulk capacitance. This bulk input capacitor is only needed if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. If low impedance power planes are used, then this 47µF capacitor is not needed.

For a buck converter, the switching duty-cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor current ripple, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1-D)}$$

In the above equation, η% is the estimated efficiency of the power module so the RMS input current at the worst case for 8A maximum current is about 4A. The input bulk capacitor can be a switcher-rated aluminum electrolytic capacitor or polymer capacitor. Each internal 10µF ceramic input capacitor is typically rated for 2 amps of RMS ripple current.

Output Capacitors

The LTM4616 is designed for low output voltage ripple noise. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be a low ESR tantalum capacitor, low ESR polymer capacitor or ceramic capacitor. The typical output capacitance range is from 47µF to 220µF. Additional output filtering may be required by the system designer, if further reduction of output ripple or dynamic transient spikes is desired. Table 3 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 3A/µs transient. The table optimizes total equivalent ESR and total bulk capacitance to optimize the transient performance. Stability criteria are considered in the Table 3 matrix. LTpowerCAD is available

APPLICATIONS INFORMATION

Table 3. Output Voltage Response Versus Component Matrix (Refer to Figure 18) 0A to 3A Load Step

TYPICAL MEASURED VALUES

C_{OUT1} VENDORS	VALUE	PART NUMBER	C_{OUT2} VENDORS	VALUE	PART NUMBER
TDK	22µF, 6.3V	C3216X7S0J226M	Sanyo POSCAP	470µF, 4V	4TPE470M
Murata	22µF, 16V	GRM31CR61C226K	C_{IN} (BULK) VENDORS	VALUE	PART NUMBER
TDK	100µF, 6.3V	C4532X5R0J107MZ	SUNCON	100µF, 10V	10CE100FH
Murata	100µF, 6.3V	GRM32ER60J107M			

V_{OUT} (V)	C_{IN} (CERAMIC)	C_{IN} (BULK)*	C_{OUT1} (CERAMIC)	C_{OUT2} (BULK)	I_{TH}	C1	C3	V_{IN} (V)	DROOP (mV)	PEAK-TO- PEAK DEVIATION (mV)	RECOVERY TIME (µs)	LOAD STEP (A/µs)	R_{FB} (kΩ)
1.0	10µF	100µF	100µF × 2	470µF	None	None	None	5	20	40	40	2.5	14.7
1.0	10µF	100µF	100µF × 2		None	None	None	5	30	60	25	2.5	14.7
1.0	10µF	100µF	100µF × 2		None	None	None	2.7	30	60	25	2.5	14.7
1.0	10µF	100µF	22µF × 1	470µF	None	None	None	2.7	25	50	25	2.5	14.7
1.2	10µF	100µF	100µF × 2		None	None	None	5	20	40	25	2.5	10
1.2	10µF	100µF	22µF × 1	470µF	None	None	None	5	20	41	25	2.5	10
1.2	10µF	100µF	100µF × 2		None	None	None	2.7	30	60	20	2.5	10
1.2	10µF	100µF	22µF × 1	470µF	None	None	None	2.7	30	60	25	2.5	10
1.5	10µF	100µF	100µF × 2		None	None	None	5	32	64	20	2.5	6.65
1.5	10µF	100µF	22µF × 1	470µF	None	None	None	5	25	50	25	2.5	6.65
1.5	10µF	100µF	100µF × 1		None	None	None	3.3	22	42	25	2.5	6.65
1.5	10µF	100µF	22µF × 1	470µF	None	None	None	3.3	25	50	25	2.5	6.65
1.5	10µF	100µF	100µF × 2		None	None	None	2.7	30	60	25	2.5	6.65
1.5	10µF	100µF	22µF × 1	470µF	None	None	None	2.7	25	50	25	2.5	6.65
1.8	10µF	100µF	100µF × 1		None	None	None	5	42	80	25	2.5	4.87
1.8	10µF	100µF	22µF × 1	470µF	None	None	None	5	25	50	30	2.5	4.87
1.8	10µF	100µF	100µF × 2		None	None	None	3.3	35	70	30	2.5	4.87
1.8	10µF	100µF	22µF × 1	470µF	None	None	None	3.3	25	50	30	2.5	4.87
1.8	10µF	100µF	100µF × 2		None	None	None	2.7	35	70	30	2.5	4.87
1.8	10µF	100µF	22µF × 1	470µF	None	None	None	2.7	35	20	30	2.5	4.87
2.5	10µF	100µF	100µF × 1		None	None	None	5	35	40	30	2.5	3.09
2.5	10µF	100µF	22µF × 1	470µF	None	None	None	5	32	65	40	2.5	3.09
2.5	10µF	100µF	100µF × 1		None	None	None	3.3	50	100	30	2.5	3.09
2.5	10µF	100µF	22µF × 1	470µF	None	None	None	3.3	32	65	40	2.5	3.09
3.3	10µF	100µF	100µF × 1		None	None	None	5	65	135	30	2.5	2.21
3.3	10µF	100µF	22µF × 1	470µF	None	None	None	5	40	87	40	2.5	2.21

*Bulk capacitance is optional if V_{IN} has very low input impedance.

for those who wish to perform additional stability analysis. Multiphase operation will reduce effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance will be more a function of stability and transient response. LTpowerCAD also calculates the output ripple reduction as the number of phases increases.

Burst Mode Operation

The LTM4616 is capable of Burst Mode operation on each regulator in which the power MOSFETs operate intermittently based on load demand, thus saving quiescent current. For applications where maximizing the efficiency at very light loads is a high priority, Burst Mode operation should be applied. To enable Burst Mode operation, simply tie the MODE pin to V_{IN}. During this operation, the peak current of the inductor is set to approximately 20% of the maximum

APPLICATIONS INFORMATION

peak current value in normal operation even though the voltage at the I_{TH} pin indicates a lower value. The voltage at the I_{TH} pin drops when the inductor's average current is greater than the load requirement. As the I_{TH} voltage drops below 0.2V, the BURST comparator trips, causing the internal sleep line to go high and turn off both power MOSFETs.

In Burst Mode operation, the internal circuitry is partially turned off, reducing the quiescent current to about 450µA for each output. The load current is now being supplied from the output capacitors. When the output voltage drops, causing I_{TH} to rise above 0.25V, the internal sleep line goes low, and the LTM4616 resumes normal operation. The next oscillator cycle will turn on the top power MOSFET and the switching cycle repeats. Each regulator can be configured for Burst Mode operation.

Pulse-Skipping Mode Operation

In applications where low output ripple and high efficiency at intermediate currents are desired, pulse-skipping mode should be used. Pulse-skipping operation allows the LTM4616 to skip cycles at low output loads, thus increasing efficiency by reducing switching loss. Floating the MODE pin or tying it to $V_{IN}/2$ enables pulse-skipping operation. This allows discontinuous conduction mode (DCM) operation down to near the limit defined by the chip's minimum on-time (about 100ns). Below this output current level, the converter will begin to skip cycles in order to maintain output regulation. Increasing the output load current slightly, above the minimum required for discontinuous conduction mode, allows constant frequency PWM. Each regulator can be configured for pulse-skipping mode.

Forced Continuous Operation

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous operation should be used. Forced continuous operation can be enabled by tying the MODE pin to GND. In this mode, inductor current is allowed to reverse during low output loads, the I_{TH} voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse. During start-up, forced continuous mode is disabled and inductor current is prevented from reversing until the LTM4616's output voltage is in regulation. Each regulator can be configured for forced continuous mode.

Multiphase Operation

For output loads that demand more than 8A of current, two outputs in LTM4616 or even multiple LTM4616s can be cascaded to run out-of-phase to provide more output current without increasing input and output voltage ripple. The CLKIN pin allows the LTC®4616 to synchronize to an external clock (between 0.75MHz and 2.25MHz) and the internal phase-locked loop allows the LTM4616 to lock onto CLKIN's phase as well. The CLKOUT signal can be connected to the CLKIN pin of the following LTM4616 stage to line up both the frequency and the phase of the entire system. Tying the PHMODE pin to SV_{IN}, SGND or $SV_{IN}/2$ (floating) generates a phase difference (between CLKIN and CLKOUT) of 180°, 120° or 90° respectively, which corresponds to a 2-phase, 3-phase or 4-phase operation. For a 6-phase example in Figure 2, the 2nd stage that is 120° out-of-phase from the 1st stage can generate a 240° (PHMODE = 0) CLKOUT signal for the 3rd stage, which then can generate a CLKOUT signal that's 420°, or 60° (PHMODE = SV_{IN}) for the 4th stage. With the 60° CLKIN input, the next two stages can shift 120° (PHMODE = 0) for each to generate a 300° signal for the 6th stage. Finally, the signal with a 60° phase shift on the 6th stage (PHMODE is floating) goes back to the 1st stage. Figure 3 shows the configuration for 12-phase operation.

A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is reduced by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used.

APPLICATIONS INFORMATION

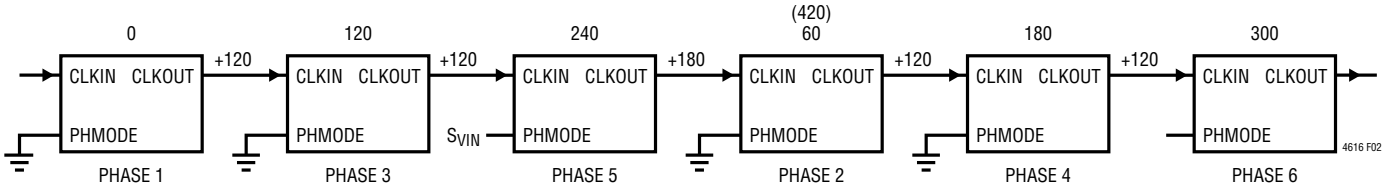


Figure 2. 6-Phase Operation

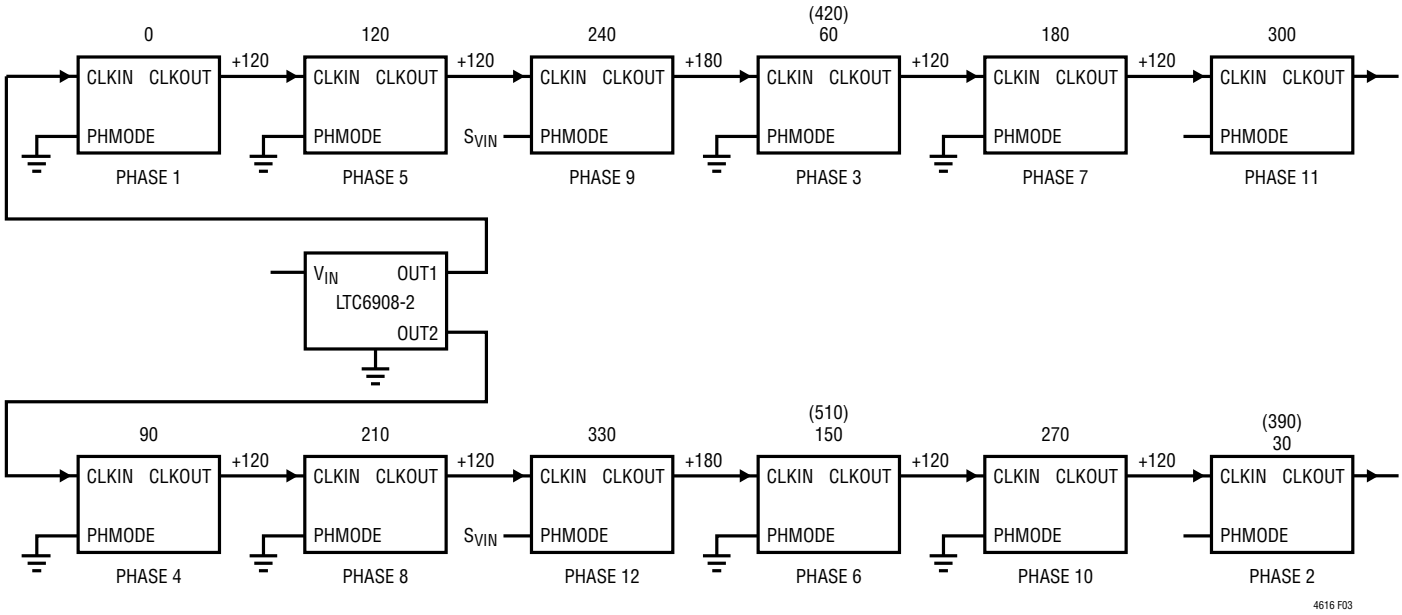


Figure 3. 12-Phase Operation

The LTM4616 device is an inherently current mode controlled device, so parallel modules will have very good current sharing. This will balance the thermals on the design. Tie the I_{TH} pins of each LTM4616 together to share the current. Current sharing is inherently guaranteed by the current mode operation of the LTM4616's DC/DC regulators. Moreover, the accuracy of current sharing between the two outputs is approximately ±15%. To reduce ground potential noise, tie the I_{THM} pins of all LTM4616s together and then connect to the SGND of the master at the point it connects to the output capacitor GND. See layout guideline in Figure 17. Figure 19 shows a schematic of the parallel design. The FB pins of the parallel module are tied together.

Input RMS Ripple Current Cancellation

Application Note 77 provides a detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivations are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases. Figure 4 shows this graph.

APPLICATIONS INFORMATION

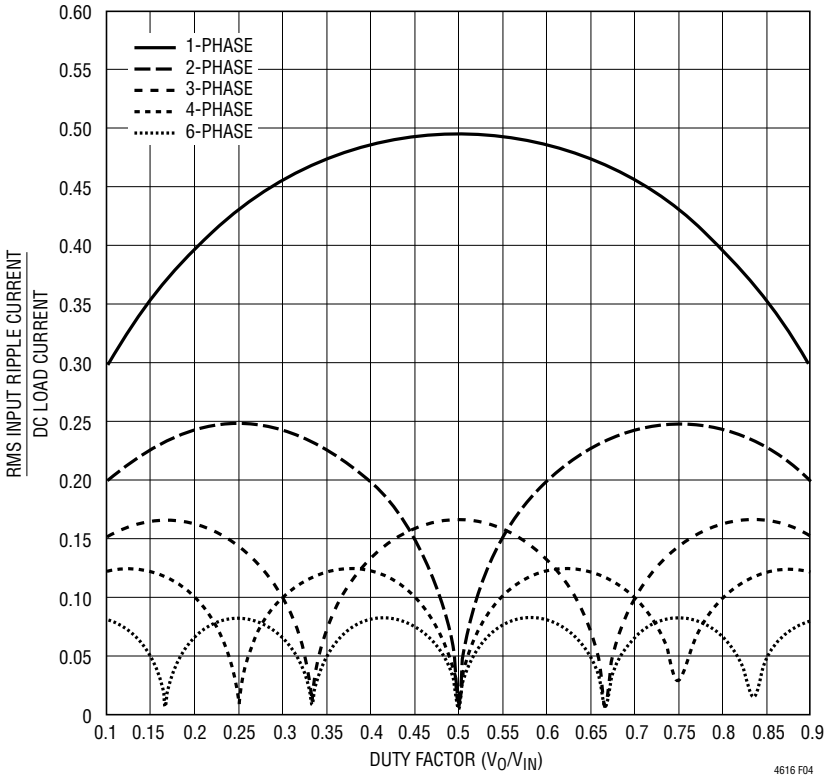


Figure 4. Normalized Input RMS Ripple Current vs Duty Factor for One to Six Channels (Phases)

Spread Spectrum Operation

Switching regulators can be particularly troublesome where electromagnetic interference (EMI) is concerned.

Switching regulators operate on a cycle-by-cycle basis to transfer power to an output. In most cases, the frequency of operation is fixed based on the output load. This method of conversion creates large components of noise at the frequency of operation (fundamental) and multiples of the operating frequency (harmonics).

To reduce this noise, the LTM4616 can run in spread spectrum operation by tying the CLKIN pin to SV_{IN}. In spread spectrum operation, the LTM4616's internal oscillator is designed to produce a clock pulse whose period is random on a cycle-by-cycle basis but fixed between 70% and 130% of the nominal frequency. This has the benefit of spreading the switching noise over a range of frequencies, thus significantly reducing the peak noise. Spread spectrum operation is disabled if CLKIN is tied to ground or if it's driven by an external frequency synchronization signal. A capacitor value of 0.01µF to 0.1µF be placed from the PLLLPF pin to ground to control the slew rate of the spread spectrum frequency change. To ensure proper start-up, add a control ramp on the TRACK pin with a resistor, R_{SR}, from TRACK to SV_{IN} and a capacitor, C_{SR}, from TRACK to ground:

$$R_{SR} \geq \frac{1}{-\left[\ln\left(1-\frac{0.592}{V_{IN}}\right)\bullet 500\bullet C_{SR}\right]}$$

Output Voltage Tracking

Output voltage tracking can be programmed externally using the TRACK pin. The output can be tracked up and down with another regulator. The master regulator's output is divided down with an external resistor divider that is the same as the slave regulator's feedback divider to implement

APPLICATIONS INFORMATION

coincident tracking. The LTM4616 uses an accurate 10k resistor internally for the top feedback resistor. Figure 5 shows an example of coincident tracking:

$$Slave = \left(1 + \frac{10k}{R_{TA}}\right) \bullet V_{TRACK}$$

V_{TRACK} is the track ramp applied to the slave's track pin. V_{TRACK} has a control range of 0V to 0.596V, or the internal reference voltage. When the master's output is divided down with the same resistor values used to set the slave's output, then the slave will coincident track with the master until it reaches its final value. The master will continue to its final value from the slave's regulation point. Voltage tracking is disabled when V_{TRACK} is more than 0.596V. R_{TA} in Figure 5 will be equal to R_{FB} for coincident tracking.

The track pin of the master can be controlled by an external ramp or by R_{SR} and C_{SR} in Figure 5 referenced to V_{IN}. The RC ramp time can be programmed using equation:

$$t = -\left(\ln\left(1 - \frac{0.596V}{V_{IN}}\right) \bullet R_{SR} \bullet C_{SR}\right)$$

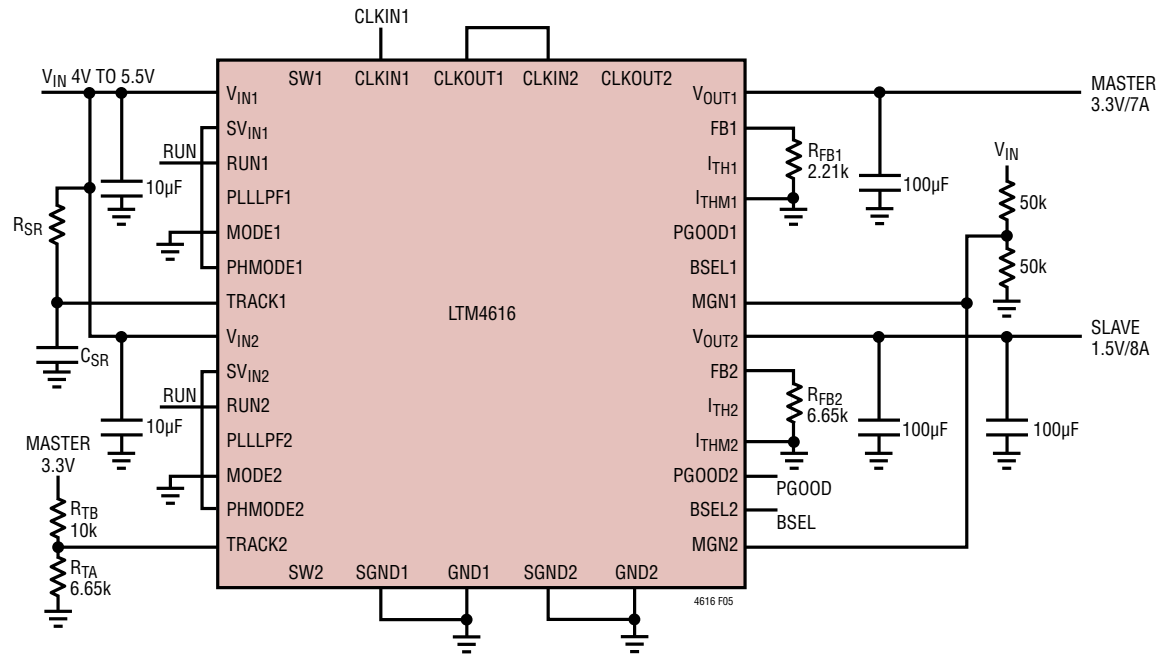
Ratiometric tracking can be achieved by a few simple calculations and the slew rate value applied to the master's track pin. As mentioned above, the TRACK pin has a control range from 0V to 0.596V. The master's TRACK pin slew rate is directly equal to the master's output slew rate in Volts/Time:

$$\frac{MR}{SR} \bullet 10k = R_{TB}$$

where MR is the master's output slew rate and SR is the slave's output slew rate in Volts/Time. When coincident tracking is desired, then MR and SR are equal, thus R_{TB} is equal to 10k. R_{TA} is derived from equation:

$$R_{TA} = \frac{0.596V}{\frac{V_{FB}}{10k} + \frac{V_{FB}}{R_{FB}} - \frac{V_{TRACK}}{R_{TB}}}$$

where V_{FB} is the feedback voltage reference of the regulator and V_{TRACK} is 0.596V. Since R_{TB} is equal to the 10k top feedback resistor of the slave regulator in coincident tracking, then R_{TA} is equal to R_{FB2} with V_{FB} = V_{TRACK}.



FOR TRACK1:
1. TIE TO VIN TO DISABLE TRACK WITH DEFAULT 100µs SOFT START
2. APPLY A CONTROL RAMP WITH R_{SR} AND C_{SR} TIED TO V_{IN} WITH $t = -(\ln(1-0.596/V_{IN}) \bullet R_{SR} \bullet C_{SR})$
3. APPLY AN EXTERNAL TRACKING RAMP DIRECTLY

Figure 5. Dual Outputs (3.3V and 1.5V) with Tracking

APPLICATIONS INFORMATION

Therefore R_{TB} = 10k and R_{TA} = 6.65k in Figure 5. Figure 6 shows the output voltage for coincident tracking.

In ratiometric tracking, a different slew rate maybe desired for the slave regulator. R_{TB} can be solved for when SR is slower than MR. Make sure that the slave supply slew rate is chosen to be fast enough so that the slave output voltage will reach it final value before the master output.

For example: MR = 3.3V/ms and SR = 1.5V/ms. Then R_{TB} = 22.1k. Solve for R_{TA} to equal to 4.87k.

For applications that do not require tracking or sequencing, simply tie the TRACK pin to SV_{IN} to let RUN control the turn on/off. Connecting TRACK to SV_{IN} also enables the ~100µs of internal soft-start during start-up.

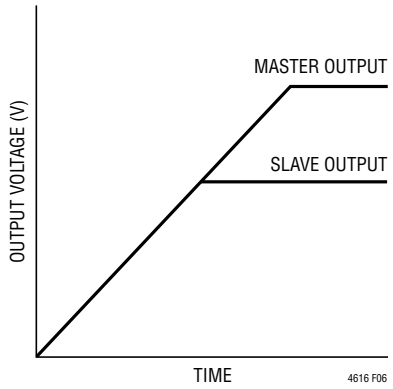


Figure 6. Output Voltage Coincident Tracking

Power Good

The PGOOD pin is an open-drain pin that can be used to monitor valid output voltage regulation. This pin monitors a ±10% window around the regulation point. As shown in Figure 20, the sequencing function can be realized in a dual output application by controlling the RUN pins and the PGOOD signals from each other. The 1.5V output begins its soft starting after the PGOOD signal of 3.3V output becomes high, and 3.3V output starts its shutdown after the PGOOD signal of 1.5V output becomes low. This can be applied to systems that require voltage sequencing between the core and sub-power supplies. The PGOOD pull-up resistor value can be determined as follows:

$$R_{PGOOD(MAX)} = \frac{SV_{IN} - V_{RUN}}{I_{PGOOD(MAX)}}$$

For example: $V_{IN} = SV_{IN} = 5V$, $V_{RUN} = 1.7V$ and $I_{PGOOD(MAX)}$ = 30µA. Solve for $R_{PGOOD(MAX)}$ to equal 110k. Selecting a value of 100k provides some margin.

Stability Compensation

The module has already been internally compensated for all output voltages. Table 2 is provided for most application requirements. LTpowerCAD is available for fine adjustments to the control loop.

Output Margining

For a convenient system stress test on the LTM4616's output, the user can program each output to ±5%, ±10% or ±15% of its normal operational voltage. Margining can be disabled by connecting the MGN pin to a voltage divider as shown in Figure 5. When the MGN pin is <0.3V, it forces negative margining, in which the output voltage is below the regulation point. When MGN is $>V_{IN}$ – 0.3V, the output voltage is forced above the regulation point. The MGN pin with a voltage divider is driven with a small tri-state gate as shown in Figure 18 for three margin states, (High, Low, and No Margin). The amount of output voltage margining is determined by the BSEL pin. When BSEL is low, it's 5%. When BSEL is high, it's 10%. When BSEL is floating, it's 15%. When margining is active, the internal output overvoltage and undervoltage comparators are disabled and PGOOD remains high.

APPLICATIONS INFORMATION

Thermal Considerations and Output Current Derating

The power loss curves in Figures 7 and 8 can be used in coordination with the load current derating curves in Figures 9 to 16 for calculating an approximate θ_{JA} thermal resistance for the LTM4616 with various heat sinking and airflow conditions. Both LTM4616 outputs are placed in parallel for a total output current of 16A, and the power loss curves are plotted for specific output voltages up to 16A. The derating curves are plotted with each output at 8A combined for a total of 16A. The output voltages are 1.2V, 2.5V and 3.3V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature increases with and without airflow. The junctions are maintained at ~115°C while lowering output current or power with increasing ambient temperature. The 115°C value is chosen to allow for 10°C of margin relative to the maximum temperature of 125°C. The decreased output current will decrease the internal module loss as ambient temperature is increased. The power loss curves in Figures 7 and 8 show this amount of power loss as a function of load current that is specified with both channels in parallel. The monitored junction temperature of 115°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example, in Figure 10 the load current is derated to 10A at ~ 80°C and the power loss for the 5V to 1.2V at 10A output is ~3.2W. If the 80°C ambient temperature is subtracted from the 115°C maximum junction temperature, then difference of 35°C divided by 3.2W equals a 10.9°C/W. Table 4 specifies a 10.5°C/W value which is very close. Table 4 and Table 5 provide equivalent thermal resistances for 1.2V and 3.3V outputs, with and without airflow and heat sinking. The printed circuit board is a 1.6mm thick four layer board with two ounce copper for the two outer layers and one ounce copper for the two inner layers. The PCB dimensions are 95mm × 76mm. The BGA heat sinks are listed below Table 5. At load currents on each channel from 3A to 8A (6A to 16A in parallel on the derating curves), the thermal resistance values in Tables 4 and 5 are fairly accurate. As the load currents go below the 3A level on each channel the thermal resistance starts to increase due to the reduced power loss on the board. The approximate thermal resistance values for these lower currents is 15°C/W.

Safety Considerations

The LTM4616 modules do not provide isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The device does support thermal shutdown and overcurrent protection.

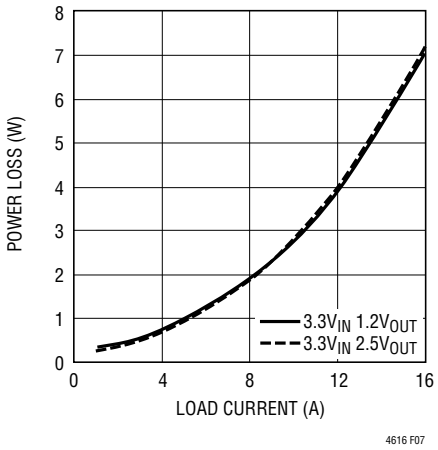


Figure 7. 1.2V, 2.5V Power Loss

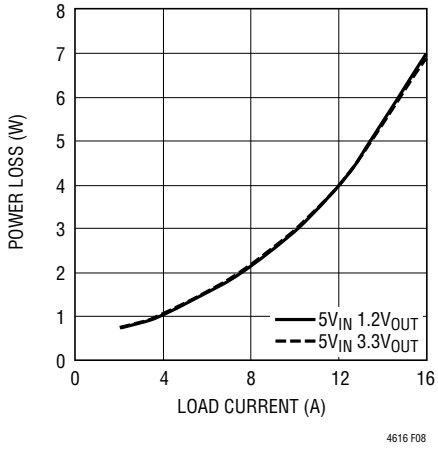


Figure 8. 1.2V, 3.3V Power Loss

APPLICATIONS INFORMATION

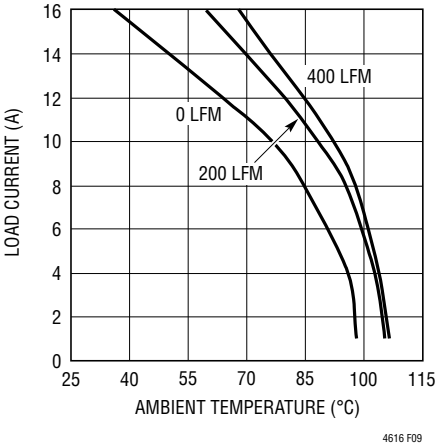


Figure 9. $5V_{IN}$ to $3.3V_{OUT}$ with No Heat Sink

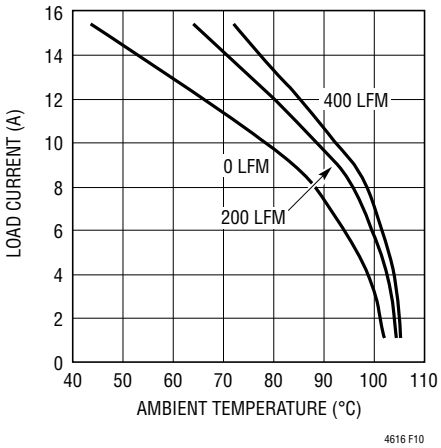


Figure 10. $5V_{IN}$ to $1.2V_{OUT}$ with No Heat Sink

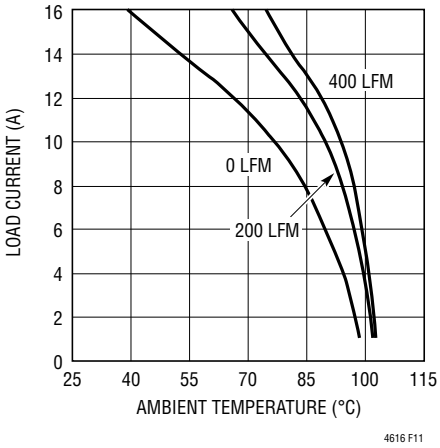


Figure 11. $5V_{IN}$ to $3.3V_{OUT}$ with BGA Heat Sink

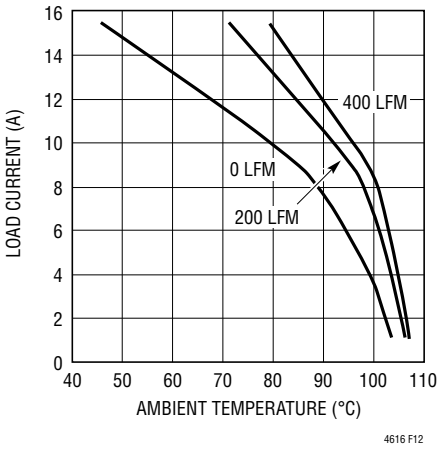


Figure 12. $5V_{IN}$ to $1.2V_{OUT}$ with BGA Heat Sink

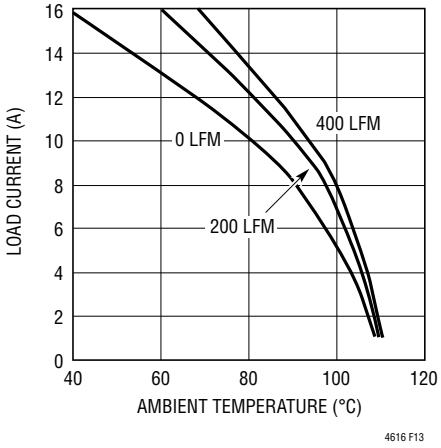


Figure 13. $3.3V_{IN}$ to $1.2V_{OUT}$ with No Heat Sink

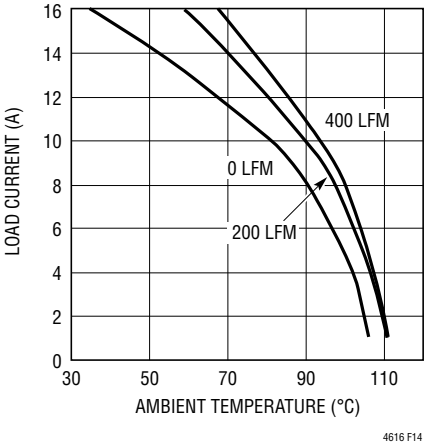


Figure 14. $3.3V_{IN}$ to $2.5V_{OUT}$ with No Heat Sink

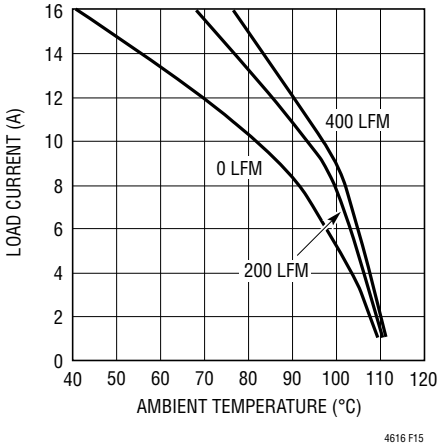


Figure 15. $3.3V_{IN}$ $1.2V_{OUT}$ with BGA Heat Sink

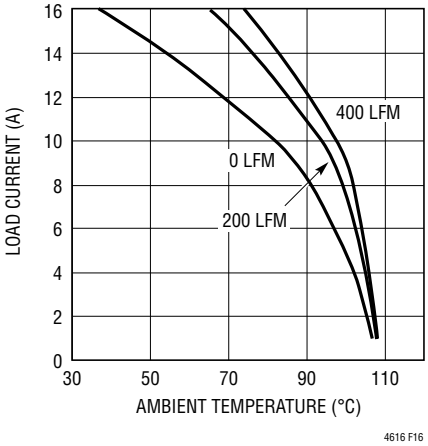


Figure 16. $3.3V_{IN}$ $2.5V_{OUT}$ with BGA Heat Sink

APPLICATIONS INFORMATION

Table 4. 1.2V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figures 10, 13	3.3, 5	Figures 7, 8	0	None	10.5
Figures 10, 13	3.3, 5	Figures 7, 8	200	None	8.0
Figures 10, 13	3.3, 5	Figures 7, 8	400	None	7.0
Figures 12, 15	3.3, 5	Figures 7, 8	0	BGA Heat Sink	9.5
Figures 12, 15	3.3, 5	Figures 7, 8	200	BGA Heat Sink	6.3
Figures 12, 15	3.3, 5	Figures 7, 8	400	BGA Heat Sink	5.2

Table 5. 3.3V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 9	5	Figure 8	0	None	10.5
Figure 9	5	Figure 8	200	None	8.0
Figure 9	5	Figure 8	400	None	7.0
Figure 11	5	Figure 8	0	BGA Heat Sink	9.8
Figure 11	5	Figure 8	200	BGA Heat Sink	7.0
Figure 11	5	Figure 8	400	BGA Heat Sink	5.5

HEAT SINK MANUFACTURER	PART NUMBER	WEBSITE
AAVID Thermalloy	375424B00034G	www.aavidthermalloy.com
Cool Innovations	4-050503P to 4-050508P	www.coolinnovations.com

APPLICATIONS INFORMATION

Layout Checklist/Example

The high integration of LTM4616 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN1}, V_{IN2}, GND1 and GND2, V_{OUT1} and V_{OUT2}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, GND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on the pads, unless they are capped or plated over.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
- For parallel modules, tie the I_{TH}, FB and I_{THM} pins together. Use an internal layer to closely connect these pins together. All of the I_{THM} pins connect to the SGND of the master regulator, then the master SGND connects to GND.

Figure 17 gives a good example of the recommended layout.

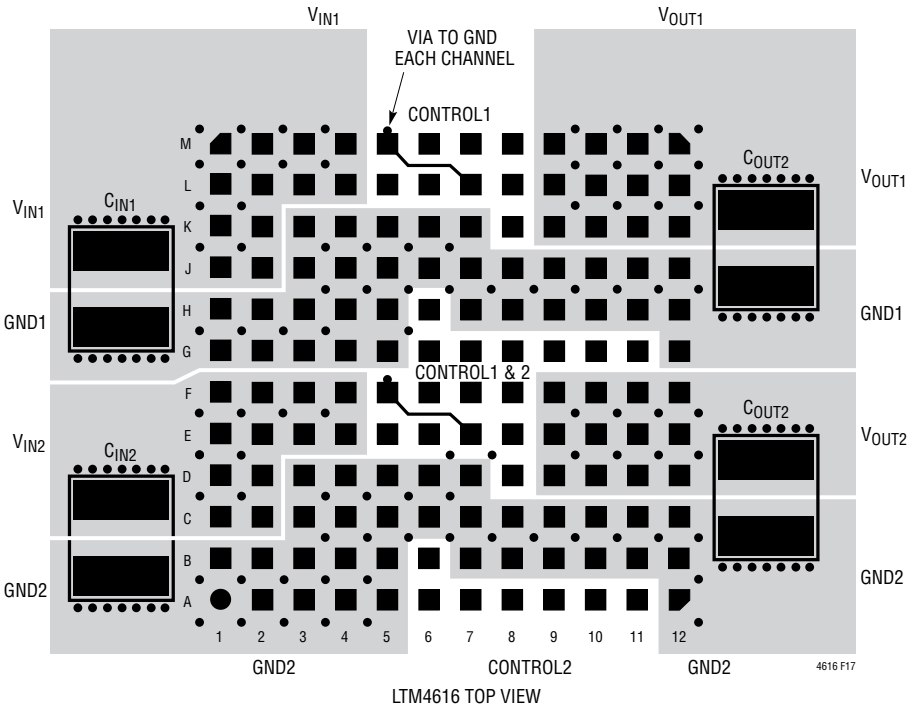
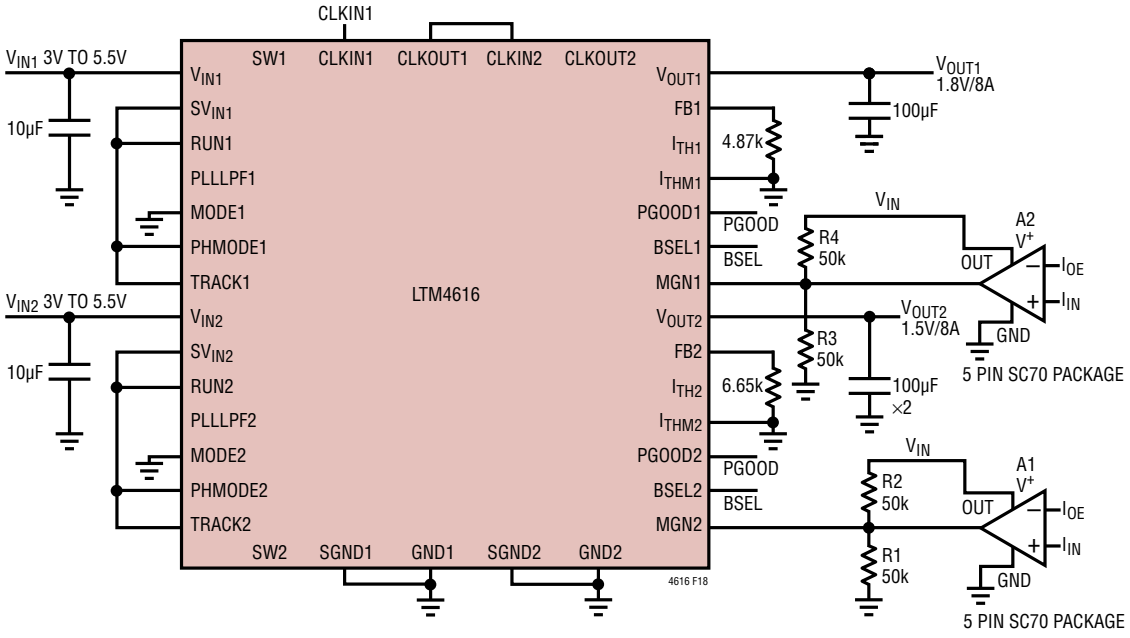


Figure 17. Recommended PCB Layout
(LGA and BGA PCB Layouts Are Identical with the Exception of Circle Pads for BGA. See Package Description.)

APPLICATIONS INFORMATION



BSEL: HIGH = 10%
FLOAT = 15%
LOW = 5%

A1, A2 PERICOM PI74ST1G126CEX
TOSHIBA TC7SZ126AFE

OE	IN	OUT	MGN	MARGIN VALUE
H	H	H	H	+ Value of BSEL Selection
H	L	L	L	– Value of BSEL Selection
L	X	Z	$V_{IN}/2$	No Margin

Figure 18. Typical 3V to 5.5V_{IN}, to 1.8V, 1.5V Outputs

APPLICATIONS INFORMATION

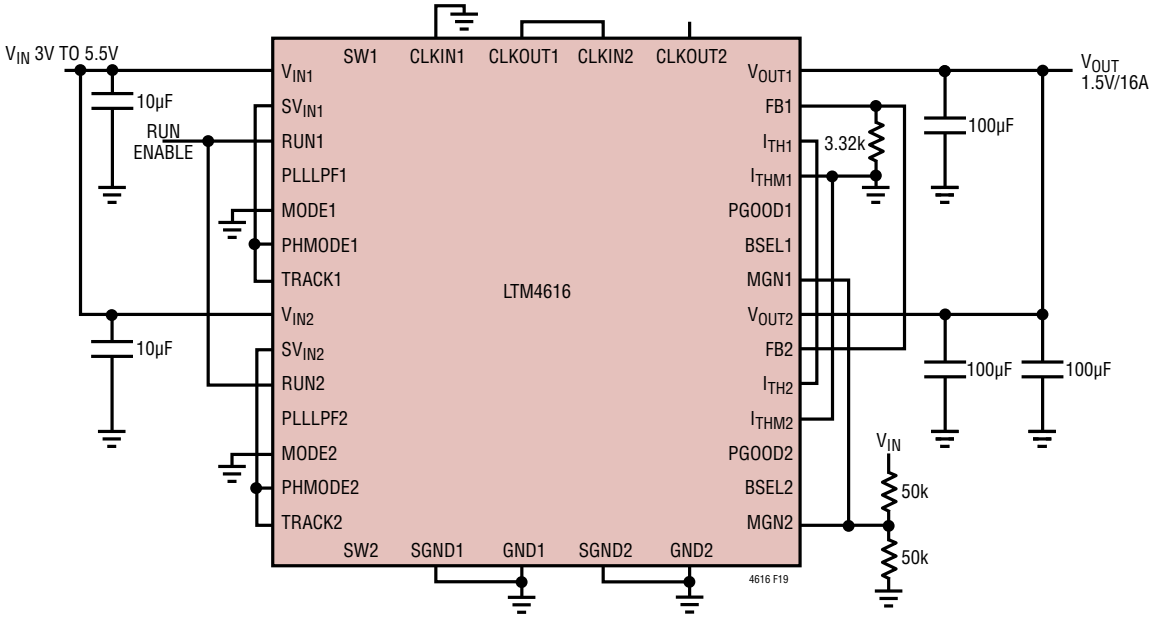


Figure 19. LTM4616 Two Outputs Parallel, 1.5V at 16A Design

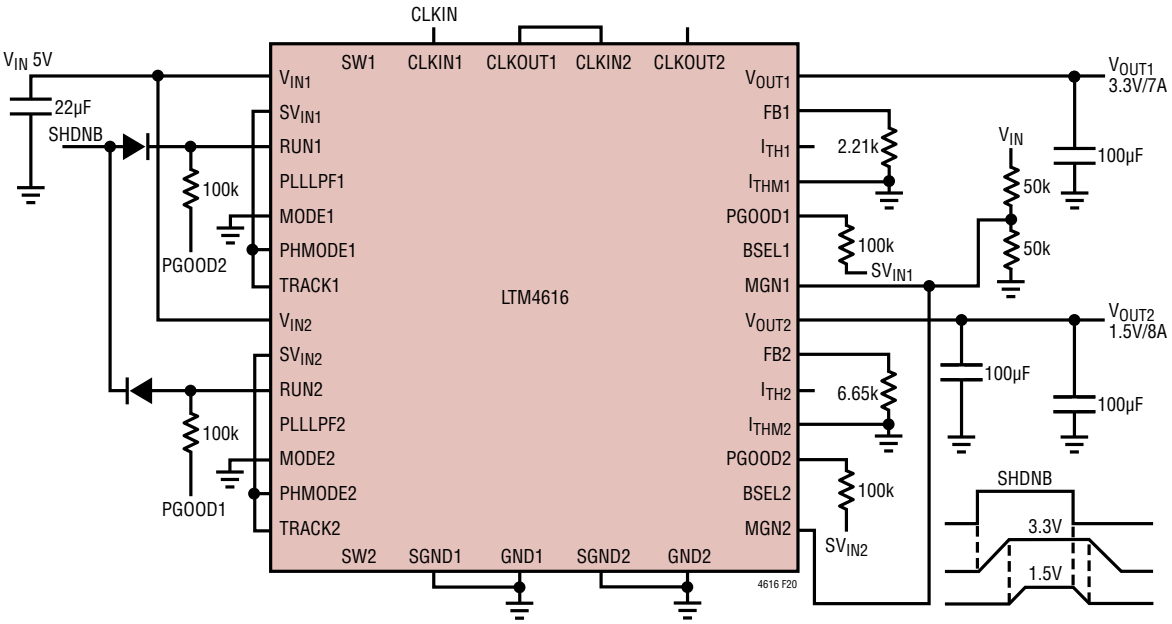
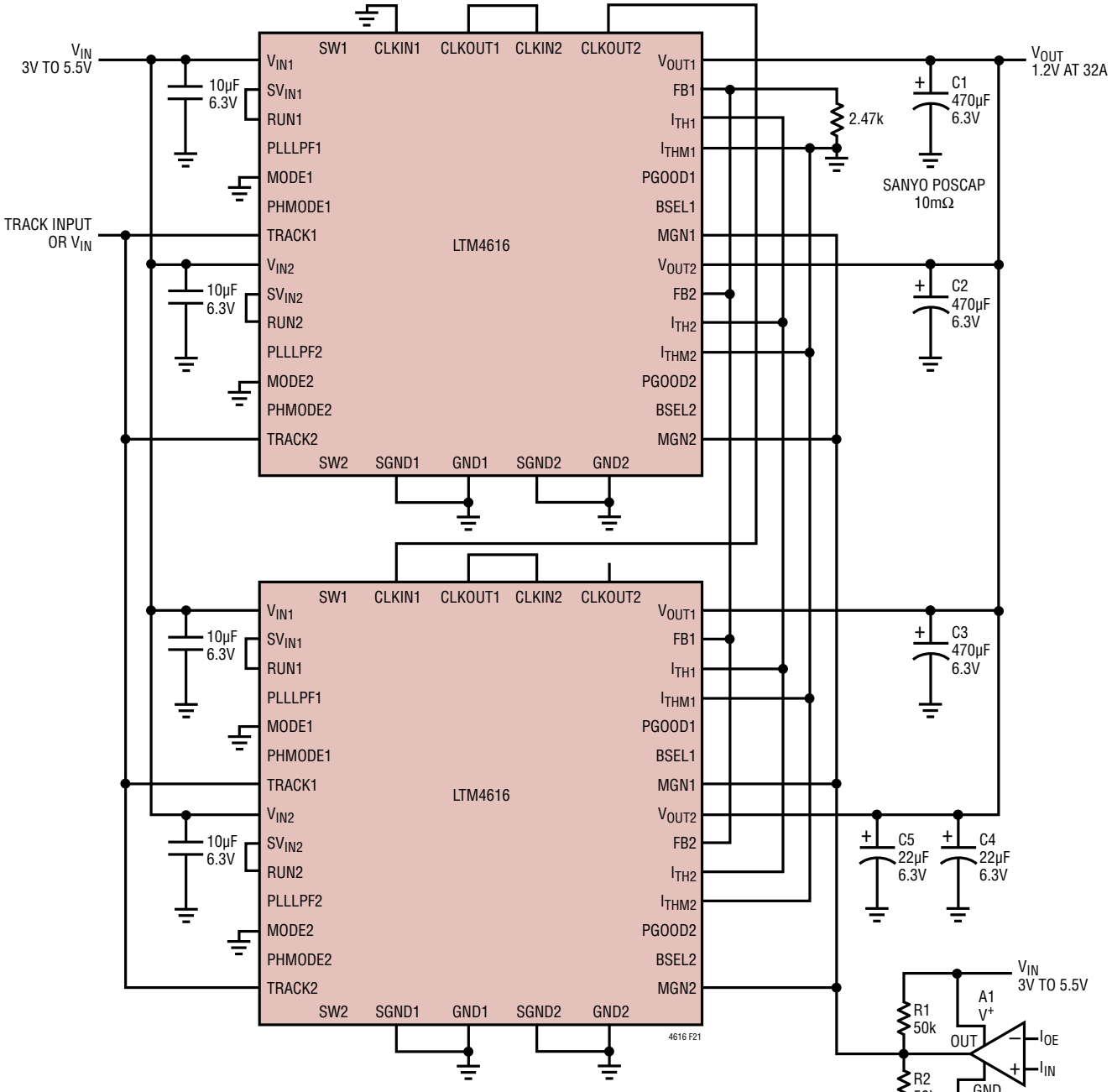


Figure 20. LTM4616 Output Sequencing Application

APPLICATIONS INFORMATION



OE	IN	OUT	MGN	MARGIN VALUE
H	H	H	H	+ Value of BSEL Selection
H	L	L	L	– Value of BSEL Selection
L	X	Z	$V_{IN}/2$	No Margin

Figure 21. Four Phase in Parallel, 1.2V at 32A

APPLICATIONS INFORMATION

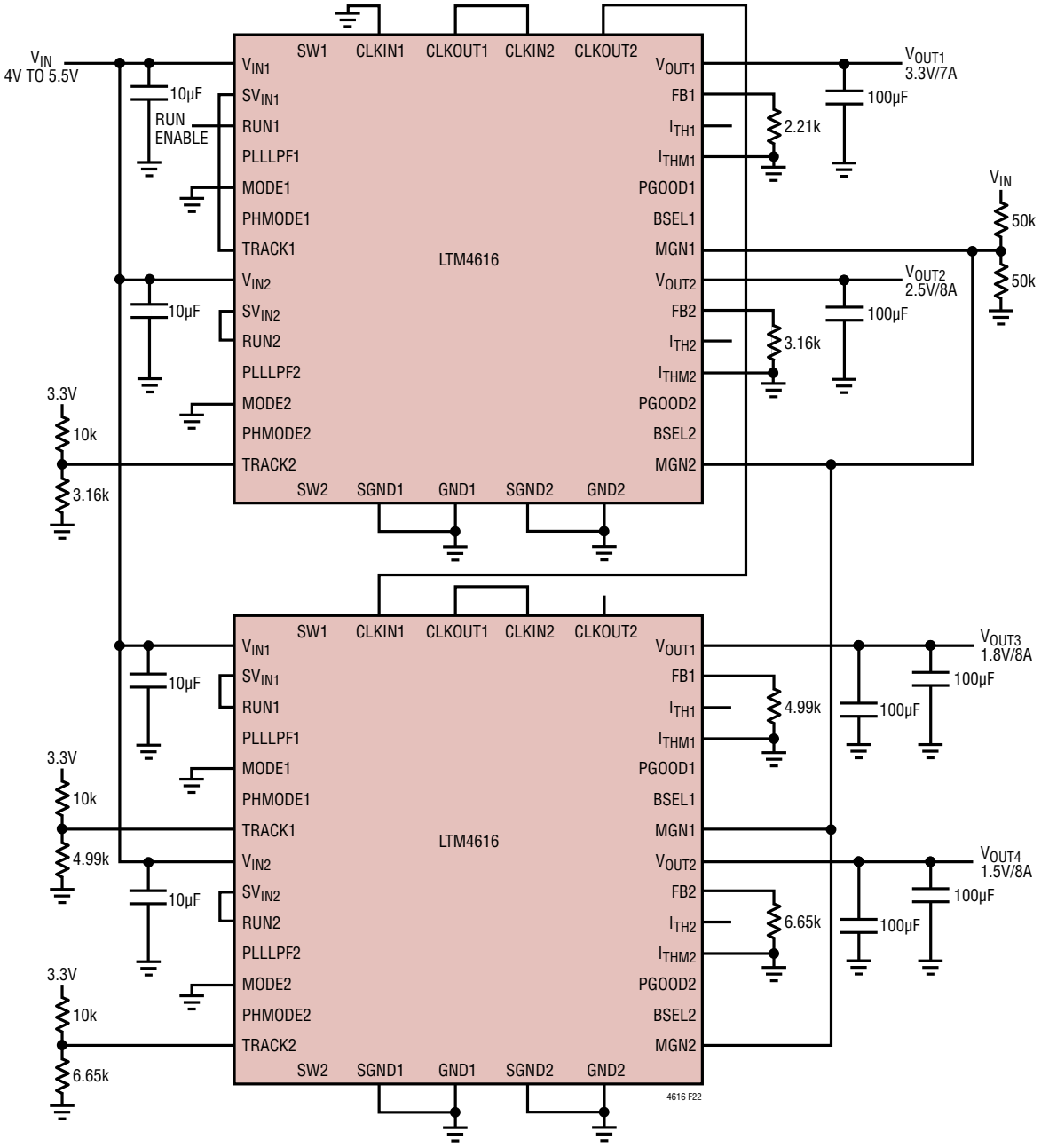


Figure 22. 4-Phase, Four Outputs (3.3V, 2.5V, 1.8V and 1.5V) with Tracking

PACKAGE DESCRIPTION

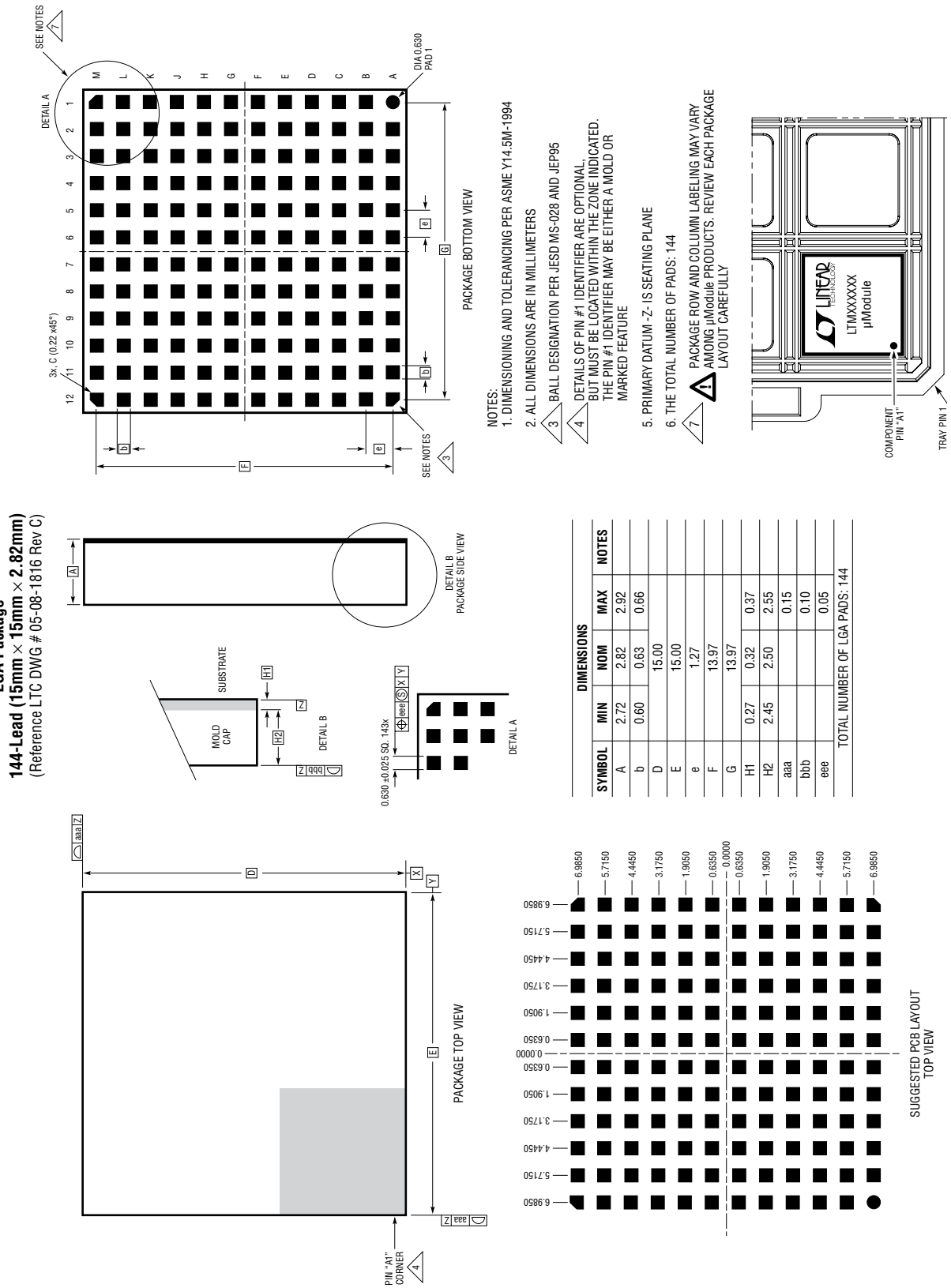
Pin Assignment Table
(Arranged by Pin Number)

PIN NAME		PIN NAME		PIN NAME		PIN NAME		PIN NAME		PIN NAME	
A1	GND1	B1	GND1	C1	V_{IN1}	D1	V_{IN1}	E1	V_{IN1}	F1	V_{IN1}
A2	GND1	B2	GND1	C2	V_{IN1}	D2	V_{IN1}	E2	V_{IN1}	F2	V_{IN1}
A3	GND1	B3	GND1	C3	GND1	D3	GND1	E3	V_{IN1}	F3	V_{IN1}
A4	GND1	B4	GND1	C4	GND1	D4	GND1	E4	V_{IN1}	F4	V_{IN1}
A5	GND1	B5	GND1	C5	GND1	D5	GND1	E5	SV_{IN1}	F5	SGND1
A6	BSEL1	B6	SW1	C6	GND1	D6	GND1	E6	PLLLPF1	F6	RUN1
A7	CLKIN1	B7	GND1	C7	GND1	D7	GND1	E7	I_{THM1}	F7	CLKOUT1
A8	MODE1	B8	GND1	C8	GND1	D8	FB1	E8	TRACK1	F8	I_{TH1}
A9	PHMODE1	B9	GND1	C9	GND1	D9	V_{OUT1}	E9	V_{OUT1}	F9	V_{OUT1}
A10	MGN1	B10	GND1	C10	GND1	D10	V_{OUT1}	E10	V_{OUT1}	F10	V_{OUT1}
A11	PGOOD1	B11	GND1	C11	GND1	D11	V_{OUT1}	E11	V_{OUT1}	F11	V_{OUT1}
A12	GND1	B12	GND1	C12	GND1	D12	V_{OUT1}	E12	V_{OUT1}	F12	V_{OUT1}

PIN NAME		PIN NAME		PIN NAME		PIN NAME		PIN NAME		PIN NAME	
G1	GND2	H1	GND2	J1	V_{IN2}	K1	V_{IN2}	L1	V_{IN2}	M1	V_{IN2}
G2	GND2	H2	GND2	J2	V_{IN2}	K2	V_{IN2}	L2	V_{IN2}	M2	V_{IN2}
G3	GND2	H3	GND2	J3	GND2	K3	GND2	L3	V_{IN2}	M3	V_{IN2}
G4	GND2	H4	GND2	J4	GND2	K4	GND2	L4	V_{IN2}	M4	V_{IN2}
G5	GND2	H5	GND2	J5	GND2	K5	GND2	L5	SV_{IN2}	M5	SGND2
G6	BSEL2	H6	SW2	J6	GND2	K6	GND2	L6	PLLLPF2	M6	RUN2
G7	CLKIN2	H7	GND2	J7	GND2	K7	GND2	L7	I_{THM2}	M7	CLKOUT2
G8	MODE2	H8	GND2	J8	GND2	K8	FB2	L8	TRACK2	M8	I_{TH2}
G9	PHMODE2	H9	GND2	J9	GND2	K9	V_{OUT2}	L9	V_{OUT2}	M9	V_{OUT2}
G10	MGN2	H10	GND2	J10	GND2	K10	V_{OUT2}	L10	V_{OUT2}	M10	V_{OUT2}
G11	PGOOD2	H11	GND2	J11	GND2	K11	V_{OUT2}	L11	V_{OUT2}	M11	V_{OUT2}
G12	GND2	H12	GND2	J12	GND2	K12	V_{OUT2}	L12	V_{OUT2}	M12	V_{OUT2}

PACKAGE DESCRIPTION

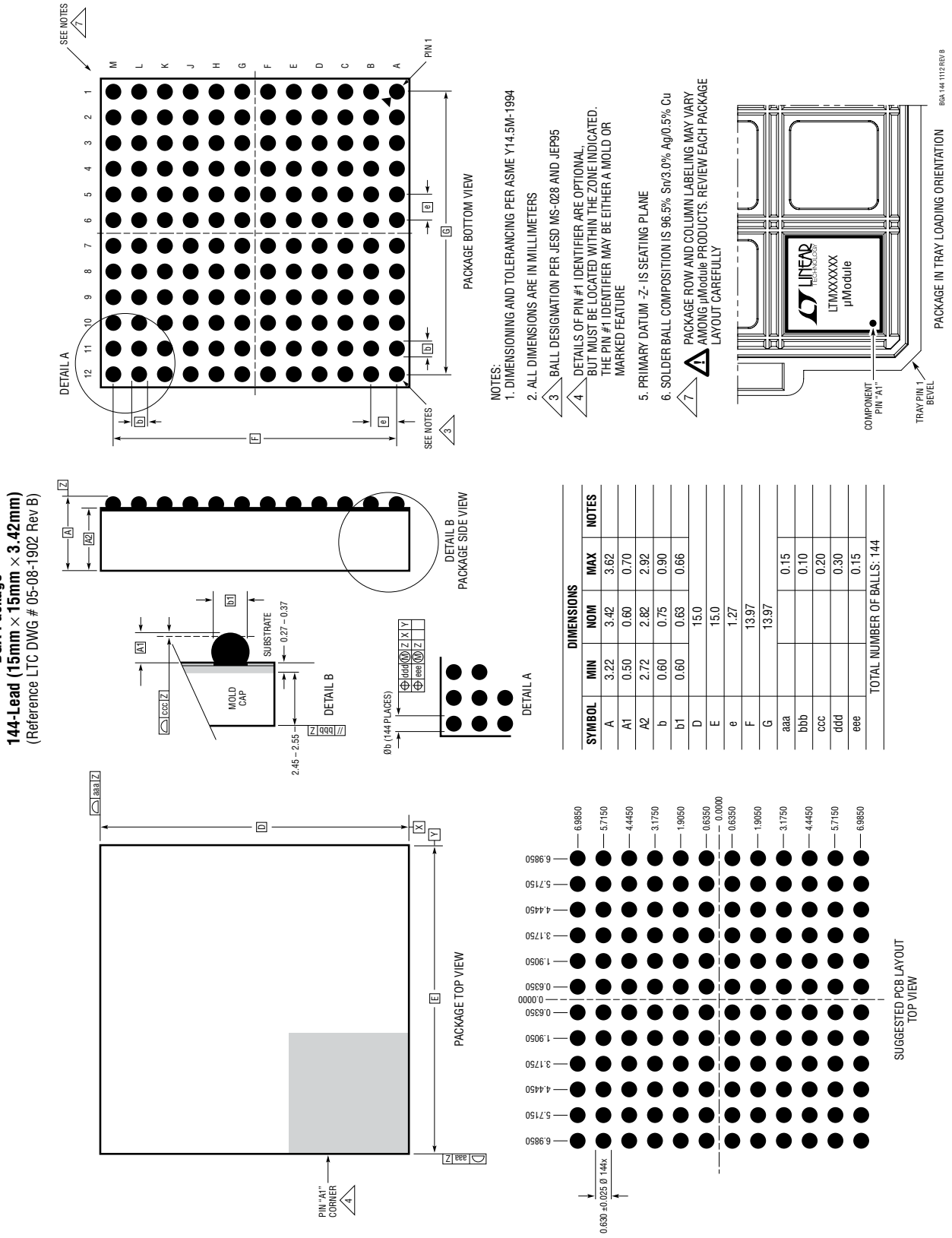
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	2.72	2.82	2.92	
b	0.60	0.63	0.66	
D		15.00		
E		15.00		
e		1.27		
F		13.97		
G		13.97		
H1	0.27	0.32	0.37	
H2	2.45	2.50	2.55	
aaa			0.15	
bbb			0.10	
eee			0.05	
TOTAL NUMBER OF LGA PADS: 144				

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	3.22	3.42	3.62	
A1	0.50	0.60	0.70	
A2	2.72	2.82	2.92	
b	0.60	0.75	0.90	
b1	0.60	0.63	0.66	
D		15.0		
E		15.0		
e		1.27		
F		13.97		
G		13.97		
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
	TOTAL NUMBER OF BALLS: 144			

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	2/11	Updated Features	1
		Updated Pin Configuration	2
		Updated Electrical Characteristics	2, 3, 4
		Replaced graphs G05 and G06	5
		Updated graph G18	6
		Updated Pin Functions	7
		Updated Simplified Block Diagram	8
		Updated Operation section	9
		Text updated in Applications Information section	10 through 20
		Updated figures 3, 5, 17, 18, 19, 20, 21, 22	13 through 24
		Updated Package Description table	25
		Added Package Photo and updated Related Parts	28
D	3/12	Added BGA package option and MP temperature grade	1
		Added BGA package option, MP temperature grade, thermal resistance, and device weight	2
		Updated Note 2	4
		Clarified Load Transient Response conditions	5
		Updated recommended heat sinks Table	20
		Corrected MGN Pin usage	24
		Added package photo	30
E	4/13	Added PGOOD leakage current and voltage low limits to Electrical Characteristics table	4
		Added Design Resources	30
F	2/14	Added SnPb BGA package option	1, 2