Ultra-Tiny, 16-Bit ΔΣ ADC with I²C Interface

FEATURES

- **GND to V_{CC} Single-Ended Input Range**
- **0.02LSB RMS Noise**
- **2LSB INL, No Missing Codes**
- **1LSB Offset Error**
- **4LSB Full-Scale Error**
- Programmable 30/60 Conversions per Second
- Single Conversion Settling Time for Multiplexed Applications
- Single-Cycle Operation with Auto Shutdown
- 400µA Supply Current
- 0.2µA Sleep Current
- Internal Oscillator—No External Components Required
- Single Supply, 2.7V to 5.5V Operation
- 2-Wire I²C Interface
- Ultra-Tiny 3mm × 2mm DFN or TSOT-23 Package

APPLICATIONS

- System Monitoring
- Environmental Monitoring
- Direct Temperature Measurements
- Instrumentation
- Industrial Process Control
- Data Acquisition
- Embedded ADC Upgrades

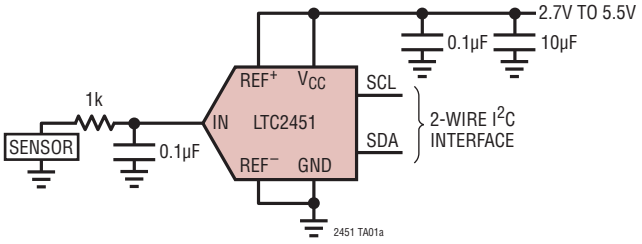
DESCRIPTION

The LTC®2451 is an ultra-tiny, 16-bit, analog-to-digital converter. The LTC2451 uses a single 2.7V to 5.5V supply, accepts a single-ended analog input voltage and communicates through an I²C interface. The converter is available in an 8-pin, 3mm × 2mm DFN or TSOT-23 package. It includes an integrated oscillator that does not require any external components. It uses a delta-sigma modulator as a converter core and provides single-cycle settling time for multiplexed applications. The LTC2451 includes a proprietary input sampling scheme that reduces the average input sampling current several orders of magnitude lower than conventional ΔΣ converters.

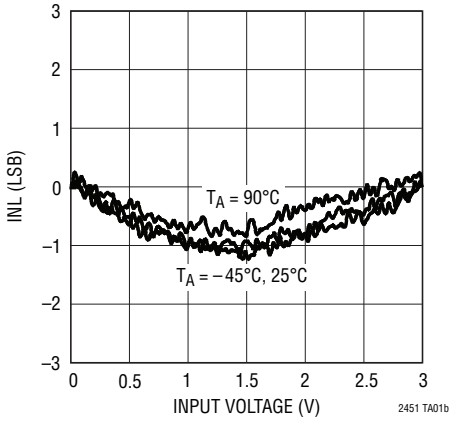
The LTC2451 is capable of up to 60 conversions per second and, due to the very large oversampling ratio, has extremely relaxed antialiasing requirements. In the 30Hz mode, the LTC2451 includes continuous internal offset calibration algorithms which are transparent to the user, ensuring accuracy over time and over the operating temperature range. The converter has external REF^+ and REF^- pins and the input voltage can range from V_{REF}^- to V_{REF}^+. If $V_{REF}^+ = V_{CC}$ and $V_{REF}^- = GND$, the input voltage can range from GND to V_{CC}.

Following a single conversion, the LTC2451 can automatically enter sleep mode and reduce its power to less than 0.2µA. If the user reads the ADC once per second, the LTC2451 consumes an average of less than 50µW from a 2.7V supply.

TYPICAL APPLICATION



Integral Nonlinearity, V_{CC} = 3V

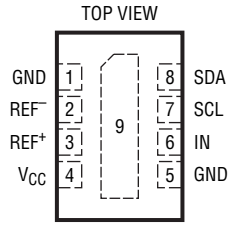


ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltage (V_{CC}) ..... –0.3V to 6V
Analog Input Voltage (V_{IN}) ..... –0.3V to (V_{CC} + 0.3V)
Reference Voltage (V_{REF}^+, V_{REF}^-) ... –0.3V to (V_{CC} + 0.3V)
Digital Voltage (V_{SDA}, V_{SCL}) ..... –0.3V to (V_{CC} + 0.3V)

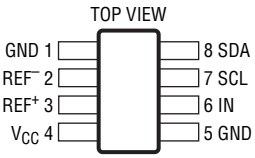
Storage Temperature Range ..... –65°C to 150°C
Operating Temperature Range
LTC2451C ..... 0°C to 70°C
LTC2451I ..... –40°C to 85°C

PIN CONFIGURATION



DDB PACKAGE
8-LEAD (3mm × 2mm) PLASTIC DFN

C/I GRADE T_{JMAX} = 125°C, θ_{JA} = 76°C/W
EXPOSED PAD (PIN 9) IS GND, MUST BE SOLDERED TO PCB



TS8 PACKAGE
8-LEAD PLASTIC TSOT-23

C/I GRADE T_{JMAX} = 125°C, θ_{JA} = 140°C/W

ORDER INFORMATION

Lead Free Finish

TAPE AND REEL (MINI)	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2451CDDB#TRMPBF	LTC2451CDDB#TRPBF	LDGQ	8-Lead Plastic (3mm × 2mm) DFN	0°C to 70°C
LTC2451IDDB#TRMPBF	LTC2451IDDB#TRPBF	LDGQ	8-Lead Plastic (3mm × 2mm) DFN	–40°C to 85°C
LTC2451CTS8#TRMPBF	LTC2451CTS8#TRPBF	LTDNS	8-Lead Plastic TSOT-23	0°C to 70°C
LTC2451ITS8#TRMPBF	LTC2451ITS8#TRPBF	LTDNS	8-Lead Plastic TSOT-23	–40°C to 85°C

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	(Note 3)	●	16			Bits
Integral Nonlinearity	(Note 4)	●		2	10	LSB
Offset Error	30Hz Mode	●		0.08	0.5	mV
Offset Error	60Hz Mode	●		0.5	2	mV
Offset Error Drift				0.02		LSB/°C
Gain Error		●		0.01	0.02	% of FS
Gain Error Drift				0.02		LSB/°C
Transition Noise				1.4		μV_{RMS}
Power Supply Rejection DC	30Hz Mode			80		dB
Power Supply Rejection DC	60Hz Mode			80		dB

ANALOG INPUT AND REFERENCES

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range		●	V_{REF^-}		V_{REF^+}	V
V_{REF^+}	Positive Reference Voltage Range	$V_{REF^+} - V_{REF^-} \geq 2.5V$	●	$V_{CC} - 2.5$		V_{CC}	V
V_{REF^-}	Negative Reference Voltage Range	$V_{REF^+} - V_{REF^-} \geq 2.5V$	●	0		$V_{CC} - 2.5$	V
C_{IN}	IN Sampling Capacitance				0.35		pF
$I_{DC\_LEAK(VIN)}$	IN DC Leakage Current	V_{IN} = GND (Note 8) V_{IN} = V_{CC} (Note 8)	● ●	–10 –10	1 1	10 10	nA nA
$I_{DC\_LEAK(REF^+, REF^-)}$	REF^+, REF^- DC Leakage Current	V_{REF} = 5V (Note 8)	●	–10	1	10	nA
I_{CONV}	Input Sampling Current (Note 5)				50		nA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current Conversion Sleep		 ● ●		 400 0.2	 700 0.5	 µA µA

I²C INPUTS AND OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage		●	$0.7V_{CC}$			V
V_{IL}	Low Level Input Voltage		●			$0.3V_{CC}$	V
V_{HYS}	Hysteresis of Schmidt Trigger Inputs	(Note 3)	●	$0.05V_{CC}$			V
V_{OL}	Low Level Output Voltage (SDA)	I = 3mA	●			0.4	V
I_{IN}	Input Leakage	$0.1V_{CC} \leq V_{IN} \leq 0.9V_{CC}$	●	–1		1	µA
C_I	Capacitance for Each I/O Pin		●	10			pF
C_B	Capacitance Load for Each Bus Line		●			400	pF

I²C TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.7V to 5.5V. (Notes 2, 7)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{CONV}	Conversion Time	30Hz Mode	●	26	33.2	46	ms
t_{CONV}	Conversion Time	60Hz Mode	●	13	16.6	23	ms
f_{SCL}	SCL Clock Frequency		●	0		400	kHz
$t_{HD(SDA)}$	Hold Time (Repeated) START Condition		●	0.6			µs
t_{LOW}	LOW Period of the SCL Pin		●	1.3			µs
t_{HIGH}	HIGH Period of the SCL Pin		●	0.6			µs
$t_{SU(STA)}$	Set-Up Time for a Repeated START Condition		●	0.6			µs
$t_{HD(DAT)}$	Data Hold Time		●	0		0.9	µs
$t_{SU(DAT)}$	Data Set-Up Time		●	100			ns
t_r	Rise Time for SDA/SCL Signals	(Note 6)	●	$20 + 0.1C_B$		300	ns
t_f	Fall Time for SDA/SCL Signals	(Note 6)	●	$20 + 0.1C_B$		300	ns
$t_{SU(STO)}$	Set-Up Time for STOP Condition		●	0.6			µs
t_{BUF}	Bus Free Time Between a STOP and START Condition		●	1.3			µs

I²C TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 2, 7)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{OF}	Output Fall Time $V_{IH(MIN)}$ to $V_{IL(MAX)}$	Bus Load C_B 10pF to 400pF (Note 6)	●	20 + 0.1C_B		250	ns
t_{SP}	Input Spike Suppression		●			50	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. All voltage values are with respect to GND. V_{CC} = 2.7V to 5.5V, unless otherwise specified. Specifications apply to both 30Hz and 60Hz modes unless otherwise specified.

$V_{REF} = V_{REF}^+ – V_{REF}^–$, $V_{REFCM} = (V_{REF}^+ + V_{REF}^–)/2$, $FS = V_{REF}^+ – V_{REF}^–$; $V_{REF}^– \le V_{IN} \le V_{REF}^+$

Note 3. Guaranteed by design, not subject to test.

Note 4. Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band. Guaranteed by design, test correlation and 3-point transfer curve measurement.

Note 5. Input sampling current is the average input current drawn from the input sampling network while the LTC2451 is actively sampling the input. C_B = capacitance of one bus line in pF.

Note 6. C_B = capacitance of one bus line in pF.

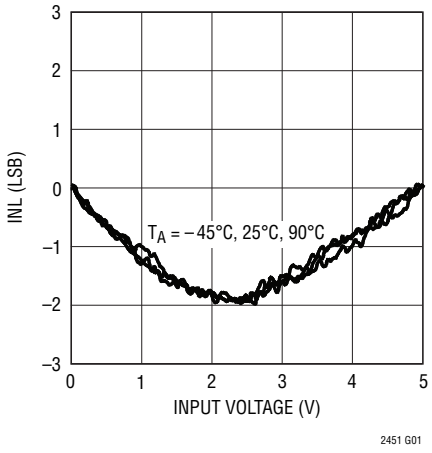
Note 7. All values refer to $V_{IH(MIN)}$ and $V_{IL(MAX)}$ levels.

Note 8. A positive current is flowing into the DUT pin.

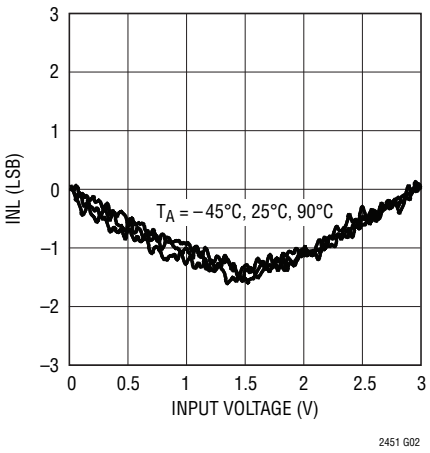
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C; graphs apply to both 30Hz and 60Hz modes, unless otherwise noted.

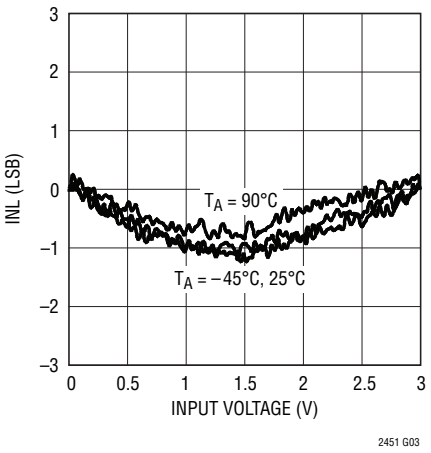
Integral Nonlinearity
$V_{CC} = V_{REF}^+ = 5V$



Integral Nonlinearity
V_{CC} = 5V, V_{REF}^+ = 3V



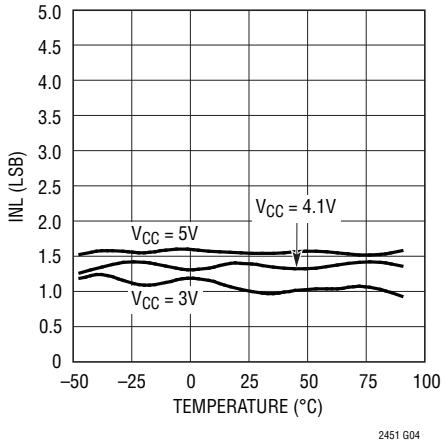
Integral Nonlinearity
$V_{CC} = V_{REF}^+ = 3V$



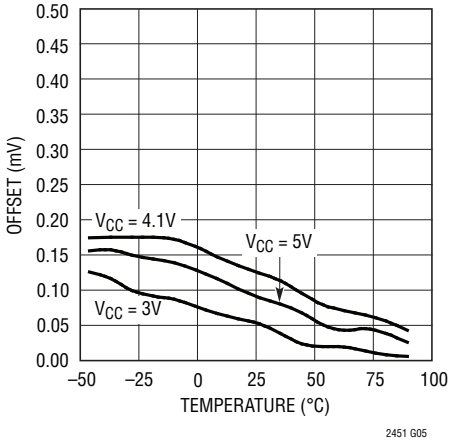
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C; graphs apply to both 30Hz and 60Hz modes, unless otherwise noted.

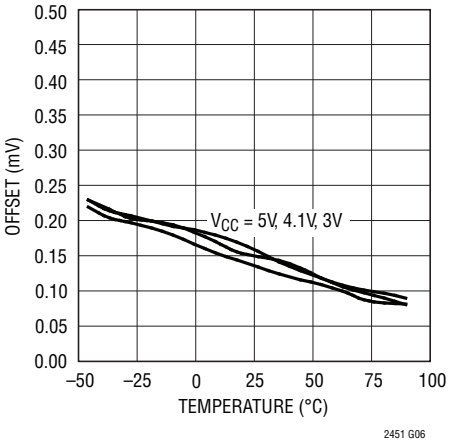
Maximum INL vs Temperature



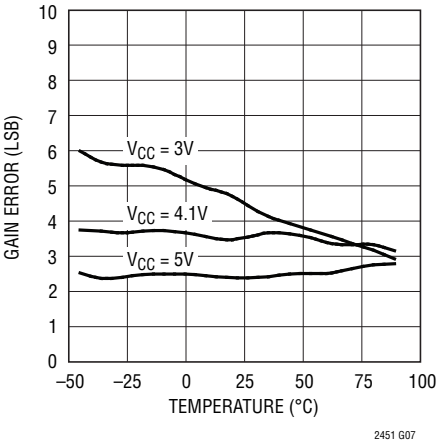
Offset Error vs Temperature 30Hz Mode



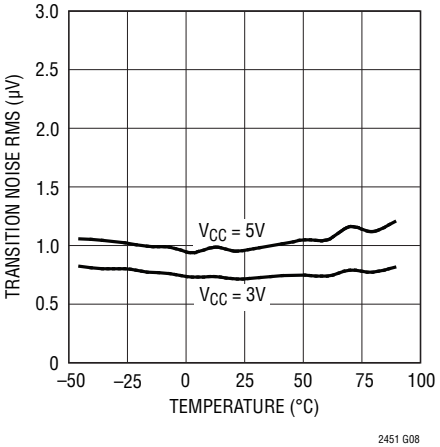
Offset Error vs Temperature 60Hz Mode



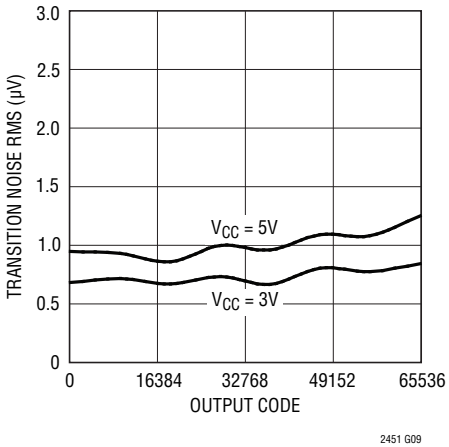
Gain Error vs Temperature



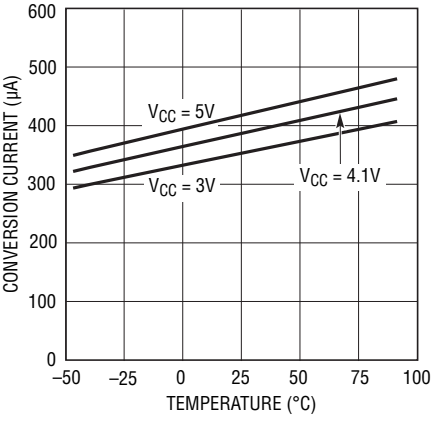
Transition Noise vs Temperature



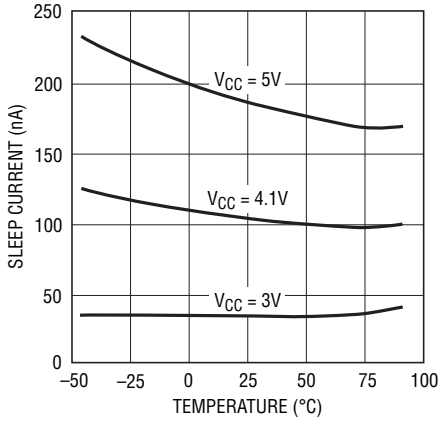
Transition Noise vs Output Code



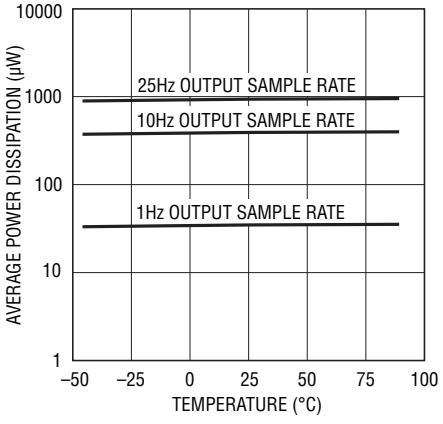
Conversion Mode Power Supply Current vs Temperature



Sleep Mode Power Supply Current vs Temperature



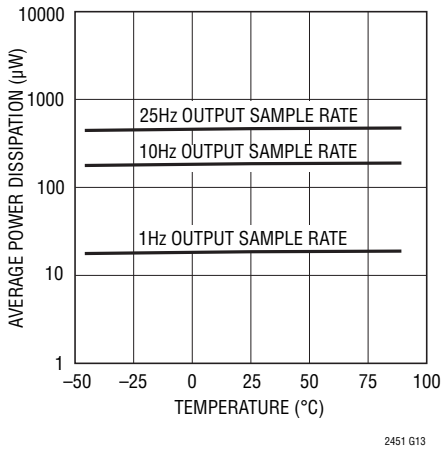
Average Power Dissipation vs Temperature V_{CC} = 3V, 30Hz Mode



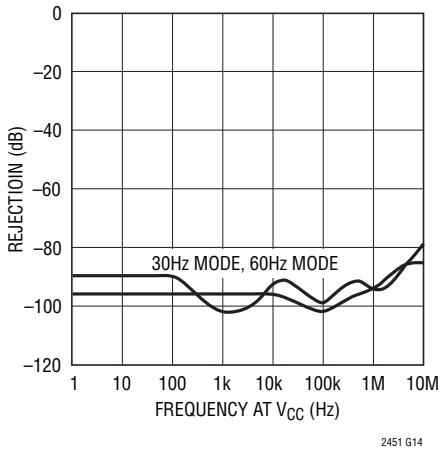
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C; graphs apply to both 30Hz and 60Hz modes, unless otherwise noted.

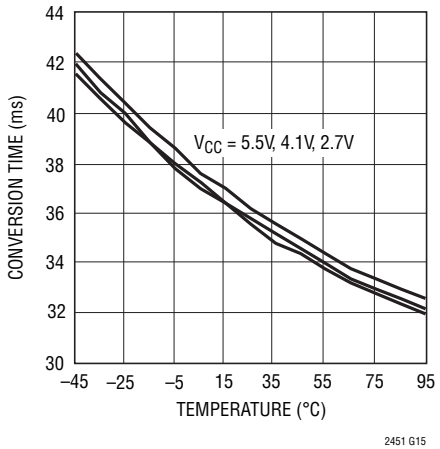
Average Power Dissipation vs Temperature V_{CC} = 3V, 60Hz Mode



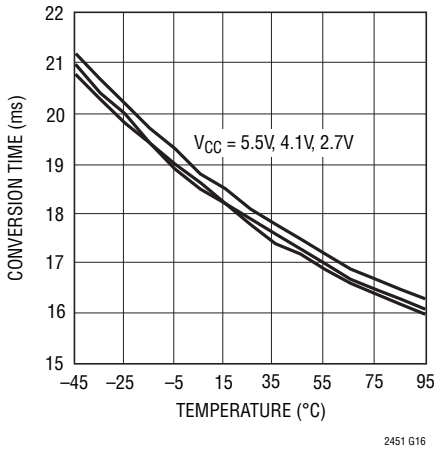
Power Supply Rejection vs Frequency at V_{CC}



Conversion Period vs Temperature 30Hz Mode



Conversion Period vs Temperature 60Hz Mode



PIN FUNCTIONS

GND (Pin 1, 5): Ground. Connect to a ground plane through a low impedance connection.

REF⁻ (Pin 2), REF⁺ (Pin 3): Differential Reference Input. The voltage on these pins can have any value between GND and V_{CC} as long as the reference positive input, REF⁺, remains more positive than the negative reference input, REF⁻, by at least 2.5V. The differential reference voltage (V_{REF} = REF⁺ to REF⁻) sets the full-scale range.

V_{CC} (Pin 4): Positive Supply Voltage. Bypass to GND (Pin 1) with a 10µF capacitor in parallel with a low series inductance 0.1µF capacitor located as close to the part as possible.

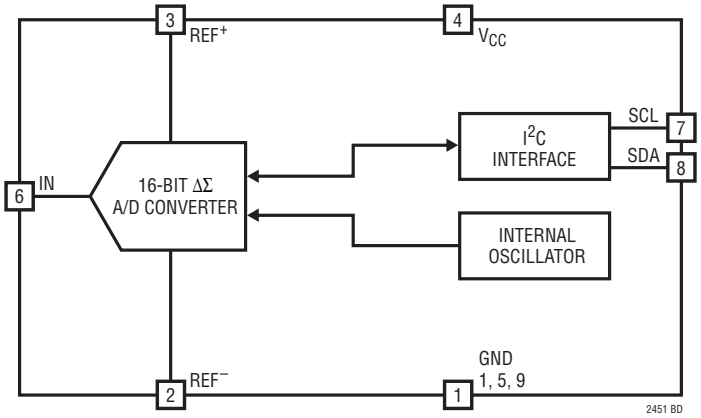
IN (Pin 6): Analog Input. IN's single-ended input range is V_{REF}^- to V_{REF}^+.

SCL (Pin 7): Serial Clock Input of the I^2C Interface. The LTC2451 can only act as a slave and the SCL pin only accepts an external serial clock. Data is shifted into the SDA pin on the rising edges of SCL and output through the SDA pin on the falling edges of SCL.

SDA (Pin 8): Bidirectional Serial Data Line of the I^2C Interface. The conversion result is output through the SDA pin. The pin is high impedance unless the LTC2451 is in the data output mode. While the LTC2451 is in the data output mode, SDA is an open-drain pull-down (which requires an external 1.7k pull-up resistor to V_{CC}).

Exposed Pad (Pin 9): Ground. Must be soldered to PCB ground.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

CONVERTER OPERATION

Converter Operation Cycle

The LTC2451 is a low power, delta-sigma analog-to-digital converter with an I^2C interface. Its operation, as shown in Figure 1, is composed of three successive states: conversion, sleep, and data input/output.

Initially, at power-up, the LTC2451 is set to its default 60Hz mode and performs a conversion. Once the conversion is complete, the device enters the sleep state. While in the sleep state, power consumption is reduced by several orders of magnitude. The part remains in the sleep state as long it is not addressed for a read or write operation. The conversion result is held indefinitely in a static shift register while the part is in the sleep state.

The device will not acknowledge an external request during the conversion state. After a conversion is finished, the device is ready to accept a read/write request. The LTC2451's address is hard wired at 0010100. Once the LTC2451 is addressed for a read operation, the device begins outputting the conversion result under the control of the serial clock (SCL). There is no latency in the conversion result. The data output is 16 bits long and outputs from MSB to LSB. Data is updated on the falling edges of SCL, allowing the user to reliably latch data on the rising edge of SCL. In write operation, the device accepts one configuration byte and the data is shifted in on the rising edges of SCL. A new conversion is initiated by a STOP condition following a valid read or write operation, or by the conclusion of a complete read cycle (all 16 bits read out of the device).

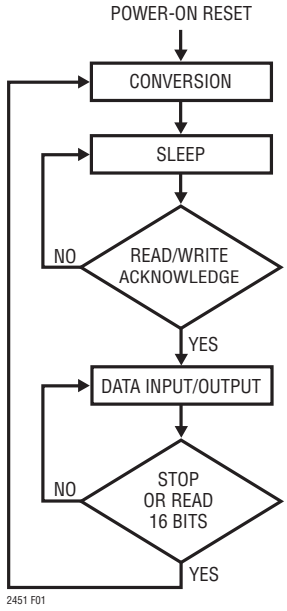


Figure 1. State Diagram

Power-Up Sequence

When the power supply voltage, V_{CC}, applied to the converter is below approximately 2.1V, the ADC performs a power-on reset. This feature guarantees the integrity of the conversion result.

When V_{CC} rises above this threshold, the converter generates an internal power-on reset (POR) signal for approximately 0.5ms. The POR signal clears all internal registers. Following the POR signal, the LTC2451 starts a conversion cycle and follows the succession of states described in Figure 1. The first conversion result following POR is accurate within the specifications of the device if the power supply voltage, V_{CC}, is restored within the operating range (2.7V to 5.5V) before the end of the POR time interval.

Ease of Use

The LTC2451 data output has no latency, filter settling delay, or redundant results associated with the conversion cycle. There is a one-to-one correspondence between the conversion and the output data. Therefore, multiplexing multiple analog input voltages requires no special actions.

In the 30Hz mode, the LTC2451 performs offset calibrations during every conversion. This calibration is transparent to the user and has no effect upon the cyclic operation previously described. The advantage of continuous calibration is stability of the ADC performance with respect to time and temperature.

The LTC2451 includes a proprietary input sampling scheme that reduces the average input current by several orders of magnitude when compared to traditional delta-sigma architectures. This allows external filter networks to interface directly to the LTC2451. Since the average input sampling current is 50nA, an external RC lowpass filter using a 1kΩ and 0.1µF results in less than 1LSB additional error.

APPLICATIONS INFORMATION

Reference Voltage Range

This converter accepts a truly differential external reference voltage. The voltage range for the REF^+ and REF^- pins covers the entire operating range of the device (GND to V_{CC}). For correct converter operation, $V_{REF}^+ - V_{REF}^- \geq 2.5V$.

The LTC2451 differential reference input range is 2.5V to V_{CC}. For the simplest operation, REF^+ can be shorted to V_{CC} and REF^- can be shorted to GND.

Input Voltage Range

Ignoring offset and full-scale errors, the converter will theoretically output an "all zero" digital result when the input is at V_{REF}^- (a zero scale input) and an "all one" digital result when the input is at V_{REF}^+ (a full-scale input). In an underrange condition, for all input voltages less than the voltage corresponding to output code 0, the converter will generate the output code 0. In an overrange condition, for all input voltages greater than the voltage corresponding to output code 65535, the converter will generate the output code 65535.

I²C INTERFACE

The LTC2451 communicates through an I²C interface. The I²C interface is a 2-wire open-drain interface supporting multiple devices and masters on a single bus. The connected devices can only pull the data line (SDA) LOW and never drive it HIGH. SDA is externally connected to the supply through a pull-up resistor. When the data line is free, it is pulled HIGH through this resistor. Data on the I²C bus can be transferred at rates up to 100k/s in the standard mode and up to 400k/s in the fast mode. The V_{CC} power should not be removed from the device when the I²C bus is active to avoid loading the I²C bus lines through the internal ESD protection diodes.

Each device on the I²C bus is recognized by a unique address stored in that device and can operate either as a transmitter or receiver, depending on the function of the device. In addition to transmitters and receivers, devices can also be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. Devices addressed by the master are considered a slave. The address of the LTC2451 is 0010100.

The LTC2451 can only be addressed as a slave. It can only transmit the last conversion result. The serial clock line, SCL, is always an input to the LTC2451 and the serial data line, SDA, is bidirectional. Figure 2 shows the definition of the I²C timing.

The START and STOP Conditions

A START (S) condition is generated by transitioning SDA from HIGH to LOW while SCL is HIGH. The bus is considered to be busy after the START condition. When the data transfer is finished, a STOP (P) condition is generated by transitioning SDA from LOW to HIGH while SCL is pulled HIGH. The bus is free after a STOP is generated. START and STOP conditions are always generated by the master.

When the bus is in use, it stays busy if a repeated START (Sr) is generated instead of a STOP condition. The repeated START (Sr) conditions are functionally identical to the START (S).

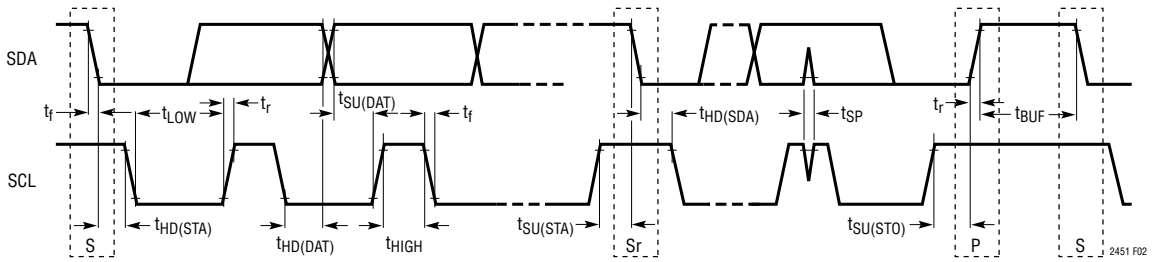


Figure 2. Definition of Timing for Fast/Standard Mode Devices on the I²C Bus

APPLICATIONS INFORMATION

Data Transferring

After the START condition, the I²C bus is busy and data transfer can begin between the master and the addressed slave. Data is transferred over the bus in groups of nine bits, one byte followed by one acknowledge (ACK) bit. The master releases the SDA line during the ninth SCL clock cycle. The slave device can issue an ACK by pulling SDA LOW or issue a not-acknowledge (NACK) by leaving the SDA line high impedance (the external pull-up resistor will hold the line high). Change of data only occurs while the clock line (SCL) is low.

Data Format

After a START condition, the master sends a 7-bit address (factory set at 0010100), followed by a read request (R) or write request (W) bit. The bit R is 1 for a read request and 0 for a write request. If the 7-bit address agrees with the LTC2451's address, the device is selected. When the device is addressed during the conversion state, it does not accept the request and issues a NACK by leaving the SDA line high. If the conversion is complete, the LTC2451 issues an ACK by pulling the SDA line LOW.

The user can send one byte of data into the LTC2451 following a write request and an ACK. The sequence is shown in Figure 3. The write sequence is used solely to set the conversion speed. The default conversion speed is 60Hz. The user can specify a 30Hz conversion speed by setting the eighth bit (S30) = 1, or specify a 60Hz conversion speed by setting the eighth bit (S30) = 0.

After a read request and an ACK, the LTC2451 can output data, as shown in Figure 4. The data output stream is 16 bits long and is shifted out on the falling edges of SCL.

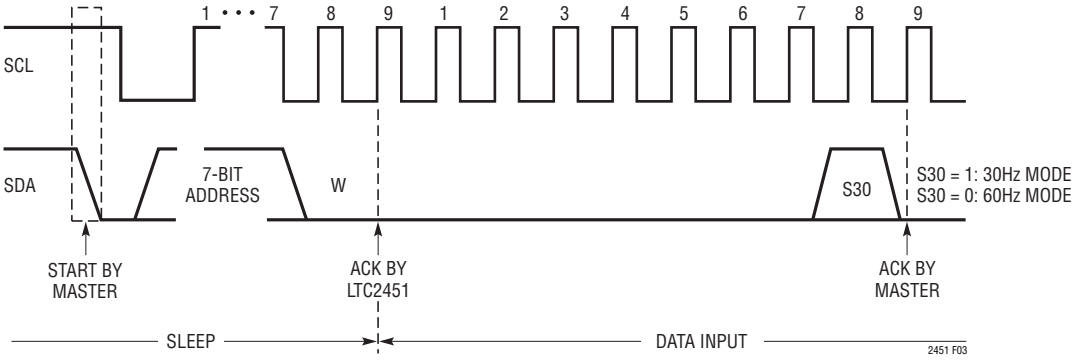


Figure 3. Timing Diagram for Write Sequence

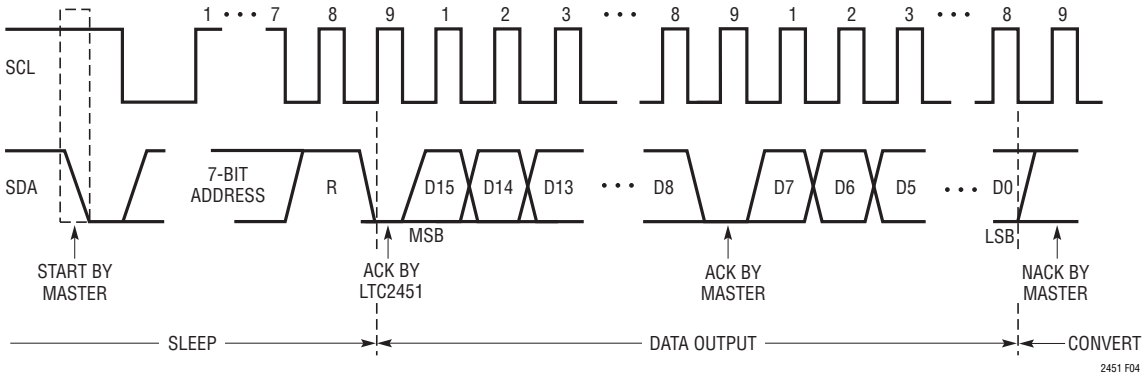


Figure 4. Timing Diagram for Read Sequence

APPLICATIONS INFORMATION

The first bit is the MSB (D15) and is followed by successively less significant bits (D14, D13 ...) until the LSB (D0) is output by the LTC2451. This sequence is summarized in Figure 5.

OPERATION SEQUENCE

Continuous Read

Conversions from the LTC2451 can be continuously read (see Figure 7). At the end of a read operation, a new conversion automatically begins. At the conclusion of the conversion cycle, the next result may be read using the method described above. If the conversion cycle is not concluded and a valid address selects the device, the LTC2451 generates a NACK signal indicating the conversion cycle is in progress.

Continuous Read/Write

Once the conversion cycle is concluded, the LTC2451 can be written to, and then read from, using the repeated START (Sr) command.

Figure 7 shows a cycle which begins with a data write, a repeated START, followed by a read, and concluded with a STOP command. The following conversion begins after all 16 bits are read out of the device, or after the STOP command, and uses the newly programmed configuration.

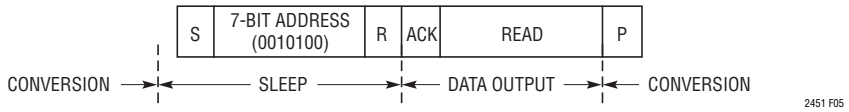


Figure 5. Conversion Sequence

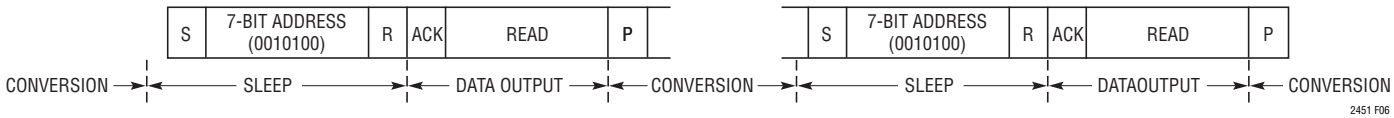


Figure 6. Consecutive Reading at the Same Configuration

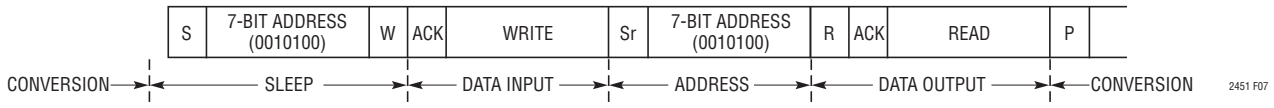


Figure 7. Write, Read, START Conversion

APPLICATIONS INFORMATION

Discarding a Conversion Result and Initiating a New Conversion with Optional Configuration Updating

At the conclusion of a conversion cycle, a write cycle can be initiated. Once the write cycle is acknowledged, a STOP (P) command initiates a new conversion. If a new configuration is required, this data can be written into the device and a STOP command initiates a new conversion (see Figure 8).

Synchronizing the LTC2451 with the Global Address Call

The LTC2451 can also be synchronized with the global address call (see Figure 9). To achieve this, the LTC2451 must first have completed the conversion cycle. The master issues a START, followed by the LTC2451 global address 1110111, and a write request. The LTC2451 will be selected and acknowledge the request. If desired, the master then sends the write byte to program the 30Hz or 60Hz mode. After the optional write byte, the master ends the write operation with a STOP. This will update the configuration registers (if a write byte was sent) and initiate a new conversion on the LTC2451, as shown in Figure 9. In order to synchronize the start of the conversion without affecting the configuration registers, the write operation can be aborted with a STOP. This initiates a new conversion on the LTC2451 without changing the configuration registers.

PRESERVING THE CONVERTER ACCURACY

The LTC2451 is designed to dramatically reduce the conversion result's sensitivity to device decoupling, PCB layout, antialiasing circuits, line and frequency perturbations. Nevertheless, in order to preserve the high accuracy capability of this part, some simple precautions are desirable.

Digital Signal Levels

Due to the nature of CMOS logic, it is advisable to keep input digital signals near GND or V_{CC}. Voltages in the range of 0.5V to V_{CC} – 0.5V may result in additional current leakage from the part.

Driving V_{CC} and GND

In relation to the V_{CC} and GND pins, the LTC2451 combines internal high frequency decoupling with damping elements, which reduce the ADC performance sensitivity to PCB layout and external components. Nevertheless, the very high accuracy of this converter is best preserved by careful low and high frequency power supply decoupling.

A 0.1µF, high quality, ceramic capacitor in parallel with a 10µF ceramic capacitor should be connected between the V_{CC} and GND pins, as close as possible to the package. The 0.1µF capacitor should be placed closest to the ADC.

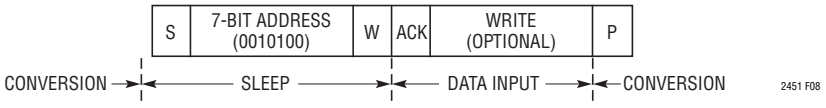


Figure 8. Start a New Conversion without Reading Old Conversion Result

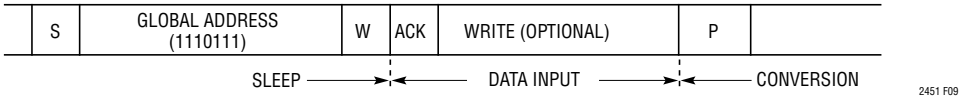


Figure 9. Synchronize the LTC2451 with the Global Address Call

APPLICATIONS INFORMATION

It is also desirable to avoid any via in the circuit path, starting from the converter V_{CC} pin, passing through these two decoupling capacitors, and returning to the converter GND pin. The area encompassed by this circuit path, as well as the path length, should be minimized.

Very low impedance ground and power planes, and star connections at both V_{CC} and GND pins, are preferable. The V_{CC} pin should have three distinct connections: the first to the decoupling capacitors described above, the second to the ground return for the input signal source, and the third to the ground return for the power supply voltage source.

Driving REF+ and REF–

A simplified equivalent circuit for REF+ and REF– is shown in Figure 10. Like all other A/D converters, the LTC2451 is only as accurate as the reference it is using. Therefore, it is important to keep the reference line quiet by careful low and high frequency power supply decoupling.

The LT6660 reference is an ideal match for driving the LTC2451's REF+ pin. The LTC6660 is available in a 2mm × 2mm DFN package with 2.5V, 3V, 3.3V and 5V options.

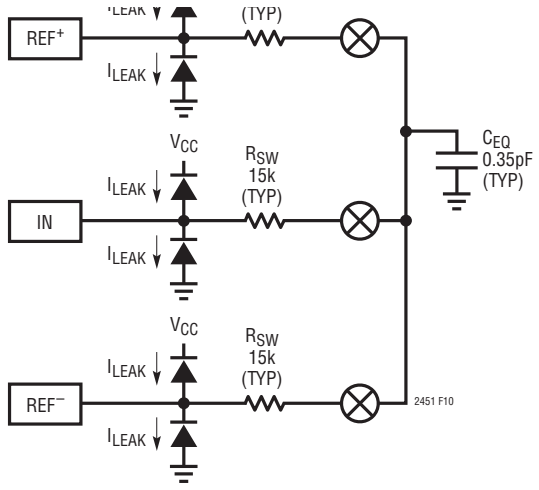


Figure 10. LTC2451 Analog Input and Reference Pins Equivalent Circuit

A 0.1µF, high quality, ceramic capacitor in parallel with a 10µF ceramic capacitor should be connected between the REF+/REF– and GND pins, as close as possible to the package. The 0.1µF capacitor should be placed closest to the ADC.

Driving IN

The input drive requirements can best be analyzed using the equivalent circuit of Figure 11. The input signal, V_{SIG}, is connected to the ADC input pin (IN) through an equivalent source resistance R_S. This resistor includes both the actual generator source resistance and any additional optional resistors connected to the input pin. An optional input capacitor, C_{IN}, is also connected between the ADC input pin and GND. This capacitor is placed in parallel with the ADC input parasitic capacitance, C_{PAR}. Depending on the PCB layout, C_{PAR} has typical values between 2pF and 15pF. In addition, the equivalent circuit of Figure 11 includes the converter equivalent internal resistor, R_{SW}, and sampling capacitor, C_{EQ}.

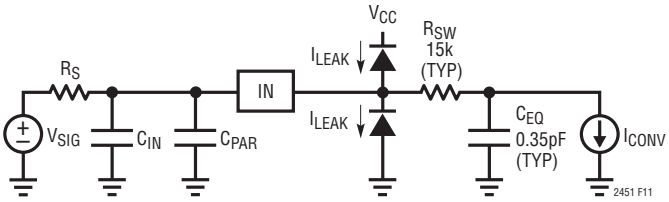


Figure 11. LTC2451 Input Drive Equivalent Circuit

APPLICATIONS INFORMATION

There are some immediate trade-offs in R_S and C_{IN} without needing a full circuit analysis. Increasing R_S and C_{IN} can provide the following benefits:

1. Due to the LTC2451's input sampling algorithm, the input current drawn by the input pin (IN) over a conversion cycle is 50nA. A high $R_S \bullet C_{IN}$ attenuates the high frequency components of the input current, and R_S values up to 1k result in <1LSB additional INL.
2. The bandwidth from V_{SIG} is reduced at the input pin. This bandwidth reduction isolates the ADC from high frequency signals, and as such provides simple anti-aliasing and input noise reduction.
3. Switching transients generated by the ADC are attenuated before they go back to the signal source.
4. A large C_{IN} gives a better AC ground at the input pin, helping reduce reflections back to the signal source.
5. Increasing R_S protects the ADC by limiting the current during an outside-the-rails fault condition.

There is a limit to how large $R_S \bullet C_{IN}$ should be for a given application. Increasing R_S beyond a given point increases the voltage drop across R_S due to the input current, to the point that significant measurement errors exist. Additionally, for some applications, increasing the $R_S \bullet C_{IN}$ product too much may unacceptably attenuate the signal at frequencies of interest.

For most applications, it is desirable to implement C_{IN} as a high quality 0.1µF ceramic capacitor and $R_S \leq 1k$. This capacitor should be located as close as possible to the input pin. Furthermore, the area encompassed by this circuit path, as well as the path length, should be minimized.

In the case of a 2-wire sensor that is not remotely grounded, it is desirable to split R_S and place series resistors in the ADC input line and in the sensor ground return line, which should be tied to the ADC GND pin using a star connection topology.

Figure 12 shows the measured LTC2451 INL versus the input voltage as a function of R_S value with an input capacitor C_{IN} = 0.1µF.

In some cases, R_S can be increased above these guidelines. The input current is negligible when the ADC is

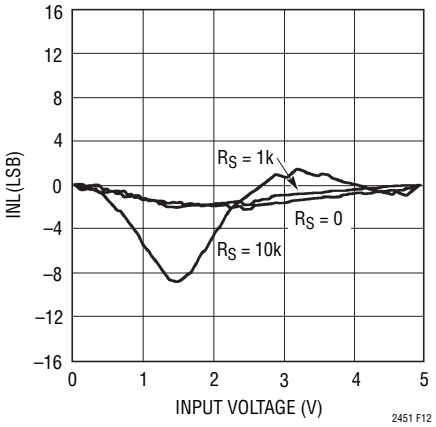


Figure 12. Measured INL vs Input Voltage, C_{IN} = 0.1µF, V_{CC} = 5V, T_A = 25°C

APPLICATIONS INFORMATION

either in sleep or I/O modes. Thus, if the time constant of the input RC circuit $\tau = R_S \bullet C_{IN}$, is of the same order of magnitude or longer than the time periods between actual conversions, then one can consider the input current to be reduced correspondingly.

These considerations need to be balanced out by the input signal bandwidth. The 3dB bandwidth $\approx 1/(2\pi R_S C_{IN})$.

Finally, if the recommended choice for C_{IN} is unacceptable for the user's specific application, an alternate strategy is to eliminate C_{IN} and minimize C_{PAR} and R_S. In practical terms, this configuration corresponds to a low impedance sensor directly connected to the ADC through minimum length traces. Actual applications include current measurements through low value sense resistors, temperature measurements, low impedance voltage source monitoring, and so on. The resultant INL versus V_{IN} is shown in Figure 13. The measurements of Figure 13 include a capacitor C_{PAR} corresponding to a minimum sized layout pad and a minimum width input trace of about 1" length.

Signal Bandwidth and Noise Equivalent Input Bandwidth

The LTC2451 includes a sinc[1] type digital filter with the first notch located at f_0 = 60Hz. As such, the 3dB input signal bandwidth is 26.54Hz. The calculated LTC2451 input signal attenuation versus frequency over a wide frequency range is shown in Figure 14. The calculated LTC2451 input signal attenuation with low frequencies is shown in Figure 15. The converter noise level is about 1.4μV_{RMS}, and can be modeled by a white noise source connected at the input of a noise-free converter.

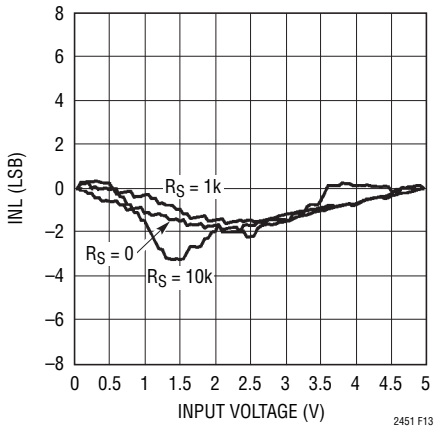


Figure 13. Measured INL vs Input Voltage, C_{IN} = 0, V_{CC} = 5V, T_A = 25°C

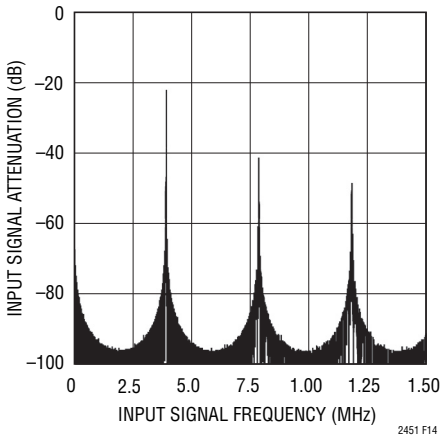


Figure 14. LTC2451 Input Signal Attenuation vs Frequency

APPLICATIONS INFORMATION

For a simple system noise analysis, the input drive circuit can be modeled as a single-pole equivalent circuit characterized by a pole location, f_i, and a noise spectral density, n_i. If the converter has an unlimited bandwidth, or at least a bandwidth substantially larger than f_i, then the total noise contribution of the external drive circuit would be:

$$V_n = n_i\sqrt{\pi / 2 \bullet f_i}$$

The total system noise level can then be estimated as the square root of the sum of (V_n^2) and the square of the LTC2451 noise floor (~2μV^2).

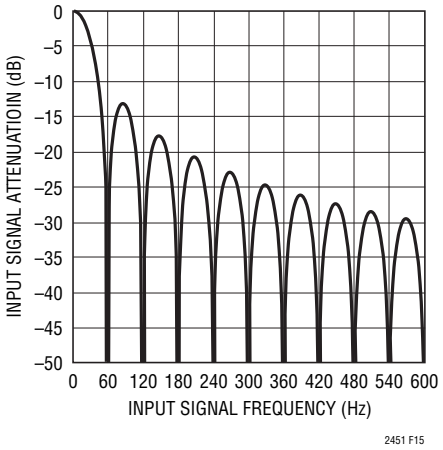
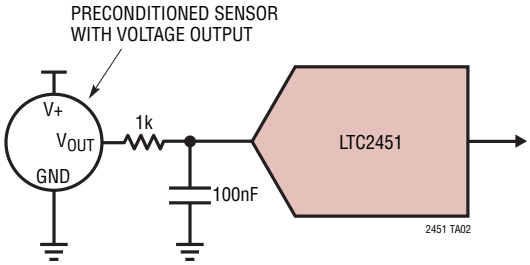


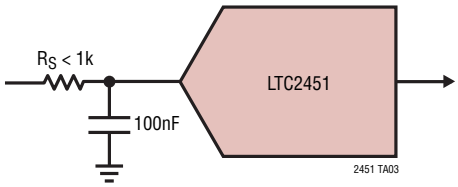
Figure 15. LTC2451 Input Signal Attenuation vs Frequency (Low Frequencies)

TYPICAL APPLICATIONS

Easy Active Input

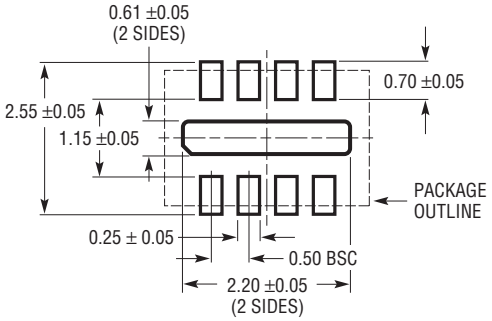


Easy Passive Input

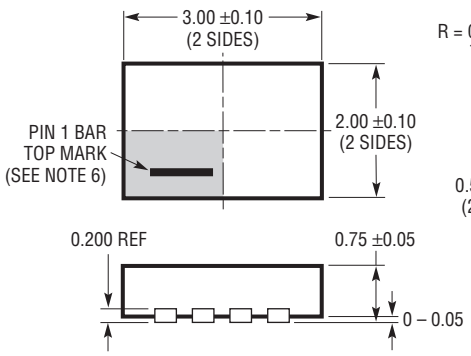


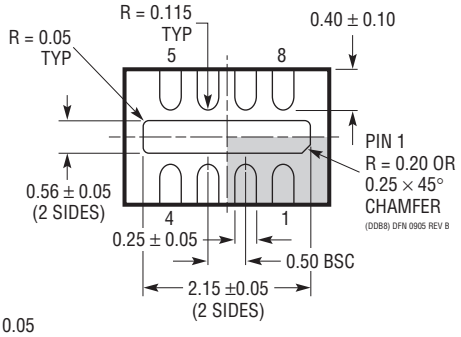
PACKAGE DESCRIPTION

DDB Package
8-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1702 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



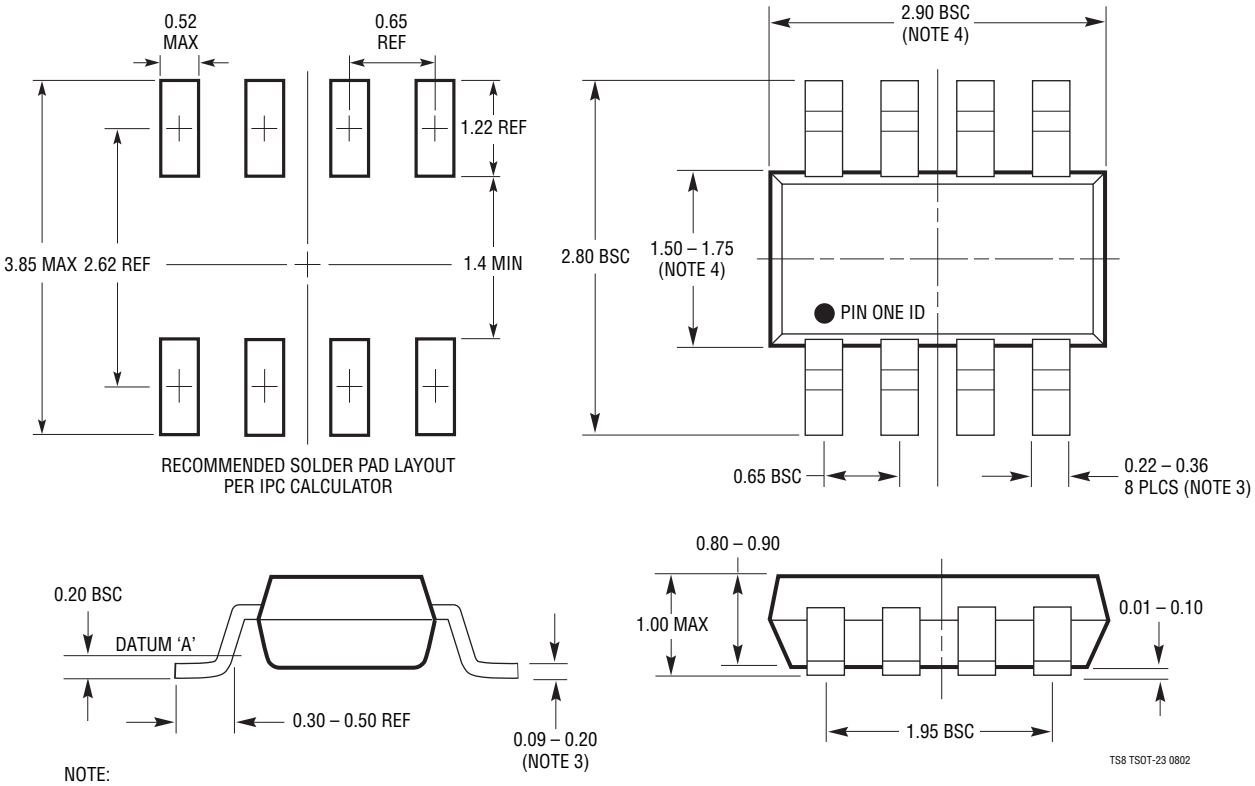


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

REVISION HISTORY (Revision history begins at Rev F)

REV	DATE	DESCRIPTION	PAGE NUMBER
F	6/10	Added text to I^2C Interface section	9
G	10/10	Revised TS8 package part numbers in Order Information section	2