I²C Controlled USB Power Manager/Charger with Overvoltage Protection

FEATURES

- **Switching Regulator with Bat-Track™ Adaptive Output Control Makes Optimal Use of Limited Input Power**
- **I²C Port for Optimal System Performance and Status Information**
- **Input Overvoltage Protection**
- **Bat-Track Control of External Step-Down Switching Regulator Maximizes Efficiency from Automotive and Other High Voltage Sources**
- **Instant-On Operation with Low Battery**
- Optional Overtemperature Battery Conditioner Improves High Temperature Battery Safety Margin
- Ideal Diode Seamlessly Connects Battery When Input Power is Limited or Unavailable
- Full-Featured Li-Ion/Polymer Battery Charger
- 1.5A Maximum Charge Current with Thermal Limiting
- Slew Control Reduces Switching EMI
- 20-Lead 3mm × 4mm × 0.75mm QFN Package

APPLICATIONS

- Media Players
- Portable Navigation Devices
- Smart Phones
- Industrial Handhelds
- Portable Medical Instruments

DESCRIPTION

The LTC®4099 is an I²C controlled high efficiency USB PowerPath™ controller and full-featured Li-Ion/Polymer battery charger. It seamlessly manages power distribution from multiple sources including USB, a wall adapter and a Li-Ion/Polymer battery.

The LTC4099 automatically limits its input current for USB compatibility. For automotive and other high voltage applications, the LTC4099 interfaces with an external switching regulator. Both the USB input and the auxiliary input controller feature Bat-Track optimized charging to provide maximum power to the application and reduced heat in high power density applications.

The I²C port allows digital control of important application parameters including input current limit, charge current and float voltage. Several status bits can also be read back via I²C.

An overvoltage protection circuit guards the LTC4099 from high voltage damage on the low voltage V_{BUS} pin. The LTC4099 is available in a 20-Lead 3mm × 4mm × 0.75mm QFN Package.

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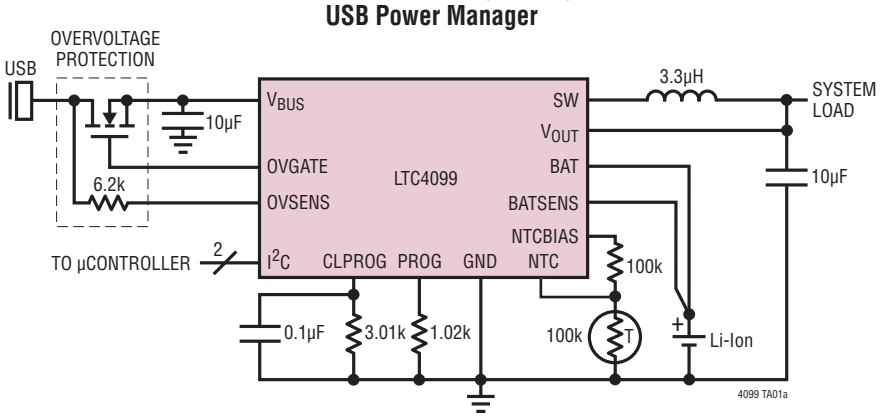
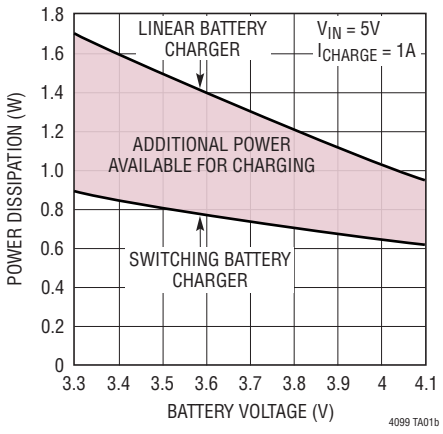
TYPICAL APPLICATION

I²C Controlled High Efficiency Battery Charger/ USB Power Manager



Reduced Power Dissipation vs Linear Battery Charger

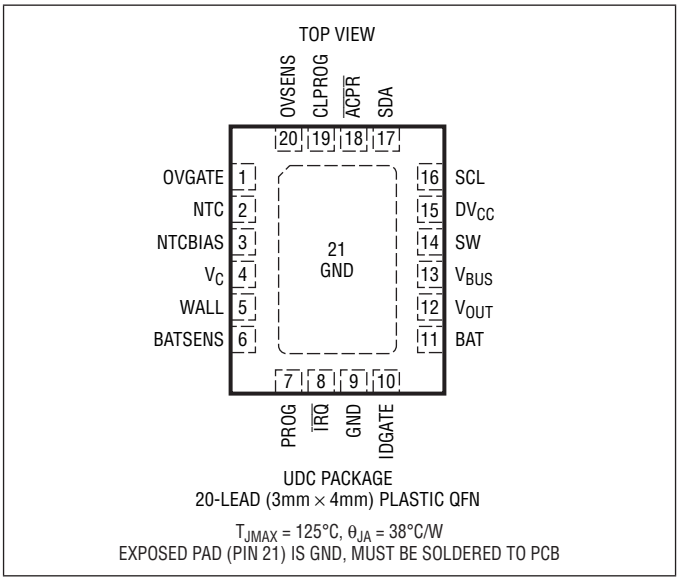


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2, 3)

V_{BUS}, WALL (Transient) t < 1ms, Duty Cycle < 1% ..... –0.3V to 7V
V_{BUS}, WALL (Static), BAT, BATSENS, $\overline{IRQ}$, NTC, DV_{CC} ..... –0.3V to 6V
SDA, SCL ..... –0.3V to Max (V_{BUS}, V_{OUT}, BAT) + 0.3V
I_{OVSENS} ..... ±10mA
I_{CLPROG} 3mA
I_{PROG}, $I_{NTCBIAS}$ 2mA
I_{OUT}, I_{SW}, I_{BAT}, I_{VBUS} 2.25A
Maximum Junction Temperature ..... 125°C
Operating Temperature Range ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C
$I_{\overline{IRQ}}$ 50mA
$I_{\overline{ACPR}}$ ..... ±5mA

PIN CONFIGURATION



UDC PACKAGE
20-LEAD (3mm × 4mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 38°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4099EPDC#PBF	LTC4099EPDC#TRPBF	DQKT	20-Lead (3mm × 4mm) Plastic UTQFN	–40°C to 85°C **(OBSOLETE)**
LTC4099EUDC#PBF	LTC4099EUDC#TRPBF	LFPY	20-Lead (3mm × 4mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{BUS} = 5V, BAT = 3.8V, DV_{CC} = 3.3V, R_{PROG} = 1.02k, R_{CLPROG} = 3.01k, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Power Supply							
V_{BUS}	Input Supply Voltage		●	4.35		5.5	V
$I_{BUS(LIM)}$	Total Input Current	100mA Mode	●	88	93	100	mA
		500mA Mode	●	460	485	500	mA
		620mA Mode		580	620	650	mA
		790mA Mode		725	790	850	mA
		1A Mode		920	965	1000	mA
		1.2A Mode		1150	1220	1295	mA
		Low Power Suspend Mode	●	0.30	0.37	0.5	mA
		High Power Suspend Mode	●	1.6	2.05	2.5	mA
I_{VBUSQ} (Note 4)	Input Quiescent Current	100mA Mode			6		mA
		500mA, 620mA, 790mA, 1A, 1.2A Modes			15		mA
		Low Power Suspend Mode			0.039		mA
		High Power Suspend Mode			0.037		mA

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
h_{CLPROG} (Note 4)	Ratio of Measured V_{BUS} Current to CLPROG Program Current	100mA Mode 500mA Mode 620mA Mode 790mA Mode 1A Mode 1.2A Mode Low Power Suspend Mode High Power Suspend Mode			220 1200 1540 1980 2420 3080 10.9 65		mA/mA mA/mA mA/mA mA/mA mA/mA mA/mA mA/mA mA/mA
I_{VOUT}	V_{OUT} Current Available Before Discharging Battery	100mA Mode, BAT = 3.3V 500mA Mode, BAT = 3.3V 620mA Mode, BAT = 3.3V 790mA Mode, BAT = 3.3V 1A Mode, BAT = 3.3V 1.2A Mode, BAT = 3.3V Low Power Suspend Mode High Power Suspend Mode		 0.23 1.6	135 672 840 1080 1251 1550 0.30 2.16	 0.41 2.46	mA mA mA mA mA mA mA mA
V_{CLPROG}	CLPROG Servo Voltage in Current Limit	Switching Modes Suspend Modes			1.18 102		V mV
V_{UVLO}	V_{BUS} Undervoltage Lockout	Rising Threshold Falling Threshold		 3.90	4.30 4.00	4.35 	V V
V_{DUVLO}	V_{BUS} to BAT Differential Undervoltage Lockout	$V_{BUS–BAT}$ Rising Threshold $V_{BUS–BAT}$ Falling Threshold			200 50		mV mV
V_{OUT}	V_{OUT} Voltage	Switching Modes, BAT = 4.2V, I_{VOUT} = 0mA, Battery Charger Off		4.3	4.5	4.7	V
		Switching Modes, BAT < 3.0V, I_{VOUT} = 0mA, Battery Charger Off		3.5	3.6	3.75	V
		USB Suspend Modes, I_{VOUT} = 250µA		4.5	4.6	4.7	V
f_{OSC}	Switching Frequency			1.96	2.25	2.65	MHz
R_{PMOS}	PMOS On-Resistance				0.18		Ω
R_{NMOS}	NMOS On-Resistance				0.30		Ω
I_{PEAK}	Peak Inductor Current Clamp	500mA to 1.2A Input Limit Modes			3		A
R_{SUSP}	Suspend LDO Output Resistance				16		Ω
Battery Charger							
V_{FLOAT}	BAT Regulated Output Voltage	4.200V Setting Selected by I^2C	 ●	4.179 4.165	4.200 4.200	4.221 4.235	V V
		4.100V Default Setting	 ●	4.079 4.065	4.100 4.100	4.121 4.135	V V
I_{CHG_RANGE}	Constant-Current Mode Charge Current Range	$I_{LIM2/1/0}$ = 101, Selectable by I^2C			500-1200		mA
$I_{CHG500mA}$	Zero-Scale Battery Charge Current	$I_{LIM2/1/0}$ = 101, $I_{CHARGE2/1/0}$ = 000		475	500	525	mA
$I_{CHG1200mA}$	Full-Scale Battery Charge Current	$I_{LIM2/1/0}$ = 101, $I_{CHARGE2/1/0}$ = 111		1100	1200	1300	mA
I_{CHG_STEP}	Charge Current I^2C Step Size	$I_{LIM2/1/0}$ = 101			100		mA
I_{BATQ}	Battery Drain Current	V_{BUS} > V_{UVLO}, Battery Charger Off, I_{VOUT} = 0µA			3.7	5	µA
		V_{BUS} = 0V, I_{VOUT} = 0µA (Ideal Diode Mode)			23	35	µA

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{PROG,TRKL}$	PROG Pin Servo Voltage in Trickle Charge	BAT < V_{TRKL}			0.100		V
h_{PROG}	Ratio of I_{BAT} to PROG Pin Current				1030		mA/mA
V_{TRKL}	Trickle Charge Threshold Voltage	BAT Rising		2.7	2.85	3	V
ΔV_{TRKL}	Trickle Charge Hysteresis Voltage				130		mV
V_{RECHRG}	Recharge Battery Threshold Voltage	Threshold Voltage Relative to V_{FLOAT}		–75	–100	–125	mV
t_{TERM_RANGE}	Safety Timer Termination Period Range	Selectable by I^2C, Timer Starts When BAT = V_{FLOAT}			1-8		Hour
t_{BADBAT}	Bad Battery Termination Time	BAT < V_{TRKL}		0.4	0.5	0.6	Hour
$V_{C/x}$	Full Capacity Charge Indication PROG Voltage (Note 5)	COVERX1/0 = 00		90	100	110	mV
		COVERX1/0 = 01		40	50	60	mV
		COVERX1/0 = 10		190	200	210	mV
		COVERX1/0 = 11		490	500	510	mV
R_{ON_CHG}	Battery Charger Power FET On-Resistance (Between V_{OUT} and BAT)	I_{BAT} = 200mA			0.18		Ω
T_{LIM}	Junction Temperature in Constant Temperature Mode	Selectable by I^2C			85, 105		°C
Bat-Track External Switching Regulator Control							
V_{WALL}	Absolute WALL Input Threshold	Rising Threshold Falling Threshold		4.15	4.3 3.2	4.45	V V
ΔV_{WALL}	Differential WALL Input Threshold	WALL–BAT Rising Threshold WALL–BAT Falling Threshold		 0	90 37	 50	mV mV
V_{OUT}	Regulation Target Under V_C Control			3.5	BAT + 0.3		V
I_{WALLQ}	WALL Quiescent Current				130		µA
$R_{\overline{ACPR}}$	$\overline{ACPR}$ Pull-Down Strength				150		Ω
$VH_{\overline{ACPR}}$	$\overline{ACPR}$ High Voltage	$I_{\overline{ACPR}}$ = 0mA			V_{OUT}		V
$VL_{\overline{ACPR}}$	$\overline{ACPR}$ Low Voltage	$I_{\overline{ACPR}}$ = 0mA			0		V
Overvoltage Protection							
$V_{OVCUTOFF}$	Overvoltage Protection Threshold	Rising Threshold, R_{OVSENS} = 6.2k		6.10	6.35	6.70	V
V_{OVGATE}	OVGATE Output Voltage	Input Below $V_{OVCUTOFF}$ Input Above $V_{OVCUTOFF}$			1.88 • V_{OVSENS} 0	12	V V
$V_{OVGATELOAD}$	OVGATE Voltage with 1µA Load	5V Through 6.2k into OVSENS		8	8.6		V
$I_{OVSENSQ}$	OVSENS Quiescent Current	V_{OVSENS} = 5V			40		µA
t_{RISE}	OVGATE Time to Reach Regulation	C_{OVGATE} = 1nF			2.5		ms
Overtemperature Battery Conditioner							
$I_{DISCHARGE}$	Overtemperature Battery Discharge Current	Only When Enabled via I^2C Control, BAT = 4.2V			180		mA
V_{ALLOW}	Maximum Allowed Overtemperature Battery Voltage	Only When Enabled via I^2C Control			3.85		V

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
NTC							
V_{TOO_COLD}	Cold Temperature Fault Threshold Voltage	Rising Threshold Hysteresis		72.3	73.8 3.6	75.3	%NTCBIAS %NTCBIAS
V_{TOO_WARM}	Hot Temperature Fault Threshold Voltage	Falling Threshold Hysteresis		31.3	32.6 3.3	33.9	%NTCBIAS %NTCBIAS
$V_{OVERTEMP}$	Critically High Temperature Fault Threshold Voltage	Falling Threshold Hysteresis		21.9	22.8 50	23.7	%NTCBIAS mV
I_{NTC}	NTC Leakage Current	NTC = NTCBIAS		–50		50	nA
Ideal Diode							
V_{FWD}	Forward Voltage	I_{VOUT} = 10mA			15		mV
$R_{DROPOUT}$	Internal Diode On-Resistance, Dropout	I_{VOUT} = 200mA			0.18		Ω
I_{MAX}	Diode Current Limit			2			A
I^2C Port							
DV_{CC}	I^2C Logic Reference			1.6		5.5	V
I_{DVCCQ}	DV_{CC} Current	SCL/SDA = 0kHz			0.2		µA
V_{DVCC_UVLO}	DV_{CC} UVLO				1		V
ADDRESS	I^2C Address			$0001001\left[\frac{R}{\overline{W}}\right]$			
$V_{\overline{IRQ}}$	$\overline{IRQ}$ Pin Output Low Voltage	$I_{\overline{IRQ}}$ = 5mA			65	100	mV
$I_{\overline{IRQ}}$	$\overline{IRQ}$ Pin Leakage Current	$V_{\overline{IRQ}}$ = 5V			0	1	µA
V_{IH}, SDA, SCL	Input High Threshold			0.7 • DV_{CC}			V
V_{IL}, SDA, SCL	Input Low Threshold					0.3 • DV_{CC}	V
I_{IH}, SDA, SCL	Input Leakage High	SDA, SCL = DV_{CC}		–1		1	µA
I_{IL}, SDA, SCL	Input Leakage Low	SDA, SCL = 0V		–1		1	µA
V_{OL}	Digital Output Low (SDA)	I_{SDA} = 3mA				0.4	V
f_{SCL}	Clock Operating Frequency					400	kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition			1.3			µs
t_{HD_SDA}	Hold Time After (Repeated) Start Condition			0.6			µs
t_{SU_SDA}	Repeated Start Condition Set-Up Time			0.6			µs
t_{SU_STO}	Stop Condition Time			0.6			µs
$t_{HD_DAT(OUT)}$	Data Hold Time			0		900	ns
$t_{HD_DAT(IN)}$	Input Data Hold Time			0			ns
t_{SU_DAT}	Data Set-Up Time			100			ns
t_{LOW}	Clock Low Period			1.3			µs
t_{HIGH}	Clock High Period			0.6			µs
t_{SP}	Spike Suppression Time					50	ns

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC4099 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: The LTC4099 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 4: Total input current is the sum of quiescent current, I_{VBUSQ}, and measured current given by:

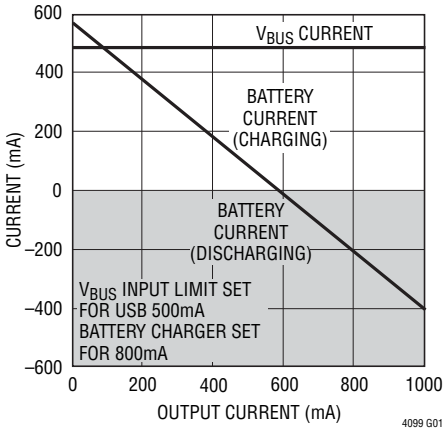
$V_{CLPROG}/R_{CLPROG} \bullet (h_{CLPROG} + 1)$

Note 5: The PROG pin always represents actual charge current. See the Full Capacity Charge Indication (C/x) section.

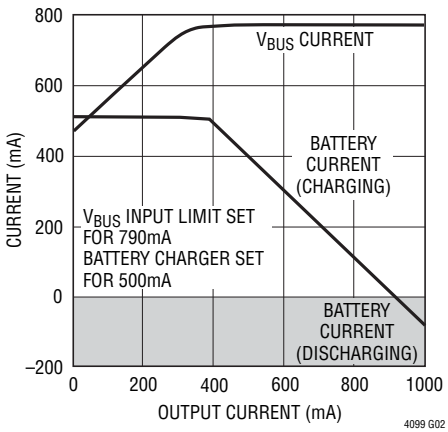
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{BUS} = 5V, BAT = 3.8V, R_{PROG} = 1.02k, R_{CLPROG} = 3.01k, unless otherwise noted.

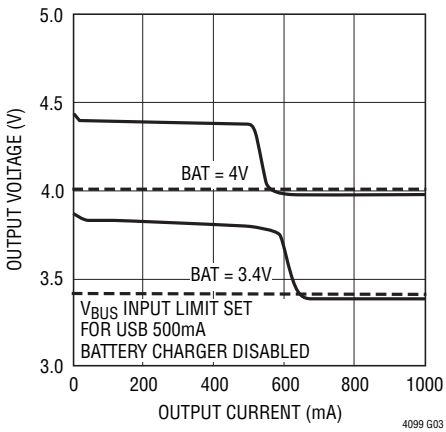
Battery and V_{BUS} Currents vs Output Current



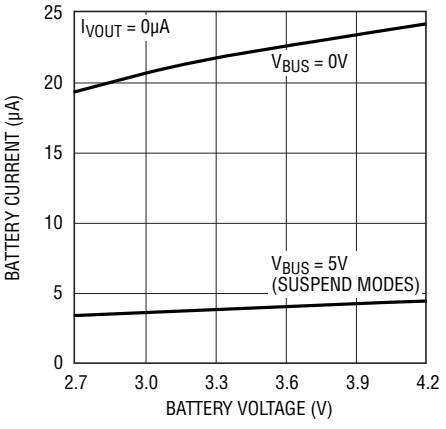
Battery and V_{BUS} Currents vs Output Current



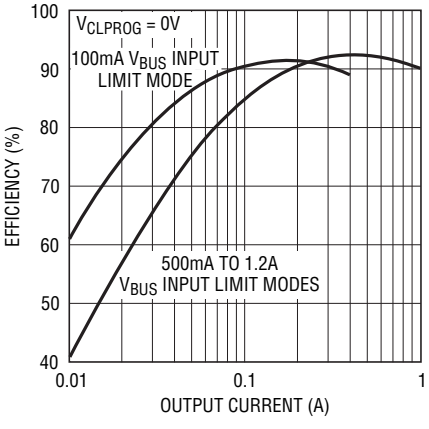
Output Voltage vs Output Current



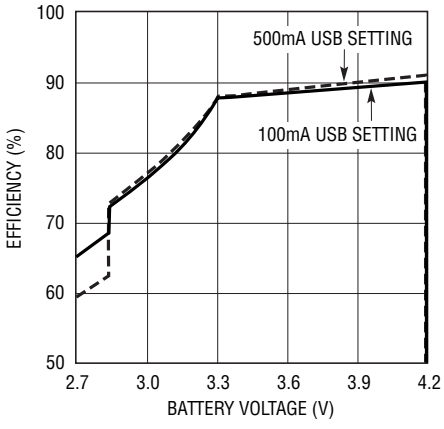
Battery Drain Current vs Battery Voltage



PowerPath Switching Regulator Efficiency vs Output Current



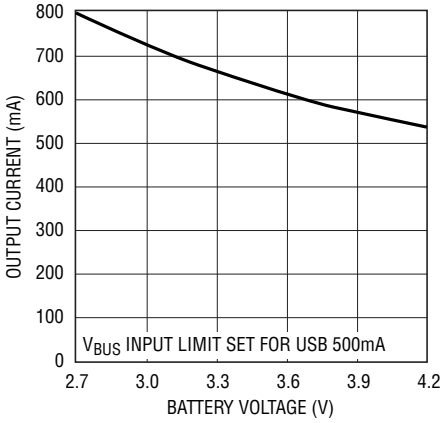
Battery Charging Efficiency vs Battery Voltage with No External Load (P_{BAT}/P_{VBUS})



TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{BUS} = 5V, BAT = 3.8V, R_{PROG} = 1.02k, R_{CLPROG} = 3.01k, unless otherwise noted.

USB Compliant Output Current Available Before Discharging Battery



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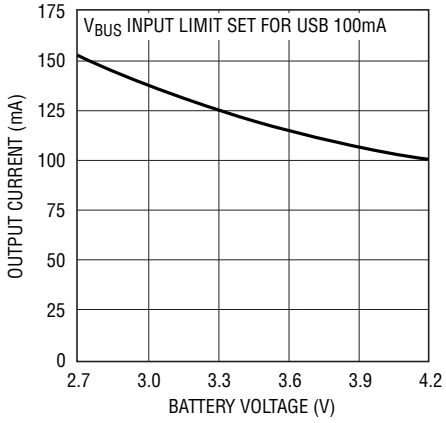
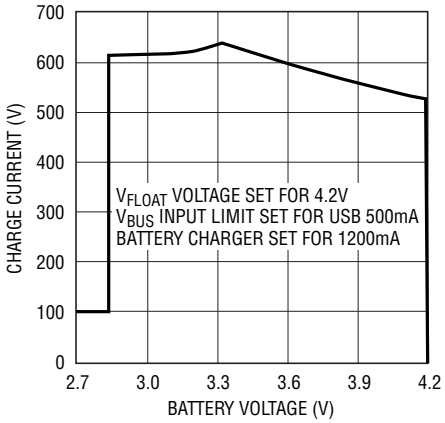


USB Limited Battery Charge Current vs Battery Voltage



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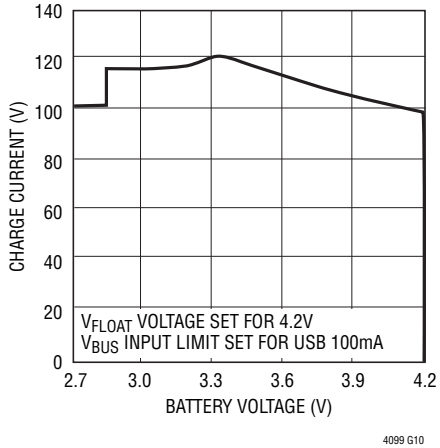
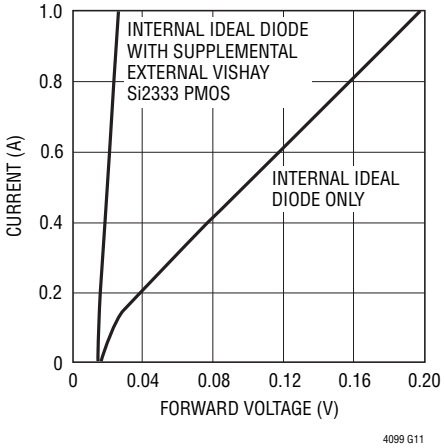
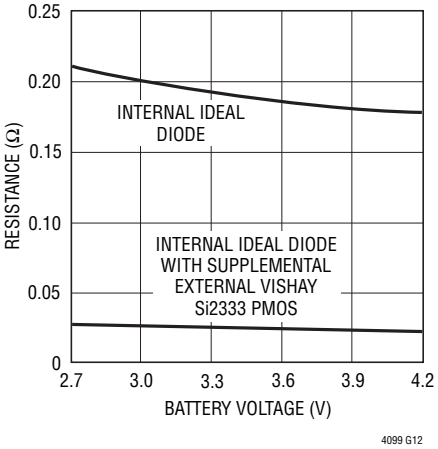


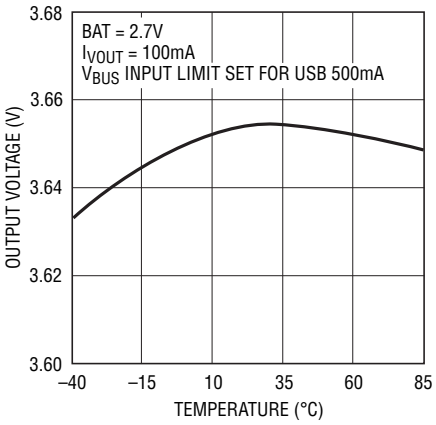
Ideal Diode V-I Characteristics



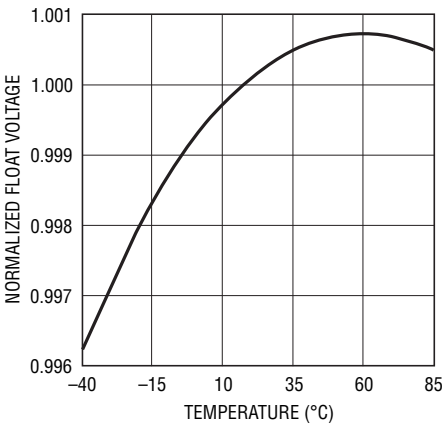
Ideal Diode Resistance vs Battery Voltage



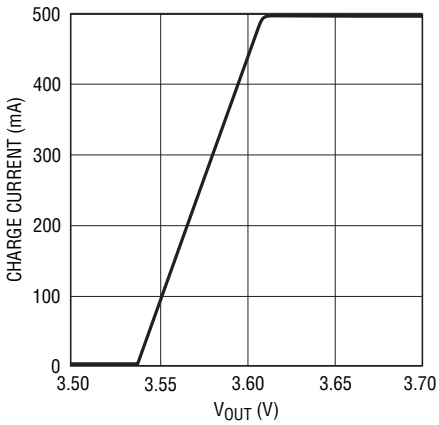
Low Battery (Instant-On) Output Voltage vs Temperature



Normalized Battery Charger Float Voltage vs Temperature



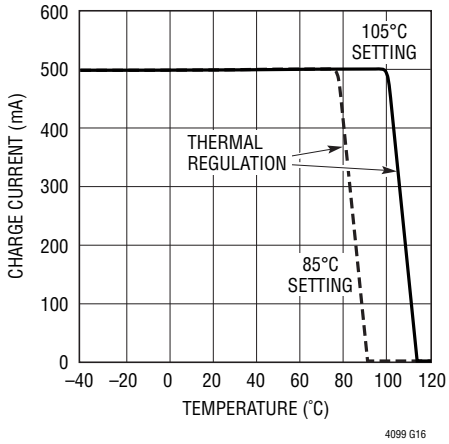
Automatic Low Battery Charge Current Reduction



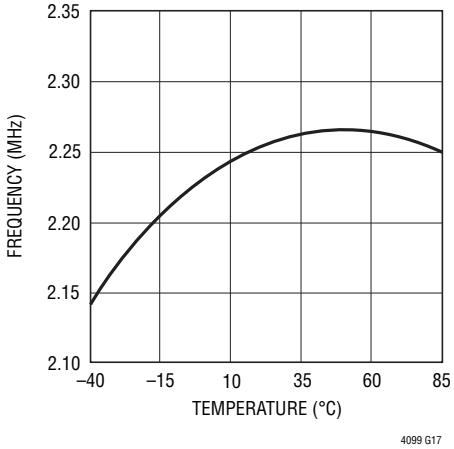
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{BUS} = 5V, BAT = 3.8V, R_{PROG} = 1.02k, R_{CLPROG} = 3.01k, unless otherwise noted.

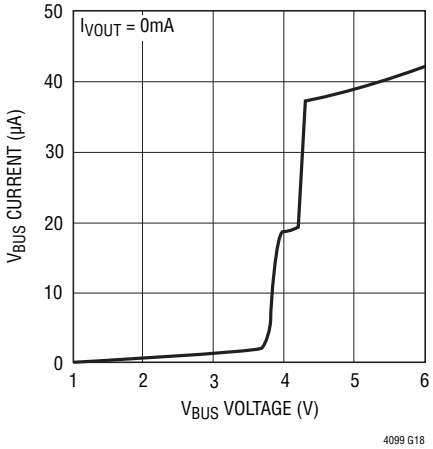
Battery Charge Current vs Temperature



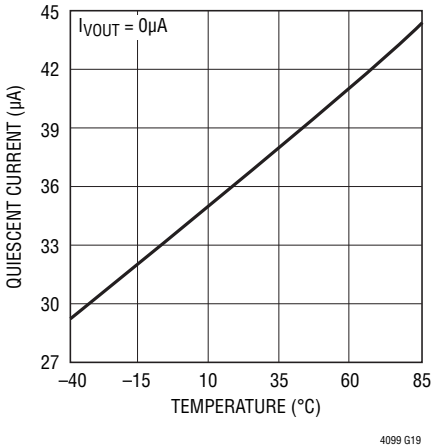
Oscillator Frequency vs Temperature



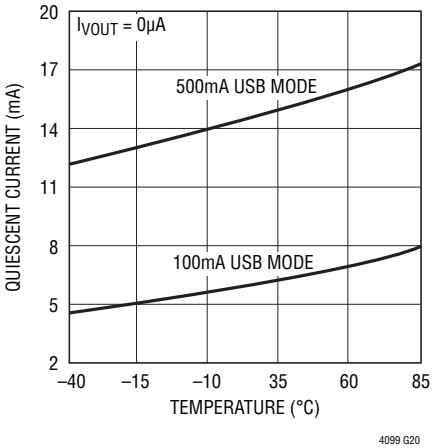
V_{BUS} Current vs V_{BUS} Voltage (Suspend)



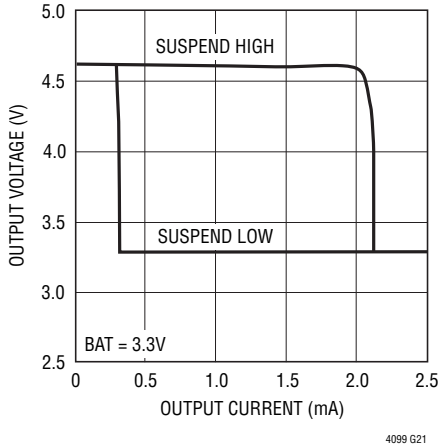
V_{BUS} Quiescent Current in Suspend vs Temperature



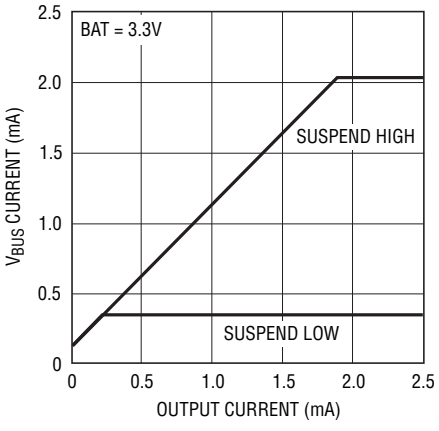
V_{BUS} Quiescent Current vs Temperature



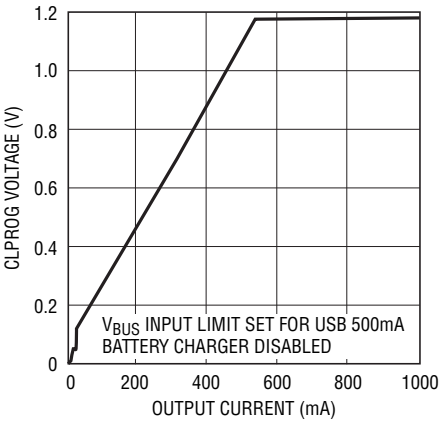
Output Voltage vs Output Current in Suspend



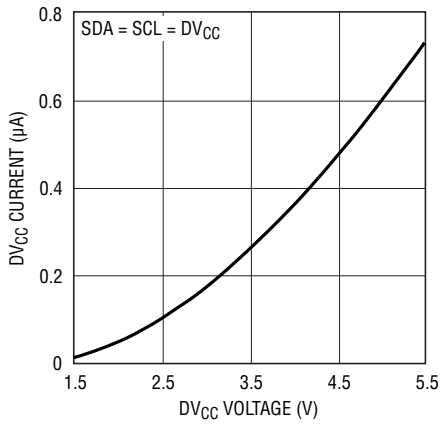
V_{BUS} Current vs Output Current in Suspend



CLPROG Voltage vs Output Current



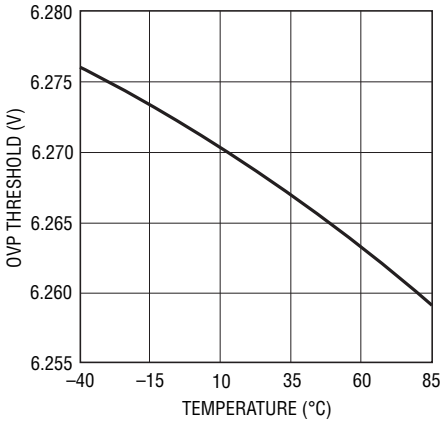
Static DV_{CC} Current vs Voltage



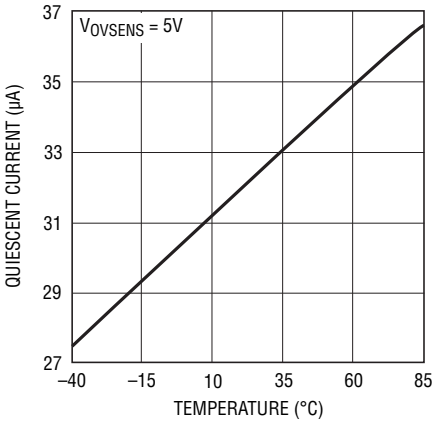
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{BUS} = 5V, BAT = 3.8V, R_{PROG} = 1.02k, R_{CLPROG} = 3.01k, unless otherwise noted.

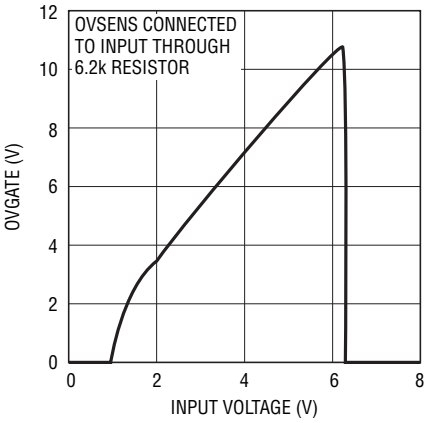
Rising Overvoltage Threshold vs Temperature



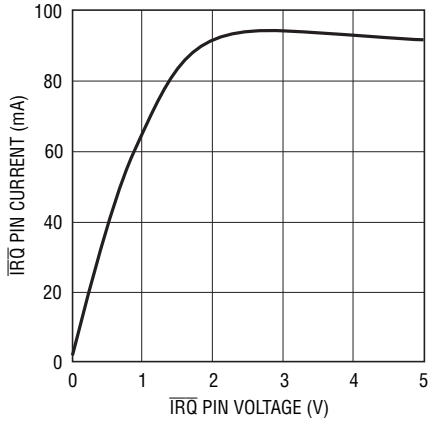
OVSENS Quiescent Current vs Temperature



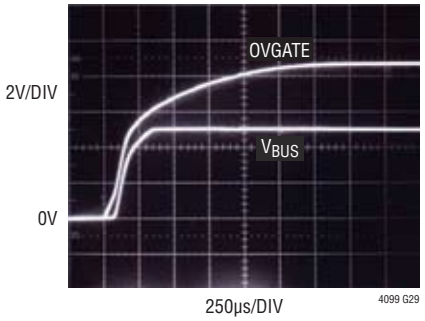
OVGATE vs OVSENS



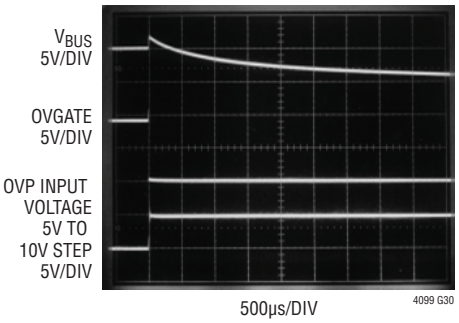
$\overline{IRQ}$ Pin Current vs Voltage (Pull-Down State)



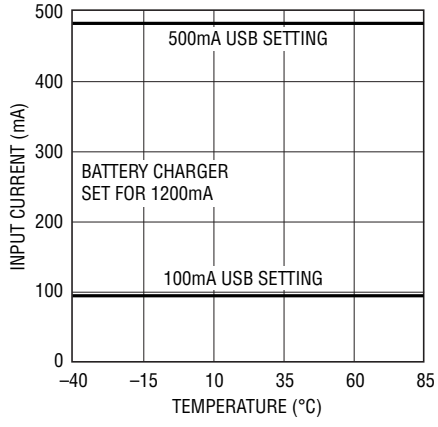
OVP Connection Waveform



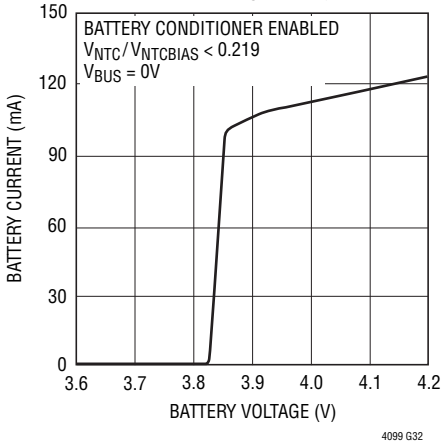
OVP Disconnect Waveform



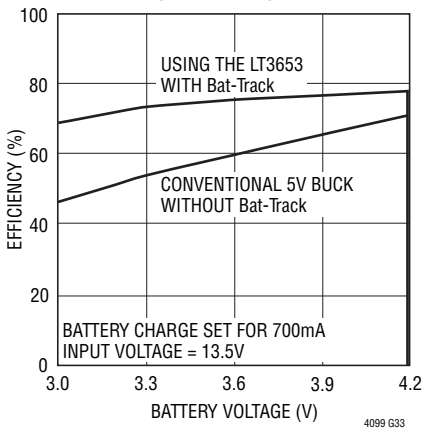
Input Current vs Temperature



Battery Safety Conditioner Discharge Current vs Battery Voltage



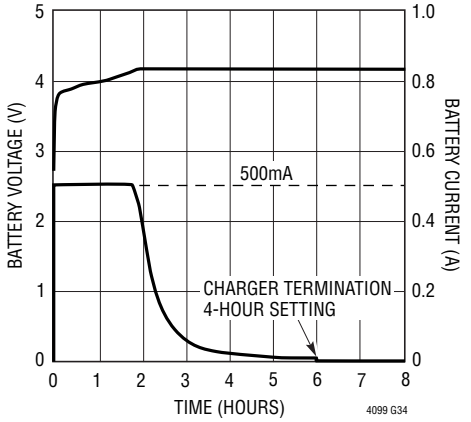
High Voltage Input Charging Efficiency vs Battery Voltage



TYPICAL PERFORMANCE CHARACTERISTICS

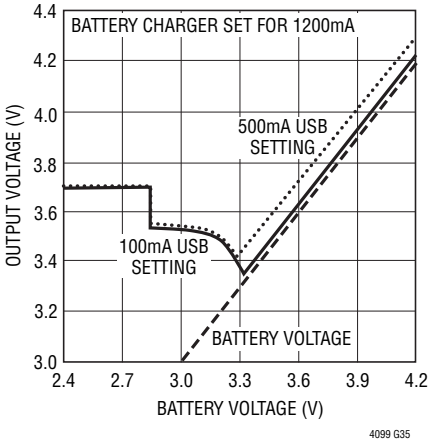
T_A = 25°C, V_{BUS} = 5V, BAT = 3.8V, R_{PROG} = 1.02k, R_{CLPROG} = 3.01k, unless otherwise noted.

Battery Charge Current and Voltage vs Time

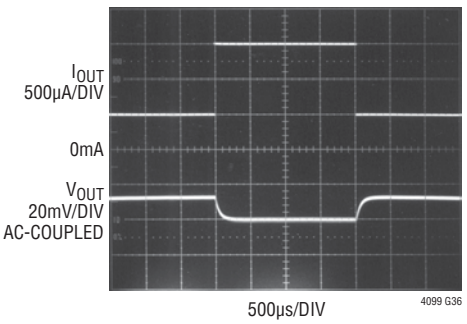


V_{BUS} INPUT LIMIT SET FOR 790mA
BATTERY CHARGER SET FOR 500mA
FLOAT VOLTAGE SET FOR 4.2V

Output Voltage vs Battery Voltage; Battery Charger Overprogrammed



Suspend LDO Transient Response (500µA to 1.5mA)



PIN FUNCTIONS

OVGATE (Pin 1): Overvoltage Protection Gate Output. Connect OVGATE to the gate pin of an external N-channel MOSFET pass transistor. The source of the transistor should be connected to V_{BUS} and the drain should be connected to the product's DC input connector. In the absence of an overvoltage condition, this pin is driven from an internal charge pump capable of creating sufficient overdrive to fully enhance the pass transistor. If an overvoltage condition is detected, OVGATE is brought rapidly to GND to prevent damage to the LTC4099. OVGATE works in conjunction with OVSENS to provide this protection.

NTC (Pin 2): Input to the Negative Temperature Coefficient Thermistor Monitoring Circuit. The NTC pin connects to a negative temperature coefficient thermistor which is typically copackaged with the battery to determine if the battery is too hot or too cold to charge. If the battery's temperature is out of range, charging is paused until the battery temperature re-enters the valid range. A low drift bias resistor is required from NTCBIAS to NTC and a thermistor is required from NTC to ground.

NTCBIAS (Pin 3): NTC Thermistor Bias Output. Connect a bias resistor between NTCBIAS and NTC, and a thermistor between NTC and GND.

V_C (Pin 4): Bat-Track Auxiliary Switching Regulator Control Output. This pin drives the V_C pin of an external Linear Technology step-down switching regulator. In conjunction with WALL and $\overline{ACPR}$, it will regulate V_{OUT} to maximize battery charger efficiency.

WALL (Pin 5): Auxiliary Power Source Sense Input. WALL is used to determine when power is available from an auxiliary power source. When power is detected, $\overline{ACPR}$ is driven low and the USB input is automatically disabled.

BATSENS (Pin 6): Battery Voltage Sense Input. For proper operation, this pin must always be connected to BAT. For best operation, connect BATSENS to BAT physically close to the Li-Ion cell.

PROG (Pin 7): Charge Current Program and Charge Current Monitor Pin. Connecting a resistor from PROG to ground programs the charge current. If sufficient input power is available in constant-current mode, this pin servos to one of eight possible I^2C controllable voltages (see Table 3). The voltage on this pin always represents the *actual* charge current by using the following formula:

$$I_{BAT} = \frac{V_{PROG}}{R_{PROG}} \bullet 1030$$

PIN FUNCTIONS

$\overline{IRQ}$ (Pin 8): Open-Drain Interrupt Output. The $\overline{IRQ}$ pin can be used to generate an interrupt due to a multitude of maskable status change events within the LTC4099. See Table 1.

GND (Pin 9, Exposed Pad Pin 21): Ground. The Exposed Pad and pin must be soldered to the PCB to provide a low electrical and thermal impedance connection to ground.

IDGATE (Pin 10): Ideal Diode Amplifier Output. This pin controls the gate of an external P-channel MOSFET transistor used to supplement the internal ideal diode. The source of the P-channel MOSFET should be connected to V_{OUT} and the drain should be connected to BAT.

BAT (Pin 11): Single-Cell Li-Ion Battery Pin. Depending on available power and load, a Li-Ion battery on BAT will either deliver system power to V_{OUT} through the ideal diode or be charged from the battery charger.

V_{OUT} (Pin 12): Output Voltage of the Switching PowerPath Controller and Input Voltage of the Battery Charger. The majority of the portable product should be powered from V_{OUT}. The LTC4099 will partition the available power between the external load on V_{OUT} and the internal battery charger. Priority is given to the external load and any extra power is used to charge the battery. An ideal diode from BAT to V_{OUT} ensures that V_{OUT} is powered even if the load exceeds the allotted power from V_{BUS} or if the V_{BUS} power source is removed. V_{OUT} should be bypassed with a low impedance multilayer ceramic capacitor.

V_{BUS} (Pin 13): Input Voltage for the Switching PowerPath Controller. V_{BUS} will usually be connected to the USB port of a computer or a DC output wall adapter. V_{BUS} should be bypassed with a low impedance multilayer ceramic capacitor.

SW (Pin 14): Switching Regulator Power Transmission Pin. The SW pin delivers power from V_{BUS} to V_{OUT} via the step-down switching regulator. An inductor should be connected from SW to V_{OUT}. See the Applications Information section for a discussion of inductance value.

DV_{CC} (Pin 15): Logic Reference for the I^2C Serial Port. A 0.01µF bypass capacitor is required.

SCL (Pin 16): Clock Input for the I^2C Serial Port. The I^2C input levels are scaled with respect to DV_{CC}.

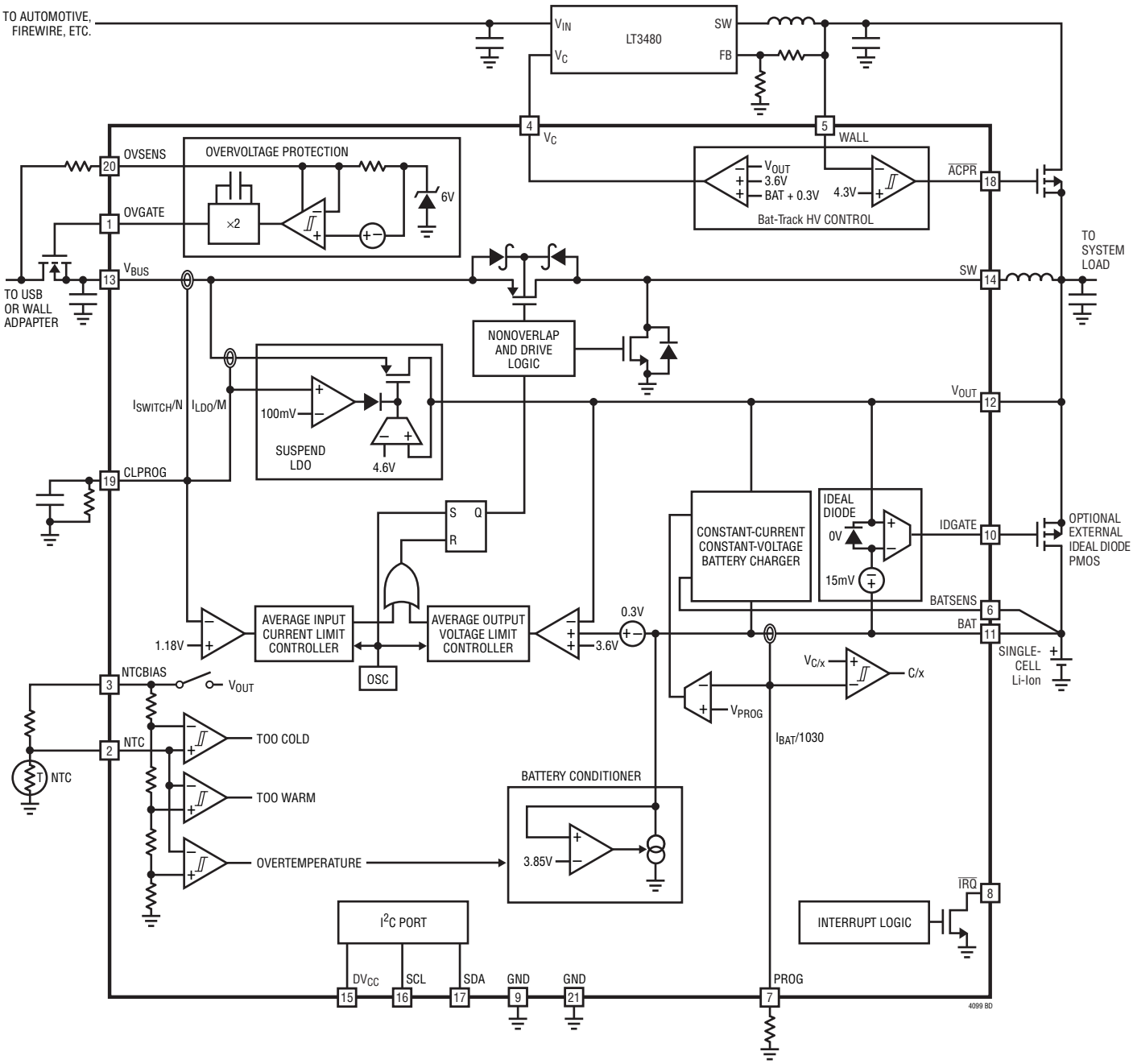
SDA (Pin 17): Data Input/Output for the I^2C Serial Port. The I^2C input levels are scaled with respect to DV_{CC}.

$\overline{ACPR}$ (Pin 18): Auxiliary Power Source Present Output (Active Low). $\overline{ACPR}$ indicates that the output of an external high voltage step-down switching regulator connected to WALL is suitable for use by the LTC4099. $\overline{ACPR}$ may be connected to the gate of an external P-channel MOSFET transistor whose source is connected to V_{OUT} and whose drain is connected to WALL. $\overline{ACPR}$ has a high level of V_{OUT} and a low level of GND.

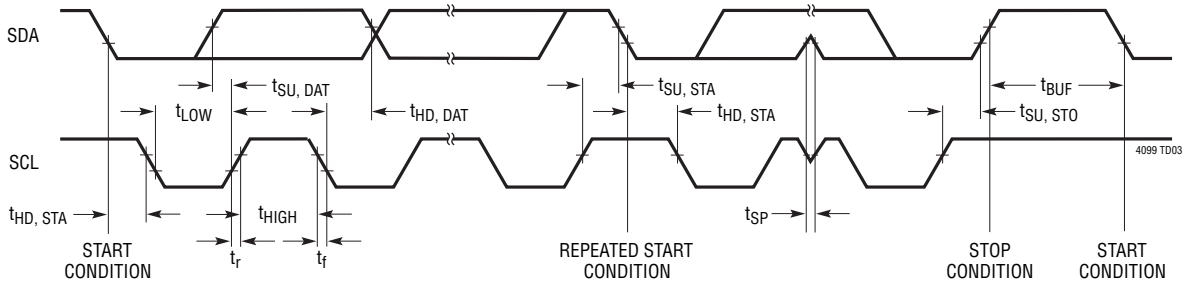
CLPROG (Pin 19): USB Current Limit Program and Monitor Pin. A 1% resistor from CLPROG to ground determines the upper limit of the current drawn from the V_{BUS} pin. A precise fraction of the input current, h_{CLPROG}, is sent to the CLPROG pin when the high side switch is on. The switching regulator delivers power until the CLPROG pin reaches 1.18V. Therefore, the current drawn from V_{BUS} will be limited to an amount given by h_{CLPROG} and R_{CLPROG}. There are a multitude of ratios for h_{CLPROG} available by I^2C control, two of which correspond to the 100mA and 500mA USB specifications (see Table 2). A multilayer ceramic averaging capacitor is also required at CLPROG for filtering.

OVSENS (Pin 20): Overvoltage Protection Sense Input. OVSENS should be connected through a 6.2k resistor to the input power connector and the drain of an external N-channel MOSFET pass transistor. When the voltage on this pin exceeds $V_{OVCUTOFF}$, the OVGATE pin will be pulled to GND to disable the pass transistor and protect the LTC4099 from potentially damaging high voltage.

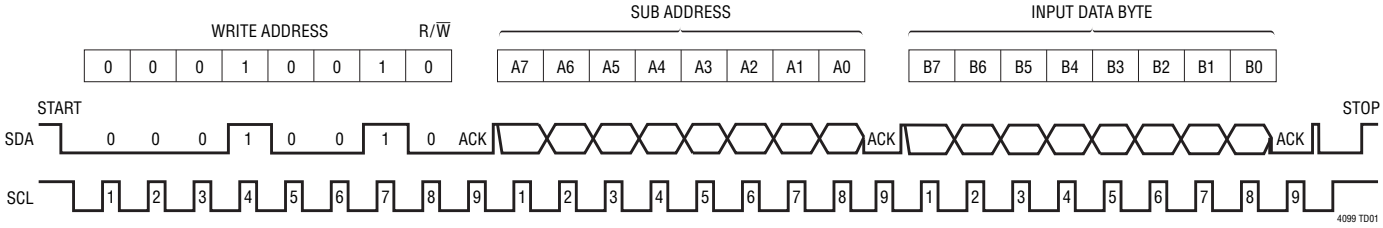
BLOCK DIAGRAM



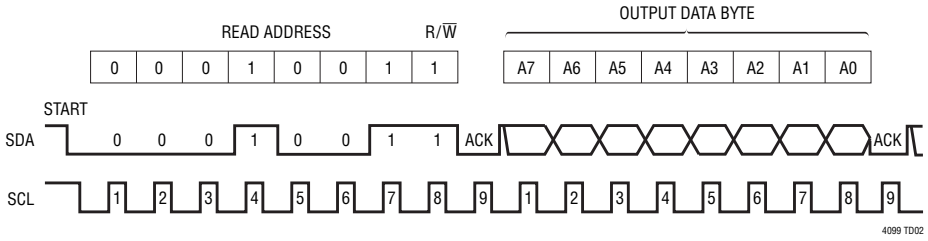
TIMING DIAGRAM



I²C Write Protocol



I²C Read Protocol



OPERATION

Introduction

The LTC4099 is an I²C controlled power manager and Li-Ion charger designed to make optimal use of the power available from a variety of sources while minimizing power dissipation and easing thermal budgeting constraints. The innovative PowerPath architecture ensures that the application is powered immediately after external voltage is applied, even with a completely dead battery, by prioritizing power to the application.

The LTC4099 includes a Bat-Track monolithic step-down switching regulator for USB, wall adapters and other 5V sources. Designed specifically for USB applications, the switching regulator incorporates a precision average input current limit for USB compatibility. Because power is conserved, the LTC4099 allows the load current on V_{OUT} to exceed the current drawn by the USB port making maximum use of the allowable USB power for battery charging. The switching regulator and battery charger communicate to ensure that the average input current never exceeds the USB specifications.

For automotive and other high voltage applications, the LTC4099 provides Bat-Track control of an external Linear Technology step-down switching regulator to maximize battery charger efficiency and minimize heat production.

When power is available from both the USB and an auxiliary input, the auxiliary input is prioritized.

The LTC4099 contains both an internal 180mΩ ideal diode as well as an ideal diode controller for use with an external P-channel MOSFET. The ideal diodes from BAT to V_{OUT} guarantee that ample power is always available to V_{OUT} even if there is insufficient or absent power at V_{BUS} or WALL.

The LTC4099 features an overvoltage protection circuit which is designed to work with an external N-channel MOSFET to prevent damage to its input caused by accidental application of high voltage.

To prevent battery drain when a device is connected to a suspended USB port, an LDO from V_{BUS} to V_{OUT} provides either a low power or high power USB suspend current to the application.

Finally, the LTC4099 has considerable adjustability built in so that power levels and status information can be controlled and monitored via a simple two wire I²C port.

Bat-Track Input Current Limited Step-Down Switching Regulator

The power delivered from V_{BUS} to V_{OUT} is controlled by a 2.25MHz constant-frequency step-down switching regulator. To meet the maximum USB load specification, the switching regulator contains a measurement and control system which ensures that the average input current remains below the level programmed at the CLPROG pin and I²C port. V_{OUT} drives the combination of the external load and the battery charger.

If the combined load does not cause the switching power supply to reach the programmed input current limit, V_{OUT} will track approximately 0.3V above the battery voltage. By keeping the voltage across the battery charger at this low level, power lost to the battery charger is minimized. Figure 1 shows the power path components.

If the combined external load plus battery charge current is large enough to cause the switching power supply to reach the programmed input current limit, the battery charger will reduce its charge current by precisely the amount necessary to enable the external load to be satisfied. Even if the battery charge current is programmed to exceed the allowable USB power, the USB specification for average input current will not be violated; the battery charger will reduce its current as needed. Furthermore, if the load current at V_{OUT} exceeds the programmed power from V_{BUS}, the extra load current will be drawn from the battery via the ideal diodes even when the battery charger is enabled.

The current out of CLPROG is a precise fraction of the V_{BUS} current. When a programming resistor and an averaging capacitor are connected from CLPROG to GND, the voltage on CLPROG represents the average input current of the switching regulator. As the input current approaches the programmed limit, CLPROG reaches 1.18V and power delivered by the switching regulator is held constant.

The input current limit has eight possible settings ranging from the USB suspend limit of 500µA up to 1.2A for wall adapter applications. Two of these settings are specifically intended for use in the 100mA and 500mA USB applications.

OPERATION

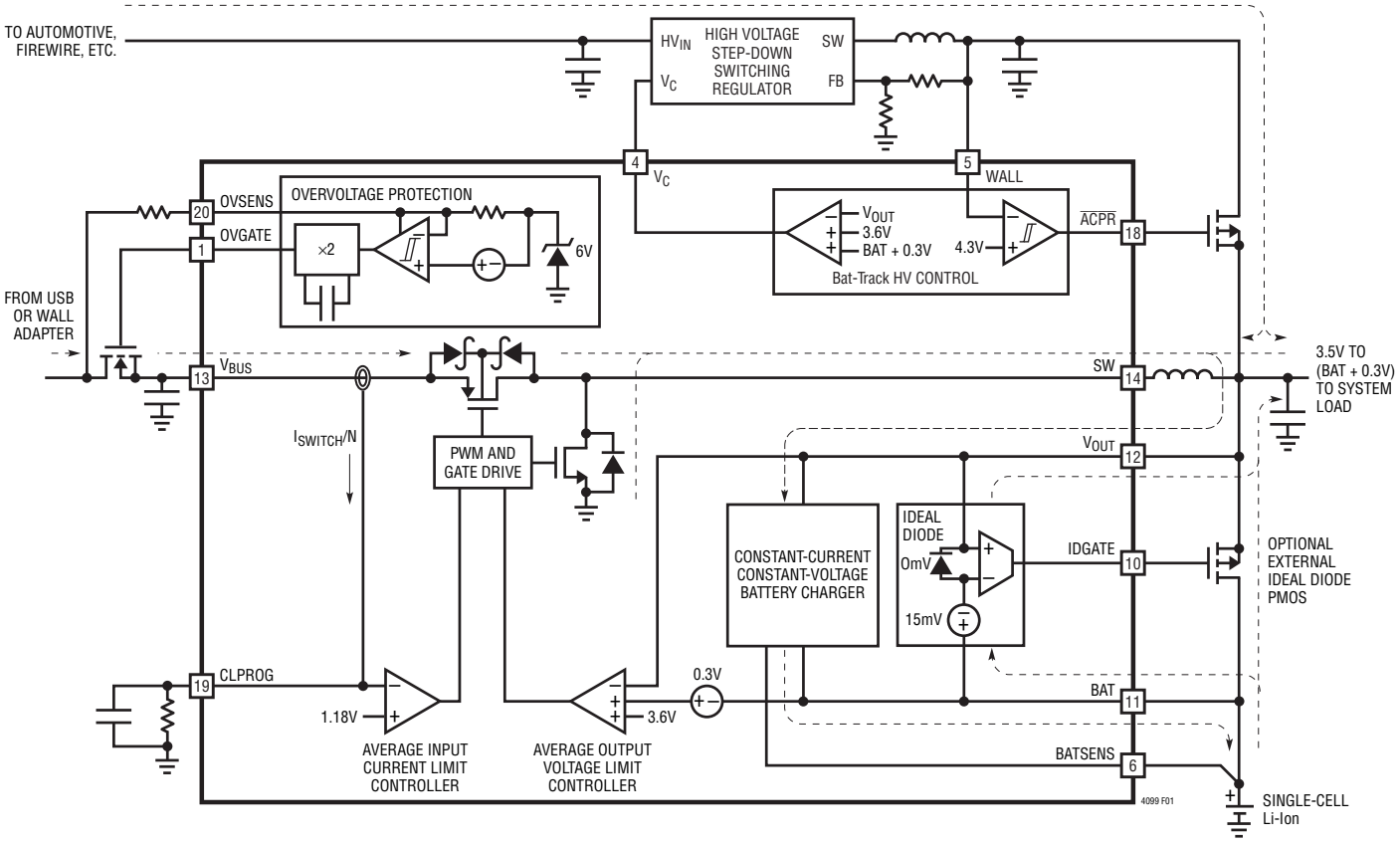


Figure 1. PowerPath Block Diagram

When the switching regulator is activated, the average input current will be limited by the CLPROG programming resistor according to the following expression:

$$I_{VBUS} = I_{VBUSQ} + \frac{V_{CLPROG}}{R_{CLPROG}} \bullet \left(h_{CLPROG} + 1\right)$$

where I_{VBUSQ} is the quiescent current of the LTC4099, V_{CLPROG} is the CLPROG servo voltage in current limit, R_{CLPROG} is the value of the programming resistor and h_{CLPROG} is the ratio of the measured current at V_{BUS} to the sample current delivered to CLPROG. Refer to the Electrical Characteristics table for values of h_{CLPROG}, V_{CLPROG} and I_{VBUSQ}. Given worst-case circuit tolerances, the USB specification for the average input current in 100mA or 500mA mode will not be violated, provided that R_{CLPROG} is 3.01k or greater. See Table 2 for other available settings of input current limit.

While not in current limit, the switching regulator's Bat-Track feature will set V_{OUT} to approximately 300mV above the voltage at BAT. However, if the voltage at BAT is below 3.3V, and the load requirement does not cause the switching regulator to exceed its current limit, V_{OUT} will regulate at a fixed 3.6V, as shown in Figure 2. This instant-on feature will allow a portable product to run immediately when power is applied without waiting for

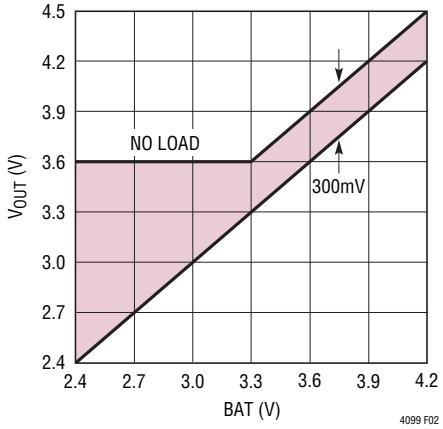


Figure 2. V_{OUT} vs BAT

OPERATION

the battery to charge. If the input-referred load current exceeds the input current limit at V_{BUS}, V_{OUT} will range between the no-load voltage and slightly below the battery voltage as indicated by the shaded region of Figure 2. If there is no battery present when this happens, V_{OUT} may collapse to ground. In such cases the input-referred load current should be maintained below the programmed input current level in order to keep the V_{OUT} and BAT voltages within specified limits.

For very low battery voltages, the battery charger acts like a load and, due to the input current limit circuit, its current will tend to pull V_{OUT} below the 3.6V instant-on voltage. To prevent V_{OUT} from falling below this level, an undervoltage circuit automatically detects that V_{OUT} is falling and reduces the battery charge current as needed. This reduction ensures that load current and voltage are always prioritized while allowing as much battery charge current as possible. See Overprogramming the Battery Charger in the Applications Information section.

The voltage regulation loop compensation is controlled by the capacitance on V_{OUT}. An MLCC capacitor of 10µF is required for loop stability. Additional capacitance beyond this value will improve transient response.

An internal undervoltage lockout circuit monitors V_{BUS} and keeps the switching regulator off until V_{BUS} rises above the rising V_{UVLO} threshold (4.3V). If V_{BUS} falls below the falling V_{UVLO} threshold (4V), system power at V_{OUT} will be drawn from the battery via the ideal diodes. The voltage at V_{BUS} must also be higher than the voltage at BAT by V_{DUVLO}, or approximately 200mV, for the switching regulator to operate.

Bat-Track Auxiliary High Voltage Switching Regulator Control

As shown in the Block Diagram, the WALL, $\overline{ACPR}$ and V_C pins can be used in conjunction with an external high voltage Linear Technology step-down switching regulator, such as the LT3480 or LT3653, to minimize heat production when operating from higher voltage sources. Bat-Track control circuitry regulates the external switching regulator's output voltage to the larger of BAT + 300mV or 3.6V in much the same way as the internal switching regulator. This maximizes battery charger efficiency while still allowing instant-on operation when the battery is deeply discharged.

The feedback network of the high voltage regulator should be set to program an output voltage between 4.5V and 5.5V. When high voltage is applied to the external regulator, WALL will rise toward this programmed output voltage. When WALL exceeds approximately 4.3V, $\overline{ACPR}$ is brought low, and the Bat-Track control of the LTC4099 overdrives the local V_C control of the external high voltage step-down switching regulator. Once the Bat-Track control is enabled, the output voltage is independent of the switching regulator feedback network.

Bat-Track control provides a significant efficiency advantage over the use of a simple 5V switching regulator output to drive the battery charger. With a 5V output driving V_{OUT}, battery charger efficiency is approximately:

$$\eta_{TOTAL} = \eta_{BUCK} \bullet \frac{V_{BAT}}{5V}$$

where η_{BUCK} is the efficiency of the high voltage switching regulator and 5V is the output voltage of the switching regulator. With a typical switching regulator efficiency of 87% and a typical battery voltage of 3.8V, the total battery charger efficiency is approximately 66%. Assuming a 1A charge current, nearly 2W of power is dissipated just to charge the battery!

With Bat-Track, battery charger efficiency is approximately:

$$\eta_{TOTAL} = \eta_{BUCK} \bullet \frac{V_{BAT}}{V_{BAT} + 0.3V}$$

With the same assumptions as above, the total battery charger efficiency is approximately 81%. This example works out to less than 1W of power dissipation, or almost 60% less heat.

See the Typical Applications section for complete circuits using the LT3480 and LT3653 with Bat-Track control.

Ideal Diode from BAT to V_{OUT}

The LTC4099 has an internal ideal diode as well as a controller for an external ideal diode. Both the internal and the external ideal diodes are always on and will respond quickly whenever V_{OUT} drops below BAT.

OPERATION

If the load current increases beyond the power allowed from the switching regulator, additional power will be pulled from the battery via the ideal diodes. Furthermore, if power to V_{BUS} (USB or wall adapter) is removed, then all of the application power will be provided by the battery via the ideal diodes. The ideal diodes will be fast enough to keep V_{OUT} from drooping with only the storage capacitance required for the switching regulator. The internal ideal diode consists of a precision amplifier that activates a large on-chip MOSFET transistor whenever the voltage at V_{OUT} is approximately 15mV (V_{FWD}) below the voltage at BAT. Within the amplifier's linear range, the small-signal resistance of the ideal diode will be quite low, keeping the forward drop near 15mV. At higher current levels, the MOSFET will be in full conduction.

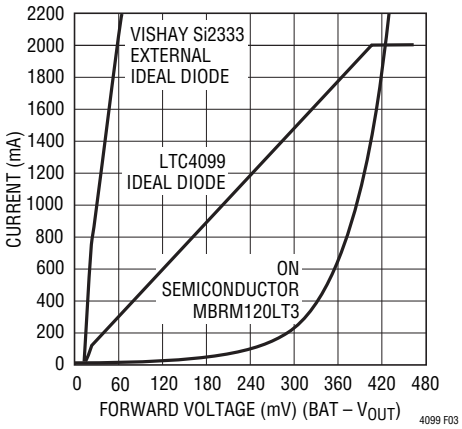


Figure 3. Ideal Diode V-I Characteristics

To supplement the internal ideal diode, an external P-channel MOSFET transistor may be added from BAT to V_{OUT}. The IDGATE pin of the LTC4099 drives the gate of the external P-channel MOSFET transistor for automatic ideal diode control. The source of the external P-channel MOSFET should be connected to V_{OUT} and the drain should be connected to BAT. Capable of driving a 1nF load, the IDGATE pin can control an external P-channel MOSFET transistor having an on-resistance of 30mΩ or lower.

Battery Charger

The LTC4099 includes a battery charger with low voltage precharge, constant-current/constant-voltage charging, C/x state-of-charge detection, automatic termination by safety timer, automatic recharge, bad cell detection and thermistor sensor input for out-of-temperature charge pausing.

Precharge

When a battery charge cycle begins, the battery charger first determines if the battery is deeply discharged. If the battery voltage is below V_{TRKL}, typically 2.85V, an automatic trickle charge feature sets the battery charge current to one-fifth of the default charge current. If the low voltage persists for more than one-half hour, the battery charger automatically terminates and indicates via the I^2C port that the battery was unresponsive.

Constant-Current

Once the battery voltage is above V_{TRKL}, the charger begins charging in full power constant-current mode. The current delivered to the battery will try to reach $V_{PROG}/R_{PROG} \bullet 1030$ where V_{PROG} can be set by the I^2C port and ranges from 500mV to 1.2V in 100mV steps. The default value of V_{PROG} is 500mV. Depending on available input power and external load conditions, the battery charger may or may not be able to charge at the full programmed rate. The external load will always be prioritized over the battery charge current. Likewise, the USB current limit programming will always be observed and only additional power will be available to charge the battery. When system loads are light, battery charge current will be maximized.

As mentioned above, the upper limit of charge current is programmed by the combination of a resistor from PROG to ground and the PROG servo voltage value set in the I^2C port. The charge current will be given by the following expression:

$$I_{CHG} = \frac{V_{PROG}}{R_{PROG}} \bullet 1030$$

Eight values of V_{PROG} may be selected by the $I_{CHARGE2}$, $I_{CHARGE1}$ and $I_{CHARGE0}$ bits in the I^2C port. See Table 3.

In either the constant-current or constant-voltage charging modes, the voltage at the PROG pin will be proportional to the actual charge current delivered to the battery. The charge current can be determined at any time by monitoring the PROG pin voltage and using the following relationship:

$$I_{BAT} = \frac{V_{PROG}}{R_{PROG}} \bullet 1030$$

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Recall, however, that in many cases the actual battery charge current, I_{BAT}, will be lower than the programmed current, I_{CHG}, due to limited input power available and prioritization of the system load drawn from V_{OUT}.

Constant-Voltage

Once the battery terminal voltage reaches the preset float voltage, the battery charger will hold the voltage steady and the charge current will decrease naturally toward zero. Two voltage settings, 4.100V and 4.200V, are available for final float voltage selection via the I^2C port. For applications that require as much run time as possible, the 4.200V setting can be selected. For applications that seek to extend battery life, the LTC4099's default setting of 4.100V should be used.

Full Capacity Charge Indication (C/x)

Since the PROG pin always represents the actual charge current flowing, even in the constant-voltage phase of charging, the PROG pin voltage represents the battery's state-of-charge during that phase. The LTC4099 has a full capacity charge indication comparator on the PROG pin which reports its results via the I^2C port. Selection levels for the C/x comparator of 50mV, 100mV, 200mV and 500mV are available by I^2C control. Recall that the PROG pin servo voltage can be programmed from 500mV to 1.2V. If the 1V servo setting represents the full charge rate of the battery (1C), then the 100mV C/x setting would be equivalent to C/10. Likewise the 200mV C/x setting would represent C/5 and the 500mV setting C/2.

Charge Termination

The battery charger has a built-in termination safety timer. When the voltage on the battery reaches the user-programmed float voltage of 4.100V or 4.200V, the safety timer is started. After the safety timer expires, charging of the battery will discontinue and no more current will be delivered. The safety timer's default ending time of four hours may be altered from one to eight hours in one-hour increments by accessing the I^2C port.

Automatic Recharge

After the battery charger terminates, it will remain off, drawing only microamperes of current from the battery. If the portable product remains in this state long enough, the battery will eventually self discharge. To ensure that the battery is always topped off, a new charge cycle will automatically begin when the battery voltage falls below V_{RECHRG} (typically 4.100V for the 4.200V float voltage setting and 4.000V for the 4.100V float voltage setting). In the event that the safety timer is running when the battery voltage falls below V_{RECHRG}, it will reset back to zero. To prevent brief excursions below V_{RECHRG} from resetting the safety timer, the battery voltage must be below V_{RECHRG} for more than 2.5ms. The charge cycle and safety timer will also restart if the V_{BUS} UVLO cycles LOW and then HIGH (e.g., V_{BUS} or WALL is removed and then replaced) or if the charger is momentarily disabled using the I^2C port.

The flow chart in Figure 4 represents the battery charger's algorithm.

Thermistor Measurement

The battery temperature is measured by placing a negative temperature coefficient (NTC) thermistor close to the battery pack. The thermistor circuitry is shown in the Block Diagram.

To use this feature, connect the thermistor between the NTC pin and ground and a bias resistor from NTCBIAS to NTC. The bias resistor should be a 1% resistor with a value equal to the value of the chosen thermistor at 25°C (R25).

The LTC4099 will pause charging when the resistance of the thermistor drops to 0.484 times the value of R25 or 4.84k for a 10k thermistor. For a Vishay curve 2 thermistor, this corresponds to approximately 45°C. If the battery charger is in constant-voltage (float) mode, the safety timer also pauses until the thermistor indicates a return to valid temperature. The LTC4099 is also designed to pause charging when the value of the thermistor increases to 2.816 times the value of R25. For a Vishay curve 2 10k thermistor, this resistance, 28.16k, corresponds to approximately 0°C. The hot and cold comparators each have approximately 4°C of hysteresis to prevent oscillation about the trip point.

If the curve 2 thermistor's temperature rises above 60°C, its value will drop to 0.2954 times R25. When this happens, the LTC4099 detects this critically high temperature and indicates it via the I^2C port (see Table 7). If this condition

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occurs, it may be desirable to have application software enforce an emergency reduction of power in the portable product. It is possible to enable the battery conditioner circuit at this temperature to reduce stress caused by simultaneous high temperature and high voltage via the I^2C port. See the Overtemperature Battery Conditioner section.

The thermistor detection circuit samples the thermistor's value continuously whenever charging is enabled and periodically when it is not. When the charger is not enabled, the thermistor is sampled for 150µs approximately every 150ms. The thermistor data available to the I^2C port is updated at the end of each sample period.

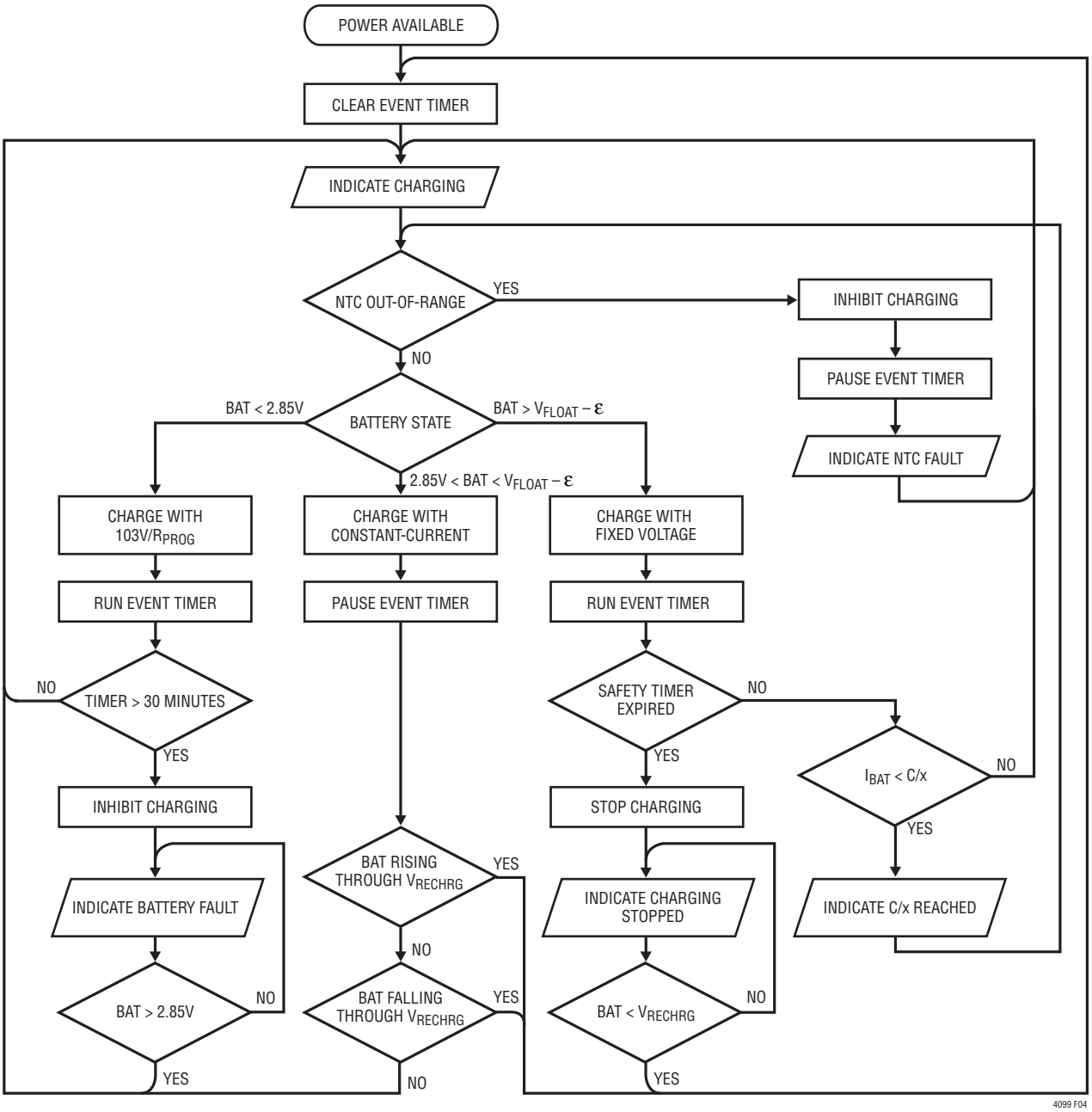

Figure 4. Battery Charger Flow Chart

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Overtemperature Battery Conditioner

Since Li-Ion batteries deteriorate with full voltage and high temperature, the LTC4099 contains an automatic battery conditioner circuit that reduces the battery voltage if both high temperature and high voltage are present simultaneously.

Recall that battery charging is inhibited if the thermistor temperature reaches 45°C. If the thermistor temperature climbs above 60°C, and the battery conditioner circuit is enabled, an internal load of approximately 180mA is applied to BAT. Once the battery voltage drops to 3.9V, or the thermistor reading drops below 58°C, the internal load is disabled. Battery charging resumes once the thermistor temperature drops below 42°C.

When activated via the I^2C port, the battery conditioner operates whether or not external power is available, charging has terminated or charging has been disabled by I^2C control.

Note that this circuit can dissipate significant power inside the LTC4099. To prevent an excessive temperature rise of the LTC4099, the LTC4099 reduces discharge current as needed to prevent a junction temperature rise above 120°C.

Thermal Regulation

To prevent thermal damage to the LTC4099 or surrounding components during normal charging, an internal thermal feedback loop will automatically decrease the programmed charge current if the die temperature rises to 105°C. This thermal regulation technique protects the LTC4099 from excessive temperature due to high power operation or high ambient thermal conditions, and allows the user to push the limits of the power handling capability with a given circuit board design. The benefit of the LTC4099 thermal regulation loop is that charge current can be set according to actual, rather than worst-case, conditions for a given application with the assurance that the charger will automatically reduce the current in worst-case conditions.

The thermal regulation set-point can be adjusted down to 85°C from the default 105°C setting using the I^2C port, as explained in the Input Data section.

Overvoltage Protection

The LTC4099 can protect itself from the inadvertent application of excessive voltage to V_{BUS} or WALL with just two external components: an N-channel MOSFET and a 6.2k resistor. The maximum safe overvoltage magnitude will be determined by the choice of the external FET and its associated drain breakdown voltage.

The overvoltage protection circuit consists of two pins. The first, OVSENS, is used to measure the externally applied voltage through an external resistor. The second, OVGATE, is an output used to drive the gate pin of the external FET. When OVSENS is below 6V, an internal charge pump will drive OVGATE to approximately 1.88 • OVSENS. This will enhance the N-channel FET and provide a low impedance connection to V_{BUS} or WALL which will, in turn, power the LTC4099. If OVSENS should rise above 6V due to a fault or use of an incorrect wall adapter, OVGATE will be pulled to GND, disabling the external FET and, therefore, protecting the LTC4099. When the voltage drops below 6V again, the external FET will be re-enabled.

See the Applications Information section for examples of multiple input protections, reverse input protection and recommended components.

Suspend LDO

The LTC4099 provides a small amount of power to V_{OUT} in suspend mode by including an LDO from V_{BUS} to V_{OUT}. This LDO will prevent the battery from running down when the portable product has access to a suspended USB port. Regulating at 4.6V, this LDO only becomes active when the internal switching converter is disabled. To remain compliant with the USB specification, the input to the LDO is current-limited so that it will not exceed the low power or high power suspend specification. If the load on V_{OUT} exceeds the suspend current limit, the additional current will come from the battery via the ideal diodes. The suspend LDO sends a scaled copy of the V_{BUS} current to the CLPROG pin, which will servo to a maximum voltage of approximately 100mV. Thus, the high power and low power suspend settings are related to the levels programmed by the same CLPROG resistor for the 100mA, 500mA and other switching power path settings. Command bits, I_{LIM2}

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through I_{LIM0} in the I^2C port determine whether the suspend LDO will limit input current to the low power setting of 500µA or the high power setting of 2.5mA.

Interrupt Generation

The $\overline{IRQ}$ pin on the LTC4099 is an open-drain output that can be used to generate an interrupt based on one or more of a multitude of maskable PowerPath/battery charger change events. The interrupt mask register column in Table 1 indicates the categories of events that can generate an interrupt. If a 1 is written to a given location in the mask register, then any change in the status data of that category will cause an interrupt to occur. For example, if a 1 is written to bit 6 of the mask register, then an interrupt will be generated when the WALL UVLO detects that either power has become available at WALL, or that power was available and is no longer available from WALL. If a 1 is written to bit 2 of the mask register, then an interrupt will be triggered by any change in the status bits of the battery charger, as given by Table 8. Likewise, a 1 at bit 3 will allow an interrupt due to any change in the thermistor status bits of Table 7.

The $\overline{IRQ}$ pin is cleared when the bus master acknowledges receipt of status data from a read operation. If the master does not acknowledge the status byte, the interrupt will not be cleared and the $\overline{IRQ}$ pin will not be released.

Upon generation of an interrupt, the current state of the LTC4099 is recorded in the I^2C port for retrieval (see Output Data).

I^2C Interface

The LTC4099 may communicate with a bus master using the standard I^2C 2-wire interface. The Timing Diagram shows the relationship of the signals on the bus. The two bus lines, SDA and SCL, must be HIGH when the bus is not in use. External pull-up resistors or current sources, such as the LTC1694 SMBus accelerator, are required on these lines. The LTC4099 is both a slave receiver and slave transmitter. The I^2C control signals, SDA and SCL, are scaled internally to the DV_{CC} supply. DV_{CC} should be connected to the same power supply as the bus pull-up resistors.

The I^2C port has an undervoltage lockout on the DV_{CC} pin. When DV_{CC} is below approximately 1V, the I^2C serial port is cleared, the LTC4099 is set to its default configuration of all zeros and interrupts will be locked out.

Bus Speed

The I^2C port is designed to be operated at speeds of up to 400kHz. It has built-in timing delays to ensure correct operation when addressed from an I^2C compliant master device. It also contains input filters designed to suppress glitches should the bus become corrupted.

START and STOP Conditions

A bus master signals the beginning of communications by transmitting a START condition. A START condition is generated by transitioning SDA from HIGH to LOW while SCL is HIGH. The master may transmit either the slave write or the slave read address. Once data is written to the LTC4099, the master may transmit a STOP condition which commands the LTC4099 to act upon its new command set. A STOP condition is sent by the master by transitioning SDA from LOW to HIGH while SCL is HIGH.

Byte Format

Each byte sent to, or received from, the LTC4099 must be eight bits long followed by an extra clock cycle for the acknowledge bit. The data should be sent to the LTC4099 most significant bit (MSB) first.

Acknowledge

The acknowledge signal is used for handshaking between the master and the slave. When the LTC4099 is written to (write address), it acknowledges its write address as well as the subsequent two data bytes. When it is read from (read address), the LTC4099 acknowledges its read address only. The bus master should acknowledge receipt of information from the LTC4099.

An acknowledge (active LOW) generated by the LTC4099 lets the master know that the latest byte of information was received. The acknowledge related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock cycle. The LTC4099 pulls

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down the SDA line during the write acknowledge clock pulse so that it is a stable LOW during the HIGH period of this clock pulse.

When the LTC4099 is read from, it releases the SDA line so that the master may acknowledge receipt of the data. Since the LTC4099 only transmits one byte of data, a master not acknowledging the data sent by the LTC4099 has no specific consequence on the operation of the I^2C port. However, without a read acknowledge from the master, a pending interrupt from the LTC4099 will not be cleared and the $\overline{IRQ}$ pin will not be released.

Slave Address

The LTC4099 responds to a 7-bit address which has been factory programmed to 0b0001001[R/$\overline{W}$]. The LSB of the address byte, known as the read/write bit, should be 0 when writing data to the LTC4099, and 1 when reading data from it. Considering the address an 8-bit word, then the write address is 0x12, and the read address is 0x13. The LTC4099 will acknowledge both its read and write addresses.

Sub-Addressed Writing

The LTC4099 has three command registers for control input. They are accessed by the I^2C port via a sub-addressed writing system.

Each write cycle of the LTC4099 consists of exactly three bytes. The first byte is always the LTC4099's write address. The second byte represents the LTC4099's sub address. The sub address is a pointer which directs the subsequent data byte within the LTC4099. The third bye consists of the data to be written to the location pointed to by the sub address. The LTC4099 contains control registers at only three sub address locations: 0x00, 0x01 and 0x02. Only the two LSBs of the sub address byte are decoded, the remaining bits are don't-cares. Therefore, a write to sub address 0x06 for example, is effectively a write to sub address 0x02.

Bus Write Operation

The master initiates communication with the LTC4099 with a START condition and the LTC4099's write address. If the address matches that of the LTC4099, the LTC4099 returns an acknowledge. The master should then deliver the sub address. Again, the LTC4099 acknowledges and the cycle is repeated for the data byte. The data byte is transferred to an internal holding latch upon the return of its acknowledge by the LTC4099. This procedure must be repeated for each sub address that requires new data. After one or more cycles of [ADDRESS][SUB-ADDRESS][DATA], the master may terminate the communication with a STOP condition. Alternatively, a repeat START condition can be initiated by the master and another chip on the I^2C bus can be addressed. This cycle can continue indefinitely, and the LTC4099 will remember the last input of valid data that it received. Once all chips on the bus have been addressed and sent valid data, a global STOP can be sent and the LTC4099 will update its command latches with the data that it had received.

Bus Read Operation

The bus master reads the status of the LTC4099 with a START condition followed by the LTC4099 read address. If the read address matches that of the LTC4099, the LTC4099 returns an acknowledge. Following the acknowledgement of its read address, the LTC4099 returns one bit of status information for each of the next eight clock cycles. A STOP command is not required for the bus read operation.

Input Data

Table 1 illustrates the three data bytes that may be written to the LTC4099. The first byte at sub address 0x00 controls the three input current limit bits I_{LIM2}-I_{LIM0}, the three battery charge current control bits $I_{CHARGE2}$-$I_{CHARGE0}$ and the two C/x state-of-charge indication control bits COVERX1 and COVERX0.

The input current limit settings are decoded according to Table 2. This table indicates the maximum current that will be drawn from the V_{BUS} pin in the event that the load at V_{OUT} (battery charger plus system load) exceeds the power available. Any additional power will be drawn from the battery. The default state for the input current limit setting is 000, representing the low power 100mA USB setting.

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The battery charger current settings are decoded in Table 3. The battery charger current settings are adjusted by selecting one of the eight servo voltages for the PROG pin. Recall that the programmed charge current is given by the expression:

$$I_{CHG} = \frac{V_{PROG}}{R_{PROG}} \bullet 1030$$

The default state for the battery charger current settings is 000, giving the lowest available servo voltage of 500mV.

The COVERX1 and COVERX0 bits are decoded in Table 4. The C/x setting controls the PROG pin level that the LTC4099's C/x comparator uses to report full capacity charge. For example, if the 100mV setting is chosen, then the LTC4099 reports that its PROG pin voltage has fallen below 100mV. For the 50mV setting, LTC4099 reports that its PROG pin voltage has fallen below 50mV. The C/x settings are adjusted by comparing the PROG pin voltage with the values shows in Table 4. The default value for the C/x setting is 00, giving 100mV detection.

The second byte of data at sub address 0x01 controls the three battery charger safety timer bits, TIMER2-TIMER0, the DISABLE_CHARGER bit, the ENABLE_BATTERY_CONDITIONER bit, the V_{FLOAT} = 4.2V control bit and the T_{REG} = 85°C control bit.

The TIMER2–TIMER0 bits control the duration of the battery charger safety timer. The safety timer starts once the LTC4099 reaches the 4.100V or the 4.200V float voltage. As long as input power is available, charging will continue in float voltage mode until the safety timer expires.

Table 1. LTC4099 Input Data Bytes

	SUB ADDRESS 0	SUB ADDRESS 1	SUB ADDRESS 2
	COMMAND REGISTER 0	COMMAND REGISTER 1	$\overline{IRQ}$ MASK REGISTER
Bit 7	I_{LIM2}	TIMER2	USBGOOD
Bit 6	I_{LIM1}	TIMER1	WALLGOOD
Bit 5	I_{LIM0}	TIMER0	BADCELL
Bit 4	$I_{CHARGE2}$	DISABLE_CHARGER	THERMAL_ REG
Bit 3	$I_{CHARGE1}$	ENABLE_ BATTERY_ CONDITIONER	THERMISTOR_ STATUS
Bit 2	$I_{CHARGE0}$	V_{FLOAT} = 4.2V	CHARGER_STATUS
Bit 1	COVERX1	T_{REG} = 85°C	Not Used
Bit 0	COVERX0	Not Used	Not Used

Table 2. I_{LIM2} – I_{LIM0} Decode

USB INPUT CURRENT LIMIT SETTINGS			
I_{LIM2}	I_{LIM1}	I_{LIM0}	I_{USB}
0	0	0	100mA*
0	0	1	500mA
0	1	0	620mA
0	1	1	790mA
1	0	0	1000mA
1	0	1	1200mA
1	1	0	Suspend Low (500µA)
1	1	1	Suspend High (2.5mA)

*Default Setting

Table 3. $I_{CHARGE2}$ – $I_{CHARGE0}$ Decode

BATTERY CHARGER CURRENT LIMIT SETTINGS				
$I_{CHARGE2}$	$I_{CHARGE1}$	$I_{CHARGE0}$	V_{PROG}	CHARGE CURRENT R_{PROG} = 1.02k
0	0	0	500mV*	500mA
0	0	1	600mV	600mA
0	1	0	700mV	700mA
0	1	1	800mV	800mA
1	0	0	900mV	900mA
1	0	1	1000mV	1000mA
1	1	0	1100mV	1100mA
1	1	1	1200mV	1200mA

*Default Setting

Table 4. C/x Decode

C/x INDICATION SETTINGS			
COVERX1	COVERX0	V_{PROG}	FULL CAPACITY CHARGE INDICATION R_{PROG} = 1.02k
0	0	100mV*	100mA*
0	1	50mV	50mA
1	0	200mV	200mA
1	1	500mV	500mA

*Default Setting

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Table 5 lists the possible safety timer settings from 1 to 8 hours, and how to decode them. The default state for the LTC4099 safety timer is 4 hours.

Table 5. Safety Timer Decode

SAFETY TIMER SETTINGS			
TIMER2	TIMER1	TIMER0	TIMEOUT
0	0	0	4 Hours*
0	0	1	5 Hours
0	1	0	6 Hours
0	1	1	7 Hours
1	0	0	8 Hours
1	0	1	1 Hour
1	1	0	2 Hours
1	1	1	3 Hours

*Default Setting

The DISABLE_CHARGER bit can be used to prevent battery charging if needed. This bit should be used with caution as it can prevent the battery charger from bringing up the battery voltage. Without the ability to address the I^2C port, only a low voltage on DV_{CC} will clear the I^2C port to its default state and re-enable charging.

The ENABLE_BATTERY_CONDITIONER bit enables the automatic battery load circuit in the event of simultaneously high battery voltage and temperature. See the Overtemperature Battery Conditioner section.

The V_{FLOAT} = 4.2V bit controls the final float voltage of the LTC4099's battery charger. A 1 in this bit position changes the charger from the default float voltage value of 4.100V to the higher 4.200V level.

The T_{REG} = 85°C control bit changes the LTC4099's battery charger junction thermal regulation temperature from its default value of 105°C to a lower setting of 85°C. This may be used to reduce heat in highly thermally compromised systems. In general, the high efficiency charging system of the LTC4099 will keep the junction temperature low enough to avoid junction thermal regulation.

The third and final byte of input data at sub address 0x02 is the mask register. The mask register determines which status change events or categories will be allowed to generate an interrupt. A 1 written to a given position in the mask register allows status change in that category to generate an interrupt. A zero in a given position in the mask register prohibits the generation of an interrupt. The start-up state of the LTC4099 is all zeros for this register indicating that no interrupts will be generated without explicit request via the I^2C port. See the Interrupt Generation section.

Output Data

One status byte may be read from the LTC4099. Table 6 represents the status byte information. A 1 read back in any of the bit positions indicates that the condition is true. For example, 1s read back from bits 7 and 2 indicate that power is available at V_{BUS}, and that the battery charger's thermistor has halted charging due to an undertemperature condition at the battery.

Table 6. LTC4099 Status Data Bytes

READ BYTE	STATUS REGISTER	
Bit 7 (MSB)	USBGOOD	
Bit 6	WALLGOOD	
Bit 5	BADCELL	
Bit 4	THERMAL REG	
Bit 3	NTC1	See Table 7
Bit 2	NTC0	
Bit 1	CHRGR1	See Table 8
Bit 0 (LSB)	CHRGR0	

Bit 7 in the status byte indicates the presence of power at V_{BUS}. Criteria for determining this status bit is derived from the undervoltage lockout circuit on V_{BUS} and is given by the electrical parameters V_{UVLO} and V_{DUVLO}.

Bit 6 indicates the presence of voltage available at the WALL pin and is derived from the WALL undervoltage lockout circuit. Like the V_{BUS} pin, this pin has both an absolute voltage detection level given by the electrical parameter V_{WALL}, as well as a level relative to BAT given by ΔV_{WALL}. Both of the conditions must be met for bit 6 to indicate the presence of power at WALL.

Bit 5 indicates that the battery has been below the precharge threshold level of approximately 2.85V for more than one-half hour while the charger was attempting to charge. When this occurs, it is usually the result of a defective cell. However, in some cases a bad cell indication may be caused by system load prioritization over battery charging. System software can test for this by forcing a reduction of system load and restarting the battery charger

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via I²C (a disable followed by an enable). If the bad cell indication returns, then the cell is definitively bad.

Bit 4 indicates that the battery charger is in thermal regulation due to excessive LTC4099 junction temperature. Recall that there are two I²C programmable junction temperature settings available at which to regulate, 85°C and 105°C. Bit 4 indicates thermal regulation at whichever setting is chosen.

Bits 3 and 2 indicate the status of the thermistor measurement circuit and are decoded in Table 7. The BATTERY TOO COLD and BATTERY TOO HOT states indicate that the thermistor temperature is out of range (either below 0°C or above 45°C for a curve 2 thermistor) and that charging has paused until a return to valid temperature. The BATTERY OVERTEMPERATURE state indicates that the battery's thermistor has reached a critical temperature (above 60°C for a curve 2 thermistor) and that long term battery capacity may be seriously compromised if the condition persists.

Table 7. NTC1, NTC0 Decode

THERMISTOR STATUS BIT DECODE		
NTC1	**NTC0**	**THERMISTOR STATUS**
0	0	NO NTC FAULT
0	1	BATTERY TOO COLD
1	0	BATTERY TOO HOT
1	1	BATTERY OVERTEMPERATURE

Table 8. CHRGR1, CHRGR0 Decode

BATTERY CHARGER STATUS BIT DECODE		
CHRGR1	**CHRGR0**	**CHARGER STATUS**
0	0	CHARGER OFF
0	1	CONSTANT-CURRENT
1	0	CONSTANT V, $I_{BAT} > C/x$
1	1	CONSTANT V, $I_{BAT} < C/x$

Bits 1 and 0 indicate the status of the battery charger, and are decoded into one of four possible battery charger states in Table 8. The constant-current state indicates that the battery charger is attempting to charge with all available current up to the constant-current level programmed, and that the battery has not yet reached the float voltage. The CONSTANT V, $I_{BAT} > C/x$ bit indicates that the battery charger has entered the float voltage phase of charging (BAT at 4.1V or 4.2V), but that the charge current is still above the C/x detection level programmed. The CONSTANT V, $I_{BAT} < C/x$ bit indicates that the battery charge current has dropped below the C/x detection level programmed, and that charging is virtually complete. Note that if the current limited USB compliant switching regulator is in input current regulation, then the actual battery charge current may be less than C/x due to insufficient available power. If the LTC4099 is in input current limit, the charge status bits will lock out (disallow) the state 1-1, indicating that charging is complete. This feature prevents false full capacity charge indications due to insufficient power to the battery charger.

The status read from the LTC4099 is captured in one of two ways. If an interrupt is currently pending, then the available data represents the state of the LTC4099 at the time the interrupt was generated. If no interrupt is pending, then the data is captured when the LTC4099 acknowledges its read address. In the case of a pending interrupt, fresh data can be assured by taking two consecutive readings of the status information and discarding the first set.

Shutdown Mode

The USB switching regulator is enabled whenever V_{BUS} is above V_{UVLO}, greater than V_{DUVLO} above BAT and the LTC4099 is not in one of the two USB suspend modes (500µA or 2.5mA). When power is available from both the USB (V_{BUS}) and WALL inputs, the auxiliary (WALL) input is prioritized and the USB switching regulator is disabled.

The battery charger will always start a charge cycle when power is detected at V_{BUS} or WALL. It can only be shut down via a command from the I²C port or by normal termination after a charge cycle.

The ideal diode is enabled at all times and cannot be disabled.

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CLPROG Resistor and Capacitor

As described in the Bat-Track Input Current Limited Step-Down Switching Regulator section, the resistor on the CLPROG pin determines the average input current limit in each of the current limit modes. The input current will be comprised of two components, the current that is used to deliver power to V_{OUT}, and the quiescent current of the switching regulator. To ensure that the USB specification is strictly met, both components of input current should be considered. The Electrical Characteristics table gives the typical values for quiescent currents in all settings, as well as current limit programming accuracy. To get as close to the 500mA or 100mA specifications as possible, a precision resistor should be used.

An averaging capacitor is required in parallel with the resistor so that the switching regulator can determine the average input current. This capacitor also provides the dominant pole for the feedback loop when current limit is reached. To ensure stability, the capacitor on CLPROG should be 0.1µF or larger.

Choosing the Inductor

Because the input voltage range and output voltage range of the power path switching regulator are both fairly narrow, the LTC4099 was designed for a specific inductance value of 3.3µH. Some inductors which may be suitable for this application are listed in Table 9.

Table 9. Recommended Inductors for the LTC4099

INDUCTOR TYPE	L (µH)	MAX I_{DC} (A)	MAX DCR (Ω)	SIZE IN mm (L × W × H)	MANUFACTURER
LPS4018	3.3	2.2	0.08	3.9 × 3.9 × 1.7	Coilcraft www.coilcraft.com
D53LC DB318C	3.3 3.3	2.26 1.55	0.034 0.070	5 × 5 × 3 3.8 × 3.8 × 1.8	Toko www.toko.com
WE-TPC Type M1	3.3	1.95	0.065	4.8 × 4.8 × 1.8	Würth Elektronik www.we-online.com
CDRH6D12 CDRH6D38	3.3 3.3	2.2 3.5	0.063 0.020	6.7 × 6.7 × 1.5 7 × 7 × 4	Sumida www.sumida.com

V_{BUS} and V_{OUT} Bypass Capacitors

The style and value of the capacitors used with the LTC4099 determine several important parameters such as regulator control loop stability and input voltage ripple. Because the LTC4099 uses a step-down switching power supply from V_{BUS} to V_{OUT}, its input current waveform contains high frequency components. It is strongly recommended that a low equivalent series resistance (ESR) multilayer ceramic capacitor be used to bypass V_{BUS}. Tantalum and aluminum capacitors are not recommended because of their high ESR. The value of the capacitor on V_{BUS} directly controls the amount of input ripple for a given load current. Increasing the size of this capacitor will reduce the input ripple. The USB specification allows a maximum of 10µF to be connected directly across the USB power bus. If the overvoltage protection circuit is used to protect V_{BUS}, then its soft-starting nature can be exploited and a larger V_{BUS} capacitor can be used if desired.

To prevent large V_{OUT} voltage steps during transient load conditions, it is also recommended that a ceramic capacitor be used to bypass V_{OUT}. The output capacitor is used in the compensation of the switching regulator. At least 10µF with low ESR are required on V_{OUT}. Additional capacitance will improve load transient performance and stability.

Multilayer ceramic chip capacitors typically have exceptional ESR performance. MLCCs combined with a tight board layout and an unbroken ground plane will yield very good performance and low EMI emissions.

There are several types of ceramic capacitors available, each having considerably different characteristics. For example, X7R ceramic capacitors have the best voltage and temperature stability. X5R ceramic capacitors have apparently higher packing density but poorer performance over their rated voltage and temperature ranges. Y5V ceramic capacitors have the highest packing density, but must be used with caution because of their extreme

APPLICATIONS INFORMATION

nonlinear characteristic of capacitance versus voltage. The actual in-circuit capacitance of a ceramic capacitor should be measured with a small AC signal and DC bias, as is expected in-circuit. Many vendors specify the capacitance versus voltage with a $1V_{RMS}$ AC test signal and, as a result, overstate the capacitance that the capacitor will present in the application. Using similar operating conditions as the application, the user must measure or request from the vendor the actual capacitance to determine if the selected capacitor meets the minimum capacitance that the application requires.

Overprogramming the Battery Charger

The USB high power specification allows for up to 2.5W to be drawn from the USB port. The LTC4099's switching regulator regulates the voltage at V_{OUT} to a level just above the voltage at BAT while limiting power to less than the amount programmed at CLPROG. The charger should be programmed, with the PROG pin, to deliver the maximum safe charging current without regard to the USB specifications. If there is insufficient current available to charge the battery at the programmed rate, the charger will reduce charge current until the system load on V_{OUT} is satisfied and the V_{BUS} current limit is satisfied. Programming the charger for more current than is available will not cause the average input current limit to be violated. It will merely allow the battery charger to make use of all available power to charge the battery as quickly as possible, and with minimal power dissipation within the charger.

Overvoltage Protection

It is possible to protect both V_{BUS} and WALL from overvoltage damage with several additional components as shown in Figure 5. Schottky diodes D1 and D2 pass the larger of V1 and V2 to R1 and OVSENS. If either V1 or V2 exceeds 6V plus the Schottky forward voltage, OVGATE will be pulled to GND and both the WALL and USB inputs will be protected. Each input is protected up to the drain-source breakdown, BV_{DSS}, of M1 and M2.

In an overvoltage condition, the OVSENS pin will be clamped at 6V. The external 6.2k resistor must be sized appropriately to dissipate the resultant power. For example, a 1/8W 6.2k resistor can have at most $\sqrt{1/8W \times 6.2k}$ = 28V applied across its terminals. With the 6V at OVSENS, the maximum overvoltage magnitude that this resistor can withstand is 34V. A 1/4W 6.2k resistor raises this value to 45V. OVSENS's absolute maximum current rating of 10mA imposes an upper limit of 68V protection.

Table 10. Recommended NMOS FETs for the Overvoltage Protection Circuit

NMOS FET	BV_{DSS}	R_{ON}	PACKAGE
FDN3725	30V	50mΩ	SOT-23
Si2302ADS	20V	70mΩ	SOT-23
NTLJS4114	30V	40mΩ	2mm × 2mm DFN
IRLML2502	20V	35mΩ	SOT-23

The charge pump output on OVGATE has limited output drive capability. Care must be taken to avoid leakage on this pin as it may adversely affect operation.

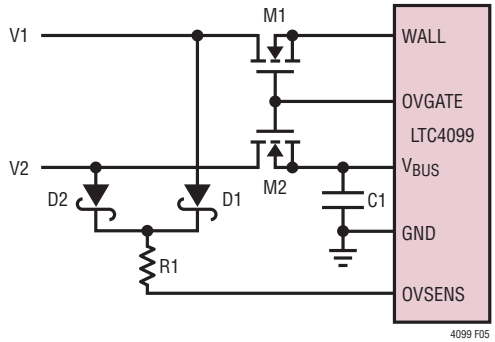


Figure 5. Dual Overvoltage Protection

APPLICATIONS INFORMATION

Reverse-Voltage Protection

The LTC4099 can also be easily protected against the application of reverse voltage, as shown in Figure 6. D1 and R1 are necessary to limit the maximum V_{GS} seen by MP1 during positive overvoltage events. D1's breakdown voltage must be safely below MP1's BV_{GS}. The circuit shown in Figure 6 offers forward voltage protection up to MN1's BV_{DSS} and reverse-voltage protection up to MP1's BV_{DSS}.

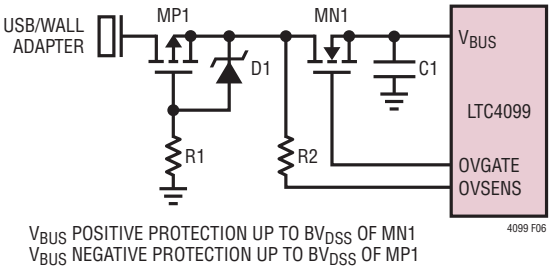


Figure 6. Dual-Polarity Voltage Protection

Alternate NTC Thermistors and Biasing

The LTC4099 provides temperature-qualified charging if a grounded thermistor and a bias resistor are connected to NTC. By using a bias resistor whose value is equal to the room temperature resistance of the thermistor (R25), the upper and lower temperatures are preprogrammed to approximately 45°C and 0°C, respectively, when using a Vishay curve 2 thermistor.

The upper and lower temperature thresholds can be adjusted by either a modification of the bias resistor value or by adding a second adjustment resistor to the circuit. If only the bias resistor is adjusted, then either the upper or the lower threshold can be modified, but not both. The other trip point will be determined by the characteristics of the thermistor. Using the bias resistor, in addition to an adjustment resistor, both the upper and the lower temperature trip points can be independently programmed with the constraint that the difference between the upper and lower temperature thresholds must increase. Examples of each technique follow.

NTC thermistors have temperature characteristics which are indicated on resistance-temperature conversion tables. The Vishay-Dale thermistor NTHS0603N02N1002-FF, used in the following examples, has a nominal value of 10k and follows the Vishay curve 2 resistance-temperature characteristic.

In the explanation below, the following notation is used.

R25 = Value of the thermistor at 25°C

R_{COLD} = Value of thermistor at the cold trip point

R_{HOT} = Value of the thermistor at the hot trip point

α_{COLD} = Ratio of R_{COLD} to R25

α_{HOT} = Ratio of R_{HOT} to R25

R_{NOM} = Primary thermistor bias resistor (see Figure 7)

R1 = Optional temperature range adjustment resistor (see Figure 8)

The trip points for the LTC4099's temperature qualification are internally programmed at 0.326 • NTCBIAS for the hot threshold and 0.738 • NTCBIAS for the cold threshold.

Therefore, the hot trip point is set when:

$$\frac{R_{HOT}}{R_{NOM} + R_{HOT}} \bullet NTCBIAS = 0.326 \bullet NTCBIAS$$

and the cold trip point is set when:

$$\frac{R_{COLD}}{R_{NOM} + R_{COLD}} \bullet NTCBIAS = 0.738 \bullet NTCBIAS$$

Solving these equations for R_{COLD} and R_{HOT} results in the following:

$R_{HOT} = 0.4839 \bullet R_{NOM}$

and

$R_{COLD} = 2.816 \bullet R_{NOM}$

By setting R_{NOM} equal to R25, the above equations result in $\alpha_{HOT} = 0.4839$ and $\alpha_{COLD} = 2.816$. Referencing these ratios to the Vishay resistance-temperature curve 2 chart gives a hot trip point of about 45°C and a cold trip point of about 0°C. The difference between the hot and cold trip points is approximately 45°C.

APPLICATIONS INFORMATION

By using a bias resistor, R_{NOM}, different in value from R25, the hot and cold trip points can be moved in either direction. The temperature span will change somewhat due to the nonlinear behavior of the thermistor. The following equations can be used to easily calculate a new value for the bias resistor:

$$R_{NOM} = \frac{\alpha_{HOT}}{0.4839} \bullet R25$$

$$R_{NOM} = \frac{\alpha_{COLD}}{2.816} \bullet R25$$

where α_{HOT} and α_{COLD} are the resistance ratios at the *desired* hot and cold trip points. Note that these equations are linked. Therefore, only one of the two trip points can be chosen; the other is determined by the default ratios designed in the LTC4099. Consider an example where a 50°C hot trip point is desired.

From the Vishay curve 2 R-T characteristics, α_{HOT} is 0.4086 at 50°C. Using the prior equation, R_{NOM} should be set to 8.45k. With this value of R_{NOM}, α_{COLD} is 2.380 and the cold trip point is about 4°C. Notice that the span is now 46°C rather than the previous 45°C. This is due to the decrease in the temperature gain of the thermistor as the absolute temperature increases.

The upper and lower temperature trip points can be independently programmed by using an additional bias resistor as shown in Figure 8. The following formulas can be used to compute the values of R_{NOM} and R1:

$$R_{NOM} = \frac{\alpha_{COLD} - \alpha_{HOT}}{2.332} \bullet R25$$

$$R1 = 0.4839 \bullet R_{NOM} - \alpha_{HOT} \bullet R25$$

For example, to set the trip points to 0°C and 50°C with a Vishay curve 2 thermistor, choose:

$$R_{NOM} = \frac{2.816 - 0.4086}{2.332} \bullet 10k = 10.32k$$

the nearest 1% value is 10.2k:

$$R1 = 0.4839 \bullet 10.2k - 0.4086 \bullet 10k = 0.850k$$

The nearest 1% value is 845Ω. The final circuit is shown in Figure 8, and results in an upper trip point of 50°C and a lower trip point of 0°C.

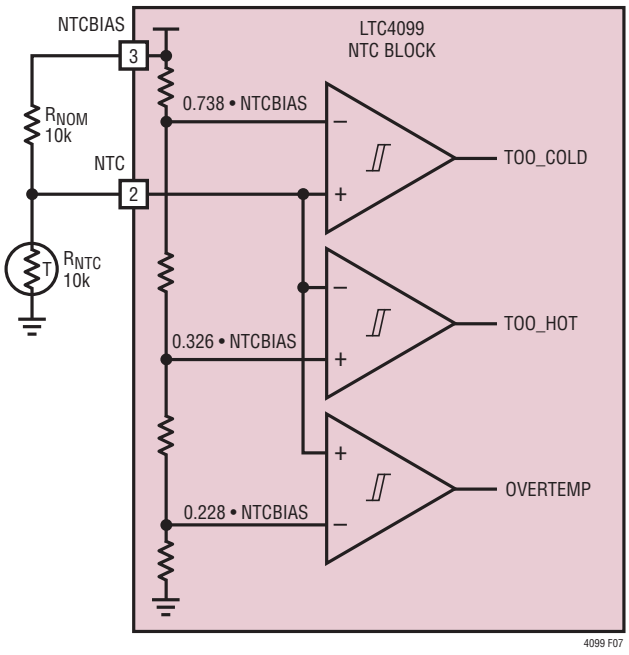


Figure 7. Standard NTC Configuration

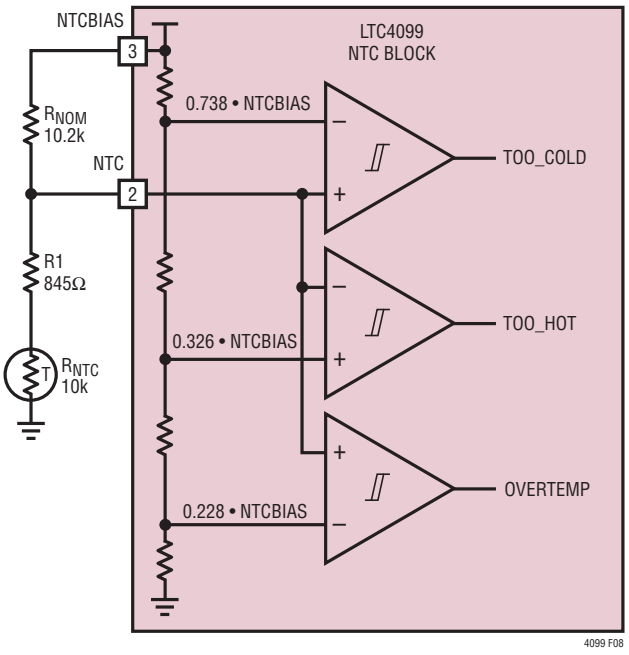


Figure 8. Modified NTC Configuration

APPLICATIONS INFORMATION

USB Inrush Limiting

Voltage overshoot on V_{BUS} may sometimes be observed when connecting the LTC4099 to a lab power supply. This overshoot is caused by long leads from the power supply to V_{BUS}. Twisting the wires together from the supply to V_{BUS} can greatly reduce the parasitic inductance of these long leads, and keep the voltage at V_{BUS} to safe levels. USB cables are generally manufactured with the power leads in close proximity, and thus fairly low parasitic inductance.

Board Layout Considerations

The Exposed Pad on the backside of the LTC4099 package must be securely soldered to the PC board ground. This is the primary ground pin in the package, and it serves as the return path for both the control circuitry and the synchronous rectifier.

Furthermore, due to its high frequency switching circuitry, it is imperative that the input capacitor, inductor, and output capacitor be as close to the LTC4099 as possible, and that there be an *unbroken* ground plane under the LTC4099 and all of its external high frequency components. High frequency currents, such as the input current on the LTC4099, tend to find their way on the ground plane along a mirror path directly beneath the incident path on the top of the board. If there are slits or cuts in the ground plane due to other traces on that layer, the current will be forced to go around the slits. If high frequency currents are not allowed to flow back through their natural least-area path, excessive voltage will build up and radiated emissions will occur (see Figure 9). There should be a group of vias directly under the grounded backside leading directly down to an internal ground plane. To minimize parasitic inductance, the ground plane should be as close as possible to the top plane of the PC board (layer 2).

The IDGATE pin for the external ideal diode controller has extremely limited drive current. Care must be taken to minimize leakage to adjacent PC board traces. 100nA of leakage from this pin will introduce an additional offset to the ideal diode of approximately 10mV. To minimize leakage, the trace can be guarded on the PC board by surrounding it with V_{OUT} connected metal, which should generally be less than 1V higher than IDGATE.

Battery Charger Stability Considerations

The LTC4099's battery charger contains both a constant-voltage and a constant-current control loop. The constant-voltage loop is stable without any compensation when a battery is connected with low impedance leads. Excessive lead length, however, may add enough series inductance to require a bypass capacitor of at least 1µF from BAT to GND.

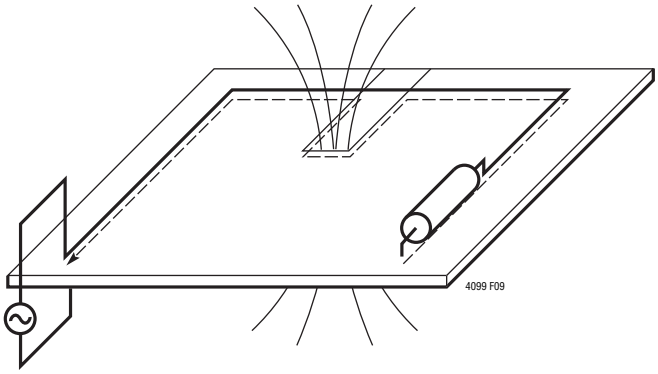


Figure 9. Higher Frequency Ground Currents Follow Their Incident Path. Slices in the Ground Plane Cause High Voltage and Increased Emissions

APPLICATIONS INFORMATION

High value, low ESR multilayer ceramic chip capacitors reduce the constant-voltage loop phase margin, possibly resulting in instability. Ceramic capacitors up to 100µF may be used in parallel with a battery, but larger ceramics should be decoupled with 0.2Ω to 1Ω of series resistance.

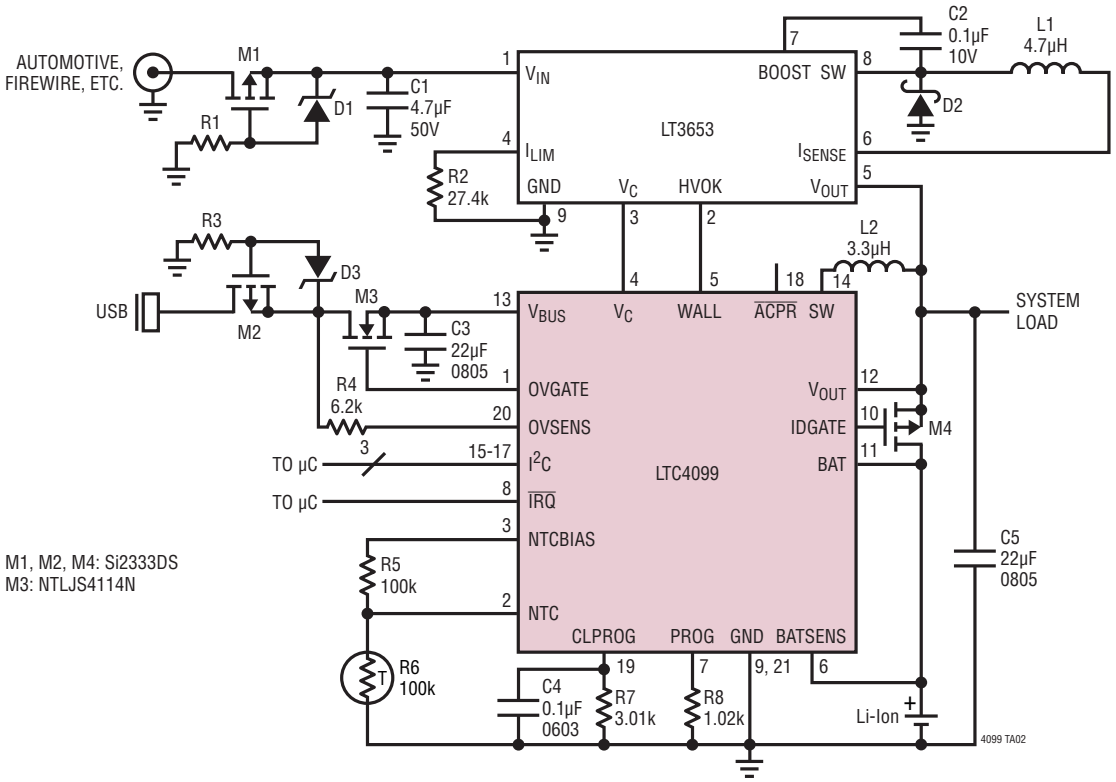
Furthermore, a 100µF MLCC in series with a 0.3Ω resistor or a 100µF OS-CON capacitor from BAT to GND is required to prevent oscillation when the battery is disconnected.

In constant-current mode, the PROG pin is in the feedback loop rather than the battery voltage. Because of the additional pole created by any PROG pin capacitance, capacitance on this pin must be kept to a minimum. With no additional capacitance on the PROG pin, the charger is stable for program resistor values as high as 25k. However, additional capacitance on this node reduces the maximum allowed program resistor. The pole frequency at the PROG pin should be kept above 100kHz. Therefore, if the PROG pin has a parasitic capacitance, C_{PROG}, the following equation should be used to calculate the maximum resistance value for R_{PROG}:

$$R_{PROG} \leq \frac{1}{2\pi \bullet 100kHz \bullet C_{PROG}}$$

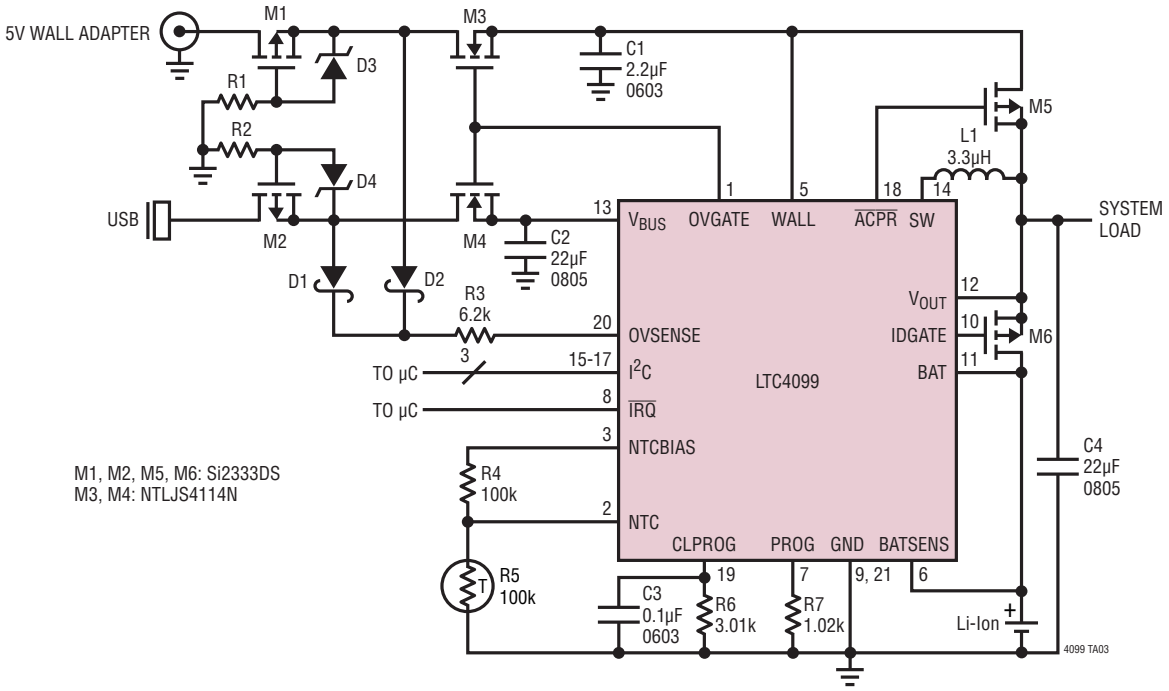
TYPICAL APPLICATIONS

High Efficiency USB/Automotive Battery Charger with Overvoltage Protection, Reverse-Voltage Protection and Low Battery Start-Up

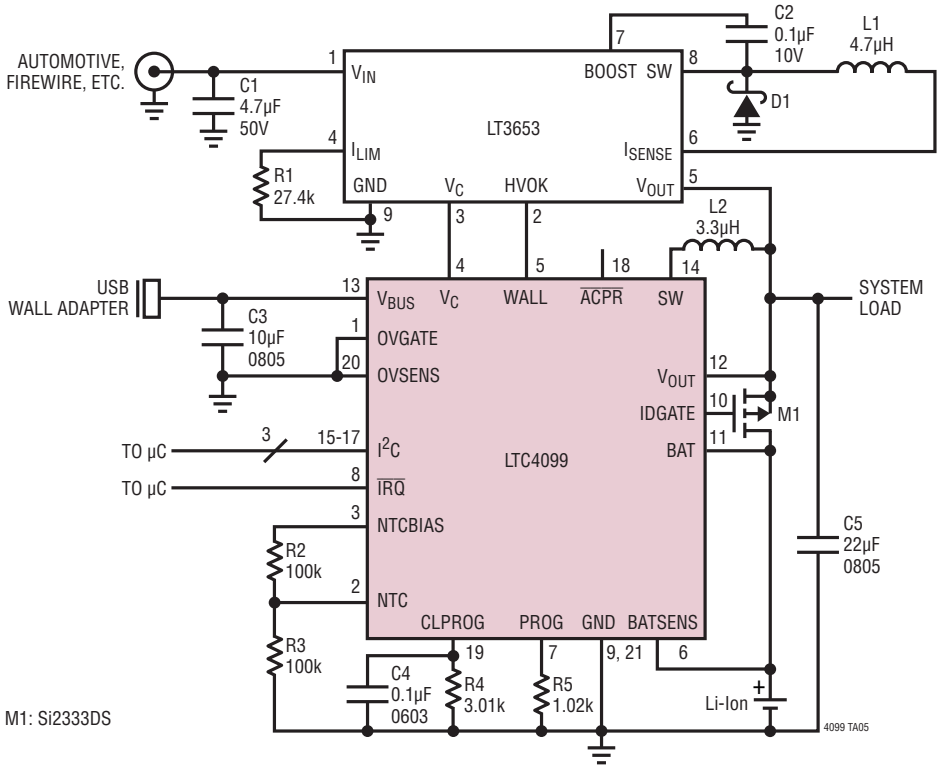


TYPICAL APPLICATIONS

USB/Wall Adapter Battery Charger with Dual Overvoltage Protection, Reverse-Voltage Protection and Low Battery Start-Up

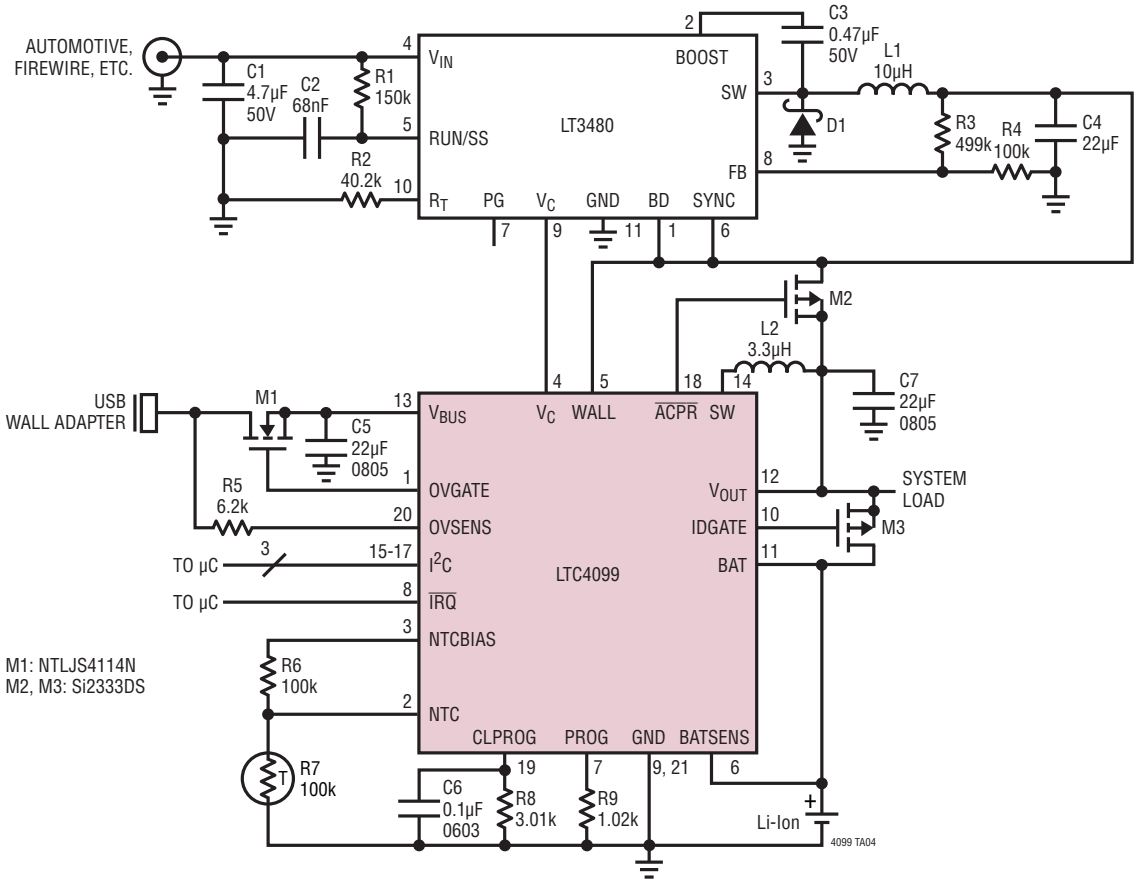


Low Component Count Power Manager with High and Low Voltage Inputs



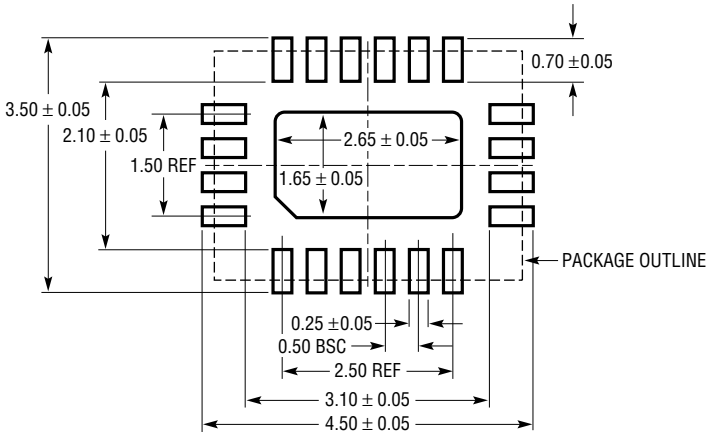
TYPICAL APPLICATIONS

USB/Automotive Switching Battery Charger with 2A Support From Automotive Input

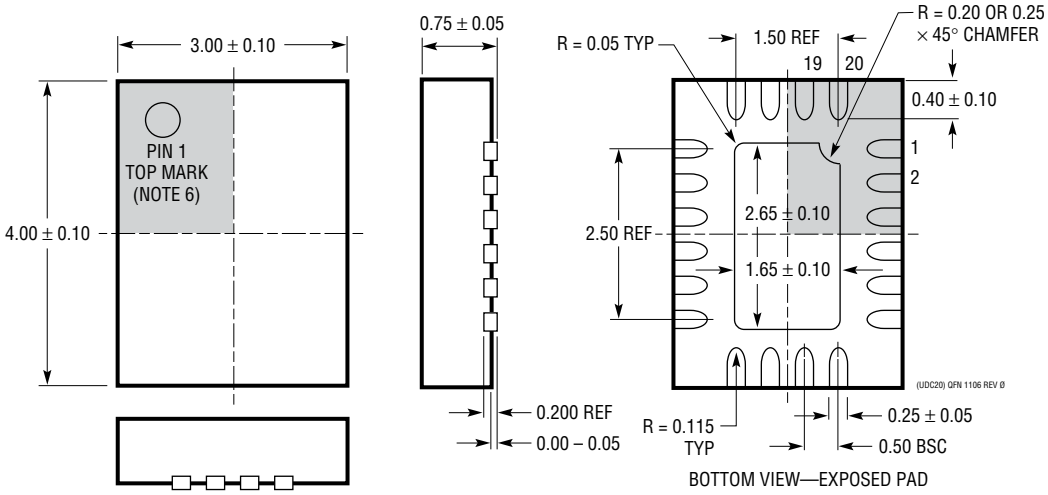


PACKAGE DESCRIPTION

UDC Package
20-Lead Plastic QFN (3mm × 4mm)
(Reference LTC DWG # 05-08-1742 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	10/09	Text Change to Features	1
		Text Changes to Description	1
		UDC Package Information Added to Pin Configuration	2
		Addition to Order Information	2
		Text Changes to Operation Section	16
		UDC Package Drawing Added	36
D	03/10	Changes to Features and Description	1
		Removal of PDC Package from Pin Configuration and Package Description	2, 34
		LTC4099EPDC Designated Obsolete in Order Information Section	2
		Changes to Electrical Characteristics	3, 4

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