3.3A Boost/Inverting DC/DC Converter with Fault Protection

FEATURES

- **3.3A, 42V Combined Power Switch**
- **Master/Slave (1.9A/1.4A) Switch Design**
- **Output Short Circuit Protection**
- **Wide Input Range: 2.5V to 22V Operating, 40V Maximum Transient**
- Switching Frequency Up to 2.5MHz
- Easily Configurable as a Boost, SEPIC, Inverting or Flyback Converter
- User Configurable Undervoltage Lockout
- Low V_{CESAT} Switch: 250mV at 2.75A (Typical)
- Can be Synchronized to External Clock
- Can Be Synchronized to other Switching Regulators
- High Gain $\overline{SHDN}$ Pin Accepts Slowly Varying Input Signals
- 14-Pin 4mm × 3mm DFN and 16-Lead MSE Packages

APPLICATIONS

- Local Power Supply
- Vacuum Fluorescent Display (VFD) Bias Supplies
- TFT-LCD Bias Supplies
- Automotive Engine Control Unit (ECU) Power

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DESCRIPTION

The LT®3581 is a PWM DC/DC converter with built-in fault protection features to aid in protecting against output shorts, input/output overvoltages, and overtemperature conditions. The part consists of a 42V master switch, and a 42V slave switch that can be tied together for a total current limit of 3.3A.

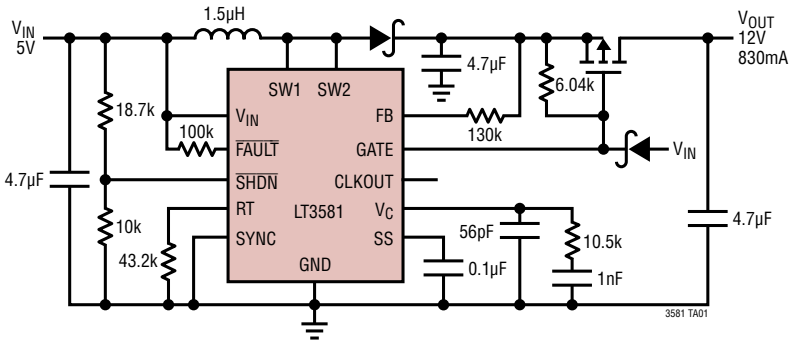
The LT3581 is ideal for many local power supply designs. It can be easily configured in Boost, SEPIC, Inverting or Flyback configurations, and is capable of generating 12V at 830mA, or –12V at 625mA from a 5V input. In addition, the LT3581's slave switch allows the part to be configured in high voltage, high power charge pump topologies that are very efficient and require fewer components than traditional circuits.

The LT3581's switching frequency range can be set between 200kHz and 2.5MHz. The part may be clocked internally at a frequency set by the resistor from the RT pin to ground, or it may be synchronized to an external clock. A buffered version of the clock signal is driven out of the CLKOUT pin, and may be used to synchronize other compatible switching regulator ICs to the LT3581.

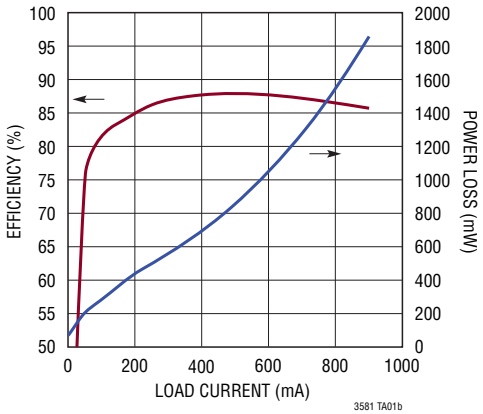
The LT3581 also features innovative $\overline{SHDN}$ pin circuitry that allows for slowly varying input signals and an adjustable undervoltage lockout function. Additional features such as frequency foldback and soft-start are integrated. The LT3581 is available in 14-Pin 4mm × 3mm DFN and 16-Lead MSE packages.

TYPICAL APPLICATION

Output Short Protected, 5V to 12V Boost Converter Operating at 2MHz



Efficiency and Power Loss vs Load Current

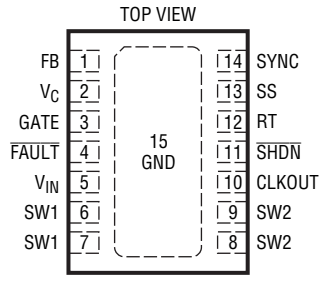


ABSOLUTE MAXIMUM RATINGS

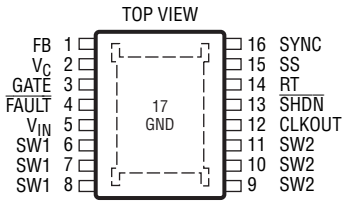
(Note 1)

V_{IN} Voltage ..... –0.3V to 40V
SW1/SW2 Voltage ..... –0.4V to 42V
RT Voltage ..... –0.3V to 5V
SS, FB Voltage ..... –0.3V to 2.5V
V_C Voltage ..... –0.3V to 2V
$\overline{SHDN}$ Voltage ..... –0.3V to 40V
SYNC Voltage ..... –0.3V to 5.5V
GATE Voltage ..... –0.3V to 80V
$\overline{FAULT}$ Voltage ..... –0.3V to 40V
$\overline{FAULT}$ Current ..... ±500µA
CLKOUT Voltage ..... –0.3V to 3V
CLKOUT Current 1mA
Operating Junction Temperature Range
LT3581E (Notes 2, 4) ..... –40°C to 125°C
LT3581I (Notes 2, 4) ..... –40°C to 125°C
LT3581H (Notes 2, 4) ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



DE14 PACKAGE
14-PIN (4mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W, θ_{JC} = 4.3°C/W
EXPOSED PAD (PIN 15) IS GND, MUST BE SOLDERED TO PCB



MSE PACKAGE
16-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 45°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3581EDE#PBF	LT3581EDE#TRPBF	3581	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LT3581IDE#PBF	LT3581IDE#TRPBF	3581	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LT3581HDE#PBF	LT3581HDE#TRPBF	3581	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 150°C
LT3581EMSE#PBF	LT3581EMSE#TRPBF	3581	16-Lead Plastic MSOP	–40°C to 125°C
LT3581IMSE#PBF	LT3581IMSE#TRPBF	3581	16-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, $V_{\overline{SHDN}}$ = V_{IN}, $V_{\overline{FAULT}}$ = V_{IN}, unless otherwise noted. (Note 2).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage		●		2.3	2.5	V
V_{IN} Overvoltage Lockout			22.1	23.5	25	V
Positive Feedback Voltage		●	1.195	1.215	1.230	V
Negative Feedback Voltage		●	3	9	16	mV
Positive FB Pin Bias Current	V_{FB} = Positive Feedback Voltage, Current into Pin	●	81	83.3	85	µA
Negative FB Pin Bias Current	V_{FB} = Negative Feedback Voltage, Current out of Pin	●	81	83.3	85.5	µA
Error Amp Transconductance	ΔI = 10µA			270		µmhos
Error Amp Voltage Gain				70		V/V
Quiescent Current	Not Switching			1.9	2.3	mA
Quiescent Current in Shutdown	$V_{\overline{SHDN}}$ = 0V			0	1	µA
Reference Line Regulation	2.5V ≤ V_{IN} ≤ 20V			0.01	0.05	%/V
Switching Frequency, f_{OSC}	R_T = 34k	●	2.25	2.5	2.75	MHz
	R_T = 432k	●	180	200	220	kHz
Switching Frequency in Foldback	Compared to Normal f_{OSC}			1/6		ratio
Switching Frequency Range	Free-Running or Synchronizing	●	200		2500	kHz
SYNC High Level for Synchronization		●	1.3			V
SYNC Low Level for Synchronization		●			0.4	V
SYNC Clock Pulse Duty Cycle	V_{SYNC} = 0V to 2V		20		80	%
Recommended Minimum SYNC Ratio f_{SYNC}/f_{OSC}				3/4		
Minimum Off-Time				45		ns
Minimum On-Time				55		ns
SW1 Current Limit	At All Duty Cycles	●	1.9	2.4	3	A
Current Sharing (SW2/SW1)				78		%
SW1 + SW2 Current Limit	At All Duty Cycles, SW2/SW1 = 78% (Note 3)	●	3.3	4.3	5.4	A
Switch V_{CESAT}	SW1 & SW2 Tied Together, I_{SW1} + I_{SW2} = 2.75A			250		mV
SW1 Leakage Current	V_{SW1} = 5V			0.01	1	µA
SW2 Leakage Current	V_{SW2} = 5V			0.01	1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, $V_{\overline{SHDN}}$ = V_{IN}, $V_{\overline{FAULT}}$ = V_{IN}, unless otherwise noted. (Note 2).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Soft-Start Charge Current	V_{SS} = 30mV, Current Flows Out of SS pin	●	5.7	8.7	11.3	µA
Soft-Start Discharge Current	Part in FAULT, V_{SS} = 2.1V, Current Flows into SS Pin	●	5.7	8.7	11.3	µA
Soft-Start High Detection Voltage	Part in FAULT	●	1.65	1.8	1.95	V
Soft-Start Low Detection Voltage	Part Exiting FAULT	●	30	50	85	mV
$\overline{SHDN}$ Minimum Input Voltage High	Active Mode, $\overline{SHDN}$ Rising (LT3581E, LT3581I) Active Mode, $\overline{SHDN}$ Rising (LT3581H) Active Mode, $\overline{SHDN}$ Falling (LT3581E, LT3581I, LT3581H)	● ● ●	1.27 1.27 1.24	1.33 1.33 1.3	1.41 1.44 1.38	V V V
$\overline{SHDN}$ Input Voltage Low	Shutdown Mode	●			0.3	V
$\overline{SHDN}$ Pin Bias Current	$V_{\overline{SHDN}}$ = 3V $V_{\overline{SHDN}}$ = 1.3V $V_{\overline{SHDN}}$ = 0V		 9.7 	40 11.4 0	60 13.4 0.1	µA µA µA
CLKOUT Output Voltage High	C_{CLKOUT} = 50pF		1.9	2.1	2.3	V
CLKOUT Output Voltage Low	C_{CLKOUT} = 50pF			5	200	mV
CLKOUT Duty Cycle	T_J = 25°C			42		%
CLKOUT Rise Time	C_{CLKOUT} = 50pF			12		ns
CLKOUT Fall Time	C_{CLKOUT} = 50pF			8		ns
GATE Pull Down Current	V_{GATE} = 3V (LT3581E, LT3581I) V_{GATE} = 3V (LT3581H) V_{GATE} = 80V (LT3581E, LT3581I, LT3581H)	● ● ●	800 700 800	933 900 933	1100 1100 1100	µA µA µA
GATE Leakage Current	V_{GATE} = 50V, GATE Off			0.01	1	µA
$\overline{FAULT}$ Output Voltage Low	50µA into $\overline{FAULT}$ Pin (LT3581E, LT3581I) 50µA into $\overline{FAULT}$ Pin (LT3581H)	● ●		100 100	300 400	mV mV
$\overline{FAULT}$ Leakage Current	$V_{\overline{FAULT}}$ = 40V, $\overline{FAULT}$ Off			0.01	1	µA
$\overline{FAULT}$ Input Voltage Low		●	700	750	800	mV
$\overline{FAULT}$ Input Voltage High		●	950	1000	1050	mV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

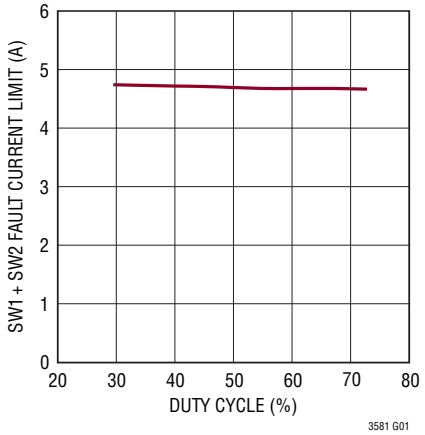
Note 2: The LT3581E is guaranteed to meet performance specifications from 0°C to 125°C. Specifications over the –40°C to 125°C junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3581I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3581H is guaranteed over the full –40°C to 150°C operating junction temperature range. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 3: Current limit guaranteed by design and/or correlation to static test.

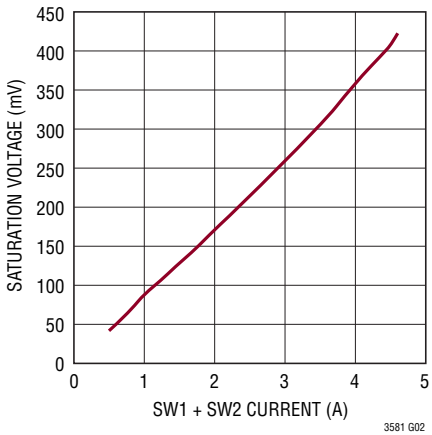
Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation over the specified maximum operating junction temperature may impair device reliability.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

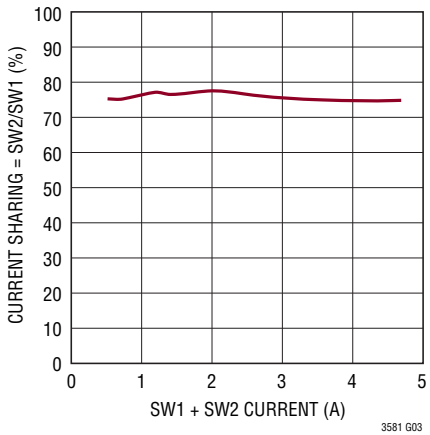
Switch Fault Current Limit vs Duty Cycle



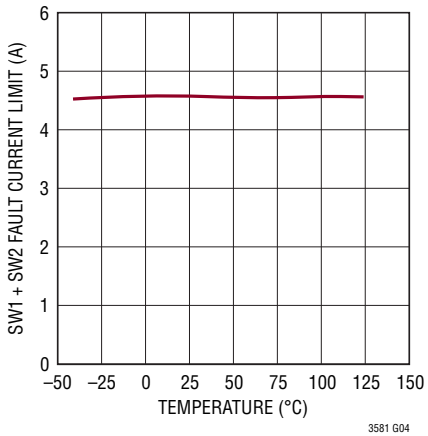
Switch Saturation Voltage with SW1 and SW2 Tied Together



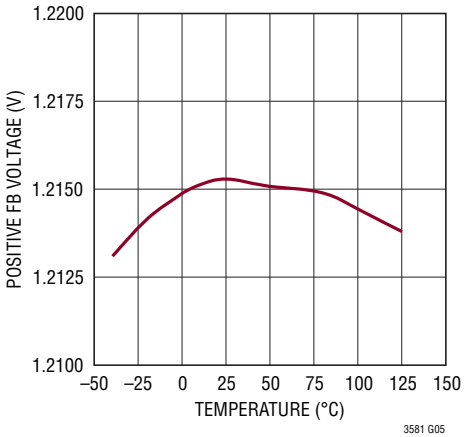
Current Sharing Between SW1 and SW2 When Tied Together



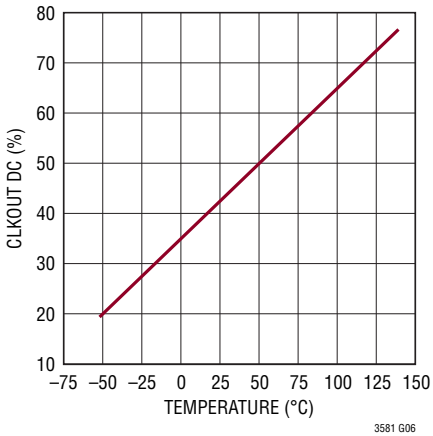
Switch Fault Current Limit vs Temperature



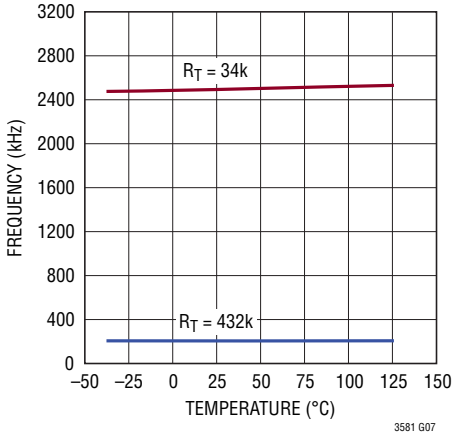
Positive Feedback Voltage vs Temperature



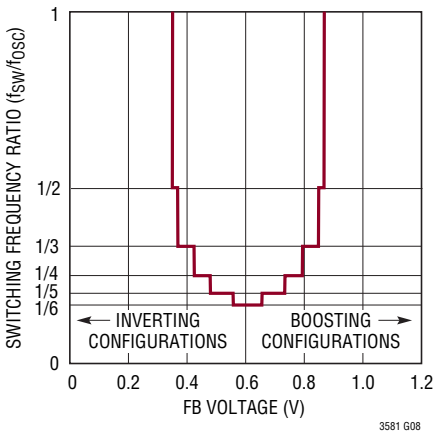
CLKOUT Duty Cycle vs Temperature



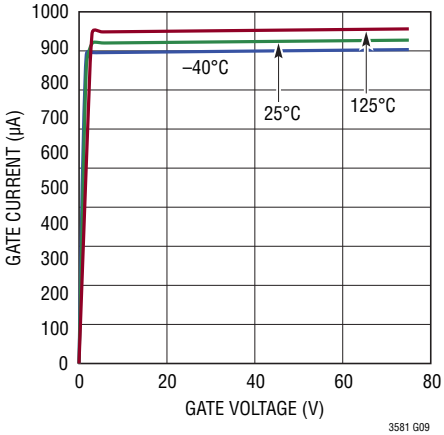
Oscillator Frequency



Frequency Foldback

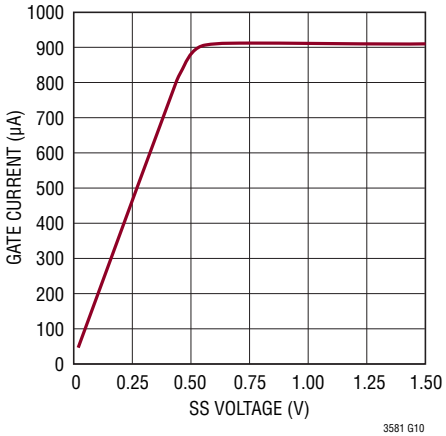


Gate Current vs Gate Voltage

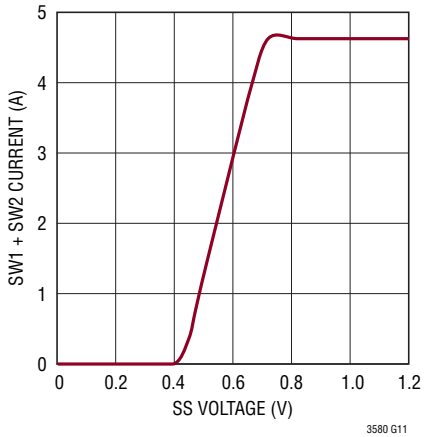


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

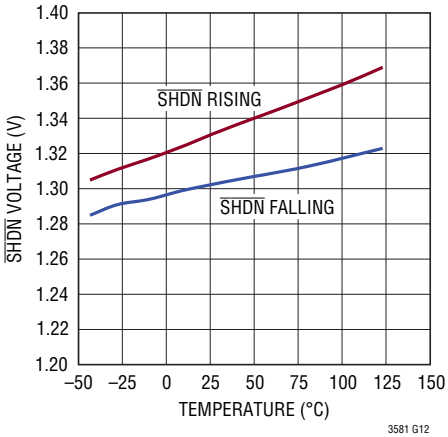
Gate Current vs SS Voltage



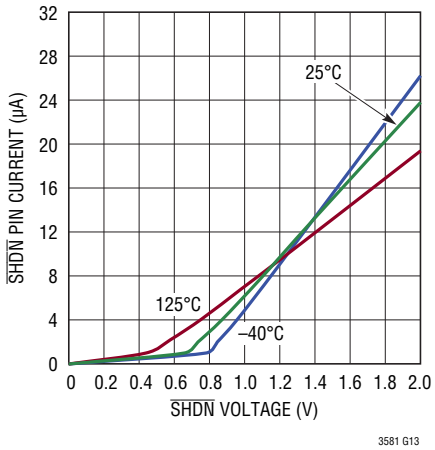
Commanded Current Limit vs SS Voltage



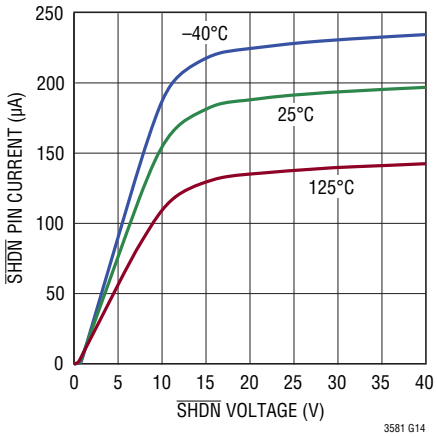
$\overline{SHDN}$ Voltage Threshold with Hysteresis



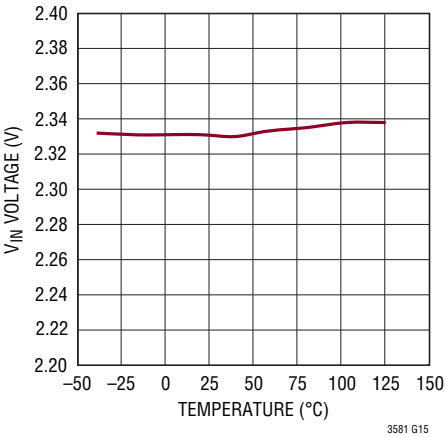
$\overline{SHDN}$ Pin Current



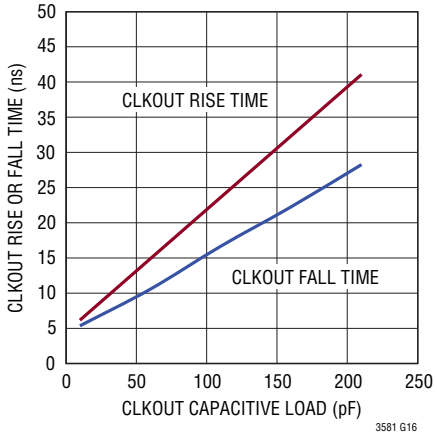
$\overline{SHDN}$ Pin Current



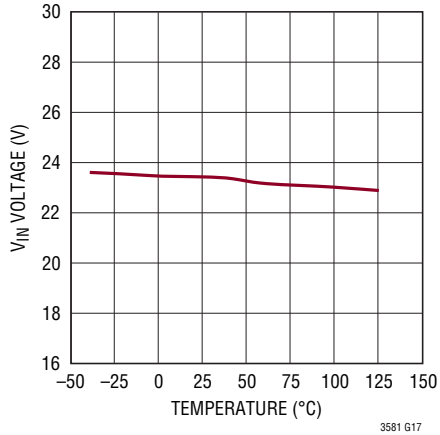
Internal UVLO



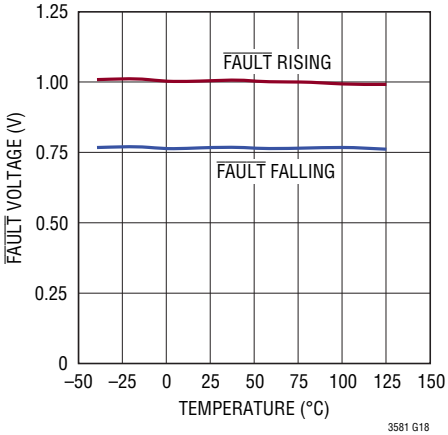
CLKOUT Rise Time at 1MHz



V_{IN} OVLO



$\overline{FAULT}$ Input Voltage Threshold with Hysteresis



PIN FUNCTIONS (DFN/MSOP)

FB (Pin 1/Pin 1): Positive and Negative Feedback Pin. For a Boost or Inverting Converter, tie a resistor from the FB pin to V_{OUT} according to the following equations:

$$R_{FB} = \left(\frac{V_{OUT} - 1.215V}{83.3 \bullet 10^{-6}}\right); \text{Boost or SEPIC Converter}$$

$$R_{FB} = \left(\frac{|V_{OUT}| + 9mV}{83.3 \bullet 10^{-6}}\right); \text{Inverting Converter}$$

V_C (Pin 2/Pin 2): Error Amplifier Output Pin. Tie external compensation network to this pin.

GATE (Pin 3/Pin 3): PMOS Gate Drive Pin. The GATE pin is a pull-down current source, used to drive the gate of an external PMOS for output short circuit protection or output disconnect. The GATE pin current increases linearly with the SS pin's voltage, with a maximum pull-down current of 933µA at SS voltages exceeding 500mV. Note that if the SS voltage is greater than 500mV and the GATE pin voltage is less than 2V, then the GATE pin looks like a 2kΩ impedance to ground. See the Appendix for more information.

$\overline{\text{FAULT}}$ (Pin 4/Pin 4): Fault Indication Pin. This active low, bidirectional pin can either be pulled low (below 750mV) by an external source, or internally by the chip to indicate a fault. When pulled low, this pin causes the power switches to turn off, the GATE pin to become high impedance, the CLKOUT pin to become disabled, and the SS pin to go through a charge/discharge sequence. The end/absence of a fault is indicated when the voltage on this pin exceeds 1V. A pull-up resistor or current source is needed on this pin to pull it above 1V in the absence of a fault.

V_{IN} (Pin 5/Pin 5): Input Supply Pin. Must be locally by-passed.

SW1 (Pins 6, 7/Pins 6,7, 8): Master Switch Pin. This is the collector of the internal master NPN power switch. Minimize the metal trace area connected to this pin to minimize EMI.

SW2 (Pins 8, 9/Pins 9, 10, 11): Slave Switch Pin. This is the collector of the internal slave NPN power switch. Minimize the metal trace area connected to this pin to minimize EMI.

CLKOUT (Pin 10/Pin 12): Clock Output Pin. Use this pin to synchronize one or more other compatible switching regulator ICs to the LT3581. The clock that this pin outputs runs at the same frequency as the internal oscillator of the part or as the SYNC pin. CLKOUT may also be used as a temperature monitor since the CLKOUT pin's duty cycle varies linearly with the part's junction temperature. Note that the CLKOUT pin is only meant to drive capacitive loads up to 50pF.

$\overline{\text{SHDN}}$ (Pin 11/Pin 13): Shutdown Pin. In conjunction with the UVLO (undervoltage lockout) circuit, this pin is used to enable/disable the chip and restart the soft-start sequence. Drive below 300mV to disable the chip. Drive above 1.33V (typical) to activate the chip and restart the soft-start sequence. Do not float this pin.

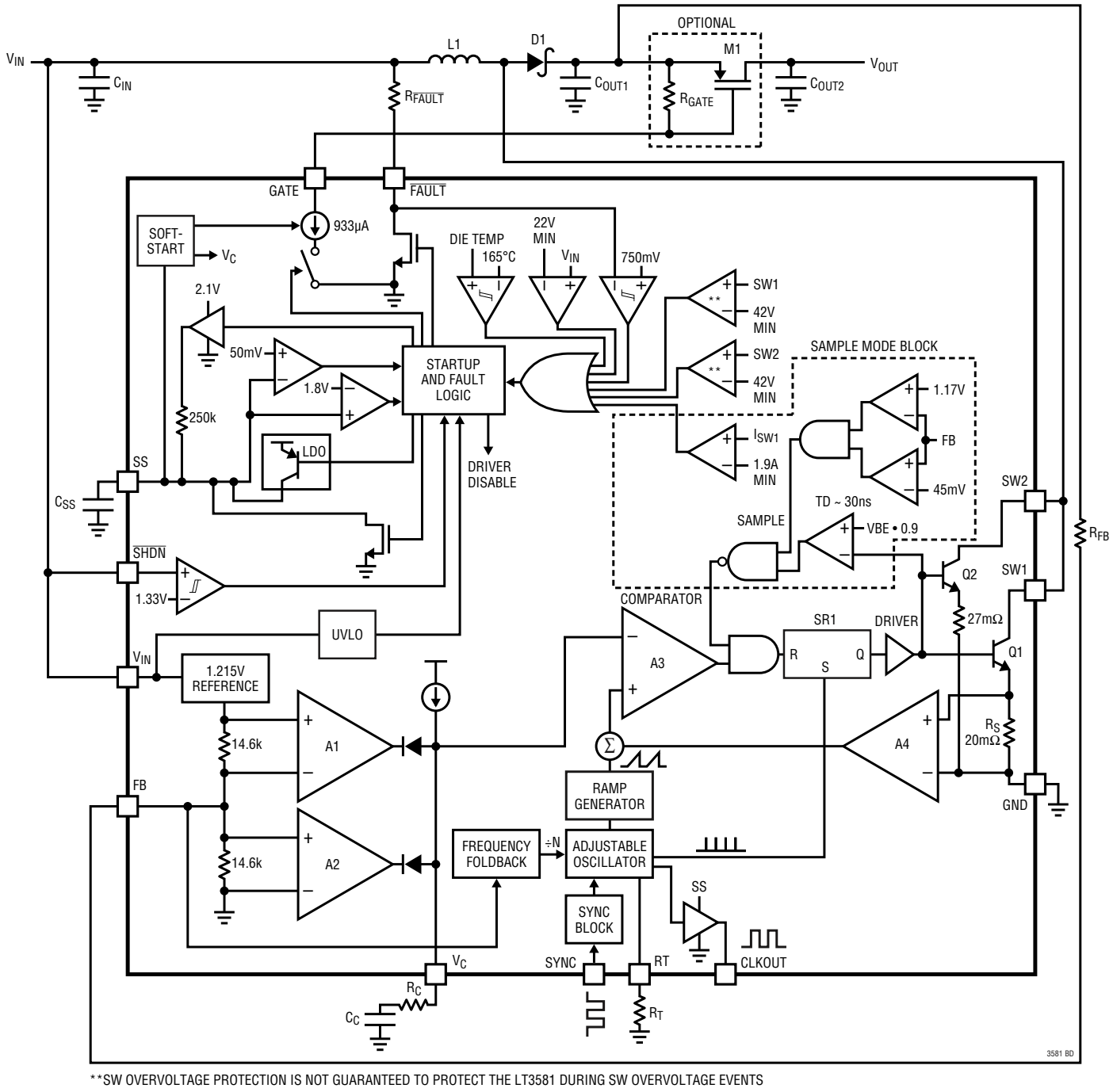
RT (Pin 12/Pin 14): Timing Resistor Pin. Adjusts the LT3581's switching frequency. Place a resistor from this pin to ground to set the frequency to a fixed free running level. Do not float this pin.

SS (Pin 13/Pin 15): Soft-Start Pin. Place a soft-start capacitor here. Upon start-up, the SS pin will be charged by a (nominally) 250k resistor to about 2.1V. During a fault, the SS pin will be slowly charged up and eventually discharged as part of a timeout sequence (see the State Diagram for more information on the SS pin's role during a fault event).

SYNC (Pin 14/Pin 16): To synchronize the switching frequency to an outside clock, simply drive this pin with a clock. The high voltage level of the clock must exceed 1.3V, and the low level must be less than 0.4V. Drive this pin to less than 0.4V to revert to the internal free running clock. See the Applications Information section for more information.

GND (Exposed Pad Pin 15/Exposed Pad Pin 17): Ground. Exposed pad must be soldered directly to local ground plane.

BLOCK DIAGRAM



**SW OVERVOLTAGE PROTECTION IS NOT GUARANTEED TO PROTECT THE LT3581 DURING SW OVERVOLTAGE EVENTS

Figure 1. Block Diagram

STATE DIAGRAM

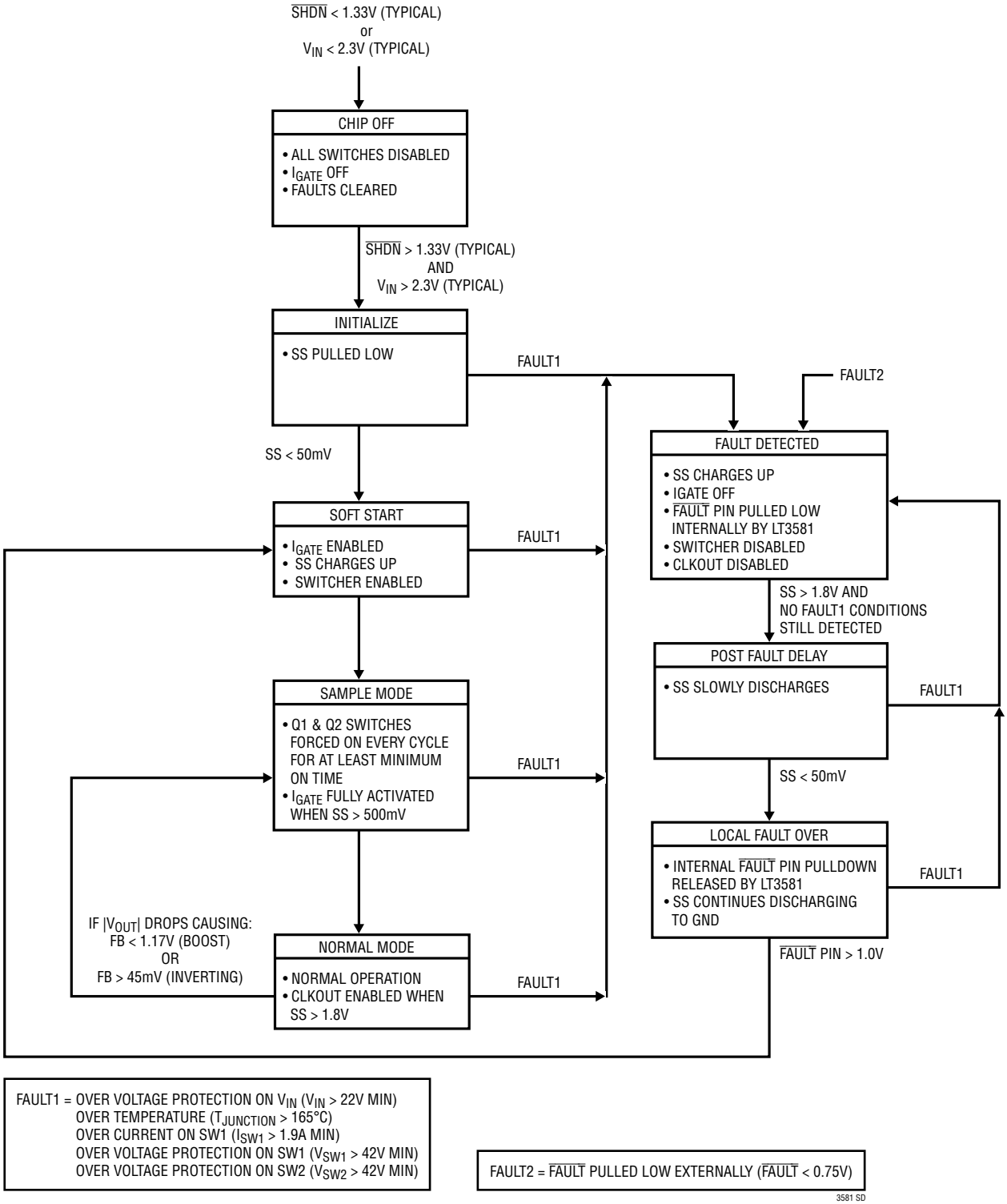


Figure 2. State Diagram

OPERATION

OPERATION – OVERVIEW

The LT3581 uses a constant-frequency, current mode control scheme to provide excellent line and load regulation. The part's undervoltage lockout (UVLO) function, together with soft-start and frequency foldback, offers a controlled means of starting up. Fault features are incorporated in the LT3581 to aid in the detection of output shorts, over-voltage, and overtemperature conditions. Refer to the Block Diagram (Figure 1) and the State Diagram (Figure 2) for the following description of the part's operation.

OPERATION – START-UP

Several functions are provided to enable a very clean start-up for the LT3581:

Precise Turn-On Voltage

The $\overline{SHDN}$ pin is compared to an internal voltage reference to give a precise turn on voltage level. Taking the $\overline{SHDN}$ pin above 1.33V (typical) enables the part. Taking the $\overline{SHDN}$ pin below 300mV shuts down the chip, resulting in extremely low quiescent current. The $\overline{SHDN}$ pin has 30mV of hysteresis to protect against glitches and slow ramping.

Undervoltage Lockout (UVLO)

The $\overline{SHDN}$ pin can also be used to create a configurable UVLO. The UVLO function sets the turn on/off of the LT3581 at a desired input voltage (V_{INUVLO}). Figure 3 shows how a resistor divider (or single resistor) from V_{IN} to the $\overline{SHDN}$ pin can be used to set V_{INUVLO}. R_{UVLO2} is optional. It may be left out, in which case set it to infinite in the equation below. For increased accuracy, set $R_{UVLO2} \leq 10k$. Pick R_{UVLO1} as follows:

$$R_{UVLO1} = \frac{V_{INUVLO} - 1.33V}{\left(\frac{1.33V}{R_{UVLO2}}\right) + 11.6\mu A}$$

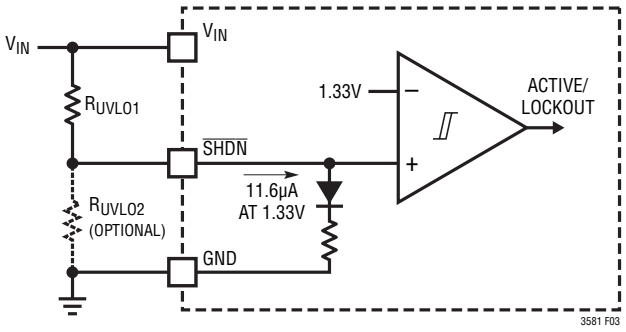


Figure 3. Configurable UVLO

The LT3581 also has internal UVLO circuitry that disables the chip when $V_{IN} < 2.3V$ (typical).

Soft-Start of Switch Current

The soft-start circuitry provides for a gradual ramp-up of the switch current (refer to Commanded Current Limit vs SS Voltage in Typical Performance Characteristics). When the part is brought out of shutdown, the external SS capacitor is first discharged which resets the states of the logic circuits in the chip. Then an integrated 250k resistor pulls the SS pin to ~1.8V. The ramp rate of the SS pin voltage is set by this 250k resistor and the external capacitor connected to this pin. Once SS gets to 1.8V, the CLKOUT pin is enabled, and an internal regulator pulls the pin up quickly to ~2.1V. Typical values for the external soft-start capacitor range from 100nF to 1µF.

Soft-Start of External PMOS (if used)

The soft-start circuitry also gradually ramps up the GATE pin pull-down current which allows an external PMOS to slowly turn on (M1 in Block Diagram). The GATE pin current increases linearly with the SS voltage, with a maximum current of 933µA when the SS voltage gets above 500mV. Note that if the GATE pin voltage is less than 2V for SS voltages exceeding 500mV, then the GATE pin impedance to ground is 2kΩ. The soft turn on of the external PMOS helps limit inrush current at start-up, making hot-plugs of LT3581s feasible and safe.

OPERATION

Sample Mode

Sample Mode is the mechanism used by the LT3581 to aid in the detection of output shorts. It refers to a state of the LT3581 where the master and slave power switches (Q1 and Q2) are turned on for a minimum period of time every clock cycle (or every few clock cycles in frequency foldback) in order to "sample" the inductor current. If the sampled current through Q1 exceeds the master switch current limit of 1.9A (min), the LT3581 triggers an overcurrent fault internally (see Operation-Fault section for details). Sample Mode is active when FB is out of regulation by more than approximately 3.7% (45mV < FB < 1.17V).

Frequency Foldback

The frequency foldback circuit reduces the switching frequency when 350mV < FB < 900mV (typical). This feature lowers the minimum duty cycle that the part can achieve, thus allowing better control of the inductor current during start-up. When the FB voltage is pulled outside of this range, the switching frequency returns to normal.

Note that the peak inductor current at start-up is a function of many variables including load profile, output capacitance, target V_{OUT}, V_{IN}, switching frequency, etc. **Test each and every application's performance at start-up to ensure that the peak inductor current does not exceed the minimum fault current limit.**

OPERATION – REGULATION

The following description of the LT3581's operation assumes that the FB voltage is close enough to its regulation target so that the part is not in sample mode. Use the Block Diagram as a reference when stepping through the following description of the LT3581 operating in regulation. At the start of each oscillator cycle, the SR latch (SR1) is set, which turns on the power switches Q1 and Q2. The collector current through the master switch, Q1, is ~1.3 times the collector current through the slave switch, Q2, when the collectors of the two switches are tied together. Q1's emitter current flows through a current sense resistor (R_S) generating a voltage proportional to the total switch current. This voltage (amplified by A4) is added to a stabilizing ramp and the resulting sum is fed into the positive terminal of the PWM comparator A3. When the voltage on the positive input of A3 exceeds the voltage on the negative input, the SR latch is reset, turning off the master and slave power switches. The voltage on the negative input of A3 (V_C pin) is set by A1 (or A2), which is simply an amplified difference between the FB pin voltage and the reference voltage (1.215V if the LT3581 is configured as a boost converter, or 9mV if configured as an inverting converter). In this manner, the error amplifier sets the correct peak current level to maintain output regulation.

As long as the part is not in fault (see Operation – Fault section) and the SS pin exceeds 1.8V, the LT3581 drives its CLKOUT pin at the frequency set by the RT pin or the SYNC pin. The CLKOUT pin can be used to synchronize other compatible switching regulator ICs (including additional LT3581s) with the LT3581. Additionally, CLKOUT's duty cycle varies linearly with the part's junction temperature, and may be used as a temperature monitor.

OPERATION – FAULT

The LT3581's $\overline{\text{FAULT}}$ pin is an active low, bidirectional pin that is pulled low to indicate a fault. Each of the following events can trigger a fault in the LT3581:

A. FAULT1 events:
   1. SW Overcurrent:
      a. I_{SW1} > 1.9A (minimum)
      b. (I_{SW1} + I_{SW2}) > 3.3A (minimum)
   2. V_{IN} Voltage > 22V (minimum)
   3. SW1 Voltage and/or SW2 Voltage > 42V (minimum)
   4. Die Temperature > 165°C

B. FAULT2 events:
   1. Pulling the $\overline{\text{FAULT}}$ pin low externally

OPERATION

Refer to the State Diagram (Figure 2) for the following description of the LT3581's operation during a fault event. When a fault is detected, in addition to the $\overline{FAULT}$ pin being pulled low internally, the LT3581 also disables its CLKOUT pin, turns off its power switches, and the GATE pin becomes high impedance. The external PMOS, M1, turns off when the gate of M1 is pulled up to its source by the external R_{GATE} resistor (see Block Diagram). With the external PMOS turned off, the power path from V_{IN} to V_{OUT} is cut off, protecting power components downstream.

At the same time, a timeout sequence commences where the SS pin is charged up to 1.8V (the SS pin will continue charging up to 2.1V and be held there in the case of a FAULT1 event that has still not ended), and then discharged to 50mV. This timeout period relieves the part, the PMOS, and other downstream power components from electrical and thermal stress for a minimum amount of time as set by the voltage ramp rate on the SS pin.

In the absence of faults, the $\overline{FAULT}$ pin is pulled high by the external $R_{\overline{FAULT}}$ resistor (typically 100k). Figure 4 shows the events that accompany the detection of an output short on the LT3581.

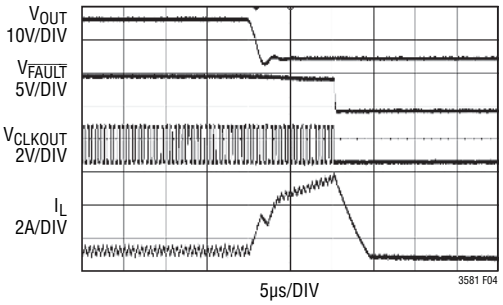


Figure 4. Output Short Circuit Protection of the LT3581

APPLICATIONS INFORMATION

BOOST CONVERTER COMPONENT SELECTION

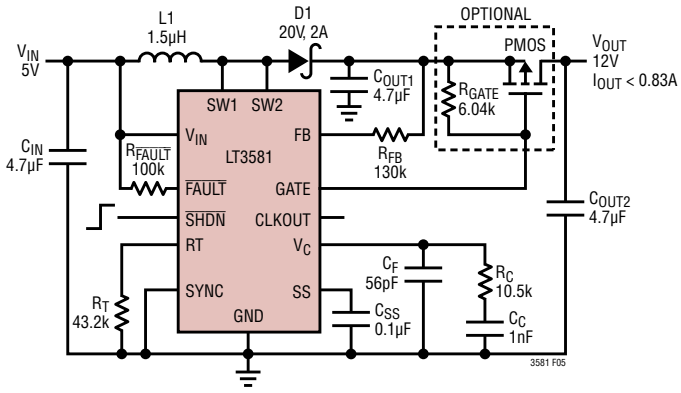


Figure 5. Boost Converter – The Component Values and Voltages Given Are Typical Values for a 2MHz, 5V to 12V Boost

The LT3581 can be configured as a Boost converter as in Figure 5. This topology allows for positive output voltages that are higher than the input voltage. An external PMOS (optional) driven by the GATE pin of the LT3581 can achieve input or output disconnect during a fault event. A single feedback resistor sets the output voltage. For output voltages higher than 40V, see the Charge Pump Aided Regulators section.

Table 1 is a step-by-step set of equations to calculate component values for the LT3581 when operating as a boost converter. Input parameters are input and output voltage, and switching frequency (V_{IN}, V_{OUT} and f_{OSC} respectively). Refer to the Appendix for further information on the design equations presented in Table 1.

Variable Definitions:

V_{IN} = Input Voltage
V_{OUT} = Output Voltage
DC = Power Switch Duty Cycle
f_{OSC} = Switching Frequency
I_{OUT} = Maximum Average Output Current
I_{RIPPLE} = Inductor Ripple Current
R_{DSON_PMOS} = R_{DSON} of External PMOS (set to 0 if not using PMOS)

Table 1. Boost Design Equations

	PARAMETERS/EQUATIONS
Step 1: Inputs	Pick V_{IN}, V_{OUT}, and f_{OSC} to calculate equations below.
Step 2: DC	$DC \cong \frac{V_{OUT} - V_{IN} + 0.5V}{V_{OUT} + 0.5V - 0.3V}$
Step 3: L1	$L_{TYP} = \frac{(V_{IN} - 0.3V) \bullet DC}{f_{OSC} \bullet 1A}$ (1) $L_{MIN} = \frac{(V_{IN} - 0.3V) \bullet (2 \bullet DC - 1)}{2.2A \bullet f_{OSC} \bullet (1 - DC)}$ (2) $L_{MAX} = \frac{(V_{IN} - 0.3V) \bullet DC}{f_{OSC} \bullet 0.35A}$ (3) • Pick L1 out of a range of inductor values where the minimum value of the range is set by L_{TYP} or L_{MIN}, whichever is higher. The maximum value of the range is set by L_{MAX}. See appendix on how to choose current rating for inductor value chosen.
Step 4: I_{RIPPLE}	$I_{RIPPLE} = \frac{(V_{IN} - 0.3V) \bullet DC}{f_{OSC} \bullet L_1}$
Step 5: I_{OUT}	$I_{OUT} = \left(3.3A - \frac{I_{RIPPLE}}{2}\right) \bullet (1 - DC)$
Step 6: D1	$V_R > V_{OUT}$; $I_{AVG} > I_{OUT}$
Step 7: C_{OUT1}, C_{OUT2}	$C_{OUT1} = C_{OUT2} \geq \frac{I_{OUT} \bullet DC}{f_{OSC}[0.01 \bullet V_{OUT} - 0.50 \bullet I_{OUT} \bullet R_{DSON\_PMOS}]}$ • If PMOS is not used, then use just one capacitor where $C_{OUT} = C_{OUT1} + C_{OUT2}$.
Step 8: C_{IN}	$C_{IN} \geq C_{VIN} + C_{PWR} \geq \frac{3.3A \bullet DC}{45 \bullet f_{OSC} \bullet 0.005 \bullet V_{IN}} + \frac{I_{RIPPLE}}{8 \bullet f_{OSC} \bullet 0.005 \bullet V_{IN}}$ • Refer to Input Capacitor Selection in Appendix for definition of C_{VIN} and C_{PWR}.
Step 9: R_{FB}	$R_{FB} = \frac{V_{OUT} - 1.215V}{83.3\mu A}$
Step 10: R_T	$R_T = \frac{87.6}{f_{OSC}} - 1$; f_{OSC} in MHz and R_T in kΩ
Step 11: PMOS	Only needed for input or output disconnect. See PMOS Selection in the Appendix for information on sizing the PMOS, R_{GATE} and picking appropriae UVLO components.

Note 1: The maximum design target for peak switch current is 3.3A and is used in this table.

Note 2: The final values for C_{OUT1}, C_{OUT2} and C_{IN} may deviate from the above equations in order to obtain desired load transient performance.

APPLICATIONS INFORMATION

SEPIC CONVERTER COMPONENT SELECTION (COUPLED OR UN-COUPLED INDUCTORS)

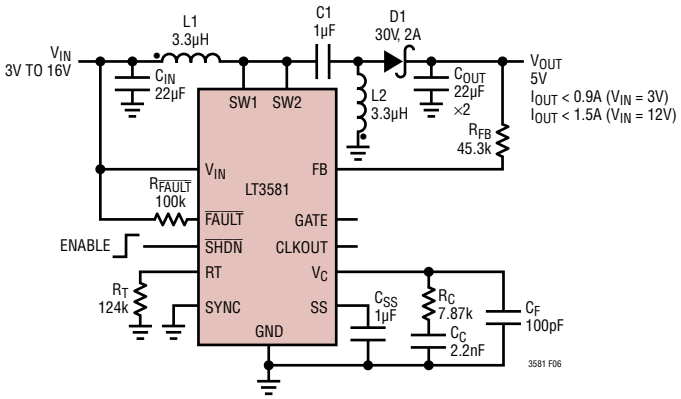


Figure 6. SEPIC Converter – The Component Values and Voltages Given Are Typical Values for a 700kHz, Wide Input Range (3V to 16V) SEPIC Converter with 5V Out

The LT3581 can also be configured as a SEPIC as shown in Figure 6. This topology allows for positive output voltages that are lower, equal, or higher than the input voltage. Output disconnect is inherently built into the SEPIC topology, meaning no DC path exists between the input and output due to capacitor C1. This implies that a PMOS controlled by the GATE pin is not required in the power path.

Table 2 is a step-by-step set of equations to calculate component values for the LT3581 when operating as a SEPIC converter. Input parameters are input and output voltage, and switching frequency (V_{IN}, V_{OUT} and f_{OSC} respectively). Refer to the Appendix for further information on the design equations presented in Table 2.

Variable Definitions:

V_{IN} = Input Voltage
V_{OUT} = Output Voltage
DC = Power Switch Duty Cycle
f_{OSC} = Switching Frequency
I_{OUT} = Maximum Average Output Current
I_{RIPPLE} = Inductor Ripple Current

Table 2. SEPIC Design Equations

	PARAMETERS/EQUATIONS
Step 1: Inputs	Pick V_{IN}, V_{OUT}, and f_{OSC} to calculate equations below.
Step 2: DC	$DC \cong \frac{V_{OUT}+0.5V}{V_{IN}+V_{OUT}+0.5V-0.3V}$
Step 3: L	$L_{TYP} = \frac{(V_{IN}-0.3V)\bullet DC}{f_{OSC}\bullet 1A}$ (1) $L_{MIN} = \frac{(V_{IN}-0.3V)\bullet(2\bullet DC-1)}{2.2A\bullet f_{OSC}\bullet(1-DC)}$ (2) $L_{MAX} = \frac{(V_{IN}-0.3V)\bullet DC}{f_{OSC}\bullet 0.35A}$ (3) • Pick L out of a range of inductor values where the minimum value of the range is set by L_{TYP} or L_{MIN}, whichever is higher. The maximum value of the range is set by L_{MAX}. See Appendix on how to choose current rating for inductor value chosen. • Pick L1 = L2 = L for coupled inductors. • Pick L1 || L2 = L for un-coupled inductors.
Step 4: I_{RIPPLE}	$I_{RIPPLE} = \frac{(V_{IN}-0.3V)\bullet DC}{f_{OSC}\bullet L}$ • L = L1 = L2 for coupled inductors. • L = L1 || L2 for un-coupled inductors.
Step 5: I_{OUT}	$I_{OUT} = \left(3.3A - \frac{I_{RIPPLE}}{2}\right)\bullet(1-DC)$
Step 6: D1	$V_R > V_{IN}+V_{OUT}$; $I_{AVG} > I_{OUT}$
Step 7: C1	$C1 \geq 1\mu F$; $V_{RATING} \geq V_{IN}$
Step 8: C_{OUT}	$C_{OUT} \geq \frac{I_{OUT}\bullet DC}{f_{OSC}\bullet 0.005\bullet V_{OUT}}$
Step 9: C_{IN}	$C_{IN} \geq C_{VIN}+C_{PWR} \geq \frac{3.3A\bullet DC}{45\bullet f_{OSC}\bullet 0.005\bullet V_{IN}} + \frac{I_{RIPPLE}}{8\bullet f_{OSC}\bullet 0.005\bullet V_{IN}}$ • Refer to Input Capacitor Selection in Appendix for definition of C_{VIN} and C_{PWR}.
Step 10: R_{FB}	$R_{FB} = \frac{V_{OUT}-1.215V}{83.3\mu A}$
Step 11: R_T	$R_T = \frac{87.6}{f_{OSC}} - 1$; f_{OSC} in MHz and R_T in kΩ

Note 1: The maximum design target for peak switch current is 3.3A and is used in this table.

Note 2: The final values for C_{OUT}, C_{IN} and C1 may deviate from the above equations in order to obtain desired load transient performance.

APPLICATIONS INFORMATION

DUAL INDUCTOR INVERTING CONVERTER COMPONENT SELECTION (COUPLED OR UN-COUPLED INDUCTORS)

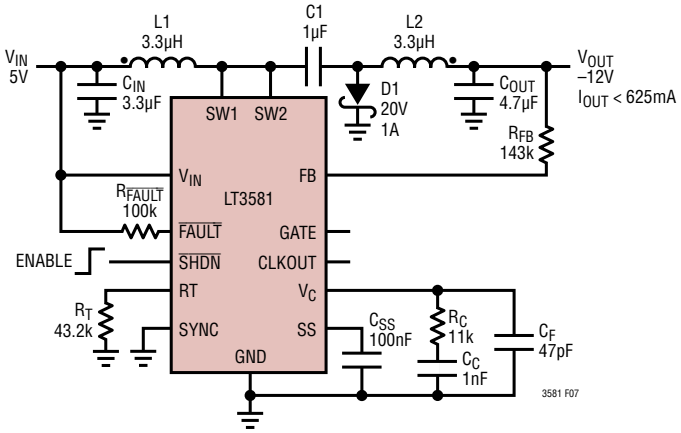


Figure 7. Dual Inductor Inverting Converter – The Component Values and Voltages Given Are Typical Values for a 2MHz, 5V to –12V Inverting Topology Using Coupled Inductors

Due to its unique FB pin, the LT3581 can work in a Dual Inductor Inverting configuration as in Figure 7. Changing the connections of L2 and the Schottky diode in the SEPIC topology results in generating negative output voltages. This solution results in very low output voltage ripple due to inductor L2 being in series with the output. Output disconnect is inherently built into this topology due to the capacitor C1.

Table 3 is a step-by-step set of equations to calculate component values for the LT3581 when operating as a dual inductor inverting converter. Input parameters are input and output voltage, and switching frequency (V_{IN}, V_{OUT} and f_{OSC} respectively). Refer to the Appendix for further information on the design equations presented in Table 3.

Variable Definitions:

V_{IN} = Input Voltage
V_{OUT} = Output Voltage
DC = Power Switch Duty Cycle
f_{OSC} = Switching Frequency
I_{OUT} = Maximum Average Output Current
I_{RIPPLE} = Inductor Ripple Current

Table 3. Dual Inductor Inverting Design Equations

	PARAMETERS/EQUATIONS
Step 1: Inputs	Pick V_{IN}, V_{OUT}, and f_{OSC} to calculate equations below.
Step 2: DC	$DC \cong \frac{\lvert V_{OUT}\rvert + 0.5V}{V_{IN} + \lvert V_{OUT}\rvert + 0.5V - 0.3V}$
Step 3: L	$L_{TYP} = \frac{(V_{IN} - 0.3V) \bullet DC}{f_{OSC} \bullet 1A}$ (1) $L_{MIN} = \frac{(V_{IN} - 0.3V) \bullet (2 \bullet DC - 1)}{2.2A \bullet f_{OSC} \bullet (1 - DC)}$ (2) $L_{MAX} = \frac{(V_{IN} - 0.3V) \bullet DC}{f_{OSC} \bullet 0.35A}$ (3) • Pick L out of a range of inductor values where the minimum value of the range is set by L_{TYP} or L_{MIN}, whichever is higher. The maximum value of the range is set by L_{MAX}. See Appendix on how to choose current rating for inductor value chosen. • Pick L1 = L2 = L for coupled inductors. • Pick L1 || L2 = L for un-coupled inductors.
Step 4: I_{RIPPLE}	$I_{RIPPLE} = \frac{(V_{IN} - 0.3V) \bullet DC}{f_{OSC} \bullet L}$ • L = L1 = L2 for coupled inductors. • L = L1 || L2 for un-coupled inductors.
Step 5: I_{OUT}	$I_{OUT} = \left(3.3A - \frac{I_{RIPPLE}}{2}\right) \bullet (1 - DC)$
Step 6: D1	$V_R > V_{IN} + \lvert V_{OUT}\rvert$; $I_{AVG} > I_{OUT}$
Step 7: C1	$C1 \geq 1\mu F$; $V_{RATING} \geq V_{IN} + \lvert V_{OUT}\rvert$
Step 8: C_{OUT}	$C_{OUT} \geq \frac{I_{RIPPLE}}{8 \bullet f_{OSC} (0.005 \bullet \lvert V_{OUT}\rvert)}$
Step 9: C_{IN}	$C_{IN} \geq C_{VIN} + C_{PWR} \geq \frac{3.3A \bullet DC}{45 \bullet f_{OSC} \bullet 0.005 \bullet V_{IN}} + \frac{I_{RIPPLE}}{8 \bullet f_{OSC} \bullet 0.005 \bullet V_{IN}}$ • Refer to Input Capacitor Selection in Appendix for definition of C_{VIN} and C_{PWR}.
Step 10: R_{FB}	$R_{FB} = \frac{\lvert V_{OUT}\rvert + 5mV}{83.3\mu A}$
Step 11: R_T	$R_T = \frac{87.6}{f_{OSC}} - 1$; f_{OSC} in MHz and R_T in kΩ

Note 1: The maximum design target for peak switch current is 3.3A and is used in this table.

Note 2: The final values for C_{OUT}, C_{IN} and C1 may deviate from the above equations in order to obtain desired load transient performance.

APPLICATIONS INFORMATION

LAYOUT GUIDELINES FOR BOOST, SEPIC, AND DUAL INDUCTOR INVERTING TOPOLOGIES

General Layout Guidelines

- To optimize thermal performance, solder the exposed ground pad of the LT3581 to the ground plane, with multiple vias around the pad connecting to additional ground planes.
- A ground plane should be used under the switcher circuitry to prevent interplane coupling and overall noise.
- High speed switching path (see specific topology for more information) must be kept as short as possible.
- The V_C, FB, and RT components should be placed as close to the LT3581 as possible, while being as far away as practically possible from the switch node. The ground for these components should be separated from the switch current path.
- Place the bypass capacitor for the V_{IN} pin as close as possible to the LT3581.
- Place the bypass capacitor for the inductor as close as possible to the inductor.
- The load should connect directly to the positive and negative terminals of the output capacitor for best load regulation.

Boost Topology Specific Layout Guidelines

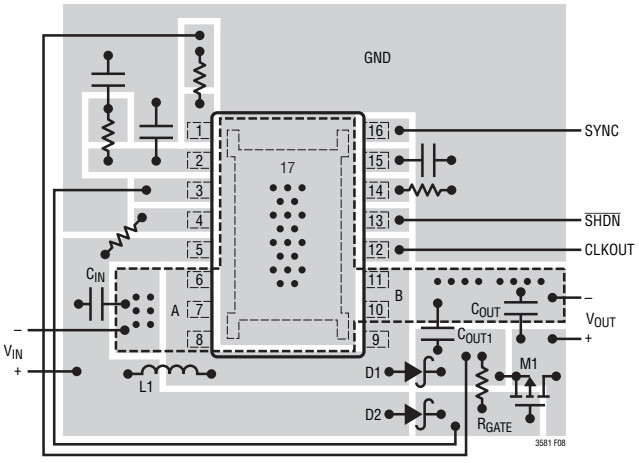
- Keep length of loop (high speed switching path) governing switch, diode D1, output capacitor C_{OUT1}, and ground return as short as possible to minimize parasitic inductive spikes at the switch node during switching.

SEPIC Topology Specific Layout Guidelines

- Keep length of loop (high speed switching path) governing switch, flying capacitor C1, diode D1, output capacitor C_{OUT}, and ground return as short as possible to minimize parasitic inductive spikes at the switch node during switching.

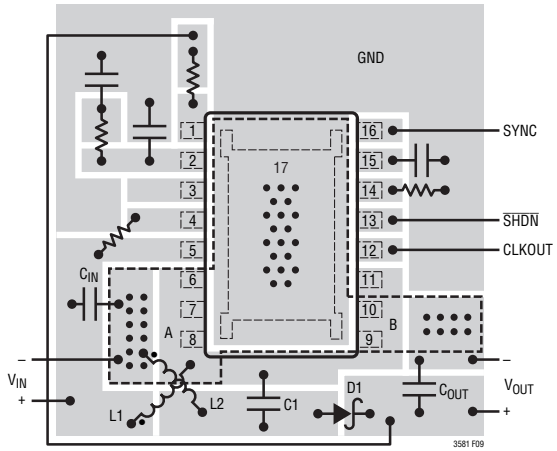
Inverting Topology Specific Layout Guidelines

- Keep ground return path from the cathode of D1 (to chip) separated from output capacitor C_{OUT}'s ground return path (to chip) in order to minimize switching noise coupling into the output.
- Keep length of loop (high speed switching path) governing switch, flying capacitor C1, diode D1, and ground return as short as possible to minimize parasitic inductive spikes at the switch node during switching.



A: RETURN C_{IN} GROUND DIRECTLY TO LT3581 EXPOSED PAD PIN 17. IT IS ADVISED TO NOT COMBINE C_{IN} GROUND WITH GND EXCEPT AT THE EXPOSED PAD.
B: RETURN C_{OUT} AND C_{OUT1} GROUND DIRECTLY TO LT3581 EXPOSED PAD PIN 17. IT IS ADVISED TO NOT COMBINE C_{OUT} AND C_{OUT1} GROUND WITH GND EXCEPT AT THE EXPOSED PAD.

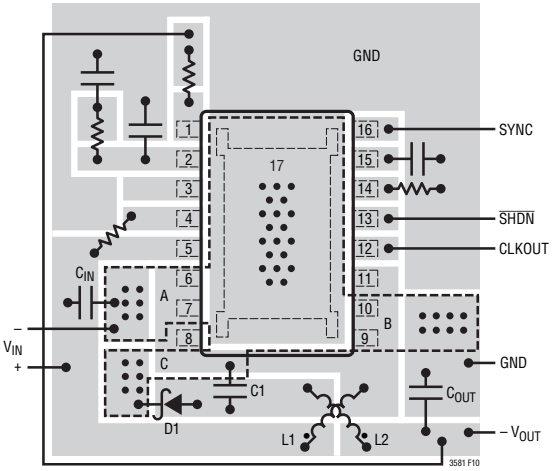
Figure 8. Suggested Component Placement for Boost Topology (MSOP Shown, DFN Similar, Not to Scale.) Pin 15 on DFN or Pin 17 on MSOP Is the Exposed Pad Which Must Be Soldered Directly to the Local Ground Plane for Adequate Thermal Performance. Multiple Vias to Additional Ground Planes Will Improve Thermal Performance



A: RETURN C_{IN} AND L2 GROUND DIRECTLY TO LT3581 EXPOSED PAD PIN 17. IT IS ADVISED TO NOT COMBINE C_{IN} AND L2 GROUND WITH GND EXCEPT AT THE EXPOSED PAD.
B: RETURN C_{OUT} GROUNDS DIRECTLY TO LT3581 EXPOSED PAD PIN 17. IT IS ADVISED TO NOT COMBINE C_{OUT} GROUND WITH GND EXCEPT AT THE EXPOSED PAD.
L1, L2: MOST COUPLED INDUCTOR MANUFACTURERS USE CROSS PINOUT FOR IMPROVED PERFORMANCE.

Figure 9. Suggested Component Placement for SEPIC Topology (MSOP Shown, DFN Similar, Not to Scale.) Pin 15 on DFN or Pin 17 on MSOP Is the Exposed Pad Which Must Be Soldered Directly to the Local Ground Plane for Adequate Thermal Performance. Multiple Vias to Additional Ground Planes Will Improve Thermal Performance

APPLICATIONS INFORMATION



A: RETURN C_{IN} GROUND DIRECTLY TO LT3581 EXPOSED PAD PIN 17. IT IS ADVISED TO NOT COMBINE C_{IN} GROUND WITH GND EXCEPT AT THE EXPOSED PAD.
B: RETURN C_{OUT} GROUND DIRECTLY TO LT3581 EXPOSED PAD PIN 17. IT IS ADVISED TO NOT COMBINE C_{OUT} GROUND WITH GND EXCEPT AT THE EXPOSED PAD.
C: RETURN D1 GROUND DIRECTLY TO LT3581 EXPOSED PAD PIN 17. IT IS ADVISED TO NOT COMBINE D1 GROUND WITH GND EXCEPT AT THE EXPOSED PAD.
L1, L2: MOST COUPLED INDUCTOR MANUFACTURERS USE CROSS PINOUT FOR IMPROVED PERFORMANCE.

Figure 10. Suggested Component Placement for Dual Inductor Inverting Topology (MSOP Shown, DFN Similar, Not to Scale.) Pin 15 on DFN or Pin 17 on MSOP Is the Exposed Pad Which Must Be Soldered Directly to the Local Ground Plane for Adequate Thermal Performance. Multiple Vias to Additional Ground Planes Will Improve Thermal Performance

THERMAL CONSIDERATIONS

Overview

For the LT3581 to deliver its full output power, it is imperative that a good thermal path be provided to dissipate the heat generated within the package. This can be accomplished by taking advantage of the thermal pad on the underside of the IC. It is recommended that multiple vias in the printed circuit board be used to conduct heat away from the IC and into a copper plane with as much area as possible.

Power and Thermal Calculations

Power dissipation in the LT3581 chip comes from four primary sources: switch I^2R losses, switch dynamic losses, NPN base drive DC losses, and miscellaneous input current losses. These formulas assume continuous mode operation, so they should not be used for calculating thermal losses or efficiency in discontinuous mode or at light load currents.

The following example calculates the power dissipation in the LT3581 for a particular boost application (V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 0.83A, f_{OSC} = 2MHz, V_D = 0.45V, V_{CESAT} = 0.21V).

To calculate die junction temperature, use the appropriate thermal resistance number and add in worst-case ambient temperature:

$$T_J = T_A + \theta_{JA} \bullet P_{TOTAL}$$

Table 4. Power Calculations Example for Boost Converter with V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 0.83A, f_{OSC} = 2MHz, V_D = 0.45V, V_{CESAT} = 0.21V

DEFINITION OF VARIABLES	EQUATIONS	DESIGN EXAMPLE	VALUE
DC = SWITCH DUTY CYCLE	$DC = \frac{V_{OUT} - V_{IN} + V_D}{V_{OUT} + V_D - V_{CESAT}}$	$DC = \frac{12V - 5V + 0.45V}{12V + 0.45V - 0.21V}$	DC = 60.9%
I_{IN} = Average Switch Current η = Power Conversion Efficiency (typically 88% at high currents)	$I_{IN} = \frac{V_{OUT} \bullet I_{OUT}}{V_{IN} \bullet \eta}$	$I_{IN} = \frac{12V \bullet 0.83A}{5V \bullet 0.88}$	I_{IN} = 2.3A
P_{SWDC} = Switch I^2R Loss (DC) R_{SW} = Switch Resistance (typically 90mΩ combined SW1 and SW2)	$P_{SWDC} = DC \bullet I_{IN}^2 \bullet R_{SW}$	$P_{SWDC} = 0.609 \bullet (2.3A)^2 \bullet 90m\Omega$	P_{SWDC} = 290mW
P_{SWAC} = Switch Dynamic Loss (AC)	$P_{SWAC} = 13ns \bullet I_{IN} \bullet V_{OUT} \bullet f_{OSC}$	$P_{SWAC} = (13ns) \bullet 2.3A \bullet 12V \bullet (2MHz)$	P_{SWAC} = 718mW
P_{BDC} = Base Drive Loss (DC)	$P_{BDC} = \frac{V_{IN} \bullet I_{IN} \bullet DC}{45}$	$P_{BDC} = \frac{5V \bullet 2.3A \bullet 0.609}{45}$	P_{BDC} = 156mW
P_{INP} = Input Power Loss	$P_{INP} = 9mA \bullet V_{IN}$	$P_{INP} = 9mA \bullet 5V$	P_{INP} = 45mW
			P_{TOTAL} = 1.209W

APPLICATIONS INFORMATION

where T_J = Die Junction Temperature, T_A = Ambient Temperature, P_{TOTAL} is the final result from the calculations shown in Table 4, and θ_{JA} is the thermal resistance from the silicon junction to the ambient air.

The published (http://www.linear.com/designtools/packaging/Linear_Technology_Thermal_Resistance_Table.pdf) θ_{JA} value is 43°C/W for the 4mm × 3mm 14-pin DFN package and 45°C/W for the 16-lead MSOP package. In practice, lower θ_{JA} values are realizable if board layout is performed with appropriate grounding (accounting for heat sinking properties of the board) and other considerations listed in the Layout Guidelines section. For instance, a θ_{JA} value of ~24°C/W was consistently achieved for both MSE and DFN packages of the LT3581 (at V_{IN} = 5V, V_{OUT} = 12V, I_{OUT} = 0.83A, f_{OSC} = 2MHz) when board layout was optimized as per the suggestions in the Board Layout Guidelines section.

Junction Temperature Measurement

The duty cycle of the CLKOUT signal is linearly proportional to die junction temperature, T_J. To get a temperature reading, measure the duty cycle of the CLKOUT signal and use the following equation to approximate the junction temperature:

$$T_J = \frac{DC_{CLKOUT} - 35\%}{0.3\%}$$

where DC_{CLKOUT} is the CLKOUT duty cycle in % and T_J is the die junction temperature in °C. Although the actual die temperature can deviate from the above equation by ±15°C, the relationship between change in CLKOUT duty cycle and change in die temperature is well defined. Basically a 1% change in CLKOUT duty cycle corresponds to a 3.33°C change in die temperature. Note that the CLKOUT pin is only meant to drive capacitive loads up to 50pF.

Thermal Lockout

A fault condition occurs when the die temperature exceeds 165°C (see Operation Section), and the part goes into thermal lockout. The fault condition ceases when the die temperature drops by ~5°C (nominal).

SWITCHING FREQUENCY

There are several considerations in selecting the operating frequency of the converter. The first is staying clear of sensitive frequency bands, which cannot tolerate any spectral noise. For example, in products incorporating RF communications, the 455kHz IF frequency is sensitive to any noise, therefore switching above 600kHz is desired. Some communications have sensitivity to 1.1MHz and in that case a 1.5MHz switching converter frequency may be employed. The second consideration is the physical size of the converter. As the operating frequency goes up, the inductor and filter capacitors go down in value and size. The tradeoff is efficiency, since the losses due to switching dynamics (see Thermal Considerations), Schottky diode charge, and other capacitive loss terms increase proportionally with frequency.

Oscillator Timing Resistor (R_T)

The operating frequency of the LT3581 can be set by the internal free-running oscillator. When the SYNC pin is driven low (< 0.4V), the frequency of operation is set by a resistor from the R_T pin to ground. An internally trimmed timing capacitor resides inside the IC. The oscillator frequency is calculated using the following formula:

$$f_{OSC} = \frac{87.6}{R_T + 1}$$

where f_{OSC} is in MHz and R_T is in k. Conversely, R_T (in k) can be calculated from the desired frequency (in MHz) using:

$$R_T = \frac{87.6}{f_{OSC}} - 1$$

APPLICATIONS INFORMATION

Clock Synchronization

The operating frequency of the LT3581 can be set by an external source by simply providing a digital clock signal into the SYNC pin (R_T resistor still required). The LT3581 will revert to its internal free-running oscillator clock (set by the R_T resistor) when the SYNC pin is driven below 0.4V for a few free-running clock periods.

Driving SYNC high for an extended period of time effectively stops the operating clock and prevents latch SR1 from becoming set (see Block Diagram). As a result, the switching operation of the LT3581 will stop and the CLKOUT pin will be held at ground.

The duty cycle of the SYNC signal must be between 20% and 80% for proper operation. Also, the frequency of the SYNC signal must meet the following two criteria:

(1) SYNC may not toggle outside the frequency range of 200kHz to 2.5MHz unless it is stopped low (below 0.4V) to enable the free-running oscillator.

(2) The SYNC frequency can always be higher than the free-running oscillator frequency (as set by the R_T resistor), f_{OSC}, but should not be less than 25% below f_{OSC}.

CLOCK SYNCHRONIZATION OF ADDITIONAL REGULATORS

The CLKOUT pin of the LT3581 can be used to synchronize one or more other compatible switching regulator ICs as shown in Figure 11.

The frequency of the master LT3581 is set by the external R_T resistor. The SYNC pin of the slave LT3581 is driven by the CLKOUT pin of the master LT3581. Note that the RT pin of the slave LT3581 must have a resistor tied to ground. It takes a few clock cycles for the CLKOUT signal to begin oscillating, and it's preferable for all LT3581s to have the same internal free-running frequency. Therefore, in general, use the same value R_T resistor for all of the synchronized LT3581s.

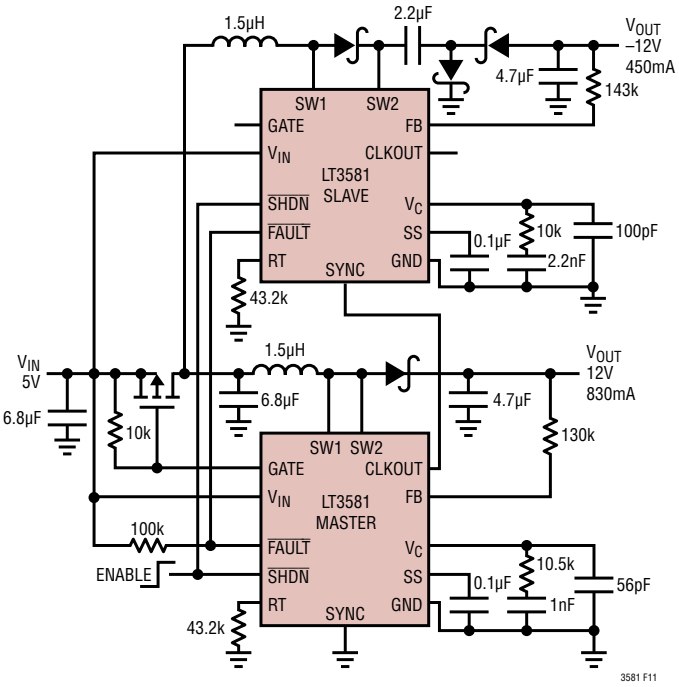


Figure 11. A Single Inductor Inverting Topology Is Synchronized with a Boost Regulator to Generate –12V and 12V Outputs. The External PMOS Helps Disconnect the Input from the Power Paths During Fault Events

Also, the $\overline{FAULT}$ pins can be tied together so that a fault condition from one LT3581 causes all of the LT3581s to enter fault, until the fault condition disappears.

CHARGE PUMP AIDED REGULATORS

Designing charge pumps with the LT3581 can offer efficient solutions with fewer components than traditional circuits because of the master/slave switch configuration on the IC. Although the slave switch, SW2, operates in phase with the master switch, SW1, it is only the current through the master switch (SW1) that is sensed by the current comparator (A4 in Block Diagram) as part of the current feedback loop. This method of operation by the master/slave switches can offer the following benefits to charge pump designs:

APPLICATIONS INFORMATION

- The slave switch, by not performing a current sense operation like the master switch, can sustain fairly large current spikes when the flying capacitors charge up. Since this current spike flows through SW2, it does not affect the operation of the current comparator (A4 in Block Diagram).
- The master switch, immune from the capacitor current spike (seen only by the slave switch) can sense the inductor current more accurately.
- Since the slave switch can sustain large current spikes, the diodes that feed current into the flying capacitors do not need current limiting resistors, leading to efficiency and thermal improvements.

High V_{OUT} Charge Pump Topology

The LT3581 can be used in a charge-pump topology as shown in Figure 12, multiplying the output of an inductive boost converter. The master switch (SW1) can be used to drive the inductive boost converter (first stage of charge pump), while the slave switch (SW2) can be used to drive one or more other charge pump stages. This topology is useful for high voltage applications including VFD bias supplies.

Single Inductor Inverting Topology

If there is a need to use just one inductor to generate a negative output voltage whose magnitude is greater than V_{IN}, the single inductor inverting topology (shown in Figure 13) can be used. Since the master and slave switches are isolated by a Schottky diode, the current spike through C1 will flow only through the slave switch, thereby preventing the current comparator, (A4 in the Block Diagram), from falsely tripping. Output disconnect is inherently built into the single inductor topology.

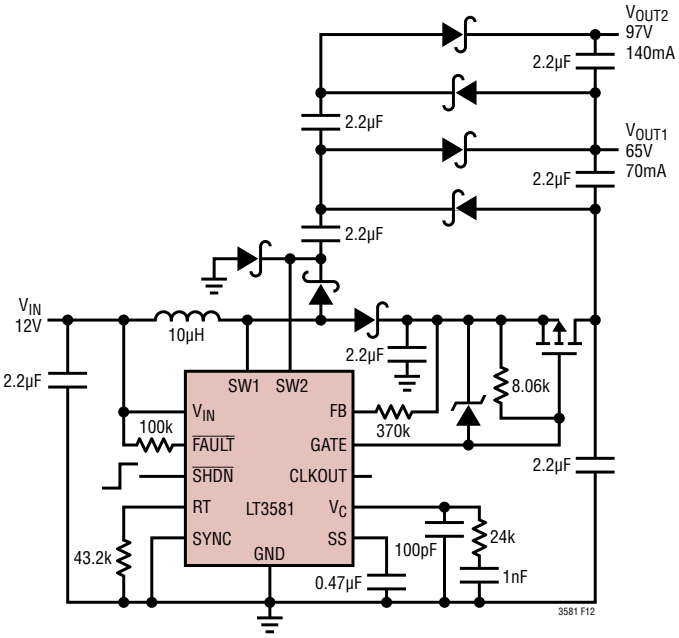


Figure 12. High V_{OUT} Charge Pump Topology Can Be Used to Build VFD Bias Supplies

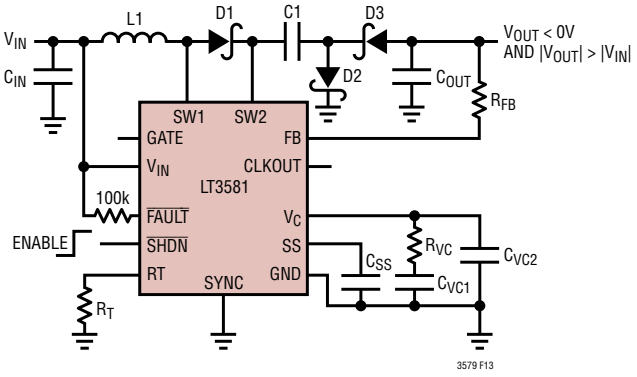


Figure 13. Single Inductor Inverting Topology

APPLICATIONS INFORMATION

HOT-PLUG

The high inrush current associated with hot-plugging V_{IN} can be largely rejected with the use of an external PMOS. A simple hot-plug controller can be designed by connecting an external PMOS in series with V_{IN}, with the gate of the PMOS being driven by the GATE pin of the LT3581. Since the GATE pin pull-down current is linearly proportional to the SS voltage, and the SS charge up time is relatively slow, the GATE pin pull-down current will increase gradually, thereby turning on the external PMOS slowly. Controlled in this manner, the PMOS acts as an input current limiter when V_{IN} hot-plugs or ramps up sharply.

Likewise, when the PMOS is connected in series with the output, inrush currents into the output capacitor can be limited during a hot-plug event. To illustrate this, the circuit in Figure 18 was re-configured by adding a large 1500µF capacitor to the output. An 18Ω resistive load was used and a 2.2µF capacitor was placed on SS. Figure 14 shows the results of hot-plugging this re-configured circuit. Notice how the inductor current is well behaved.

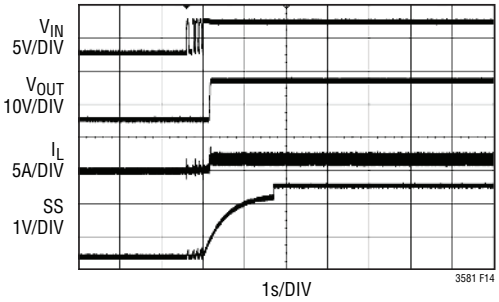


Figure 14. Inrush Current Is Well Controlled in Spite Of Hot-Plugging the Re-configured Boost Converter in Figure 18

APPENDIX

SETTING THE OUTPUT VOLTAGE

The output voltage is set by connecting a resistor (R_{FB}) from V_{OUT} to the FB pin. R_{FB} is determined by using the following equation:

$$R_{FB} = \frac{|V_{OUT} - V_{FB}|}{83.3\mu A}$$

where V_{FB} is 1.215V (typical) for non-inverting topologies (i.e. boost and SEPIC regulators) and 5mV (typical) for inverting topologies.

POWER SWITCH DUTY CYCLE

In order to maintain loop stability and deliver adequate current to the load, the power NPNs (Q1 and Q2 in the Block Diagram) cannot remain "on" for 100% of each clock cycle. The maximum allowable duty cycle is given by:

$$DC_{MAX} = \frac{(T_P - MinOffTime)}{T_P} \bullet 100\%$$

where T_P is the clock period and MinOffTime (found in the Electrical Characteristics) is typically 60ns.

Conversely, the power NPNs (Q1 and Q2 in the Block Diagram) cannot remain "off" for 100% of each clock cycle, and will turn on for a minimum on time (MinOnTime) when in regulation. This MinOnTime governs the minimum allowable duty cycle given by:

$$DC_{MIN} = \frac{(MinOnTime)}{T_P} \bullet 100\%$$

Where T_P is the clock period and MinOnTime (found in the Electrical Characteristics) is typically 100ns.

The application should be designed such that the operating duty cycle is between DC_{MIN} and DC_{MAX}.

Duty cycle equations for several common topologies are given below where V_D is the diode forward voltage drop and V_{CESAT} is the collector to emitter saturation voltage of the switch. V_{CESAT}, with SW1 and SW2 tied together, is typically 250mV when the combined switch current ($I_{SW1} + I_{SW2}$) is 2.75A.

For the boost topology (see Figure 5):

$$DC_{BOOST} \cong \frac{V_{OUT} - V_{IN} + V_D}{V_{OUT} + V_D - V_{CESAT}}$$

For the SEPIC or Dual Inductor Inverting topology (see Figures 6 and 7):

$$DC_{SEPIC\_\&\_INVERT} \cong \frac{V_D + |V_{OUT}|}{V_{IN} + |V_{OUT}| + V_D - V_{CESAT}}$$

For the Single Inductor Inverting topology (see Figure 13):

$$DC_{SI\_INVERT} = \frac{|V_{OUT}| - V_{IN} + V_{CESAT} + 3 \bullet V_D}{|V_{OUT}| + 3 \bullet V_D}$$

The LT3581 can be used in configurations where the duty cycle is higher than DC_{MAX}, but it must be operated in the discontinuous conduction mode so that the effective duty cycle is reduced.

INDUCTOR SELECTION

General Guidelines: The high frequency operation of the LT3581 allows for the use of small surface mount inductors. For high efficiency, choose inductors with high frequency core material, such as ferrite, to reduce core losses. Also to improve efficiency, choose inductors with more volume for a given inductance. The inductor should have low DCR (copper-wire resistance) to reduce I^2R losses, and must be able to handle the peak inductor current without saturating. Note that in some applications, the current handling requirements of the inductor can be lower, such as in the SEPIC topology where each inductor only carries one half of the total switch current. Molded chokes or chip inductors usually do not have enough core area to support peak inductor currents in the 2A to 6A range. To minimize radiated noise, use a toroidal or shielded inductor. See Table 5 for a list of inductor manufacturers.

Table 5. Inductor Manufacturers

Sumida	CDR6D28MN and CDR7D28MN Series	www.sumida.com
Coilcraft	MSD7342 Series	www.coilcraft.com
Vishay	IHLP-1616BZ-01, IHLP-2020BZ-01 and IHLP-2525CZ-01 Series	www.vishay.com
Taiyo Yuden	NR Series	www.t-yuden.com
Wurth	WE-PD Series	www.we-online.com
TDK	VLF, SLF and RLF Series	www.tdk.com

APPENDIX

Minimum Inductance

Although there can be a tradeoff with efficiency, it is often desirable to minimize board space by choosing smaller inductors. When choosing an inductor, there are three conditions that limit the minimum inductance: (1) providing adequate load current, (2) avoidance of subharmonic oscillations and (3) supplying a minimum ripple current to avoid false tripping of the current comparator.

Adequate Load Current

Small value inductors result in increased ripple currents and thus, due to the limited peak switch current, decrease the average current that can be provided to the load. In order to provide adequate load current, L should be at least:

$$L_{BOOST} > \frac{DC \bullet (V_{IN} - V_{CESAT})}{2 \bullet f_{OSC} \bullet \left(I_{PK} - \frac{|V_{OUT}| \bullet I_{OUT}}{V_{IN} \bullet \eta}\right)} \quad \text{Boost Topology}$$

or

$$L_{DUAL} > \frac{DC \bullet (V_{IN} - V_{CESAT})}{2 \bullet f_{OSC} \bullet \left(I_{PK} - \frac{|V_{OUT}| \bullet I_{OUT}}{V_{IN} \bullet \eta} - I_{OUT}\right)} \quad \text{SEPIC or Inverting Topologies}$$

where:

L_{BOOST} = L_1 for Boost Topologies (see Figure 5)
L_{DUAL} = $L_1 = L_2$ for Coupled Dual Inductor Topologies (see Figures 6 and 7)
L_{DUAL} = $L_1 \,||\, L_2$ for Uncoupled Dual Inductor Topologies (see Figures 6 and 7)
DC = Switch Duty Cycle (see Power Switch Duty Cycle section in Appendix)
I_{PK} = Maximum Peak Switch Current; should not exceed 3.3A for a combined SW1 + SW2 current, or 1.9A of SW1 current if SW1 is being used by itself.
η = Power Conversion Efficiency (typically 88% for Boost and 75% for Dual Inductor Topologies at High Currents)
f_{OSC} = Switching Frequency
I_{OUT} = Maximum Output Current

Negative values of L_{BOOST} or L_{DUAL} indicate that the output load current, I_{OUT}, exceeds the switch current limit capability of the LT3581.

Avoiding Sub-Harmonic Oscillations

The LT3581's internal slope compensation circuit will prevent sub-harmonic oscillations that can occur when the duty cycle is greater than 50%, provided that the inductance exceeds a certain minimum value. In applications that operate with duty cycles greater than 50%, the inductance must be at least:

$$L_{MIN} = \frac{(V_{IN} - V_{CESAT}) \bullet (2 \bullet DC - 1)}{2.2A \bullet f_{OSC} \bullet (1 - DC)}$$

where:

L_{MIN} = L_1 for Boost Topologies (see Figure 5)
L_{MIN} = $L_1 = L_2$ for Coupled Dual Inductor Topologies (see Figures 6 and 7)
L_{MIN} = $L_1 \,||\, L_2$ for Uncoupled Dual Inductor Topologies (see Figures 6 and 7)

Maximum Inductance

Excessive inductance can reduce ripple current to levels that are difficult for the current comparator (A4 in the Block Diagram) to cleanly discriminate, causing duty cycle jitter and/or poor regulation. The maximum inductance can be calculated by:

$$L_{MAX} = \frac{V_{IN} - V_{CESAT}}{350mA} \bullet \frac{DC}{f_{OSC}}$$

where:

L_{MAX} = L_1 for Boost Topologies (see Figure 5)
L_{MAX} = $L_1 = L_2$ for Coupled Dual Inductor Topologies (see Figures 6 and 7)
L_{MAX} = $L_1 \,||\, L_2$ for Uncoupled Dual Inductor Topologies (see Figures 6 and 7)

APPENDIX

Inductor Current Rating

Inductors must have a rating greater than their peak operating current, or else they could saturate and hence contribute to losses in efficiency. The maximum inductor current (considering start-up and steady-state conditions) is given by:

$$I_{L\_PEAK} = I_{LIM} + \frac{V_{IN} \bullet T_{MIN\_PROP}}{L}$$

where:

I_{L_PEAK} = Peak Inductor Current in L_1 for a Boost Topology, or the Peak of the sum of the Inductor Currents in L1 and L2 for Dual Inductor Topologies.

I_{LIM}** = 3.3A with SW1 and SW2 Tied Together, or 1.9A with just SW1 (This assumes usage of an inductor whose core material soft-saturates such as powdered iron core).

T_{MIN_PROP} = 100ns (Propagation Delay through the Current Feedback Loop).

**If using an inductor whose core material saturates hard (e.g., ferrite), then pick I_{LIM} to be 5.4A with SW1 and SW2 tied together, or 3A when just SW1 is used.

Note that these equations offer conservative results for the required inductor current ratings. The current ratings could be lower for applications with light loads, if the SS capacitor is sized appropriately to limit inductor currents at start-up.

DIODE SELECTION

Schottky diodes, with their low forward voltage drops and fast switching speeds, are recommended for use with the LT3581. Choose a Schottky diode with low parasitic capacitance to reduce reverse current spikes through the power switch of the LT3581. The Central Semiconductor Corp. CMMSH2-40 diode is a very good choice with a 40V reverse voltage rating and an average forward current of 2A.

OUTPUT CAPACITOR SELECTION

Low ESR (equivalent series resistance) capacitors should be used at the output to minimize the output ripple voltage. Multilayer ceramic capacitors are an excellent choice, as they have extremely low ESR and are available in very small packages. X5R or X7R dielectrics are preferred, as these materials retain their capacitance over wide voltage and temperature ranges. A 10µF to 22µF output capacitor is sufficient for most applications, but systems with very low output currents may need only 2.2µF to 10µF. Always use a capacitor with a sufficient voltage rating. Many ceramic capacitors, particularly 0805 or 0603 case sizes, have greatly reduced capacitance at the desired output voltage. Tantalum Polymer or OS-CON capacitors can be used, but it is likely that these capacitors will occupy more board area than a ceramic, and will have higher ESR with greater output ripple.

INPUT CAPACITOR SELECTION

Ceramic capacitors make a good choice for the input decoupling capacitor, and should be placed such that it is in close proximity to the V_{IN} of the chip as well as to the inductor connected to the input of the power path. If it is not possible to optimally place a single input capacitor, then use two separate capacitors—use one at the V_{IN} of the chip (see equation for C_{VIN} in Tables 1, 2 and 3) and one at the input to the power path (see equation for C_{PWR} in Tables 1, 2 and 3) A 4.7µF to 20µF input capacitor is sufficient for most applications.

Table 6 shows a list of several ceramic capacitor manufacturers. Consult the manufacturers for detailed information on their entire selection of ceramic parts.

Table 6: Ceramic Capacitor Manufacturers

AVX	www.avxcorp.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com

PMOS SELECTION

An external PMOS, controlled by the LT3581's GATE pin, can be used to facilitate input or output disconnect. The GATE pin turns on the PMOS gradually during start-up (see Soft-Start of External PMOS in the Operation section), and turns the PMOS off when the LT3581 is in shutdown or in fault.

APPENDIX

The use of the external PMOS, controlled by the GATE pin, is particularly beneficial when dealing with unintended output shorts in a boost regulator. In a conventional boost regulator, the inductor, Schottky diode, and power switches are susceptible to damage in the event of an output short to ground. Using an external PMOS in the boost regulator's power path (path from V_{IN} to V_{OUT}) controlled by the GATE pin, will serve to disconnect the input from the output when the output has a short to ground, thereby helping save the IC, and the other components in the power path from damage. Ensure that both, the diode and the inductor can survive low duty cycle current pulses of 3 to 4 times their steady state levels.

The PMOS chosen must be capable of handling the maximum input or output current depending on whether the PMOS is used at the input (see Figure 11) or the output (see Figure 18).

Ensure that the PMOS is biased with enough source to gate voltage (V_{SG}) to enhance the device into the triode mode of operation. The higher the V_{SG} voltage that biases the PMOS into triode, the lower the R_{DSON} of the PMOS, thereby lowering power dissipation in the device during normal operation, as well as improving the efficiency of the application in which the PMOS is used. The following equations show the relationship between R_{GATE} (see Block Diagram) and the desired V_{SG} that the PMOS is biased with:

$$V_{SG} = \begin{cases} V_{IN}\dfrac{R_{GATE}}{R_{GATE}+2k\Omega} \text{ if } V_{GATE} < 2V \\ 933\mu A \bullet R_{GATE} \text{ if } V_{GATE} \geq 2V \end{cases}$$

When using a PMOS, it is advisable to configure the specific application for undervoltage lockout (see the Operations section). The goal is to have V_{IN} get to a certain minimum voltage where the PMOS has sufficient headroom to attain a high enough V_{SG}, which prevents it from entering the saturation mode of operation during start-up.

Figure 18 shows the PMOS connected in series with the output to act as an output disconnect during a fault condition. The Schottky diode from the V_{IN} pin to the GATE pin is optional and helps turn off the PMOS quicker in the event of hard shorts. The resistor divider from V_{IN} to the $\overline{SHDN}$ pin sets a UVLO of 4V for this application.

Connecting the PMOS in series with the output offers certain advantages over connecting it in series with the input:

- Since the load current is always less than the input current for a boost converter, the current rating of the PMOS goes down.
- A PMOS in series with the output can be biased with a higher overdrive voltage than a PMOS used in series with the input, since $V_{OUT} > V_{IN}$. This higher overdrive results in a lower R_{DSON} rating for the PMOS, thereby improving the efficiency of the regulator.

In contrast, an input connected PMOS works as a simple hot-plug controller (covered in more detail in the Hot-Plug section). The input connected PMOS also functions as an inexpensive means of protecting against multiple output shorts in boost applications that synchronize the LT3581 with other compatible ICs (see Figure 11).

Table 7 shows a list of several discrete PMOS manufacturers. Consult the manufacturers for detailed information on their entire selection of PMOS devices.

Table 7. Discrete PMOS Manufacturers

Vishay	www.vishay.com
Fairchild Semiconductor	www.fairchildsemi.com

COMPENSATION – ADJUSTMENT

To compensate the feedback loop of the LT3581, a series resistor-capacitor network in parallel with an optional single capacitor should be connected from the V_C pin to GND. For most applications, choose a series capacitor in the range of 1nF to 10nF with 2.2nF being a good starting value. The optional parallel capacitor should range in value from 47pF to 160pF with 100pF being a good starting value. The compensation resistor, R_C, is usually in the range of 5k to 50k with 10k being a good starting value. A good technique to compensate a new application is to use a 100k potentiometer in place of the series resistor R_C. With the series and parallel capacitors at 2.2nF and 100pF respectively, adjust the potentiometer while observing the transient response and the optimum value for R_C can be

APPENDIX

found. Figures 15a to 15c illustrate this process for the circuit of Figure 18 with a load current stepped between 540mA and 800mA. Figure 15a shows the transient response with R_C equal to 1k. The phase margin is poor as evidenced by the excessive ringing in the output voltage and inductor current. In Figure 15b, the value of R_C is increased to 3k, which results in a more damped response. Figure 15c shows the results when R_C is increased further to 10.5k. The transient response is nicely damped and the compensation procedure is complete.

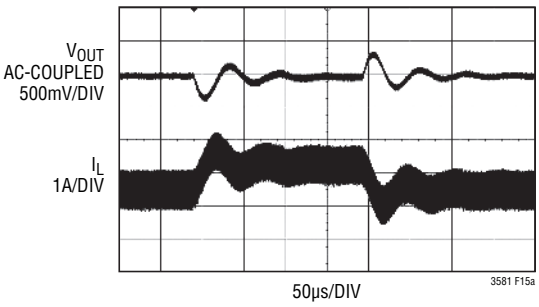


Figure 15a. Transient Response Shows Excessive Ringing

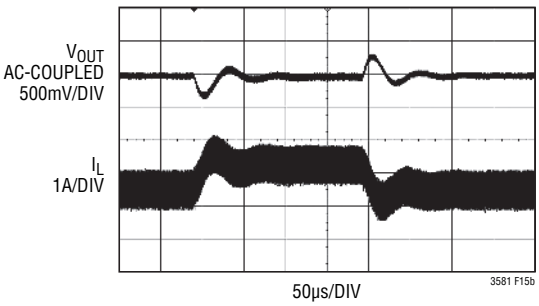


Figure 15b. Transient Response is Better

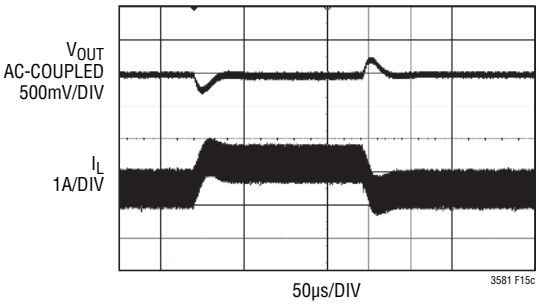


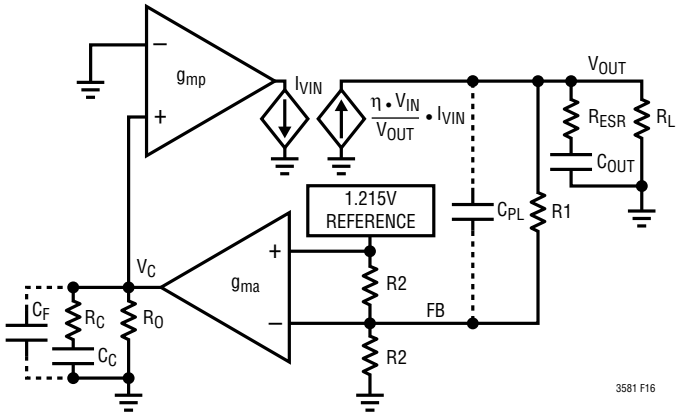
Figure 15c. Transient Response is Well Damped

COMPENSATION – THEORY

Like all other current mode switching regulators, the LT3581 needs to be compensated for stable and efficient operation. Two feedback loops are used in the LT3581: a fast current loop which does not require compensation, and a slower voltage loop which does. Standard Bode plot analysis can be used to understand and adjust the voltage feedback loop.

As with any feedback loop, identifying the gain and phase contribution of the various elements in the loop is critical. Figure 16 shows the key equivalent elements of a boost converter. Because of the fast current control loop, the power stage of the IC, inductor and diode have been replaced by a combination of the equivalent transconductance amplifier g_{mp} and the current controlled current source (which converts I_{VIN} to $\eta V_{IN}/V_{OUT} \bullet I_{VIN}$). g_{mp} acts as a current source where the peak input current, I_{VIN}, is proportional to the V_C voltage. η is the efficiency of the switching regulator and is typically about 80%.

Note that the maximum output currents of the g_{mp} and g_{ma} stages are finite. The output of the g_{mp} stage is limited by the minimum switch current limit (see Electrical Specifications) and the output of the g_{ma} stage is nominally limited to about ±12µA.



C_C: COMPENSATION CAPACITOR
C_{OUT}: OUTPUT CAPACITOR
C_{PL}: PHASE LEAD CAPACITOR
C_F: HIGH FREQUENCY FILTER CAPACITOR
g_{ma}: TRANSCONDUCTOR AMPLIFIER INSIDE IC
g_{mp}: POWER STAGE TRANSCONDUCTANCE AMPLIFIER
R_C: COMPENSATION RESISTOR
R_L: OUTPUT RESISTANCE DEFINED AS $V_{OUT}/I_{LOAD(MAX)}$
R_O: OUTPUT RESISTANCE OF g_{ma}
R1, R2; FEEDBACK RESISTOR DIVIDER NETWORK
R_{ESR}: OUTPUT CAPACITOR ESR

Figure 16. Boost Converter Equivalent Model

APPENDIX

From Figure 16, the DC gain, poles and zeros can be calculated as follows:

DC Gain:

(Breaking loop at FB pin)

$$A_{DC} = A_{OL}(0) = \frac{\partial V_C}{\partial V_{FB}} \bullet \frac{\partial I_{VIN}}{\partial V_C} \bullet \frac{\partial V_{OUT}}{\partial I_{VIN}} \bullet \frac{\partial V_{FB}}{\partial V_{OUT}} =$$

$$\left(g_{ma} \bullet R_O\right) \bullet g_{mp} \bullet \left(\eta \bullet \frac{V_{IN}}{V_{OUT}} \bullet \frac{R_L}{2}\right) \bullet \frac{0.5R_2}{R_1 + 0.5R_2}$$

$$\text{Output Pole: } P1 = \frac{2}{2 \bullet \pi \bullet R_L \bullet C_{OUT}}$$

$$\text{Error Amp Pole: } P2 = \frac{1}{2 \bullet \pi \bullet \left[R_O + R_C\right] \bullet C_C}$$

$$\text{Error Amp Zero: } Z1 = \frac{1}{2 \bullet \pi \bullet R_C \bullet C_C}$$

$$\text{ESR Zero: } Z2 = \frac{1}{2 \bullet \pi \bullet R_{ESR} \bullet C_{OUT}}$$

$$\text{RHP Zero: } Z3 = \frac{V_{IN}^2 \bullet R_L}{2 \bullet \pi \bullet V_{OUT}^2 \bullet L}$$

$$\text{High Frequency Pole: } P3 > \frac{f_S}{3}$$

$$\text{Phase Lead Zero: } Z4 = \frac{1}{2 \bullet \pi \bullet R1 \bullet C_{PL}}$$

$$\text{Phase Lead Pole: } P4 = \frac{1}{2 \bullet \pi \bullet \frac{R1 \bullet \frac{R2}{2}}{R1 + \frac{R2}{2}} \bullet C_{PL}}$$

Error Amp Filter Pole:

$$P5 = \frac{1}{2 \bullet \pi \bullet \frac{R_C \bullet R_O}{R_C + R_O} \bullet C_F}, C_F < \frac{C_C}{10}$$

The current mode zero (Z3) is a right half plane zero which can be an issue in feedback control design, but is manageable with proper external component selection.

Using the circuit in Figure 18 as an example, Table 8 shows the parameters used to generate the Bode plot shown in Figure 17.

Table 8. Bode Plot Parameters

PARAMETER	VALUE	UNITS	COMMENT
R_L	14.5	Ω	Application Specific
C_{OUT}	9.4	µF	Application Specific
R_{ESR}	1	mΩ	Application Specific
R_O	305	kΩ	Not Adjustable
C_C	1000	pF	Adjustable
C_F	56	pF	Optional/Adjustable
C_{PL}	0	pF	Optional/Adjustable
R_C	10.5	kΩ	Adjustable
R1	130	kΩ	Adjustable
R2	14.6	kΩ	Not Adjustable
V_{REF}	1.215	V	Not Adjustable
V_{OUT}	12	V	Application Specific
V_{IN}	5	V	Application Specific
g_{ma}	270	µmho	Not Adjustable
g_{mp}	15.1	mho	Not Adjustable
L	1.5	µH	Application Specific
f_{OSC}	2	MHz	Adjustable

From Figure 17, the phase is –130° when the gain reaches 0dB giving a phase margin of 50°. The crossover frequency is 17kHz, which is more than three times lower than the frequency of the RHP zero Z3 to achieve adequate phase margin.

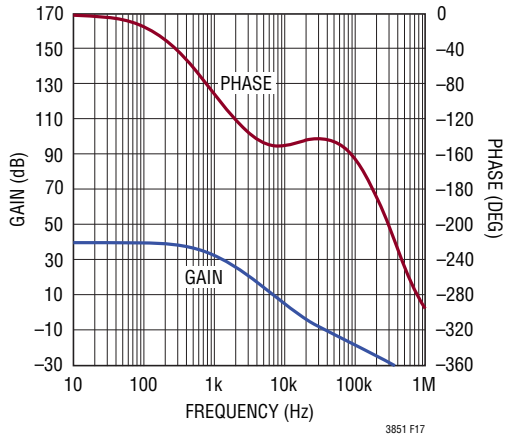
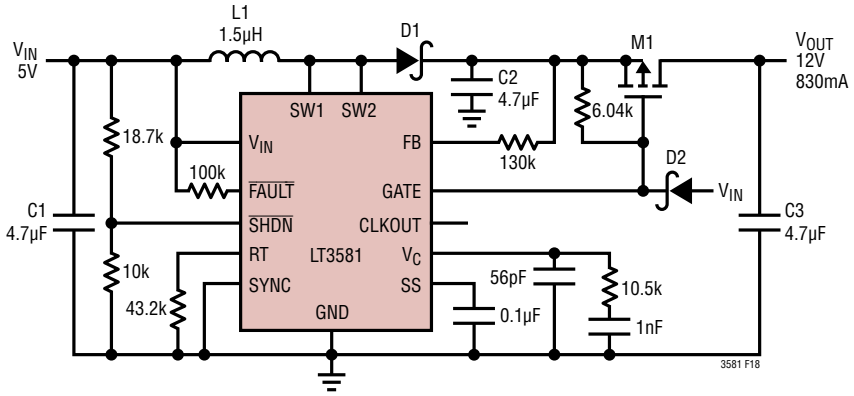


Figure 17. Bode Plot for Example Boost Converter

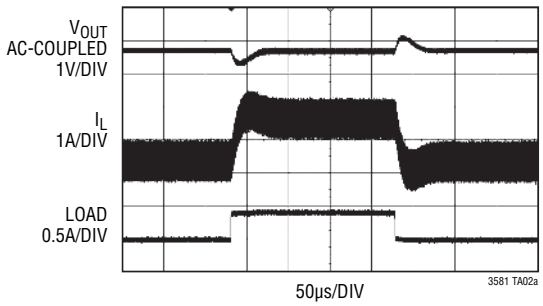
TYPICAL APPLICATIONS



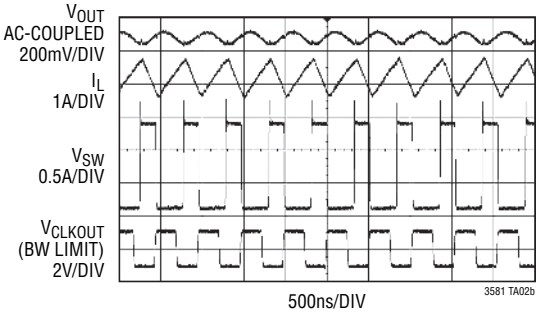
C1: 4.7µF, 16V, X7R, 1206
C2, C3: 4.7µF, 25V, X7R, 1206
D1: DIODES INC. PD3S230H-7
D2: VISHAY MSS2P3
L1: SUMIDA CDR6D28MN-IR5
M1: VISHAY SILICONIX SI7123DN

Figure 18. 2MHz, 5V to 12V, 830mA Boost Converter with Output Short Circuit Protection

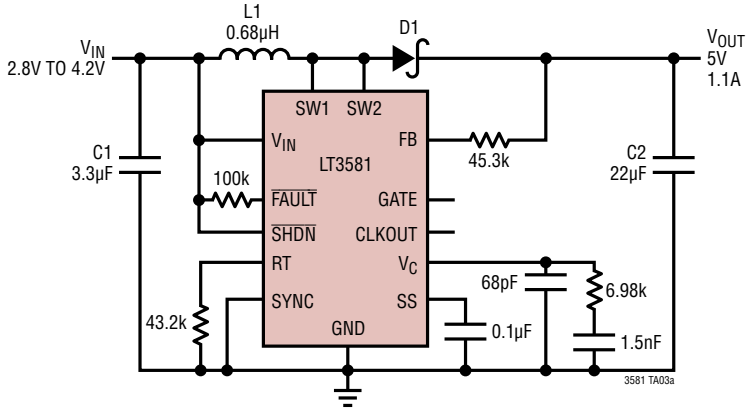
Transient Response with 430mA to 830mA to 430mA Load Step



Switching Waveforms with 830mA Load

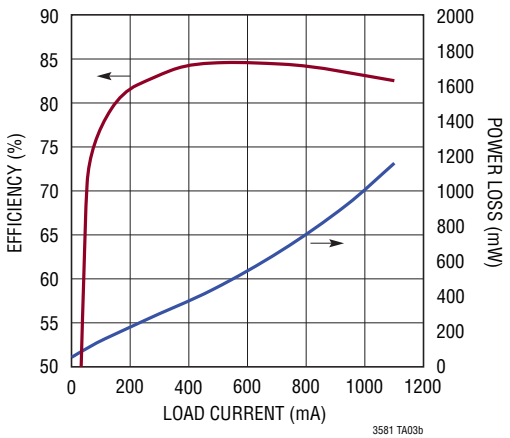


2MHz, 5V, 1.1A Boost Converter Operates from an Input Range of 2.8V to 4.2V



C1: 3.3µF, 16V, X7R, 1206
C2: 22µF, 16V, X7R, 1210
D1: DIODES INC. PD3S230H-7
L1: VISHAY IHLP1616 BZ-01-OR68 (ONLY 4.1mm × 4.5mm × 2mm)

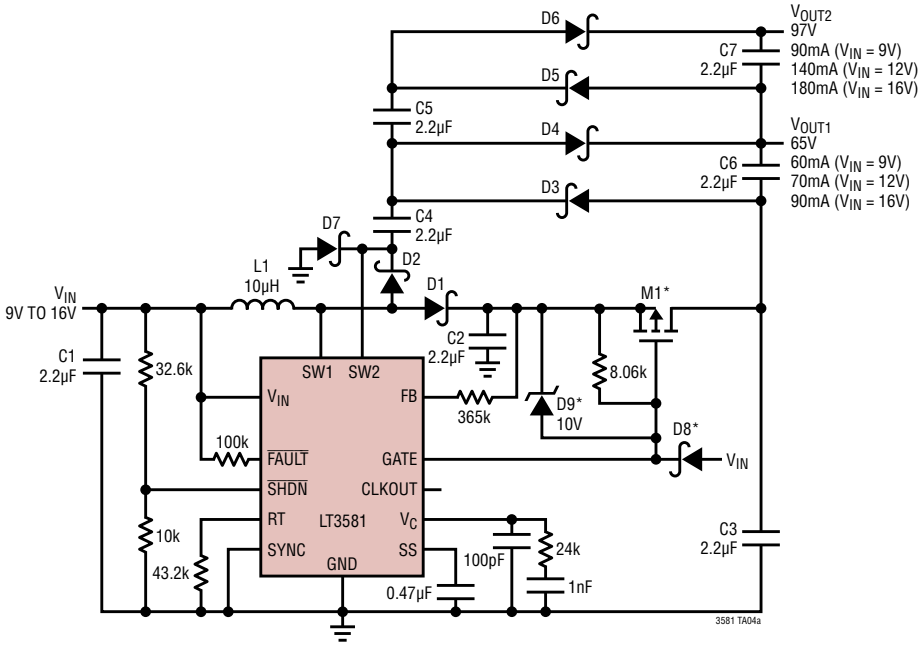
Efficiency and Power Loss at V_{IN} = 3.3V



TYPICAL APPLICATIONS

High Efficiency, VFD (Vacuum Fluorescent Display) Power Supply Switches at 2MHz to Avoid AM Band

DANGER HIGH VOLTAGE! OPERATION BY HIGH VOLTAGE TRAINED PERSONNEL ONLY

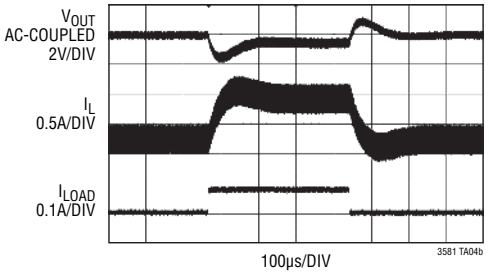


C1: 2.2µF, 25V, X7R, 1206
C2 TO C7: 2.2µF, 50V, X7R, 1206
D1 TO D7: CENTRAL SEMI SOD123F

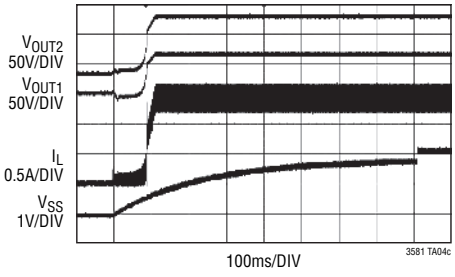
D8: CENTRAL SEMI CMDSH-3TR
D9: CENTRAL SEMI CMHZ5240B-LTZ
L1: TAIYO YUDEN NR6045T100M
M1: VISHAY SILICONIX SI7611DN

*OPTIONAL,
FOR OUTPUT SHORT-CIRCUIT
PROTECTION

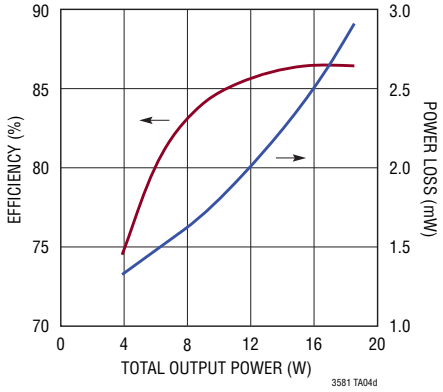
Transient Response with 60mA to 140mA to 60mA Load Step on V_{OUT2} (V_{IN} = 12V)



Start-Up Waveforms

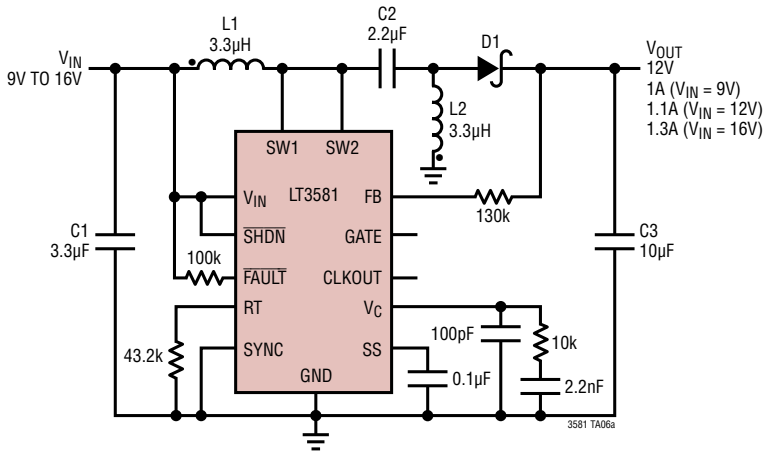


Efficiency and Power Loss at V_{IN} = 12V



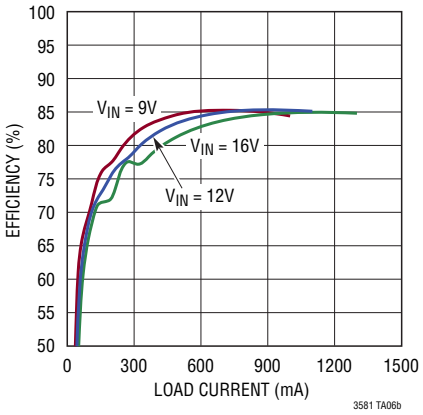
TYPICAL APPLICATIONS

2MHz, 12V SEPIC Converter Can Accept Input Voltages from 9V to 16V

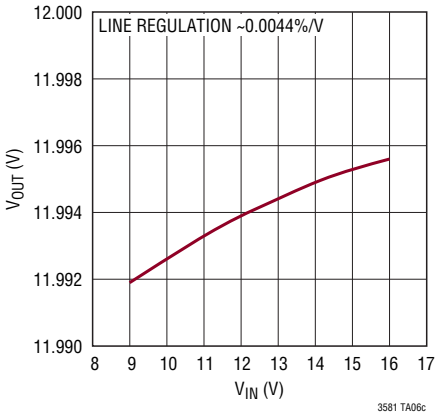


C1: 3.3µF, 25V, X7R, 1206
C2: 2.2µF, 50V, X7R, 1206
C3: 10µF, 25V, X7R, 1210
D1: CENTRAL SEMI CTLSH2-40M832
L1, L2: COILCRAFT MSD7342-332MLB

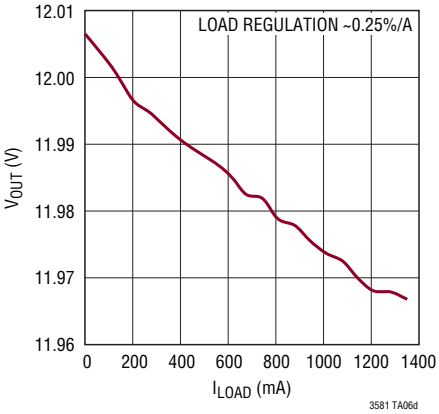
Efficiency



Line Regulation with No Load

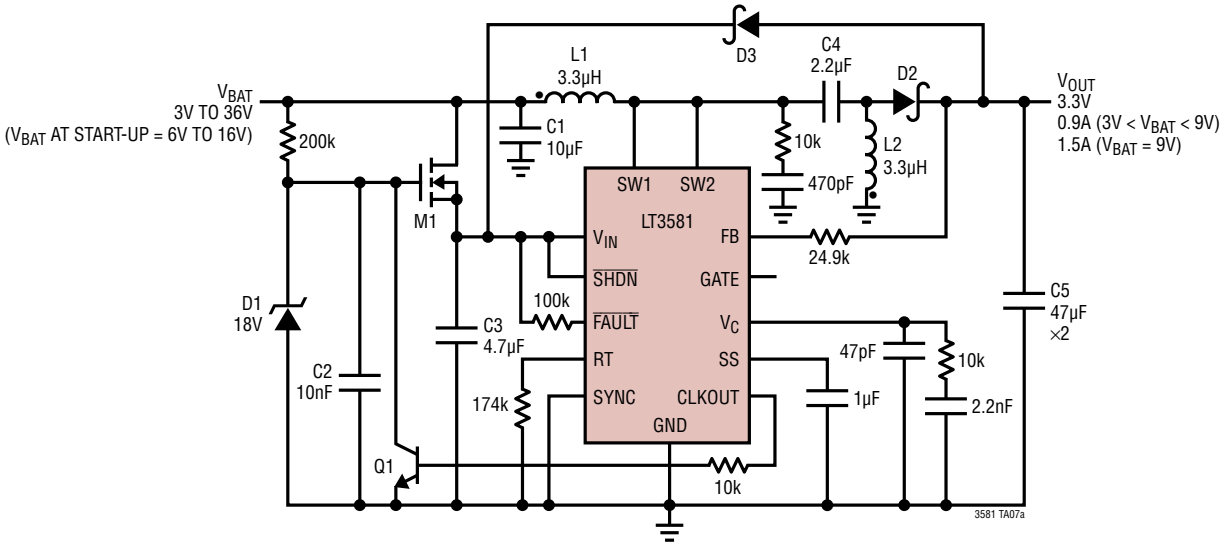


Load Regulation at V_{IN} = 12



TYPICAL APPLICATIONS

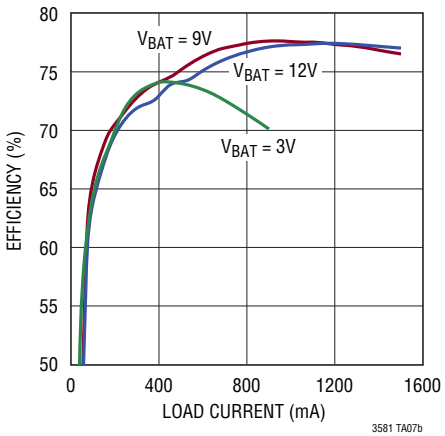
Wide Input Range, 3.3V SEPIC Converter Can Operate from 3V to 36V



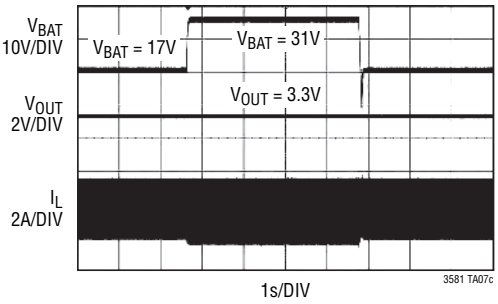
C1: 10µF, 50V, X7R, 1210
C2: 10nF, 25V, X7R, 0603
C3: 4.7µF, 25V, X7R, 1206
C4: 2.2µF, 50V, X7R, 1206
C5: 47µF, 10V, X7R, 1210
D1: CENTRAL SEMI CMHZ5248B-LTZ

D2: CENTRAL SEMI CMMSH2-40
D3: DIODES INC. PD3S230H-7
L1, L2: COILCRAFT MSD7342-332MLB
M1: 2N7002
Q1: MMBT3904

Efficiency

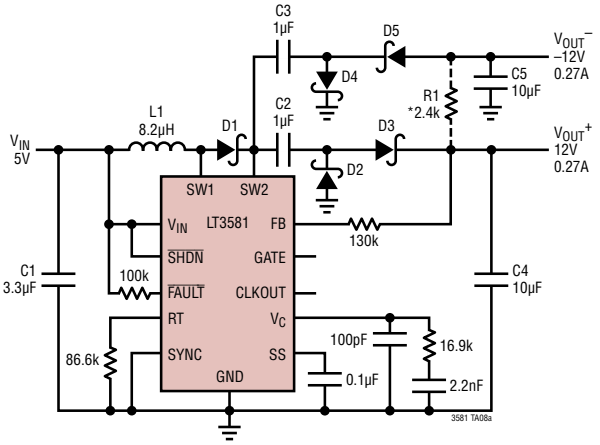


Wide Input Range SEPIC Can Ride Through V_{BAT} Voltages that Are Higher than V_{IN_OVP}



TYPICAL APPLICATIONS

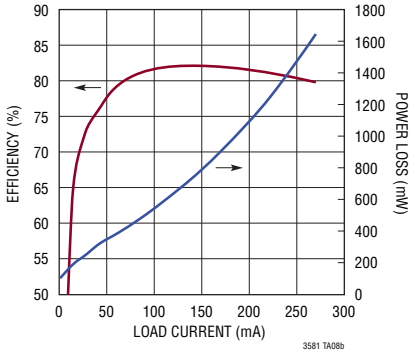
1MHz, ±12V Charge Pump Topology Uses Only Single Inductor



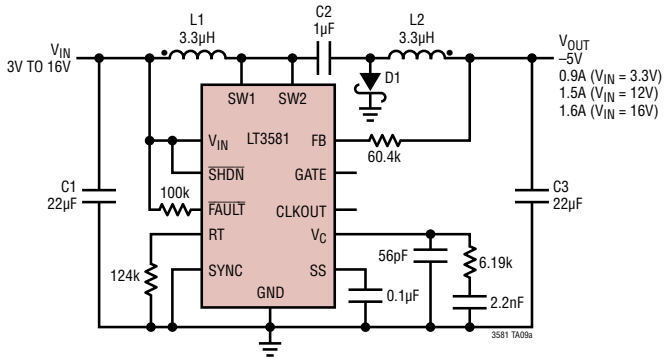
C1: 3.3µF, 25V, X7R, 1206
C2, C3: 1µF, 25V, X7R, 1206
C4, C5: 10µF, 50V, X7R, 1210
D1 TO D5: DIODES INC. PD3S230H-7
L1: VISHAY IHLP-2525CZ-01-8R2
R1: 2.4k, 2W

*IF DRIVING ASYMMMETRICAL LOADS, PLACE A 2.4k, 2W RESISTOR FROM THE 12V OUTPUT TO THE –12V OUTPUT FOR IMPROVED LOAD REGULATION OF THE –12V OUTPUT

Efficiency and Power Loss with Symmetric Load

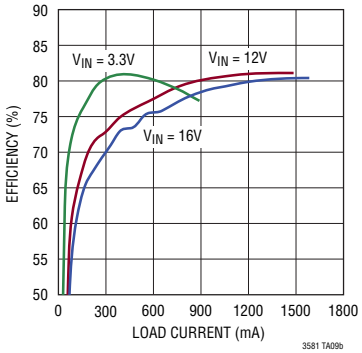


700kHz, –5V Inverting Converter Can Accept Input Voltages from 3V to 16V

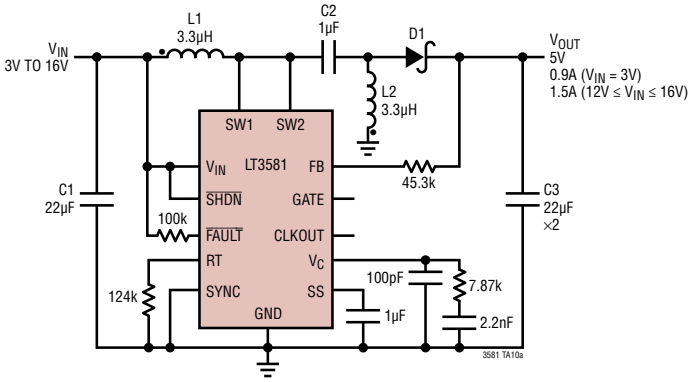


C1: 22µF, 25V, X7R, 1210
C2: 1µF, 50V, X7R, 1206
C3: 22µF, 16V, X7R, 1210
D1: VISHAY SSB44
L1, L2: COILCRAFT MSD7342-332MLB

Efficiency

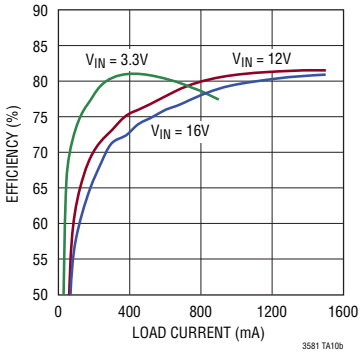


700kHz, 5V SEPIC Can Accept Input Voltages from 3V to 16V



C1: 22µF, 25V, X7R, 1210
C2: 1µF, 50V, X7R, 1206
C3: 22µF, 16V, X7R, 1210
D1: DIODES INC. B230LA
L1, L2: COILCRAFT MSD7342-332MLB

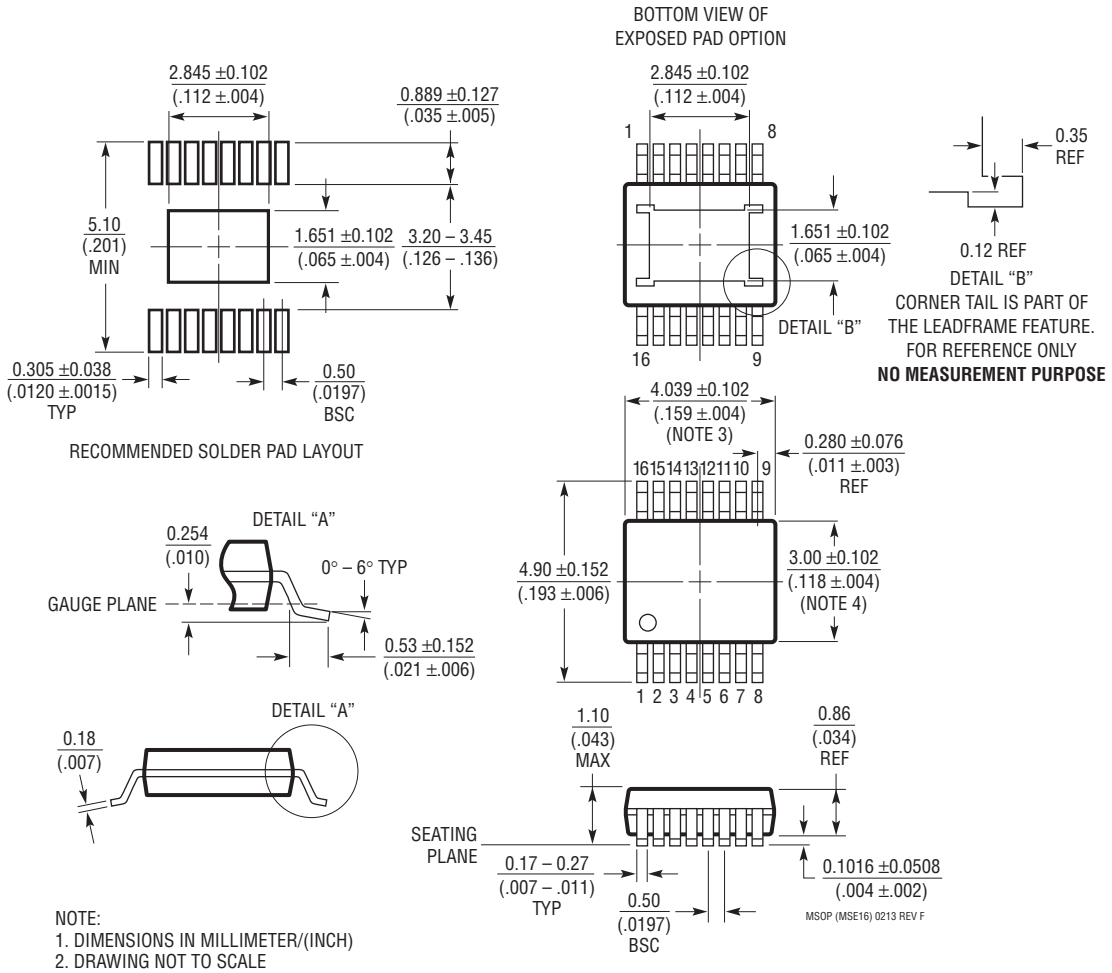
Efficiency



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev F)

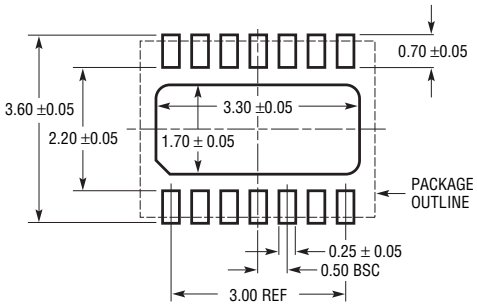


NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

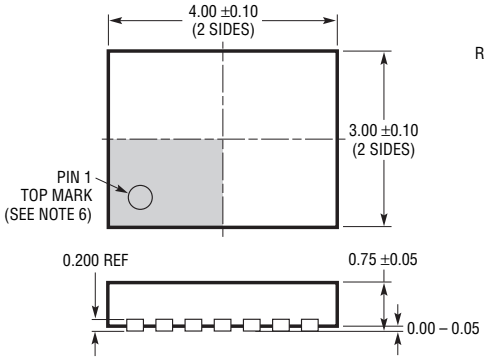
PACKAGE DESCRIPTION

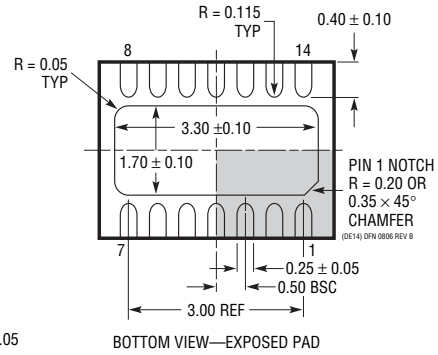
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DE Package
14-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1708 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED





BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	11/13	Added H-grade to Absolute Maximum Ratings table and Order Information table	2
		Clarified Electrical Characteristics	4
B	07/14	Clarified FAULT Output Voltage Low on Electrical Characteristics table, Typ was 150, changed to 100	4

LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.