1 to 8 Output, Multiphase Silicon Oscillator with Spread Spectrum Modulation

FEATURES

- **1-, 2-, 3-, 4-, 5-, 6-, 7- or 8-Phase Outputs**
- **One External Resistor Sets the Output Frequency from 12.5kHz to 6.67MHz**
- **Optional Spread Spectrum Frequency for Improved EMI Performance**
- **±10% Frequency Spreading**
- **Outputs Can Be Held Low or Floated (Hi-Z)**
- Three Spread Spectrum Modulation Rates $f_{OUT}/16$, $f_{OUT}/32$ and $f_{OUT}/64$
- 400µA Supply Current
- Operates from a Single 2.7V to 5.5V Supply
- Fast Start-Up Time
- First Cycle Accurate
- Outputs Are High Impedance Until Frequency Settles
- MS16 Package

APPLICATIONS

- Synchronizing Multiple Switching Power Supplies

DESCRIPTION

The LTC®6909 is an easy to use precision oscillator that can provide 1-, 2-, 3-, 4-, 5-, 6-, 7- or 8-phase synchronized outputs. The LTC6909 also offers spread spectrum frequency modulation (SSFM), which can be enabled to improve electromagnetic compatibility (EMC) performance.

Eight separate outputs provide up to eight rail-to-rail, 50% duty cycle clock signals. Using three logic inputs, the outputs are configured for phase separation, ranging from 45° to 120° (three to eight phases). The clock outputs can also be held low or configured for Hi-Z. A single resistor, combined with the phase configuration, sets the output frequency, based on the following formula:

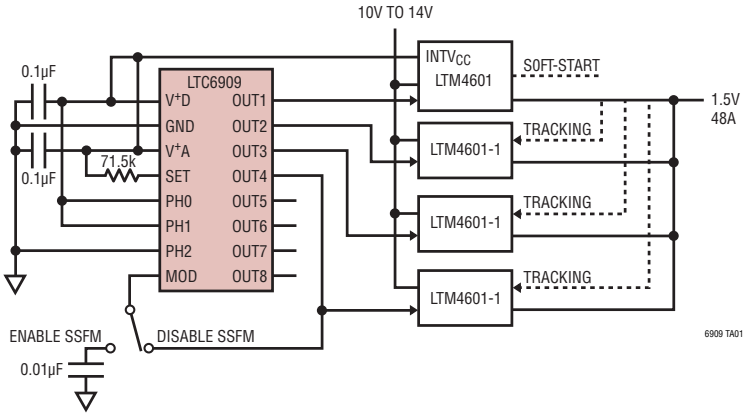
$$f_{OUT} = 20MHz \bullet 10k/(R_{SET} \bullet PH)$$

where PH = 3, 4, 5, 6, 7 or 8

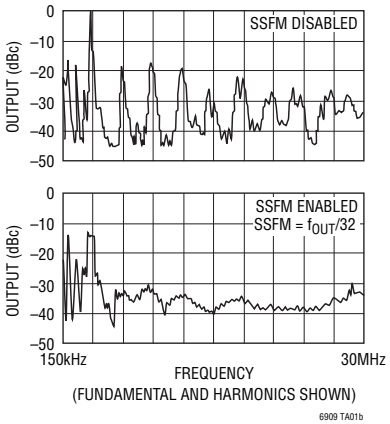
The LTC6909 can be used in applications requiring only one or two output phases. Alternatively, the LTC6908 family of parts provides the same two output signals but in a smaller SOT-23 or 2mm × 3mm DFN package. The LTC6908-1 provides complimentary (180°) outputs while the LTC6908-2 provides quadrature (90°) outputs.

TYPICAL APPLICATION

Providing a 4-Phase Synchronizing Clock to LTM Modules



150kHz to 30MHz Output Frequency Spectrum (9kHz Res BW)

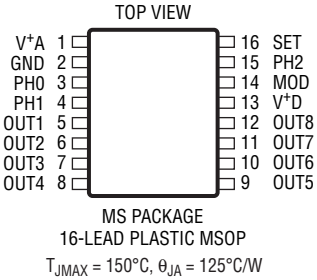


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage (V^+A) to GND 6V
Supply Voltage (V^+D) to GND 6V
Maximum Voltage
on Any Pin ..... (GND – 0.3V) ≤ V_{PIN} ≤ (V^+ + 0.3V)
Operating Temperature Range (Note 2)
LTC6909C ..... –40°C to 85°C
LTC6909I ..... –40°C to 85°C
LTC6909H ..... –40°C to 125°C
Specified Temperature Range (Note 3)
LTC6909C ..... 0°C to 70°C
LTC6909I ..... –40°C to 85°C
LTC6909H ..... –40°C to 125°C
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



MS PACKAGE
16-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 125°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6909CMS#PBF	LTC6909CMS#TRPBF	6909	16-Lead Plastic MSOP	0°C to 70°C
LTC6909IMS#PBF	LTC6909IMS#TRPBF	6909	16-Lead Plastic MSOP	–40°C to 85°C
LTC6909HMS#PBF	LTC6909HMS#TRPBF	6909	16-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C or as noted. Test conditions are $V^+ = V^+A = V^+D$ = 2.7V to 5.5V, R_L = 5k, C_L = 5pF unless otherwise noted. The modulation is turned off (MOD is connected to OUT1) and PH = 8 unless otherwise specified. R_{SET} is defined as the resistor connected from the SET pin to the V^+A pin.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Δf_{MASTER}	Frequency Accuracy (Notes 4, 5)	V^+ = 5V, PH = 3	500kHz ≤ f_{MASTER} ≤ 10MHz			±1	±2.5	%
			500kHz ≤ f_{MASTER} ≤ 10MHz	●		±2.5	±3	%
			100kHz ≤ f_{MASTER} < 500kHz	●		±3	±4.5	%
			10MHz ≤ f_{MASTER} ≤ 20MHz	●		±2.7	±3.5	%
		V^+ = 2.7V, PH = 3	500kHz ≤ f_{MASTER} ≤ 10MHz			±0.5	±2.5	%
			500kHz ≤ f_{MASTER} ≤ 10MHz	●		±2	±3	%
			100kHz ≤ f_{MASTER} < 500kHz	●		±2.5	±4.5	%
$\Delta f_{OUT}/\Delta T$	Frequency Drift Over Temperature	R_{SET} = 100k		●		±0.004		%/°C
$\Delta f_{OUT}/\Delta V^+$	Frequency Drift Over Supply	V^+ = 4.5V to 5.5V, R_{SET} = 100k		●		0.4	0.9	%/V
		V^+ = 2.7V to 3.6V, R_{SET} = 100k		●		0.04	0.35	%/V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C or as noted. Test conditions are $V^+ = V^+A = V^+D$ = 2.7V to 5.5V, R_L = 5k, C_L = 5pF unless otherwise noted. The modulation is turned off (MOD is connected to OUT1) and PH = 8 unless otherwise specified. R_{SET} is defined as the resistor connected from the SET pin to the V^+A pin.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
R_{SET}	Range of the R_{SET} Resistor Connected Between the V^+A Pin and the SET Pin	4.5V ≤ V^+ ≤ 5.5V 2.7V ≤ V^+ ≤ 4.5V		10 20		2000 2000	kΩ kΩ
	Frequency Spread with SSFM Enabled	R_{SET} = 100k MOD Pin = V^+, GND or Open	●	±7	±10	±13	%
	Long-Term Stability of the Output Frequency (Note 9)				300		ppm/√kHr
	Duty Cycle (Note 6)	SSFM Disabled	●	45	50	55	%
V^+A, V^+D	Operating Supply Voltage Range		●	2.7		5.5	V
I_S	V^+ Combined Supply Current	R_{SET} = 2M, R_L = ∞, PH = 8, MOD = V^+, (f_{OUT} = 12.5kHz), SSFM = f_{OUT}/64 V^+ = 5V V^+ = 2.7V	 ● ●		 0.6 0.55	 0.85 0.8	 mA mA
		R_{SET} = 20k, R_L = ∞, PH = 3, MOD = GND, (f_{OUT} = 3.33MHz), SSFM = f_{OUT}/16 V^+ = 5V V^+ = 2.7V	 ● ●		 2.4 1.55	 2.7 1.8	 mA mA
		R_{SET} = 2M, R_L = ∞, PH = 8, MOD = OUT1, (f_{OUT} = 12.5kHz), SSFM Off V^+ = 5V V^+ = 2.7V	 ● ●		 0.4 0.37	 0.65 0.6	 mA mA
V_{IH_MOD}	High Level MOD Input Voltage		●	V^+ – 0.4			V
V_{IL_MOD}	Low Level MOD Input Voltage		●			0.4	V
I_{MOD}	MOD Input Current (Note 7)	MOD Pin = V^+, V^+ = 5V MOD Pin = GND, V^+ = 5V	● ●	 –4	2 –2	4	µA µA
V_{IH_PH}	High Level PHx Input Voltage	PHx Refers to PH0, PH1 and PH2	●	V^+ – 0.4			V
V_{IL_PH}	Low Level PHx Input Voltage	PHx Refers to PH0, PH1 and PH2	●			0.4	V
I_{IN_PHX}	Digital Input Current, PH0, PH1, PH2	0V < V_{IN} < V^+	●			±1	µA
V_{OH}	High Level Output Voltage (OUT1 Through OUT8)(Note 7)	V^+ = 5V: No Load V^+ = 5V: 5mA Load to GND	 ●	 4.35	4.92 4.65	 	V V
		V^+ = 2.7V: No Load V^+ = 2.7V: 3mA Load to GND	 ●	 2.1	2.63 2.4	 	V V
V_{OL}	Low Level Output Voltage (OUT1 Through OUT8)(Note 7)	V^+ = 5V: No Load V^+ = 5V: 5mA Load to V^+	 ●		0.07 0.25	 0.55	V V
		V^+ = 2.7V: No Load V^+ = 2.7V: 3mA Load to V^+	 ●		0.07 0.25	 0.55	V V
t_r	Output Rise Time (Note 8)	V^+ = 5V V^+ = 2.7V			1.6 2.5		ns ns
t_f	Output Fall Time (Note 8)	V^+ = 5V V^+ = 2.7V			1.6 2		ns ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: LTC6909C and the LTC6909I are guaranteed functional over the operating temperature range of –40°C to 85°C.

Note 3: The LTC6909C is guaranteed to meet specified performance from 0°C to 70°C. The LTC6909C is designed, characterized and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LTC6909I is guaranteed to meet specified performance from –40°C to 85°C. The LTC6909H is guaranteed to meet specified performance from –40°C to 125°C.

ELECTRICAL CHARACTERISTICS

Note 4: f_{MASTER} is the internal master oscillator frequency. The output frequency is f_{MASTER}/PH. The PH value is determined by the connections of the PH0, PH1 and PH2 pins as described in the Applications Information section.

Note 5: Frequency accuracy is defined as the deviation from the f_{OUT} equation. f_{MASTER} = 20MHz • 10k/R_{SET}, f_{OUT} = 20MHz • 10k/(R_{SET} • PH), PH = 3, 4, 5, 6, 7 or 8.

Note 6: Guaranteed by 5V test.

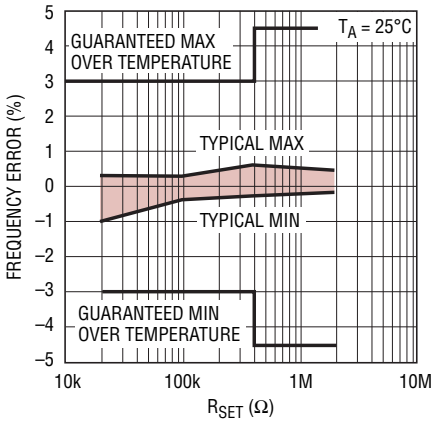
Note 7: To conform to the Logic IC Standard, current out of a pin is defined as a negative value.

Note 8: Output rise and fall times are measured between the 10% and the 90% power supply levels with no output loading. These specifications are based on characterization.

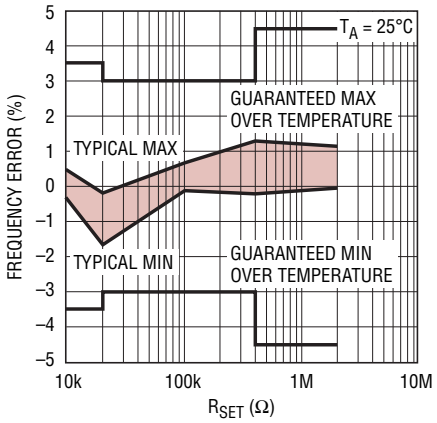
Note 9: Long term drift on silicon oscillators is primarily due to the movement of ions and impurities within the silicon and is tested at 30°C under otherwise nominal operating conditions. Long term drift is specified as ppm/$\sqrt{kHr}$ due to the typically nonlinear nature of the drift. To calculate drift for a set time period, translate that time into thousands of hours, take the square root and multiply by the typical drift number. For instance, a year is 8.77kHr and would yield a drift of 888ppm at 300ppm/$\sqrt{kHr}$. Drift without power applied to the device (aging) may be approximated as 1/10th of the drift with power, or 30ppm/$\sqrt{kHr}$ for a 300ppm/$\sqrt{kHr}$ device.

TYPICAL PERFORMANCE CHARACTERISTICS

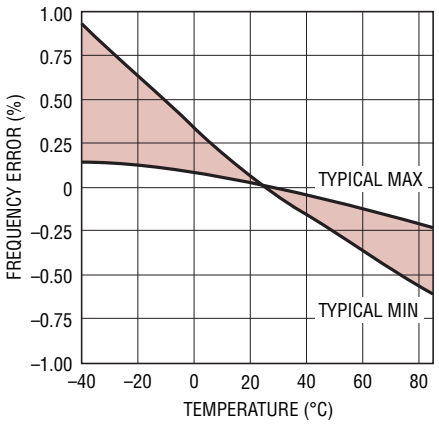
Frequency Error vs R_{SET}, V^+ = 2.7V



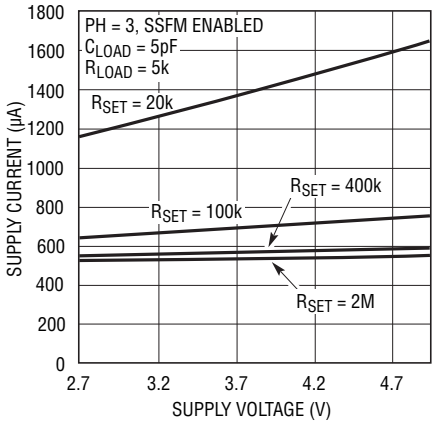
Frequency Error vs R_{SET}, V^+ = 5V



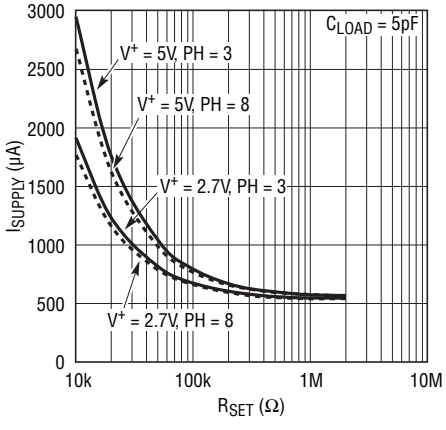
Frequency Error vs Temperature



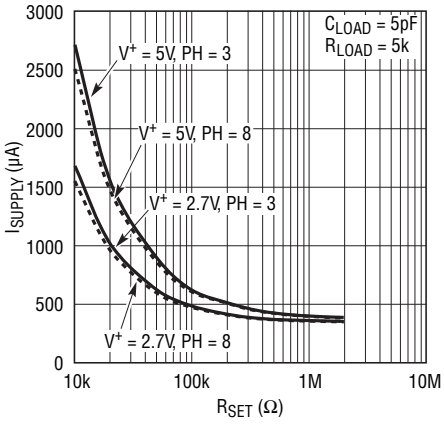
Supply Current vs Supply Voltage



Supply Current vs R_{SET} (SSFM Enabled)

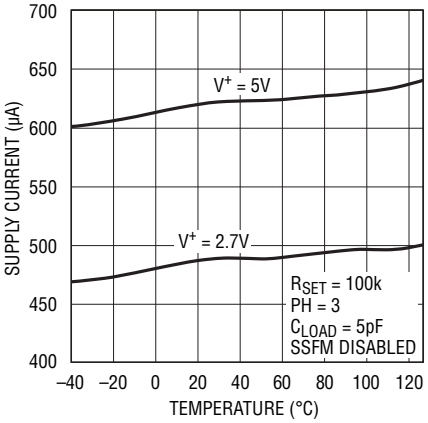


Supply Current vs R_{SET} (SSFM Disabled)

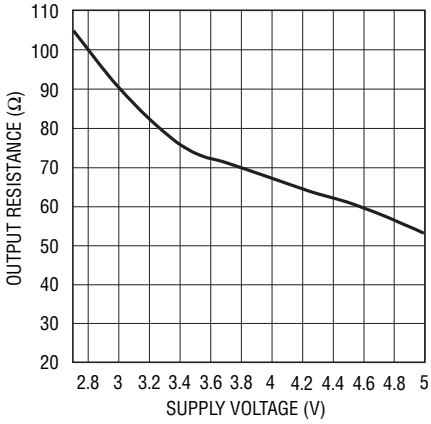


TYPICAL PERFORMANCE CHARACTERISTICS

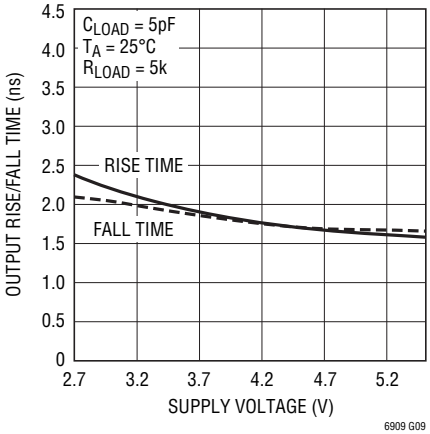
Supply Current vs Temperature



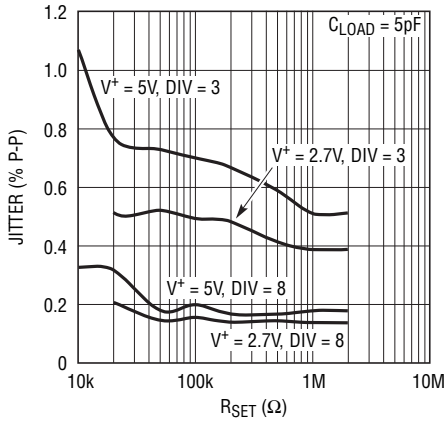
Typical Output Resistance vs Supply Voltage



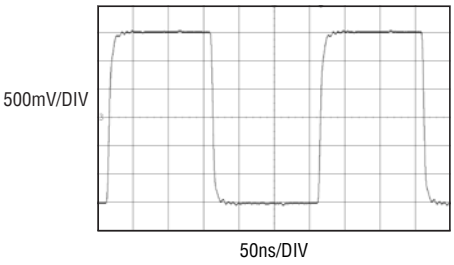
Output Rise/Fall Time vs Supply Voltage



Jitter vs R_{SET}

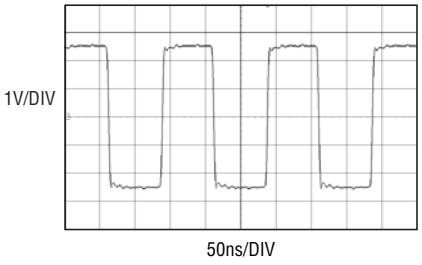


Output Operating at 3.33MHz



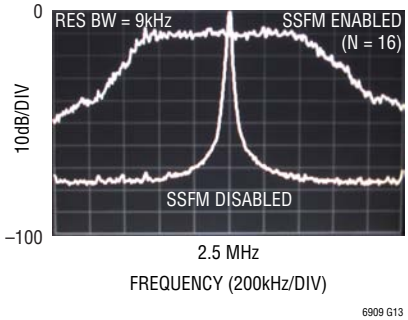
V+ = 3.3V
CLOAD = 15pF
RLOAD = 5k

Output Operating at 6.66MHz



V+ = 5V
CLOAD = 15pF
RLOAD = 5k

Output Frequency Spectrum SSFM Enable and Disabled



PIN FUNCTIONS

V⁺A (Pin 1): Analog Voltage Supply (2.7V ≤ V⁺A ≤ 5.5V). This supply should be kept free of noise and ripple. It should be bypassed directly to GND with a 0.1µF or greater low ESR capacitor. V⁺A and V⁺D must be connected to the same supply voltage.

GND (Pin 2): Ground Connections. Should be tied to a ground plane for best performance.

PH0, PH1, PH2 (Pins 3, 4, 15): Output Phasing Selection Pins. These are standard CMOS logic input pins and they do not have an internal pull-up or pull-down. These pins must be connected to a valid logic input 0 or 1 voltage. Connect the pins to GND for a logic 0 and to the V⁺D pin for a logic 1. These pins configure the output phase relationships as follows:

PH2	PH1	PH0	MODE
0	0	0	All Outputs Are Floating (Hi-Z)
0	0	1	All Outputs Are Held Low
0	1	0	3-Phase Mode (PH = 3)
0	1	1	4-Phase Mode (PH = 4)
1	0	0	5-Phase Mode (PH = 5)
1	0	1	6-Phase Mode (PH = 6)
1	1	0	7-Phase Mode (PH = 7)
1	1	1	8-Phase Mode (PH = 8)

The PH0, PH1, PH2 pin connections not only determine the phase relationship of the output signals but also divide the master oscillator frequency by the value PH.

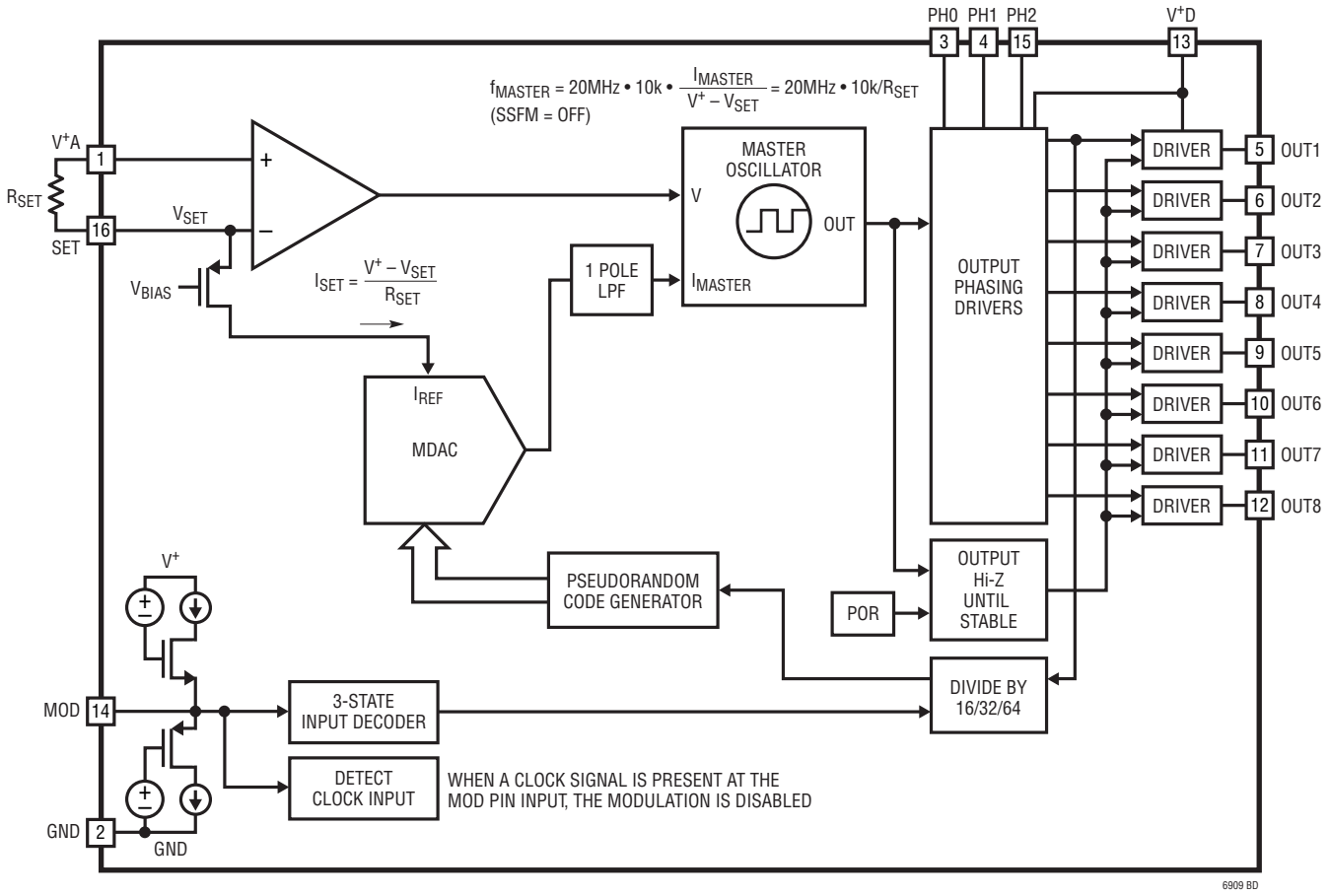
OUT1 Through OUT8 (Pins 5 Through 12): Oscillator Outputs. These are CMOS rail-to-rail logic outputs with a series resistance of approximately 40Ω, capable of driving 1k and/or 50pF loads. Larger loads may cause minor frequency inaccuracies due to supply bounce at high frequencies. When any output pin is not in use, it is in a floating, high impedance state. The outputs are also held in a high impedance state during start-up. After the part's internal frequency setting loop has settled, the outputs are active, clean and operating at the set frequency (first cycle accurate).

V⁺D (Pin 13): Digital Voltage Supply (2.7V ≤ V⁺D ≤ 5.5V). This pin should be bypassed directly to GND with a 0.1µF or greater low ESR capacitor. V⁺D and V⁺A must be connected to the same supply voltage.

MOD (Pin 14): Spread Spectrum Frequency Modulation Setting Input. This input selects among four modulation rate settings. The MOD pin should be tied to ground for an $f_{OUT}/16$ modulation rate. Floating the MOD pin selects an $f_{OUT}/32$ modulation rate. The MOD pin should be tied to V⁺D for the $f_{OUT}/64$ modulation rate. Tying one of the active outputs to the MOD pin turns the modulation off. To detect a floating MOD pin, the LTC6909 attempts to pull the pin to the midsupply point. This is realized with two internal current sources, one tied to V⁺D and MOD and the other one tied to GND and MOD. Therefore, driving the MOD pin high requires sourcing approximately 2µA. Likewise, driving the MOD pin low requires sinking approximately 2µA. **When the MOD pin is floated for the $f_{OUT}/32$ modulation rate, it must be bypassed using a 1nF or larger, capacitor to GND.** Any AC signal coupling to the MOD pin could potentially be detected and stop the frequency modulation.

SET (Pin 16): Frequency Setting Resistor Input. The value of the resistor connected between this pin and V⁺A determines the frequency of the master oscillator. The output frequency, f_{OUT}, is the master oscillator frequency divided by PH as set by the PH0, PH1 and PH2 pin connections. The voltage on this pin is held approximately 1.1V below V⁺A. For best performance, use a precision metal film resistor with a value between 20k and 400k, and limit the capacitance on the pin to less than 10pF. Resistor values outside of this range will have some loss of accuracy as noted in the Electrical Characteristics table.

BLOCK DIAGRAM



OPERATION

As shown in the Block Diagram, the LTC6909's master oscillator is controlled by the ratio of the voltage between the V+A and SET pins and the current entering the SET pin (I_{MASTER}). When the spread spectrum frequency modulation (SSFM) is disabled, I_{MASTER} is strictly determined by the ($V^+A - V_{SET}$) voltage and the R_{SET} resistor. When SSFM is enabled, I_{MASTER} is modulated by a filtered pseudorandom noise (PRN) signal. Here the I_{MASTER} current is a random value uniformly distributed between (I_{SET} – 10%) and (I_{SET} + 10%). In this way, the frequency is modulated to produce an approximately flat frequency spectrum, centered about the set frequency with a bandwidth equal to approximately 20% of the center frequency.

The voltage on the SET pin is forced to approximately 1.1V below V+A by the PMOS transistor and its gate bias voltage. This voltage is accurate to ±5% at a particular input current and supply voltage (see Figure 1). The LTC6909 is optimized for use with resistors between 20k and 400k corresponding to master oscillator frequencies between 500kHz and 10MHz. Accurate master oscillator frequencies up to 20MHz (R_{SET} = 10k) are attainable if the supply voltage is greater than 4V. The R_{SET} resistor, connected between the V+A and SET pins, locks together the ($V^+A - V_{SET}$) voltage and the current I_{SET}. This allows the parts to attain excellent frequency accuracy regardless of the precision of the SET pin. The master oscillation frequency is:

$$f_{MASTER} = 20MHz \bullet 10k/R_{SET}$$

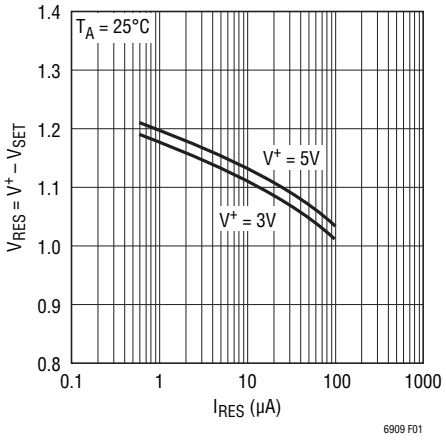


Figure 1. $V^+ - V_{SET}$ Variation with I_{RES}

When the spread spectrum frequency modulation (SSFM) is disabled, the master oscillator frequency is stationary. When SSFM is enabled, the master oscillator frequency varies from 0.9 • f_{MASTER} to 1.1 • f_{MASTER}.

Output Frequency and Configurations

The output frequency of the LTC6909 is set by the R_{SET} resistor value and the connections of the PH0, PH1 and PH2 logic input pins. The following formula defines the relationship:

$$f_{OUT} = 20MHz \bullet 10k/(R_{SET} \bullet PH)$$

where PH = 3, 4, 5, 6, 7 or 8 and is defined as follows:

PH2	PH1	PH0	MODE
0	0	0	All Outputs Are Floating (Hi-Z)
0	0	1	All Outputs Are Held Low
0	1	0	3-Phase Mode (PH = 3)
0	1	1	4-Phase Mode (PH = 4)
1	0	0	5-Phase Mode (PH = 5)
1	0	1	6-Phase Mode (PH = 6)
1	1	0	7-Phase Mode (PH = 7)
1	1	1	8-Phase Mode (PH = 8)

The PH0, PH1 and PH2 pins are standard logic input pins. These pins do not have any active pull-up or pull-down circuitry. As such, they cannot be left floating and must be connected to a valid logic high or low voltage. The PH0, PH1 and PH2 pin connections not only divide the master oscillator frequency by the value PH but also determine the phase relationship between the output signals. Figure 2 shows the output waveforms for each of the eight possible output configurations.

Note that 2-phase, complementary (180° phase shifted) outputs are available in the 4-, 6- and 8-phase modes by choosing the correct pair of signals. For example, in 4-phase mode, OUT1 and OUT3 (or OUT2 and OUT4) are complementary.

OPERATION

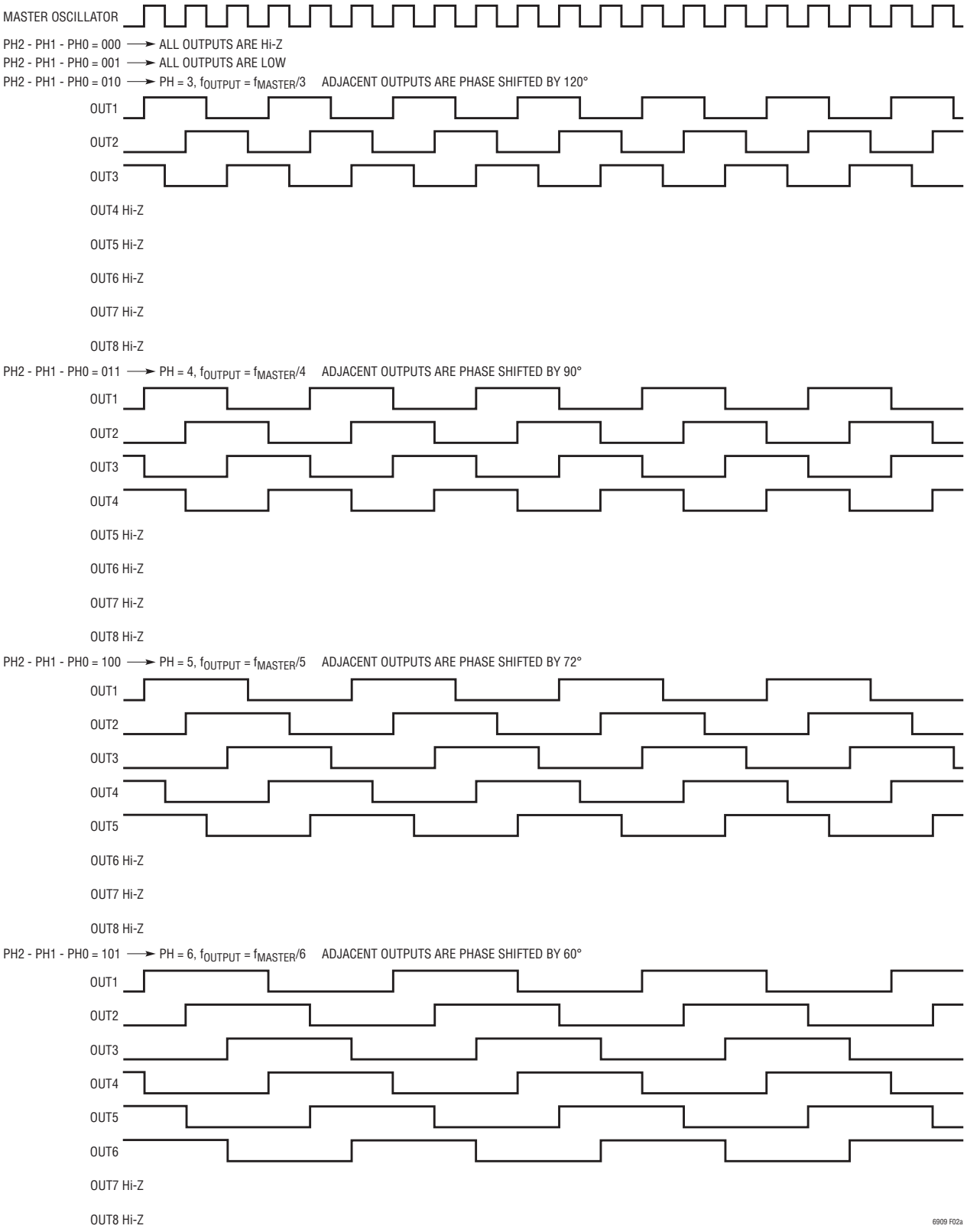


Figure 2a. Output Waveforms for Different PH Settings

OPERATION

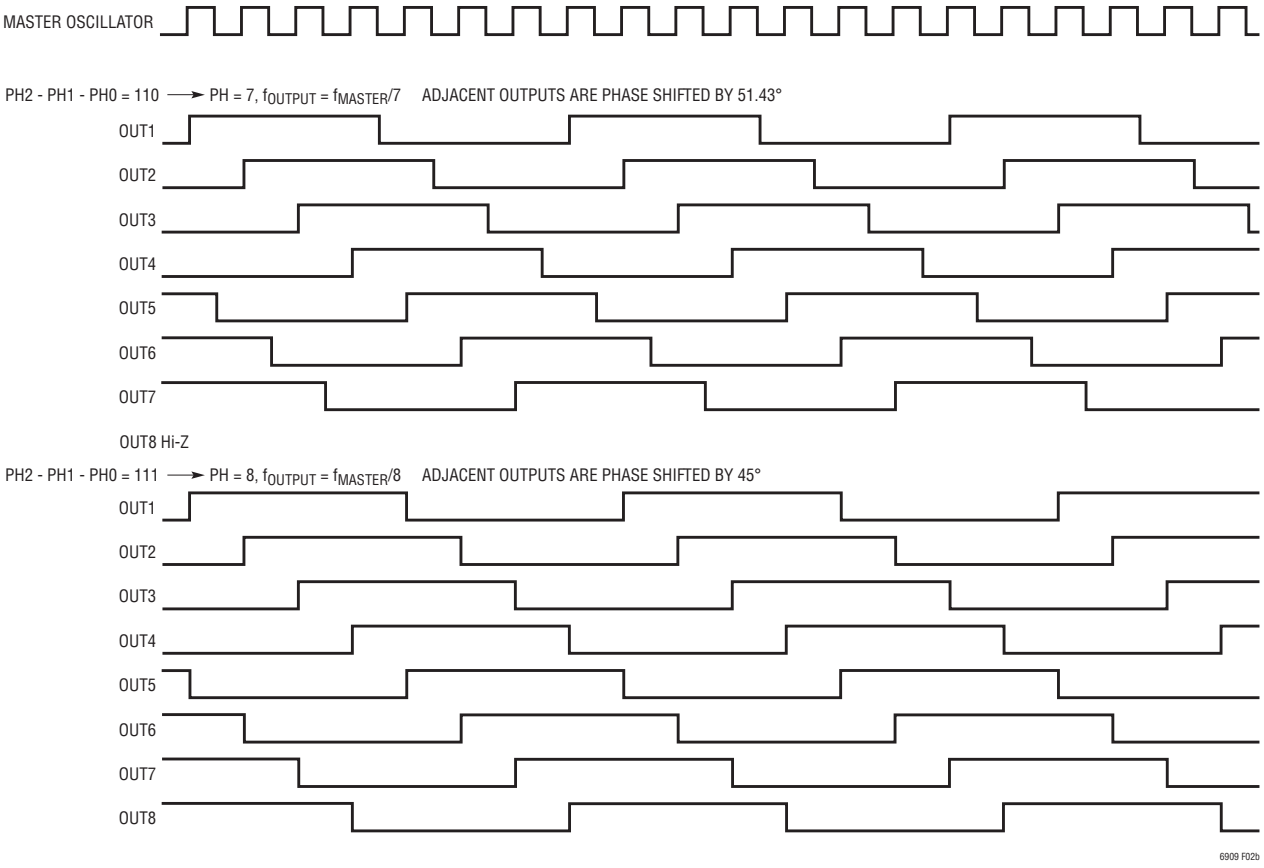


Figure 2b. Output Waveforms for Different PH Settings

OPERATION

Spread Spectrum Frequency Modulation

The LTC6909 can operate with spread spectrum frequency modulation (SSFM). In this mode, the oscillator's frequency is modulated by a pseudorandom noise (PRN) signal to spread the oscillator's energy over a wide frequency band. This spreading decreases the peak electromagnetic radiation levels and improves electromanetic compatibility (EMC) performance.

The amount of frequency spreading is fixed at 20% (±10%), where frequency spreading is defined as:

Frequency Spreading (in %) = 100 • ($f_{MAX} – f_{MIN}$)/f_{OUT}

The I_{MASTER} current is a dynamic signal generated by a multiplying digital-to-analog converter (MDAC) referenced to I_{SET} and lowpass filtered. I_{MASTER} varies in a psuedorandom noise-like manner between 0.9 • I_{SET} and 1.1 • I_{SET}. This causes the output frequency to vary in a pseudorandom noise-like manner between 0.9 • f_{OUT} and 1.1 f_{OUT}.

To disable the SSFM, connect one of the active outputs to the MOD pin. An AC detector circuit shuts down the modulation circuitry if a frequency in the vicinity of the output frequency is detected at the MOD pin.

As stated previously, the modulating waveform is a pseudorandom noise-like waveform. The pseudorandom signal is generated by a linear feedback shift register that is 15 bits long. The pseudorandom sequence will repeat every ($2^{15} – 1$) • N clock cycles. This guarantees a repetition rate below 13Hz for output frequencies up to 6.67MHz. Seven bits of the shift register are sent in parallel to the MDAC which produces the modulating current waveform. Being a digitally generated signal, the output of the MDAC is not a perfectly smooth waveform, but consists of (2^7) discrete steps that change every shift register clock cycle. Note that the shift register clock is the output frequency, f_{OUT}, divided by N, where N is the modulation rate divider setting, which is determined by the state of the MOD pin. The MOD pin should be tied to ground for the N = 16 setting. Floating the MOD pin selects N = 32. The MOD pin should be tied to V^+ for the N = 64 setting.

The output of the MDAC is then filtered by a lowpass filter with a corner frequency set to the modulation rate (f_{OUT}/N). This limits the rate of frequency change and softens the corners of the frequency control signal, but allows the waveform to fully settle at each frequency step. The rise and fall times of this single pole filter are approximately 0.35/f_{CORNER}. This is beneficial for clocking switching regulators, as discussed in the Applications Information section. Figure 3 illustrates how the output frequency varies over time.

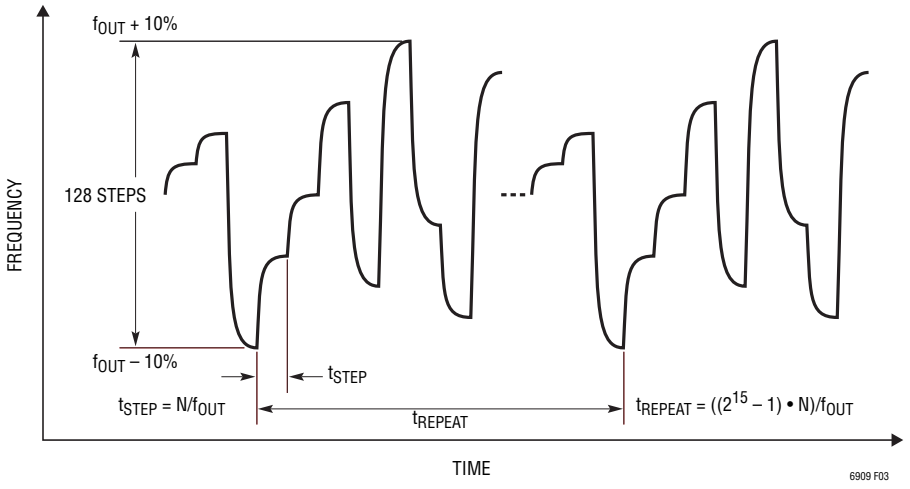


Figure 3

APPLICATIONS INFORMATION

SELECTING THE FREQUENCY-SETTING RESISTOR

The LTC6909 has a master oscillator frequency range spanning 100kHz to 20MHz depending on the R_{SET} resistor value. However, accuracy may suffer if the oscillator is operated at a master oscillator frequency greater than 10MHz with a supply voltage lower than 4V. With a linear correspondence between the master oscillator period and the R_{SET} resistance, a simple equation relates resistance with frequency.

R_{SET} =10k • 20MHz/f_{MASTER}

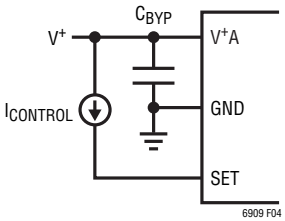
R_{SETMIN} = 10k (5V supply), 20k (2.7V supply),

R_{SETMAX} = 2M

Any R_{SET} resistor tolerance will shift the output frequency by the same amount.

ALTERNATIVE METHODS OF SETTING THE OUTPUT FREQUENCY OF THE LTC6909

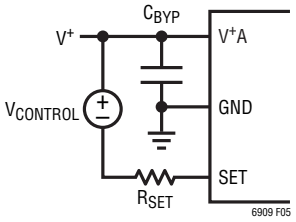
The oscillator may be programmed by any method that sources a current into the SET pin. The circuit in Figure 4 sets the oscillator frequency using a programmable current source and in the expression for f_{OUT}, the resistor R_{SET} is replaced by the ratio of 1.1V/$I_{CONTROL}$. As already explained in the Operation section, the voltage difference between V^+ and SET is approximately 1.1V ±5%, therefore, the Figure 4 circuit is less accurate than if a resistor controls the output frequency.



f_{MASTER} = 10k • (20MHz/1.13V) • $I_{CONTROL}$(A)

Figure 4. Current Controlled Oscillator

Figure 5 shows the LTC6909 configured as a V_{CO}. A voltage source is connected in series with an external 10k resistor. The master oscillator frequency, f_{MASTER}, will vary with $V_{CONTROL}$, that is the voltage source connected between V^+ and the SET pin. Again, this circuit decouples



f_{OUT} = 10k • 20MHz/R_{SET}(1 – $V_{CONTROL}$/1.13V)

Figure 5. Voltage Controlled Oscillator

the relationship between the input current and the voltage between V^+ and SET; the frequency accuracy will be degraded. The oscillator frequency, however, will increase monotonically with decreasing $V_{CONTROL}$.

SETTING THE MODULATION RATE OF THE LTC6909

The modulation rate of the LTC6909 is equal to f_{OUT}/N, where N is the modulation rate divider setting, which is determined by the state of the MOD pin. The MOD pin should be tied to ground for the N = 16 setting. Floating the MOD pin selects N = 32. The MOD pin should be tied to V^+ for the N = 64 setting. To disable the SSFM, connect one of the active outputs to the MOD pin. An AC detector circuit shuts down the modulation circuitry if a frequency that is close to the output frequency is detected at the MOD pin.

When the MOD pin is floated, for the f_{OUT}/32 modulation rate, it must be bypassed by at least a 1nF capacitor to GND. Any AC signal coupling to the MOD pin could potentially be detected and stop the frequency modulation.

DRIVING LOGIC CIRCUITS

The outputs of the LTC6909 are suitable for driving general digital logic circuits. However, the form of frequency spreading used in the LTC6909 may not be suitable for many logic designs. Many logic designs have fairly tight timing and cycle-to-cycle jitter requirements. These systems often benefit from a spread spectrum clocking system where the frequency is slowly and linearly modulated by a triangular waveform, not a pseudorandom waveform. This type of frequency spreading maintains a minimal difference in the timing from one clock edge to the next adjacent clock edge (cycle-to-cycle jitter). The LTC6909 uses a pseudorandom modulating signal where the frequency

APPLICATIONS INFORMATION

transitions have been slowed and the corners rounded by a first order lowpass filter with a corner frequency set to the modulation rate (f_{OUT}/N), where N is the modulation rate divider setting, which is determined by the state of the MOD pin. This filtered modulating signal may be acceptable for many logic systems but the cycle-to-cycle jitter issues must be considered carefully.

DRIVING SWITCHING REGULATORS

The LTC6909 is designed primarily to provide an accurate and stable clock for switching regulator systems. The CMOS logic outputs are suitable for directly driving most switching regulators and switching controllers. Linear Technology has a broad line of fully integrated switching regulators and switching regulator controllers designed for synchronization to an external clock. All of these parts have one pin assigned for external clock input. The nomenclature varies depending on the part's family history. SYNC, PLLIN, SYNC/MODE, EXTCLK, FCB and S/S (shorthand for SYNC/SHDN) are examples of clock input pin names used with Linear Technology ICs.

For the best EMC performance, the LTC6909 should be run with the MOD pin tied to ground (SSFM enabled, modulation rate set to f_{OUT}/16). Regulatory testing is done with strictly specified bandwidths and conditions. Modulating faster than, or as close to, the test bandwidth as possible gives the lowest readings. The optimal modulating rate is not as straightforward when the goal is to lower radiated signal levels interfering with other circuitry in the system. The modulation rate will have to be evaluated with the specific system conditions to determine the optimal rate. Depending on the specific frequency synchronization method a switching regulator employs, the modulation rate must be within the synchronization capability of the regulator. Many regulators use a phase-locked loop (PLL) for synchronization. For these parts, the PLL loop filter should be designed to have sufficient capture range and bandwidth.

The frequency hopping transitions of the LTC6909 are slowed by a lowpass filter. The corner frequency of this filter is set to the modulation rate (f_{OUT}/N), where N is the modulation rate divider setting, which is determined by the state of the MOD pin. The MOD pin should be tied to ground for the N = 16 setting. Floating the MOD pin selects N = 32. The MOD pin should be tied to V^+ for the N = 64 setting. This is an important feature when driving a switching regulator. The switching regulator is itself a servo loop with a bandwidth typically on the order of 1/10 to 1/20 of the operating frequency. When the clock frequency's transition is within the bandwidth of the switching regulator, the regulator's output stays in regulation. If the transition is too sharp, beyond the bandwidth of the switching regulator, the regulator's output will experience a sharp jump and then settle back into regulation. If the bandwidth of the regulator is sufficiently high, beyond f_{OUT}/N, then there will not be any regulation issues.

One aspect of the output voltage that will change is the output ripple voltage. Every switching regulator has some output ripple at the clock frequency. For most switching regulator designs with fixed MOSFET's, fixed inductor, fixed capacitors, the amount of ripple will vary with the regulator's operating frequency (the main exception being hysteretic architecture regulators). An increase in frequency results in lower ripple and a frequency decrease gives more ripple. This is true for static frequencies or dynamic frequency modulated systems. If the modulating signal was a triangle wave, the regulator's output would have a ripple that is amplitude modulated by the triangle wave. This repetitive signal on the power supply could cause system problems by mixing with other desired signals creating distortion. Depending on the switching regulator's inductor design and triangle wave frequency, it may even result in an audible noise. The LTC6909 uses a pseudorandom noise-like signal. On an oscilloscope, it looks essentially noise-like of even amplitude. The signal is broadband and any mixing issues are eliminated. Additionally, the pseudorandom signal repeats at such a low rate that it is well below the audible range.

The LTC6909 with the spread spectrum frequency modulation enabled results in improved EMC performance. If the bandwidth of the switching regulator is sufficient, not a difficult requirement in most cases, the regulator's regulation, efficiency and load response are maintained while

APPLICATIONS INFORMATION

peak electromagnetic radiation (or conduction) is reduced. Output ripple may be somewhat increased, but its behavior is very much like noise and its system impact is benign.

SUPPLY BYPASSING, SIGNAL CONNECTIONS AND PCB LAYOUT

Using the LTC6909 in spread spectrum mode naturally eliminates any concerns for output frequency accuracy and stability as it is continually hopping to new settings. In fixed frequency applications however, some attention to V^+ supply voltage ripple is required to minimize additional output frequency error. Ripple frequency components on the supply line near the programmed output frequency of the LTC6909 in excess of $30mV_{P-P}$ could create an additional 0.2% of frequency error. In applications where a fixed frequency LTC6909 output clock is used to synchronize the same switching regulator that provides the V^+ supply to the oscillator, noticeable jitter of the clock may occur if the ripple exceeds $30mV_{P-P}$.

The LTC6909's accuracy is affected as described above by supply ripple on the V^+A pin only. The V^+D pin is essentially insensitive to supply ripple. The V^+A pin supplies the power for the analog section of the LTC6909 and its current is largely constant for a given R_{SET} resistor value. The V^+D pin supplies the digital section including the output drivers and its current requirement consists mainly of large bursts that digital circuitry requires when switching. The peak current required by the output drivers is by far the largest. The current is mainly dependent on output capacitive loading and the supply voltage.

Figure 6 shows how to connect the V^+A and V^+D supply pins to the power supply as well as a suggested PCB layout. The PCB layout assumes a two layer board with a ground plane in the layer beneath the part and 0805 sized passive components. The PCB layout in Figure 6 is a guide and need not be followed exactly. However, there are several items to note from the layout as follows:

1. There should be a ground plane underneath and around the part. Connect the GND pin to this plane through multiple (three to four minimum) vias to minimize inductance.
2. Place the bypass capacitors, C1 and C2, as close to the V^+A and V^+D pins as possible to minimize the inductance between the capacitor's lead and the part's pins.
3. The connection to the V^+A and V^+D pins to the main supply should be through a low impedance path. If the board has a V^+ power plane, use it instead of the top layer connection shown in Figure 6. Use multiple vias (three to four minimum) at each point to connect the V^+A and V^+D pins to the V^+ plane to minimize the inductance.
4. Connect the bypass capacitors, C1 and C2, directly to the GND pin using a low inductance path. The connection from C1 to the GND pin is easily done directly on the top layer. The C2 path is more difficult but is accomplished through multiple vias to the ground plane.
5. Connect the R_{SET} resistor directly to the SET pin and the V^+A pin. Connecting the resistor to the V^+ supply through any manner other than directly to the V^+A pin will result greater frequency error.
6. Provide a ground shield around the R_{SET} resistor and its connections to V^+A and SET. The SET pin is a fairly high impedance point and is susceptible to interference from noisy signal lines such as the part's CMOS outputs OUT1 through OUT8.
7. Route the output signals, OUT1 through OUT8, away from the SET pin as soon as possible to minimize coupling.
8. When using the LTC6909 with spread spectrum disabled, an active output is connected to the MOD pin. This is best done by routing the OUT1 signal under the part as shown in Figure 6. The ground shield between this trace and the R_{SET} resistor is very important to minimize coupling of the OUT1 signal into the SET pin.

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9. The connections for PH0, PH1 and PH2 are not shown in Figure 6. These pins are connected to either GND or V^+D depending on the output phasing required for the application. Connection to ground is done underneath the part. Connecting PH2 to V^+D is also straightforward. Connecting PH0 or PH1 to V^+D may require one or both traces to go down a layer. If you are dynamically changing one or all of the PH pins, place a 10k resistor in series with the signal line. Locate the resistor fairly close to the PH pin. This signal typically comes from a microcontroller or the power good signal from a switching regulator and is usually quite noisy. The series resistor provides some isolation between the noisy signal and the LTC6909.

START-UP ISSUES AND CONSIDERATIONS

The start-up time and settling time to within 1% of the final value is estimated by the following equation:

$$t_{START} \approx R_{SET} \bullet \left(\frac{25\mu s}{1k} \right) + 10\mu s$$

For instance, with R_{SET} = 100k, the LTC6909 will settle to within 1% of its 1MHz final value in approximately 260µs. Figure 7 shows the start-up time for various R_{SET} resistors.

To assist in an orderly start-up sequence, the LTC6909's outputs are in a high impedance state for the first 128 master clock cycles after power-up. This ensures that the first clock cycle is very close to the desired operating frequency.

Powering up and down complex multiphase switching regulator circuits is always chaotic and can have serious system consequences if it is not done carefully. In addition to the LTC6909's muting of the outputs to ensure first cycle accuracy, the PH0-PH1-PH2 codes 000 (all outputs are

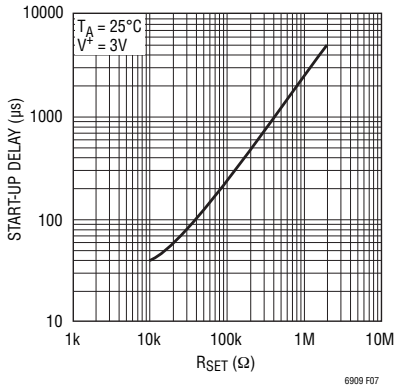
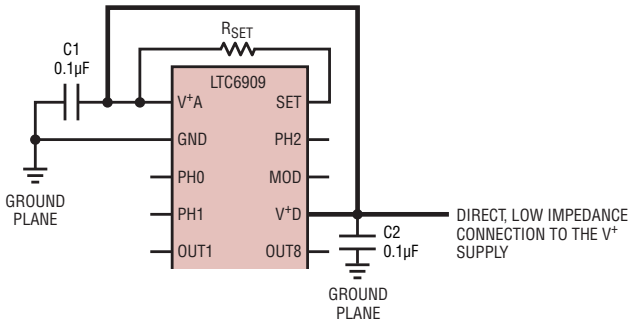


Figure 7. Start-Up Time



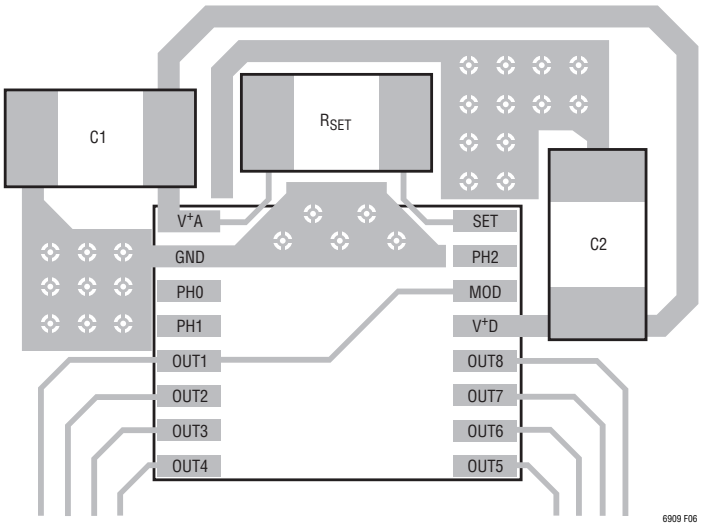


Figure 6. Supply Bypassing and PCB Layout

APPLICATIONS INFORMATION

high impedance) and 001 (all outputs are low) are useful for controlling the clocking of switching regulators during start-up. At start-up, most switching regulators ignore the clock input until a power good state is achieved. Nearly all of Linear Technology's switching regulators operate in this manner. However, some switching regulators from other vendors do not ignore the clock input on start-up and yet are not synchronizable until the power good state is reached. Attempting to synchronize these switching regulators before they reach the power good state can lead to problems. For these switching regulators it is best to have the LTC6909 held in the PH0-PH1-PH2 codes 000 or 001 until the switching regulator issues a power good signal. In most cases, simply connecting a switching regulator's power good signal to the PH0, PH1 and/or PH2 pins accomplishes this. At most, an additional single logic inverter is required to switch from either the 000 or 001 states to any of the other six states through a power good signal.

Another way to use the PH0, PH1 and PH2 inputs to assist with power-up/down issues is to use an external part to provide a supply monitor or an undervoltage lockout (UVLO). There are several parts available that combine a comparator with a reference to fulfill this function. The LTC6909 does not have its own internal UVLO. If the supply is below 2.7V, frequency accuracy may suffer. At a supply voltage around 2V or lower, the LTC6909 will operate erratically or will stop. It may stop randomly in a logic high or low state.

Figure 8 shows a circuit using an LTC1998 to monitor the supply voltage and control the logic state of the PH0 and PH1 pins. The LTC1998's threshold is set at 2.5V with 50mV of hysteresis. On power-up, as the supply ramps up, the LTC1998 holds PH0 and PH1 low, keeping the LTC6909's outputs in a high impedance state. Once the supply is above 2.55V, the LTC1998 pulls the PH0 and PH1 pins high, setting the LTC6909 into the 4-phase operating mode. On power-down, the supply ramps down and the LTC1998's output goes low once the supply is below 2.45V. This puts the LTC6909's outputs in the high impedance state. All switch overs are synchronized to the LTC6909's internal oscillator to avoid glitches and runt pulses.

To adjust the on/off supply voltage threshold, change the configuration of the LTC1998. As with the power good signal, at most an additional single logic inverter is required to switch from either the 000 or 001 states to any of the other six states.

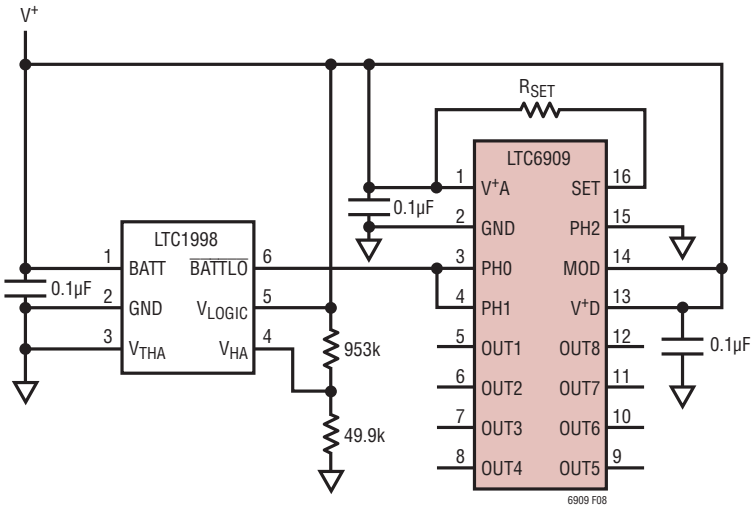
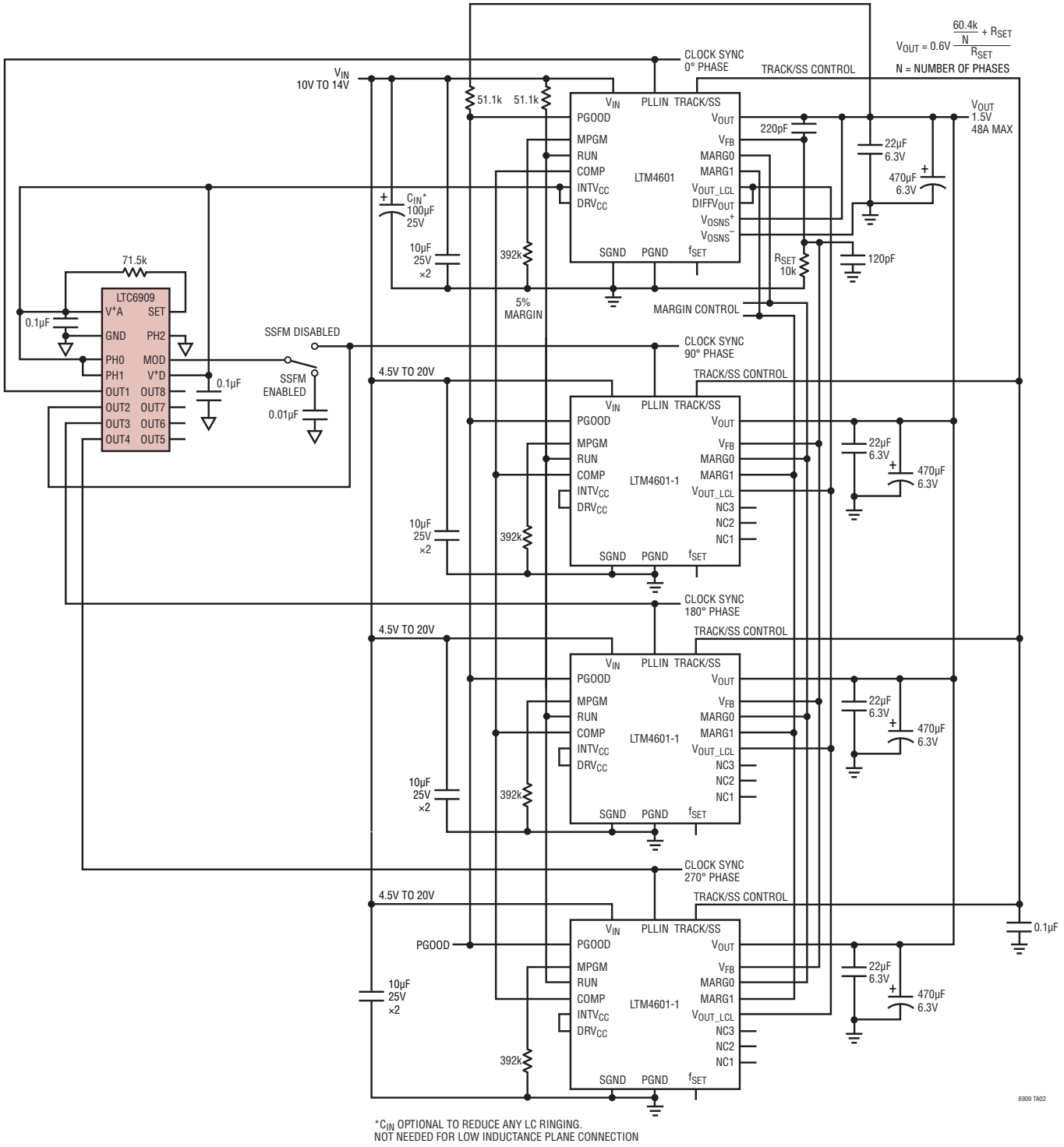


Figure 8. Adding a UVLO Feature to the LTC6909. In This Example, the LTC6909 Is in 4-Phase Mode for a V+ > ≈2.5V (PHx = 011) and the Outputs Are All High Impedance for V+ < ≈2.5V (PHx = 000)

TYPICAL APPLICATIONS

Simply Parallel Multiple DC/DC µModule® Regulator Systems to Achieve Higher Output Current. Board Layout Is as Easy as Copying and Pasting Each µModule Regulator's Layout With Very Few External Components Required

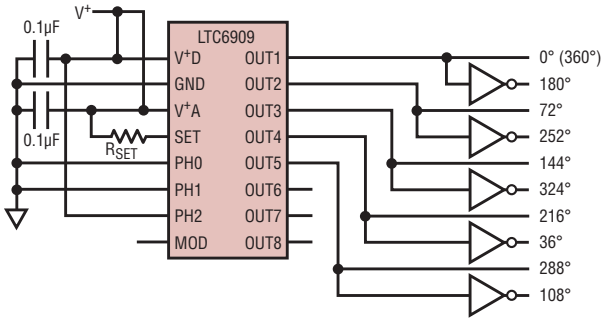


*C_{IN} OPTIONAL TO REDUCE ANY LC RINGING.
NOT NEEDED FOR LOW INDUCTANCE PLANE CONNECTION

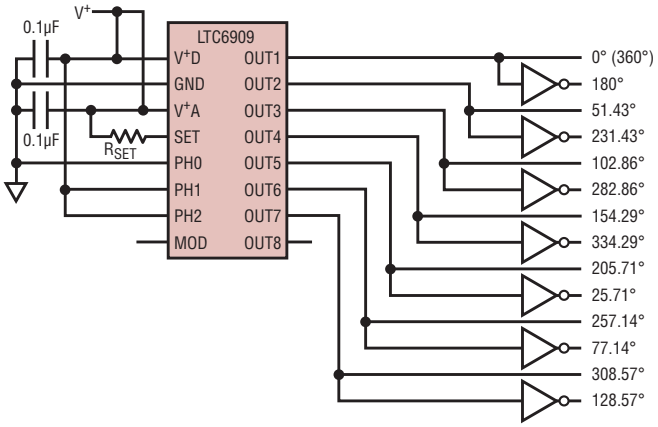
TYPICAL APPLICATIONS

Using Additional Standard Logic Inverters to Achieve 10- and 14-Phase Outputs (Inverters Are 74HC04 or Equivalent)

10 OUTPUT PHASES (OUTPUTS SHIFTED BY 36 DEGREES)



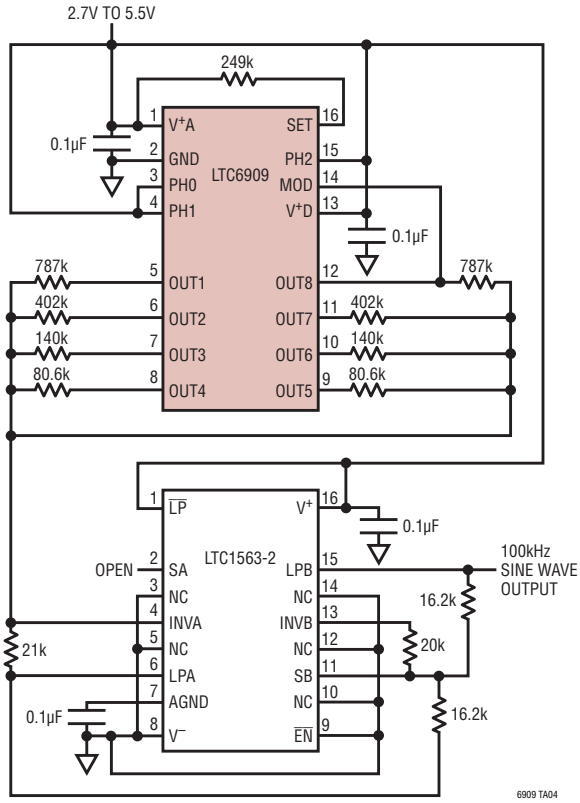
14 OUTPUT PHASES (OUTPUTS SHIFTED BY 25.71 DEGREES)

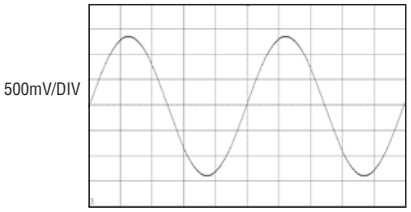


6909 TA03

TYPICAL APPLICATIONS

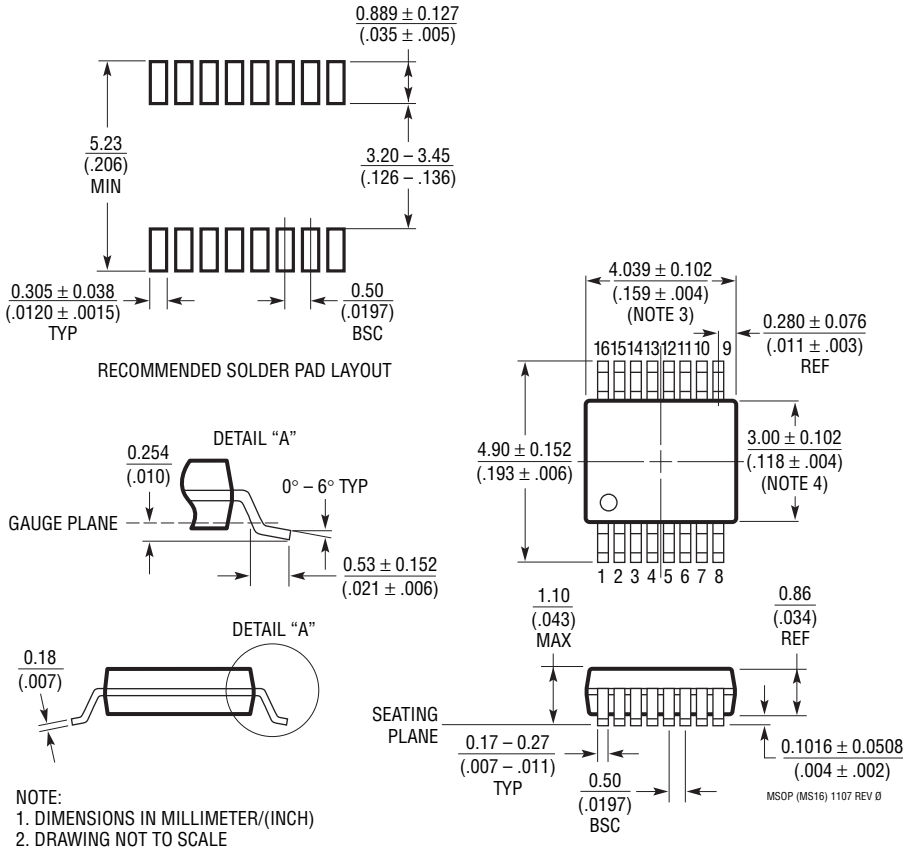
Combining Eight Outputs With a Lowpass Filter to Create a Sine Wave





PACKAGE DESCRIPTION

MS Package
16-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1669 Rev Ø)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	1/11	Revised typical value for Δf_{MASTER}, 10MHz ≤ f_{MASTER} ≤ 20MHz to ±2.7.	2
		Revised Typical Applications drawings for 10 and 14 output phases.	18