Small Footprint, Wide V_{IN} Range Synchronous Step-Down DC/DC Controller

FEATURES

- **Wide Operating V_{IN} Range: 4.5V to 38V**
- **R_{SENSE} or DCR Current Sensing**
- **±1% 0.8V Reference Accuracy Over Temperature**
- **400kHz Switching Frequency**
- Dual N-channel MOSFET Synchronous Drive
- Very Low Dropout Operation: 97% Duty Cycle
- Starts Up Into Pre-Biased Output
- Adjustable Output Voltage Soft-Start
- Output Current Foldback Limiting (Disabled During Soft-Start)
- Output Overvoltage Protection
- 5V LDO for External Gate Drive
- OPTI-LOOP® Compensation Minimizes C_{OUT}
- Low Shutdown I_Q: 15µA
- Tiny Thermally Enhanced 12-Pin 2mm × 3mm DFN and MSOP Packages

APPLICATIONS

- Automotive Systems
- Telecom Systems
- Industrial Equipment
- Distributed DC Power Systems

DESCRIPTION

The LTC3854® is a high performance synchronous step-down switching DC/DC controller that drives an all N-channel synchronous power MOSFET stage.

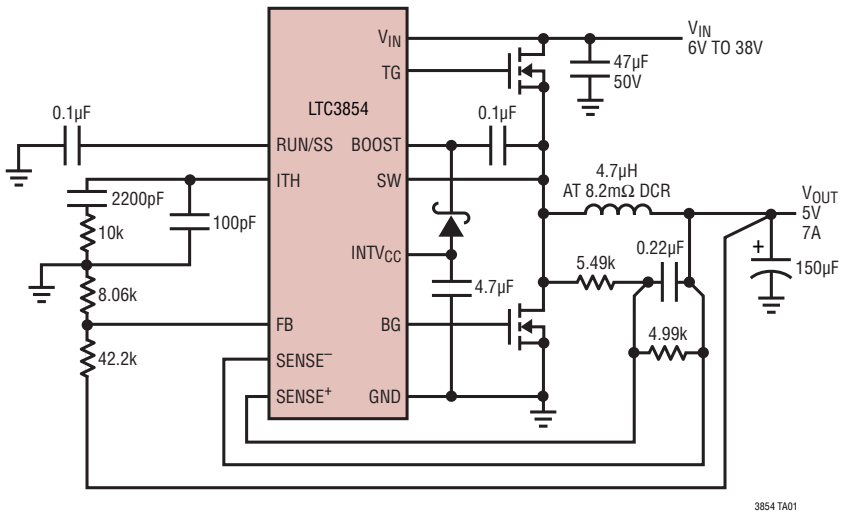
The LTC3854 features a 400kHz constant frequency current mode architecture. The LTC3854 operates from a 4.5V to 38V (40V absolute maximum) input voltage range and regulates the output voltage from 0.8V to 5.5V.

The RUN/SS pin provides both soft-start and enable features. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. Current foldback limits MOSFET dissipation during short circuit conditions. Current foldback functions are disabled during soft-start.

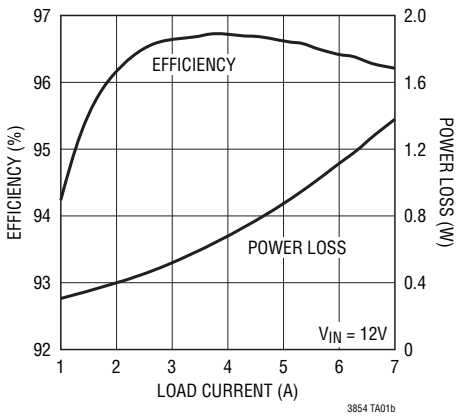
The LTC3854 has a minimum on-time at 75ns, making it well suited for high step-down ratios. The strong onboard MOSFET drivers allow the use of high power external MOSFETs to produce output currents up to 20A.

TYPICAL APPLICATION

High Efficiency Synchronous Step-Down Converter



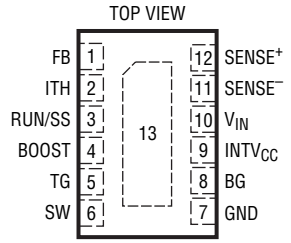
Efficiency and Power Loss vs Load Current



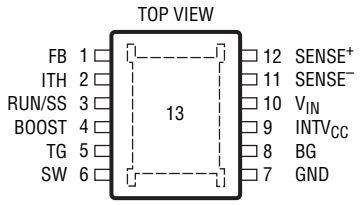
ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage (V_{IN}) ..... 40V to –0.3V
Top Side Driver Voltage (BOOST) ..... 46V to –0.3V
Switch Voltage (SW) ..... 40V to –5.0V
$INTV_{CC}$, BOOST-SW ..... 6V to –0.3V
$SENSE^+$, $SENSE^-$ ..... 6V to –0.3V
RUN/SS ..... 6V to –0.3V
ITH, FB Voltages ..... 2.7V to –0.3V
$INTV_{CC}$ Peak Output Current (Note 8) 40mA
Operating Temperature Range
(Notes 2, 3) ..... –40°C to 85°C
Maximum Junction Temperature ..... 125°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



DDB PACKAGE
12-LEAD (3mm × 2mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 76°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB



MSE PACKAGE
12-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, θ_{JA} = 40°C/W, θ_{JC} = 16°C/W
EXPOSED PAD (PIN 13) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3854EDDB#PBF	LTC3854EDDB#TRPBF	LDPC	12-Lead (3mm × 2mm) Plastic DFN	–40°C to 85°C
LTC3854IDDB#PBF	LTC3854IDDB#TRPBF	LDPC	12-Lead (3mm × 2mm) Plastic DFN	–40°C to 85°C
LTC3854EMSE#PBF	LTC3854EMSE#TRPBF	3854	12-Lead Plastic MSOP	–40°C to 85°C
LTC3854IMSE#PBF	LTC3854IMSE#TRPBF	3854	12-Lead Plastic MSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V, V_{RUN} = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
V_{IN}	Operating Input Voltage Range			4.5		38	V
V_{FB}	Regulated Feedback Voltage	(Note 4); ITH Voltage = 1.2V	●	0.792	0.8	0.808	V
I_{FB}	Feedback Current	(Note 4)			±5	±50	nA
$V_{REFLNREG}$	Reference Voltage Line Regulation	V_{IN} = 6V to 38V (Note 4)			0.002	0.02	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 4) Measured in Servo Loop; Δ_{ITH} Voltage = 0.7V to 1.2V Measured in Servo Loop; Δ_{ITH} Voltage = 1.2V to 2V	● ●		0.1 –0.1	0.5 –0.5	% %
gm	Transconductance Amplifier gm	ITH = 1.2V; Sink/Source = 5µA (Note 4)			2.0		mmho
gm_{GBW}	Transconductance Amplifier GBW	ITH = 1.2V; (Guaranteed by Design)			3		MHz
I_Q	Input DC Supply Current Normal Mode Shutdown	 (Note 5) RUN = 0V			 2 10	 3 25	 mA µA
UVLO	Undervoltage Lockout	V_{IN} Ramping Down; Measured at $INTV_{CC}$	●	3.0	3.5		V
$UVLO_{HYST}$	Undervoltage Lockout Hysteresis	V_{IN} Ramping Down then Up; Measured at $INTV_{CC}$			350		mV
V_{OVL}	Feedback Overvoltage Lockout	Measured at FB	●	0.86	0.88	0.90	V
I_{SENSE}	Sense Pins Source Current	V_{SENSE}– = V_{SENSE}+ = 3.3V			±0.5	±1	µA
DF_{MAX}	Maximum Duty Factor	In Dropout		97	98		%
$I_{RUN/SS}$	Soft-Start Charge Current	RUN/SS = 0V		0.6	1.25	2.0	µA
V_{RUN/SS_SD}	Shutdown Threshold	RUN/SS Pin Must be Taken Below this Value to Reset Part (or Put into Shutdown Mode)			0.4		V
V_{RUN/SS_ON}	Soft-Start Threshold	Soft-Start Mode			1.2		V
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	FB = 0.7V, V_{SENSE}– = 3.3V, V_{IN} = 6V		40	50	65	mV
TG R_{UP}	TG Driver Pull-Up On Resistance	TG High			2.5		Ω
TG R_{DOWN}	TG Driver Pull-Down On Resistance	TG Low			2.1		Ω
BG R_{UP}	BG Driver Pull-Up On Resistance	BG High			2.5		Ω
BG R_{DOWN}	BG Driver Pull-down On Resistance	BG Low			1.2		Ω
 TG t_r TG t_f	TG Transition Time: Rise Time Fall Time	(Note 6) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 25 25		 ns ns
 BG t_r BG t_f	BG Transition Time: Rise Time Fall Time	(Note 6) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 25 25		 ns ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver			30		ns
BG/TG t_{2D}	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver			30		ns
$t_{ON(MIN)}$	Minimum On-Time	(Note 7)			75		ns
$INTV_{CC}$ Linear Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	6V < V_{IN} < 38V		4.8	5.0	5.2	V
V_{LDO} INT	$INTV_{CC}$ Load Regulation	I_{CC} = 0 to 20mA			0.2	1.0	%
Oscillator							
f_{SW}	Switching Frequency			360	400	440	kHz

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3854E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3854I is guaranteed to meet performance specifications over the full –40°C to 85°C operating temperature range.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation PD according to the following formulas:

LTC3854DDB: $T_J = T_A + (P_D \bullet 76°C/W)$

LTC3854MSE: $T_J = T_A + (P_D \bullet 40°C/W)$

Note 4: The LTC3854 is tested in a feedback loop that servos V_{ITH} to a specified voltage and measures the resultant V_{FB}.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

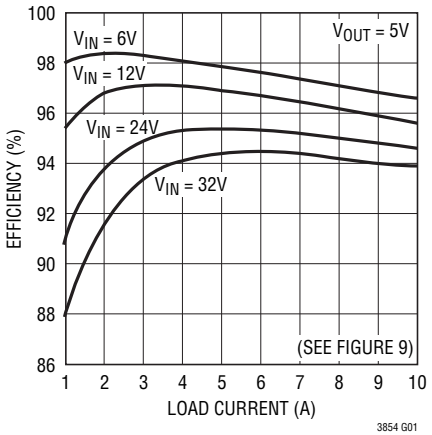
Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels. Not 100% tested in production.

Note 7: The minimum on-time condition is specified for an inductor peak-to-peak ripple current 40% of I_{MAX} (see Minimum On-Time Considerations in the Applications Information section).

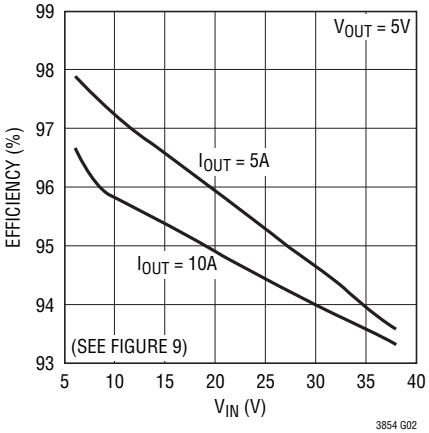
Note 8: The LTC3854 maximum LDO current specification assumes there is no external DC load current being pulled from $INTV_{CC}$ pin.

TYPICAL PERFORMANCE CHARACTERISTICS

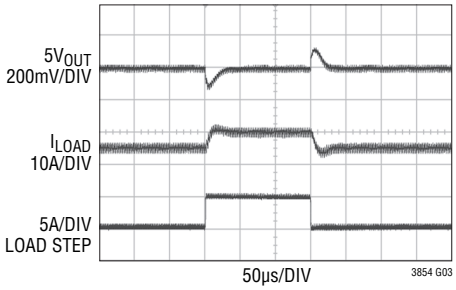
Efficiency vs Output Current



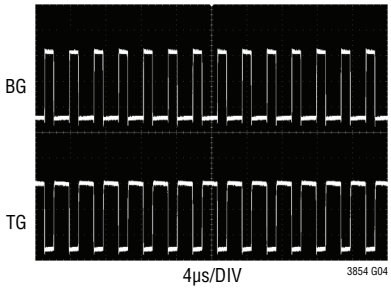
Efficiency vs Input Voltage



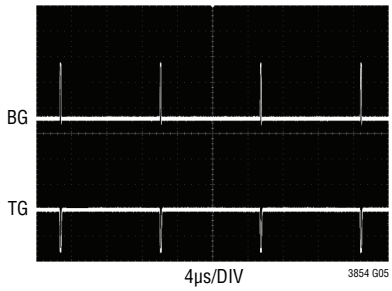
5A Load Step V_{OUT} = 5V, V_{IN} = 24V



Top Gate and Bottom Gate in Forced Continuous Mode

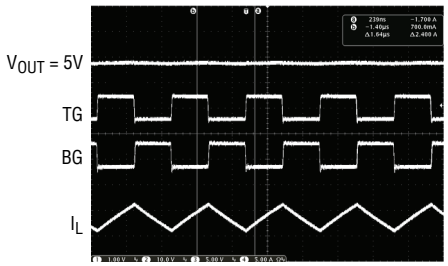


Top Gate and Bottom Gate in Dropout

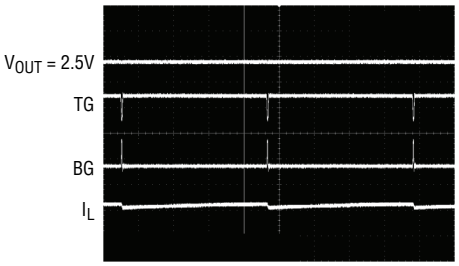


TYPICAL PERFORMANCE CHARACTERISTICS

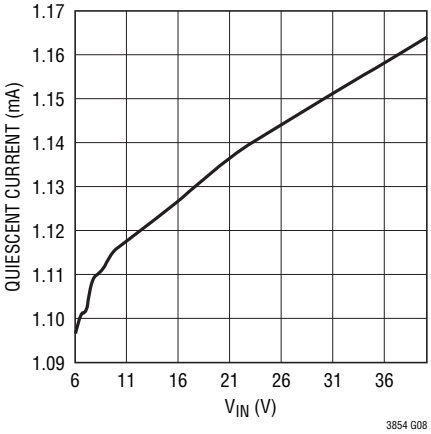
Switching Waveforms at No Load



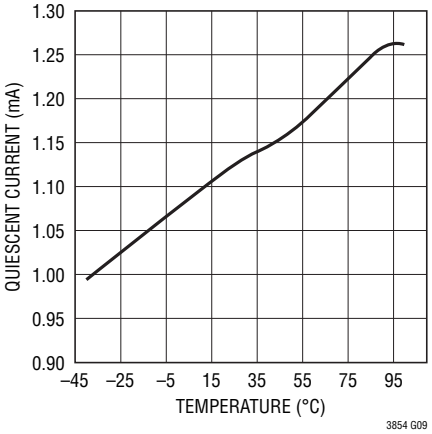
Switching Waveforms at High Duty Cycle, No Load



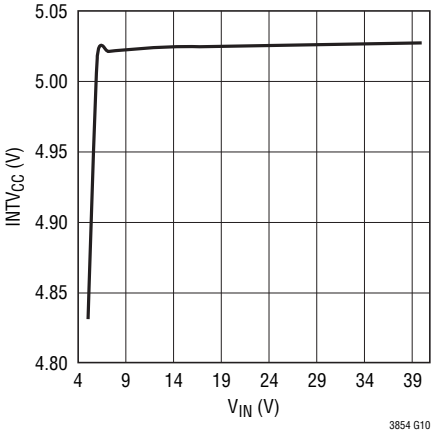
Quiescent Current vs V_{IN}



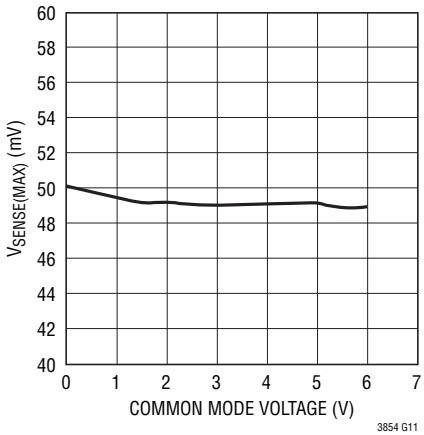
Quiescent Current vs Temperature



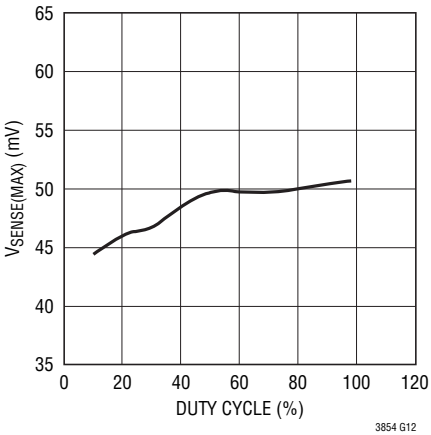
$INTV_{CC}$ vs Input Voltage



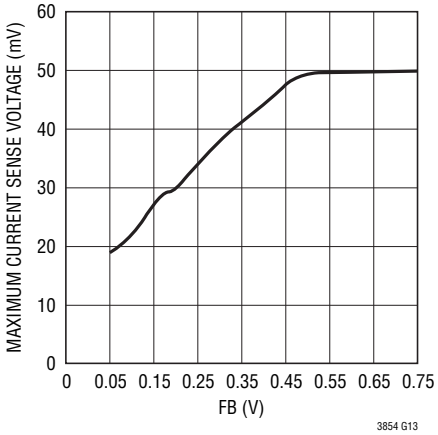
Maximum Current Sense Threshold vs Sense Common Mode Voltage



Maximum Current Sense Threshold vs Duty Cycle

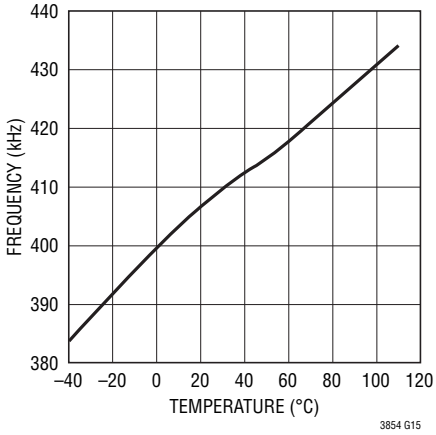


Maximum Current Sense Voltage vs Feedback Voltage (Current Foldback)

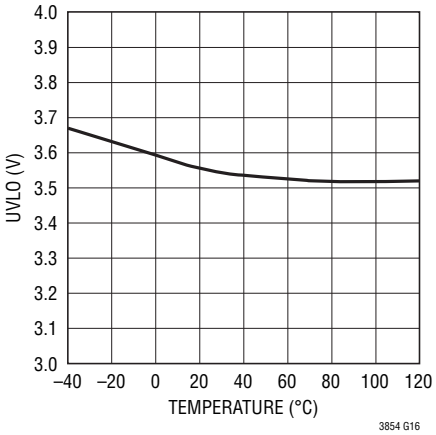


TYPICAL PERFORMANCE CHARACTERISTICS

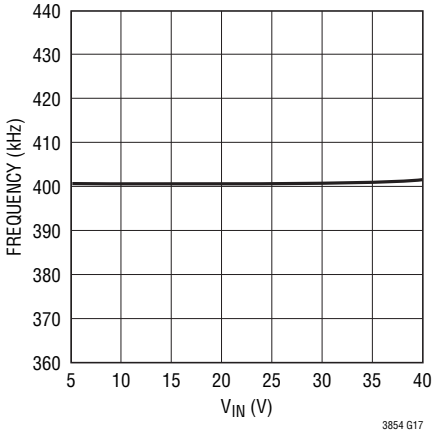
Oscillator Frequency vs Temperature



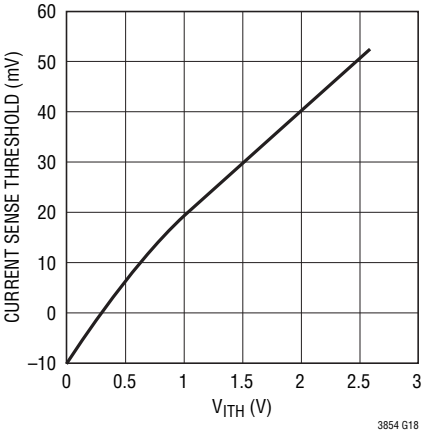
Undervoltage Lockout Falling Threshold vs Temperature



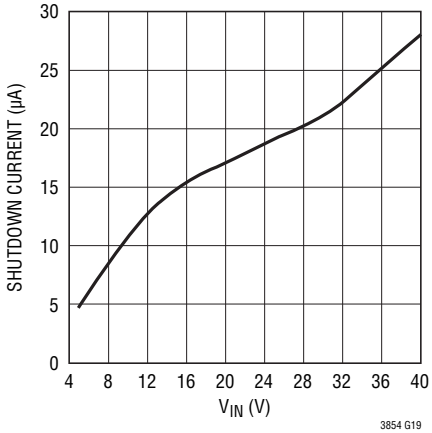
Oscillator Frequency vs V_{IN}



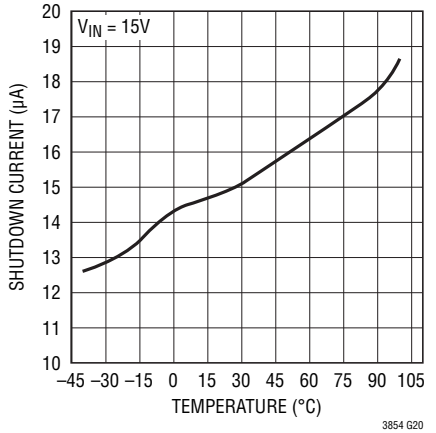
Current Sense Threshold vs I_{TH} Voltage



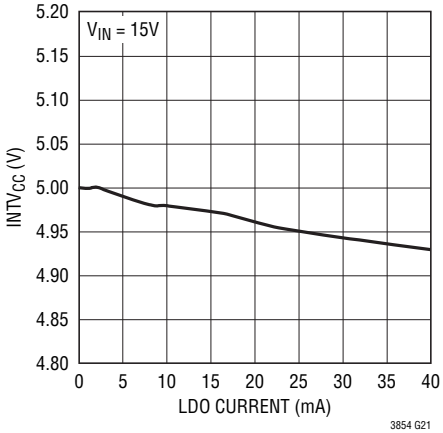
Shutdown Current vs Input Voltage



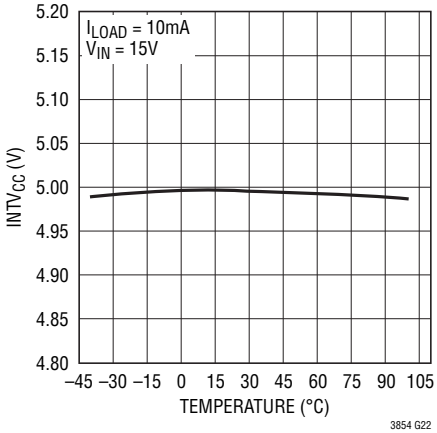
Shutdown Current vs Temperature



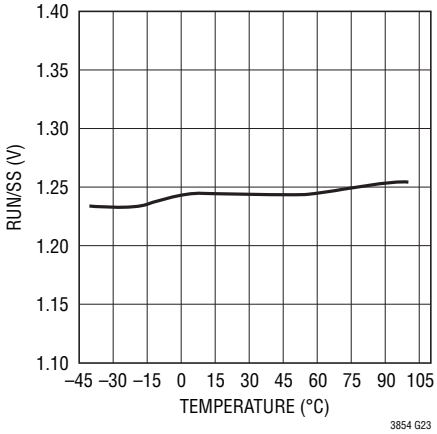
$INTV_{CC}$ Load Regulation



$INTV_{CC}$ vs Temperature



RUN/SS Shutdown Threshold vs Temperature



PIN FUNCTIONS

FB (Pin 1): Error Amplifier Feedback Input. This pin receives the remotely-sensed feedback voltage from an external resistor divider across the output.

ITH (Pin 2): Error Amplifier Output and Switching Regulator Compensation Point. The current comparator trip point increases with this control voltage.

RUN/SS (Pin 3): Run Control, Soft-Start. If the voltage on this pin is held below 0.4V, the part is in shutdown. If the pin is released the capacitance to ground at this pin sets the soft-start ramp rate. An internal 1.25µA soft-start current is always charging this pin.

BOOST (Pin 4): Bootstrapped Supply to the Top Side Floating Driver. A low ESR capacitor is connected between the BOOST and SW pins and an external Schottky diode is tied between the BOOST and $INTV_{CC}$ pins. The voltage swing on the BOOST pin is $INTV_{CC}$ to (V_{IN} + $INTV_{CC}$).

TG (Pin 5): High Current Gate Drive for Top N-channel MOSFET. This is the output of floating driver with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltage.

SW (Pin 6): Switch Node Connection to Inductor. The voltage swing on this pin is from a Schottky diode (external) forward voltage (when this diode is added across the N-channel synchronous MOSFET) below ground to V_{IN}.

GND (Pin 7): Small Signal and Power Ground. This is the high current ground for the gate driver. The internal signal ground is Kelvin connected to this pin for noise suppression.

BG (Pin 8): High Current Gate Drive for Bottom (Synchronous) N-channel MOSFET. The voltage swing at this pin is from ground to $INTV_{CC}$.

$INTV_{CC}$ (Pin 9): Output of the Internal 5V Low Dropout Regulator. The driver and control circuits are powered from this voltage. Must be decoupled to power ground with a minimum of 2.2µF low ESR ceramic capacitor (X5R or better).

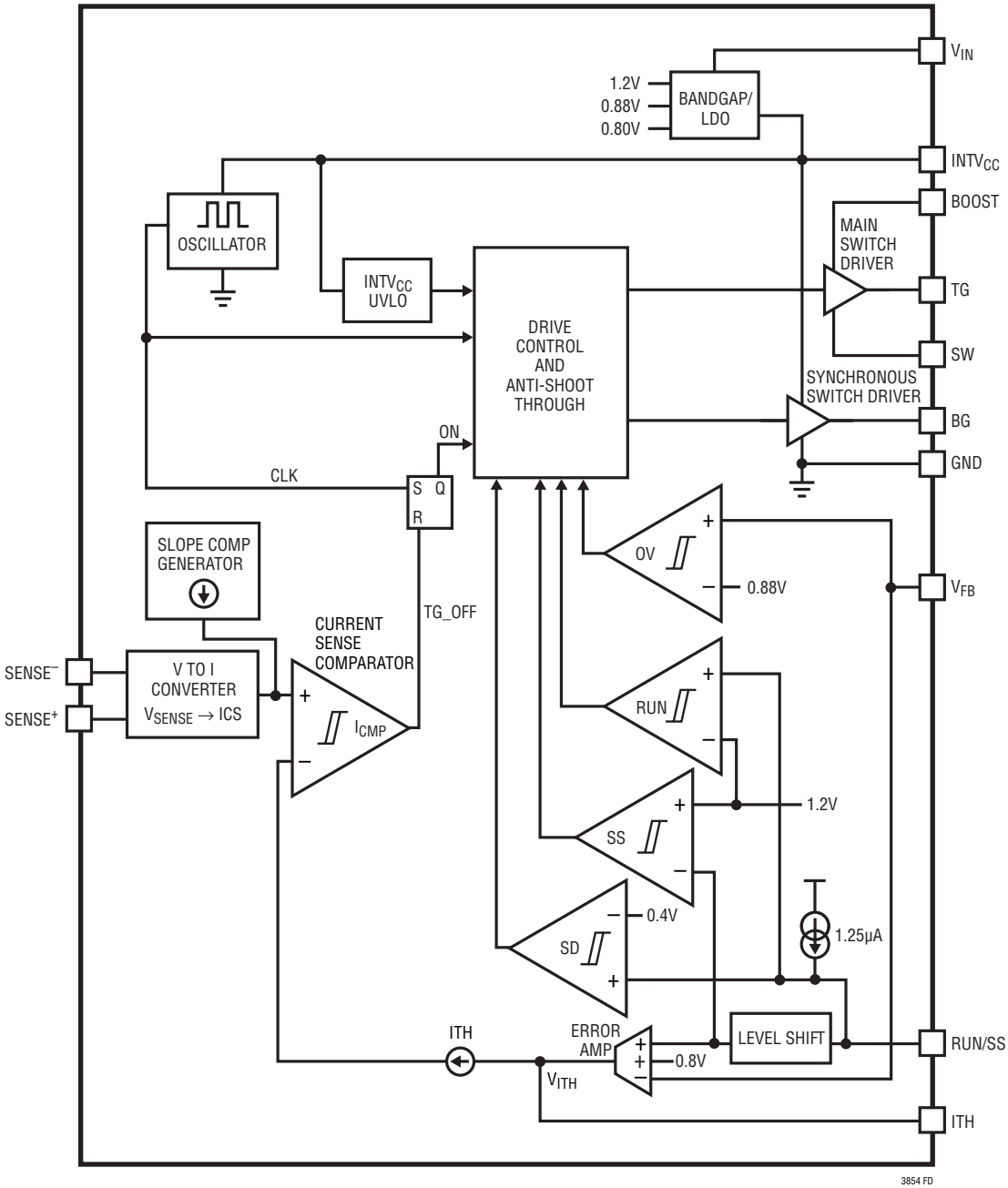
V_{IN} (Pin 10): Main Supply Pin. A bypass capacitor should be tied between this pin and the signal ground pin.

$SENSE^-$ (Pin 11): The (–) Input to the Differential Current Comparator.

$SENSE^+$ (Pin 12): The (+) Input to the Differential Current Comparator. The ITH pin voltage and controlled offsets between the $SENSE^-$ and $SENSE^+$ pins in conjunction with R_{SENSE} (or R_{DCR}) set the peak current trip threshold.

SGND (Exposed Pad Pin 13): The exposed pad must be soldered to PCB ground for electrical contact and rated thermal performance.

FUNCTIONAL DIAGRAM



OPERATION

Main Control Loop

The LTC3854 is a constant-frequency, peak current mode step-down controller. During normal operation, the top MOSFET is turned on when the clock sets the RS latch, and is turned off when the main current comparator, I_{CMP}, resets the RS latch. The peak inductor current at which I_{CMP} resets the RS latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier EA. The V_{FB} pin receives the voltage feedback signal, which is compared to the internal reference voltage by the EA. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.8V reference, which in turn causes the ITH voltage to increase until the average inductor current matches the new load current. After the top MOSFET has turned off, the bottom MOSFET is turned on until the beginning of the next cycle.

$INTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. An internal 5V low dropout linear regulator supplies $INTV_{CC}$ power from V_{IN}.

The top MOSFET driver is biased from a floating bootstrap capacitor C_B, which recharges during each off cycle through an external Schottky diode when the top MOSFET turns off. If the input voltage V_{IN} decreases to a voltage close to V_{OUT}, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector then forces the top MOSFET off for 1/10 of the clock period every fourth cycle to allow C_B to recharge.

Shutdown and Start-Up (RUN/SS)

The LTC3854 is shut down using the RUN/SS pin. Pulling this pin below 1.2V disables the controller and most of the internal circuitry, including the $INTV_{CC}$ regulator.

However, for RUN/SS>0.8V the internal bandgap is functional and the input current will be greater than the minimum shutdown current. To keep the part in a true shutdown mode the RUN/SS pin should be held below 0.4V. Releasing RUN/SS pin allows an internal 1.25µA current to pull up the pin and enable the controller. Alternatively, the RUN/SS pin may be externally pulled up or driven directly by logic. Be careful not to exceed the Absolute Maximum Rating of 6V on this pin.

The start-up of the controller's output voltage V_{OUT} is governed by the voltage on the RUN/SS pin until RUN/SS > 2V.

When the voltage on the RUN/SS pin is greater than 1.2V and less than 2V the LTC3854 regulates the V_{FB} voltage to 1.2V below the RUN/SS pin voltage. The RUN/SS pin programs the soft-start period through an external capacitor from the RUN/SS pin to GND. An internal 1.25µA pull-up current charges this capacitor creating a voltage ramp on the RUN/SS pin. As the RUN/SS voltage rises linearly from 1.2V to 2V, V_{OUT} rises smoothly from zero to the target output voltage. When the LTC3854 is in undervoltage lockout the external MOSFETs are held off.

Frequency of Operation

The LTC3854 operates at a fixed frequency of 400kHz.

Output Overvoltage Protection

An overvoltage comparator, OV, guards against transient overshoots (>10%) as well as other more serious conditions that may overvoltage the output. In such cases, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

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The LTC3854 can be configured to use either DCR (inductor winding resistance) sensing or low value resistor sensing. The choice of the two current sensing schemes is largely a design tradeoff between cost, power consumption, and accuracy. DCR sensing is becoming popular because it eliminates expensive current sensing resistors and is more power efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. Other external component selection is driven by the load requirement, and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and inductor value. Next, the power MOSFETs and Schottky diodes are selected. Finally, input and output capacitors are selected. The Typical Application shown on the first page can be configured for operation up to 38V on V_{IN}.

SENSE+ and SENSE– Pins

The SENSE+ and SENSE– pins are the inputs to the current comparator. The common mode input voltage range of the current comparator is 0V to 5.5V. Both SENSE pins are high impedance inputs with small input bias currents of less than 1µA. When the SENSE pins ramp up from 0V to 1.4V, small bias currents flow out of the SENSE pins. When the SENSE pins ramp down from 5.5V to 1.1V, the small bias currents flow into the SENSE pins. The high impedance inputs to the current comparator allow accurate DCR sensing.

Using a Sense Resistor for Current Sensing

A typical sensing circuit using a discrete resistor is shown in Figure 1. R_{SENSE} is chosen based on the required output current.

The current comparator has a maximum threshold of 50mV. The input common mode range of the current comparator is 0V to 5.5V. The current comparator threshold sets the peak of the inductor current, yielding a maximum average output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current, ΔI_L. Allowing a margin of 20% for variations in the IC and external component values yields:

$$R_{SENSE} = 0.8 \bullet \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

Inductor DCR Sensing

For applications requiring the highest possible efficiency, the LTC3854 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 2. The DCR of the inductor represents the small amount of DC copper winding resistance, which can be less than 1mΩ for today's low value, high current inductors. When the external R1||R2•C1 time constant is chosen to be equal to the L/DCR time constant, the voltage drop across the external

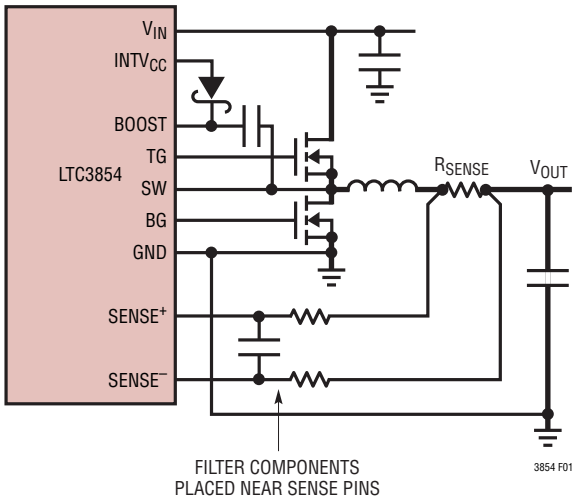

Figure 1. Using a Resistor to Sense Current with the LTC3854

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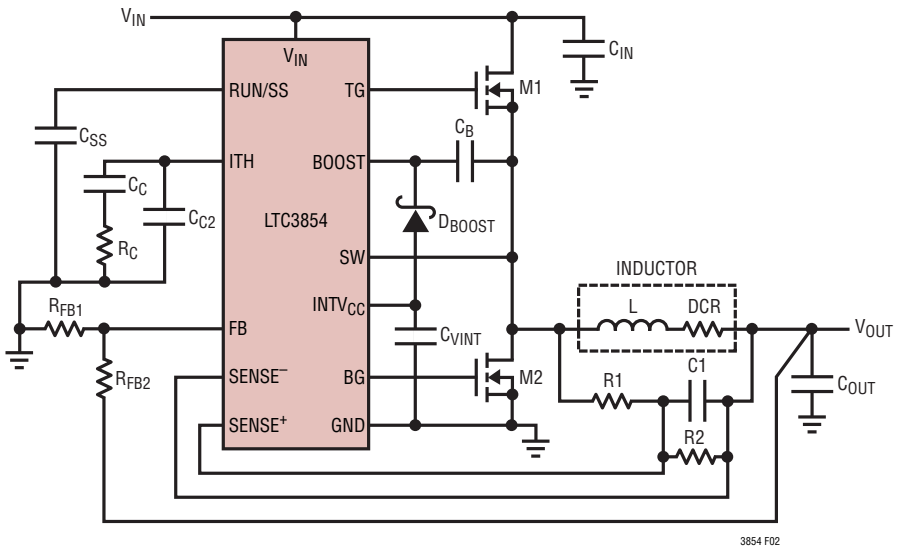

Figure 2. Buck Regulator Using DCR Current Sense

capacitor is equal to the voltage drop across the inductor DCR • R2/(R1+R2). R2 may be used to scale the voltage across the same terminals when the DCR is greater than the target sense resistance. Check the manufacturer's datasheet for specifications regarding the inductor DCR, in order to properly dimension the external filter components. The DCR of the inductor can also be measured using a precision RLC meter.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant-frequency architectures by preventing subharmonic oscillations at high duty cycles. It is accomplished internally by adding a compensating ramp to the inductor current signal. Normally, this results in a reduction of maximum inductor peak current for high duty cycles. However, the LTC3854 uses a novel scheme that allows the maximum inductor peak current to remain unaffected throughout all duty cycles.

Inductor Value Calculation

The inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance or frequency and increases with higher V_{IN}.

$$L_{MIN} = \frac{1}{\Delta I_L \bullet f_{SW}} \bullet V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Accepting larger values of ΔI_L allows the use of low value inductors, but results in a higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $I_L = 0.4 \bullet (I_{MAX})$. The maximum ΔI_L occurs at the maximum input voltage.

Option 1: DCR within desired range

$$R1 \bullet C1 = \frac{L}{DCR} \text{ (R2 not used)}$$

Option 2: DCR > desired R_{SENSE}

$$R1||R2 \bullet C1 = \frac{L}{DCR} \text{ (at 20°C)}$$

$$R_{SENSE}(EQ) = DCR(MAX) \bullet \frac{R2}{R1+R2}$$

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Inductor Core Selection

Once the value for L is determined, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies; allowing design goals to concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Power MOSFET and Schottky Diode (Optional) Selection

Two external power MOSFETs must be selected for the LTC3854 controller: one N-channel MOSFET for the top (main) switch, and one N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak drive levels are set by the $INTV_{CC}$ voltage. This voltage is 5V during start-up. Consequently, logic-level threshold MOSFETs can be used in most applications. The only exception is if low input voltage is expected (V_{IN} < 5V); then, sub-logic level threshold MOSFETs ($V_{GS(TH)}$ < 3V) should be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; most of the logic level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the on-resistance $R_{DS(ON)}$, Miller capacitance C_{MILLER}, input voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in V_{DS}. This result is then multiplied by the ratio of the applied V_{DS} to the gate charge curve specified V_{DS}. When the IC is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}} = D$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}} = 1 - D$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)} + (V_{IN})^2\left(\frac{I_{MAX}}{2}\right)(R_{DR})(C_{MILLER})\bullet\left[\frac{1}{V_{INTVCC} - V_{TH(MIN)}} + \frac{1}{V_{TH(MIN)}}\right](f)$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ and R_{DR} (approximately 2Ω) is the effective driver resistance at the MOSFET's Miller threshold voltage. $V_{TH(MIN)}$ is the typical MOSFET minimum threshold voltage.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which are highest at high input voltages. For V_{IN} < 20V, the high current efficiency generally improves with larger MOSFETs, while for V_{IN} > 20V the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during short-circuit when the synchronous switch is on close to 100% of the period.

The term (1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but δ = 0.005/°C can be used as an approximation for low voltage MOSFETs.

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An optional Schottky diode connected from GND (anode) to the SW node (cathode) conducts during the dead time between the conduction of the two power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on, storing charge during the dead time and requiring a reverse recovery period that could cost as much as 3% in efficiency at high V_{IN}. A 1A to 3A Schottky is generally a good size due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance.

Soft-Start

When the LTC3854 is configured to soft-start by itself, a capacitor must be connected to the RUN/SS pin. The LTC3854 is in the shutdown state if the RUN/SS pin voltage is below 1.2V. The RUN/SS pin has an internal 1.25µA pull-up current and should be externally pulled low (<0.4V) to keep IC in shutdown mode.

Once the RUN/SS pin voltage reaches 1.2V, the LTC3854 is enabled. As the RUN/SS pin moves from 1.2V to 2V the LTC3854 operates in a forced discontinuous mode with the bottom gate turning on only one time for every four clock cycles to allow the output to come up to its required value. During this time the error amp compares the FB pin to a level shifted version of the RUN/SS pin allowing the output to come up in a controlled fashion. Current foldback is disabled during this phase to ensure smooth soft-start or tracking. Once the RUN/SS pin is greater than 2V the LTC3854 operates in forced continuous mode. The LTC3854 output voltage is soft-start controlled when RUN/SS is between 1.2V and 2V. The total soft-start time can be calculated as:

$$t_{SOFT\text{-}START} = 0.8 \bullet \frac{C_{SS}}{1.25\mu A}$$

If the RUN/SS pin is externally driven beyond 2V (5V is recommended) the soft-start feature is disabled and the LTC3854 will immediately go into forced continuous mode. Care must be taken to insure the RUN/SS pin has either a capacitor tied to it or is driven externally. **Do not let this pin float.**

$INTV_{CC}$ Regulator

The LTC3854 features a PMOS low dropout linear regulator (LDO) that supplies power to $INTV_{CC}$ from the V_{IN} supply. $INTV_{CC}$ powers the gate drivers and much of the LTC3854's internal circuitry. The LDO regulates the voltage at the $INTV_{CC}$ pin to 5V when V_{IN} is greater than 6V.

The LDO supplies a peak current of 40mA and must be bypassed to ground with a minimum of 2.2µF low ESR ceramic capacitor. Good bypassing is needed to supply the high transient currents required by the MOSFET gate-drivers.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3854 to be exceeded. The $INTV_{CC}$ current, which is dominated by the gate-charge current, is supplied by the 5V LDO.

Power dissipation for the IC in this case is highest and is equal to $V_{IN} \bullet I_{INTVCC}$. The gate-charge current is dependent on operating frequency (400kHz), and the Q_G of the power MOSFETs, as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 3 of the Electrical Characteristics section. For example, if the LTC3854 $INTV_{CC}$ current is limited to less than 17mA from a 36V supply in the DFN package; then the junction temperature is:

$$T_J = 70°C + [(17mA \bullet 36V) \bullet (76°C/W)] = 116.5°C$$

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked during operation at maximum V_{IN}.

Topside MOSFET Driver Supply (C_B, DB)

An external bootstrap capacitor C_B connected from the BOOST pin to the SW pin and supplies the gate drive voltage for the topside MOSFET. Capacitor C_B in the Functional Diagram is charged though external diode DB from $INTV_{CC}$ when the SW pin is low. When the topside MOSFET is to be turned on, the driver places the C_B voltage across the gate source of the MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{INTVCC}$. The value of the boost

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capacitor C_B needs to be at least 100 times that of the total input capacitance of the topside MOSFET. The reverse breakdown of the external Schottky diode must be greater than $V_{IN(MAX)}$. When adjusting the gate-drive level, the final arbiter is the total input current for the regulator. If a change is made and the input current decreases, then the efficiency has improved. If there is no change in input current, then there is no change in efficiency.

Undervoltage Lockout

The LTC3854 has two functions that help protect the controller in case of undervoltage conditions. A precision UVLO comparator constantly monitors the $INTV_{CC}$ voltage to ensure that an adequate gate-drive voltage is present. Switching action is disabled when $INTV_{CC}$ is below 3.5V. To prevent oscillation caused by a disturbance on $INTV_{CC}$, the UVLO comparator has 350mV of hysteresis.

Another way to detect an undervoltage condition is to monitor the V_{IN} supply. The RUN/SS pin has a precision turn-on reference of 1.2V, enabling a resistor divider to V_{IN} to turn on the IC when V_{IN} is above the desired value.

It is recommended that the resistor divider be used if the input voltage will be quickly cycled on and off.

C_{IN} Selection

In forced continuous mode, the source current of the top N-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used.

$$I_{RMS} = \frac{I_{OUT}}{2}$$

The maximum RMS capacitor current is:

$$I_{RMS} = \frac{I_{MAX}}{V_{IN}}\left[\left(V_{OUT}\right)\bullet\left(V_{IN} - V_{OUT}\right)\right]^{1/2}$$

This formula has a maximum at $V_{IN} = 2\bullet V_{OUT}$, where $I_{RMS} = I_{OUT}/2$.

This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question.

C_{OUT} Selection

The selection of C_{OUT} is primarily determined by the effective series resistance (ESR) to minimize voltage ripple. The output ripple (ΔV_{OUT}) in continuous mode is:

$$\Delta V_{OUT} = \Delta I_L\left(ESR + \frac{1}{8\bullet f_{SW}\bullet C_{OUT}}\right)$$

Where f_{SW} = 400kHz, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. With $\Delta I_L = 0.3 I_{OUT(MAX)}$ and allowing 2/3 of the ripple due to ESR, the output ripple will be less than 50mV at max V_{IN} assuming:

$$C_{OUT}\ \text{Required ESR} < 2.2\ R_{SENSE}$$

$$C_{OUT} > \frac{1}{8 f_{SW} R_{SENSE}}$$

The first condition relates to the ripple current into the ESR of the output capacitance while the second term guarantees that the output capacitance does not significantly discharge during the operating frequency period due to ripple current. The choice of smaller output capacitance increases the ripple voltage due to the discharging term but can be compensated with capacitors of very low ESR to maintain the ripple voltage at or below 50mV. The I_{TH} pin OPTI-LOOP compensation components can be optimized to provide stable, high performance transient response regardless of the output capacitors selected. The selection of output capacitors for applications with large load current transients is primarily determined by the voltage tolerance specifications of the load. The resistive component of the capacitor, ESR, multiplied by the load current change plus any output voltage ripple must be within the voltage tolerance of the load.

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The required ESR due to a load current step is:

$$ESR \leq \frac{\Delta V}{\Delta I}$$

where ΔI is the change in current from full load to zero load (or minimum load) and ΔV is the allowed voltage deviation (not including any droop due to finite capacitance).

The amount of capacitance needed is determined by the maximum energy stored in the inductor. The capacitance must be sufficient to absorb the change in inductor current when a high current to low current transition occurs. The opposite load current transition is generally determined by the control loop OPTI-LOOP components, so make sure not to over compensate and slow down the response. The minimum capacitance to assure the inductors' energy is adequately absorbed is:

$$C_{OUT} > \frac{L(\Delta I)^2}{2(\Delta V)V_{OUT}}$$

Manufacturers such as Nichicon, United Chemi-Con and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor electrolyte capacitor available from Sanyo has the lowest (ESR)(size) product of any aluminum electrolytic at a somewhat higher price. An additional ceramic capacitor in parallel with OS-CON capacitors is recommended to reduce the inductive effects.

In surface mount applications, ESR, RMS current handling and load step specifications may require multiple capacitors in parallel. Aluminum electrolytic, dry tantalum and special polymer capacitors are available in surface mount packages. Special polymer surface mount capacitors offer very low ESR but have much lower capacitive density per unit volume than other capacitor types. These capacitors offer a very cost-effective output capacitor solution and are an ideal choice when combined with a controller having high loop bandwidth. Tantalum capacitors offer the highest capacitance density and are often used as output capacitors for switching regulators having controlled soft-start. Several excellent surge-tested choices are the AVX TPS, AVX TPSV or the KEMET T51 0 series of surface mount tantalums, available in case heights ranging from 1.5mm to 4.1mm. Aluminum electrolytic capacitors can be used in cost-driven applications, provided that consideration is given to ripple current ratings, temperature and long-term reliability. A typical application will require several aluminum electrolytic capacitors in parallel. A combination of the above mentioned capacitors will often result in maximizing performance and minimizing overall cost. Other capacitor types include Nichicon PL series, NEC Neocap, Panasonic SP and Sprague 595D series. Consult manufacturers for other specific recommendations.

Like all components, capacitors are not ideal. Each capacitor has its own benefits and limitations. Combinations of different capacitor types have proven to be a very cost effective solution. Remember also to include high frequency decoupling capacitors. They should be placed as close as possible to the power pins of the load. Any inductance present in the circuit board traces negates their usefulness.

Setting Output Voltage

The LTC3854 output voltage is set by an external feedback resistive divider carefully placed across the output, as shown in Figure 3. The regulated output voltage is determined by:

$$V_{OUT} = 0.8\left(1 + \frac{R_B}{R_A}\right)$$

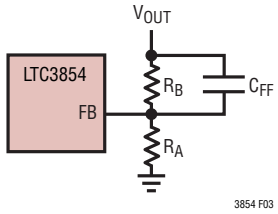

Figure 3. Feed-Forward Capacitor on FB Pin

To improve the frequency response, a feed-forward capacitor, C_{FF}, may be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

Fault Conditions: Current Foldback

The LTC3854 includes current foldback to help limit load current when the output is shorted to ground. If the output falls below 40% of its nominal output level, the maximum

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sense voltage is progressively lowered from its maximum programmed value to 25% of the maximum value. Foldback current limiting is disabled during soft-start.

Minimum and Maximum On-Time Considerations

Minimum on-time $t_{ON(MIN)}$ is the smallest time duration that the LTC3854 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that

$$\frac{V_{OUT}}{V_{IN} \bullet f_{SW}} > t_{ON(MIN)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase.

The minimum on-time for the LTC3854 is approximately 75ns. However, as the peak sense voltage decreases the minimum on-time gradually increases. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

Care should also be taken for applications where the duty cycle can approach the maximum given in the data sheet (98%). In all low dropout applications, such as V_{OUT} = 5V and $V_{IN(MIN)}$ = 4.5V, careful selection of the bottom synchronous MOSFET is required. For applications where the input voltage can drop below the targeted output voltage, and subsequently ramp up, a low threshold synchronous MOSFET with a small total gate charge should be chosen. This selection for the bottom synchronous MOSFET will insure that the bottom gate minimum on-time is sufficient in dropout to allow for the initial boost capacitor refresh that is needed to adequately turn on the top side driver and begin the switching cycle. Another method to guarantee performance in this type of application is to increase the minimum output load to 50mA. This minimum load will allow the user to choose larger MOSFETs for delivery of large currents when V_{IN} is in the normal operating range yet still provide an adequate safety margin and good overall performance in dropout with a slow ramping V_{IN}.

Efficiency Considerations

The efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

%Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3854 circuits: 1) IC V_{IN} current, 2) $INTV_{CC}$ regulator current, 3) I^2R losses, 4) Topside MOSFET transition losses.

1. The V_{IN} current is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents. V_{IN} current typically results in a small (<0.1%) loss.

2. $INTV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG}$ = $f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs.

3. I^2R losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor, current sense resistor. In continuous mode, the average output current flows through L and R_{SENSE}, but is "chopped" between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L and R_{SENSE} to obtain

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I^2R losses. For example, if each $R_{DS(ON)}$ = 10mΩ, DCR = 10mΩ, R_{SENSE} = 5mΩ then the total resistance is 25mΩ. This results in losses ranging from 2% to 8% as the output current increases from 3A to 15A for a 5V output, or a 3% to 12% loss for a 3.3V output. Efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

4. Transition losses apply only to the topside MOSFET(s), and become significant only when operating at high input voltages (typically 15V or greater). Transition losses can be estimated from:

   Transition Loss = $1.7V_{IN}^2 \bullet I_{O(MAX)} \bullet C_{RSS} \bullet f_S$

Other "hidden" losses such as copper trace and the battery internal resistance can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these "system" level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20µF to 40µF of capacitance having a maximum of 20mΩ to 50mΩ of ESR. Other losses including Schottky conduction losses during dead time and inductor core losses generally account for less than 2% total additional loss.

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \bullet$ ESR, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. The availability of the ITH pin not only allows optimization of control loop behavior but also provides a DC coupled and AC filtered closed loop response test point. The DC step, rise time and settling at this test point truly reflects the closed loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The ITH external components shown in the Typical Application circuit will provide an adequate starting point for most applications.

The ITH series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. Placing a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the ITH pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this

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sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3854. These items are also illustrated graphically in the layout diagram of Figure 4. Check the following in your layout:

1) Are the signal and power grounds segregated? The LTC3854 GND pin should tie to the ground plane close to the output capacitor(s). The low current or signal ground trace should make a single point connection directly to the GND pin. The synchronous MOSFET source pins should connect to the input capacitor(s) ground.

2) Does the V_{FB} pin connect directly to the feedback resistors? The resistive divider R1, R2 must be connected between the (+) plate of C_{OUT} and signal ground. The 47pF to 100pF capacitor should be as close as possible to the LTC3854. Be careful locating the feedback resistors too far away from the LTC3854. The V_{FB} line should not be routed close to any other nodes with high slew rates.

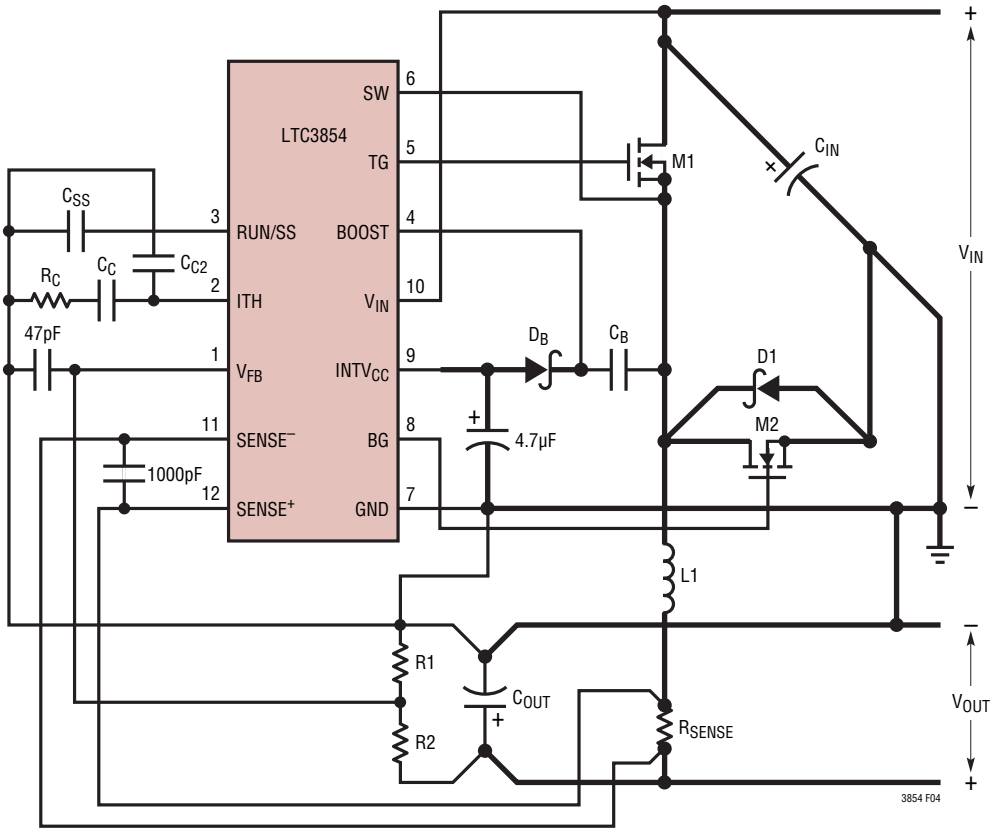


Figure 4. LTC3854 Layout Diagram

APPLICATIONS INFORMATION

3) Are the SENSE– and SENSE+ leads routed together with minimum PC trace spacing? The filter capacitor between SENSE+ and SENSE– should be as close as possible to the LTC3854. Ensure accurate current sensing with Kelvin connections as shown in Figure 5. Series resistance can be added to the SENSE lines to increase noise rejection.

4) Does the (+) terminal of C_{IN} connect to the drain of the topside MOSFET(s) as closely as possible? This capacitor provides the AC current to the MOSFET(s).

5) Is the $INTV_{CC}$ decoupling capacitor connected closely between $INTV_{CC}$ and GND? This capacitor carries the MOSFET driver peak currents.

6) Keep the switching node (SW), top gate node (TG), bottom gate node (BG) and boost node (BOOST) away from sensitive small-signal nodes, especially from the voltage and current sensing feedback pins. All of these nodes have very large and fast moving signals and therefore should be kept on the "output side" (Pins 4,5,6 and 8) of the LTC3854 GND and occupy minimum PC trace area.

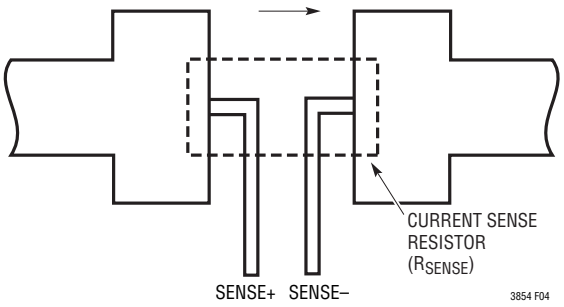


Figure 5. Kelvin Sensing R_{SENSE}

PC Board Layout Debugging

It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to dropout.

The duty cycle percentage should be maintained from cycle to cycle in a well-designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required. A 1Ω to 10Ω boost resistor may help to improve noise immunity. This resistor is placed between the BOOST pin and the node formed by the cathode of the boost Schottky and the positive terminal of the boost capacitor.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, Schottky and the top MOSFET components to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the GND pin of the IC.

APPLICATIONS INFORMATION

Design Example

Consider the design of a 1.2V, 15A buck regulator with a V_{IN} range of 4.5V to 28V using a DCR sensing scheme.

Inductor Selection

Assuming an inductor ripple of 40% of I_{OUT}, L can be calculated for the worst case of $V_{IN} = V_{IN(MAX)}$.

$$L_{MIN} = \frac{1}{\Delta I_L \bullet f_{SW}} \bullet V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

$$L_{MIN} = \frac{1}{0.40 \bullet 15A \bullet 400kHz} \bullet 1.2V \bullet \left(1 - \frac{1.2V}{20V}\right)$$

$$L_{MIN} = 0.47\mu H$$

Next, determine the DCR of the inductor. When provided, use the manufacturer's maximum value, usually given at 25°C. Increase this value to account for the temperature coefficient of resistance, which is approximately 0.4%/°C. A conservative value for TL_{MAX} is 100°C which corresponds to a delta of 0.3. To allow the converter to source 15A with an inductor temperature of 100°C without hitting maximum current limit we need a DCR at 25°C of:

$$DCR(25°C) = \frac{0.8 \bullet V_{SENSE(MAX)}}{\left(I_{MAX} + \frac{\Delta I_L}{2}\right) \bullet (1 + \delta)}$$

$$DCR(25°C) = \frac{0.8 \bullet 50mV}{\left(15A + \frac{15A \bullet 0.4}{2}\right) \bullet (1 + 0.3)}$$

$$DCR(25°C) = 1.7m\Omega$$

The 0.56µH inductor from the IHLP4040DZ-01 series has a typical DCR of 1.7mΩ and a maximum of 1.8mΩ and as I_{SAT} of 49A. The saturation current is well above our operating current maximum.

The maximum inductor will be the DC value plus one half the ripple current. Using this inductor gives an inductor ripple current of 6A (keeping the ripple current high will also help insure the minimum on-time requirement of 75ns is not violated).

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)} \bullet f_{SW}}$$

$$t_{ON(MIN)} = \frac{1.2V}{20V \bullet 400kHz}$$

$$t_{ON(MIN)} = 150ns$$

To choose R1 for DCR sensing we use:

$$R1 \bullet C1 = \frac{L}{DCR} \text{ at } 25°C$$

Choosing C1 = 100nF and using the maximum DCR value at 25°C, we get:

$$R1 = \frac{0.56\mu H}{1.8m\Omega \bullet 100nF}$$

$$R1 = 3.11k$$

Choose 3.09k.

Output Capacitor Selection

The output voltage AC ripple due to capacitive impedance and ESR in normal continuous mode operation can be calculated from:

$$\Delta V_{OUT} = \Delta I_L \left(ESR + \frac{1}{8 \bullet f_{SW} \bullet C_{OUT}}\right)$$

The second term is the AC capacitive impedance part of the above equation and used alone will yield a minimum C_{OUT} of:

$$C_{OUT} > \frac{\Delta I_L}{8 \bullet f_{SW} \bullet \Delta V_{OUT}}$$

$$C_{OUT} > \frac{0.4 \bullet 15A}{8 \bullet 400kHz \bullet 0.01 \bullet 1.2V}$$

$$C_{OUT} > 156\mu F$$

APPLICATIONS INFORMATION

However, the amount of capacitance needed is determined not only by the allowed ripple in steady state but by the maximum energy stored in the inductor. The capacitance must be sufficient in value to absorb the change in inductor current when a high current to low current transient occurs. The minimum capacitance to assure the inductor's energy is adequately absorbed during a 5A load step for a maximum overshoot of 2% is:

$$C_{OUT} \geq \frac{L \bullet \Delta I_L^{\,2}}{2 \bullet \Delta V_{OUT} \bullet V_{OUT}}$$

$$C_{OUT} \geq \frac{0.56\mu H \bullet (5A)^2}{0.02 \bullet 1.2V}$$

$$C_{OUT} \geq 583\mu F$$

A maximum overshoot or undershoot of 2% for a 5A load step will require an ESR of:

$$ESR < 0.02 \bullet \frac{V_{OUT}}{\Delta I_{LOAD}} = 0.02 \bullet \frac{1.2V}{5A} \leq 5m\Omega$$

Several quality capacitors are available with low enough ESR.

Multilayer ceramic capacitors tend to have very low ESR values. It is also a good practice to reduce the ESL by putting several capacitors in parallel on the output (a parallel bank of larger and smaller capacitors will improve performance in both a DC and a transient condition).

To keep ripple very low and design for any possible large excursions in current 2x 330µF (tantalum or polymer surface) and 1x 47µF polymer low ESR type were connected in parallel.

Choosing FB Resistors (See Figure 3)

$$V_{OUT} = 0.8\left(1 + \frac{R_B}{R_A}\right)$$

$$R_B = 0.5R_A$$

Using 1% 10.0k for R_A gives 1% 4.99k for R_B.

Choosing C_{IN} Capacitors

C_{IN} is chosen for a RMS current rating of at least $I_{OUT(MAX)}/2$ = 6A. Again, keeping ESR low will improve performance and reduce power loss (several capacitors in parallel is once again a good choice). We will use an 180µF 25V electrolytic with 2x 10µF 25V low ESR ceramic capacitors connected in parallel.

Choosing MOSFETs

The power dissipation in the main and synchronous FETs can be easily estimated. Choosing a Renesas RJK0305DPB for the main FET results in the following parameters:

BV_{DSS} = 30V

$R_{DS(ON)}$ = 13mΩ maximum at 25°C, V_{GS} = 4.5V

Q_{GD} = 1.5nC at V_{DS}, test 10V results in C_{MILLER} = 1.5nC/10V = 150pF

Q_G = 8nC, typical, at V_{GS} = 4.5V

V_{MILLER} = 2.8V

At V_{IN} = 20V, I_{OUT} = 15A, estimated T_J = 100°C for the top FET and given

V_{INTVCC} = 5.0V

$R_{DR,PULLUP}$ = 2.6Ω

$R_{DR,PULLDOWN}$ = 1.5Ω

the total losses in the main FET will be:

$$P_{MAIN} = \frac{1.2V}{20V} \bullet (15A)^2 \bullet \left(1 + 0.005 \bullet (100°C - 25°C)\right) \bullet 13m\Omega + (20V)^2 \bullet \frac{15A}{2} \bullet 150pF \bullet \left(\frac{2.5\Omega}{5V - 2.8V} + \frac{1.2\Omega}{2.8V}\right) \bullet f_{SW}$$

$$P_{MAIN} = 0.55W$$

APPLICATIONS INFORMATION

Choosing an RJK0330DPB for the bottom FET will provide:

BV_{DSS} = 30V

$R_{DS(ON)}$ = 3.9mΩ maximum at 25°C, V_{GS} = 4.5V

Q_G = 27nC, typical, at V_{GS} = 4.5V

$$P_{SYNC} = \frac{20V - 1.2V}{20V} \bullet (15A)^2 \bullet (1 + 0.005 \bullet (100°C - 25°C)) \bullet 3.9m\Omega$$

$$P_{SYNC} = 1.1W$$

Assuming a thermal resistance of 40°C/W for the main and synchronous FETs, the resulting junction temperatures at an ambient of 60°C will be 82°C and 104°C, respectively. Some airflow may be required for higher ambient temperatures. A maximum MOSFET junction temperature of 110°C at worst case ambient generally provides adequate margin.

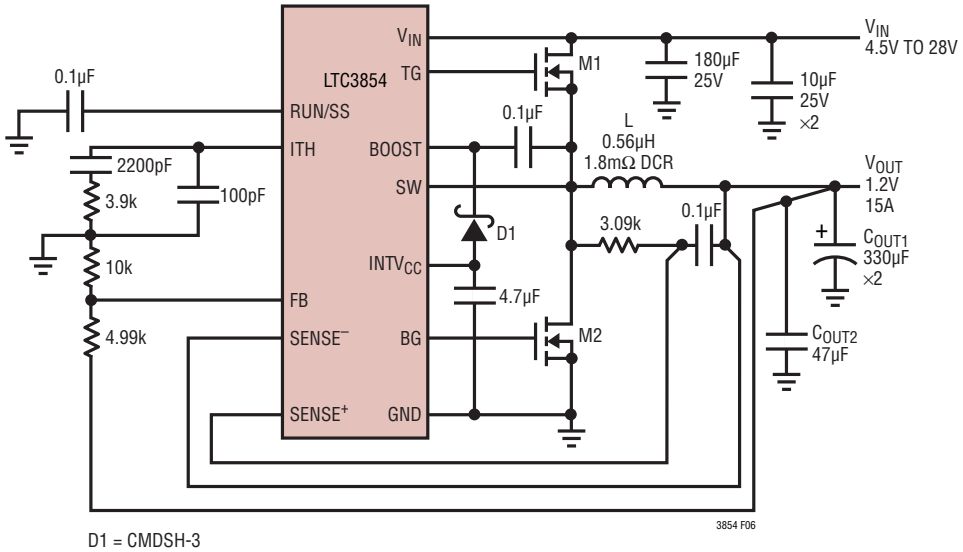
Given a typical Q_G of 8nC for the RJK0305DPB and 27nC for the RJK0330DPB and the 400kHz switching frequency, the current supplied by $INTV_{CC}$ will be:

$I_{GATECHG}$ = (8nC + 27nC) • 400kHz = 14mA

The resulting controller temperature at 60°C and a 20V input will be:

T_J = 60°C + 20V • 14mA • 76°C/W = 81°C

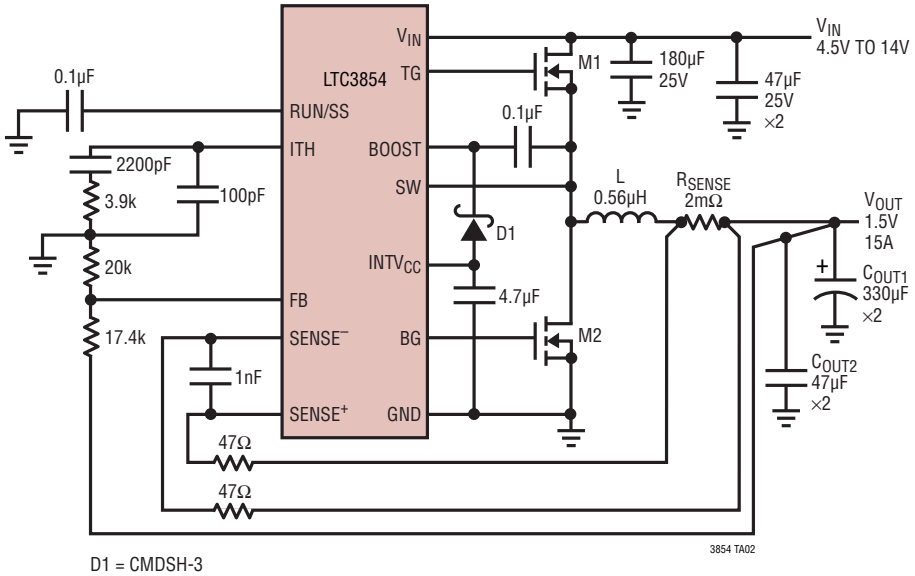
which is well under the maximum junction temperature of 125°C.



D1 = CMDSH-3
M1 = RENESAS RJK0305DPB
M2 = RENESAS RJK0330DPB
L = VISHAY IHLP4040DZ-01 0.56µH
C_{OUT1} = SANYO 2R5TPE330M9
C_{OUT2} = MURATA GRM31CR60J476K

Figure 6. 1.2V/15A Converter from Design Example

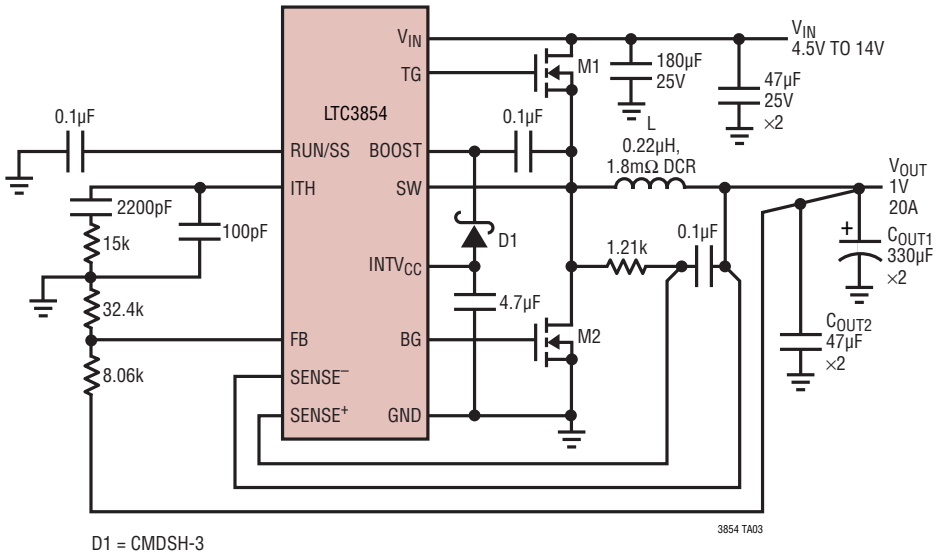
TYPICAL APPLICATIONS



D1 = CMDSH-3
M1 = RENESAS RJK0305DPB
M2 = RENESAS RJK0330DPB
L = TOKO FDA1055-R56M
C_{OUT1} = SANYO 2R5TPE330M9
C_{OUT2} = MURATA GRM31CR60J476K

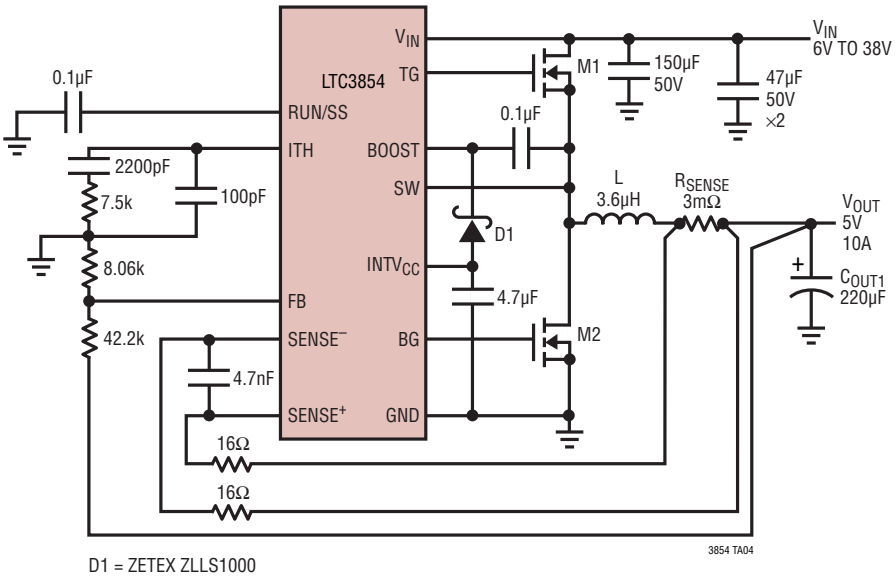
Figure 7. 1.5V/15A R_{SENSE} Application

TYPICAL APPLICATIONS



D1 = CMDSH-3
M1, M2 = VISHAY Si7866ADP
L = SUMIDA CDEP104NP-0R2NC
C_{OUT1} = SANYO 2RSTPE330M9
C_{OUT2} = MURATA GRM31CR60J476K

Figure 8. 1.0V/20A DCR Sense Application

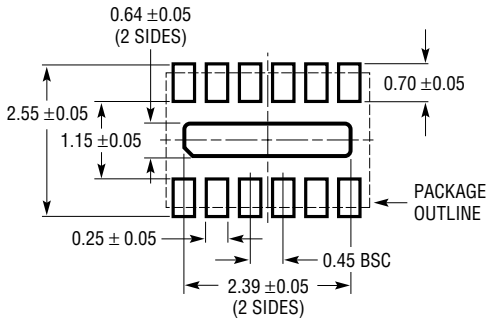


D1 = ZETEX ZLLS1000
M1, M2 = INFINEON BSC093N04LS
L = COILTRONICS HC1-3R6-R
C_{OUT1} = SANYO 6TPE220MI

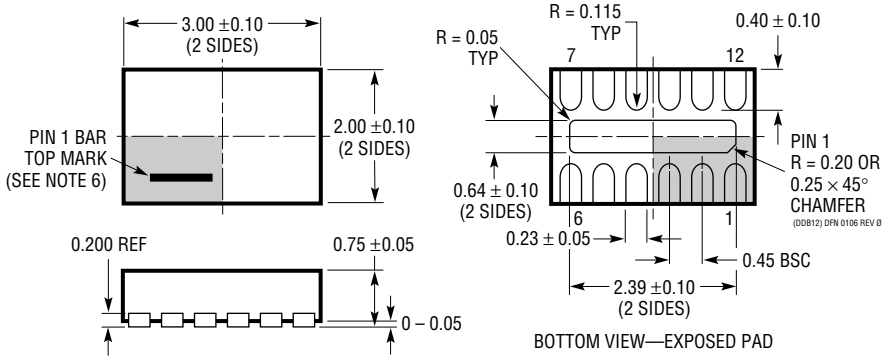
Figure 9. 5.0V/10A R_{SENSE} Application

PACKAGE DESCRIPTION

DDB Package
12-Lead Plastic DFN
(Reference LTC DWG # 05-08-1723 Rev Ø)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

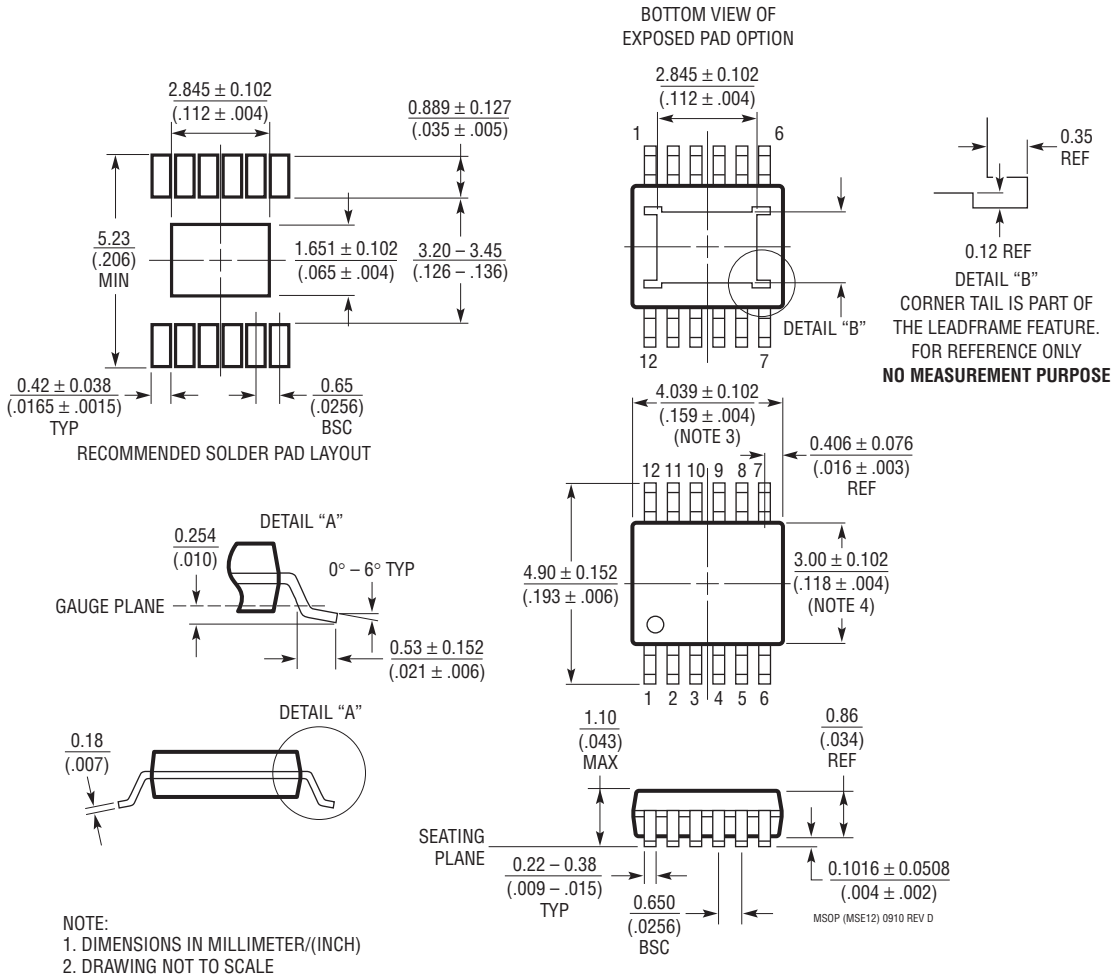


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

MSE Package
12-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1666 Rev D)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/09	Edits to Typical Application	1
		Updated Efficiency Graph	1
		Edit to Electrical Characteristics and Notes	3, 4
		Text Changes to Pin Functions	7
		Change to Functional Diagram	8
		Updated Related Parts Table	28
B	2/11	Updated TG R_{DOWN} and BG R_{DOWN} Typical values	3
		Updated MSE package from Rev B to Rev D	26