Virtual Remote Sense Controller

FEATURES

- **Tight Load Regulation with Highly Resistive Cables without Requiring Remote Sense Wiring**
- Compatible with Isolated and Nonisolated Power Supplies
- ±1% Internal Voltage Reference
- 5mA Sink Current Capability
- Soft-Correct Reduces Turn-On Transients
- Undervoltage and Overvoltage Protection
- Pin-Programmable Dither Frequency
- Optional Spread Spectrum Dither
- Wide V_{IN} Range: 3.1V to 50V
- 24-Lead SSOP Package

APPLICATIONS

- 12V High Intensity Lamps
- 28V Industrial Systems
- High Power (>40 Watts) CAT5 Cable Systems
- Wiring Drop Cancellation for Notebook Computer Battery Charging
- AC and DC Adaptors
- Well-Logging and Other Remote Instrumentation
- Surveillance Equipment

DESCRIPTION

The LT®4180 solves the problem of providing tight load regulation over long, highly resistive cables without requiring an additional pair of remote sense wires. This Virtual Remote Sense™ device continuously interrogates the line impedance and corrects the power supply output voltage via its feedback loop to maintain a steady voltage at the load regardless of current changes.

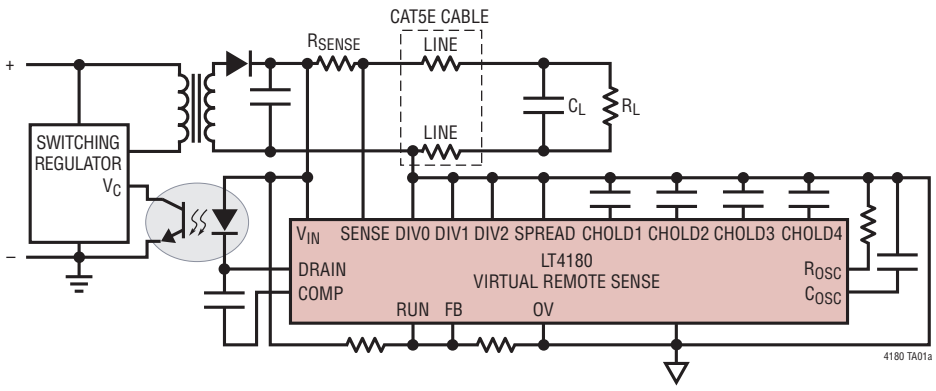
The LT4180 is a full-featured controller with 5mA opto-isolator sink capability, under/overvoltage lockout, soft-start and a ±1% internal voltage reference. The Virtual Remote Sense feature set includes user-programmable dither frequency and optional spread spectrum dither.

The LT4180 works with any topology and type of isolated or nonisolated power supply, including DC/DC converters and adjustable linear regulators.

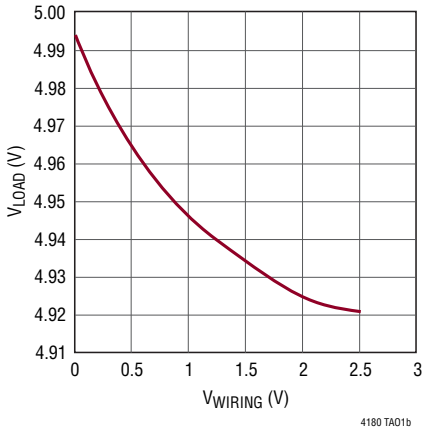
The LT4180 is available in a 24-lead, SSOP package.

TYPICAL APPLICATION

Isolated Power Supply with Virtual Remote Sense



V_{LOAD} vs V_{WIRE}

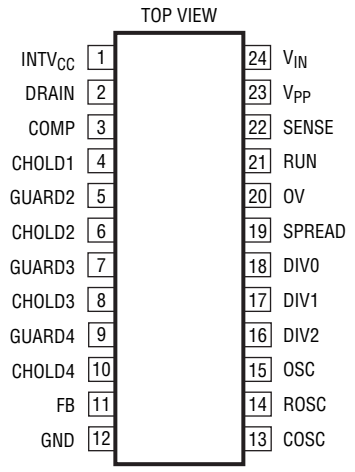


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} ..... –0.3V to 52V
SENSE..... V_{IN} – 0.3V to V_{IN}
INTVCC, RUN, FB, OV, ROSC, OSC,
DIV0, DIV1, DIV2, SPREAD, CHOLD1,
CHOLD2, CHOLD3, CHOLD4, DRAIN, COMP,
GUARD2, GUARD3, GUARD4, V_{PP} ..... –0.3V to 5.5V
V_{IN} Pin Current..... 10mA
INTVCC Pin Current ..... –10mA
COSC Pin Current..... 3.3mA
Maximum Junction Temperature ..... 125°C
Operating Junction Temperature Range (Note 2)
E-, I-Grades ..... –40°C to 125°C
MP-Grade ..... –55°C to 125°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



GN PACKAGE
24-LEAD NARROW PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 85°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT4180EGN#PBF	LT4180EGN#TRPBF	LT4180GN	24-Lead Narrow Plastic SSOP	–40°C to 125°C
LT4180IGN#PBF	LT4180IGN#TRPBF	LT4180GN	24-Lead Narrow Plastic SSOP	–40°C to 125°C
LT4180MPGN#PBF	LT4180MPGN#TRPBF	LT4180GN	24-Lead Narrow Plastic SSOP	–55°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = SENSE = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Supply Voltage		●	3.10		50	V
IV_{IN}	Input Quiescent Current	ROSC Open, COSC Open, SENSE = V_{IN}	●		1	2	mA
V_{REF}	Reference Voltage	V_{CHOLD2} = V_{CHOLD3} = 1.2V, Measured at CHOLD4 During Track ΔV_{OUT} Clock Phase	 ●	1.209 1.197	1.221 1.221	1.233 1.245	V V
I_{LIM}	Open-Drain Current Limit	With FB = V_{REF} + 200mV, OSC Stopped with Voltage Feedback Loop Closed		5	12	17	mA
V_{OL}	DRAIN Low Voltage	V_{IN} = 3V				0.3	V
V_{INTVCC}	LDO Regulator Output Voltage	V_{IN} = 5V			3.15		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = SENSE = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{INTVCC}	LDO Regulator Output Voltage in Dropout	V_{IN} = 2.5V	2.2			V
V_{OV}	Overvoltage Threshold	Rising		1.21		V
V_{OHYST}	Overvoltage Input Hysteresis	$V_{RISING} – V_{FALLING}$	15		80	mV
V_{RUN}	Run Threshold	Falling		1.21		V
V_{RHYST}	Run Input Hysteresis	$V_{RISING} – V_{FALLING}$	15		80	mV
I_{FB}	Input Bias Current		–0.2		0.2	µA
$A_{V(RATIO)}$	Current Amplifier Gain Ratio	A_{VL}/A_{VH}, A_V Measured in V/V	0.891	0.9	0.909	
I_{SENSE}	Current Amplifier Input Bias Current	Measured at SENSE with SENSE = V_{IN}	–1		1	µA
A_V	ΔV_{FB} Amplifier Gain		9.7	10	10.3	V/V
I_{CHOLD1}	Track/Hold Charging Current	Measured at CHOLD1 with V_{CHOLD1} = 1.2V		±60		µA
I_{CHOLD2}	Track/Hold Charging Current	Measured at CHOLD2 with V_{CHOLD2} = 1.2V		±25		µA
I_{CHOLD3}	Track/Hold Charging Current	Measured at CHOLD3 with V_{CHOLD3} = 1.2V		±25		µA
I_{CHOLD4}	Track/Hold Charging Current	Measured at CHOLD4 with V_{CHOLD4} = 1.5V, V_{CHOLD2} = 1V, V_{CHOLD3} = 1.2V		10		µA
		Measured at CHOLD4 with V_{CHOLD4} = 1.5V, V_{CHOLD2} = 1.4V, V_{CHOLD3} = 1.2V		–200		µA
I_{SC}	Soft-Correct Current	Measured at CHOLD4			±1.5	µA
I_{LKG1}	Track/Hold Leakage Current	Measured at CHOLD1 with V_{CHOLD1} = 1.2V			±1	µA
I_{LKG2}	Track/Hold Leakage Current	Measured at CHOLD2 with V_{CHOLD2} = 1.2V			±1	µA
I_{LKG3}	Track/Hold Leakage Current	Measured at CHOLD3 with V_{CHOLD3} = 1.2V			±1	µA
I_{LKG4}	Track/Hold Leakage Current	Measured at CHOLD4 with V_{CHOLD4} = 1.2V			±1	µA
f_{OSC}	Oscillator Frequency	R_{OSC} = 20k, C_{OSC} = 1nF	170	200	230	kHz
g_{mFB}	Voltage Error Amplifier Transconductance	Measured from FB to COMP, V_{COMP} = 2V, OSC Stopped with Voltage Feedback Loop Closed		120		µmho
g_{mIAMP}	Current Amplifier Transconductance	Measured from SENSE to COMP, V_{COMP} = 2V, OSC Stopped with Current Feedback Loop Closed		700		µmho

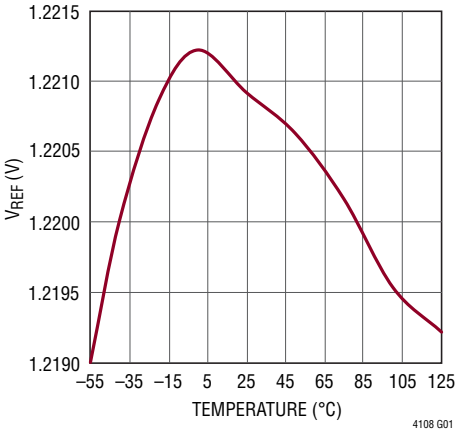
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. The LT4180E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design characterization and correlation with statistical process controls. The LT4180I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT4180MP is guaranteed over the full –55°C to 125°C operating junction temperature range.

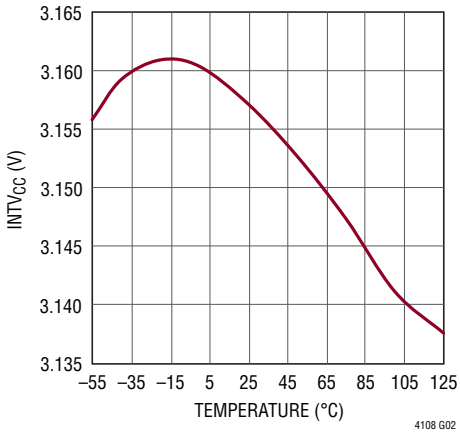
Note 3. Positive current is defined as flowing into a pin.

TYPICAL PERFORMANCE CHARACTERISTICS

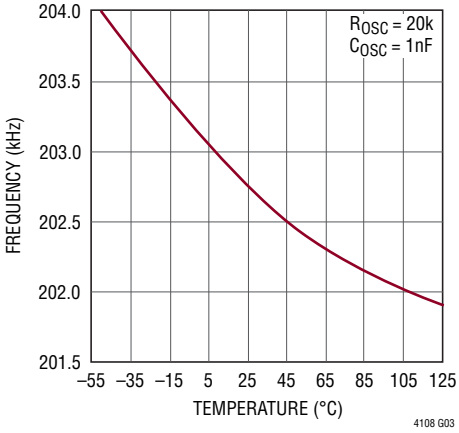
V_{REF} vs Temperature



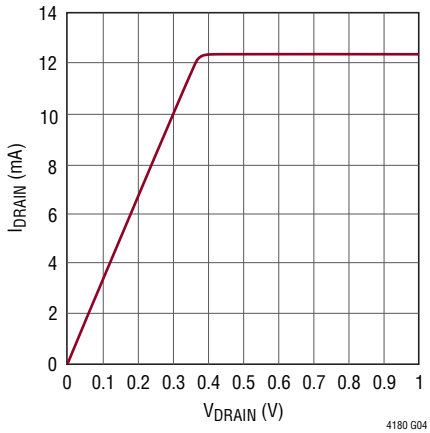
$INTV_{CC}$ vs Temperature



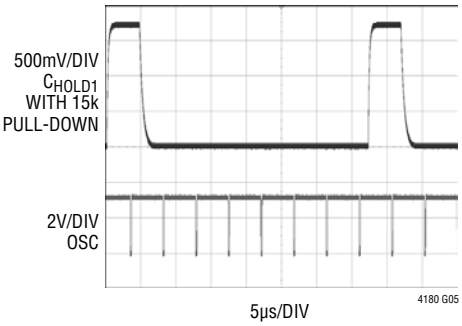
Oscillator Frequency vs Temperature



I_{DRAIN} vs V_{DRAIN}



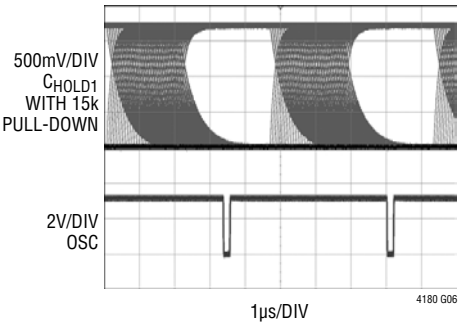
Normal Timing



5µs/DIV

TRIGGERED ON CHOLD1

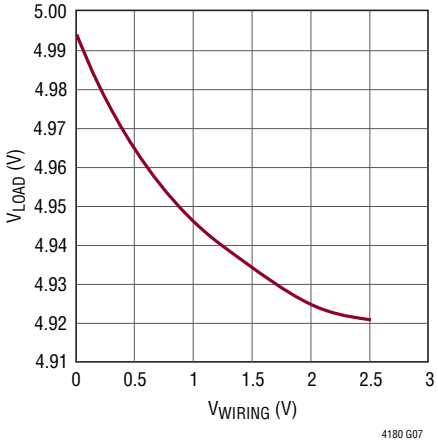
Spread Spectrum Timing



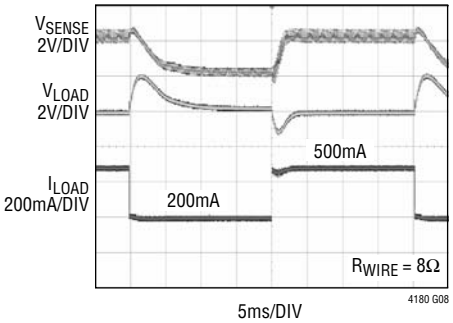
1µs/DIV

TRIGGERED ON OSC

V_{LOAD} vs V_{WIRE}



Load Step in 12V Linear Application

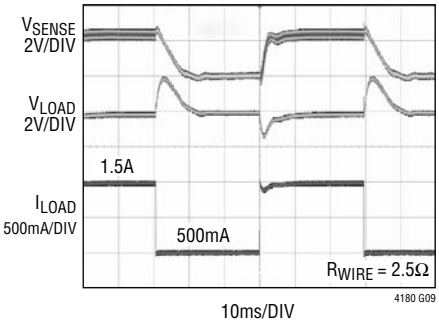


5ms/DIV

200mA TO 500mA LOAD TRANSIENT

100µF LOAD CAP

Load Step in Buck Application



10ms/DIV

500mA TO 1.5A LOAD TRANSIENT

470µF LOAD CAP

PIN FUNCTIONS

$INTV_{CC}$ (Pin 1): The LDO Output. A low ESR ceramic capacitor provides decoupling and output compensation. 1µF or more should be used.

DRAIN (Pin 2): Open-Drain of the Output Transistor. This pin drives either the LED in an opto-isolator, or pulls down on the regulator control pin.

COMP (Pin 3): Gate of the Output Transistor. This pin allows additional compensation. It must be left open if unused.

CHOLD1 (Pin 4): Connects to track/hold amplifier hold capacitor. The other end of this capacitor should be Kelvin connected to GND.

GUARD2 (Pin 5): Guard Ring Drive for CHOLD2.

CHOLD2 (Pin 6): Connects to track/hold amplifier hold capacitor. The other end of this capacitor should be Kelvin connected to GND.

GUARD3 (Pin 7): Guard Ring Drive for CHOLD3.

CHOLD3 (Pin 8): Connects to track/hold amplifier hold capacitor. The other end of this capacitor should be Kelvin connected to GND.

GUARD4 (Pin 9): Guard Ring Drive for CHOLD4.

CHOLD4 (Pin 10): Connects to track/hold amplifier hold capacitor. The other end of this capacitor should be Kelvin connected to GND.

FB (Pin 11): Receives the feedback voltage from an external resistor divider across the main output. An (optional) capacitor to ground may be added to eliminate high frequency noise. The time constant for this RC network should be no greater than 0.1 times the dither frequency. For example, with f_{DITHER} = 1kHz, τ = 0.1ms.

GND (Pin 12): Ground.

COSC (Pin 13): Oscillator Timing Capacitor. Oscillator frequency is set by this capacitor and ROSC. For best accuracy, the minimum recommended capacitance is 100pF.

ROSC (Pin 14): Oscillator Timing Resistor. Oscillator frequency is set by this resistor and COSC.

OSC (Pin 15): Oscillator Output. This output may be used to synchronize the switching regulator to the Virtual Remote Sense. This is a high current output capable of driving opto-isolators. Other isolation methods may also be used with this output.

DIV2 (Pin 16): Dither Division Ratio Programming Pin.

DIV1 (Pin 17): Dither Division Ratio Programming Pin.

DIV0 (Pin 18): Dither Division Ratio Programming Pin.

Use the following table to program the dither division ratio (f_{OSC}/f_{DITHER})

Table 1. Programming the Dither Division Ratio (f_{OSC}/f_{DITHER})

DIV2	DIV1	DIV0	DIVISION RATIO
0	0	0	8
0	0	1	16
0	1	0	32
0	1	1	64
1	0	0	128
1	0	1	256
1	1	0	512
1	1	1	1024

For example, $f_{DITHER} = f_{OSC}/128$ with DIV2 = 1 and DIV1 = DIV0 = 0.

SPREAD (Pin 19): Spread Spectrum Enable Input. Dither phasing is pseudo-randomly adjusted when SPREAD is tied high.

OV (Pin 20): Overvoltage Comparator Input. This prevents line drop correction when wiring drops would cause excessive switching power supply output voltage. Set OV so $V_{REG(MAX)} \leq 1.50V_{LOAD}$.

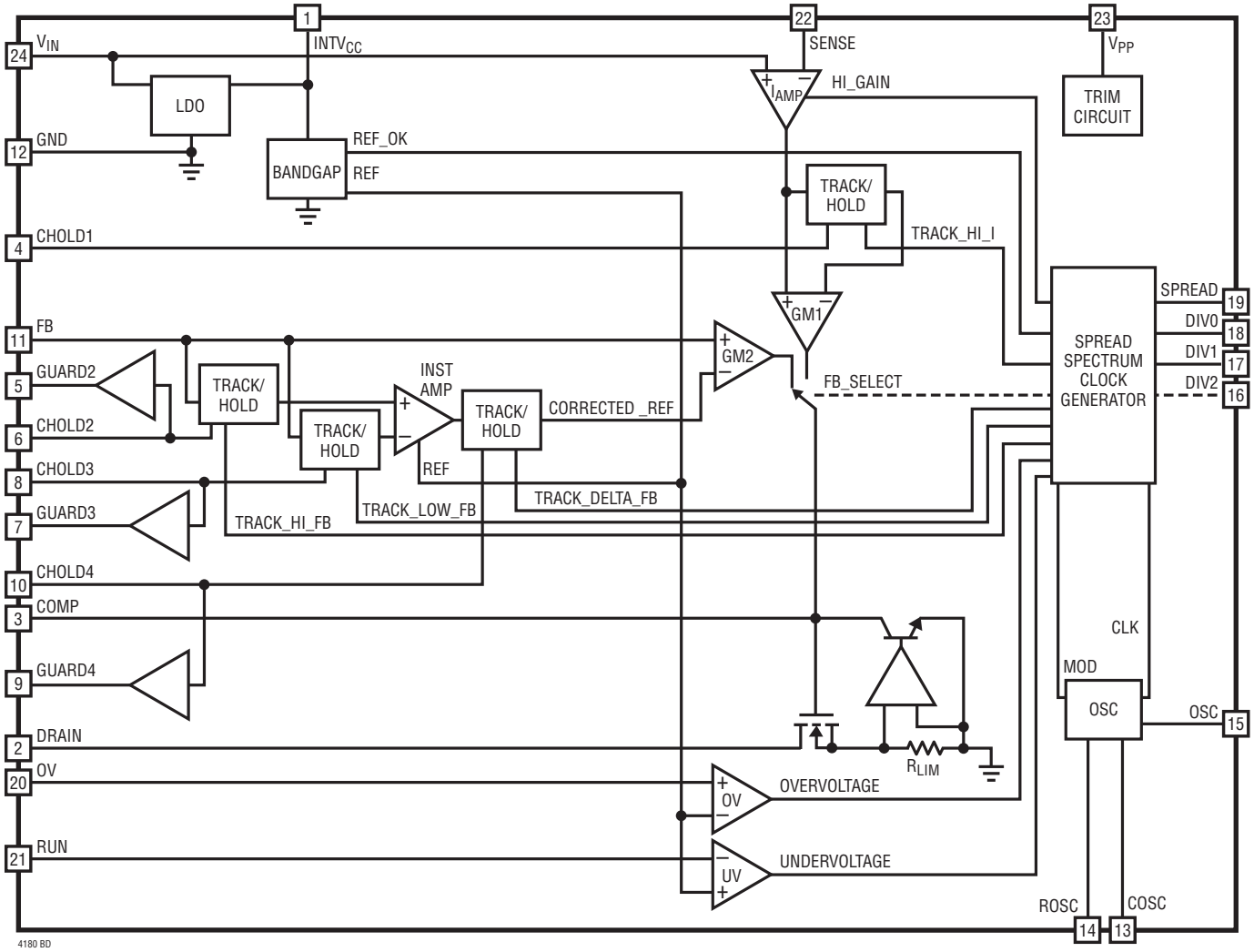
RUN (Pin 21): The RUN pin provides the user with an accurate means for sensing the input voltage and programming the start-up threshold for the line drop corrector.

SENSE (Pin 22): Current Sense Input. This input connects to the current sense resistor. Kelvin connect to R_{SENSE}.

V_{PP} (Pin 23): Connect this pin to $INTV_{CC}$.

V_{IN} (Pin 24): Main Supply Pin. V_{IN} must be locally bypassed to ground. Kelvin connect the current sense resistor to this pin and minimize interconnect resistance.

BLOCK DIAGRAM



OPERATION

Voltage drops in wiring can produce considerable load regulation errors in electrical systems (Figure 1). As load current, I_L, increases the voltage drop in the wiring (I_L • RW) increases and the voltage delivered to the system (V_L) drops. The traditional approach to solving this problem, remote sensing, regulates the voltage at the load, increasing the power supply voltage (V_{OUT}) to compensate for voltage drops in the wiring. While remote sensing works well, it does require an additional pair of wires to measure at the load, which may not always be practical.

The LT4180 eliminates the need for a pair of remote sense wires by creating a Virtual Remote Sense. Virtual remote sensing is achieved by measuring the incremental change in voltage that occurs with an incremental change in current in the wiring (Figure 2). This measurement can then be used to infer the total DC voltage drop in the wiring, which can then be compensated for. The Virtual Remote Sense takes over control of the power supply via the feedback pin (V_{FB}) of the power supply maintaining tight regulation of load voltage, V_L.

The LT4180 operates by modulating the output current of the regulator and looking at the resulting voltage change. A large output capacitor is placed across the load so the AC impedance at the load is low. *[Normally, a capacitor appears across the load in remote sensing situations to keep the impedance low at that point].* This capacitor is large enough that the AC impedance at the load is very low compared to the line resistance. When the output current is modulated, any voltage change that appears across the terminals of the LT4180 is due to the resistance in the line since the AC resistance at the load is very low.

There are four sample-and-hold capacitors in the LT4180. The operation cycles through several stages to obtain the correction voltage. First, the output voltage is regulated and the control point is sampled and held. The control loop is then switched to a current regulating control loop and the output current is changed by 10%. Two sample-and-hold currents store the voltage at the high current and low current level of the modulation. This voltage change is the result of a 10% change in current, making the voltage change 10% of the total drop in the line. The voltage change is amplified by a factor of 10.

The amplified voltage change that occurs with the current is again sampled and held and is used as the correction voltage. The correction voltage is summed into the output and this corrects for the line drop. Since this correction is actually open-loop, the actual voltage at the load is not measured. The ability of the LT4180 to correct for line drops is dependent upon the accuracy of the computations.

The LT4180 can correct better than 50 to 1 for line drops. For example, a 10V drop in the line becomes a 200mV change at the load.

The frequency of the correction cycle can be set from over 32kHz down to less than 250Hz, depending on the size of the capacitors in the system. For very large capacitors in high current systems, the dither correction clock would be run more slowly. In simpler systems with smaller output capacitors, the dither can be run at a higher frequency. If the load contains frequencies similar to the dither, beat notes can result between the load and the LT4180. A spread spectrum option on the LT4180 allows the device to change phasing during the correction cycle so that it will not interfere with load pulses.

Finally, the LT4180 takes into account all resistances between the LT4180 and the load capacitor. It can correct for cable connections, line resistances and varying contact resistances. By measuring the peak change at the output of the LT4180 one can monitor the impedance between the LT4180 and the load, and detect increasing impedances

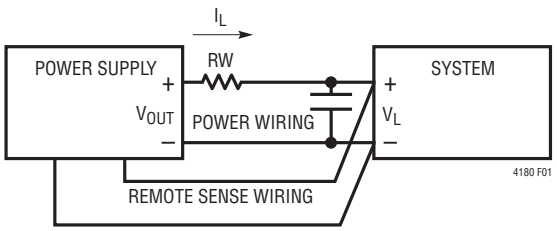


Figure 1. Traditional Remote Sensing

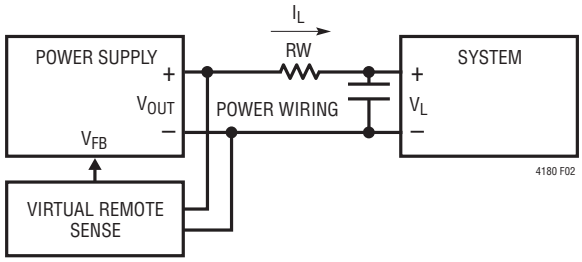


Figure 2. Virtual Remote Sensing

OPERATION

from degrading contacts. Making the capacitor larger can minimize the voltage ripple at the load due to a combination of load regulation and the dither frequency of the LT4180.

Figure 3 shows the timing diagram for Virtual Remote Sense. A new cycle begins when the power supply and Virtual Remote Sense close the loop around V_{OUT} (regulate V_{OUT} = H). Both V_{OUT} and I_{OUT} slew and settle to a new value, and these values are stored in the Virtual Remote Sense (track V_{OUT} high = L and track I_{OUT} = L). The V_{OUT} feedback loop is opened and a new feedback loop is set up commanding the power supply to deliver 90% of the previously measured current ($0.9I_{OUT}$). V_{OUT} drops to a new value as the power supply reaches a new steady state, and this information is also stored in the Virtual Remote Sense. At this point, the change in output voltage (ΔV_{OUT}) for a –10% change in output current has been measured and is stored in the Virtual Remote Sense. This voltage is used during the next Virtual Remote Sense cycle to compensate for voltage drops due to wiring resistance.

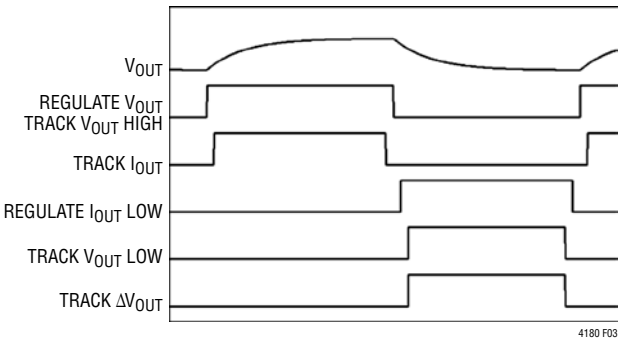


Figure 3. Simplified Timing Diagram, Virtual Remote Sense

APPLICATIONS INFORMATION

INTRODUCTION

The LT4180 is designed to interface with a variety of power supplies and regulators having either an external feedback or control pin. In Figure 4, the regulator error amplifier (which is a g_m amplifier) is disabled by tying its inverting input to ground. This converts the error amplifier into a constant-current source which is then controlled by the drain pin of the LT4180. This is the preferred method of interfacing because it eliminates the regulator error amplifier from the control loop which simplifies compensation and provides best control loop response.

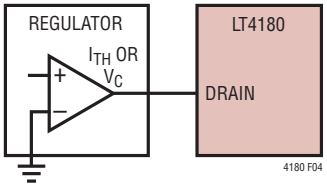


Figure 4. Nonisolated Regulator Interface

For proper operation, increasing control voltage should correspond to increasing regulator output. For example, in the case of a current mode switching power supply, the control pin ITH should produce higher peak currents as the ITH pin voltage is made more positive.

Isolated power supplies and regulators may also be used by adding an opto-coupler (Figure 5). LT4180 output voltage $INTV_{CC}$ supplies power to the opto-coupler LED. In situations where the control pin V_C of the regulator may exceed 5V, a cascode may be added to keep the DRAIN pin of the LT4180 below 5V (Figure 6). Use a low VT MOSFET for the cascode transistor.

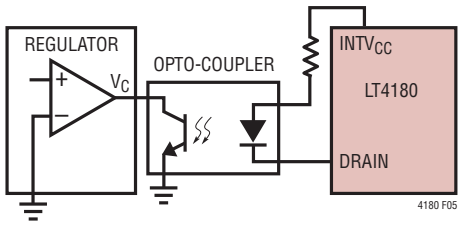


Figure 5. Isolated Power Supply Interface

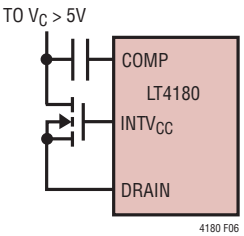


Figure 6. Cascoded DRAIN Pin for Isolated Supplies

APPLICATIONS INFORMATION

DESIGN PROCEDURE

The first step in the design procedure is to determine whether the LT4180 will control a linear or switching supply/regulator. If using a switching power supply or regulator, it is recommended that the supply be synchronized to the LT4180 by connecting the OSC pin to the SYNC pin (or equivalent) of the supply.

If the power supply is synchronized to the LT4180, the power supply switching frequency is determined by:

$$f_{OSC} = \frac{4}{R_{OSC} \bullet C_{OSC}}$$

Recommended values for R_{OSC} are between 20k and 100k (with 30.1k the optimum for best accuracy) and greater than 100pF for C_{OSC}. C_{OSC} may be reduced to as low as 50pF, but oscillator frequency accuracy will be somewhat degraded.

The following example synchronizes a 250kHz switching power supply to the LT4180. In this example, start with R_{OSC} = 30.1k:

$$C_{OSC} = \frac{4}{250kHz \bullet 30.1k} = 531pF$$

This example uses 470pF. For 250kHz:

$$R_{OSC} = \frac{4}{250kHz \bullet 470pF} = 34.04k$$

The closest standard 1% value is 34k.

The next step is to determine the highest practical dither frequency. This may be limited either by the response time of the power supply or regulator, or by the propagation time of the wiring connecting the load to the power supply or regulator.

First determine the settling time (to 1% of final value) of the power supply. The settling time should be the worst-case value (over the whole operating envelope: V_{IN}, I_{LOAD}, etc.).

$$F1 = \frac{1}{2 \bullet t_{SETTLING}} Hz$$

For example, if the power supply takes 1ms to settle (worst-case) to within 1% of final value:

$$F1 = \frac{1}{2 \bullet 1e-3} = 500Hz$$

Next, determine the propagation time of the wiring. In order to ignore transmission line effects, the dither period should be approximately twenty times longer than this. This will limit dither frequency to:

$$F2 = \frac{V_F}{20 \bullet 1.017ns/ft \bullet L} Hz$$

Where V_F is the velocity factor (or velocity of propagation), and L is the length of the wiring (in feet).

For example, assume the load is connected to a power supply with 1000ft of CAT5 cable. Nominal velocity of propagation is approximately 70%.

$$F2 = \frac{0.7}{20 \bullet 1.017e-9 \bullet 1000} = 34.4kHz$$

The maximum dither frequency should not exceed F1 or F2 (whichever is less):

$$f_{DITHER} < \min (F1, F2).$$

Continuing this example, the dither frequency should be less than 500Hz (limited by the power supply).

With the dither frequency known, the division ratio can be determined:

$$D_{RATIO} = \frac{f_{OSC}}{f_{DITHER}} = \frac{250,000}{500} = 500$$

The nearest division ratio is 512 (set DIV0 = L, DIV1 = DIV2 = H). Based on this division ratio, nominal dither frequency will be:

$$f_{DITHER} = \frac{f_{OSC}}{D_{RATIO}} = \frac{250,000}{512} = 488Hz$$

After the dither frequency is determined, the minimum load decoupling capacitor can be determined. This load capacitor must be sufficiently large to filter out the dither signal at the load.

APPLICATIONS INFORMATION

$$C_{LOAD} = \frac{2.2}{R_{WIRE} \bullet 2 \bullet f_{DITHER}}$$

Where C_{LOAD} is the minimum load decoupling capacitance, R_{WIRE} is the minimum wiring resistance of one conductor of the wiring pair, and f_{DITHER} is the minimum dither frequency.

Continuing the example, our CAT5 cable has a maximum 9.38Ω/100m conductor resistance.

Maximum wiring resistance is:

$R_{WIRE} = 2 \bullet 1000ft \bullet 0.305m/ft \bullet 0.0938\Omega/m$

$R_{WIRE} = 57.2\Omega$

With an oscillator tolerance of ±15%, the minimum dither frequency is 414.8Hz, so the minimum decoupling capacitance is:

$$C_{LOAD} = \frac{2.2}{57.2\Omega \bullet 2 \bullet 414.8Hz} = 46.36\mu F$$

This is the minimum value. Select a nominal value to account for all factors which could reduce the nominal, such as initial tolerance, voltage and temperature coefficients and aging.

CHOLD Capacitor Selection and Compensation

CHOLD1

A 47nF capacitor will suffice for most applications. A smaller value might allow faster recovery from a sudden load change, but care must be taken to ensure full load p-p ripple at this node is kept within 5mV:

$$CHOLD2 = CHOLD3 = \frac{2.5nF}{f_{DITHER}(kHz)}$$

For a dither frequency of 488Hz:

$$CHOLD2 = CHOLD3 = \frac{2.5nF}{0.488(kHz)} = 5.12nF$$

NPO ceramic or other capacitors with low leakage and dielectric absorption should be used for all HOLD capacitors.

Set CHOLD4 to 1µF. This value will be adjusted later.

Compensation

Start with a 47pF capacitor between the COMP and DRAIN pins of the LT4180. Add an RC network in parallel with the 47pF capacitor, 10k and 10nF are good starting values. Once the output voltage has been confirmed to regulate at the desired level at no load, increase the load current to the 100% level and monitor the wire current (dither current) with a current probe. Verify the dither current resembles a square wave with the desired dither frequency.

If the output voltage is too low, increase the value of the 10k resistor until some overshoot is observed at the leading edge of the dither current waveform. If the output voltage is still too low, decrease the value of the 10nF capacitor and repeat the previous step. Repeat this process until the full load output voltage increases to within 1% below the no load level. Refer to Figures 7a, 7b and 7c, which show compensation of the 12V 1.5A buck regulator Typical Application on the data sheet. Check for proper voltage drop correction over the load range. The dither current should have good half-wave symmetry. Namely, the waveform should have similar rise and fall times, enough settling time at top and bottom and minimum to no over/undershoot.

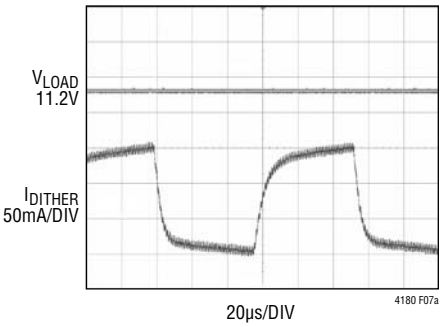


Figure 7a. Dither Current and V_{OUT} with 10nF, 10k Compensation 1.5A Load

APPLICATIONS INFORMATION

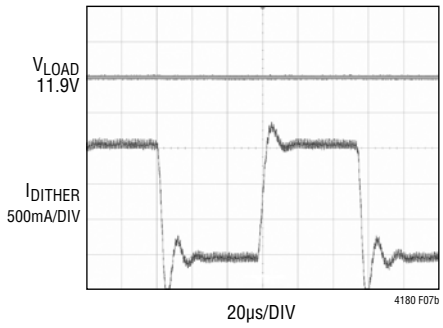


Figure 7b. Dither Current and V_{OUT} with 10nF, 37k Compensation 1.5A Load

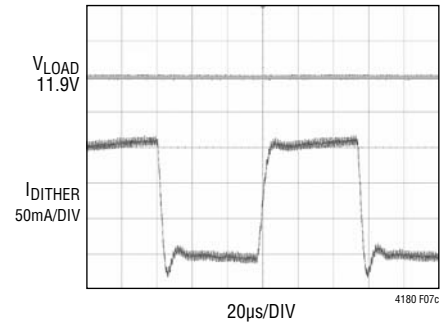


Figure 7c. Dither Current and V_{OUT} with 3.3nF, 28k Compensation 1.5A Load

Set Final Value of CHOLD4

Set the minimum value for CHOLD4, by performing a transient load test of 30% to 60% of the load and set the value of CHOLD4 to where a nicely damped waveform is observed. Refer to Figures 8a and 8b for an illustration.

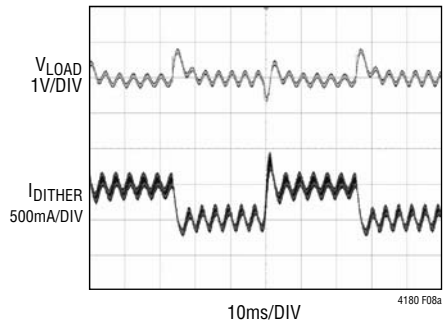


Figure 8a. 500mA to 1A Transient Response Test with CHOLD4 = 25nF CHOLD4 Too Small

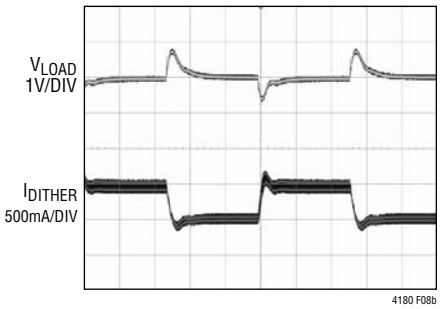


Figure 8b. 500mA to 1A Transient Response Test with CHOLD4 = 47nF Nicely Damped Behavior

After all the CHOLD values have been finalized, check for proper voltage drop correction and converter behavior (start-up, regulation, etc.), over the load and input voltage ranges.

Setting Output Voltage, Undervoltage and Overvoltage Thresholds

The RUN pin has accurate rising and falling thresholds which may be used to determine when Virtual Remote Sense operation begins. Undervoltage threshold should never be set lower than the minimum operating voltage of the LT4180 (3.1V).

The overvoltage threshold should be set slightly greater than the highest voltage which will be produced by the power supply or regulator:

$$V_{OUT(MAX)} = V_{LOAD(MAX)} + V_{WIRE(MAX)}$$

$V_{OUT(MAX)}$ should never exceed 1.5 • V_{LOAD}

Since the RUN and OV pins connect to MOSFET input comparators, input bias currents are negligible and a common voltage divider can be used to set both thresholds (Figure 9).

APPLICATIONS INFORMATION

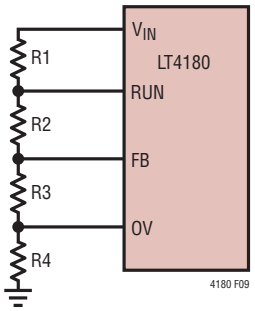


Figure 9. Voltage Divider for Output Voltage, UVL and OVL

The voltage divider resistors can be calculated from the following equations:

$$R_T = \frac{V_{OV}}{200\mu A},\quad R4 = \frac{1.22V}{200\mu A}$$

Where R_T is the total divider resistance and V_{OV} is the overvoltage set point.

Find the equivalent series resistance for R2 and R3 (R_{SERIES}). This resistance will determine the RUN voltage level.

$$R_{SERIES} = \left(\frac{1.22 \bullet R_T}{V_{UVL}}\right) - R4$$

$$R1 = R_T - R_{SERIES} - R4$$

$$R3 = \frac{1.22V - \left(V_{OUT(NOM)} \bullet \frac{R4}{R_T}\right)}{\frac{V_{OUT(NOM)}}{R_T}}$$

Where V_{UVL} is the RUN voltage and $V_{OUT(NOM)}$ is the nominal output voltage desired.

For example, with $V_{UVL} = 4V$, $V_{OV} = 7.5V$ and $V_{OUT(NOM)} = 5V$,

$$R_T = \frac{7.5V}{200\mu A} = 37.5k$$

$$R4 = \frac{1.22V}{200\mu A} = 6.1k$$

$$R_{SERIES} = \left(\frac{1.22V \bullet 37.5k}{4V}\right) - 6.1k = 5.34k$$

$$R1 = 37.5k - 5.34k - 6.1k = 26.06k$$

$$R3 = \frac{1.22V - \left(\frac{5V \bullet 6.1k}{37.5k}\right)}{\frac{5V}{37.5k}} = 3.05k$$

$$R2 = R_{SERIES} - R3 = 2.29k$$

R_{SENSE} SELECTION

Select the value of R_{SENSE} so that it produces a 100mV voltage drop at maximum load current. For best accuracy, V_{IN} and SENSE should be Kelvin connected to this resistor.

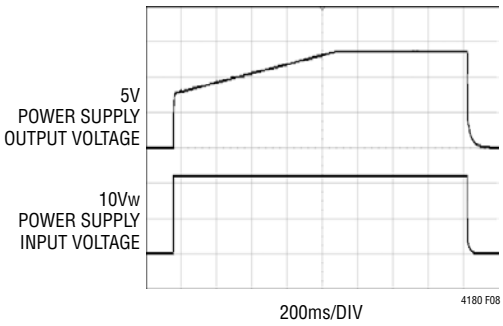


Figure 10. Soft-Correct Operation, C_{HOLD4} = 1µF

Soft-Correct Operation

The LT4180 has a soft-correct function which insures orderly start-up. When the RUN pin rising threshold is first exceeded (indicating V_{IN} has crossed its undervoltage lockout threshold), power supply output voltage is set to a value corresponding to zero wiring voltage drop (no correction for wiring). Over a period of time (determined by CHOLD4), the power supply output voltage ramps up to account for wiring voltage drops, providing best load-end voltage regulation. A new soft-correct cycle is also initiated whenever an overvoltage condition occurs.

APPLICATIONS INFORMATION

Using Guard Rings

The LT4180 includes a total of four track/holds in the Virtual Remote Sense path. For best accuracy, all leakage sources on the CHOLD pins should be minimized.

At very low dither frequencies, the circuit board layout may include guard rings which should be tied to their respective guard ring drivers.

To better understand the purpose of guard rings, a simplified model of hold capacitor leakage (with and without guard rings) is shown in Figure 11. Without guard rings, a large difference voltage may exist between the hold capacitor (Pin 1) node and adjacent conductors (Pin 2) producing substantial leakage current through the leakage resistance (R_{LKG}). By adding a guard ring driver with approximately the same voltage as the voltage on the hold capacitor node, the difference voltage across R_{LKG1} is reduced substantially thereby reducing leakage current on the hold capacitor.

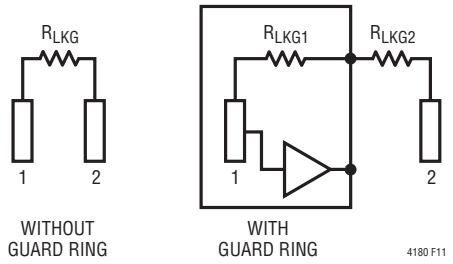


Figure 11. Simplified Leakage Models (with and without Guard Rings)

Synchronization

Linear and switching power supplies and regulators may be used with the LT4180. In most applications regulator interference should be negligible. For those applications where accurate control of interference spectrum is desirable, an oscillator output has been provided so that switching supplies may be synchronized to the LT4180 (Figure 12). The OSC pin was designed so that it may directly connect to most regulators, or drive opto-isolators (for isolated power supplies).

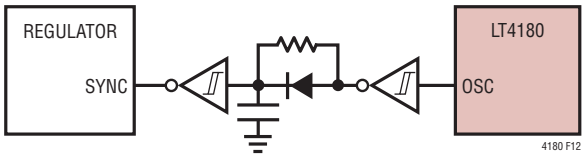


Figure 12. Clock Interface for Synchronization

Spread Spectrum Operation

Virtual Remote Sense functionality relies on sampling techniques. Because switching power supplies are commonly used, the LT4180 uses a variety of techniques to minimize potential interference (in the form of beat notes which may occur between the dither frequency and power supply switching frequency). Besides several types of internal filtering, and the option for Virtual Remote Sense/power supply synchronization, the LT4180 also provides spread spectrum operation.

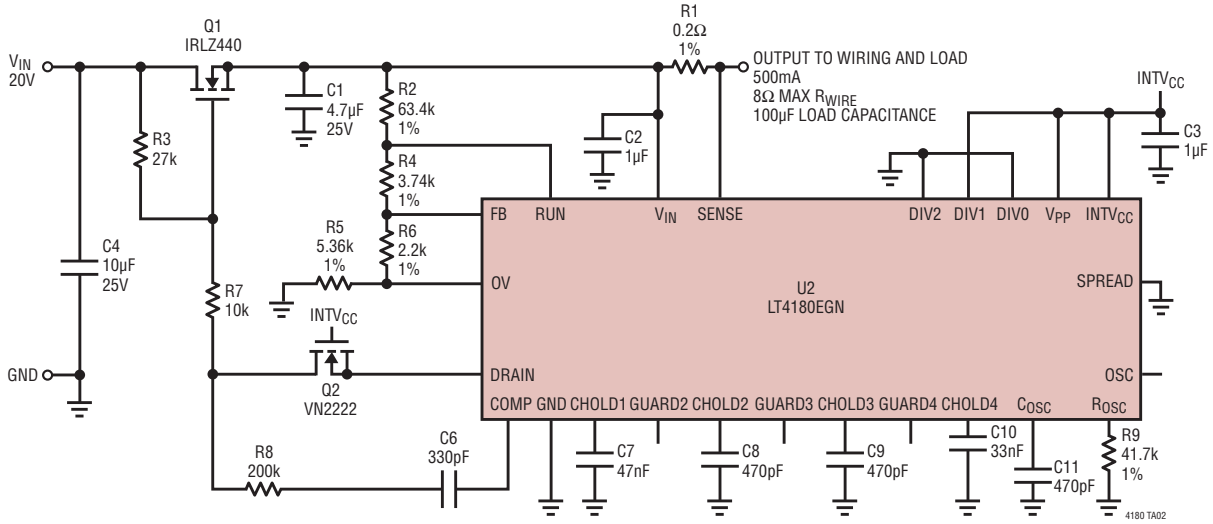
By enabling spread spectrum operation, low modulation index pseudo-random phasing is applied to Virtual Remote Sense timing. This has the effect of converting any remaining narrow-band interference into broadband noise, reducing its effect.

Increasing Voltage Correction Range

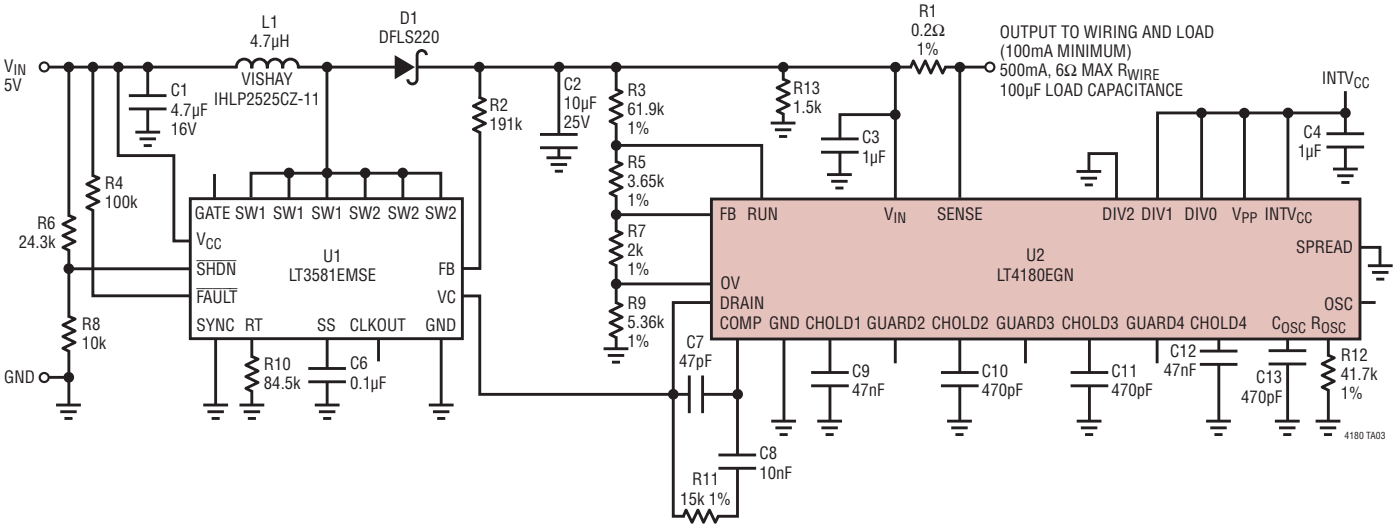
Correction range may be slightly improved by regulating $INTV_{CC}$ to 5V. This may be done by placing an LDO between V_{IN} and $INTV_{CC}$. Contact Linear Technology Applications for more information.

TYPICAL APPLICATIONS

12V, 500mA Linear Regulator

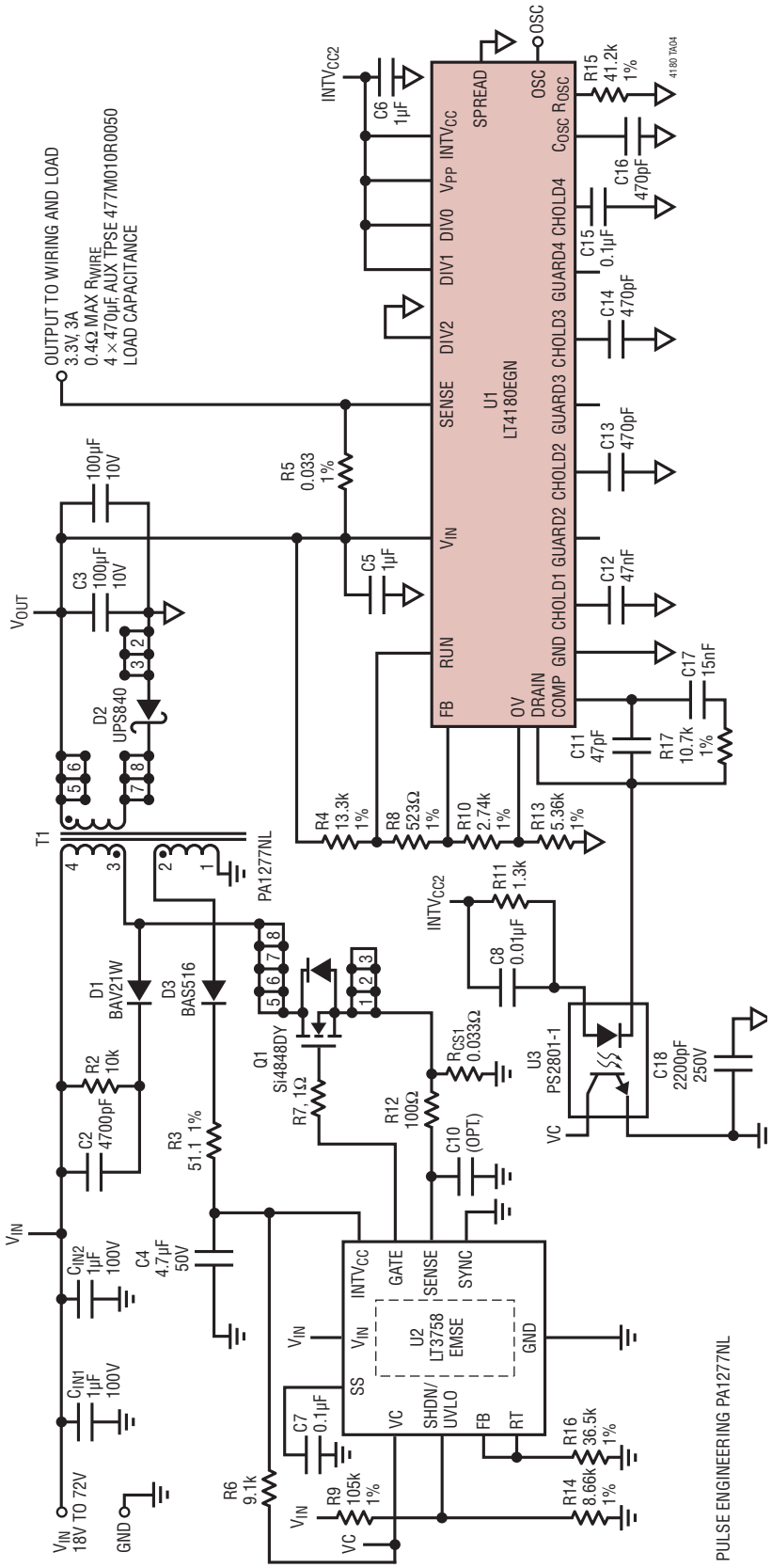


12V, 500mA Boost Regulator



TYPICAL APPLICATIONS

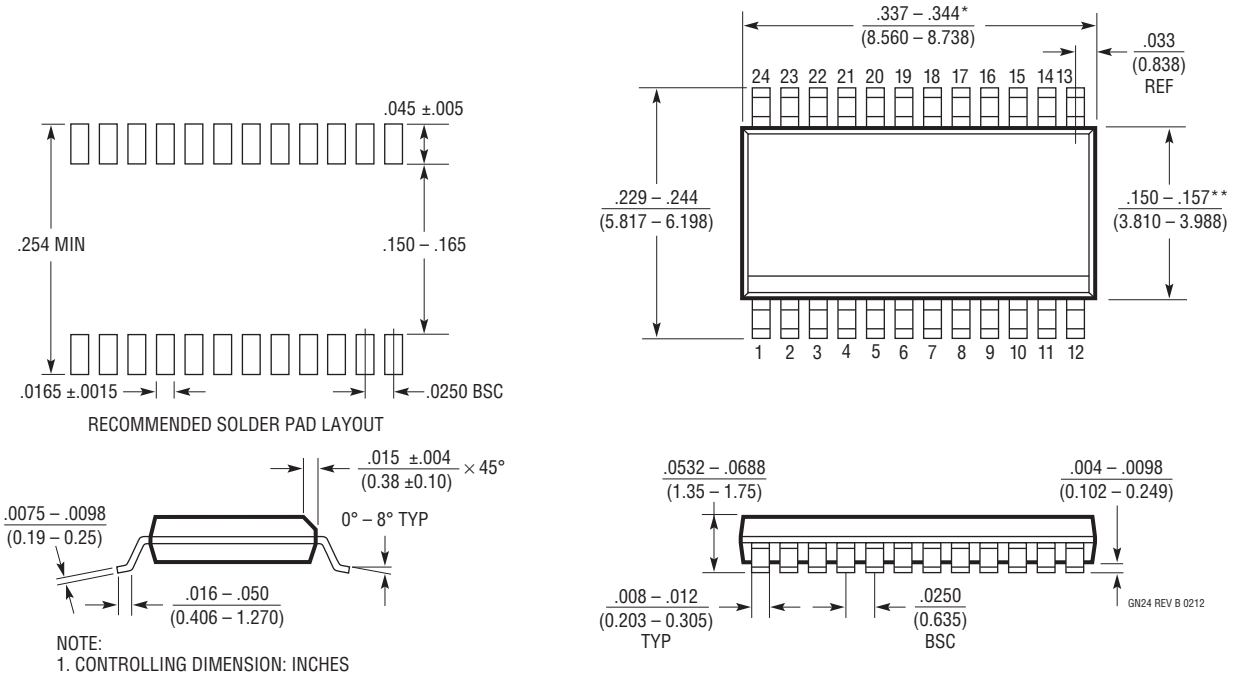
3.3V Isolated Flyback Regulator



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

GN Package
24-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641 Rev B)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	6/11	Revised Typical Applications drawings	1, 13, 14, 18
		Revised Electrical Characteristics	2, 3
		Replaced curves G08 and G09 in Typical Performance Characteristics	4
		Replaced text for CHOLD Capacitor Selection and Compensation section and deleted Power Supply Current Limiting paragraph in Applications Information section	10, 11
B	4/13	Revised schematics	14, 15, 18