40MHz to 10GHz RMS Power Detector with 57dB Dynamic Range

FEATURES

- **Frequency Range: 40MHz to 10GHz**
- **Linear Dynamic Range: Up to 57dB**
- **Accurate RMS Power Measurement of High Crest Factor Modulated Waveforms**
- **Exceptional Accuracy Over Temperature: ±0.5dB (Typ)**
- **Low Linearity Error within Dynamic Range**
- **Single-Ended or Differential RF Inputs**
- **Fast Response Time: 90ns Rise Time**
- Low Supply Current: 41.6mA at 3.3V (Typ)
- Small 3mm × 3mm DFN10
- AEC-Q100 Qualified for Automotive Applications

APPLICATIONS

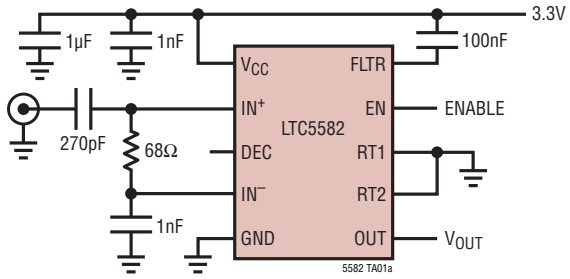
- RMS Power Measurement
- PA Power Control
- Receive and Transmit Gain Control
- LTE, WiMAX, W-CDMA, CDMA2K, TD-SCDMA, EDGE Basestations
- Point-to-Point Microwave Links
- RF Instrumentation

DESCRIPTION

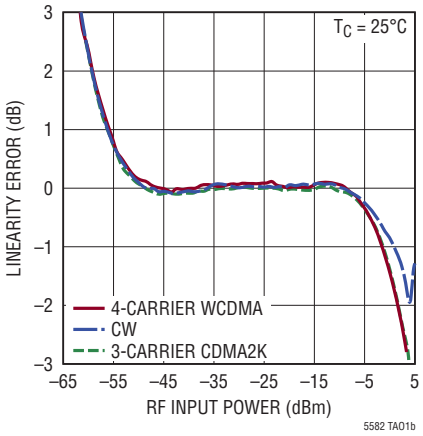
The LTC®5582 is a 40MHz to 10GHz RMS responding power detector. It is capable of accurate power measurement of an AC signal with wide dynamic range, from –60dBm to 2dBm depending on frequency. The power of the AC signal in an equivalent decibel-scaled value is precisely converted into DC voltage on a linear scale, independent of the crest factor of the input signal waveforms. The LTC5582 is suitable for precision RF power measurement and level control for a wide variety of RF standards, including LTE, WiMAX, W-CDMA, CDMA2000, TD-SCDMA, and EDGE. The DC output is buffered with a low output impedance amplifier capable of driving a high capacitance load. Consult factory for more information. The part is packaged in a 10-lead 3mm × 3mm DFN. It is pin-to-pin compatible with the LT5570.

TYPICAL APPLICATION

40MHz to 6GHz RMS Power Detector



Linearity Error vs RF Input Power 2140MHz Modulated Waveforms

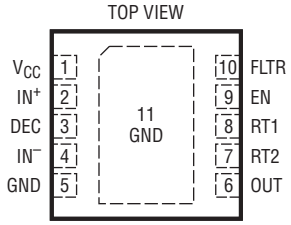


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltage 3.8V
Enable Voltage ..... –0.3V to V_{CC} + 0.3V
Input Signal Power (Single-Ended, 50Ω) 18dBm
Input Signal Power (Differential, 50Ω) 24dBm
T_{JMAX} ..... 150°C
Case Operating Temperature Range (T_C):
I-Grade (Note 2) ..... –40°C to 105°C
H-Grade (Note 3) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 125°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC5582IDD#PBF	LTC5582IDD#TRPBF	LFGZ	10-Lead 3mm × 3mm Plastic DFN	–40°C to 105°C
LTC5582HDD#PBF	LTC5582HDD#TRPBF	LFGZ	10-Lead 3mm × 3mm Plastic DFN	–40°C to 125°C
AUTOMOTIVE PRODUCTS**				
LTC5582IDD#3ZZPBF	LTC5582IDD#3ZZPBF	LFGZ	10-Lead 3mm × 3mm Plastic DFN	–40°C to 105°C
LTC5582HDD#3ZZPBF	LTC5582HDD#3ZZPBF	LFGZ	10-Lead 3mm × 3mm Plastic DFN	–40°C to 125°C

Consult ADI Marketing for parts specified with wider operating temperature ranges.
Consult ADI Marketing for information on non-standard lead based finish parts.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #3ZZ suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = 3.3V, EN = 3.3V. Test circuit is shown in Figure 1. (Notes 2 and 3).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AC Input						
Input Frequency Range (Note 5)				40 to 10000		MHz
Input Impedance	Differential			400//0.5		Ω//pF
f_{RF} = 450MHz						
RF Input Power Range	CW; Single-Ended, 50Ω			–57 to 2		dBm
Linear Dynamic Range (Note 6)	±1dB Linearity Error			59		dB
Output Slope				29.5		mV/dB
Logarithmic Intercept (Notes 4, 6)				–86.2		dBm
Output Variation vs Temperature	Normalized to Output at 25°C, Pin = –50dBm to 0dBm	●		±0.5		dB
Deviation from CW Response	11dB Peak to Average Ratio (3-Carrier CDMA2K) 12dB Peak to Average Ratio (4-Carrier WCDMA)			0.1 0.1		dB dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = 3.3V, EN = 3.3V. Test circuit is shown in Figure 1. (Notes 2 and 3).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
2nd Order Harmonic Distortion	At RF Input; CW Input; PIN = 0dBm			67		dBc
3rd Order Harmonic Distortion	At RF Input; CW Input; PIN = 0dBm			62		dBc
f_{RF} = 880MHz						
RF Input Power Range	CW; Single-Ended, 50Ω			–57 to 2		dBm
Linear Dynamic Range (Note 6)	±1dB Linearity Error			59		dB
Output Slope				29.3		mV/dB
Logarithmic Intercept (Notes 4, 6)				–86.4		dBm
Output Variation vs Temperature	Normalized to Output at 25°C, Pin = –50dBm to 0dBm	●		±0.5		dB
Deviation from CW Response	11dB Peak to Average Ratio (3-Carrier CDMA2K) 12dB Peak to Average Ratio (4-Carrier WCDMA)			0.1 0.1		dB dB
2nd Order Harmonic Distortion	At RF Input; CW Input; PIN = 0dBm			69		dBc
3rd Order Harmonic Distortion	At RF Input; CW Input; PIN = 0dBm			59		dBc
f_{RF} = 2140MHz						
RF Input Power Range	CW; Single-Ended, 50Ω			–56 to 1		dBm
Linear Dynamic Range (Note 6)	±1dB Linearity Error		50	57		dB
Output Slope			26	29.5	33	mV/dB
Logarithmic Intercept (Notes 4, 6)			–98	–85	–72	dBm
Output Variation vs Temperature	Normalized to Output at 25°C, Pin = –47dBm to 0dBm	●		±0.5		dB
Deviation from CW Response	11 dB Peak to Average Ratio (3-Carrier CDMA2K) 12dB Peak to Average Ratio (4-Carrier WCDMA)			0.1 0.1		dB dB
f_{RF} = 2700MHz						
RF Input Power Range	CW; Single-Ended, 50Ω			–55 to 1		dBm
Linear Dynamic Range (Note 6)	±1dB Linearity Error			56		dB
Output Slope				29.8		mV/dB
Logarithmic Intercept (Notes 4, 6)				–83.8		dBm
Output Variation vs Temperature	Normalized to Output at 25°C, Pin = –47dBm to 0dBm	●		±0.5		dB
Deviation from CW Response	12dB Peak to Average Ratio (WiMAX OFDM)			0.2		dB
f_{RF} = 3800MHz						
RF Input Power Range	CW; Single-Ended, 50Ω			–51 to 2		dBm
Linear Dynamic Range (Note 6)	±1dB Linearity Error			53		dB
Output Slope				30.3		mV/dB
Logarithmic Intercept (Notes 4, 6)				–81		dBm
Output Variation vs Temperature	Normalized to Output at 25°C, Pin = –51dBm to 2dBm	●		±1		dB
Deviation from CW Response	12dB Peak to Average Ratio (WiMAX OFDM)			0.2		dB
f_{RF} = 5800MHz						
RF Input Power Range	CW; Single-Ended, 50Ω			–46 to 3		dBm
Linear Dynamic Range (Note 6)	±1dB Linearity Error			49		dB
Output Slope				30.9		mV/dB
Logarithmic Intercept (Notes 4, 6)				–74.7		dBm
Output Variation vs Temperature	Normalized to Output at 25°C, Pin = –46dBm to 2dBm	●		±1		dB
Deviation from CW Response	12dB Peak to Average Ratio (WiMAX OFDM)			0.2		dB

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_C = 25°C. V_{CC} = 3.3V, EN = 3.3V. Test circuit is shown in Figure 1. (Notes 2 and 3).

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Interface						
Output DC Voltage	No RF Signal Present			0.69		V
Output Impedance				100		Ω
Output Current	Maximum			±5		mA
Rise Time, 10% to 90%	0.8V to 2.4V, C3 = 8nF, f_{RF} = 100MHz			90		nS
Fall Time, 90% to 10%	2.4V to 0.8V, C3 = 8nF, f_{RF} = 100MHz			5		µS
Enable (EN) Low = Off, High = On						
EN Input High Voltage (On)		●	1			V
EN Input Low Voltage (Off)		●			0.4	V
Enable Pin Input Current	EN = 3.3V			125	200	µA
Turn ON Time	V_{OUT} within 10% of Final Value, C3 = 8nF			2.8		µs
Turn OFF Time	V_{OUT} < 0.8V, C3 = 8nF			40		µs
Power Supply						
Supply Voltage			3.1	3.3	3.5	V
Supply Current				41.6	52	mA
Shutdown Current	EN = 0V, V_{CC} = 3.5V			0.1	10	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC5582IDD is guaranteed functional over the case temperature range –40°C to 105°C. All limits at –40°C and 105°C are guaranteed by design and production sample testing.

Note 3: The LTC5582HDD is guaranteed functional over the case temperature range –40°C to 125°C. All limits at –40°C and 125°C are guaranteed by 100% production testing.

Note 4: Logarithmic Intercept is an extrapolated input power level from the best fitted log-linear straight line, where the output voltage is 0V.

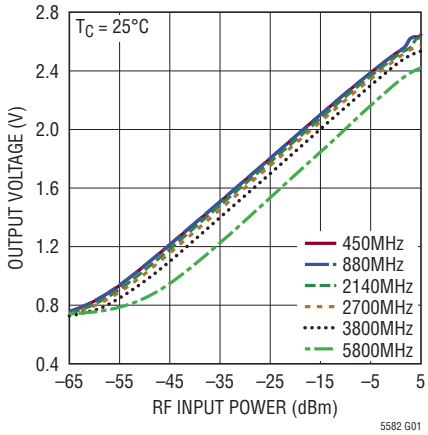
Note 5: Operation over a wider frequency range is possible with reduced performance. Consult the factory for information and assistance.

Note 6: The linearity error is calculated by the difference between the incremental slope of the output and the average output slope from –50dBm to –5dBm for frequencies up to 5.8GHz, and –25dBm to –5dBm for 8GHz and 10GHz. The dynamic range is defined as the range over which the linearity error is within ±1dB.

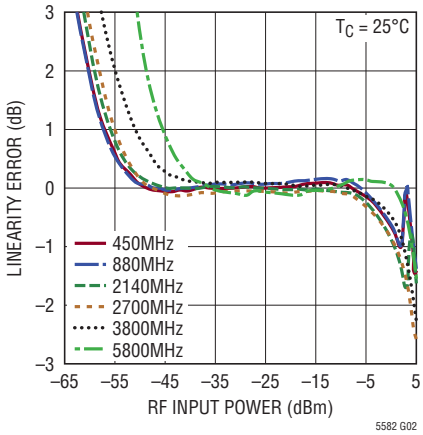
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, T_C = 25°C, R_{T1} = 0Ω, R_{T2} = 0Ω unless otherwise noted. Test circuits shown in Figure 1.

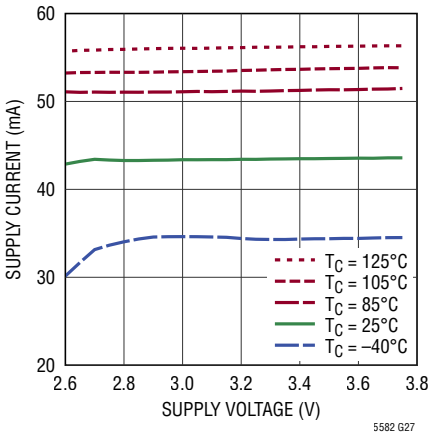
Output Voltage vs RF Input Power



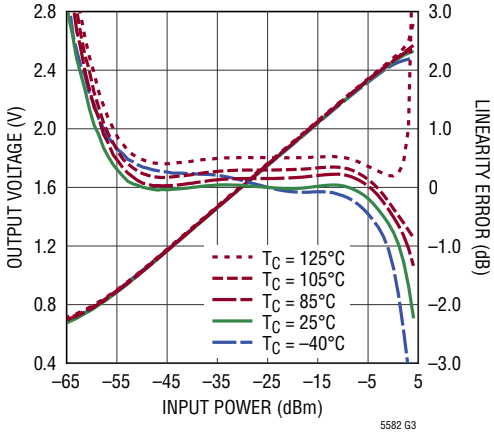
Linearity Error vs RF Input Power



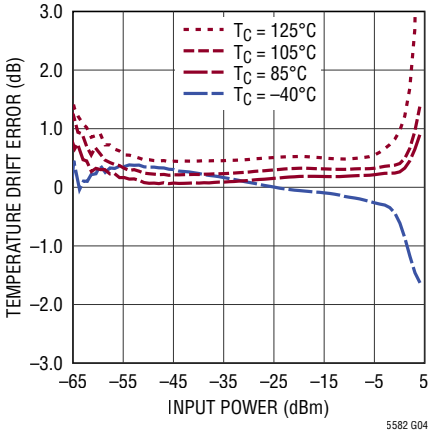
Supply Current vs Supply Voltage



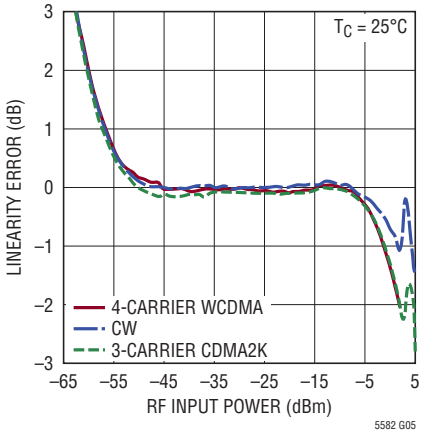
Output Voltage, Linearity Error vs RF Input Power, 450MHz



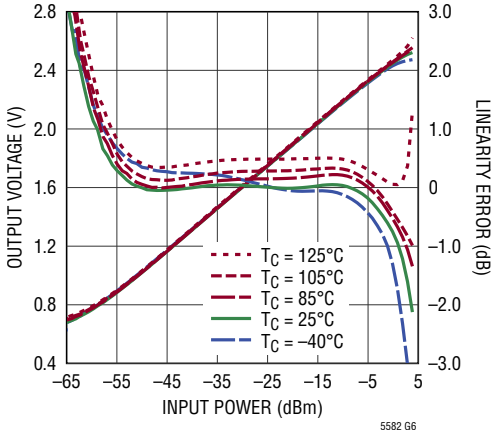
Output Voltage Temperature Variation from 25°C, 450MHz



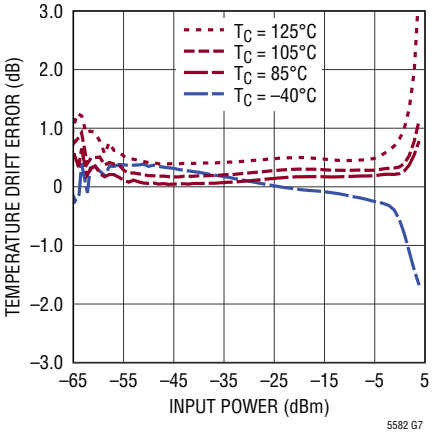
Linear Error vs RF Input Power, Modulated Waveforms, 450MHz



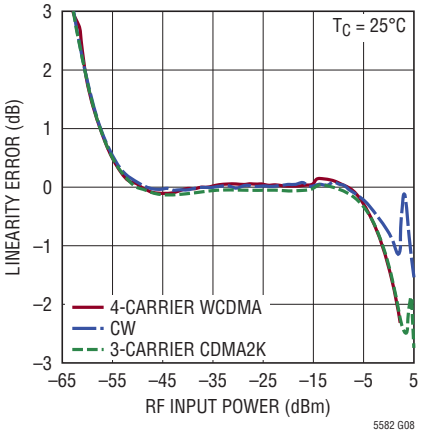
Output Voltage, Linearity Error vs RF Input Power, 880MHz



Output Voltage Temperature Variation from 25°C, 880MHz



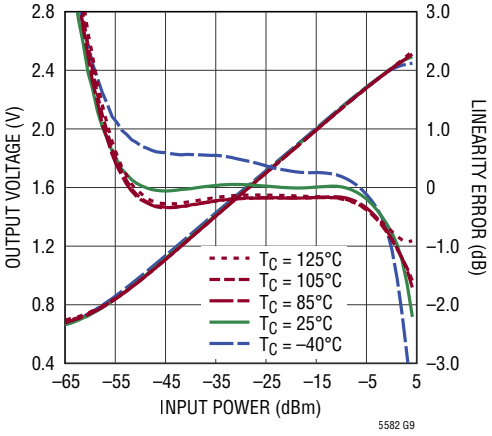
Linear Error vs RF Input Power, Modulated Waveforms, 880MHz



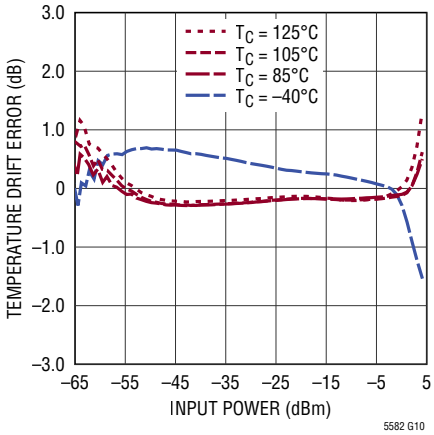
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, T_C = 25°C, R_{T1} = 0Ω, R_{T2} = 0Ω unless otherwise noted. Test circuits shown in Figure 1.

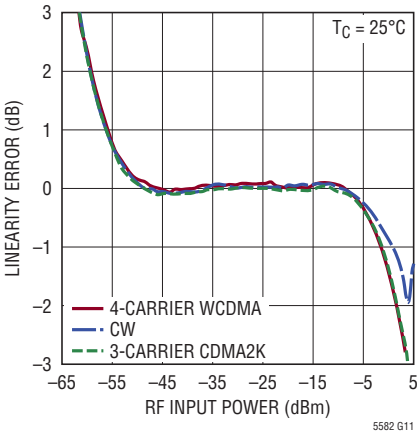
Output Voltage, Linearity Error vs RF Input Power, 2140MHz



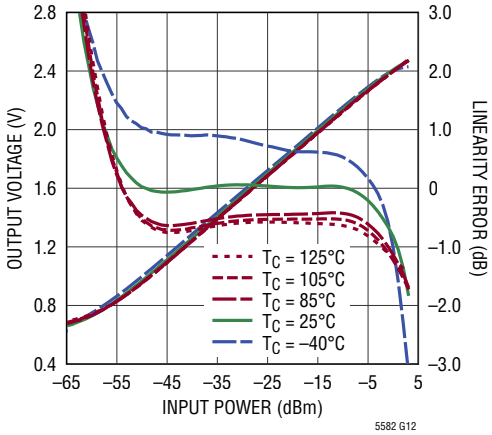
Output Voltage Temperature Variation from 25°C, 2140MHz



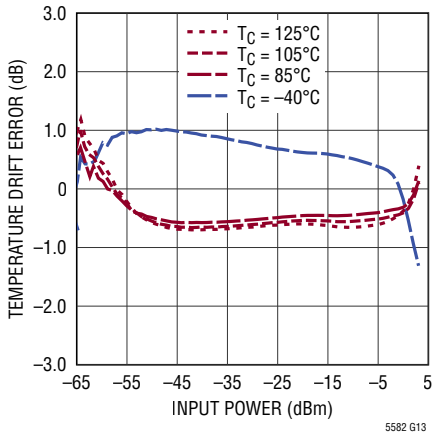
Linear Error vs RF Input Power, Modulated Waveforms, 2140MHz



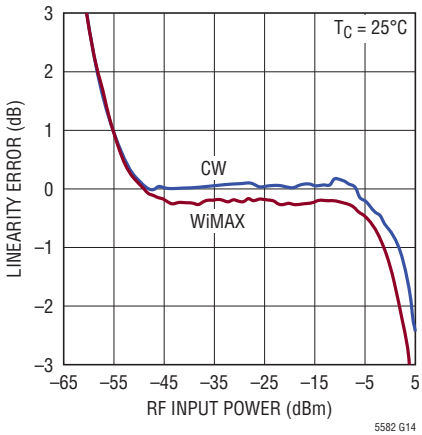
Output Voltage, Linearity Error vs RF Input Power, 2700MHz



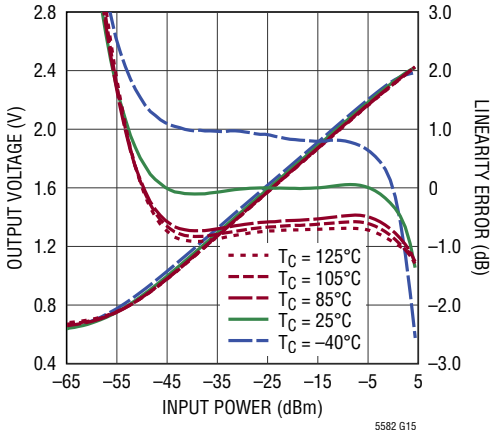
Output Voltage Temperature Variation from 25°C, 2700MHz



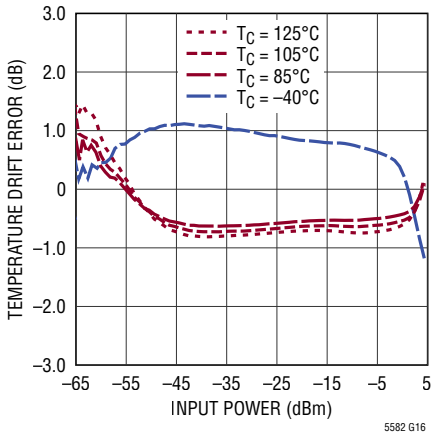
Linear Error vs RF Input Power, Modulated Waveforms, 2700MHz



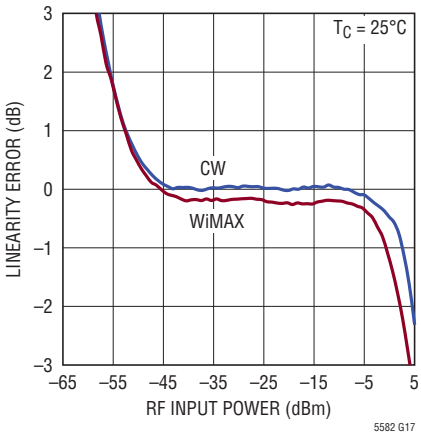
Output Voltage, Linearity Error vs RF Input Power, 3800MHz



Output Voltage Temperature Variation from 25°C, 3800MHz



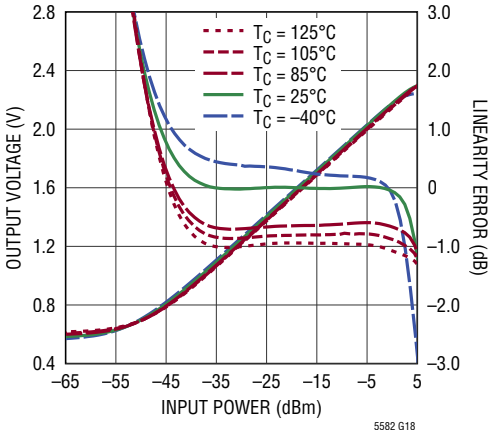
Linear Error vs RF Input Power, Modulated Waveforms, 3800MHz



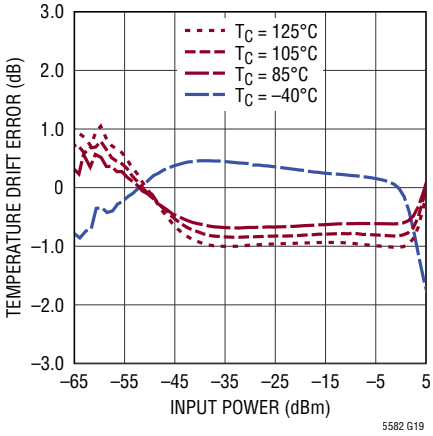
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, T_C = 25°C, R_{T1} = 0Ω, R_{T2} = 0Ω unless otherwise noted. Test circuits shown in Figure 1.

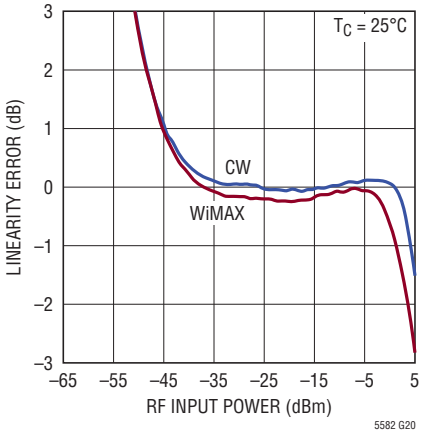
Output Voltage, Linearity Error vs RF Input Power, 5800MHz



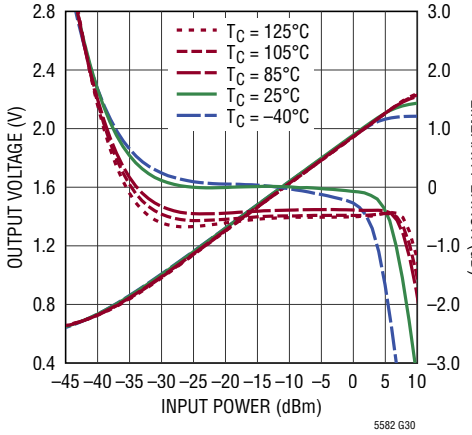
Output Voltage Temperature Variation from 25°C, 5800MHz



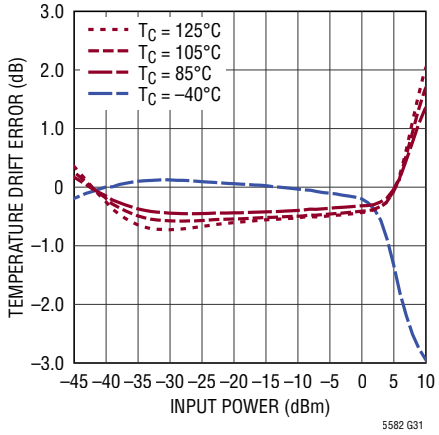
Linear Error vs RF Input Power, Modulated Waveforms, 5800MHz



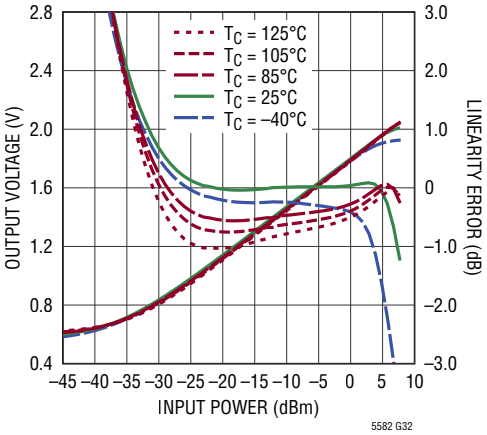
Output Voltage, Linearity Error vs RF Input Power, 8GHz



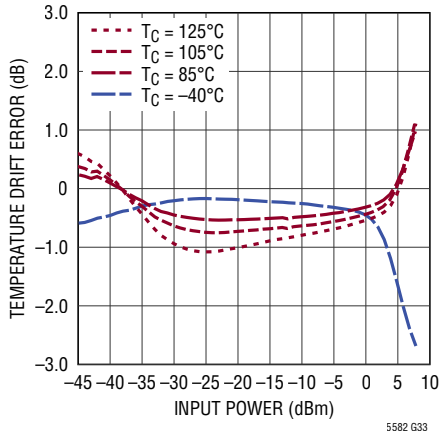
Output Voltage Temperature Variation from 25°C, 8GHz



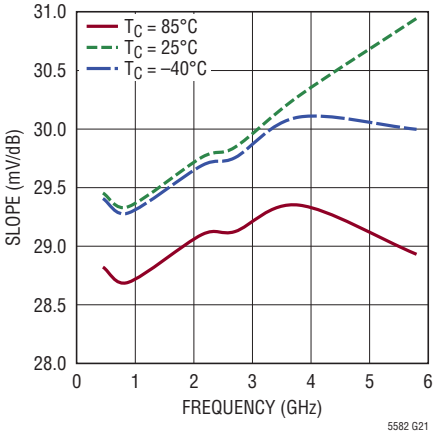
Output Voltage Linearity Error vs RF Input Power, 10GHz



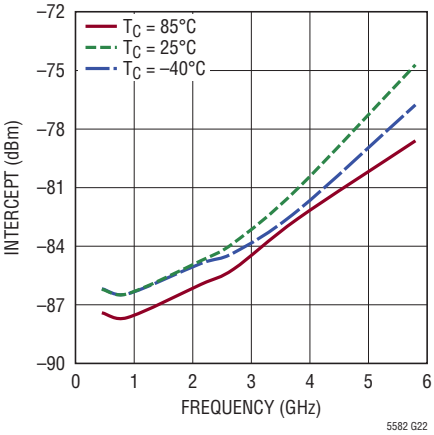
Output Voltage Temperature Variation from 25°C, 10GHz



Slope vs Frequency



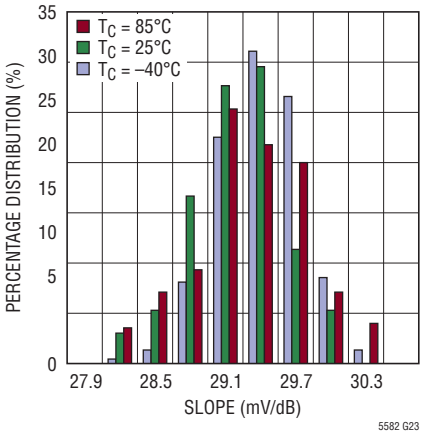
Logarithmic Intercept vs Frequency



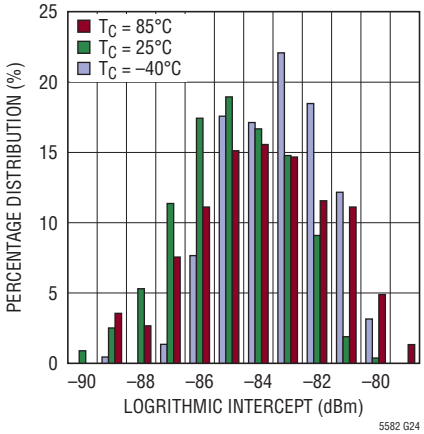
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 3.3V, EN = 3.3V, T_C = 25°C, R_{T1} = 0Ω, R_{T2} = 0Ω unless otherwise noted. Test circuits shown in Figure 1.

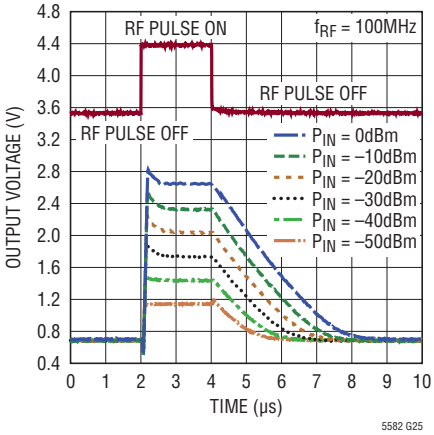
Slope Distribution vs Temperature, 2140MHz



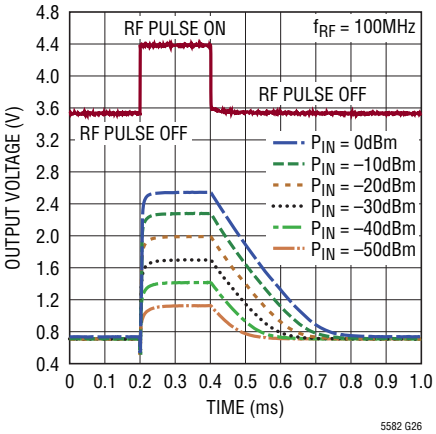
Logarithmic Intercept Distribution vs Temperature, 2140MHz



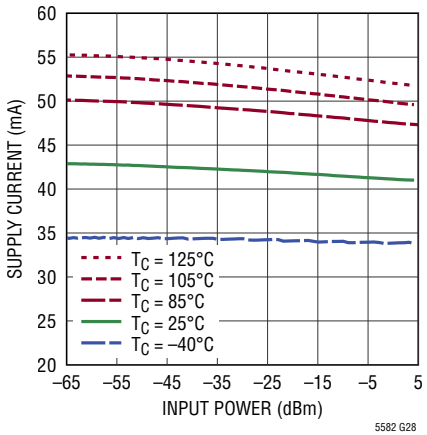
Output Transient Response, C3 = 8nF



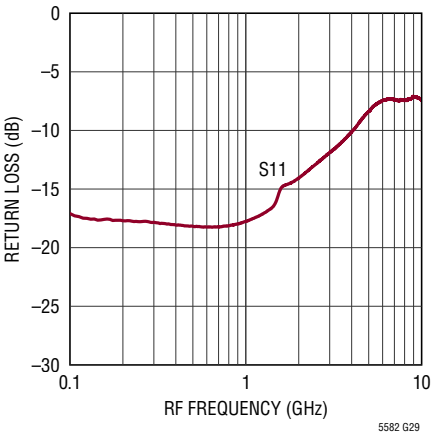
Output Transient Response, C3 = 1µF



Supply Current vs RF Input Power



RF Input Return Loss vs Frequency



PIN FUNCTIONS

V_{CC} (Pin 1): Power Supply Pin. Typical current consumption is 41.6mA at room temperature. This pin should be externally bypassed with 1nF and 1µF chip capacitors.

IN^+, IN^- (Pins 2, 4): Differential Input Signal Pins. Either one can be driven with a single-ended signal while the other is AC-coupled to ground. These pins can also be driven with a differential signal. The pins are internally biased to 1.585V and should be DC blocked externally. The differential impedance is typically 400Ω. The impedance of each pin to the DEC pin is 200Ω.

DEC (Pin 3): Input Common Mode Decoupling Pin. This pin is internally biased to 1.585V and connected to an on-chip 50pF capacitor to ground. The impedance between DEC and IN^+ (or IN^-) is 200Ω. The pin can be connected to the center tap of an external balun when terminated differentially. The pin can be floating or connected to ground via an AC-decoupling capacitor when driven either in single-ended or differential input configuration.

GND (Pin 5, Exposed Pad Pin 11): Circuit Ground Return for the Entire IC. This must be soldered to the printed circuit board ground plane.

OUT (Pin 6): DC Output Pin. The output impedance is mainly determined by an internal 100Ω series resistance which provides protection if the output is shorted to ground.

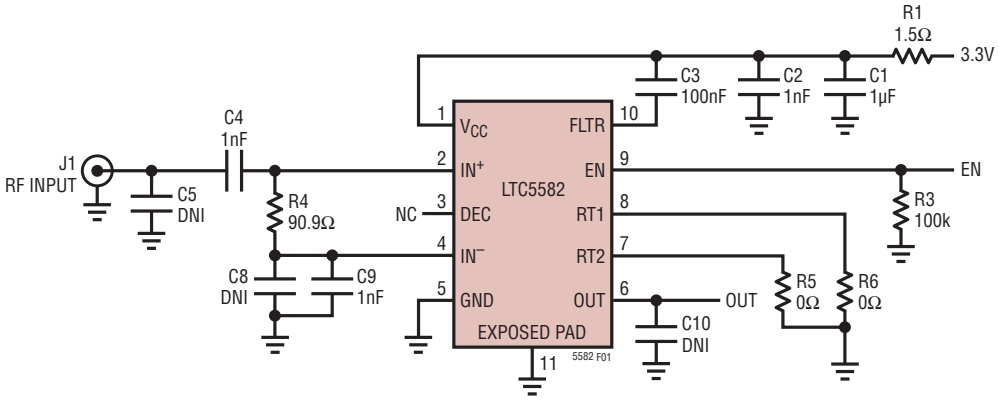
RT2 (Pin 7): Optional Control Pin for 2nd-Order Output Temperature Compensation. Connect this pin to ground to disable it. The output voltage will decrease with respect to the room temperature (25°C) by connecting it to ground via an off-chip resistor when the ambient temperature is either higher or lower.

RT1 (Pin 8): Optional Control Pin for 1st-Order Output Temperature Compensation. Connect this pin to ground to disable it. The output voltage will increase inversely proportional to ambient temperature.

EN (Pin 9): Enable Pin. An applied voltage above 1V will activate the bias for the IC. For an applied voltage below 0.4V, the circuits will be shut down (disabled) with a reduction in power supply current. If the enable function is not required, then this pin can be connected to V_{CC}. Typical enable pin input current is 100µA for EN = 3.3V. Note that at no time should the Enable pin voltage be allowed to exceed V_{CC} by more than 0.3V.

FLTR (Pin 10): Connection for an External Filtering Capacitor C3. A minimum of 8nF capacitance is required for stable AC average power measurement. This capacitor should be connected to V_{CC}.

TEST CIRCUITS



REF DES	VALUE	SIZE	PART NUMBER
C1	1uF	0402	MURATA GRM155R60J105KE19
C2	1nF	0402	MURATA GRM155R71H102KA01
C3	100nF	0402	TDK CID05X7R1C104K
C4	10nF	0402	PPI0402BB103KW500
C5	0.4pF	0402	MURATA GJM1555C1HR40BB01
C8	6.8pF	0402	MURATA GJM1555C1H6R8DB01
C9	180pF	0402	MURATA GRM1555C1H181JA01
R1	1.5Ω	0603	VISHAY CRCW06031R50JNEA
R3	100KΩ	0402	VISHAY CRCW0402100KFKED
R4	91Ω	0402	RK731ETTP90R9F
R5	2k	0402	VISHAY CRCW04022K00FKEA
R6	0	0402	VISHAY CRCW0402020000Z0ED

Figure 1. Test Schematic Optimized for 40MHz to 5500MHz in Single-Ended Input Configuration

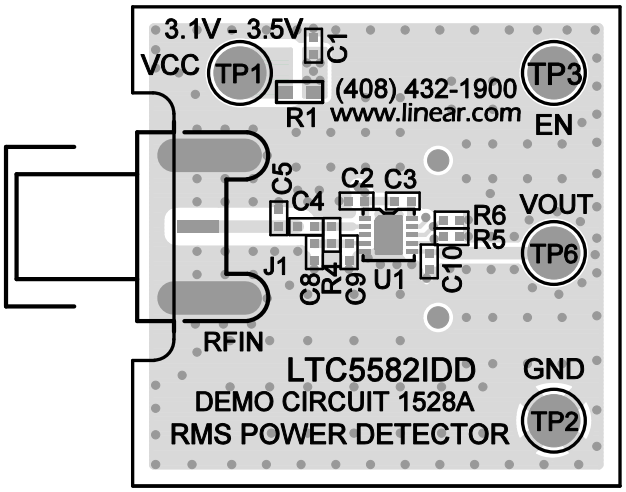


Figure 2. Top Side of Evaluation Board

APPLICATIONS INFORMATION

The LTC5582 is a true RMS RF power detector, capable of measuring an RF signal over the frequency range from 40MHz to 10GHz, independent of input waveforms with different crest factors such as CW, CDMA2K, WCDMA, LTE and WiMAX signals. Up to 60dB dynamic range is achieved with a very stable output within the full temperature range from –40°C to 125°C. Its sensitivity can be as low as –57dBm up to 2.7GHz even with single-ended 50Ω input termination.

RF Inputs

The differential RF inputs are internally biased at 1.585V. The differential impedance is 400Ω. These pins should be DC blocked when connected to ground or other matching components.

The LTC5582 can be driven in a single-ended configuration as illustrated in Figure 3. The single-ended input impedance vs frequency is detailed in Table 1. The DEC Pin can be either left floating or AC-coupled to ground via an external capacitor. While the RF signal is applied to the IN^+ (or IN^-) Pin, the other pin IN^- (or IN^+) should be AC-coupled to ground. By simply terminating a 91Ω resistor between the IN^+ and IN^- Pins and coupling the non-signal side to ground using a 1nF capacitor, broadband 50Ω input matching can be achieved with typical return loss better than 10dB from 40MHz to 5.5GHz. At higher RF frequencies, additional matching components may be needed.

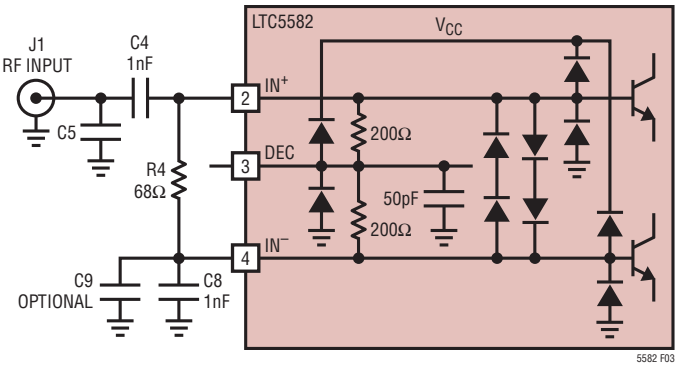


Figure 3. Single-Ended Input Configuration

Table 1. Single-Ended Input Impedance (DEC Floating)

FREQUENCY (MHZ)	INPUT IMPEDANCE (Ω)	S11	
		MAG	ANGLE (°)
40	220.7-j63.0	0.655	–7.0
100	195.2-j47.3	0.611	–7.1
200	175.1-j37.6	0.571	–7.3
400	200.9-j42.2	0.618	–6.3
600	159.8-j52.9	0.563	–11.5
800	154.8-j52.4	0.554	–12.2
1000	158.6-j57.1	0.568	–12.4
1200	164.1-j81.1	0.612	–14.7
1400	138.1-j110.5	0.650	–21.0
1600	102.7-j113.3	0.659	–28.5
1800	80.1-j103.1	0.647	–35.3
2000	67.1-j92.0	0.628	–41.3
2200	58.4-j82.3	0.607	–46.7
2400	52.9-j74.5	0.586	–52.0
2600	48.5-j67.6	0.566	–57.0
2800	44.8-j61.5	0.546	–62.0
3000	41.8-j56.1	0.526	–66.9
3200	41.8-j56.3	0.508	–72.0
3400	37.3-j47.0	0.490	–77.1
3600	35.4-j42.9	0.473	–80.2
3800	33.9-j39.1	0.457	–87.7
4000	32.4-j35.5	0.445	–93.1
4200	31.1-j32.3	0.429	–98.8
4400	29.9-j29.1	0.416	–104.7
4600	28.9-j26.2	0.405	–110.7
4800	27.9-j23.3	0.395	–117.0
5000	27.0-j20.5	0.388	–123.5
5200	26.2-j17.8	0.382	–130.2
5400	25.4-j15.2	0.376	–136.9
5600	24.7-j12.6	0.376	–144.1
5800	24.0-j10.0	0.377	–151.3
6000	23.3-j7.5	0.377	–158.4

The LTC5582 differential inputs can also be driven from a fully balanced source as shown in Figure 4. When the signal source is a single-ended 50Ω, conversion to a differential signal can be achieved using a 1:8 balun to match the internal 400Ω input impedance to the 50Ω source. This impedance transformation results in 9dB voltage gain, thus 9dB improvement in sensitivity is obtained

APPLICATIONS INFORMATION

while the overall dynamic range remains the same. At high frequency, additional LC elements may be needed for the input impedance matching due to the parasitics of the transformer and PCB traces.

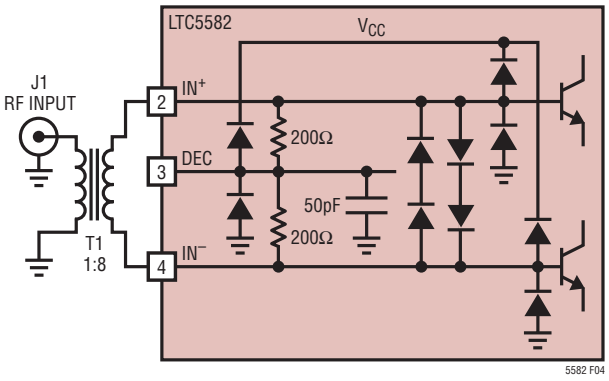


Figure 4. Differential Input Configuration

Due to the high input impedance of the LTC5582, a narrow band L-C matching network can be also used to convert a single-ended input to differential signal as shown in Figure 5. By this means, the sensitivity and overall linear dynamic range of the detector will be very similar to the one using 1:8 RF input balun. The conversion gain is strongly dependent on the loss (or Q) of the matching network, particularly at high frequency. The lower the Q, the lower the conversion gain. However, the matching bandwidth is correspondingly wider. The following formulas are provided to calculate the input matching network for single-ended-to-differential conversion at low RF frequency (i.e., below 1GHz).

$$C_{S1} = C_{S2} = \frac{1}{\pi fc\sqrt{50R_{IN}}} = \frac{2.25 \bullet 10^9}{fc} \quad (pF)$$

$$L_M = \frac{\sqrt{50R_{IN}}}{2\pi fc} = \frac{2.25 \bullet 10^{10}}{fc} \quad (nH)$$

where R_{IN} is the differential input resistance (400Ω) and fc is the center RF operating frequency.

As an example, Figure 6 shows that good input return loss is achieved from 300MHz to 400MHz when C_{S1} = C_{S2} = 6.8pF and L_M = 66nH. Figure 7 show the sensitivity is also improved by 8dB at 350MHz while the dynamic range remains the same.

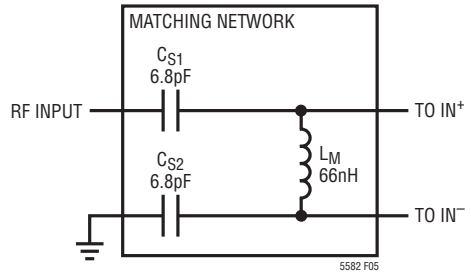


Figure 5. Single-Ended-to-Differential Conversion

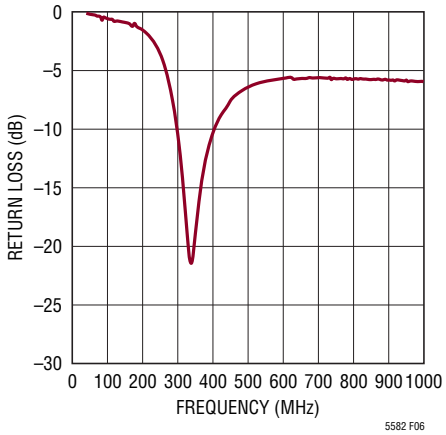


Figure 6. RF Input Return Loss

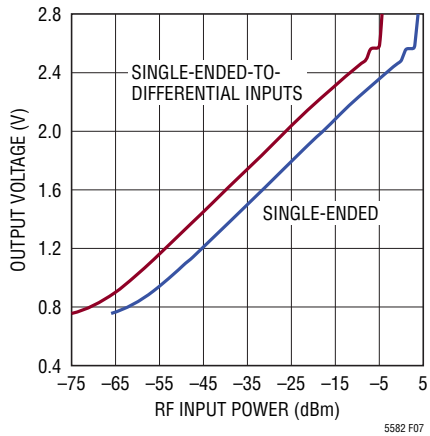


Figure 7. Output Voltage vs RF Input Power

Although these equations give a good starting point, it is usually necessary to adjust the component values after building and testing the circuit. As the RF operating frequency increases, the real values of C_{S1}, C_{S2}, L_M will deviate from the above equations due to parasitics of the components, device and PCB layout.

APPLICATIONS INFORMATION

For a 50Ω input termination, the approximate RF input power range of the LTC5582 is from –60dBm to 2dBm, even with high crest factor signals such as a 4-carrier W-CDMA waveform, and the minimum detectable RF power level varies as the input RF frequency increases. The linear dynamic range can also be shifted to suit a particular application need. By simply inserting an attenuator in front of the RF input, the power range is shifted higher by the amount of the attenuation.

The sensitivity of LTC5582 is dictated by the broadband input noise power that also determines the output DC offset voltage. When the inputs are terminated differently, the DC output voltage may vary slightly. When the input noise power is minimized, the DC offset voltage is also reduced to the minimum. And the detector's sensitivity and dynamic range will be improved accordingly.

External Filtering (FLTR) Capacitor

This pin is internally biased at V_{CC} – 0.43V via a 1.2k resistor from the voltage supply, V_{CC}. To assure stable operation of the LTC5582, an external capacitor C3 with a value of 8nF or higher is required to connect from the FLTR Pin to V_{CC} to avoid an abnormal start-up condition. Don't connect this filtering capacitor to ground or any other low voltage reference at any time.

This external capacitor value has a dominant effect on the output transient response. The lower the capacitance, the faster the output rise and fall times. For signals with AM content such as W-CDMA, significant ripple can be observed when the loop bandwidth set by C3 is close to the modulation bandwidth of the signal. A 4-carrier W-CDMA RF signal is used as an example in this case. The trade-offs of the residual ripple vs the output transient times are as shown in Figure 8.

In general, the LTC5582 output ripple remains relatively constant regardless of the RF input power level for a fixed C3 and modulation format of the RF signal. Typically, C3 must be selected to smooth out the ripple to achieve the desired accuracy of RF power measurement.

Output Interface

The output buffer amplifier of the LTC5582 is shown in Figure 9. This Class AB buffer amplifier can source and sink 5mA current to and from the load. The output impedance is determined primarily by the 100Ω series resistor connected to the output of the buffer amplifier inside the chip. This will prevent overstress on internal devices in the event that the output is shorted to ground.

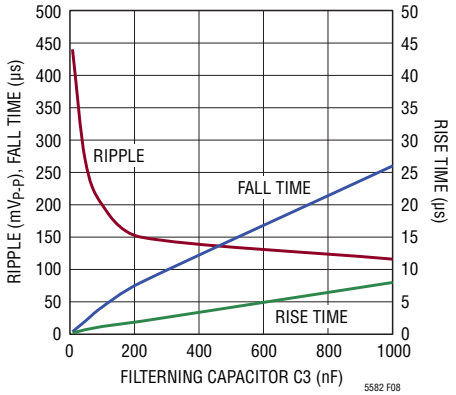


Figure 8. Residual Ripple, Output Transient Times vs Filtering Capacitor C3

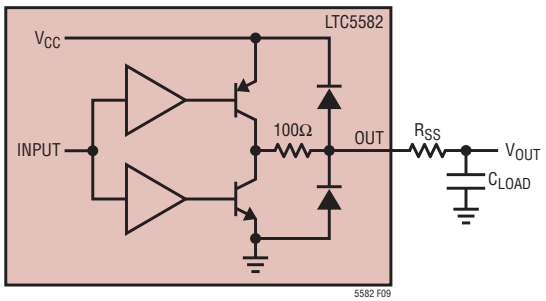


Figure 9. Simplified Schematic of the Output Interface

The –3dB small-signal bandwidth of the buffer amplifier is about 22.4MHz and the full-scale rise/fall time can be as fast as 80ns, limited by the slew rate of the internal circuit instead. When the output is resistively terminated or open, the fastest output transient response is achieved when a large signal is applied to the RF input. The rise time of the LTC5582 is about 90ns and the fall time is 5µs, respectively, for full-scale pulsed RF input power when C3 = 8nF. The speed of the output transient response is dictated mainly by the filtering capacitor C3 (at least 8nF) at the FLTR Pin. See the detailed output transient response in the Typical Performance Characteristics section. When the RF input has AM content, residual ripple may be present at the output depending upon the low frequency content of the modulated RF signal. This ripple can be reduced with a

APPLICATIONS INFORMATION

larger filtering capacitor C3 at the expense of a slower transient response.

Since the output buffer amplifier of the LTC5582 is capable of driving an arbitrary capacitive load, the residual ripple can be further filtered at the output with a series resistor R_{SS} and a large shunt capacitor C_{LOAD}. See Figure 9. This lowpass filter also reduces the output noise by limiting the output noise bandwidth. When this RC network is designed properly, a fast output transient response can be maintained with a reduced residual ripple. For example, we can estimate C_{LOAD} with an output voltage swing of 1.7V at 2140MHz. In order not to allow the maximum 5mA souring current to limit the fall time (about 5µs), the maximum value of C_{LOAD} can be chosen as follows:

$$C_{LOAD} \le 5mA \bullet \frac{\text{allowable additional time}}{1.7V} =$$

$$5mA \bullet \frac{0.25\mu s}{1.7V} = 735pF$$

Once C_{LOAD} is determined, R_{SS} can be chosen properly to form a RC low-pass filter with a corner frequency of $1/[2\pi(R_{SS} + 100) \bullet C_{LOAD}]$.

In general, the rise time of the LTC5582 is much shorter than the fall time. However, when the output RC filter is used, the rise time can be dominated by the time constant of this filter. Accordingly, the rise time becomes very similar to the fall time. Although the maximum sinking capability of the LTC5582 is 5mA, it is recommended that the output load resistance should be greater than 1.2k in order to achieve the full output voltage swing.

Temperature Compensation of Logarithmic Intercept

The simplified interface schematic of the intercept temperature compensation is shown in Figure 10. The adjustment of the output voltage can be described by the following equation with respect to the ambient temperature:

$$\Delta V_{OUT} = -TC1 \bullet (T_A - T_{NOM}) - TC2 \bullet (T_A - T_{NOM})^2 - detV1 - detV2$$

where TC1 and TC2 are the 1st-order and 2nd-order temperature compensation coefficients, respectively; T_A is the actual ambient temperature; and T_{NOM} is the reference room temperature; detV1 and detV2 are the output voltage variations when R_{T1} and R_{T2} are not set to zero at room temperature. The temperature coefficients TC1 and

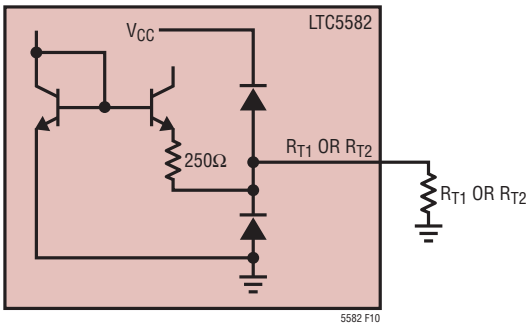


Figure 10. Simplified Interface Circuit Schematic of the Control Pins R_{T1} and R_{T2}

TC2 are shown as functions of the tuning resistors R_{T1} and R_{T2} in Figures 11 and 12, respectively.

When Pins RT1 and RT2 are shorted to ground, the temperature compensation circuit is disabled automatically. Table 2 lists the suggested R_{T1} and R_{T2} values at various

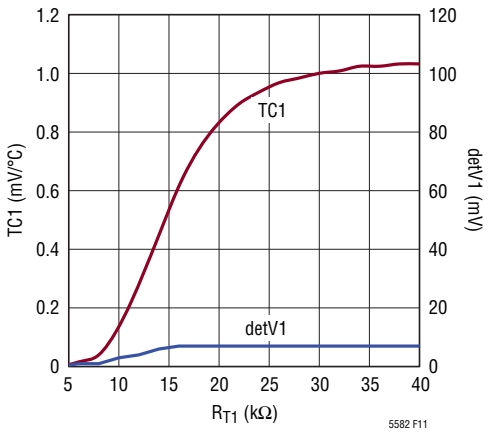


Figure 11. 1st-Order Temperature Compensation Coefficient TC1 vs R_{T1} Value

RF frequencies for the best output performance over temperature.

Table 2. Suggested R_{T1} and R_{T2} Values for Optimal Temperature Performance vs RF Frequency

FREQUENCY (MHz)	R_{T1} (kΩ)	R_{T2} (kΩ)
450	12	2
880	12	2
2140	0	2
2700	0	1.6

Rev. C

APPLICATIONS INFORMATION

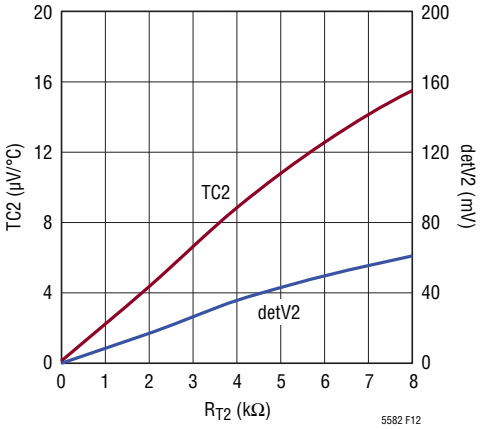


Figure 12. 2nd-Order Temperature Compensation Coefficient TC2 vs R_{T2} Value

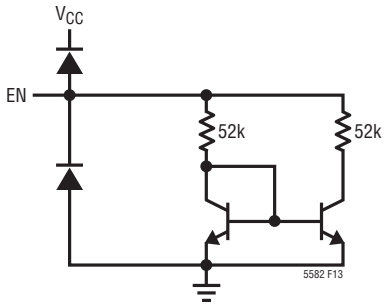


Figure 13. Enable Pin Simplified Circuit

3600	0	1.6
5800	0	3

Enable Interface

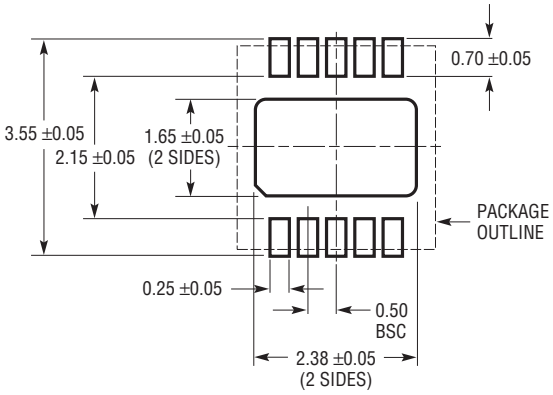
A simplified schematic of the EN Pin interface is shown in Figure 13. The enable voltage necessary to turn on the LTC5582 is 1V. To disable or turn off the chip, this voltage should be below 0.4V. It is important that the voltage applied to the EN pin should never exceed V_{CC} by more than 0.3V. Otherwise, the supply current may be sourced through the upper ESD protection diode connected at the EN pin. Under no circumstances should voltage be applied to the EN Pin before the supply voltage is applied to the V_{CC} pin. If this occurs, damage to the IC may result.

Supply Voltage Ramping

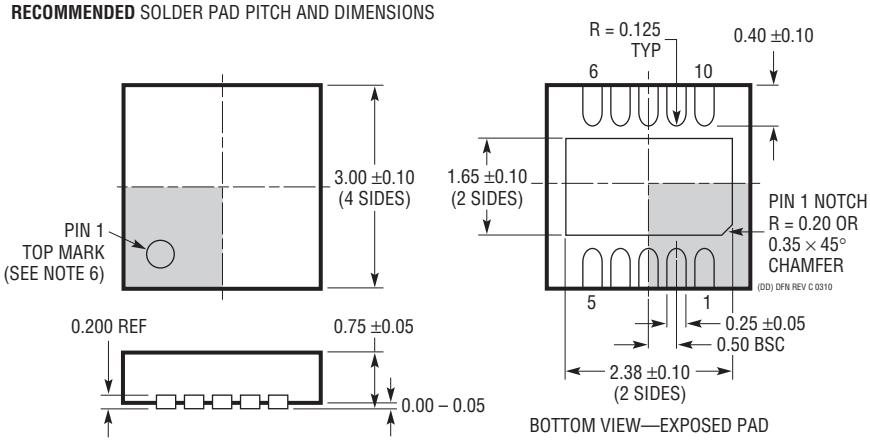
Fast ramping of the supply voltage can cause a current glitch in the internal ESD protection circuits. Depending on the supply inductance, this could result in a supply voltage overshooting at the initial transient that exceeds the maximum rating. A supply voltage ramp time of greater than 1ms is recommended. In case this voltage ramp time is not controllable, a small (i.e., 1.5Ω) series resistor should be inserted in-between V_{CC} Pin and the supply voltage source to mitigate the problem and self-protect the IC. The R1 shown in Figure 1 is served for this purpose.

PACKAGE DESCRIPTION

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS



BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	06/18	Changed LTC5582IDD#PBF and LTC5582IDD#TRPBF temperature range to –40°C to 105°C. Added a LTC5582HDD#PBF and LTC5582HDD#TRPBF grade with temperature range of –40°C to 125°C. Extended Typical Performance Characteristics plots to include 125°C case, where applicable.	2
B	11/19	Add automotive-qualified versions of this product.	1, 2
C	11/22	Schematic and Evaluation Board part list corrections.	10, 11