IEEE 802.3at PD with Synchronous No-Opto Flyback Controller and 12V Aux Support

FEATURES

- **25.5W IEEE 802.3at Compliant (Type 2) PD**
- **10V to 57V Auxiliary Power Input**
- **Shutdown Pin for Flexible Auxiliary Power Support**
- **Integrated State-of-the-Art No-Opto Synchronous Flyback Controller**
  - **Isolated Power Supply Efficiency >92%**
  - **88% Efficiency Including Diode Bridge and Hot Swap™ FET**
- **Superior EMI Performance**
- **Robust 100V 0.7Ω (Typ) Integrated Hot Swap MOSFET**
- IEEE 802.3at *High Power Available* Indicator
- Integrated Signature Resistor and Programmable Class Current
- Undervoltage, Overvoltage and Thermal Protection
- Short-Circuit Protection with Auto-Restart
- Programmable Soft-Start and Switching Frequency
- Complementary Power Good Indicators
- Thermally Enhanced 7mm × 4mm DFN Package

APPLICATIONS

- VoIP Phones with Advanced Display Options
- Dual-Radio Wireless Access Points
- PTZ Security Cameras
- RFID Readers
- Industrial Controls

DESCRIPTION

The LTC®4278 is an integrated Powered Device (PD) controller and switching regulator intended for high power IEEE 802.3at and 802.3af applications. With a wide input voltage range, the LTC4278 is specifically designed to support PD applications that include a low-voltage auxiliary power input such as a 12V wall adaptor. The inclusion of a shutdown pin provides simple implementation of both PoE and auxiliary dominate applications. In addition, the LTC4278 supports both 1-event and 2-event classifications as defined by the IEEE, thereby allowing the use in a wide range of product configurations.

The LTC4278 synchronous, current mode, flyback controller generates multiple supply rails in a single conversion step providing for the highest system efficiency while maintaining tight regulation across all outputs. The LTC4278 includes Linear Technology's patented No-Opto feedback topology to provide full IEEE 802.3 isolation without the need of an opto-isolator circuit. A true soft-start function allows graceful ramp-up of all output voltages.

The LTC4278 is available in a space saving 32-lead DFN package.

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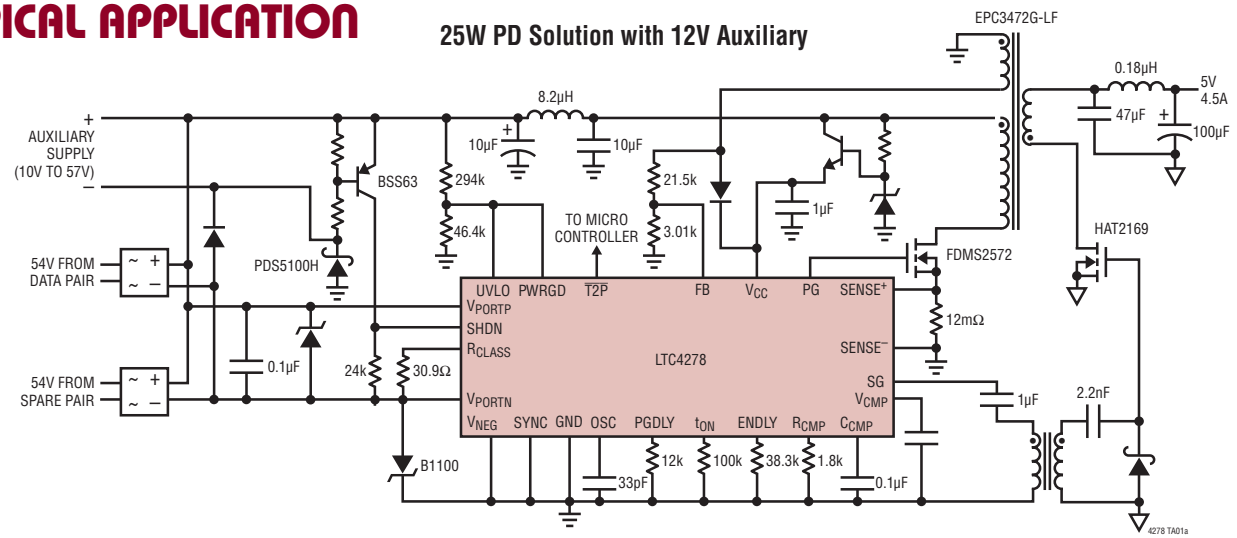
TYPICAL APPLICATION

25W PD Solution with 12V Auxiliary



ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Pins with Respect to V_{PORTN}

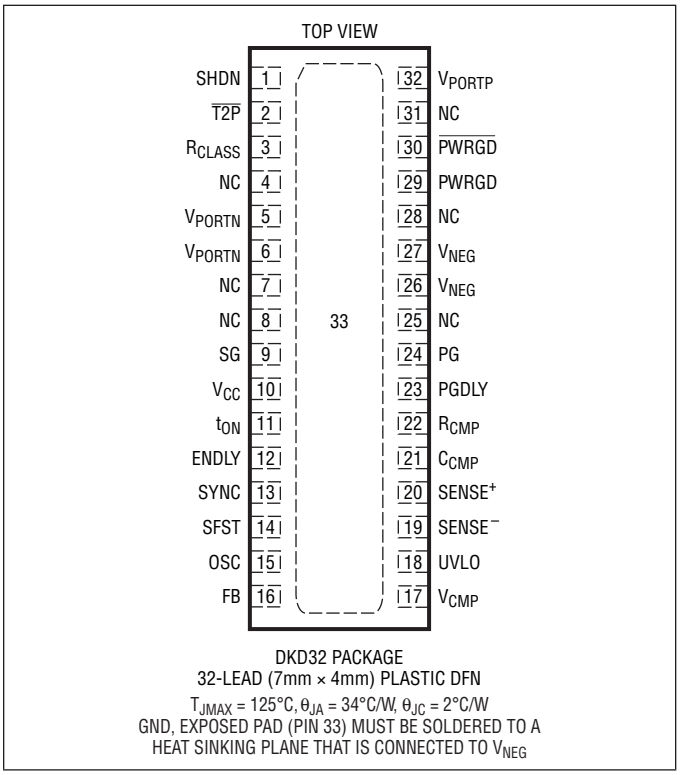
V_{PORTP} Voltage ..... –0.3V to 100V
V_{NEG} Voltage ..... –0.3V to V_{PORTP}
V_{NEG} Pull-Up Current 1A
SHDN ..... –0.3V to 100V
R_{CLASS}, Voltage ..... –0.3V to 7V
R_{CLASS} Source Current 50mA
PWRGD Voltage (Note 3)
  Low Impedance Source ..... V_{NEG} –0.3V to V_{NEG} +11V
  Sink Current 5mA
$\overline{PWRGD}$, $\overline{T2P}$ Voltage ..... –0.3V to 100V
$\overline{PWRGD}$, $\overline{T2P}$ Sink Current 10mA

Pins with Respect to GND

V_{CC} Voltage ..... –0.3V to 22V
$SENSE^-$, $SENSE^+$ Voltage ..... –0.5V to +0.5V
UVLO, SYNC Voltage ..... –0.3V to V_{CC}
FB Current ..... ±2mA
V_{CMP} Current ..... ±1mA

Operating Ambient Temperature Range
  LTC4278C ..... 0°C to 70°C
  LTC4278I ..... –40°C to 85°C

PIN CONFIGURATION



DKD32 PACKAGE
32-LEAD (7mm × 4mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W, θ_{JC} = 2°C/W
GND, EXPOSED PAD (PIN 33) MUST BE SOLDERED TO A HEAT SINKING PLANE THAT IS CONNECTED TO V_{NEG}

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4278CDKD#PBF	LTC4278CDKD#TRPBF	4278	32-Lead (7mm × 4mm) Plastic DFN	0°C to 70°C
LTC4278IDKD#PBF	LTC4278IDKD#TRPBF	4278	32-Lead (7mm × 4mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Interface Controller (Note 4)						
Operating Input Voltage	At V_{PORTP} (Note 5)				60	V
Signature Range		●	1.5		9.8	V
Classification Range		●	12.5		21	V
ON Voltage		●			37.2	V
OFF Voltage		●	30.0			V
Overvoltage Lockout				71		V
ON/OFF Hysteresis Window		●	4.1			V
Signature/Class Hysteresis Window		●	1.4			V
Reset Threshold	State Machine Reset for 2-Event Classification	●	2.57		5.40	V
Supply Current						
Supply Current at 57V	Measured at V_{PORTP} Pin	●			1.35	mA
Class 0 Current	V_{PORTP} = 17.5V, No R_{CLASS} Resistor	●			0.40	mA
Signature						
Signature Resistance	1.5V ≤ V_{PORTP} ≤ 9.8V (Note 6)	●	23.25		26	kΩ
Invalid Signature Resistance, SHDN Invoked	1.5V ≤ V_{PORTP} ≤ 9.8V, V_{SHDN} = 3V (Note 6)	●			11	kΩ
Invalid Signature Resistance During Mark Event	(Notes 6, 7)	●			11	kΩ
Classification						
Class Accuracy	10mA < I_{CLASS} < 40mA, 12.5V < V_{PORTP} < 21V (Notes 8, 9)	●			±3.5	%
Classification Stability Time	V_{PORTP} Pin Step to 17.5V, R_{CLASS} = 30.9, I_{CLASS} Within 3.5% of Ideal Value (Notes 8, 9)	●			1	ms
Normal Operation						
Inrush Current	V_{PORTP} = 54V, V_{NEG} = 3V	●	60	100	180	mA
Power FET On-Resistance	Tested at 600mA into V_{NEG}, V_{PORTP} = 54V	●		0.7	1.0	Ω
Power FET Leakage Current at V_{NEG}	V_{PORTP} = SHDN = V_{NEG} = 57V	●			1	µA
Digital Interface						
SHDN Input High Level Voltage		●	3			V
SHDN Input Low Level Voltage		●			0.45	V
SHDN Input Resistance	V_{PORTP} = 9.8V, SHDN = 9.65V	●	100			kΩ
$\overline{PWRGD}$, $\overline{T2P}$ Output Low Voltage	Tested at 1mA, V_{PORTP} = 54V. For $\overline{T2P}$, Must Complete 2-Event Classification to See Active Low	●			0.15	V
$\overline{PWRGD}$, $\overline{T2P}$ Leakage Current	Pin Voltage Pulled 57V, V_{PORTP} = V_{PORTN} = 0V	●			1	µA
PWRGD Output Low Voltage	Tested at 0.5mA, V_{PORTP} = 52V, V_{NEG} = 48V, Output Voltage Is With Respect to V_{NEG}	●			0.4	V
PWRGD Clamp Voltage	Tested at 2mA, V_{NEG} = 0V, Voltage With Respect to V_{NEG}	●	12		16.5	V
PWRGD Leakage Current	V_{PWRGD} = 11V, V_{NEG} = 0V, Voltage With Respect to V_{NEG}	●			1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PWM Controller (Note 10)						
Power Supply						
V_{CC} Operating Range		●	4.5		20	V
V_{CC} Supply Current (I_{CC})	V_{CMP} = Open (Note 11)	●	4	6.4	10	mA
V_{CC} Shutdown Current	V_{CMP} = Open, V_{UVLO} = 0V	●		50	150	µA
Feedback Amplifier						
Feedback Regulation Voltage (V_{FB})		●	1.220	1.237	1.251	V
Feedback Pin Input Bias Current	R_{CMP} Open			200		nA
Feedback Amplifier Transconductance	ΔI_C = ±10µA	●	700	1000	1400	µmho
Feedback Amplifier Source or Sink Current		●	25	55	90	µA
Feedback Amplifier Clamp Voltage	V_{FB} = 0.9V V_{FB} = 1.4V			2.56 0.84		V V
Reference Voltage Line Regulation	12V ≤ V_{CC} ≤ 18V	●		0.005	0.05	%/V
Feedback Amplifier Voltage Gain	V_{CMP} = 1.2V to 1.7V			1400		V/V
Soft-Start Charging Current	V_{SFST} = 1.5V		16	20	25	µA
Soft-Start Discharge Current	V_{SFST} = 1.5V, V_{UVLO} = 0V		0.7	1.3		mA
Control Pin Threshold (V_{CMP})	Duty Cycle = Min			1		V
Gate Outputs						
PG, SG Output High Level		●	6.6	7.4	8	V
PG, SG Output Low Level		●		0.01	0.05	V
PG, SG Output Shutdown Strength	V_{UVLO} = 0V; I_{PG}, I_{SG} = 20mA	●		1.6	2.3	V
PG Rise Time	C_{PG} = 1nF			11		ns
SG Rise Time	C_{SG} = 1nF			15		ns
PG, SG Fall Time	C_{PG}, C_{SG} = 1nF			10		ns
Current Amplifier						
Switch Current Limit at Maximum V_{CMP}	V_{SENSE}^+	●	88	98	110	mV
$\Delta V_{SENSE}/\Delta V_{CMP}$				0.07		V/V
Sense Voltage Overcurrent Fault Voltage	V_{SENSE}^+, V_{SFST} < 1V	●		206	230	mV
Timing						
Switching Frequency (f_{OSC})	C_{OSC} = 100pF	●	84	100	110	kHz
Oscillator Capacitor Value (C_{OSC})	(Note 12)		33		200	pF
Minimum Switch On Time ($t_{ON(MIN)}$)				200		ns
Flyback Enable Delay Time (t_{ENDLY})				265		ns
PG Turn-On Delay Time (t_{PGDLY})				200		ns
Maximum Switch Duty Cycle		●	85	88		%
SYNC Pin Threshold		●		1.53	2.1	V
SYNC Pin Input Resistance				40		kΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Load Compensation						
Load Compensation to V_{SENSE} Offset Voltage	V_{RCMP} with V_{SENSE}^+ = 0V			0.8		mV
Feedback Pin Load Compensation Current	V_{SENSE}^+ = 20mV, V_{FB} = 1.230V			20		µA
UVLO Function						
UVLO Pin Threshold (V_{UVLO})		●	1.215	1.240	1.265	V
UVLO Pin Bias Current	V_{UVLO} = 1.2V V_{UVLO} = 1.3V		–0.25 –4.50	0.1 –3.4	0.25 –2.50	µA µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Pins with 100V absolute maximum guaranteed for T ≥ 0°C, otherwise 90V.

Note 3: Active high PWRGD internal clamp self-regulates to 14V with respect to V_{NEG}.

Note 4: All voltages are with respect to V_{PORTN} pin unless otherwise noted.

Note 5: Input voltage specifications are defined with respect to LTC4278 pins and meet IEEE 802.3af/at specifications when the input diode bridge is included.

Note 6: Signature resistance is measured via the ΔV/ΔI method with the minimum ΔV of 1V. The LTC4278 signature resistance accounts for the additional series resistance in the input diode bridge.

Note 7: An invalid signature after the 1st classification event is mandated by the IEEE802.3at standard. See the Applications Information section.

Note 8: Class accuracy is with respect to the ideal current defined as 1.237/R_{CLASS} and does not include variations in R_{CLASS} resistance.

Note 9: This parameter is assured by design and wafer level testing.

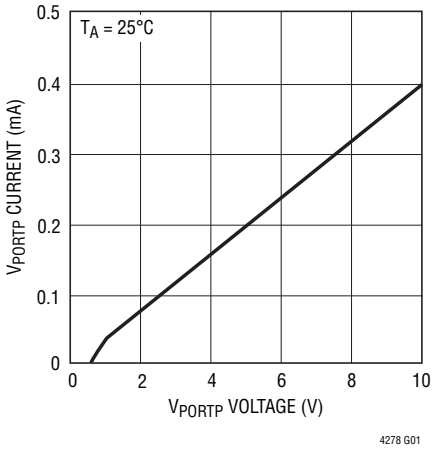
Note 10: V_{CC} = 14V; PG, SG Open; V_{CMP} = 1.4V, V_{SENSE}^- = 0V, R_{CMP} = 1k, R_{tON} = 90k, R_{PGDLY} = 27.4k, R_{ENDLY} = 90k, unless otherwise specified. All voltages are with respect to GND.

Note 11: Supply current does not include gate charge current to the MOSFETs. See the Applications Information section.

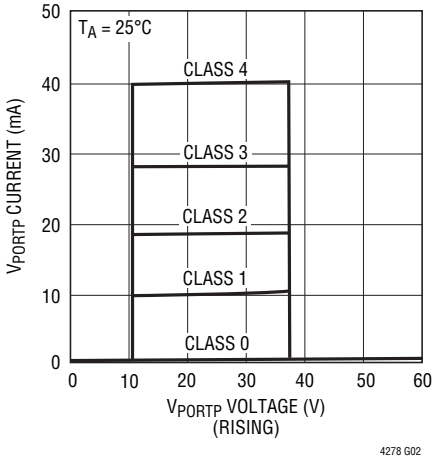
Note 12: Component value range guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

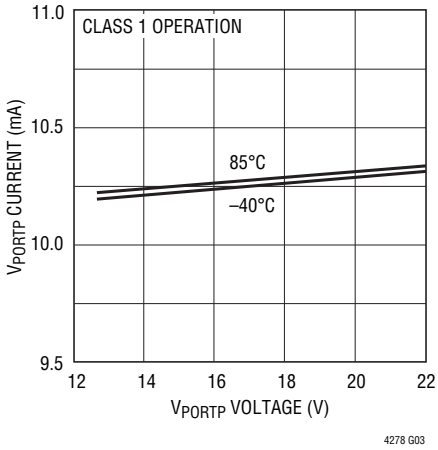
Input Current vs Input Voltage 25k Detection Range



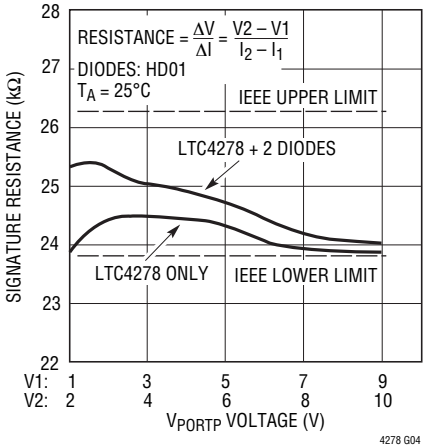
Input Current vs Input Voltage



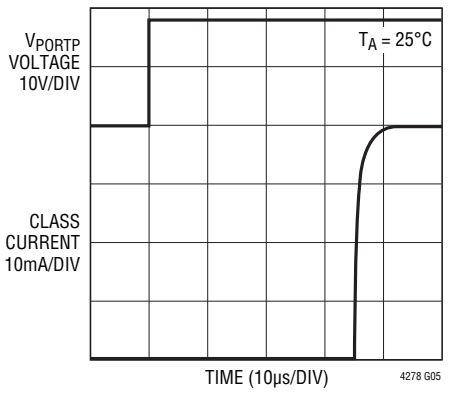
Input Current vs Input Voltage



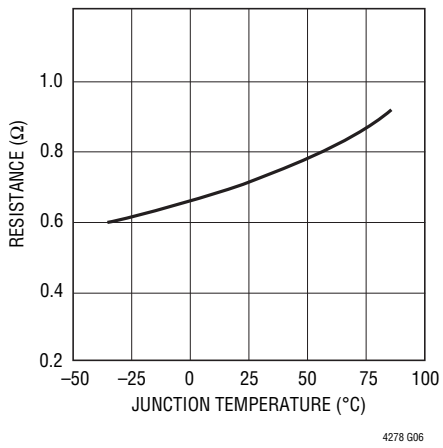
Signature Resistance vs Input Voltage



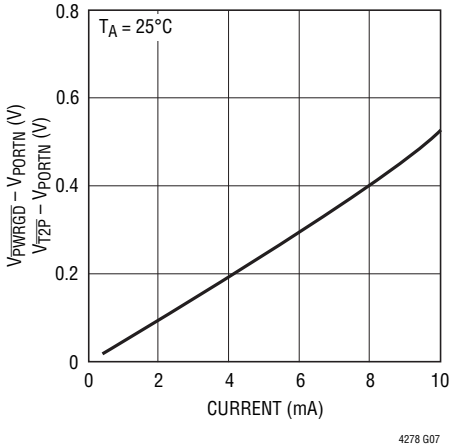
Class Operation vs Time



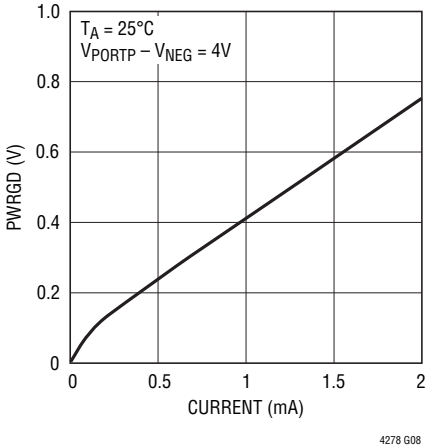
On-Resistance vs Temperature



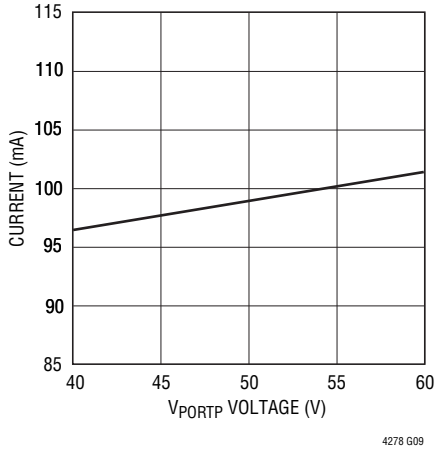
$\overline{PWRGD}$, $\overline{T2P}$ Output Low Voltage vs Current



Active High PWRGD Output Low Voltage vs Current

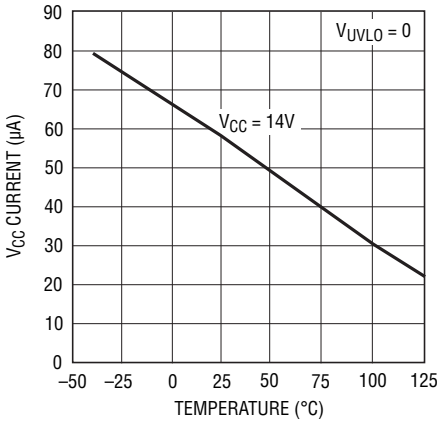


Inrush Current vs Input Voltage

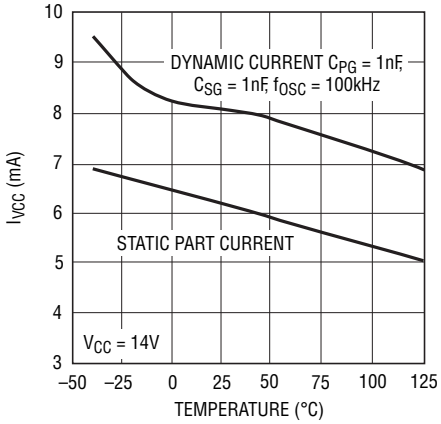


TYPICAL PERFORMANCE CHARACTERISTICS

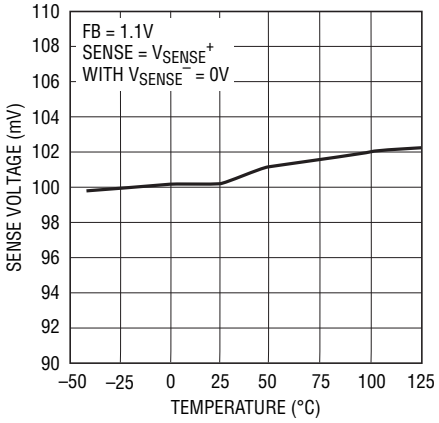
V_{CC} Shutdown Current vs Temperature



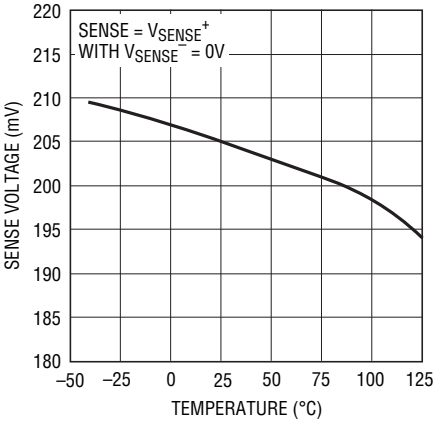
V_{CC} Current vs Temperature



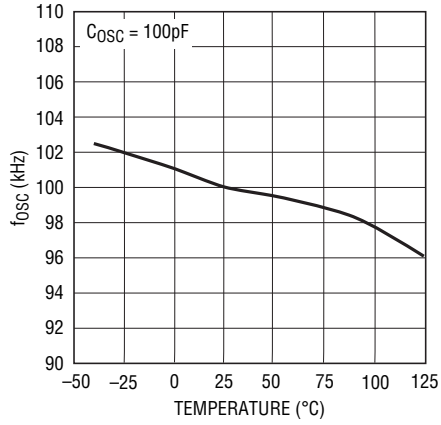
SENSE Voltage vs Temperature



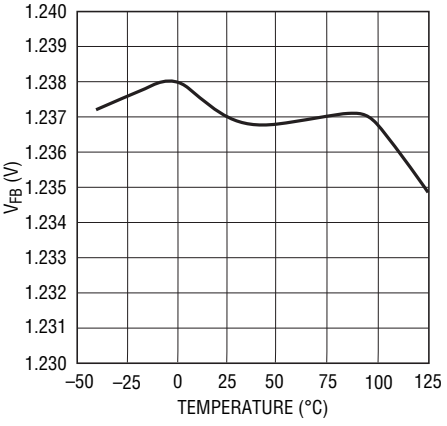
SENSE Fault Voltage vs Temperature



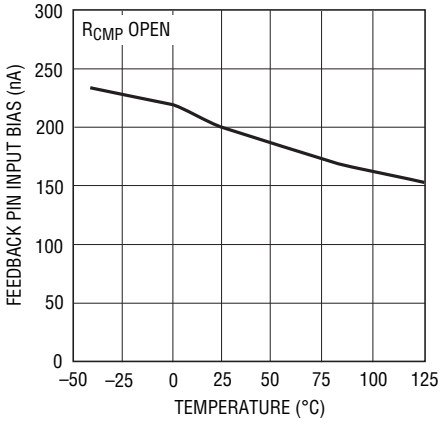
Oscillator Frequency vs Temperature



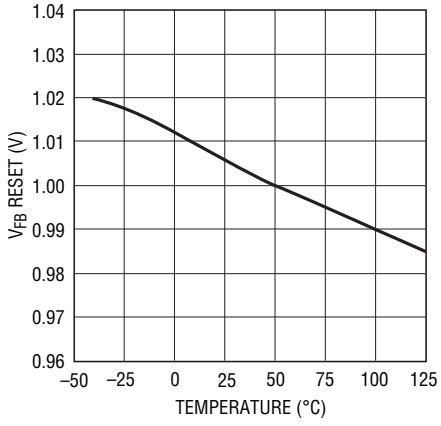
V_{FB} vs Temperature



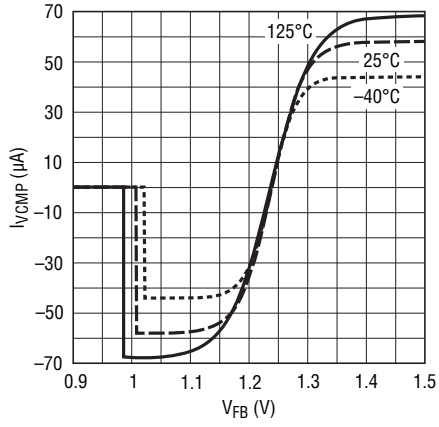
Feedback Pin Input Bias vs Temperature



V_{FB} Reset vs Temperature

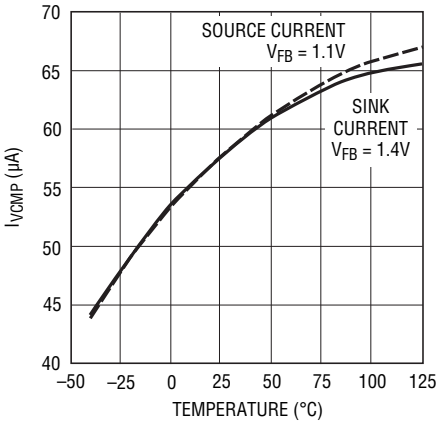


Feedback Amplifier Output Current vs V_{FB}

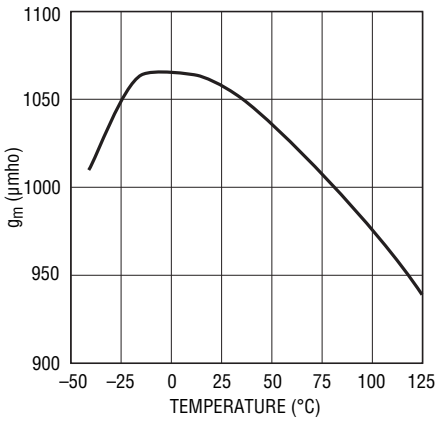


TYPICAL PERFORMANCE CHARACTERISTICS

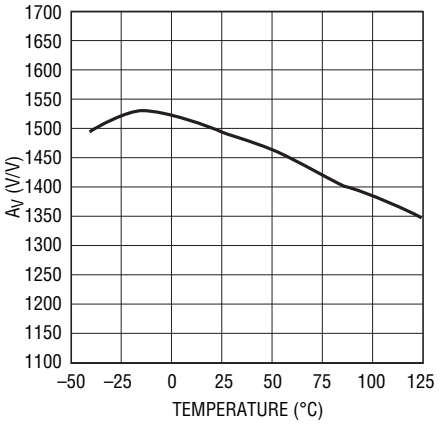
Feedback Amplifier Source and Sink Current vs Temperature



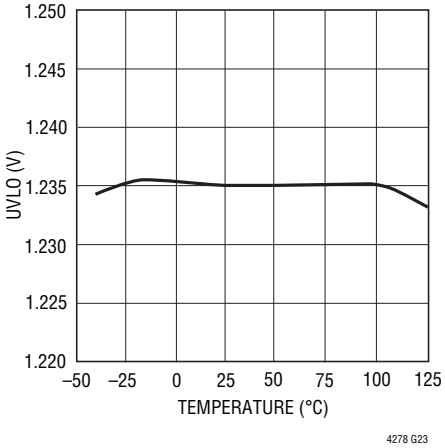
Feedback Amplifier g_m vs Temperature



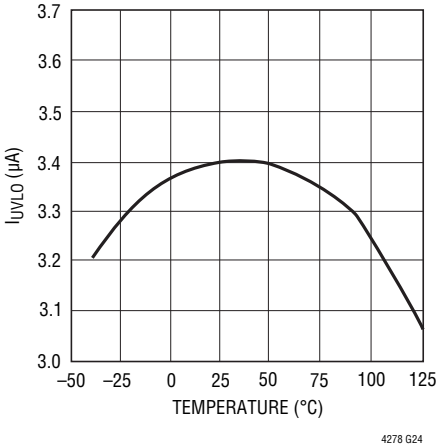
Feedback Amplifier Voltage Gain vs Temperature



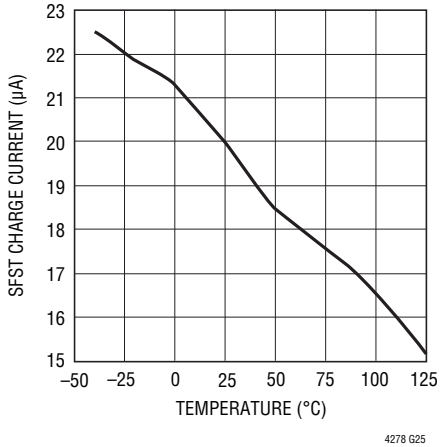
UVLO vs Temperature



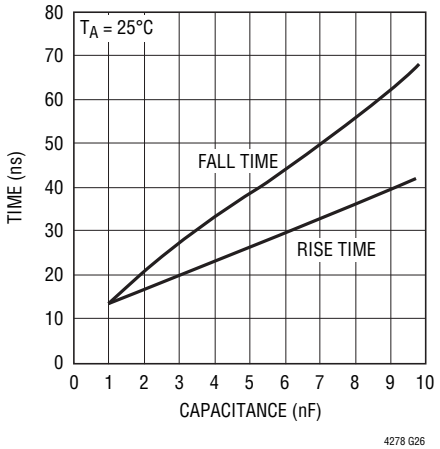
I_{UVLO} Hysteresis vs Temperature



Soft-Start Charge Current vs Temperature

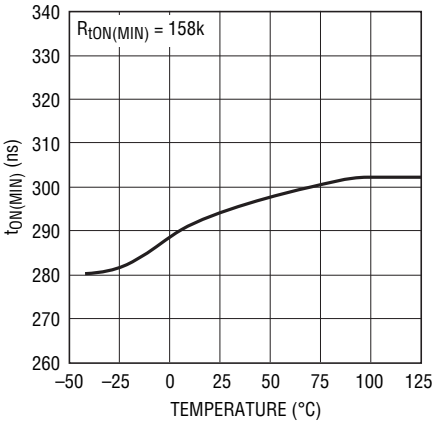


PG, SG Rise and Fall Times vs Load Capacitance

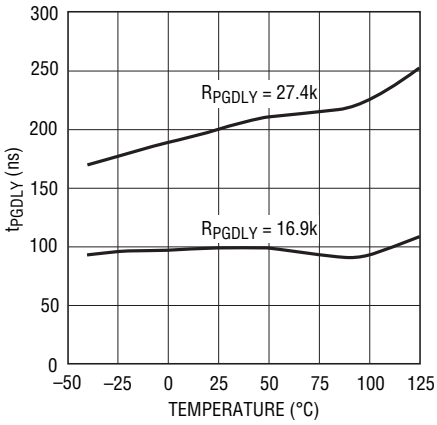


TYPICAL PERFORMANCE CHARACTERISTICS

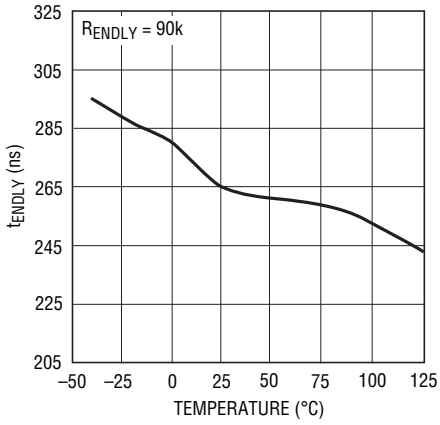
Minimum PG On-Time vs Temperature



PG Delay Time vs Temperature



Enable Delay Time vs Temperature



PIN FUNCTIONS

SHDN (Pin 1): Shutdown Input. Use this pin for auxiliary power application. Drive SHDN high to disable LTC4278 operation and corrupt the signature resistance. If unused, tie SHDN to V_{PORTN}.

$\overline{T2P}$ (Pin 2): Type 2 PSE Indicator, Open-Drain. Low impedance indicates the presence of a Type 2 PSE.

R_{CLASS} (Pin 3): Class Select Input. Connect a resistor between R_{CLASS} and V_{PORTN} to set the classification load current (see Table 2).

NC (Pins 4, 7, 8, 25, 28, 31): No Connect.

V_{PORTN} (Pins 5, 6): Input Voltage, Negative Rail. Pin 5 and Pin 6 must be electrically tied together at the package.

SG (Pin 9): Synchronous Gate Drive Output. This pin provides an output signal for a secondary-side synchronous rectifier. Large dynamic currents may flow during voltage transitions. See the Applications Information section for details.

V_{CC} (Pin 10): Supply Voltage Pin. Bypass this pin to GND with a low ESR ceramic capacitor. See the Applications Information section for details.

t_{ON} (Pin 11): Pin for external programming resistor to set the minimum time that the primary switch is on for each cycle. Minimum turn-on facilitates the isolated feedback method. See the Applications Information section for details.

ENDLY (Pin 12): Pin for external programming resistor to set enable delay time. The enable delay time disables the feedback amplifier for a fixed time after the turn-off of the primary-side MOSFET. This allows the leakage inductance voltage spike to be ignored for flyback voltage sensing. See the Applications Information section for details.

SYNC (Pin 13): External Sync Input. This pin is used to synchronize the internal oscillator with an external clock. The positive edge of the clock causes the oscillator to discharge causing PG to go low (off) and SG high (on). The sync threshold is typically 1.5V. Tie to ground if unused. See the Applications Information section for details.

SFST (Pin 14): Soft-Start. This pin, in conjunction with a capacitor (C_{SFST}) to GND, controls the ramp-up of peak primary current through the sense resistor. It is also used to control converter inrush at start-up. The SFST clamps the V_{CMP} voltage and thus limits peak current until soft-start is complete. The ramp time is approximately 70ms per µF of capacitance. Leave SFST open if not using the soft-start function.

OSC (Pin 15): Oscillator. This pin, in conjunction with an external capacitor (C_{OSC}) to GND, defines the controller oscillator frequency. The frequency is approximately 100kHz • 100/C_{OSC} (pF).

FB (Pin 16): Feedback Amplifier Input. Feedback is usually sensed via a third winding and enabled during the flyback period. This pin also sinks additional current to compensate for load current variation as set by the R_{CMP} pin. Keep the Thevenin equivalent resistance of the feedback divider at roughly 3k.

V_{CMP} (Pin 17): Frequency Compensation Control. V_{CMP} is used for frequency compensation of the switcher control loop. It is the output of the feedback amplifier and the input to the current comparator. Switcher frequency compensation components are placed on this pin to GND. The voltage on this pin is proportional to the peak primary switch current. The feedback amplifier output is enabled during the synchronous switch on time.

UVLO (Pin 18): Undervoltage Lockout. A resistive divider from V_{PORTP} to this pin sets an undervoltage lockout based upon V_{PORTP} level (not V_{CC}). When the UVLO pin is below its threshold, the gate drives are disabled, but the part draws its normal quiescent current from V_{CC}.

The bias current on this pin has hysteresis such that the bias current is sourced when UVLO threshold is exceeded. This introduces a hysteresis at the pin equivalent to the bias current change times the impedance of the upper divider resistor. The user can control the amount of hysteresis by adjusting the impedance of the divider. Tie the UVLO pin to V_{CC} if not using this function. See the Applications

PIN FUNCTIONS

Information section for details. This pin is used for the UVLO function of the switching regulator. The PD interface section has an internal UVLO.

SENSE$^-$, SENSE$^+$ (Pins 19, 20): Current Sense Inputs. These pins are used to measure primary-side switch current through an external sense resistor. Peak primary-side current is used in the converter control loop. Make Kelvin connections to the sense resistor R_{SENSE} to reduce noise problems. SENSE$^-$ connects to the GND side. At maximum current (V_{CMP} at its maximum voltage) SENSE pins have 100mV threshold. The signal is blanked (ignored) during the minimum turn-on time.

C_{CMP} (Pin 21): Load Compensation Capacitive Control. Connect a capacitor from C_{CMP} to GND in order to reduce the effects of parasitic resistances in the feedback sensing path. A 0.1µF ceramic capacitor suffices for most applications. Short this pin to GND when load compensation is not needed.

R_{CMP} (Pin 22): Load Compensation Resistive Control. Connect a resistor from R_{CMP} to GND in order to compensate for parasitic resistances in the feedback sensing path. In less demanding applications, this resistor is not needed and this pin can be left open. See the Applications Information section for details.

PGDLY (Pin 23): Primary Gate Delay Control. Connect an external programming resistor (R_{PGDLY}) to set delay from synchronous gate turn-off to primary gate turn-on. See the Applications Information section for details.

PG (Pin 24): Primary Gate Drive. PG is the gate drive pin for the primary-side MOSFET switch. Large dynamic currents flow during voltage transitions. See the Applications Information section for details.

V_{NEG} (Pins 26, 27): System Negative Rail. Connects V_{NEG} to V_{PORTN} through an internal power MOSFET. Pin 26 and Pin 27 must be electrically tied together at the package.

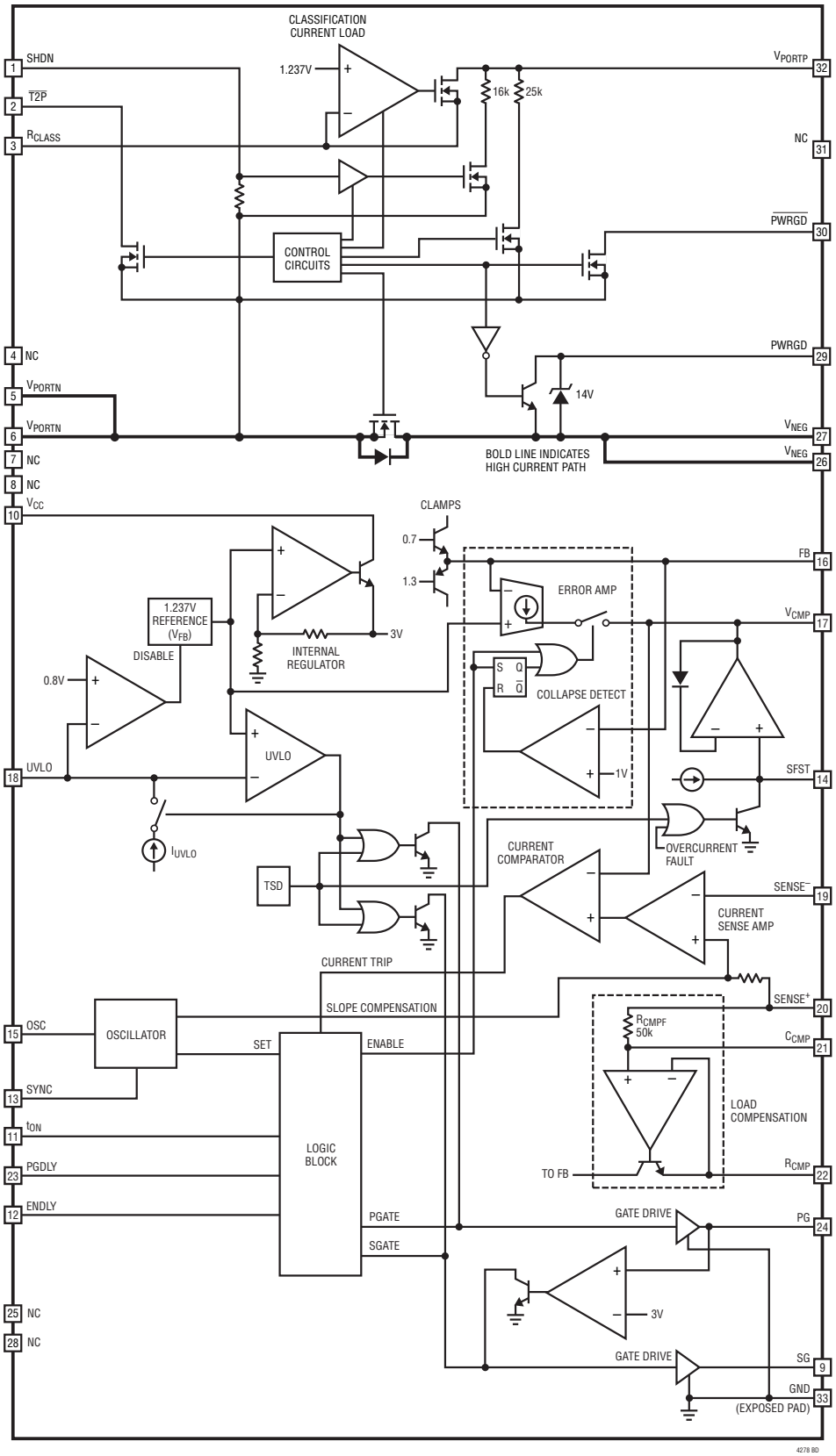
PWRGD (Pin 29): Power Good Output, Open-Collector. High impedance signals power-up completion. PWRGD is referenced to V_{NEG} and features a 14V clamp.

$\overline{\text{PWRGD}}$ (Pin 30): Complementary Power Good Output, Open-Drain. Low impedance signals power-up completion. $\overline{\text{PWRGD}}$ is referenced to V_{PORTN}.

V_{PORTP} (Pin 32): Positive Power Input. Tie to the input port power through the input diode bridge.

Exposed Pad (Pin 33): Ground. This is the negative rail connection for both signal ground and gate driver grounds of the flyback controller. This pin should be connected to V_{NEG}.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

OVERVIEW

Power over Ethernet (PoE) continues to gain popularity as more products are taking advantage of having DC power and high speed data available from a single RJ45 connector. As PoE continues to grow in the marketplace, powered device (PD) equipment vendors are running into the 12.95W power limit established by the IEEE 802.3af standard.

The IEE802.3at standard establishes a higher power allocation for Power over Ethernet while maintaining backwards compatibility with the existing IEEE 802.3af systems. Power sourcing equipment (PSE) and powered devices are distinguished as Type 1 complying with the IEEE 802.3af/IEEE 802.3at power levels, or Type 2 complying with the IEEE 802.3at power levels. The maximum available power of a Type 2 PD is 25.5W.

The IEEE 802.3at standard also establishes a new method of acquiring power classification from a PD and communicating the presence of a Type 2 PSE. A Type 2 PSE has the option of acquiring PD power classification by performing 2-event classification (layer 1) or by communicating with the PD over the data line (layer 2). In turn, a Type 2 PD must be able to recognize both layers of communications and identify a Type 2 PSE.

The LTC4278 is specifically designed to support the front end of a PD that must operate under the IEEE 802.3at standard. In particular, the LTC4278 provides the $\overline{T2P}$ indicator bit which recognizes 2-event classification. This indicator bit may be used to alert the LTC4278 output load that a Type 2 PSE is present. With an internal signature resistor, classification circuitry, inrush control, and thermal shutdown, the LTC4278 is a complete PD Interface solution capable of supporting in the next generation PD applications.

MODES OF OPERATION

The LTC4278 has several modes of operation depending on the input voltage applied between the V_{PORTP} and V_{PORTN} pins. Figure 1 presents an illustration of voltage and current waveforms the LTC4278 may encounter with the various modes of operation summarized in Table 1.

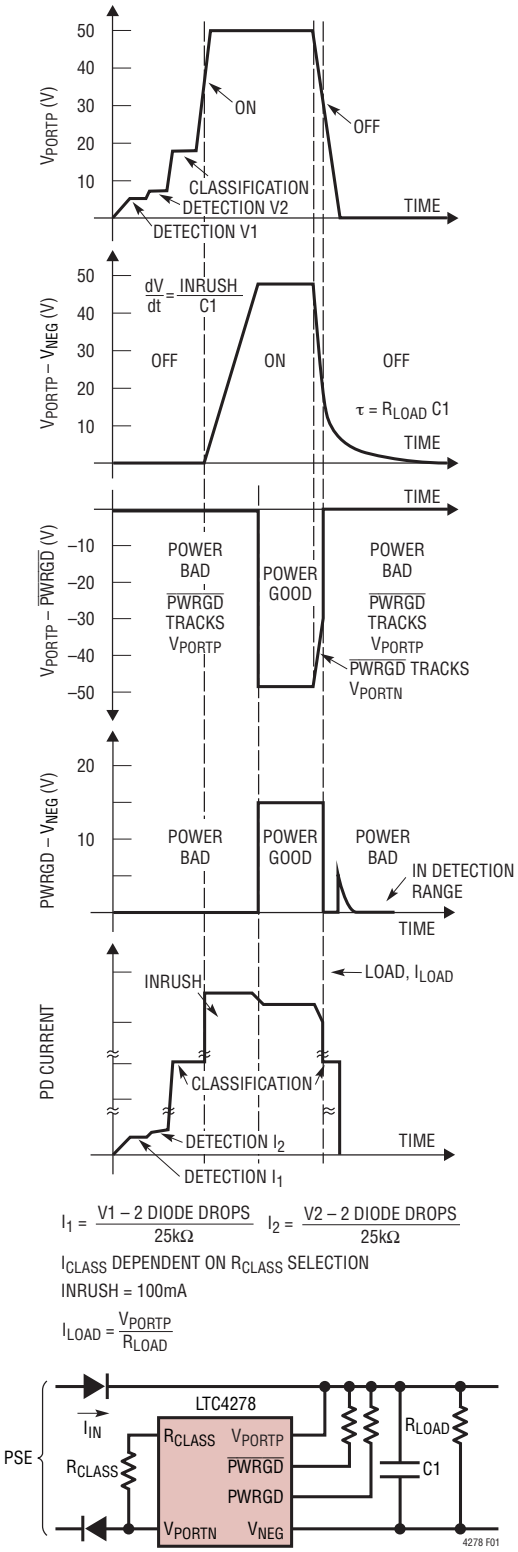


Figure 1. V_{NEG}, $\overline{PWRGD}$, PWRGD and PD Current as a Function of Input Voltage

APPLICATIONS INFORMATION

Table 1. LTC4278 Modes of Operation as a Function of Input Voltage

$V_{PORTP}–V_{PORTN}$ (V)	LTC4278 MODES OF OPERATION
0V to 1.4V	Inactive (Reset After 1st Classification Event)
1.5V to 9.8V (5.4V to 9.8V)	25k Signature Resistor Detection Before 1st Classification Event (Mark, 11k Signature Corrupt After 1st Classification Event)
12.5V to ON/OFF*	Classification Load Current Active
ON/OFF* to 60V	Inrush and Power Applied To PD Load
>71V	Overvoltage Lockout, Classification and Hot Swap Are Disabled

*ON/OFF includes hysteresis. Rising input threshold, 37.2V Max. Falling input threshold, 30V Min.

These modes satisfy the requirements defined in the IEEE 802.3af/IEEE 802.3at specification.

INPUT DIODE BRIDGE

In the IEEE 802.3af/IEEE 802.3at standard, the modes of operation reference the input voltage at the PD's RJ45 connector. Since the PD must handle power received in either polarity from either the data or the spare pair, input diode bridges BR1 and BR2 are connected between the RJ45 connector and the LTC4278 (Figure 2).

The input diode bridge introduces a voltage drop that affects the range for each mode of operation. The LTC4278 compensates for these voltage drops so that a PD built with the LTC4278 meets the IEEE 802.3af/IEEE 802.3at-established voltage ranges. Note the Electrical Characteristics are referenced with respect to the LTC4278 package pins.

DETECTION

During detection, the PSE looks for a 25k signature resistor which identifies the device as a PD. The PSE will apply two voltages in the range of 2.8V to 10V and measures the corresponding currents. Figure 1 shows the detection voltages V1 and V2 and the corresponding PD current. The PSE calculates the signature resistance using the $\Delta V/\Delta I$ measurement technique.

The LTC4278 presents its precision, temperature-compensated 25k resistor between the V_{PORTP} and V_{PORTN} pins, alerting the PSE that a PD is present and requests power to be applied. The LTC4278 signature resistor also compensates for the additional series resistance introduced by the input diode bridge. Thus a PD built with the LTC4278 conforms to the IEEE 802.3af/IEEE 802.3at specifications.

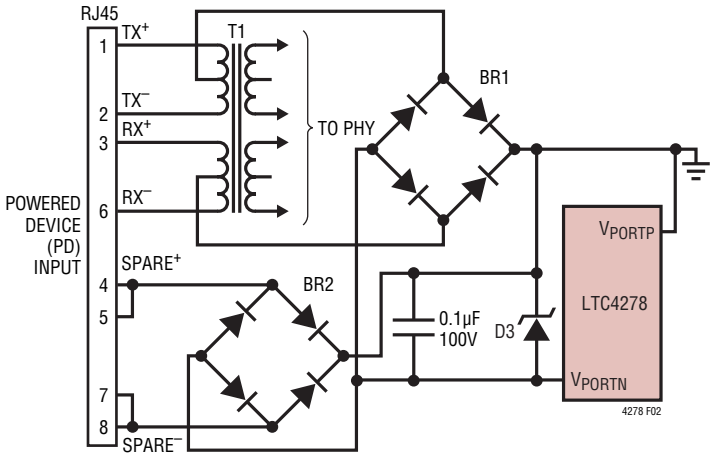


Figure 2. PD Front End Using Diode Bridges on Main and Spare Inputs

APPLICATIONS INFORMATION

SIGNATURE CORRUPT OPTION

In some designs that include an auxiliary power option, it is necessary to prevent a PD from being detected by a PSE. The LTC4278 signature resistance can be corrupted with the SHDN pin (Figure 3). Taking the SHDN pin high will reduce the signature resistor below 11k which is an invalid signature per the IEEE 802.3af/IEEE 802.3at specification, and alerts the PSE not to apply power. Invoking the SHDN pin also ceases operation for classification and disconnects the LTC4278 load from the PD input. If this feature is not used, connect SHDN to V_{PORTN}.

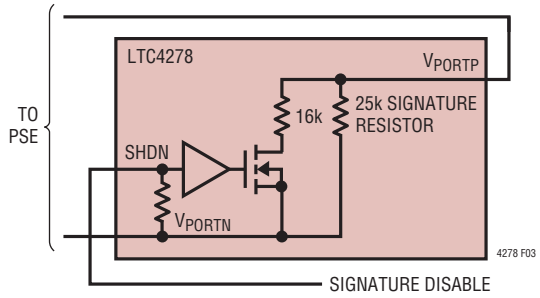


Figure 3. 25k Signature Resistor with Disable

CLASSIFICATION

Classification provides a method for more efficient power allocation by allowing the PSE to identify a PD power classification. Class 0 is included in the IEEE specification for PDs that do not support classification. Class 1-3 partitions PDs into three distinct power ranges. Class 4 includes the new power range under IEEE802.3at (see Table 2).

During classification probing, the PSE presents a fixed voltage between 15.5V and 20.5V to the PD (Figure 1). The LTC4278 asserts a load current representing the PD power classification. The classification load current is programmed with a resistor R_{CLASS} that is chosen from Table 2.

Table 2. Summary of Power Classifications and LTC4278 R_{CLASS} Resistor Selection

CLASS	USAGE	MAXIMUM POWER LEVELS AT INPUT OF PD (W)	NOMINAL CLASSIFICATION LOAD CURRENT (mA)	LTC4278 R_{CLASS} RESISTOR (Ω, 1%)
0	Type 1	0.44 to 12.95	< 0.4	Open
1	Type 1	0.44 to 3.84	10.5	124
2	Type 1	3.84 to 6.49	18.5	69.8
3	Type 1	6.49 to 12.95	28	45.3
4	Type 2	12.95 to 25.5	40	30.9

2-EVENT CLASSIFICATION AND THE $\overline{T2P}$ PIN

A Type 2 PSE may declare the availability of high power by performing a 2-event classification (layer 1) or by communicating over the high speed data line (layer 2). A Type 2 PD must recognize both layers of communication. Since layer 2 communication takes place directly between the PSE and the LTC4278 load, the LTC4278 concerns itself only with recognizing 2-event classification.

In 2-event classification, a Type 2 PSE probes for power classification twice. Figure 4 presents an example of a 2-event classification. The 1st classification event occurs when the PSE presents an input voltage between 15.5V to 20.5V and the LTC4278 presents a class 4 load current. The PSE then drops the input voltage into the mark voltage range of 7V to 10V, signaling the 1st mark event. The PD in the mark voltage range presents a load current between 0.25mA to 4mA.

The PSE repeats this sequence, signaling the 2nd Classification and 2nd mark event occurrence. This alerts the LTC4278 that a Type 2 PSE is present. The Type 2 PSE then applies power to the PD and the LTC4278 charges up the reservoir capacitor C1 with a controlled inrush current. When C1 is fully charged, and the LTC4278 declares power good, the $\overline{T2P}$ pin presents an active low signal, or low impedance output with respect to V_{PORTN}. The $\overline{T2P}$ output becomes inactive when the LTC4278 input voltage falls below undervoltage lockout threshold.

APPLICATIONS INFORMATION

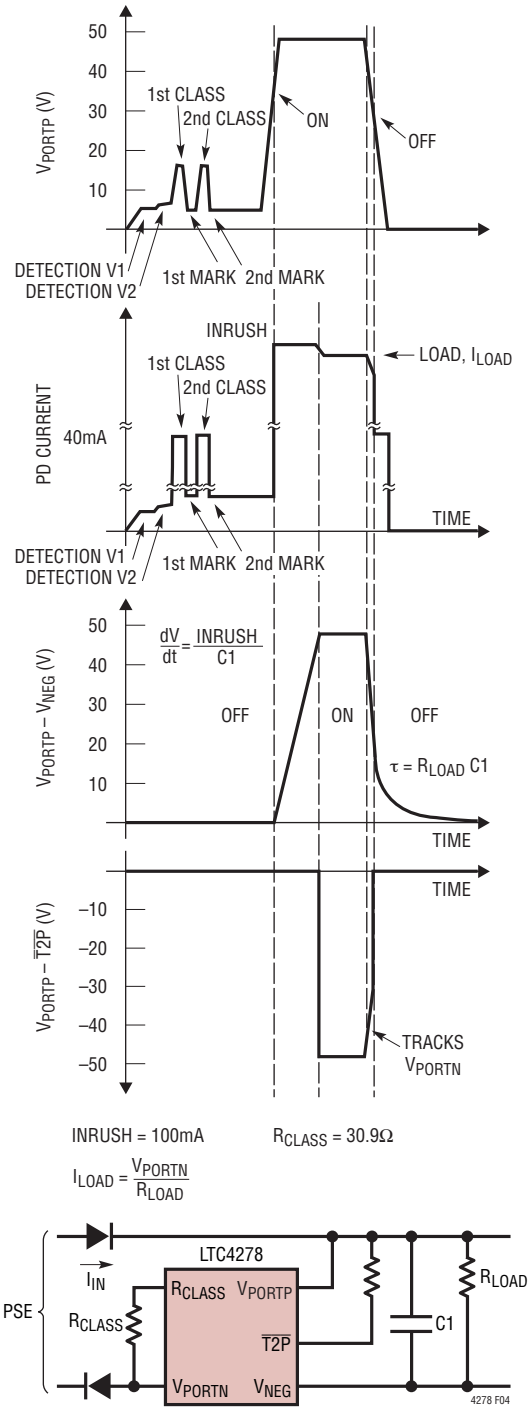


Figure 4. V_{NEG}, $\overline{T2P}$ and PD Current as a Result of 2-Event Classification

SIGNATURE CORRUPT DURING MARK

As a member of the IEEE 802.3at working group, Linear Technology noted that it is possible for a Type 2 PD to receive a false indication of a 2-event classification if a PSE port is pre-charged to a voltage above the detection voltage range before the first detection cycle. The IEEE working group modified the standard to prevent this possibility by requiring a Type 2 PD to corrupt the signature resistance during the mark event, alerting the PSE not to apply power. The LTC4278 conforms to this standard by corrupting the signature resistance. This also discharges the port before the PSE begins the next detection cycle.

PD STABILITY DURING CLASSIFICATION

Classification presents a challenging stability problem due to the wide range of possible classification load current. The onset of the classification load current introduces a voltage drop across the cable and increases the forward voltage of the input diode bridge. This may cause the PD to oscillate between detection and classification with the onset and removal of the classification load current.

The LTC4278 prevents this oscillation by introducing a voltage hysteresis window between the detection and classification ranges. The hysteresis window accommodates the voltage changes a PD encounters at the onset of the classification load current, thus providing a trouble-free transition between detection and classification modes.

The LTC4278 also maintains a positive I-V slope throughout the classification range up to the on-voltage. In the event a PSE overshoots beyond the classification voltage range, the available load current aids in returning the PD back into the classification voltage range. (The PD input may otherwise be "trapped" by a reverse-biased diode bridge and the voltage held by the 0.1µF capacitor).

INRUSH CURRENT

Once the PSE detects and optionally classifies the PD, the PSE then applies powers on the PD. When the LTC4278 input voltage rises above the on-voltage threshold, LTC4278 connects V_{NEG} to V_{PORTN} through the internal power MOSFET.

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To control the power-on surge currents in the system, the LTC4278 provides a fixed inrush current, allowing C1 to ramp up to the line voltage in a controlled manner.

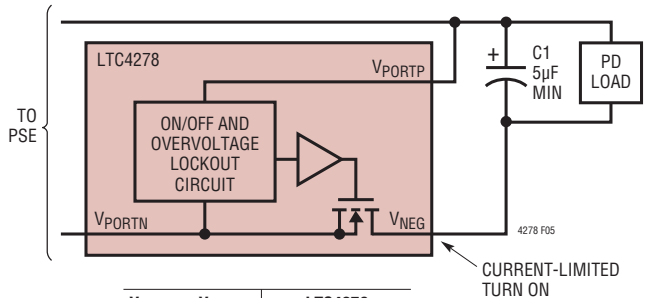
The LTC4278 keeps the PD inrush current below the PSE current limit to provide a well controlled power-up characteristic that is independent of the PSE behavior. This ensures a PD using the LTC4278 interoperability with any PSE.

TURN-ON/TURN-OFF THRESHOLD

The IEEE 802.3af/at specification for the PD dictates a maximum turn-on voltage of 42V and a minimum turn-off voltage of 30V. This specification provides an adequate voltage to begin PD operation, and to discontinue PD operation when the input voltage is too low. In addition, this specification allows PD designs to incorporate an ON/OFF hysteresis window to prevent start-up oscillations.

The LTC4278 features an ON/OFF hysteresis window (see Figure 5) that conforms with the IEEE 802.3af/at specification and accommodates the voltage drop in the cable and input diode bridge at the onset of the inrush current.

Once C1 is fully charged, the LTC4278 turns on is internal MOSFET and passes power to the PD load. The LTC4278 continues to power the PD load as long as the input voltage does not fall below the OFF threshold. When the LTC4278 input voltage falls below the OFF threshold, the PD load is disconnected, and classification mode resumes. C1 discharges through the LTC4278 circuitry.



$V_{PORTP} - V_{PORTN}$ VOLTAGE	LTC4278 POWER MOSFET
0V TO ON*	OFF
>ON*	ON
<OFF*	OFF
>OVLO	OFF

*INCLUDES ON/OFF HYSTERESIS
ON THRESHOLD ≅ 36.1V
OFF THRESHOLD ≅ 30.7V
OVLO THRESHOLD ≅ 71.0V

Figure 5. LTC4278 ON/OFF and Overvoltage Lockout

COMPLEMENTARY POWER GOOD

When LTC4278 fully charges the load capacitor (C1), power good is declared and the LTC4278 load can safely begin operation. The LTC4278 provides complementary power good signals that remain active during normal operation and are de-asserted when the input voltage falls below the OFF threshold, when the input voltage exceeds the overvoltage lockout (OVLO) threshold, or in the event of a thermal shutdown (see Figure 6).

The PWRGD pin features an open collector output referenced to V_{NEG} which can interface directly with the UVLO pin. When power good is declared and active, the PWRGD pin is high impedance with respect to V_{NEG}. An internal 14V clamp protects the UVLO pin from an excessive voltage.

The active low $\overline{PWRGD}$ pin connects to an internal, open-drain MOSFET referenced to V_{PORTN} and may be used as an indicator bit when power good is declared and active. The $\overline{PWRGD}$ pin is low impedance with respect to V_{PORTN}.

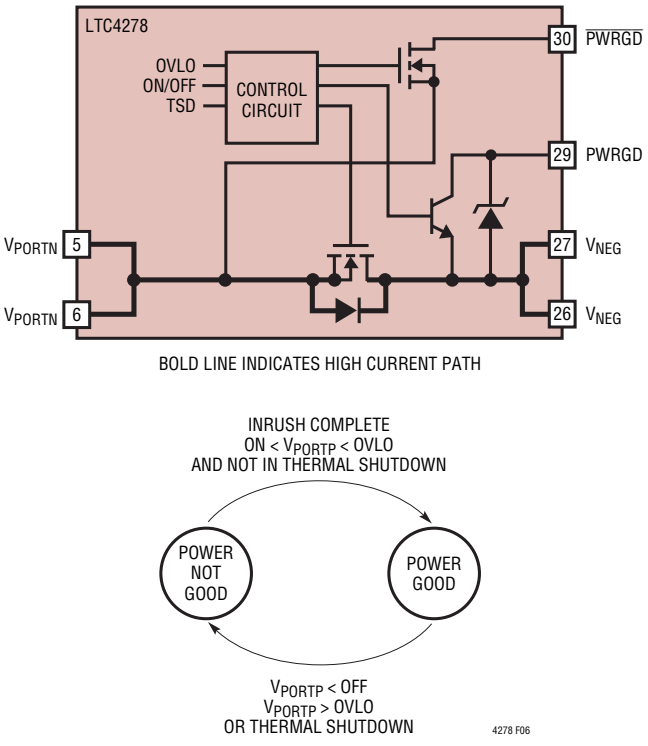


Figure 6. LTC4278 Power Good Functional and State Diagram

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PWRGD PIN WHEN SHDN IS INVOKED

In PD applications where an auxiliary power supply invokes the SHDN feature, the PWRGD pin becomes high impedance. This prevents the PWRGD pin that is connected to the UVLO pin from interfering with the DC/DC converter operations when powered by an auxiliary power supply.

OVERVOLTAGE LOCKOUT

The LTC4278 includes an overvoltage lockout (OVLO) feature (Figure 6) which protects the LTC4278 and its load from an overvoltage event. If the input voltage exceeds the OVLO threshold, the LTC4278 discontinues PD operation. Normal operations resume when the input voltage falls below the OVLO threshold and when C1 is charged up.

THERMAL PROTECTION

The IEEE 802.3af/at specification requires a PD to withstand any applied voltage from 0V to 57V indefinitely. However, there are several possible scenarios where a PD may encounter excessive heating.

During classification, excessive heating may occur if the PSE exceeds the 75ms probing time limit. At turn-on, when the load capacitor begins to charge, the instantaneous power dissipated by the PD interface can be large before it reaches the line voltage. And if the PD experiences a fast input positive voltage step in its operational mode (for example, from 37V to 57V), the instantaneous power dissipated by the PD Interface can be large.

The LTC4278 includes a thermal protection feature which protects the LTC4278 from excessive heating. If the LTC4278 junction temperature exceeds the over-temperature threshold, the LTC4278 discontinues PD operations and power good becomes inactive. Normal operation resumes when the junction temperature falls below the overtemperature threshold and when C1 is charged up.

EXTERNAL INTERFACE AND COMPONENT SELECTION

Transformer

Nodes on an Ethernet network commonly interface to the outside world via an isolation transformer. For PDs, the isolation transformer must also include a center tap on the RJ45 connector side (see Figure 7).

The increased current levels in a Type 2 PD over a Type 1 increase the current imbalance in the magnetics which can interfere with data transmission. In addition, proper termination is also required around the transformer to provide correct impedance matching and to avoid radiated and conducted emissions. Transformer vendors such as Bel Fuse, Coilcraft, Halo, Pulse, and Tyco (Table 4) can assist in selecting an appropriate isolation transformer and proper termination methods.

Table 4. Power over Ethernet Transformer Vendors

VENDOR	CONTACT INFORMATION
Bel Fuse Inc.	206 Van Vorst Street Jersey City, NJ 07302 Tel: 201-432-0463 www.belfuse.com
Coilcraft Inc.	1102 Silver Lake Road Gary, IL 60013 Tel: 847-639-6400 www.coilcraft.com
Halo Electronics	1861 Landings Drive Mountain View, CA 94043 Tel: 650-903-3800 www.haloelectronics.com
PCA Electronics	16799 Schoenborn Street North Hills, CA 91343 Tel: 818-892-0761 www.pca.com
Pulse Engineering	12220 World Trade Drive San Diego, CA 92128 Tel: 858-674-8100 www.pulseeng.com
Tyco Electronics	308 Constitution Drive Menlo Park, CA 94025-1164 Tel: 800-227-7040 www.circuitprotection.com

Input Diode Bridge

Figure 2 shows how two diode bridges are typically connected in a PD application. One bridge is dedicated to the data pair while the other bridge is dedicated to the spare pair. The LTC4278 supports the use of either silicon or Schottky input diode bridges. However, there are tradeoffs in the choice of diode bridges.

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An input diode bridge must be rated above the maximum current the PD application will encounter at the temperature the PD will operate. Diode bridge vendors typically call out the operating current at room temperature, but derate the maximum current with increasing temperature. Consult the diode bridge vendors for the operating current derating curve.

A silicon diode bridge can consume over 4% of the available power in some PD applications. Using Schottky diodes can help reduce the power loss with a lower forward voltage.

A Schottky bridge may not be suitable for some high temperature PD application. The leakage current has a voltage dependency that can reduce the perceived signature resistance. In addition, the IEEE 802.3af/at specification mandates the leakage back-feeding through the unused bridge cannot generate more than 2.8V across a 100k resistor when a PD is powered with 57V.

Sharing Input Diode Bridges

At higher temperatures, a PD design may be forced to consider larger bridges in a bigger package because the maximum operating current for the input diode bridge is drastically derated. The larger package may not be acceptable in some space-limited environments.

One solution to consider is to reconnect the diode bridges so that only one of the four diodes conducts current in each package. This configuration extends the maximum operating current while maintaining a smaller package profile. Figure 7 shows how to reconnect the two diode bridges. Consult the diode bridge vendors for the derating curve when only one of four diodes is in operation.

Input Capacitor

The IEEE 802.3af/at standard includes an impedance requirement in order to implement the AC disconnect function. A 0.1µF capacitor (C14 in Figure 7) is used to meet this AC impedance requirement.

Transient Voltage Suppressor

The LTC4278 specifies an absolute maximum voltage of 100V and is designed to tolerate brief overvoltage events. However, the pins that interface to the outside world can routinely see excessive peak voltages. To protect the LTC4278, install a transient voltage suppressor (D3) between the input diode bridge and the LTC4278 as shown in Figure 7.

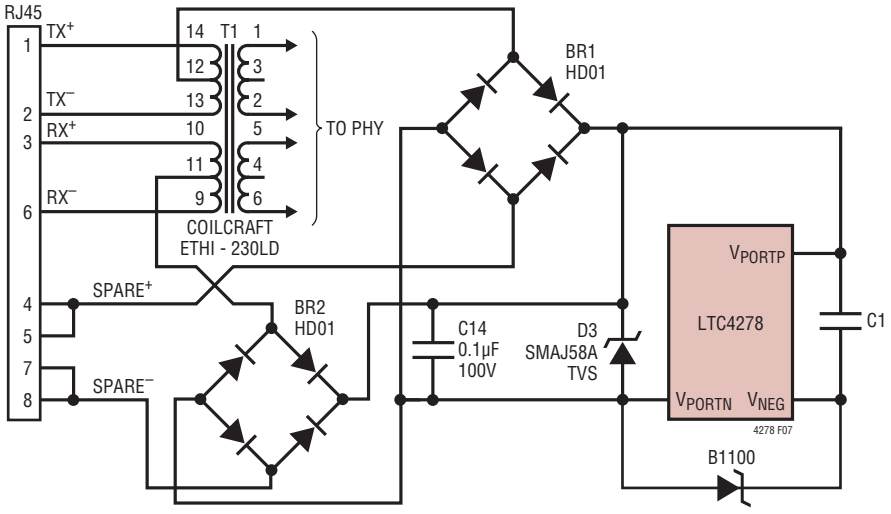

Figure 7. PD Front-End with Isolation Transformer, Diode Bridges, Capacitors, and a Transient Voltage Suppressor (TVS)

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Classification Resistor (R_{CLASS})

The R_{CLASS} resistor sets the classification load current, corresponding to the PD power classification. Select the value of R_{CLASS} from Table 2 and connect the resistor between the R_{CLASS} and V_{PORTN} pins as shown in Figure 4, or float the R_{CLASS} pin if the classification load current is not required. The resistor tolerance must be 1% or better to avoid degrading the overall accuracy of the classification circuit.

Load Capacitor

The IEEE 802.3af/at specification requires that the PD maintains a minimum load capacitance of 5µF and does not specify a maximum load capacitor. However, if the load capacitor is too large, there may be a problem with inadvertent power shutdown by the PSE.

This occurs when the PSE voltage drops quickly. The input diode bridge reverses bias, and the PD load momentarily powers off the load capacitor. If the PD does not draw power within the PSE's 300ms disconnection delay, the PSE may remove power from the PD. Thus, it is necessary to evaluate the load current and capacitance to ensure that an inadvertent shutdown cannot occur.

The load capacitor can store significant energy when fully charged. The PD design must ensure that this energy is not inadvertently dissipated in the LTC4278. For example, if the V_{PORTP} pin shorts to V_{PORTN} while the capacitor is charged, current will flow through the parasitic body diode of the internal MOSFET and may cause permanent damage to the LTC4278.

$\overline{T2P}$ Interface

When a 2-event classification sequence successfully completes, the LTC4278 recognizes this sequence, and provides an indicator bit, declaring the presence of a Type 2 PSE. The open-drain output provides the option to use this signal to communicate to the LTC4278 load, or to leave the pin unconnected.

Figure 8 shows two interface options using the $\overline{T2P}$ pin and the opto-isolator. The $\overline{T2P}$ pin is active low and connects to an opto-isolator to communicate across the DC/DC converter isolation barrier. The pull-up resistor R_P is sized according to the requirements of the opto-isolator operating current, the pull-down capability of the $\overline{T2P}$ pin, and the choice of V^+. V^+ for example can come from the PoE supply rail (which the LTC4278 V_{PORTP} is tied to), or from the voltage source that supplies power to the DC/DC converter. Option 1 has the advantage of not drawing power unless $\overline{T2P}$ is declared active.

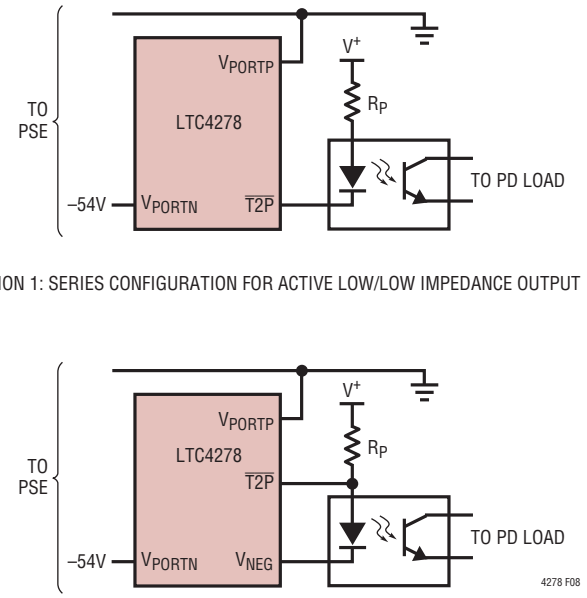

Figure 8. $\overline{T2P}$ Interface Examples

Shutdown Interface

To corrupt the signature resistance, the SHDN pin can be driven high with respect to V_{PORTN}. If unused, connect SHDN directly to V_{PORTN}.

Auxiliary Power Source

In some applications, it is desirable to power the PD from an auxiliary power source such as a wall adapter.

Auxiliary power can be injected into an LTC4278-based PD at the input of the LTC4278 V_{PORTN}, at V_{NEG}, or even the power supply output. In addition, some PD applications may desire auxiliary supply dominance or may be configured

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for PoE dominance. Furthermore, PD applications may also opt for a seamless transition — that is, without power disruption — between PoE and auxiliary power.

The most common auxiliary power option injects power at V_{NEG}. Figure 9 presents an example of this application. In this example, the auxiliary port injects 48V onto the line via diode D1. The components surrounding the SHDN pin are selected so that the LTC4278 does not disconnect power to the output until the auxiliary supply exceeds 36V.

This configuration is an auxiliary-dominant configuration. That is, the auxiliary power source supplies the power even if PoE power is already present. This configuration also provides a seamless transition from PoE to auxiliary power when auxiliary power is applied, however, the removal of auxiliary power to PoE power is not seamless.

Contact Linear Technology applications support for detail information on implementing a custom auxiliary power supply.

IEEE 802.3at SYSTEM POWER-UP REQUIREMENT

Under the IEEE 802.3at standard, a PD must operate under 12.95W in accordance with IEEE 802.3at standard until it recognizes a Type 2 PSE. Initializing PD operation in 12.95W mode eliminates interoperability issue in case a Type 2 PD connects to a Type 1 PSE. Once the PD recognizes a Type 2 PSE, the IEEE 802.3at standard requires the PD to wait 80ms in 12.95W operation before 25.5W operation can commence.

MAINTAIN POWER SIGNATURE

In an IEEE 802.3af/at system, the PSE uses the maintain power signature (MPS) to determine if a PD continues to require power. The MPS requires the PD to periodically draw at least 10mA and also have an AC impedance less than 26.25k in parallel with 0.05µF. If one of these conditions is not met, the PSE may disconnect power to the PD.

SWITCHING REGULATOR OVERVIEW

The LTC4278 includes a current mode converter designed specifically for use in an isolated flyback topology employing synchronous rectification. The LTC4278 operation is similar to traditional current mode switchers. The major difference is that output voltage feedback is derived via sensing the output voltage through the transformer. This precludes the need of an opto-isolator in isolated designs, thus greatly improving dynamic response and reliability. The LTC4278 has a unique feedback amplifier that samples a transformer winding voltage during the flyback period and uses that voltage to control output voltage. The internal blocks are similar to many current mode controllers. The differences lie in the feedback amplifier and load

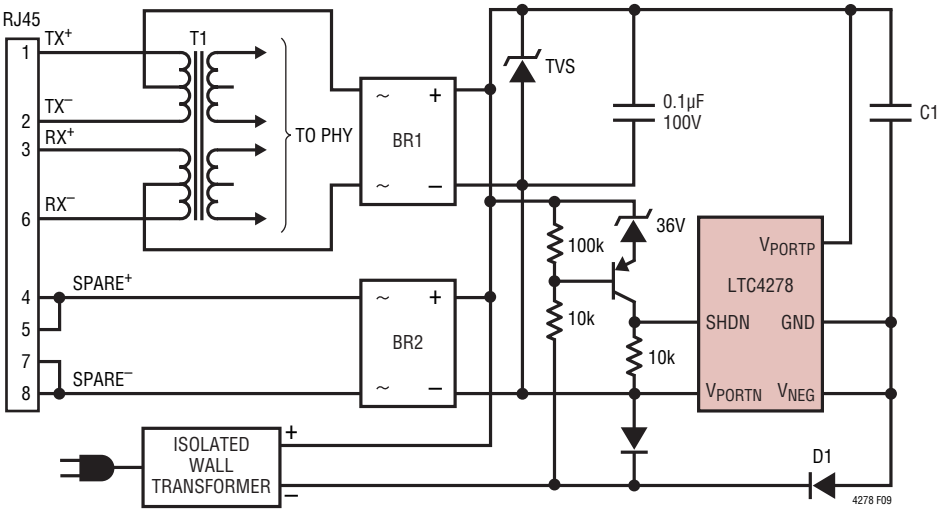

Figure 9. Auxiliary Power Dominant PD Interface Example

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compensation circuitry. The logic block also contains circuitry to control the special dynamic requirements of flyback control. For more information on the basics of current mode switcher/controllers and isolated flyback converters see Application Note 19.

Feedback Amplifier—Pseudo DC Theory

For the following discussion, refer to the simplified Switching Regulator Feedback Amplifier diagram (Figure 10A). When the primary-side MOSFET switch MP turns off, its drain voltage rises above the V_{PORTP} rail. Flyback occurs when the primary MOSFET is off and the synchronous secondary MOSFET is on. During flyback the voltage on nondriven transformer pins is determined by the secondary voltage. The amplitude of this flyback pulse, as seen on the third winding, is given as:

$$V_{FLBK} = \frac{V_{OUT} + I_{SEC} \bullet \left(ESR + R_{DS(ON)}\right)}{N_{SF}}$$

$R_{DS(ON)}$ = on-resistance of the synchronous MOSFET MS

I_{SEC} = transformer secondary current

ESR = impedance of secondary circuit capacitor, winding and traces

N_{SF} = transformer effective secondary-to-flyback winding turns ratio (i.e., N_S/N_{FLBK})

The flyback voltage is scaled by an external resistive divider R1/R2 and presented at the FB pin. The feedback amplifier compares the voltage to the internal bandgap reference. The feedback amp is actually a transconductance amplifier whose output is connected to V_{CMP} only during a period in the flyback time. An external capacitor on the V_{CMP} pin integrates the net feedback amp current to provide the control voltage to set the current mode trip point. The regulation voltage at the FB pin is nearly equal to the bandgap reference V_{FB} because of the high gain in the overall loop. The relationship between V_{FLBK} and V_{FB} is expressed as:

$$V_{FLBK} = \frac{R1+R2}{R2} \bullet V_{FB}$$

Combining this with the previous V_{FLBK} expression yields an expression for V_{OUT} in terms of the internal reference, programming resistors and secondary resistances:

$$V_{OUT} = \left(\frac{R1+R2}{R2} \bullet V_{FB} \bullet N_{SF}\right) - I_{SEC} \bullet \left(ESR + R_{DS(ON)}\right)$$

The effect of nonzero secondary output impedance is discussed in further detail (see Load Compensation Theory). The practical aspects of applying this equation for V_{OUT} are found in subsequent sections of the Applications Information.

Feedback Amplifier Dynamic Theory

So far, this has been a pseudo-DC treatment of flyback feedback amplifier operation. But the flyback signal is a pulse, not a DC level. Provision is made to turn on the flyback amplifier only when the flyback pulse is present, using the enable signal as shown in the timing diagram (Figure 10b).

Minimum Output Switch On Time ($t_{ON(MIN)}$)

The LTC4278 affects output voltage regulation via flyback pulse action. If the output switch is not turned on, there is no flyback pulse and output voltage information is not available. This causes irregular loop response and start-up/latchup problems. The solution is to require the primary switch to be on for an absolute minimum time per each oscillator cycle. To accomplish this the current limit feedback is blanked each cycle for $t_{ON(MIN)}$. If the output load is less than that developed under these conditions, forced continuous operation normally occurs. See subsequent discussions in the Applications Information section for further details.

Enable Delay Time (ENDLY)

The flyback pulse appears when the primary-side switch shuts off. However, it takes a finite time until the transformer primary-side voltage waveform represents the output voltage. This is partly due to rise time on the primary-side MOSFET drain node, but, more importantly, is due

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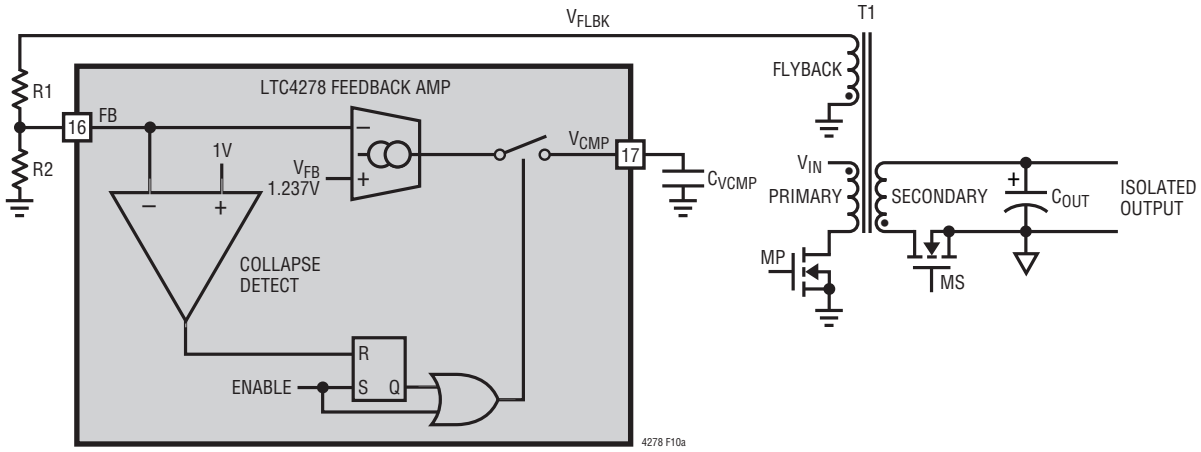

Figure 10a. LTC4278 Switching Regulator Feedback Amplifier

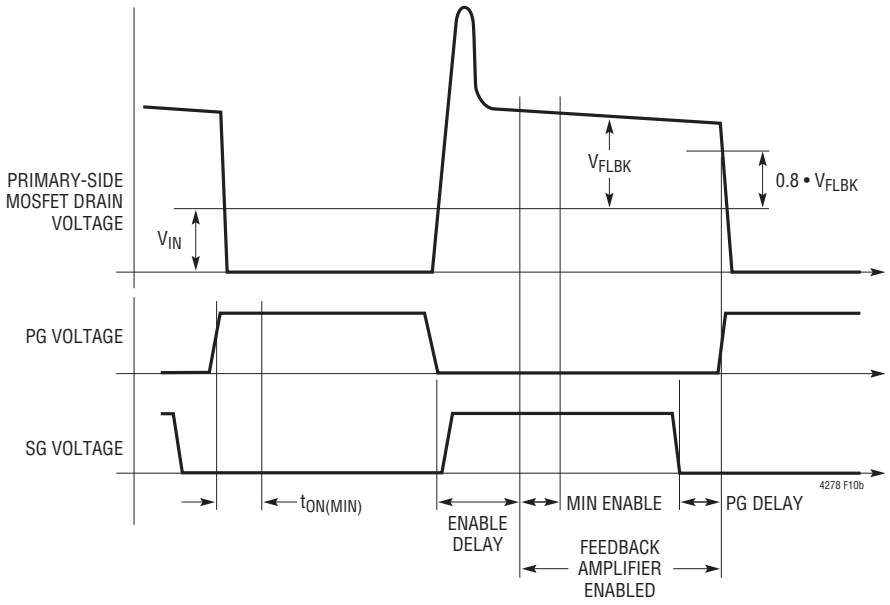

Figure 10b. LTC4278 Switching Regulator Timing Diagram

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to transformer leakage inductance. The latter causes a voltage spike on the primary side, not directly related to output voltage. Some time is also required for internal settling of the feedback amplifier circuitry. In order to maintain immunity to these phenomena, a fixed delay is introduced between the switch turn-off command and the enabling of the feedback amplifier. This is termed "enable delay." In certain cases where the leakage spike is not sufficiently settled by the end of the enable delay period, regulation error may result. See the subsequent sections for further details.

Collapse Detect

Once the feedback amplifier is enabled, some mechanism is then required to disable it. This is accomplished by a collapse detect comparator, which compares the flyback voltage (FB) to a fixed reference, nominally 80% of V_{FB}. When the flyback waveform drops below this level, the feedback amplifier is disabled.

Minimum Enable Time

The feedback amplifier, once enabled, stays on for a fixed minimum time period, termed "minimum enable time." This prevents lockup, especially when the output voltage is abnormally low, e.g., during start-up. The minimum enable time period ensures that the V_{CMP} node is able to "pump up" and increase the current mode trip point to the level where the collapse detect system exhibits proper operation. This time is set internally.

Effects of Variable Enable Period

The feedback amplifier is enabled during only a portion of the cycle time. This can vary from the fixed minimum enable time described to a maximum of roughly the off switch time minus the enable delay time. Certain parameters of feedback amp behavior are directly affected by the variable enable period. These include effective transconductance and V_{CMP} node slew rate.

Load Compensation Theory

The LTC4278 uses the flyback pulse to obtain information about the isolated output voltage. An error source is caused by transformer secondary current flow through the synchronous MOSFET $R_{DS(ON)}$ and real life nonzero impedances of the transformer secondary and output capacitor. This was represented previously by the expression, $I_{SEC} \bullet (ESR + R_{DS(ON)})$. However, it is generally more useful to convert this expression to effective output impedance. Because the secondary current only flows during the off portion of the duty cycle (DC), the effective output impedance equals the lumped secondary impedance divided by off time DC.

Since the off-time duty cycle is equal to 1 – DC, then:

$$R_{S(OUT)} = \frac{ESR + R_{DS(ON)}}{1 - DC}$$

where:

$R_{S(OUT)}$ = effective supply output impedance

DC = duty cycle

$R_{DS(ON)}$ and ESR are as defined previously

This impedance error may be judged acceptable in less critical applications, or if the output load current remains relatively constant. In these cases, the external FB resistive divider is adjusted to compensate for nominal expected error. In more demanding applications, output impedance error is minimized by the use of the load compensation function. Figure 11 shows the block diagram of the load compensation function. Switch current is converted to a voltage by the external sense resistor, averaged and lowpass filtered by the internal 50k resistor R_{CMPF} and the external capacitor on C_{CMP}. This voltage is impressed across the external R_{CMP} resistor by op amp A1 and transistor Q3 producing a current at the collector of Q3 that is subtracted from the FB node. This effectively increases the voltage required at the top of the R1/R2 feedback divider to achieve equilibrium.

The average primary-side switch current increases to maintain output voltage regulation as output loading increases. The increase in average current increases R_{CMP} resistor current which affects a corresponding increase in sensed output voltage, compensating for the IR drops.

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Assuming relatively fixed power supply efficiency, Eff, power balance gives:

$$P_{OUT} = Eff \bullet P_{IN}$$

$$V_{OUT} \bullet I_{OUT} = Eff \bullet V_{IN} \bullet I_{IN}$$

Average primary-side current is expressed in terms of output current as follows:

$$I_{IN} = K1 \bullet I_{OUT}$$

where:

$$K1 = \frac{V_{OUT}}{V_{IN} \bullet Eff}$$

So, the effective change in V_{OUT} target is:

$$\Delta V_{OUT} = K1 \bullet \frac{R_{SENSE}}{R_{CMP}} \bullet R1 \bullet N_{SF} \bullet \Delta I_{OUT}$$

thus:

$$\frac{\Delta V_{OUT}}{\Delta I_{OUT}} = K1 \bullet \frac{R_{SENSE}}{R_{CMP}} \bullet R1 \bullet N_{SF}$$

where:

K1 = dimensionless variable related to V_{IN}, V_{OUT} and efficiency, as previously explained

R_{SENSE} = external sense resistor

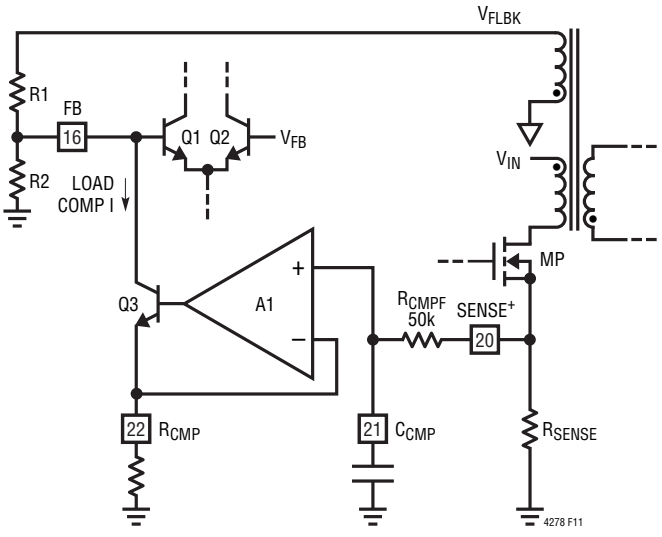

Figure 11. Load Compensation Diagram

Nominal output impedance cancellation is obtained by equating this expression with $R_{S(OUT)}$:

$$K1 \bullet \frac{R_{SENSE}}{R_{CMP}} \bullet R1 \bullet N_{SF} = \frac{ESR + R_{DS(ON)}}{1 - DC}$$

Solving for R_{CMP} gives:

$$R_{CMP} = K1 \bullet \frac{R_{SENSE} \bullet (1 - DC)}{ESR + R_{DS(ON)}} \bullet R1 \bullet N_{SF}$$

The practical aspects of applying this equation to determine an appropriate value for the R_{CMP} resistor are discussed subsequently in the Applications Information section.

Transformer Design

Transformer design/specification is the most critical part of a successful application of the LTC4278. The following sections provide basic information about designing the transformer and potential tradeoffs. If you need help, the LTC Applications group is available to assist in the choice and/or design of the transformer.

Turns Ratios

The design of the transformer starts with determining duty cycle (DC). DC impacts the current and voltage stress on the power switches, input and output capacitor RMS currents and transformer utilization (size vs power). The ideal turns ratio is:

$$N_{IDEAL} = \frac{V_{OUT}}{V_{IN}} \bullet \frac{1 - DC}{DC}$$

Avoid extreme duty cycles, as they generally increase current stresses. A reasonable target for duty cycle is 50% at nominal input voltage.

For instance, if we wanted a 48V to 5V converter at 50% DC then:

$$N_{IDEAL} = \frac{5}{48} \bullet \frac{1 - 0.5}{0.5} = \frac{1}{9.6}$$

In general, better performance is obtained with a lower turns ratio. A DC of 45.5% yields a 1:8 ratio.

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Note the use of the external feedback resistive divider ratio to set output voltage provides the user additional freedom in selecting a suitable transformer turns ratio. Turns ratios that are the simple ratios of small integers; e.g., 1:1, 2:1, 3:2 help facilitate transformer construction and improve performance.

When building a supply with multiple outputs derived through a multiple winding transformer, lower duty cycle can improve cross regulation by keeping the synchronous rectifier on longer, and thus, keep secondary windings coupled longer. For a multiple output transformer, the turns ratio between output windings is critical and affects the accuracy of the voltages. The ratio between two output voltages is set with the formula $V_{OUT2} = V_{OUT1} \bullet N21$ where N21 is the turns ratio between the two windings. Also keep the secondary MOSFET $R_{DS(ON)}$ small to improve cross regulation.

The feedback winding usually provides both the feedback voltage and power for the LTC4278. Set the turns ratio between the output and feedback winding to provide a rectified voltage that under worst-case conditions is greater than the the preregulator maximum supply voltage. For example if the preregulator maximum output were 7V:

$$N_{SF} > \frac{V_{OUT}}{7 + V_F}$$

where:

V_F = Diode Forward Voltage

For our example: $N_{SF} > \frac{5}{7 + 0.7} = \frac{1}{1.56}$

We will choose $\frac{1}{3}$

Leakage Inductance

Transformer leakage inductance (on either the primary or secondary) causes a spike after the primary-side switch turn-off. This is increasingly prominent at higher load currents, where more stored energy is dissipated. Higher flyback voltage may break down the MOSFET switch if it has too low a BV_{DSS} rating.

One solution to reducing this spike is to use a clamp circuit to suppress the voltage excursion. However, suppressing the voltage extends the flyback pulse width. If the flyback pulse extends beyond the enable delay time, output voltage regulation is affected. The feedback system has a deliberately limited input range, roughly ±50mV referred to the FB node. This rejects higher voltage leakage spikes because once a leakage spike is several volts in amplitude, a further increase in amplitude has little effect on the feedback system. Therefore, it is advisable to arrange the clamp circuit to clamp at as high a voltage as possible, observing MOSFET breakdown, such that leakage spike duration is as short as possible. Application Note 19 provides a good reference on clamp design.

As a rough guide, leakage inductance of several percent (of mutual inductance) or less may require a clamp, but exhibit little to no regulation error due to leakage spike behavior. Inductances from several percent up to, perhaps, ten percent, cause increasing regulation error.

Avoid double digit percentage leakage inductances. There is a potential for abrupt loss of control at high load current. This curious condition potentially occurs when the leakage spike becomes such a large portion of the flyback waveform that the processing circuitry is fooled into thinking that the leakage spike itself is the real flyback signal!

It then reverts to a potentially stable state whereby the top of the leakage spike is the control point, and the trailing edge of the leakage spike triggers the collapse detect circuitry. This typically reduces the output voltage abruptly to a fraction, roughly one-third to two-thirds of its correct value.

Once load current is reduced sufficiently, the system snaps back to normal operation. When using transformers with considerable leakage inductance, exercise this worst-case check for potential bistability:

1. Operate the prototype supply at maximum expected load current.
2. Temporarily short-circuit the output.
3. Observe that normal operation is restored.

If the output voltage is found to hang up at an abnormally low value, the system has a problem. This is usually evident by simultaneously viewing the primary-side MOSFET drain voltage to observe firsthand the leakage spike behavior.

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A final note—the susceptibility of the system to bistable behavior is somewhat a function of the load current/voltage characteristics. A load with resistive—i.e., I = V/R behavior—is the most apt to be bistable. Capacitive loads that exhibit $I = V^2/R$ behavior are less susceptible.

Secondary Leakage Inductance

Leakage inductance on the secondary forms an inductive divider on the transformer secondary, reducing the size of the flyback pulse. This increases the output voltage target by a similar percentage. Note that unlike leakage spike behavior, this phenomenon is independent of load. Since the secondary leakage inductance is a constant percentage of mutual inductance (within manufacturing variations), the solution is to adjust the feedback resistive divider ratio to compensate.

Winding Resistance Effects

Primary or secondary winding resistance acts to reduce overall efficiency (P_{OUT}/P_{IN}). Secondary winding resistance increases effective output impedance, degrading load regulation. Load compensation can mitigate this to some extent but a good design keeps parasitic resistances low.

Bifilar Winding

A bifilar, or similar winding, is a good way to minimize troublesome leakage inductances. Bifilar windings also improve coupling coefficients, and thus improve cross regulation in multiple winding transformers. However, tight coupling usually increases primary-to-secondary capacitance and limits the primary-to-secondary breakdown voltage, so is not always practical.

Primary Inductance

The transformer primary inductance, L_P, is selected based on the peak-to-peak ripple current ratio (X) in the transformer relative to its maximum value. As a general rule, keep X in the range of 20% to 40% (i.e., X = 0.2 to 0.4). Higher values of ripple will increase conduction losses, while lower values will require larger cores.

Ripple current and percentage ripple is largest at minimum duty cycle; in other words, at the highest input voltage. L_P is calculated from the following equation.

$$L_P = \frac{\left(V_{IN(MAX)} \bullet DC_{MIN}\right)^2}{f_{OSC} \bullet X_{MAX} \bullet P_{IN}} = \frac{\left(V_{IN(MAX)} \bullet DC_{MIN}\right)^2 \bullet Eff}{f_{OSC} \bullet X_{MAX} \bullet P_{OUT}}$$

where:

f_{OSC} is the oscillator frequency

DC_{MIN} is the DC at maximum input voltage

X_{MAX} is ripple current ratio at maximum input voltage

Using common high power PoE values, a 48V (41V < V_{IN} < 57V) to 5V/5.3A converter with 90% efficiency, P_{OUT}= 26.5W and P_{IN} = 29.5W. Using X = 0.4 N = 1/8 and f_{OSC} = 200kHz:

$$DC_{MIN} = \frac{1}{1 + \frac{N \bullet V_{IN(MAX)}}{V_{OUT}}} = \frac{1}{1 + \frac{1}{8} \bullet \frac{57}{5}} = 41.2\%$$

$$L_P = \frac{(57V \bullet 0.412)^2}{200kHz \bullet 0.4 \bullet 26.5W} = 260\mu H$$

Optimization might show that a more efficient solution is obtained at higher peak current but lower inductance and the associated winding series resistance. A simple spreadsheet program is useful for looking at tradeoffs.

Transformer Core Selection

Once L_P is known, the type of transformer is selected. High efficiency converters use ferrite cores to minimize core loss. Actual core loss is independent of core size for a fixed inductance, but decreases as inductance increases. Since increased inductance is accomplished through more turns of wire, copper losses increase. Thus, transformer design balances core and copper losses. Remember that increased winding resistance will degrade cross regulation and increase the amount of load compensation required.

The main design goals for core selection are reducing copper losses and preventing saturation. Ferrite core material saturates hard, rapidly reducing inductance

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when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and, consequently, output voltage ripple. Do not allow the core to saturate! The maximum peak primary current occurs at minimum V_{IN}:

$$I_{PK} = \frac{P_{IN}}{V_{IN(MIN)} \bullet DC_{MAX}} \bullet \left(1 + \frac{X_{MIN}}{2}\right)$$

now:

$$DC_{MAX} = \frac{1}{1 + \frac{N \bullet V_{IN(MIN)}}{V_{OUT}}} = \frac{1}{1 + \frac{1}{8} \bullet \frac{41}{5}} = 49.4\%$$

$$X_{MIN} = \frac{\left(V_{IN(MIN)} \bullet DC_{MAX}\right)^2}{f_{OSC} \bullet L_P \bullet P_{IN}} = \frac{\left(41 \bullet 49.4\%\right)^2}{200kHz \bullet 260\mu H \bullet 29.5W} = 0.267$$

Using the example numbers leads to:

$$I_{PK} = \frac{29.5W}{41 \bullet 0.494} \bullet \left(1 + \frac{0.267}{2}\right) = 1.65A$$

Multiple Outputs

One advantage that the flyback topology offers is that additional output voltages can be obtained simply by adding windings. Designing a transformer for such a situation is beyond the scope of this document. For multiple windings, realize that the flyback winding signal is a combination of activity on all the secondary windings. Thus load regulation is affected by each winding's load. Take care to minimize cross regulation effects.

Setting Feedback Resistive Divider

The expression for V_{OUT} developed in the Operation section is rearranged to yield the following expression for the feedback resistors:

$$R1 = R2\left(\frac{\left[V_{OUT} + I_{SEC} \bullet \left(ESR + R_{DS(ON)}\right)\right]}{V_{FB} \bullet N_{SF}} - 1\right)$$

Continuing the example, if ESR + $R_{DS(ON)}$ = 8mΩ, R2 = 3.32k, then:

$$R1 = 3.32k\left(\frac{5 + 5.3 \bullet 0.008}{1.237 \bullet 1/3} - 1\right) = 37.28k$$

choose 37.4k.

It is recommended that the Thevenin impedance of the resistive divider (R1||R2) is roughly 3k for bias current cancellation and other reasons.

Current Sense Resistor Considerations

The external current sense resistor is used to control peak primary switch current, which controls a number of key converter characteristics including maximum power and external component ratings. Use a noninductive current sense resistor (no wire-wound resistors). Mounting the resistor directly above an unbroken ground plane connected with wide and short traces keeps stray resistance and inductance low.

The dual sense pins allow for a full Kelvin connection. Make sure that $SENSE^+$ and $SENSE^-$ are isolated and connect close to the sense resistor.

Peak current occurs at 100mV of sense voltage V_{SENSE}. So the nominal sense resistor is V_{SENSE}/I_{PK}. For example, a peak switch current of 10A requires a nominal sense resistor of 0.010Ω Note that the instantaneous peak power in the sense resistor is 1W, and that it is rated accordingly. The use of parallel resistors can help achieve low resistance, low parasitic inductance and increased power capability.

Size R_{SENSE} using worst-case conditions, minimum L_P, V_{SENSE} and maximum V_{IN}. Continuing the example, let us assume that our worst-case conditions yield an I_{PK} of 40% above nominal, so I_{PK} = 2.3A. If there is a 10% tolerance on R_{SENSE} and minimum V_{SENSE} = 88mV, then R_{SENSE} • 110% = 88mV/2.3A and nominal R_{SENSE} = 35mΩ. Round to the nearest available lower value, 33mΩ.

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Selecting the Load Compensation Resistor

The expression for R_{CMP} was derived in the Operation section as:

$$R_{CMP} = K1 \bullet \frac{R_{SENSE} \bullet (1-DC)}{ESR + R_{DS(ON)}} \bullet R1 \bullet N_{SF}$$

Continuing the example:

$$K1 = \left(\frac{V_{OUT}}{V_{IN} \bullet Eff} \right) = \frac{5}{48 \bullet 90\%} = 0.116$$

$$DC = \frac{1}{1 + \frac{N \bullet V_{IN(NOM)}}{V_{OUT}}} = \frac{1}{1 + \frac{1}{8} \bullet \frac{48}{5}} = 45.5\%$$

$$\text{If } ESR + R_{DS(ON)} = 8m\Omega$$

$$R_{CMP} = 0.116 \bullet \frac{33m\Omega \bullet (1-0.455)}{8m\Omega} \bullet 37.4k\Omega \bullet \frac{1}{3}$$

$$= 3.25k$$

This value for R_{CMP} is a good starting point, but empirical methods are required for producing the best results. This is because several of the required input variables are difficult to estimate precisely. For instance, the ESR term above includes that of the transformer secondary, but its effective ESR value depends on high frequency behavior, not simply DC winding resistance. Similarly, K1 appears as a simple ratio of V_{IN} to V_{OUT} times efficiency, but theoretically estimating efficiency is not a simple calculation.

The suggested empirical method is as follows:

1. Build a prototype of the desired supply including the actual secondary components.
2. Temporarily ground the C_{CMP} pin to disable the load compensation function. Measure output voltage while sweeping output current over the expected range. Approximate the voltage variation as a straight line.

   $\Delta V_{OUT}/\Delta I_{OUT} = R_{S(OUT)}$.
3. Calculate a value for the K1 constant based on V_{IN}, V_{OUT} and the measured efficiency.
4. Compute:

$$R_{CMP} = K1 \bullet \frac{R_{SENSE}}{R_{S(OUT)}} \bullet R1 \bullet N_{SF}$$

5. Verify this result by connecting a resistor of this value from the R_{CMP} pin to ground.
6. Disconnect the ground short to C_{CMP} and connect a 0.1µF filter capacitor to ground. Measure the output impedance $R_{S(OUT)} = \Delta V_{OUT}/\Delta I_{OUT}$ with the new compensation in place. $R_{S(OUT)}$ should have decreased significantly. Fine tuning is accomplished experimentally by slightly altering R_{CMP}. A revised estimate for R_{CMP} is:

$$R'_{CMP} = R_{CMP} \bullet \left(1 + \frac{R_{S(OUT)CMP}}{R_{S(OUT)}} \right)$$

where R'_{CMP} is the new value for the load compensation resistor. $R_{S(OUT)CMP}$ is the output impedance with R_{CMP} in place and $R_{S(OUT)}$ is the output impedance with no load compensation (from step 2).

Setting Frequency

The switching frequency of the LTC4278 is set by an external capacitor connected between the OSC pin and ground. Recommended values are between 200pF and 33pF, yielding switching frequencies between 50kHz and 250kHz. Figure 12 shows the nominal relationship between external capacitance and switching frequency. Place the capacitor as close as possible to the IC and minimize OSC

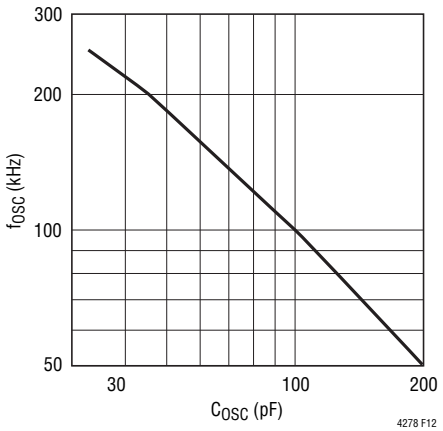

Figure 12. f_{OSC} vs OSC Capacitor Values

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trace length and area to minimize stray capacitance and potential noise pick-up.

You can synchronize the oscillator frequency to an external frequency. This is done with a signal on the SYNC pin. Set the LTC4278 frequency 10% slower than the desired external frequency using the OSC pin capacitor, then use a pulse on the SYNC pin of amplitude greater than 2V and with the desired frequency. The rising edge of the SYNC signal initiates an OSC capacitor discharge forcing primary MOSFET off (PG voltage goes low). If the oscillator frequency is much different from the sync frequency, problems may occur with slope compensation and system stability. Also, keep the sync pulse width greater than 500ns.

Selecting Timing Resistors

There are three internal "one-shot" times that are programmed by external application resistors: minimum on-time, enable delay time and primary MOSFET turn-on delay. These are all part of the isolated flyback control technique, and their functions are previously outlined in the Theory of Operation section. The following information should help in selecting and/or optimizing these timing values.

Minimum Output Switch On-Time ($t_{ON(MIN)}$)

Minimum on-time is the programmable period during which current limit is blanked (ignored) after the turn-on of the primary-side switch. This improves regulator performance by eliminating false tripping on the leading edge spike in the switch, especially at light loads. This spike is due to both the gate/source charging current and the discharge of drain capacitance. The isolated flyback sensing requires a pulse to sense the output. Minimum on-time ensures that the output switch is always on a minimum time and that there is always a signal to close the loop.

The LTC4278 does not employ cycle skipping at light loads. Therefore, minimum on-time along with synchronous rectification sets the switch over to forced continuous mode operation.

The $t_{ON(MIN)}$ resistor is set with the following equation

$$R_{tON(MIN)}\,(k\Omega) = \frac{t_{ON(MIN)}\,(ns) - 104}{1.063}$$

Keep $R_{tON(MIN)}$ greater than 70k. A good starting value is 160k.

Enable Delay Time (ENDLY)

Enable delay time provides a programmable delay between turn-off of the primary gate drive node and the subsequent enabling of the feedback amplifier. As discussed earlier, this delay allows the feedback amplifier to ignore the leakage inductance voltage spike on the primary side. The worst-case leakage spike pulse width is at maximum load conditions. So, set the enable delay time at these conditions.

While the typical applications for this part use forced continuous operation, it is conceivable that a secondary-side controller might cause discontinuous operation at light loads. Under such conditions, the amount of energy stored in the transformer is small. The flyback waveform becomes "lazy" and some time elapses before it indicates the actual secondary output voltage. The enable delay time should be made long enough to ignore the "irrelevant" portion of the flyback waveform at light loads.

Even though the LTC4278 has a robust gate drive, the gate transition time slows with very large MOSFETs. Increase delay time as required when using such MOSFETs.

The enable delay resistor is set with the following equation:

$$R_{ENDLY}\,(k\Omega) = \frac{t_{ENDLY}\,(ns) - 30}{2.616}$$

Keep R_{ENDLY} greater than 40k. A good starting point is 56k.

Primary Gate Delay Time (PGDLY)

Primary gate delay is the programmable time from the turn-off of the synchronous MOSFET to the turn-on of the primary-side MOSFET. Correct setting eliminates overlap

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between the primary-side switch and secondary-side synchronous switch(es) and the subsequent current spike in the transformer. This spike will cause additional component stress and a loss in regulator efficiency.

The primary gate delay resistor is set with the following equation:

$$R_{PGDLY}\,(k\Omega) = \frac{t_{PGDLY}\,(ns) + 47}{9.01}$$

A good starting point is 15k.

Soft-Start Function

The LTC4278 contains an optional soft-start function that is enabled by connecting an external capacitor between the SFST pin and ground. Internal circuitry prevents the control voltage at the V_{CMP} pin from exceeding that on the SFST pin. There is an initial pull-up circuit to quickly bring the SFST voltage to approximately 0.8V. From there it charges to approximately 2.8V with a 20µA current source.

The SFST node is discharged to 0.8V when a fault occurs. A fault occurs when the current sense voltage is greater than 200mV or the IC's thermal (overtemperature) shutdown is tripped. When SFST discharges, the V_{CMP} node voltage is also pulled low to below the minimum current voltage. Once discharged and the fault removed, the SFST charges up again. In this manner, switch currents are reduced and the stresses in the converter are reduced during fault conditions.

The time it takes to fully charge soft-start is:

$$t_{ss} = \frac{C_{SFST} \bullet 1.4V}{20\mu A} = 70k\Omega \bullet C_{SFST}\,(\mu F)$$

Switcher's UVLO Pin Function

The UVLO pin provides a user programming undervoltage lockout. This is typically used to provide undervoltage lockout based on V_{IN}. The gate drivers are disabled when UVLO is below the 1.24V UVLO threshold. An external resistive divider between the input supply and ground is used to set the turn-on voltage.

The bias current on this pin depends on the pin voltage and UVLO state. The change provides the user with adjustable UVLO hysteresis. When the pin rises above the UVLO threshold a small current is sourced out of the pin, increasing the voltage on the pin. As the pin voltage drops below this threshold, the current is stopped, further dropping the voltage on UVLO. In this manner, hysteresis is produced.

Referring to Figure 13, the voltage hysteresis at V_{IN} is equal to the change in bias current times R_A. The design procedure is to select the desired V_{IN} referred voltage hysteresis, V_{UVHYS}. Then:

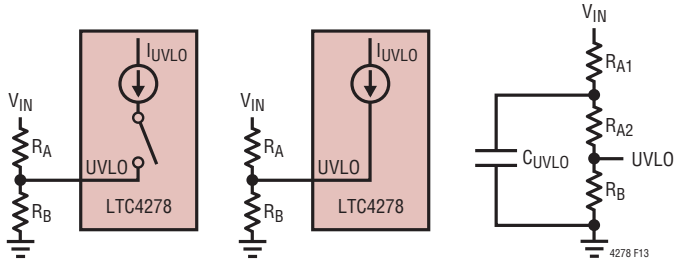
$$R_A = \frac{V_{UVHYS}}{I_{UVLO}}$$

where:

$I_{UVLO} = I_{UVLOL} - I_{UVLOH}$ is approximately 3.4µA

R_B is then selected with the desired turn-on voltage:

$$R_B = \frac{R_A}{\left(\frac{V_{IN(ON)}}{V_{UVLO}} - 1\right)}$$



(13a) UV Turning On (13b) UV Turning Off (13c) UV Filtering

Figure 13. UVLO Pin Function and Recommended Filtering

APPLICATIONS INFORMATION

If we wanted a V_{IN}-referred trip point of 36V, with 1.8V (5%) of hysteresis (on at 36V, off at 34.2V):

$$R_A = \frac{1.8V}{3.4\mu A} = 529k,\ \text{use } 523k$$

$$R_B = \frac{523k}{\left(\frac{36V}{1.23V} - 1\right)} = 18.5k,\ \text{use } 18.7k$$

Even with good board layout, board noise may cause problems with UVLO. You can filter the divider but keep large capacitance off the UVLO node because it will slow the hysteresis produced from the change in bias current. Figure 13c shows an alternate method of filtering by splitting the R_A resistor with the capacitor. The split should put more of the resistance on the UVLO side.

Converter Start-Up

The standard topology for the LTC4278 uses a third transformer winding on the primary side that provides both the feedback information and local V_{CC} power for the LTC4278 (Figure 14). This power bootstrapping improves converter efficiency but is not inherently self-starting. Start-Up is affected with an external *preregulator* circuit that conditions the input line voltage for the LTC4278 during start-up.

Upon application of power, C_{VCC} is charged via the preregulator, thereby providing an appropriate supply voltage at the V_{CC} pin for the LTC4278. This supply voltage is typically in the range 7V and is used during start-up. After converter startup, the third transformer winding becomes energized and is designed to generate a higher voltage than the preregulator. The higher voltage of the third winding turns off QPR and provides an efficient method to power the LTC4278.

Design of the V_{CC} power circuitry involves selecting appropriate voltage ranges for both the preregulator and the third transformer winding. The preregulator voltage is set as low as possible while ensuring it's worst-case minimum voltage is high enough to drive the switching FETs gates during the startup period. The third winding output voltage is selected to ensure that it's worst-case minimum voltage exceeds the preregulator voltage in order to turn off Q_{PR}. If the two voltage ranges overlap, the only disadvantage is that a small degradation in efficiency may occur. It is also necessary to verify that the worst-case maximum winding voltage is not high enough to damage the B-E junction of Q_{PR}.

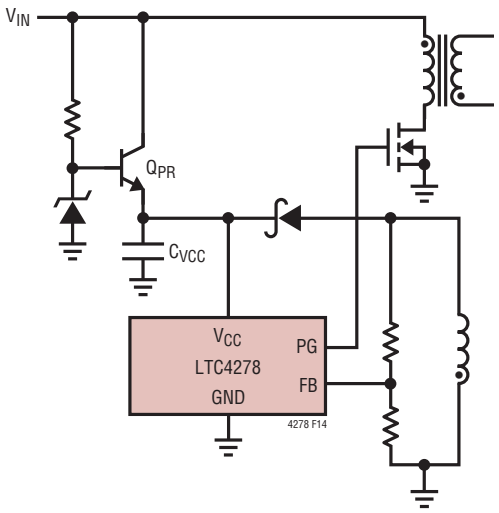


Figure 14. Typical Power Bootstrapping

Control Loop Compensation

Loop frequency compensation is performed by connecting a capacitor network from the output of the feedback amplifier (V_{CMP} pin) to ground as shown in Figure 15. Because of the sampling behavior of the feedback amplifier, compensation is different from traditional current mode controllers. Normally only C_{VCMP} is required. R_{VCMP} can be used to add a zero, but the phase margin improvement traditionally offered by this extra resistor is usually already accomplished by the nonzero secondary circuit impedance. C_{VCMP2} can be used to add an additional high frequency pole and is usually sized at 0.1 times C_{VCMP}.

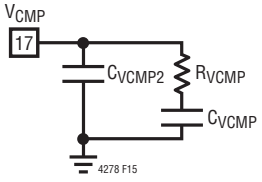


Figure 15. V_{CMP} Compensation Network

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In further contrast to traditional current mode switchers, V_{CMP} pin ripple is generally not an issue with the LTC4269-1. The dynamic nature of the clamped feedback amplifier forms an effective track/hold type response, whereby the V_{CMP} voltage changes during the flyback pulse, but is then held during the subsequent switch-on portion of the next cycle. This action naturally holds the V_{CMP} voltage stable during the current comparator sense action (current mode switching).

Application Note 19 provides a method for empirically tweaking frequency compensation. Basically, it involves introducing a load current step and monitoring the response.

Slope Compensation

The LTC4278 incorporates current slope compensation. Slope compensation is required to ensure current loop stability when the DC is greater than 50%. In some switching regulators, slope compensation reduces the maximum peak current at higher duty cycles. The LTC4278 eliminates this problem by having circuitry that compensates for the slope compensation so that maximum current sense voltage is constant across all duty cycles.

Minimum Load Considerations

At light loads, the LTC4278 derived regulator goes into forced continuous conduction mode. The primary-side switch always turns on for a short time as set by the $t_{ON(MIN)}$ resistor. If this produces more power than the load requires, power will flow back into the primary during the off period when the synchronization switch is on. This does not produce any inherently adverse problems, although light load efficiency is reduced.

Maximum Load Considerations

The current mode control uses the V_{CMP} node voltage and amplified sense resistor voltage as inputs to the current comparator. When the amplified sense voltage exceeds the V_{CMP} node voltage, the primary-side switch is turned off.

In normal use, the peak switch current increases while FB is below the internal reference. This continues until V_{CMP} reaches its 2.56V clamp. At clamp, the primary-side MOSFET will turn off at the rated 100mV V_{SENSE} level. This repeats on the next cycle.

It is possible for the peak primary switch currents as referred across R_{SENSE} to exceed the max 100mV rating because of the minimum switch on time blanking. If the voltage on V_{SENSE} exceeds 205mV after the minimum turn-on time, the SFST capacitor is discharged, causing the discharge of the V_{CMP} capacitor. This then reduces the peak current on the next cycle and will reduce overall stress in the primary switch.

Short-Circuit Conditions

Loss of current limit is possible under certain conditions such as an output short-circuit. If the duty cycle exhibited by the minimum on-time is greater than the ratio of secondary winding voltage (referred-to-primary) divided by input voltage, then peak current is not controlled at the nominal value. It ratchets up cycle-by-cycle to some higher level. Expressed mathematically, the requirement to maintain short-circuit control is:

$$DC_{MIN} = t_{ON(MIN)} \bullet f_{OSC} < \frac{I_{SC} \bullet \left(R_{SEC} + R_{DS(ON)}\right)}{V_{IN} \bullet N_{SP}}$$

where:

$t_{ON(MIN)}$ is the primary-side switch minimum on-time

I_{SC} is the short-circuit output current

N_{SP} is the secondary-to-primary turns ratio (N_{SEC}/N_{PRI}) (other variables as previously defined)

Trouble is typically encountered only in applications with a relatively high product of input voltage times secondary to primary turns ratio and/or a relatively long minimum switch on time. Additionally, several real world effects such as transformer leakage inductance, AC winding losses and output switch voltage drop combine to make this simple theoretical calculation a conservative estimate. Prudent

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design evaluates the switcher for short-circuit protection and adds any additional circuitry to prevent destruction.

Output Voltage Error Sources

The LTC4278's feedback sensing introduces additional minor sources of errors. The following is a summary list:

- The internal bandgap voltage reference sets the reference voltage for the feedback amplifier. The specifications detail its variation.
- The external feedback resistive divider ratio directly affects regulated voltage. Use 1% components.
- Leakage inductance on the transformer secondary reduces the effective secondary-to-feedback winding turns ratio (NS/NF) from its ideal value. This increases the output voltage target by a similar percentage. Since secondary leakage inductance is constant from part to part (within a tolerance) adjust the feedback resistor ratio to compensate.
- The transformer secondary current flows through the impedances of the winding resistance, synchronous MOSFET $R_{DS(ON)}$ and output capacitor ESR. The DC equivalent current for these errors is higher than the load current because conduction occurs only during the converter's off-time. So, divide the load current by (1 – DC).

If the output load current is relatively constant, the feedback resistive divider is used to compensate for these losses. Otherwise, use the LTC4278 load compensation circuitry (see Load Compensation). If multiple output windings are used, the flyback winding will have a signal that represents an amalgamation of all these windings impedances. Take care that you examine worst-case loading conditions when tweaking the voltages.

Power MOSFET Selection

The power MOSFETs are selected primarily on the criteria of on-resistance $R_{DS(ON)}$, input capacitance, drain-to-source breakdown voltage (BV_{DSS}), maximum gate voltage (V_{GS}) and maximum drain current ($ID_{(MAX)}$).

For the primary-side power MOSFET, the peak current is:

$$I_{PK(PRI)} = \frac{P_{IN}}{V_{IN(MIN)} \bullet DC_{MAX}} \bullet \left(1 + \frac{X_{MIN}}{2}\right)$$

where X_{MIN} is peak-to-peak current ratio as defined earlier.

For each secondary-side power MOSFET, the peak current is:

$$I_{PK(SEC)} = \frac{I_{OUT}}{1 - DC_{MAX}} \bullet \left(1 + \frac{X_{MIN}}{2}\right)$$

Select a primary-side power MOSFET with a BVDSS greater than:

$$BV_{DSS} \geq I_{PK} \sqrt{\frac{L_{LKG}}{C_P}} + V_{IN(MAX)} + \frac{V_{OUT(MAX)}}{N_{SP}}$$

where NSP reflects the turns ratio of that secondary-to primary winding. LLKG is the primary-side leakage inductance and CP is the primary-side capacitance (mostly from the drain capacitance (COSS) of the primary-side power MOSFET). A clamp may be added to reduce the leakage inductance as discussed.

For each secondary-side power MOSFET, the BV_{DSS} should be greater than:

$$BV_{DSS} \geq V_{OUT} + V_{IN(MAX)} \bullet N_{SP}$$

Choose the primary-side MOSFET $R_{DS(ON)}$ at the nominal gate drive voltage (7.5V). The secondary-side MOSFET gate drive voltage depends on the gate drive method.

Primary-side power MOSFET RMS current is given by:

$$I_{RMS(PRI)} = \frac{P_{IN}}{V_{IN(MIN)} \sqrt{DC_{MAX}}}$$

For each secondary-side power MOSFET RMS current is given by:

$$I_{RMS(SEC)} = \frac{I_{OUT}}{\sqrt{1 - DC_{MAX}}}$$

Calculate MOSFET power dissipation next. Because the primary-side power MOSFET operates at high V_{DS}, a transition power loss term is included for accuracy. C_{MILLER} is the most critical parameter in determining the transition loss, but is not directly specified on the data sheets.

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C_{MILLER} is calculated from the gate charge curve included on most MOSFET data sheets (Figure 16).

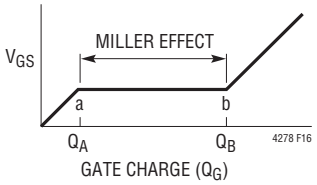

Figure 16. Gate Charge Curve

The flat portion of the curve is the result of the Miller (gate to-drain) capacitance as the drain voltage drops. The Miller capacitance is computed as:

$$C_{MILLER} = \frac{Q_B - Q_A}{V_{DS}}$$

The curve is done for a given V_{DS}. The Miller capacitance for different V_{DS} voltages are estimated by multiplying the computed C_{MILLER} by the ratio of the application V_{DS} to the curve specified V_{DS}.

With C_{MILLER} determined, calculate the primary-side power MOSFET power dissipation:

$$P_{D(PRI)} = I_{RMS(PRI)}^2 \bullet R_{DS(ON)}(1+\delta) + V_{IN(MAX)} \bullet \frac{P_{IN(MAX)}}{DC_{MIN}} \bullet R_{DR} \bullet \frac{C_{MILLER}}{V_{GATE(MAX)} - V_{TH}} \bullet f_{OSC}$$

where:

R_{DR} is the gate driver resistance (≈10Ω)

V_{TH} is the MOSFET gate threshold voltage

f_{OSC} is the operating frequency

$V_{GATE(MAX)}$ = 7.5V for this part

(1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve. If you don't have a curve, use δ = 0.005/°C • ΔT for low voltage MOSFETs.

The secondary-side power MOSFETs typically operate at substantially lower V_{DS}, so you can neglect transition losses. The dissipation is calculated using:

$$P_{DIS(SEC)} = I_{RMS(SEC)}^2 \bullet R_{DS(ON)}(1 + \delta)$$

With power dissipation known, the MOSFETs' junction temperatures are obtained from the equation:

$$T_J = T_A + P_{DIS} \bullet \theta_{JA}$$

where T_A is the ambient temperature and θ_{JA} is the MOSFET junction to ambient thermal resistance.

Once you have T_J iterate your calculations recomputing δ and power dissipations until convergence.

Gate Drive Node Consideration

The PG and SG gate drivers are strong drives to minimize gate drive rise and fall times. This improves efficiency, but the high frequency components of these signals can cause problems. Keep the traces short and wide to reduce parasitic inductance.

The parasitic inductance creates an LC tank with the MOSFET gate capacitance. In less than ideal layouts, a series resistance of 5Ω or more may help to dampen the ringing at the expense of slightly slower rise and fall times and poorer efficiency.

The LTC4278 gate drives will clamp the max gate voltage to roughly 7.5V, so you can safely use MOSFETs with maximum V_{GS} of 10V and larger.

Synchronous Gate Drive

There are several different ways to drive the synchronous gate MOSFET. Full converter isolation requires the synchronous gate drive to be isolated. This is usually accomplished by way of a pulse transformer. Usually the pulse driver is used to drive a buffer on the secondary, as shown in the application on the front page of this data sheet.

However, other schemes are possible. There are gate drivers and secondary-side synchronous controllers available that provide the buffer function as well as additional features.

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Capacitor Selection

In a flyback converter, the input and output current flows in pulses, placing severe demands on the input and output filter capacitors. The input and output filter capacitors are selected based on RMS current ratings and ripple voltage.

Select an input capacitor with a ripple current rating greater than:

$$I_{RMS(PRI)} = \frac{P_{IN}}{V_{IN(MIN)}} \sqrt{\frac{1-DC_{MAX}}{DC_{MAX}}}$$

Continuing the example:

$$I_{RMS(PRI)} = \frac{29.5W}{41V} \sqrt{\frac{1-49.4\%}{49.4\%}} = 0.728A$$

Keep input capacitor series resistance (ESR) and inductance (ESL) small, as they affect electromagnetic interference suppression. In some instances, high ESR can also produce stability problems because flyback converters exhibit a negative input resistance characteristic. Refer to Application Note 19 for more information.

The output capacitor is sized to handle the ripple current and to ensure acceptable output voltage ripple. The output capacitor should have an RMS current rating greater than:

$$I_{RMS(SEC)} = I_{OUT} \sqrt{\frac{DC_{MAX}}{1-DC_{MAX}}}$$

Continuing the example:

$$I_{RMS(SEC)} = 5.3A \sqrt{\frac{49.4\%}{1-49.4\%}} = 5.24A$$

This is calculated for each output in a multiple winding application.

ESR and ESL along with bulk capacitance directly affect the output voltage ripple. The waveforms for a typical flyback converter are illustrated in Figure 17.

The maximum acceptable ripple voltage (expressed as a percentage of the output voltage) is used to establish a starting point for the capacitor values. For the purpose of simplicity, we will choose 2% for the maximum output ripple, divided equally between the ESR step and the charging/discharging ΔV. This percentage ripple changes, depending on the requirements of the application. You can modify the following equations.

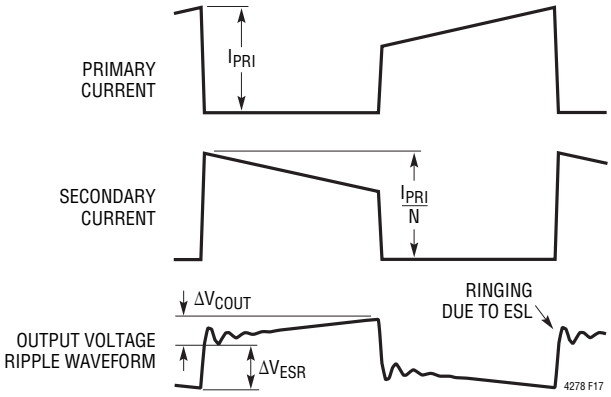

Figure 17. Typical Flyback Converter Waveforms

For a 1% contribution to the total ripple voltage, the ESR of the output capacitor is determined by:

$$ESR_{COUT} \le 1\% \bullet \frac{V_{OUT} \bullet (1-DC_{MAX})}{I_{OUT}}$$

The other 1% is due to the bulk C component, so use:

$$C_{OUT} \ge \frac{I_{OUT}}{1\% \bullet V_{OUT} \bullet f_{OSC}}$$

In many applications, the output capacitor is created from multiple capacitors to achieve desired voltage ripple, reliability and cost goals. For example, a low ESR ceramic capacitor can minimize the ESR step, while an electrolytic capacitor satisfies the required bulk C.

Continuing our example, the output capacitor needs:

$$ESR_{COUT} \le 1\% \bullet \frac{5V \bullet (1-49.4\%)}{5.3A} = 4m\Omega$$

$$C_{OUT} \ge \frac{5.3A}{1\% \bullet 5 \bullet 200kHz} = 600\mu F$$

These electrical characteristics require paralleling several low ESR capacitors possibly of mixed type.

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One way to reduce cost and improve output ripple is to use a simple LC filter. Figure 18 shows an example of the filter.

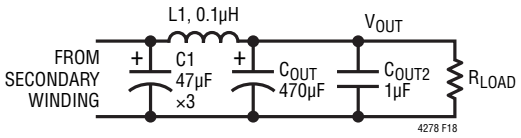

Figure 18.

The design of the filter is beyond the scope of this data sheet. However, as a starting point, use these general guidelines. Start with a C_{OUT} 1/4 the size of the nonfilter solution. Make C1 1/4 of C_{OUT} to make the second filter pole independent of C_{OUT}. C1 may be best implemented with multiple ceramic capacitors. Make L1 smaller than the output inductance of the transformer. In general, a 0.1µH filter inductor is sufficient. Add a small ceramic capacitor (C_{OUT2}) for high frequency noise on V_{OUT}. For those interested in more details refer to "Second-Stage LC Filter Design," Ridley, Switching Power Magazine, July 2000 p8-10.

Circuit simulation is a way to optimize output capacitance and filters, just make sure to include the component parasitic. LTC SwitcherCAD® is a terrific free circuit simulation tool that is available at www.linear.com. Final optimization of output ripple must be done on a dedicated PC board. Parasitic inductance due to poor layout can significantly impact ripple. Refer to the PC Board Layout section for more details.

ELECTRO STATIC DISCHARGE AND SURGE PROTECTION

The LTC4278 is specified to operate with an absolute maximum voltage of –100V and is designed to tolerate brief overvoltage events. However, the pins that interface to the outside world (primarily V_{PORTN} and V_{PORTP}) can routinely see peak voltages in excess of 10kV. To protect the LTC4278, it is highly recommended that the SMAJ58A unidirectional 58V transient voltage suppressor be installed between the diode bridge and the LTC4278 (D3 in Figure 2).

ISOLATION

The 802.3 standard requires Ethernet ports to be electrically isolated from all other conductors that are user accessible. This includes the metal chassis, other connectors and any auxiliary power connection. For PDs, there are two common methods to meet the isolation requirement. If there will be any user accessible connection to the PD, then an isolated DC/DC converter is necessary to meet the isolation requirements. If user connections can be avoided, then it is possible to meet the safety requirement by completely enclosing the PD in an insulated housing. In all PD applications, there should be no user accessible electrical connections to the LTC4278 or support circuitry other than the RJ-45 port.

LAYOUT CONSIDERATIONS FOR THE LTC4278

The LTC4278's PD front end is relatively immune to layout problems. Excessive parasitic capacitance on the R_{CLASS} pin should be avoided. Include a PCB heat sink to which the exposed pad on the bottom of the package can be soldered. This heat sink should be electrically connected to GND. For optimum thermal performance, make the heat sink as large as possible. Voltages in a PD can be as large as 57V for PoE applications, so high voltage layout techniques should be employed. The SHDN pin should be separated from other high voltage pins, like V_{PORTP}, V_{NEG}, to avoid the possibility of leakage currents shutting down the LTC4278. If not used, tie SHDN to V_{PORTN}. The load capacitor connected between V_{PORTP} and V_{NEG} of the LTC4278 can store significant energy when fully charged. The design of a PD must ensure that this energy is not inadvertently dissipated in the LTC4278. The polarity-protection diodes prevent an accidental short on the cable from causing damage. However if, V_{PORTN} is shorted to V_{PORTP} inside the PD while capacitor C1 is charged,

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current will flow through the parasitic body diode of the internal MOSFET and may cause permanent damage to the LTC4278.

In order to minimize switching noise and improve output load regulation, connect the GND pin of the LTC4278 directly to the ground terminal of the V_{CC} decoupling capacitor, the bottom terminal of the current sense resistor and the ground terminal of the input capacitor, using a ground plane with multiple vias. Place the V_{CC} capacitor immediately adjacent to the V_{CC} and GND pins on the IC package. This capacitor carries high di/dt MOSFET gate drive currents. Use a low ESR ceramic capacitor.

Take care in PCB layout to keep the traces that conduct high switching currents short, wide and with minimal overall loop area. These are typically the traces associated with the switches. This reduces the parasitic inductance and also minimizes magnetic field radiation. Figure 19 outlines the critical paths.

Keep electric field radiation low by minimizing the length and area of traces (keep stray capacitances low). The drain of the primary-side MOSFET is the worst offender in this category. Always use a ground plane under the switcher circuitry to prevent coupling between PCB planes.

Check that the maximum BV_{DSS} ratings of the MOSFETs are not exceeded due to inductive ringing. This is done by viewing the MOSFET node voltages with an oscilloscope. If it is breaking down, either choose a higher voltage device, add a snubber or specify an avalanche-rated MOSFET.

Place the small-signal components away from high frequency switching nodes. This allows the use of a pseudo-Kelvin connection for the signal ground, where high di/dt gate driver currents flow out of the IC ground pin in one direction (to the bottom plate of the V_{CC} decoupling capacitor) and small-signal currents flow in the other direction.

Keep the trace from the feedback divider tap to the FB pin short to preclude inadvertent pick-up.

For applications with multiple switching power converters connected to the same input supply, make sure that the input filter capacitor for the LTC4278 is not shared with other converters. AC input current from another converter could cause substantial input voltage ripple which could interfere with the LTC4278 operation. A few inches of PC trace or wire ($L \cong 100nH$) between the C_{IN} of the LTC4278 and the actual source V_{IN}, is sufficient to prevent current sharing problems.

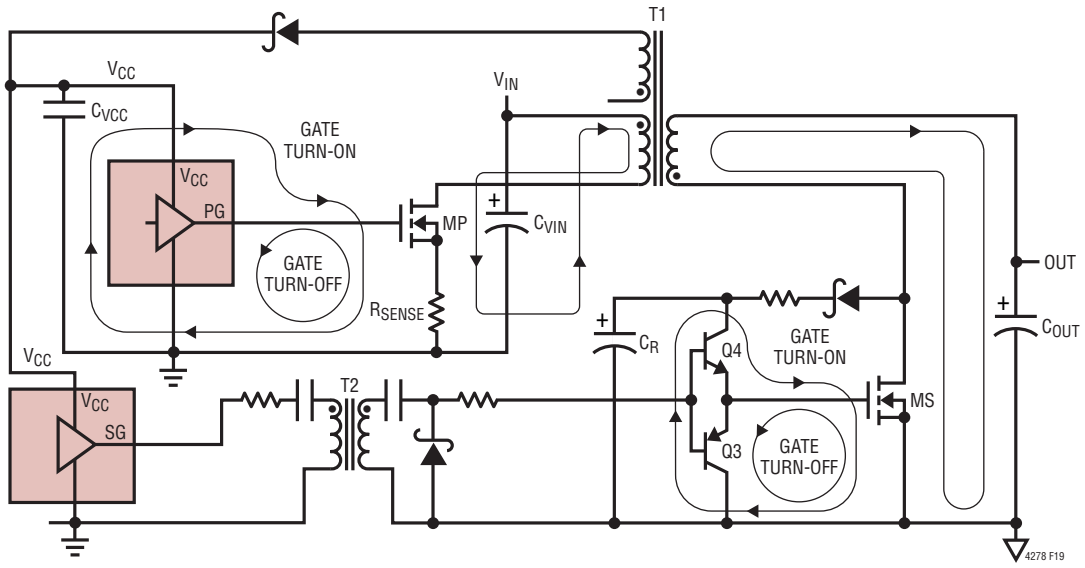
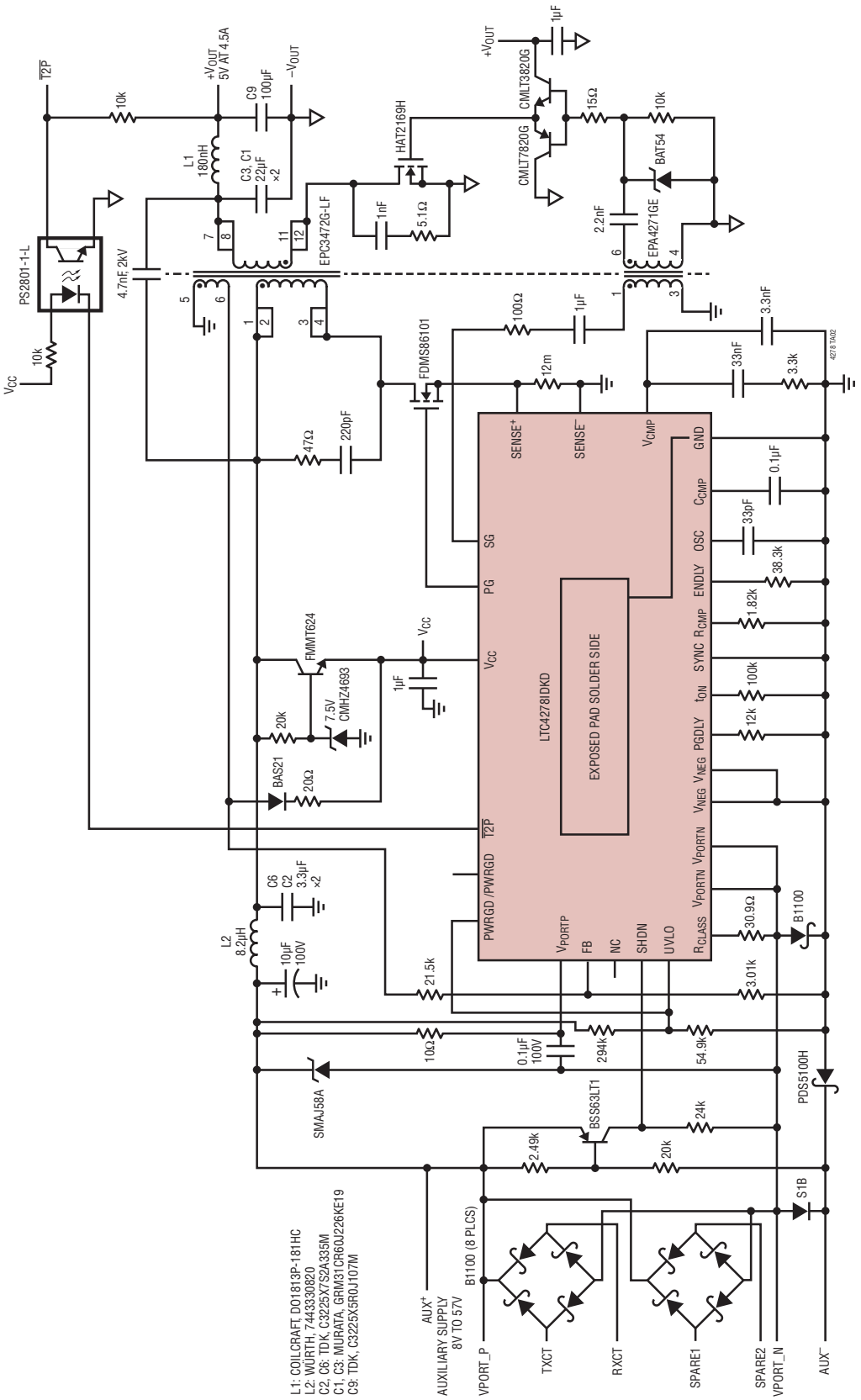


Figure 19. Layout Critical High Current Paths

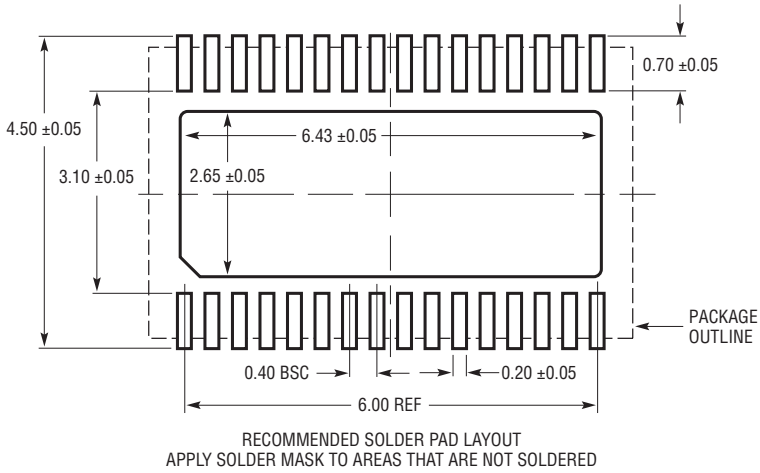
TYPICAL APPLICATION

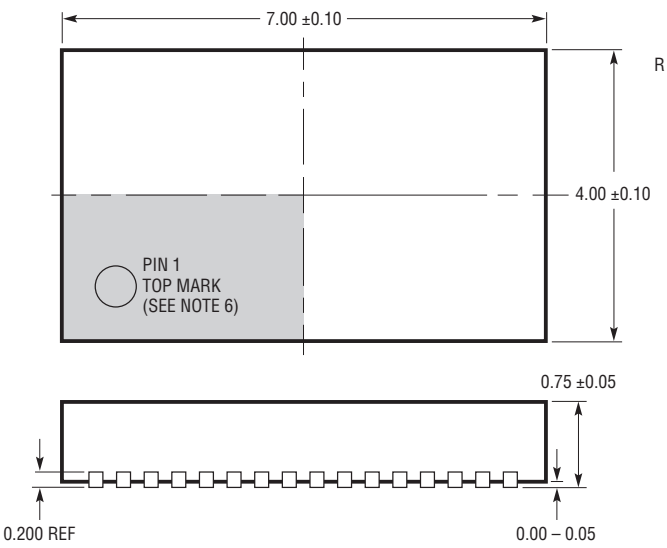


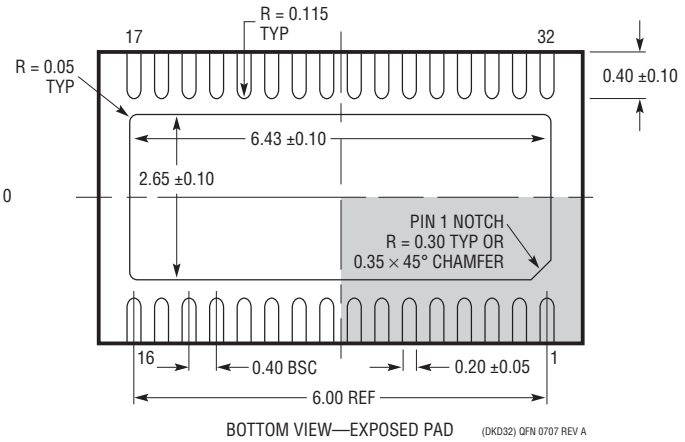
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DKD Package
32-Lead Plastic DFN (7mm × 4mm)
(Reference LTC DWG # 05-08-1734 Rev A)







NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WXXX) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.20mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	3/12	Added B1100 to schematic	1, 19
		Revised Max Junction Temperature	2
		Added Typical Application	39
C	4/12	Updated component values on Typical Application	1
		Updated Maximum Junction Temperature to 125°C	2
		Updated Typical Application	39

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