Programmable Hex Voltage Supervisor with EEPROM and Comparator Outputs

FEATURES

- **Supervises 6 Power Supplies**
- **I²C Adjustable UV and OV Trip Points**
- **Guaranteed Threshold Accuracy: ±1% (Maximum)**
- **I²C/SMBus Interface**
- **Internal EEPROM**
- **Six Comparator Outputs**
- Fast Comparator Response Time: 7.5µs
- 256 Programmable Thresholds per Channel
- Three Range Settings per Channel
- Two General Purpose Inputs
- Three General Purpose Inputs/Outputs
- Programmable Output Delays
- Can Be Powered from 3.3V, or 3.4V to 13.9V
- 24-Pin 4mm × 5mm QFN and SSOP Packages

APPLICATIONS

- High Availability Computer Systems
- Network Servers
- Telecom Equipment
- Data Storage Systems

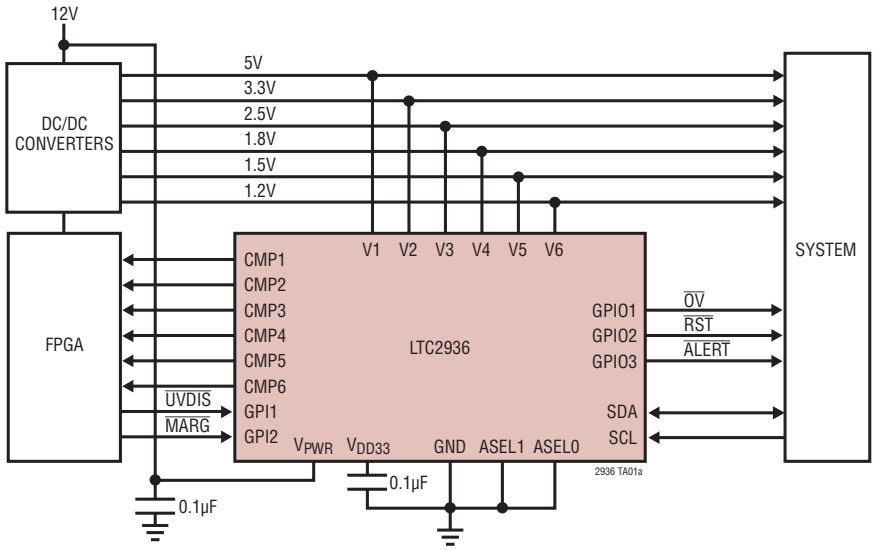
DESCRIPTION

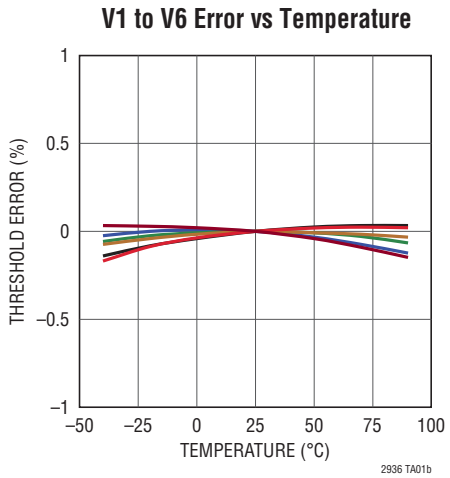
The LTC®2936 is an EEPROM configurable voltage supervisor which can simultaneously monitor up to six power supply voltage inputs. Each voltage detector offers I²C programmable overvoltage/undervoltage thresholds in various ranges and increments and a dedicated comparator output.

Two general purpose inputs (GPI) can be configured as programmable manual reset ($\overline{MR}$), UV disable ($\overline{UVDIS}$), margin ($\overline{MARG}$), Write Protect ($\overline{WP}$) or auxiliary comparator (AUXC) inputs. Three general purpose pins (GPIO) can be configured for input or output operation. When configured as an input, a GPIO pin can be mapped to any other GPIO configured as output. The GPIO pins can also be configured as $\overline{ALERT}$ or fault outputs. Faults can be configured with programmable delay-on-release times. Output type and polarity are also configurable.

Status and history registers log faults and can be polled via the I²C interface. A fault snapshot is also backed up in internal EEPROM. All parameters are programmable via the I²C interface. Configuration EEPROM supports autonomous operation without additional software.

TYPICAL APPLICATION





ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltages
- V_{PWR} ..... –0.3V to 14V
- V_{DD33} ..... –0.3V to 3.6V

Digital Input/Output Voltages
- SDA, SCL, GPI1, GPI2 ..... –0.3V to 6V
- GPIO1-GPIO3, CMP1-CMP6 ..... –0.3V to 14V
- ASEL0, ASEL1 ..... –0.3V to V_{DD33}

Analog Voltages
- V1-V6 ..... –0.3V to 6V

Operating Temperature Range
- LTC2936C ..... 0°C to 70°C
- LTC2936I ..... –40°C to 85°C

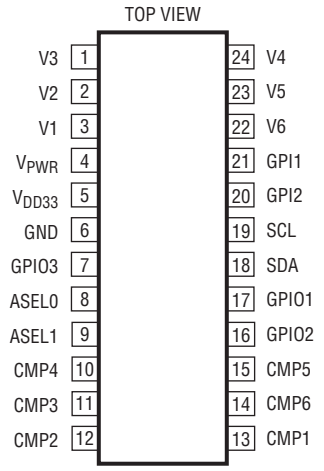
Storage Temperature Range ..... –65°C to 150°C*

Maximum Junction Temperature ..... 125°C*

Lead Temperature Range (Soldering, 10 sec)
- SSOP Package ..... 300°C

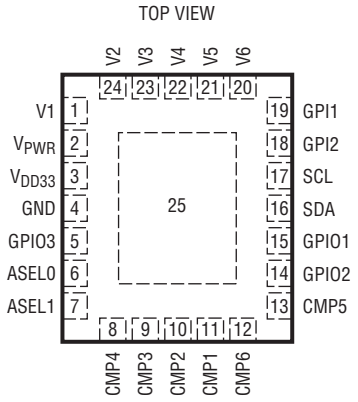
* See Applications Information section for detailed EEPROM derating information for junction temperatures in excess of 85°C.

PIN CONFIGURATION



GN PACKAGE
24-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 88°C/W, θ_{JCtop} = 30°C/W



UFD PACKAGE
24-LEAD (4mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 43°C/W, $\theta_{JCbottom}$ = 3.4°C/W
EXPOSED PAD (PIN 25) IS GND
PCB CONNECTION IS OPTIONAL

ORDER INFORMATION http://www.linear.com/product/LTC2936#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2936CGN#PBF	LTC2936CGN#TRPBF	LTC2936GN	24-Lead Plastic SSOP	0°C to 70°C
LTC2936IGN#PBF	LTC2936IGN#TRPBF	LTC2936GN	24-Lead Plastic SSOP	–40°C to 85°C
LTC2936CUFD#PBF	LTC2936CUFD#TRPBF	2936	24-Lead (4mm × 5mm) Plastic QFN	0°C to 70°C
LTC2936IUFD#PBF	LTC2936IUFD#TRPBF	2936	24-Lead (4mm × 5mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and V_{PWR} = 12V (Note 2).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Characteristics							
V_{PWR}	V_{PWR} Supply Voltage Range		●	3.4		13.9	V
V_{DD33}	V_{DD33} Regulator Output Voltage	I_{VDD33} = –1mA	●	3.23	3.3	3.37	V
I_{DD}	V_{DD33} Regulator Current Limit	V_{DD33} = 0V	●	–10			mA
V_{DDEXT}	V_{DD33} Supply Voltage Range	V_{DD33} = V_{PWR}	●	3.13	3.3	3.47	V
I_{PWR}	V_{PWR} Supply Current	 Writing to EEPROM	● ●			0.7 1.5	mA mA
I_{VDDEXT}	V_{DDEXT} Supply Current	 Writing to EEPROM	● ●			0.7 1.5	mA mA
Voltage Supervisor Characteristics							
V_{RANGE}	V*n* Monitoring Range	Precision Range Low Range Medium Range	● ● ●	0.2 0.5 1		1.2 3 5.8	V
V_{STEP}	V*n* Threshold Programming Step (LSB)	Precision Range Low Range Medium Range			4 10 20		mV
V_{ERR}	V*n* Threshold Accuracy	Precision Range, 0.6V < V*n* < 1.2V Precision Range, 0.2V < V*n* < 0.6V Low Range, 1.5V < V*n* < 3V Low Range, 0.5V < V*n* < 1.5V Medium Range, 3V < V*n* < 5.8V Medium Range, 1V< V*n* <3V	● ● ● ● ● ●			±1 ±6 ±1 ±15 ±1 ±30	% mV % mV % mV
R_{IN}	V*n* Input Impedance	Low and Medium Range and High Range	●	400	600		kΩ
I_{IN}	V*n* Input Current	Precision Range, 1.2V Input	●			±10	nA
t_{RT}	V*n* Comparator Response Time	2 LSB of Overdrive 20 LSB of Overdrive	 ●		15 7.5	 10	µs µs
Manual Reset Characteristics							
t_{MRI}	Input Pulse Width	Active Low	●	5			µs
t_{MRR}	Glitch Rejection				1		µs
CMP*n* Output Characteristics							
V_{OL}	Low Output Voltage	I_{SINK} = 3mA	●			0.4	V
I_{LEAK}	Leakage Current	V_{CMP} = 13.9V	●			±2	µA
I_{PU}	Internal Pull-up Current	V_{CMP} = 2V	●	–5	–15	–30	µA
GPI*n* Characteristics							
V_{ITH}	Input Threshold Voltage		●	0.6	1	1.4	V
I_{LEAK}	Leakage Current	V_{GPI} = 6V	●			±2	µA
I_{PU}	Internal Pull-up Current	V_{GPI} = 2V	●	–5	–15	–30	µA
Auxiliary Comparator Characteristics							
V_{ACIN}	Input Threshold Voltage		●	0.49	0.5	0.51	V
I_{ACIN}	Input Current	Input Voltage = 0.5V	●			±10	nA
t_{ACRT}	Response time	40mV Overdrive			25		µs
GPIO*n* Characteristics							
V_{OL}	Low Output Voltage	I_{SINK} = 3mA	●			0.4	V
V_{ITH}	Input Threshold Voltage		●	0.6	1	1.4	V
I_{LEAK}	Leakage Current	V_{GPIO} = 13.9V	●			±2	µA
I_{PU}	Internal Pull-up Current	V_{GPIO} = 2V	●	–5	–15	–30	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and V_{PWR} = 12V (Note 2).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{DRO}	Programmable Output Delay-On-Release GPIO1_DELAY_ON_RELEASE, GPIO2_DELAY_ON_RELEASE and GPIO3_DELAY_ON_RELEASE	000b	●		0.001	0.050	ms
		001b	●	1	1.6	2.1	ms
		010b	●	4.5	6.4	8.3	ms
		011b	●	17.9	25.6	33.3	ms
		100b	●	35.8	51.2	66.6	ms
		101b	●	143.3	204.8	266.3	ms
		110b	●	286.6	409.6	532.6	ms
		111b	●	1146	1638	2130	ms
EEPROM Characteristics							
Retention	Retention (Notes 5, 6)		●	10			Years
Endurance	Endurance (Notes 5, 6)		●	10,000			Cycles
t_{EEFS}	Fault Storage Time (Note 4)	Backup Fault Storage Operation			10		ms
t_{EEPR}	Programming Time	I^2C NAK's During STORE_USER Operation			100		ms
t_{EERU}	Restore Time	RESTORE_USER Command			1		ms
Digital Inputs SCL, SDA							
V_{IH}	High Level Input Voltage		●	2.0			V
V_{IL}	Low Level Input Voltage		●			0.8	V
V_{HYST}	Input Hysteresis (Note 4)				40		mV
I_{LEAK}	Input Leakage Current	SCL, SDA = GND to 5.5V	●	–1		1	µA
Digital Output SDA							
V_{OL}	Digital Output Low Voltage	I_{SINK} = 3mA	●			0.4	V
Digital Inputs ASEL0, ASEL1							
V_{IH}	Input High Threshold Voltage		●			V_{DD33} – 0.4	V
V_{IL}	Input Low Threshold Voltage		●	0.4			V
$I_{IH,IL}$	High, Low Input Current	ASEL*n* = 0, V_{DD33}	●	–20		20	µA
I_{FLOAT}	High Z Input Current	0.5V< ASEL*n* < V_{DD33} – 0.5V	●	–10		10	µA
Serial Bus Timing Characteristics (Note 3)							
f_{SCL}	Serial Clock Frequency		●	10		400	kHz
t_{LOW}	Serial Clock Low Period		●	1.3			µs
t_{HIGH}	Serial Clock High Period		●	0.6			µs
t_{BUF}	Bus Free Time Between Stop and Start		●	1.3			µs
$t_{HD,STA}$	Start Condition Hold Time		●	600			ns
$t_{SU,STA}$	Start Condition Setup Time		●	600			ns
$t_{SU,STO}$	Stop Condition Setup Time		●	600			ns
$t_{HD,DAT}$	Data Hold Time	LTC2936 Receiving Data	●	0			ns
		LTC2936 Transmitting Data	●	300			ns
$t_{SU,DAT}$	Data Setup Time		●	100			ns
t_{SP}	Pulse Width of Spike Suppressed				100		ns
$t_{TIMEOUT\_BUS}$	Time Allowed to Complete Any PMBus Command After Which Time SDA Will Be Released and Command Terminated				32		ms

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. The LTC2936 is tested with $T_A = T_{CASE}$.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

Note 3: Maximum capacitive load, C_B, for SCL and SDA is 400pF. Data and clock rise time (t_r) and fall time (t_f) are:

$(20 + 0.1 \bullet C_B)$ (ns) < t_r < 300ns, and

$(20 + 0.1 \bullet C_B)$ (ns) < t_f < 300ns

C_B = capacitance of one bus line in pF. SCL and SDA external pull-up voltage, V_{IO}, is 3V < V_{IO} < 5.5V.

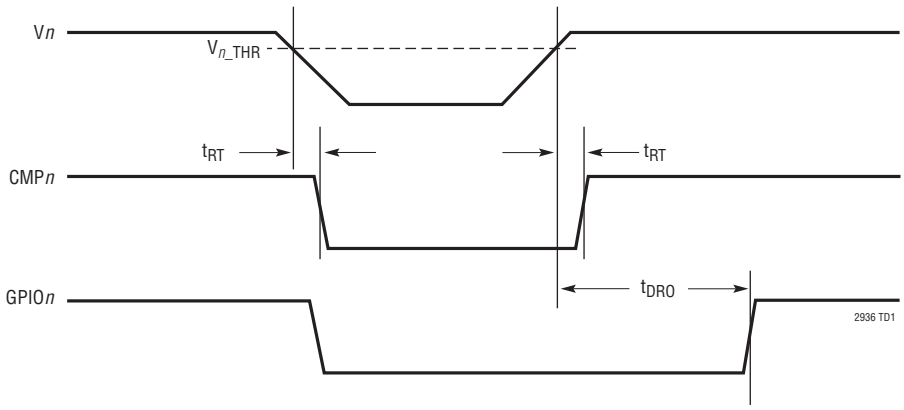
Note 4: Guaranteed by design, not directly tested.

Note 5: EEPROM endurance and retention are guaranteed by design, characterization and correlation with statistical process controls. The minimum retention specification applies for devices whose EEPROM has been cycled less than the minimum endurance specification.

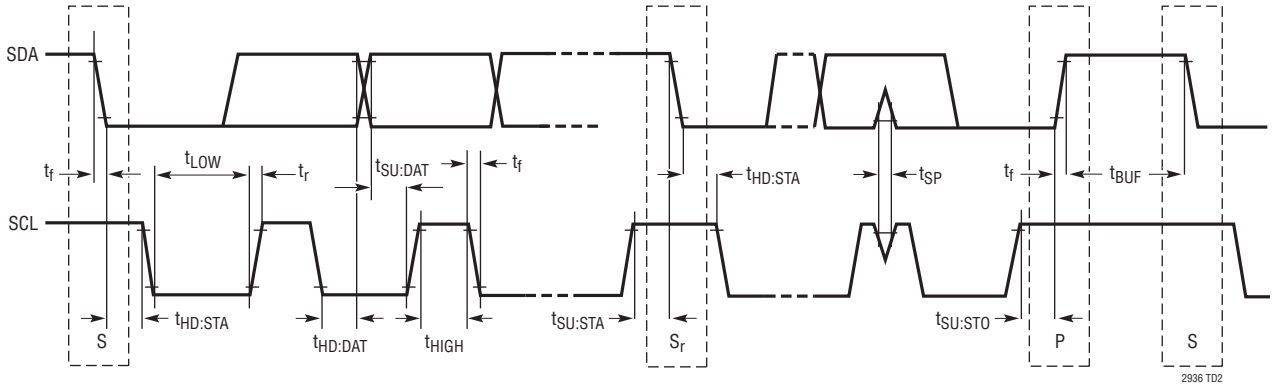
Note 6: EEPROM endurance and retention will be degraded when T_J > 85°C.

TIMING DIAGRAMS

V*n* Supervisor Timing

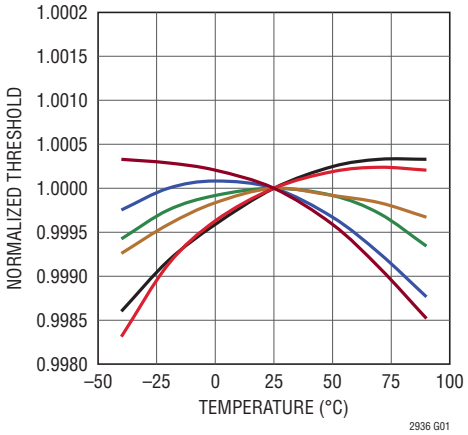


I²C Timing

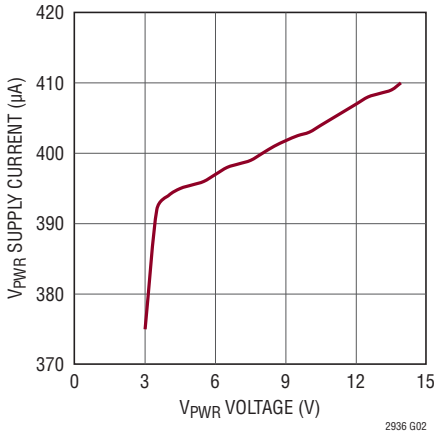


TYPICAL PERFORMANCE CHARACTERISTICS

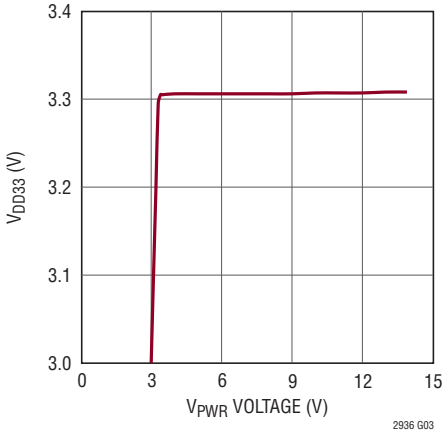
Normalized V1 to V6 Threshold vs Temperature



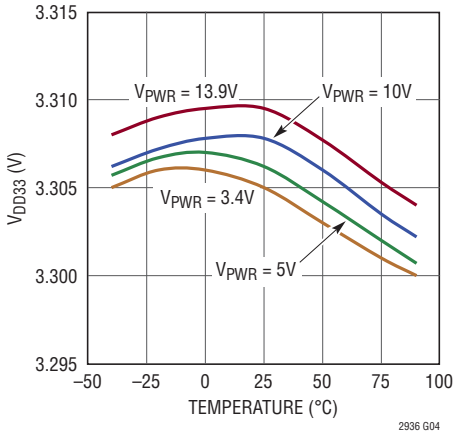
V_{PWR} Supply Current vs Voltage



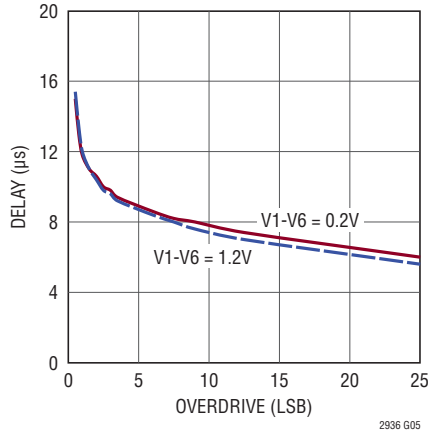
V_{DD33} vs V_{PWR} Supply Voltage



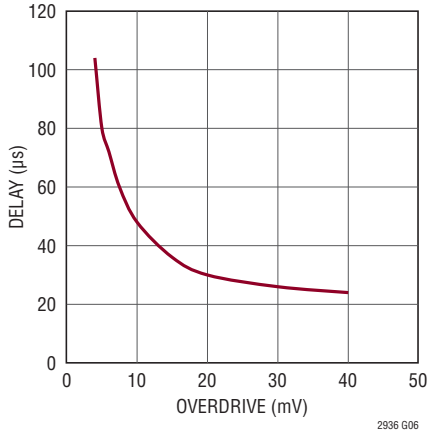
V_{DD33} vs Temperature



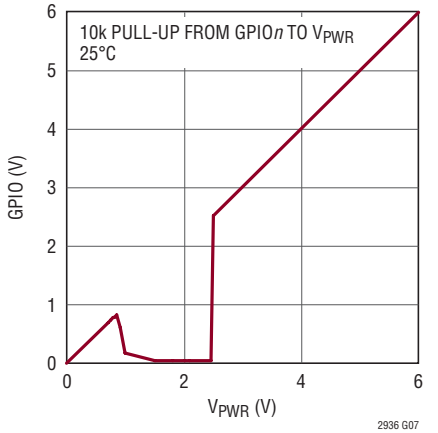
V1-V6 Comp Response Time vs Overdrive



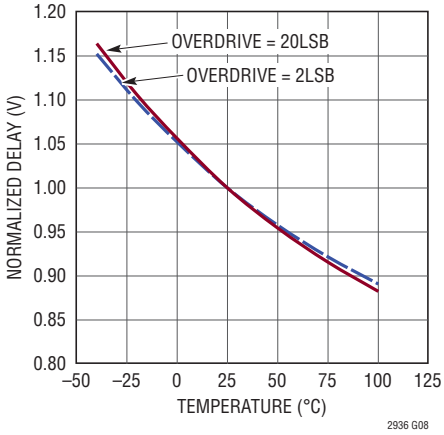
Auxiliary Comp Response Time vs Overdrive



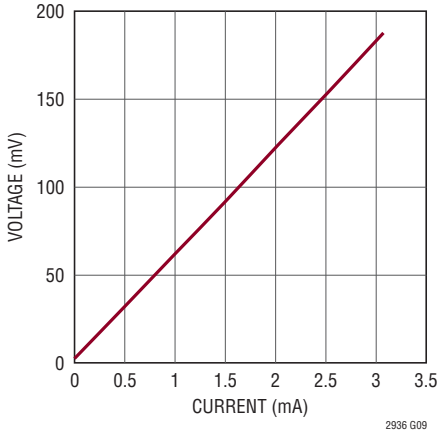
GPIO Pins During Power-Up



Normalized GPIO Delay vs Temperature



GPIO Voltage vs Output Sink Current



PIN FUNCTIONS

ASEL0, ASEL1: I²C Bus Address Select Inputs. Can be connected to ground, V_{DD33} or can be left unconnected to select 1 out of 9 addresses.

CMP1-CMP6: Comparator Open-Drain Outputs. These pins assert low in response to a user-programmable combination of UV and OV conditions on the associated channels. Each output has a 15µA pull-up to V_{DD33}.

Exposed Pad (QFN Package Only): Ground. The exposed pad may be left open or connected to device ground.

GND: Ground.

GPI1, GPI2: General Purpose Inputs. Configurable as one of five possibilities (no duplication):

- Manual reset ($\overline{MR}$) input, active low, 15µA pull-up to V_{DD33}
- UV disable ($\overline{UVDIS}$), active low, 15µA pull-up to V_{DD33}. Outputs ignore UV faults.
- Margin ($\overline{MARG}$), active low, 15µA pull-up to V_{DD33}. Outputs ignore both UV and OV faults.
- Write Protect ($\overline{WP}$), active low, 15µA pull-up to V_{DD33}. I²C write commands are ignored.
- Hi-Z Auxiliary Comparator (AUXC) Input. Programmable polarity.

GPIO1, GPIO2, GPIO3: General Purpose Input/Output. Each GPIO is configurable as either input, open-drain output, or weak pull-up output. Output polarity is programmable. When configured as outputs, these pins respond to selectable UV conditions, OV conditions, $\overline{MR}$, auxiliary comparator output, or other input-configured GPIO*n* with programmable delay-on-release. These pins can also be configured as $\overline{ALERT}$ per SMBus standard. When configured as inputs, each pin can be mapped to any other output. These pins have an optional 15µA pull-up to V_{DD33}. Unused GPIO pins should be tied to V_{DD33} or have their pull-up enabled.

SCL: I²C Serial Clock (400kHz Maximum). Needs external pull-up resistor.

SDA: I²C Serial Data. Needs external pull-up resistor.

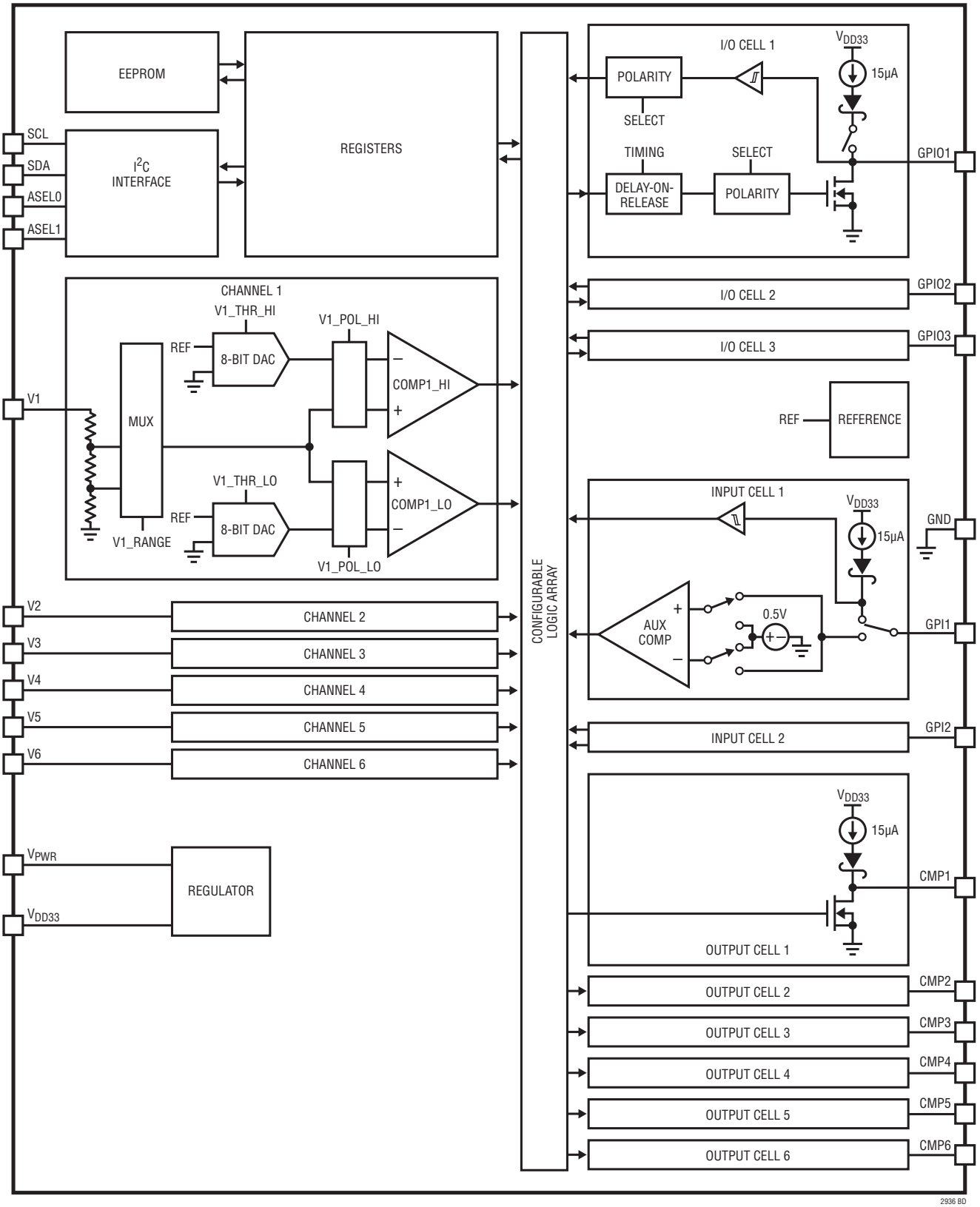
V1-V6: Voltage Supervisor Input. Programmable thresholds from 0.2V to 1.2V in 4mV increments (precision range), from 0.5V to 3V in 10mV increments (low range) or from 1V to 5.8V in 20mV increments (medium range). See the Applications Information section for information on unused channels.

V_{DD33}: 3.3V Internal Regulator Output. A 100nF capacitor to ground is required. The internal regulator can be disabled by connecting V_{PWR} to V_{DD33} and operating from an external 3.3V supply.

V_{PWR}: Power Supply Input (Internal Regulator Input). Power supply range is 3.4V to 13.9V. Bypass this pin to ground with a 100nF (or greater) capacitor. The internal regulator can be disabled by connecting V_{PWR} to V_{DD33} and operating from an external 3.3V supply.

PIN NAME	PIN TYPE	PIN (SSOP)	PIN (QFN)
V3	IN	1	23
V2	IN	2	24
V1	IN	3	1
V_{PWR}	IN	4	2
V_{DD33}	OUT/IN	5	3
GND	GND	6	4, 25
GPIO3	IN/OUT	7	5
ASEL0	IN	8	6
ASEL1	IN	9	7
CMP4	OUT	10	8
CMP3	OUT	11	9
CMP2	OUT	12	10
CMP1	OUT	13	11
CMP6	OUT	14	12
CMP5	OUT	15	13
GPIO2	IN/OUT	16	14
GPIO1	IN/OUT	17	15
SDA	IN/OUT	18	16
SCL	IN	19	17
GPI2	IN	20	18
GPI1	IN	21	19
V6	IN	22	20
V5	IN	23	21
V4	IN	24	22

BLOCK DIAGRAM



OPERATION

The LTC2936 can perform the following operations:

- Accept I²C bus programming commands.
- Simultaneously monitor up to six inputs with respect to I²C bus programmed fault limits and assert/de-assert the associated CMP*n* outputs in response to OV and/or UV faults.
- Configure and monitor for OV/UV faults using two independent comparators per channel.
- Configure two general purpose inputs as manual reset ($\overline{MR}$), undervoltage disable ($\overline{UVDIS}$), margin ($\overline{MARG}$), write protect ($\overline{WP}$) or auxiliary comparator (AUXC) inputs.
- Configure three general purpose inputs/outputs (GPIO*n*) to output faults, inputs from GPI*n* or from other GPIO*n*.
- Independently select each general purpose output polarity and type (open-drain or weak pull-up).
- Independently select each general purpose output response delay-on-release (with respect to the moment its condition is internally cleared).
- Generate interrupt ($\overline{ALERT}$) signals in response to any voltage faults, as well as the logic state of the inputs.
- Store register contents to EEPROM.
- Store voltage and timing fault history to EEPROM.
- Restore EEPROM contents into the operating memory, by I²C command and at power-up.
- Report voltage fault status and history.
- Hardware and/or software write-protect the operating memory.

THRESHOLD ACCURACY

The LTC2936 ±1% threshold accuracy specification improves the reliability of the system over supervisors with wider threshold tolerances. A less accurate voltage supervisor increases the required system voltage margin. This in turn increases the probability of system malfunction.

Consider a 5V ±10% supply: it may vary between 4.5V and 5.5V and the circuitry powered by it must operate reliably within this band. An ideal, perfectly accurate supervisor would generate a reset at exactly 4.5V. The LTC2936 threshold varies ±1% around the nominal threshold voltage, in the medium range, if the selected value is greater than 3V. The reset threshold band and the power supply tolerance bands should not overlap, in order to prevent false alarms when the power supply actually meets its specified tolerance band (see Figure 1).

A ±10% threshold is usually set to 11% below the nominal input voltage, or 4.45V in this example. The threshold is guaranteed to be within the 4.4V to 4.5V band over temperature. To prevent malfunction, the powered system must operate reliably down to 4.4V.

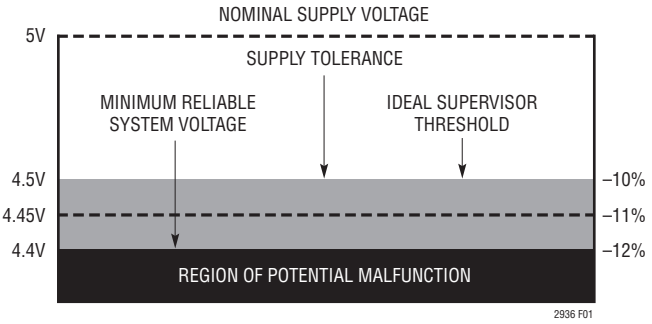


Figure 1. 1% Threshold Accuracy Improves System Reliability

OPERATION

I²C Serial Digital Interface

The LTC2936 communicates with a host (master) using the I²C serial bus interface. The Timing Diagram shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines.

The LTC2936 is a transmit/receive slave only device. The master device must initiate data transfer on the bus by generating SCL to allow the transfer. In the event of an OV/UV fault, the LTC2936 can be configured to assert the $\overline{\text{ALERT}}$ output low in order to notify the host.

Slave Address

The LTC2936 can respond to one of 9 addresses. By connecting the address ASEL0 and ASEL1 inputs to V_{DD33}, GND, or by floating them, the slave address is determined as shown in the following table. The LTC2936 always responds to the special addresses.

LTC2936 Address Look-Up Table

ASEL0	0	Hi-Z	1	0	Hi-Z	1	0	Hi-Z	1
ASEL1	**0**	**0**	**0**	**Hi-Z**	**Hi-Z**	**Hi-Z**	**1**	**1**	**1**
7-Bit Address	0x50	0x51	0x52	0x53	0x54	0x55	0x58	0x59	0x5A
8-Bit Address	0xA0	0xA2	0xA4	0xA6	0xA8	0xAA	0xB0	0xB2	0xB4

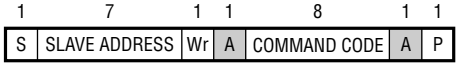
LTC2936 Special Slave Addresses

7-BIT ADDRESS	8-BIT ADDRESS	DESCRIPTION
0x0C	0x19	Alert Response Address, Independent of the ASEL pin.
0x73	0xE6	Global address to which all LTC2936's will respond. Independent of the ASEL pin.

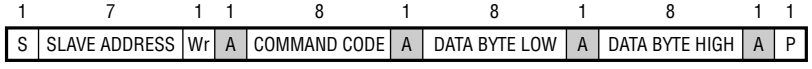
Communication Protocols

S START CONDITION
Sr REPEATED START CONDITION
Rd READ (BIT VALUE OF 1)
Wr WRITE (BIT VALUE OF 0)
A ACKNOWLEDGE
$\overline{A}$ NOT ACKNOWLEDGE
P STOP CONDITION
□ MASTER TO SLAVE
▒ SLAVE TO MASTER

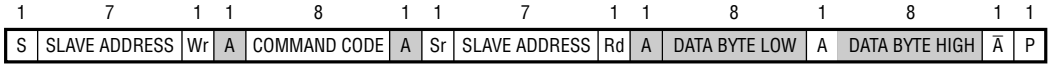
Send Byte Format



Write Word Format



Read Word Format



2936 F00

OPERATION

Register Command Set

COMMAND FUNCTION	DESCRIPTION	R/W/S (See Note)	DATA LENGTH (BITS)	COMMAND BYTE	DEFAULT VALUE
WRITE_PROTECT	Contains lock key code and write lock.	R/W	16	0x00	1010_1010_1010_1000b
GPI_CONFIG	Configure GPI2 and GPI1 assignment, GPIO*n* mapping and $\overline{MR}$ internal response.	R/W	16	0x01	X001_0000_X000_0000b
GPIO1_CONFIG	Configure GPIO1 type, delay-on-release and mapping to GPIO2, GPIO3.	R/W	16	0x02	X000_0000_0010_1011b
GPIO2_3_CONFIG	Configure GPIO3 type, delay-on-release and mapping to GPIO1 and GPIO2. Configure GPIO2 type, delay-on-release and mapping to GPIO1 and GPIO3.	R/W	16	0x03	0010_1011_0010_1011b
V1_THR	Encode high and low voltage thresholds on channel V1.	R/W	16	0x04	1110_0110_1011_0100b
V2_THR	Encode high and low voltage thresholds on channel V2.	R/W	16	0x05	1000_1001_0110_1000b
V3_THR	Encode high and low voltage thresholds on channel V3.	R/W	16	0x06	0101_1101_0100_0100b
V4_THR	Encode high and low voltage thresholds on channel V4.	R/W	16	0x07	1001_1001_0111_0101b
V5_THR	Encode high and low voltage thresholds on channel V5	R/W	16	0x08	0111_1000_0101_1010b
V6_THR	Encode high and low voltage thresholds on channel V6.	R/W	16	0x09	0101_0111_0011_1111b
V1_CONFIG	Encode comparator range, polarity and GPIO*n* mapping.	R/W	16	0x0A	XXX0_1100_1000_1001b
V2_CONFIG	Encode comparator range, polarity and GPIO*n* mapping.	R/W	16	0x0B	XXX0_1100_1000_1001b
V3_CONFIG	Encode comparator range, polarity and GPIO*n* mapping.	R/W	16	0x0C	XXX0_1100_1000_1001b
V4_CONFIG	Encode comparator range, polarity and GPIO*n* mapping.	R/W	16	0x0D	XXX0_1101_1000_1001b
V5_CONFIG	Encode comparator range, polarity and GPIO*n* mapping.	R/W	16	0x0E	XXX0_1101_1000_1001b
V6_CONFIG	Encode comparator range, polarity and GPIO*n* mapping.	R/W	16	0x0F	XXX0_1101_1000_1001b
HISTORY_WORD	Read the fault history. Read only.	R	16	0x11	NA
PADS	Return the status of the GPI*n*, GPIO*n* and CMP*n* pins.	R	16	0x1A	NA
CLEAR_HISTORY	Clear volatile memory history register. Write only.	S	0	0x1B	NA
STORE_USER	Store volatile memory to EEPROM. Write only.	S	0	0x1C	NA
RESTORE_USER	Restore volatile memory from EEPROM. Write only.	S	0	0x1D	NA
BACKUP_WORD	Read the EEPROM backup of the first fault history. Read only.	R	16	0x1E	NA
STATUS_WORD	Read the fault status. Read only.	R	16	0x1F	NA

Note: R = Read, W = Write, S = Send Byte.

OPERATION

DETAILED COMMAND REGISTER DESCRIPTIONS

WRITE_PROTECT (Command Byte 0x00)

The WRITE_PROTECT command provides the ability to prevent any write operations into the volatile memory, if WRITE_LOCK = 1. KEY may be changed when WRITE_LOCK = 0, or in the same command that sets WRITE_LOCK = 1.

When locked, WRITE_LOCK can only be written to 0 if KEY matches the existing value in memory. For effective protection against false writes, KEY should contain at least one bit set to 1.

Writes to supported commands are ignored when WRITE_LOCK = 1 or when a GPI*n* input configured for $\overline{WP}$ is held low. All commands may be read regardless of the WRITE_LOCK bit setting.

WRITE_PROTECT Data Contents

BIT(S)	SYMBOL	PURPOSE
b[15:2]	KEY	Must match against programmed combination in order to deactivate write lock. Factory default 10_1010_1010_1010b (0x2AAA).
b[1]	Reserved	Ignore
b[0]	WRITE_LOCK	0: Unlocked. Writes to volatile memory are permitted. 1: Locked. Writing to volatile memory is not permitted. To unlock, set WRITE_LOCK = 0 with the appropriate key. If a GPI*n* input is configured for $\overline{WP}$, and is low, then reading WRITE_PROTECT will always return WRITE_LOCK = 1. Factory default 0.

OPERATION

GPI_CONFIG (Command Byte 0x01)

The GPI_CONFIG command configures internal response to a manual reset, sets each GPI function, and optionally maps GPI pins configured as Manual Reset ($\overline{MR}$) or Auxiliary Comparator (AUXC) to one or more GPIO pins.

GPI_CONFIG Data Contents

BIT(S)	SYMBOL	OPERATION
b[15]	Reserved	Ignore
b[14]	GPI2_MR_RESPONSE	Effective only if the input GPI2 is $\overline{MR}$ configured. 0: Disable CLEAR_HISTORY response. 1: Enable CLEAR_HISTORY response on falling edge of GPI2. Factory default 0.
b[13:11]	GPI2_CONFIG	000b: Manual Reset ($\overline{MR}$) active low, 15µA pull-up. 001b: Reserved. 010b: Margin ($\overline{MARG}$) active low, 15µA pull-up. Overvoltage and undervoltage faults are inhibited. 011b: UV Disable ($\overline{UVDIS}$) active low, 15µA pull-up. Undervoltage faults are inhibited. 100b: Write Protect ($\overline{WP}$). 101b: Auxiliary Comparator (AUXC) positive input on GPI2. 110b: and 111b: Auxiliary Comparator (AUXC) negative input on GPI2. Factory default 010b.
b[10]	MAP_GPI2_TO_GPIO3	0: GPI2 input is not mapped to GPIO3. 1: GPI2 input is mapped to GPIO3 if configured as $\overline{MR}$ or AUXC. Factory default 0.
b[9]	MAP_GPI2_TO_GPIO2	0: GPI2 input is not mapped to GPIO2. 1: GPI2 input is mapped to GPIO2 if configured as $\overline{MR}$ or AUXC. Factory default 0.
b[8]	MAP_GPI2_TO_GPIO1	0: GPI2 input is not mapped to GPIO1. 1: GPI2 input is mapped to GPIO1 if configured as $\overline{MR}$ or AUXC. Factory default 0.
b[7]	Reserved	Ignore
b[6]	GPI1_MR_RESPONSE	Effective only if the input GPI1 is $\overline{MR}$ configured. 0: Disable CLEAR_HISTORY response. 1: Enable CLEAR_HISTORY response on falling edge of GPI1. Factory default 0.
b[5:3]	GPI1_CONFIG	000b: Manual Reset ($\overline{MR}$) active low, 15µA pull-up. 001b: Reserved. 010b: Margin ($\overline{MARG}$) active low, 15µA pull-up. Overvoltage and undervoltage faults are inhibited. 011b: UV Disable ($\overline{UVDIS}$) active low, 15µA pull-up. Undervoltage faults are inhibited. 100b: Write Protect ($\overline{WP}$). 101b: Auxiliary Comparator (AUXC) positive input on GPI1. 110b: and 111b: Auxiliary Comparator (AUXC) negative input on GPI1. Factory default 000b.
b[2]	MAP_GPI1_TO_GPIO3	0: GPI1 input is not mapped to GPIO3. 1: GPI1 input is mapped to GPIO3 if configured as $\overline{MR}$ or AUXC. Factory default 0.
b[1]	MAP_GPI1_TO_GPIO2	0: GPI1 input is not mapped to GPIO2. 1: GPI1 input is mapped to GPIO2 if configured as $\overline{MR}$ or AUXC. Factory default 0.
b[0]	MAP_GPI1_TO_GPIO1	0: GPI1 input is not mapped to GPIO1. 1: GPI1 input is mapped to GPIO1 if configured as $\overline{MR}$ or AUXC. Factory default 0.

OPERATION

GPIO1_CONFIG (Command Byte 0x02)

The GPIO1_CONFIG command configures the GPIO1 mapping, delay-on-release time, output type, and polarity. If GPIO1_TYPE_AND_POLARITY is configured as $\overline{\text{ALERT}}$ (100b or 111b), the output is latched and cleared after the LTC2936 acknowledges the alert response address (see SMBus protocol), HISTORY_WORD is read, or a CLEAR_HISTORY command is received. Only one GPIO*n* pin should be configured as $\overline{\text{ALERT}}$. GPIO*n*_DELAY_ON_RELEASE does not apply to a GPIO*n* pin configured as $\overline{\text{ALERT}}$.

WD_GPIO1_CONFIG Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:8]	Reserved	Ignore
b[7]	MAP_GPIO1_TO_GPIO3	0: GPIO1 input is not mapped to GPIO3. 1: GPIO1 input is mapped to GPIO3. Factory default 0.
b[6]	MAP_GPIO1_TO_GPIO2	0: GPIO1 input is not mapped to GPIO2. 1: GPIO1 input is mapped to GPIO2. Factory default 0.
b[5:3]	GPIO1_DELAY_ON_RELEASE	000b: Delay selected is 0. 001b: Delay selected is 1.6ms. 010b: Delay selected is 6.4ms. 011b: Delay selected is 26ms. 100b: Delay selected is 51ms. 101b: Delay selected is 205ms. 110b: Delay selected is 410ms. 111b: Delay selected is 1.64s. Factory default 101b (205ms).
b[2:0]	GPIO1_TYPE_AND_POLARITY	000b: Active H input. 001b: Active L input. 010b: Active H open-drain output. 011b: Active L open-drain output. 100b: Active L open-drain $\overline{\text{ALERT}}$ output. 101b: Active H, weak pull-up output. 110b: Active L, weak pull-up output. 111b: Active L, weak pull-up $\overline{\text{ALERT}}$ output. Factory default 011b (Active L open-drain output).

OPERATION

GPIO2_3_CONFIG (Command Byte 0x03)

The GPIO2_3_CONFIG command configures GPIO2 and GPIO3 mapping, delay-on-release time, output type, and polarity. If GPIO2_TYPE_AND_POLARITY is configured as $\overline{\text{ALERT}}$ (100b or 111b), or GPIO3_TYPE_AND_POLARITY is configured as $\overline{\text{ALERT}}$ (100b or 111b), the output is latched, and is cleared after the LTC2936 acknowledges the alert response address (see SMBus protocol), HISTORY_WORD is read, or a CLEAR_HISTORY command is received. Only one GPIO*n* pin should be configured as $\overline{\text{ALERT}}$. GPIO*n*_DELAY_ON_RELEASE does not apply to a GPIO*n* pin configured as $\overline{\text{ALERT}}$.

GPIO2_3_CONFIG Data Contents

BIT(S)	SYMBOL	OPERATION
b[15]	MAP_GPIO3_TO_GPIO2	0: GPIO3 is not mapped into GPIO2. 1: GPIO3 is mapped into GPIO2. Factory default 0.
b[14]	MAP_GPIO3_TO_GPIO1	0: GPIO3 is not mapped into GPIO1. 1: GPIO3 is mapped into GPIO1. Factory default 0.
b[13:11]	GPIO3_DELAY_ON_RELEASE	000b: Delay selected is 0. 001b: Delay selected is 1.6ms. 010b: Delay selected is 6.4ms. 011b: Delay selected is 26ms. 100b: Delay selected is 51ms. 101b: Delay selected is 205ms. 110b: Delay selected is 410ms. 111b: Delay selected is 1.64s. Factory default 101b (205ms).
b[10:8]	GPIO3_TYPE_AND_POLARITY	000b: Active H input. 001b: Active L input. 010b: Active H open-drain output. 011b: Active L open-drain output. 100b: Active L open-drain $\overline{\text{ALERT}}$ output. 101b: Active H, weak pull-up output. 110b: Active L, weak pull-up output. 111b: Active L, weak pull-up $\overline{\text{ALERT}}$ output. Factory default 011b (Active L open-drain output).
b[7]	MAP_GPIO2_TO_GPIO3	0: GPIO2 is not mapped into GPIO3. 1: GPIO2 is mapped into GPIO3. Factory default 0.
b[6]	MAP_GPIO2_TO_GPIO1	0: GPIO2 is not mapped into GPIO1. 1: GPIO2 is mapped into GPIO1. Factory default 0.
b[5:3]	GPIO2_DELAY_ON_RELEASE	000b: Delay selected is 0. 001b: Delay selected is 1.6ms. 010b: Delay selected is 6.4ms. 011b: Delay selected is 26ms. 100b: Delay selected is 51ms. 101b: Delay selected is 205ms. 110b: Delay selected is 410ms. 111b: Delay selected is 1.64s. Factory default 101b (205ms).
b[2:0]	GPIO2_TYPE_AND_POLARITY	000b: Active H input. 001b: Active L input. 010b: Active H open-drain output. 011b: Active L open-drain output. 100b: Active L open-drain $\overline{\text{ALERT}}$ output. 101b: Active H, weak pull-up output. 110b: Active L, weak pull-up output. 111b: Active L, weak pull-up $\overline{\text{ALERT}}$ output. Factory default 011b (Active L open-drain output).

OPERATION

V1_THR (Command Byte 0x04), V2_THR (0x05), V3_THR (0x06), V4_THR (0x07),V5_THR (0x08), V6_THR (0x09)

The V*n*_THR command allows the user to specify the high and low threshold monitoring voltages on each channel.

V*n*_THR Data Contents Channels V1 to V6

BIT(S)	SYMBOL	OPERATION
b[15:8]	V*n*_THR_HI	The COMP*n*_HI threshold. See the Applications Information section. Factory default settings of 0xE6, 0x89, 0x5D, 0x99, 0x78, 0x57 correspond to 5.5V, 3.64V, 2.76V, 1.98V, 1.65V and 1.32V for channels V1 to V6, respectively.
b[7:0]	V*n*_THR_LO	The COMP*n*_LO threshold. See the Applications Information section. Factory default settings of 0xB4, 0x68, 0x44, 0x75, 0x5A, 0x3F correspond to 4.5V, 2.98V, 2.26V, 1.62V 1.35V and 1.08V for channels V1 to V6, respectively.

V1_CONFIG (Command Byte 0x0A), V2_CONFIG (0x0B), V3_CONFIG (0x0C), V4_CONFIG (0x0D), V5_CONFIG (0x0E), V6_CONFIG (0x0F)

The V*n*_CONFIG command programs V1 through V6 comparator range, polarity and mapping to GPIO*n* and CMP*n*.

V*n*_CONFIG Data Contents Channels V1 to V6

BIT(S)	SYMBOL	OPERATION
b[15:13]	Reserved	Ignore
b[12]	CMP*n*_LATCH	0: CMP*n* output not latched. 1: CMP*n* output latched. Factory default 0.
b[11]	MAP_COMP*n*_HI_TO_CMP*n*	0: High comparator not mapped to CMP*n*. 1: High comparator mapped to CMP*n*. Factory default 1.
b[10]	MAP_COMP*n*_LO_TO_CMP*n*	0: Low comparator not mapped to CMP*n*. 1: Low comparator mapped to CMP*n*. Factory default 1.
b[9:8]	V*n*_RANGE	00b: Medium Range. 01b: Low Range. 10b and 11b: Precision Range. Factory defaults are 00b on V1-V3 and 01b on V4-V6.
b[7]	V*n*_POL_HI	Controls polarity of COMP*n*_HI output reported by STATUS_WORD. See STATUS_WORD description for details. 0: Undervoltage. Indicates a fault when the input voltage is below V*n*_THR_HI. 1: Overvoltage. Indicates a fault when the input voltage is above V*n*_THR_HI. Factory default 1.
b[6]	V*n*_POL_LO	Controls polarity of COMP*n*_LO output reported by STATUS_WORD. See STATUS_WORD description for details. 0: Undervoltage. Indicates a fault when the input voltage is below V*n*_THR_LO. 1: Overvoltage. Indicates a fault when the input voltage is above V*n*_THR_LO. Factory default 0.
b[5]	MAP_COMP*n*_HI_TO_GPIO3	0: High comparator not mapped to GPIO3. 1: High comparator mapped to GPIO3. Factory default 0.
b[4]	MAP_COMP*n*_HI_TO_GPIO2	0: High comparator not mapped to GPIO2. 1: High comparator mapped to GPIO2. Factory default 0.

OPERATION

V*n*_CONFIG Data Contents Channels V1 to V6

b[3]	MAP_COMP*n*_HI_TO_GPIO1	0: High comparator not mapped to GPIO1. 1: High comparator mapped to GPIO1. Factory default 1.
b[2]	MAP_COMP*n*_LO_TO_GPIO3	0: Low comparator not mapped to GPIO3. 1: Low comparator mapped to GPIO3. Factory default 0.
b[1]	MAP_COMP*n*_LO_TO_GPIO2	0: Low comparator not mapped to GPIO2. 1: Low comparator mapped to GPIO2. Factory default 0.
b[0]	MAP_COMP*n*_LO_TO_GPIO1	0: Low comparator not mapped to GPIO1. 1: Low comparator mapped to GPIO1. Factory default 1.

HISTORY_WORD (Command Byte 0x11)

The HISTORY_WORD command returns two bytes of information with a summary of the faults since power was applied or HISTORY_WORD was last cleared. HISTORY_WORD is located in volatile memory and is automatically updated each time a fault occurs. HISTORY_WORD is cleared using the CLEAR_HISTORY command.

HISTORY_WORD Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:13]	Reserved	Ignore
b[12]	V6_HI_LATCHED_FAULT	1: Latched V6_HI_FAULT. 0: No fault.
b[11]	V6_LO_LATCHED_FAULT	1: Latched V6_LO_FAULT. 0: No fault.
b[10]	V5_HI_LATCHED_FAULT	1: Latched V5_HI_FAULT. 0: No fault.
b[9]	V5_LO_LATCHED_FAULT	1: Latched V5_LO_FAULT. 0: No fault.
b[8]	V4_HI_LATCHED_FAULT	1: Latched V4_HI_FAULT. 0: No fault.
b[7]	V4_LO_LATCHED_FAULT	1: Latched V4_LO_FAULT. 0: No fault.
b[6]	V3_HI_LATCHED_FAULT	1: Latched V3_HI_FAULT. 0: No fault.
b[5]	V3_LO_LATCHED_FAULT	1: Latched V3_LO_FAULT. 0: No fault.
b[4]	V2_HI_LATCHED_FAULT	1: Latched V2_HI_FAULT. 0: No fault.
b[3]	V2_LO_LATCHED_FAULT	1: Latched V2_LO_FAULT. 0: No fault.
b[2]	V1_HI_LATCHED_FAULT	1: Latched V1_HI_FAULT. 0: No fault.
b[1]	V1_LO_LATCHED_FAULT	1: Latched V1_LO_FAULT. 0: No fault.
b[0]	Reserved	Ignore

OPERATION

PADS (Command Byte 0x1A)

The PADS register returns the status of the GPI*n*, GPIO*n* and CMP*n* pads.

PADS Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:11]	Reserved	Ignore
b[10]	GPI2_STATUS	0: GPI2 pin is logic low. 1: GPI2 pin is logic high.
b[9]	GPI1_STATUS	0: GPI1 pin is logic low. 1: GPI1 pin is logic high.
b[8]	GPIO3_STATUS	0: GPIO3 pin is logic low. 1: GPIO3 pin is logic high.
b[7]	GPIO2_STATUS	0: GPIO2 pin is logic low. 1: GPIO2 pin is logic high.
b[6]	GPIO1_STATUS	0: GPIO1 pin is logic low. 1: GPIO1 pin is logic high.
b[5]	CMP6_STATUS	0: CMP6 pin is logic low. 1: CMP6 pin is logic high.
b[4]	CMP5_STATUS	0: CMP5 pin is logic low. 1: CMP5 pin is logic high.
b[3]	CMP4_STATUS	0: CMP4 pin is logic low. 1: CMP4 pin is logic high.
b[2]	CMP3_STATUS	0: CMP3 pin is logic low. 1: CMP3 pin is logic high.
b[1]	CMP2_STATUS	0: CMP2 pin is logic low. 1: CMP2 pin is logic high.
b[0]	CMP1_STATUS	0: CMP1 pin is logic low. 1: CMP1 pin is logic high.

CLEAR_HISTORY (Command Byte 0x1B)

The CLEAR_HISTORY command clears all the faults logged in the volatile HISTORY_WORD register. A manual reset performs the same operation if GPI*n*_MR_RESPONSE = 1. Clearing HISTORY_WORD does not affect the STATUS_WORD content. Processing of the CLEAR_HISTORY command typically takes less than 10ms, and the part will not acknowledge other I^2C operations during that time.

STORE_USER (Command Byte 0x1C)
RESTORE_USER (Command Byte 0x1D)

The STORE_USER and RESTORE_USER commands access nonvolatile EEPROM memory. Once a command is stored in EEPROM using STORE_USER, it will be restored to volatile operating memory with the RESTORE_USER command or when the part powers up.

BACKUP_WORD (Command Byte 0x1E)

After the first fault occurs, HISTORY_WORD is written to EEPROM for backup. Any subsequent BACKUP_WORD write following a fault is inhibited until the CLEAR_HISTORY command is issued. BACKUP_WORD can be retrieved by sending a RESTORE_USER command followed by a BACKUP_WORD read. BACKUP_WORD can be cleared in EEPROM by sending a CLEAR_HISTORY command followed by a STORE_USER command.

OPERATION

STATUS_WORD (Command Byte 0x1F)

The STATUS_WORD command returns two bytes of information with a summary of the current faults. The STATUS_WORD content is read directly from the comparators and is a snapshot of the current state. STATUS_WORD faults may be disabled by setting GPI1_CONFIG = 010b ($\overline{\text{MARG}}$), GPI1_CONFIG = 011b ($\overline{\text{UVDIS}}$), GPI2_CONFIG = 010b ($\overline{\text{MARG}}$) or GPI2_CONFIG = 011b ($\overline{\text{UVDIS}}$) and asserting the appropriate GPI*n* pin.

STATUS_WORD Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:13]	Reserved	Ignore
b[12]	V6_HI_FAULT	V6_POL_HI = 1 (default). 1: Fault (V6 greater than V6_THR_HI). 0: No fault (V6 less than V6_THR_HI). V6_POL_HI = 0. 1: Fault (V6 less than V6_THR_HI). 0: No fault (V6 greater than V6_THR_HI).
b[11]	V6_LO_FAULT	V6_POL_LO = 1. 1: Fault (V6 greater than V6_THR_LO). 0: No fault (V6 less than V6_THR_LO). V6_POL_LO = 0 (default). 1: Fault (V6 less than V6_THR_LO). 0: No fault (V6 greater than V6_THR_LO).
b[10]	V5_HI_FAULT	V5_POL_HI = 1 (default). 1: Fault (V5 greater than V5_THR_HI). 0: No fault (V5 less than V5_THR_HI). V5_POL_HI = 0. 1: Fault (V5 less than V5_THR_HI). 0: No fault (V5 greater than V5_THR_HI).
b[9]	V5_LO_FAULT	V5_POL_LO = 1. 1: Fault (V5 greater than V5_THR_LO). 0: No fault (V5 less than V5_THR_LO). V5_POL_LO = 0 (default). 1: Fault (V5 less than V5_THR_LO). 0: No fault (V5 greater than V5_THR_LO).
b[8]	V4_HI_FAULT	V4_POL_HI = 1 (default). 1: Fault (V4 greater than V4_THR_HI). 0: No fault (V4 less than V4_THR_HI). V4_POL_HI = 0. 1: Fault (V4 less than V4_THR_HI). 0: No fault (V4 greater than V4_THR_HI).
b[7]	V4_LO_FAULT	V4_POL_LO = 1. 1: Fault (V4 greater than V4_THR_LO). 0: No fault (V4 less than V4_THR_LO). V4_POL_LO = 0 (default). 1: Fault (V4 less than V4_THR_LO). 0: No fault (V4 greater than V4_THR_LO).

OPERATION

STATUS_WORD Data Contents

b[6]	V3_HI_FAULT	V3_POL_HI = 1 (default). 1: Fault (V3 greater than V3_THR_HI). 0: No fault (V3 less than V3_THR_HI). V3_POL_HI = 0. 1: Fault (V3 less than V3_THR_HI). 0: No fault (V3 greater than V3_THR_HI).
b[5]	V3_LO_FAULT	V3_POL_LO = 1. 1: Fault (V3 greater than V3_THR_LO). 0: No fault (V3 less than V3_THR_LO). V3_POL_LO = 0 (default). 1: Fault (V3 less than V3_THR_LO). 0: No fault (V3 greater than V3_THR_LO).
b[4]	V2_HI_FAULT	V2_POL_HI = 1 (default). 1: Fault (V2 greater than V2_THR_HI). 0: No fault (V2 less than V2_THR_HI). V2_POL_HI = 0. 1: Fault (V2 less than V2_THR_HI). 0: No fault (V2 greater than V2_THR_HI).
b[3]	V2_LO_FAULT	V2_POL_LO = 1. 1: Fault (V2 greater than V2_THR_LO). 0: No fault (V2 less than V2_THR_LO). V2_POL_LO = 0 (default). 1: Fault (V2 less than V2_THR_LO). 0: No fault (V2 greater than V2_THR_LO).
b[2]	V1_HI_FAULT	V1_POL_HI = 1 (default). 1: Fault (V1 greater than V1_THR_HI). 0: No fault (V1 less than V1_THR_HI). V1_POL_HI = 0. 1: Fault (V1 less than V1_THR_HI). 0: No fault (V1 greater than V1_THR_HI).
b[1]	V1_LO_FAULT	V1_POL_LO = 1. 1: Fault (V1 greater than V1_THR_LO). 0: No fault (V1 less than V1_THR_LO). V1_POL_LO = 0 (default). 1: Fault (V1 less than V1_THR_LO). 0: No fault (V1 greater than V1_THR_LO).
b[0]	Reserved	Ignore

APPLICATIONS INFORMATION

Power Supply

The LTC2936 is powered from the V_{PWR} input and generates a regulated 3.3V supply on the V_{DD33}. A 100nF external capacitor from V_{PWR} to GND is required in order to decouple any supply noise. A 100nF external capacitor from V_{DD33} to GND is required to properly compensate the internal voltage regulator.

To power the LTC2936 directly from an external 3.3V power supply, connect the V_{PWR} and V_{DD33} pins together and connect them to the external 3.3V supply. This mode of operation is useful for reducing power dissipation.

Power-Up Condition

When power is applied, the part turns on and the EEPROM contents are loaded into the volatile operating memory. This operation typically takes less than 200µs.

Voltage Threshold Programming

The medium range is based on a full scale of 0.9V to 6V. The 8-bit programming step size is 20mV. On the medium range, threshold accuracy below 1V and above 5.8V is not specified, but the thresholds are reachable.

The command byte for the voltage threshold can be calculated for the medium range with the following equation:

$$\text{Command Byte} = \text{ROUND}\,[50 \bullet (V_{TH} - 0.9)]$$

The low range is based on a full scale of 0.45V to 3V. The 8-bit programming step size is 10mV. On the low range, threshold accuracy below 0.5V is not specified, but the thresholds are reachable.

The command byte for the voltage threshold can be calculated for the low range with the following equation:

$$\text{Command Byte} = \text{ROUND}\,[100 \bullet (V_{TH} - 0.45)]$$

The precision range is based on a full scale of 0.18V to 1.2V. The 8-bit programming step size is 4mV. On the low range, threshold accuracy below 0.2V is not specified, but the thresholds are reachable.

The command byte for the voltage threshold can be calculated for the V2 to V6 precision range with the following equation:

$$\text{Command Byte} = \text{ROUND}\,[250 \bullet (V_{TH} - 0.18)]$$

Unused Channels

The user must connect all unused channel inputs to ground , program their configuration words (V*n*_CONFIG) to 0x01C0, and program their thresholds (V*n*_THR) to 0x0000 in order to avoid false faults.

Auxiliary Comparators

Two additional auxiliary comparators can be connected to the general purpose inputs with either their inverting or their noninverting input while the other input internally connects to a 0.5V reference voltage. These low offset, low drift comparators can be used for additional monitoring purposes.

If the tap point on an external resistive divider from an external voltage, V_{TRIP}, to GND (see Figure 2) connects to the auxiliary comparator input, the trip voltage is:

$$V_{TRIP} = 0.5V \bullet \left(1 + \frac{R1}{R2}\right)$$

In a negative voltage application (also shown in Figure 2) the resistive divider is connected between the negative voltage being sensed and V_{DD33}, and the trip voltage is:

$$V_{TRIP} = 0.5V - 2.8V \bullet \left(\frac{R3}{R4}\right)$$

The minimum value for R4 is limited by the V_{DD33} current sourcing capability at:

$$\frac{3.3V - 0.5V}{1mA} = 2.8k\Omega$$

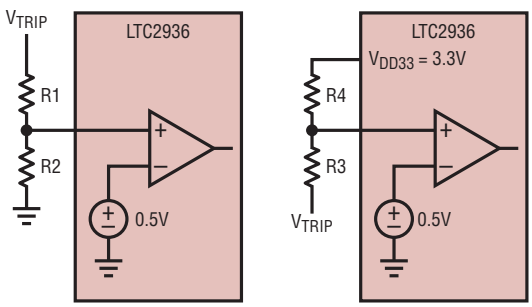


Figure 2. Auxiliary Comparator Usage

APPLICATIONS INFORMATION

Manual Reset

When a GPI*n* pin is configured as $\overline{MR}$, the input is active low. If GPI*n*_MR_RESPONSE = 1, the HISTORY_WORD register is cleared when $\overline{MR}$ is pulled low. An internal 15µA current source pulls $\overline{MR}$ to V_{DD33}. The $\overline{MR}$ input can also be mapped to a GPIO pin and combined with COMP*n*_HI and COMP*n*_LO faults to generate a system reset signal.

UV Disable

When a GPI*n* pin is configured as $\overline{UVDIS}$, the input is active low. When $\overline{UVDIS}$ is grounded, the LTC2936 does not respond to UV type faults. This feature is useful when power cycling the monitored supply. An internal 15µA current source pulls $\overline{UVDIS}$ to V_{DD33}.

Margin

When a GPI*n* pin is configured as $\overline{MARG}$, the input is active low. When $\overline{MARG}$ is grounded, the LTC2936 does not respond to any OV or UV faults. This feature is useful when margining the monitored supply. An internal 15µA current source pulls $\overline{MARG}$ to V_{DD33}.

Outputs

The GPIO*n* and CMP*n* outputs are open-drain, with an internal 15µA current source pulling to V_{DD33} (optional on the GPIO*n* outputs) and can tolerate a pull-up voltage up to 14V.

All faults, GPI*n,* or other GPIO*n* inputs mapped to a GPIO*n* output are combined with a logical OR function.

The GPIO*n* pins have programmable delay-on-release timing. The GPIO*n* pin asserts its active state immediately and de-asserts after the delay-on-release time has elapsed. Any fault causing a GPIO*n* pin to assert while its delay-on-release timer is active will reset the delay-on-release timer.

When a GPIO*n* indicates an alert, the alert may be cleared using the standard SMBus Alert Response Address (ARA) protocol. Alerts may also be cleared by reading (or clearing) HISTORY_WORD unless the condition causing the alert persists.

The CMP*n* outputs can be configured as non-latching (default) or latching. Latched CMP*n* outputs can be reset by asserting $\overline{MR}$ low or by issuing a CLEAR_HISTORY command. The CMP*n* outputs are active low.

Write Protect Features

When the WRITE_LOCK bit is set high, or a GPI*n* pin configured as $\overline{WP}$ is pulled low, all I^2C write word commands are ignored. This feature protects against accidental writing. The lock bit may still be written when the device is write-protected if the provided value for KEY matches the value in memory.

EEPROM

The user may save and restore configuration data to the operating memory registers at any time with STORE_USER and RESTORE_USER commands. Upon power-up, user-stored data is automatically loaded into the operating memory. The part ignores I^2C commands while performing EEPROM transactions.

Nondestructive operation above T_A = 85°C is possible, but may result in a slight degradation of the retention characteristics. The degradation in EEPROM retention for temperatures exceeding 85°C can be approximated by calculating the acceleration factor:

$$AF = e^{\left[\left(\frac{E_a}{k}\right)\bullet\left(\frac{1}{T_{USE}+273}-\frac{1}{T_{STRESS}+273}\right)\right]}$$

where:

AF = acceleration factor
E_a = activation energy = 1.5eV
$k = 8.617 \bullet 10^{-5}$ eV/°K
T_{USE} = 85°C maximum specified junction temperature
T_{STRESS} = actual junction temperature °C

Example: calculate effect on retention when operating at a junction temperature of 95°C for 10 hours.

T_{STRESS} = 95°C, T_{USE} = 85°C, AF = 3.74

So the overall retention of the EEPROM was degraded by 37.4 hours as a result of operation at a junction temperature of 95°C for 10 hours. Note that the effect of this overstress is negligible when compared to the overall EEPROM retention rating of 10 years (87,600 hours) at a temperature of 85°C.

APPLICATIONS INFORMATION

Negative Supply Power Monitor

Figure 3 illustrates how to configure the LTC2936 to monitor a negative supply rail. Assume the need to monitor the following supply rails: 1.5V, 3.3V, 5V and –5V, within a ±5% system specification.

Channels V1 and V2 are set to medium range, channel V3 is set to low range, channel V4 is set to precision range, and channels V5 and V6 are not used.

Select medium range for V1 and V2 (1V to 6V):

V1_THR_HI = ROUND[50 • (5 • 1.06 – 0.9)] = 220

V1_THR_LO = ROUND[50 • (5 • 0.94 – 0.9)] = 190

V2_THR_HI = ROUND[50 • (3.3 • 1.06 – 0.9)] = 130

V2_THR_LO = ROUND[50 • (3.3 • 0.94 – 0.9)] = 110

Select low range for V3 (0.5V to 3V):

V3_THR_HI = ROUND[100 • (1.5 • 1.06 –0.45)] = 114

V3_THR_LO = ROUND[100 • (1.5 • 0.94 –0.45)] = 96

To monitor –5V, use an external resistive divider connected between V_{DD33} and the negative rail. The voltage at V_{DD33} is 3.3V. In order to minimize the error introduced by the leakage current into the V4 input pin, the output of this divider is targeted to lie within the precision voltage range (0.2V to 1.2V). The OV and UV thresholds for the –5V rail are calculated as follows:

$$V5_{MIN} = \frac{(3.3 \bullet R1) - 1.05 \bullet (5 \bullet R2)}{R1 + R2} > 0.2V$$

$$V5_{MAX} = \frac{(3.3 \bullet R1) - 0.95 \bullet (5 \bullet R2)}{R1 + R2} < 1.2V$$

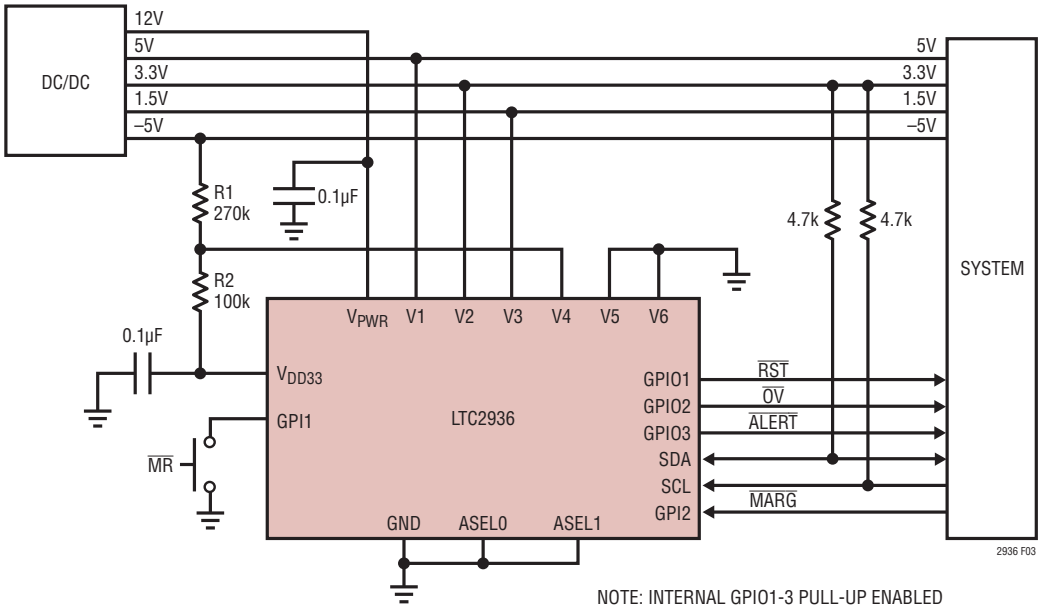


Figure 3. Negative Power Supply Monitor

APPLICATIONS INFORMATION

R1 = 270k ±0.1% and R2 = 100k ±0.1% satisfy the previous relationships. The programming codes can be calculated as shown in the following equations:

$$V4_{MIN} = \frac{(3.3 \cdot 0.98) \cdot (270 \cdot 0.999) - (1.05 \cdot 5) \cdot (100 \cdot 1.001)}{(270 \cdot 0.999) + (100 \cdot 1.001)} = 0.938V$$

$$V4_{MAX} = \frac{(3.3 \cdot 1.02) \cdot (270 \cdot 1.001) - (0.95 \cdot 5) \cdot (100 \cdot 0.999)}{(270 \cdot 1.001) + (100 \cdot 0.999)} = 1.176V$$

V4_THR_HI = ROUND[250 • (0.938 • 0.99 – 0.18)] = 187

V4_THR_LO = ROUND[250 • (1.176 • 1.01 – 0.18)] = 252

The normal polarities of the OV and UV comparators need to be swapped, since a drop of the negative supply below its specified absolute value increases $V4_{MAX}$ beyond its encoded threshold. An increase of the negative supply above its specified absolute value decreases $V4_{MIN}$ below its encoded threshold.

The GPIO*n* outputs are programmed as $\overline{RST}$ (active low system reset), $\overline{OV}$ (active low system OV) and $\overline{ALERT}$ (active low $\overline{ALERT}$, see SMBus specification). The UV comparators are mapped to GPIO1 and GPIO3. The OV comparators are mapped to GPIO2 and GPIO3. The GPI1 input is configured as $\overline{MR}$ (manual reset) and is mapped to GPIO1. The GPI2 input is configured as $\overline{MARG}$ (margin testing) allowing the system to disable OV and UV faults during margin testing.

APPLICATIONS INFORMATION

Five Supply Power-Up Sequencer

Figure 4 illustrates how to use the LTC2936 CMP*n* outputs to enable DC/DC converters sequentially, at power-up. The system is powered by a 12V source, which is also monitored.

The system starts-up when the pushbutton is pressed and the LTC2950-1 takes the RUN pin of the LTM4600 high. This forces the LTM4600 to generate 5V, which also supplies the other 4 DC/DC converters.

The LTC2936 is configured to monitor 5V on V1, 3.3V on V2, 2.5V on V3, –5V on V4, 1.8V on V5 and 12V on V6. When the programmed threshold is reached on V1, CMP1 pulls high, which enables the 3.3V converter. When the programmed threshold is reached on V2, CMP2 pulls high, which enables the 2.5V converter. When all converters have been enabled and power is good, CMP5 pulls high. GPIO1 is configured to pull high 6.4ms after CMP5.

If the $\overline{KILL}$ input of the LTC2950-1 is not forced high within 512ms of initial power-up, EN pulls low and the LTM4600 is powered down.

In the event that the external 12V supply drops below its programmed threshold, CMP6 and GPIO2 will pull low after 1.6ms. The LTC2950-1 then receives a logic low on the $\overline{KILL}$ input, which powers down the LTM4600 and the sequencing circuit.

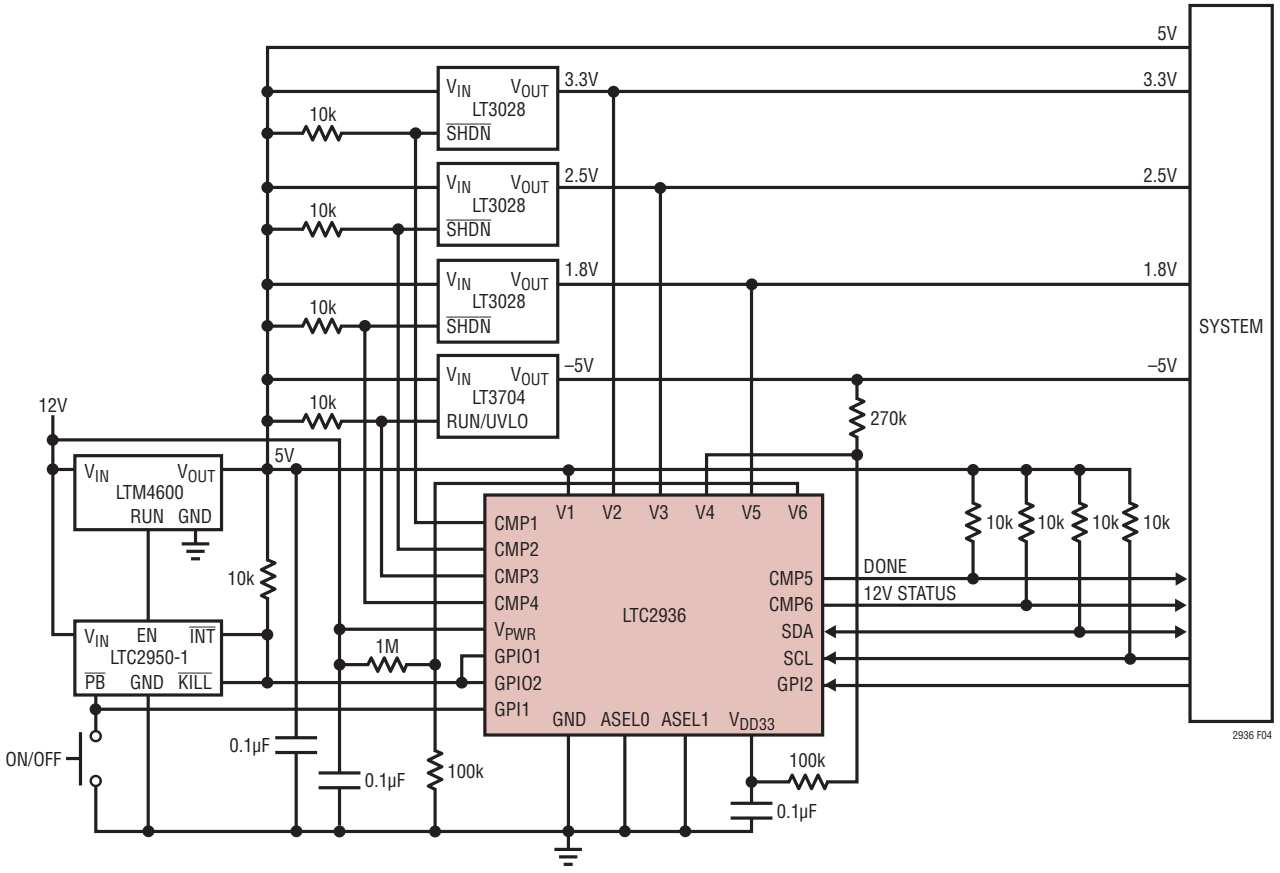


Figure 4. Five Supply Power-Up Sequencer

APPLICATIONS INFORMATION

Seven Power Supply Monitor

Figure 5 illustrates how to use the LTC2936 auxiliary comparators to expand power supply monitoring to seven channels. The system is powered by a 5V source, which is also monitored. The 9V rail can be monitored, in addition to the six input channels (5V, 3.3V, 2.5V, 1.8V, 1.5V and 24V), using an external resistive divider which feeds the OV and UV tap voltages to the auxiliary comparators on inputs GPI1 and GPI2.

Since the auxiliary comparators' thresholds are fixed at 0.5V ±10mV, to monitor a 9V ±10% power supply, the following equations apply:

$$\frac{R2+R3}{R1+R2+R3}=\frac{0.51V}{0.9\bullet 9V}$$

$$\frac{R3}{R1+R2+R3}=\frac{0.49V}{1.1\bullet 9V}$$

For R3 = 8.87k, the equations yield: R2 = 2.4k and R1 = 168k.

The GPI1 comparator monitors the UV limit and is programmed for negative polarity. The GPI2 comparator monitors the OV limit and is programmed for positive polarity.

A second resistive divider is used to divide the 24V rail voltage down to 1.08V, in order to use the low leakage, low range of the V6 channel.

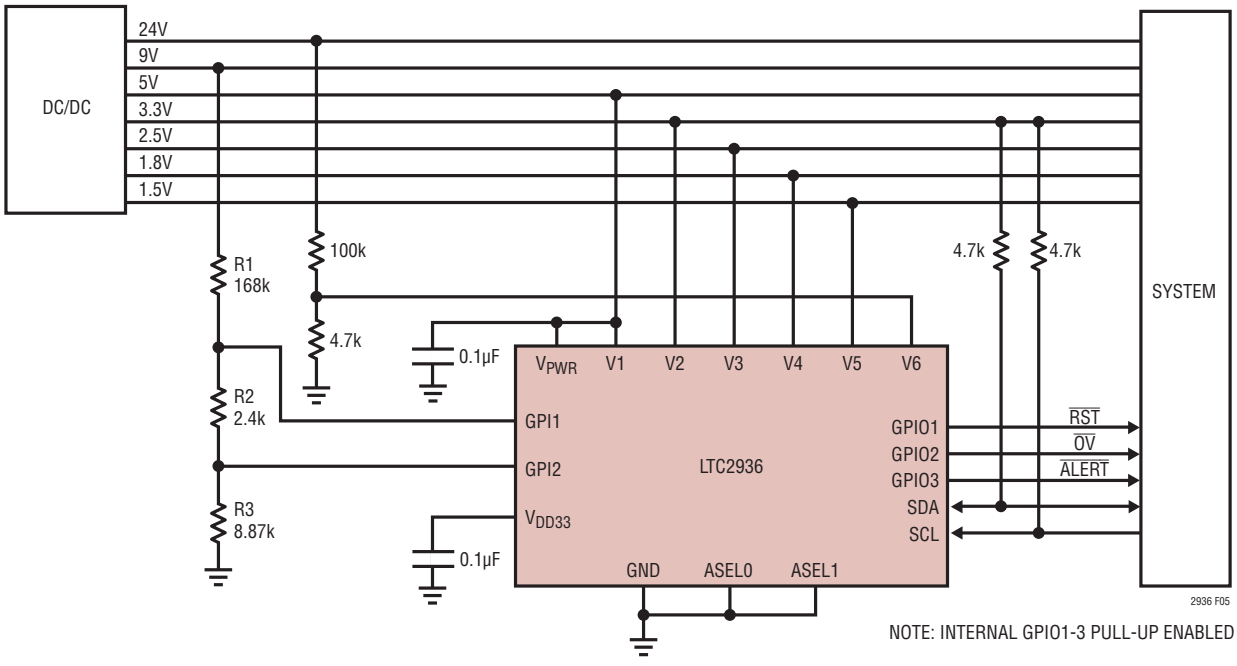
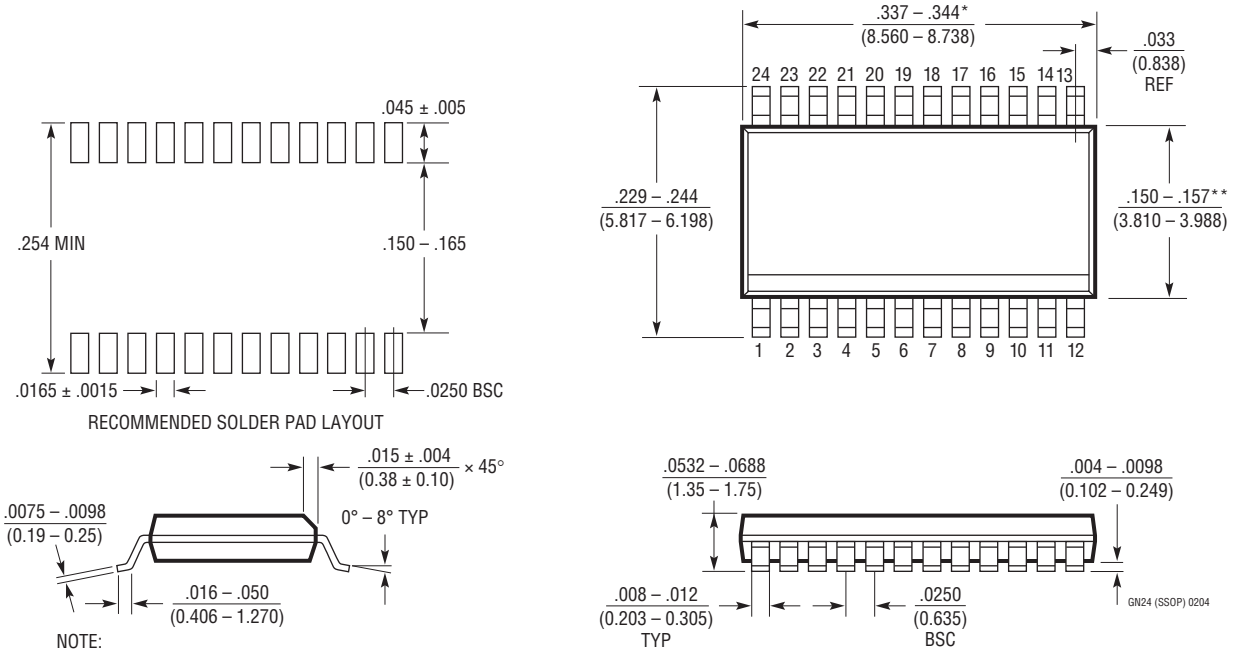


Figure 5. Seven Power Supply Monitor

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC2936#packaging for the most recent package drawings.

GN Package
24-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{(\text{MILLIMETERS})}$
3. DRAWING NOT TO SCALE

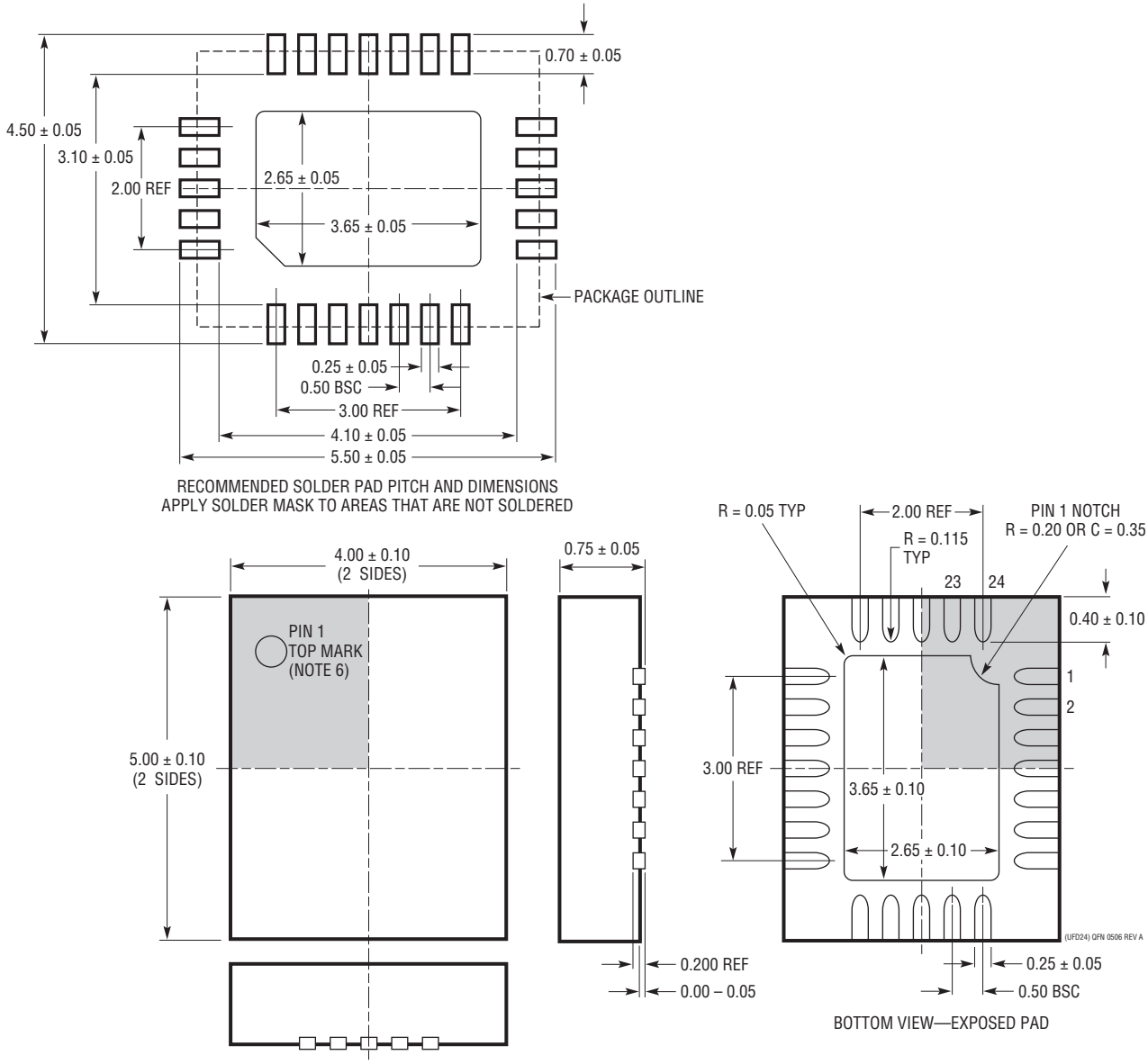
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/product/LTC2936#packaging for the most recent package drawings.

UFD Package
24-Lead Plastic QFN (4mm × 5mm)
(Reference LTC DWG # 05-08-1696 Rev A)



NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	0117	Added 4.7k pull-ups in Figure 3.	23