Isolated Flyback Converter without an Opto-Coupler

FEATURES

- **3V to 40V Input Voltage Range**
- **2.5A, 60V Integrated NPN Power Switch**
- **Boundary Mode Operation**
- **No Transformer Third Winding or Optoisolator Required for Regulation**
- **Improved Primary-Side Winding Feedback Load Regulation**
- V_{OUT} Set with Two External Resistors
- BIAS Pin for Internal Bias Supply and Power NPN Driver
- Programmable Soft-Start
- Programmable Power Switch Current Limit
- Thermally Enhanced 16-Lead TSSOP

APPLICATIONS

- Industrial, Automotive and Medical Isolated Power Supplies

DESCRIPTION

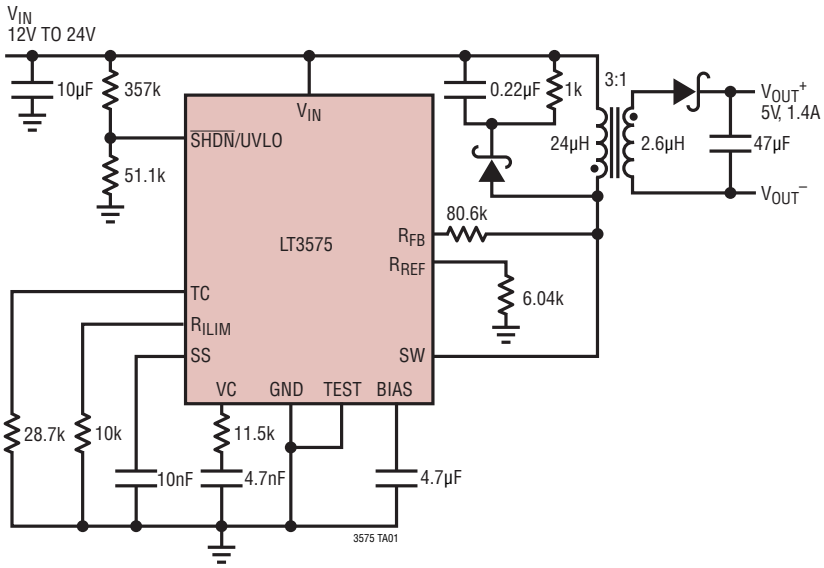
The LT®3575 is a monolithic switching regulator specifically designed for the isolated flyback topology. No third winding or optoisolator is required for regulation. The part senses the isolated output voltage directly from the primary side flyback waveform. A 2.5A, 60V NPN power switch is integrated along with all control logic into a 16-lead TSSOP package.

The LT3575 operates with input supply voltages from 3V to 40V, and can deliver output power up to 14W with no external power switch.The LT3575 utilizes boundary mode operation to provide a small magnetic solution with improved load regulation.

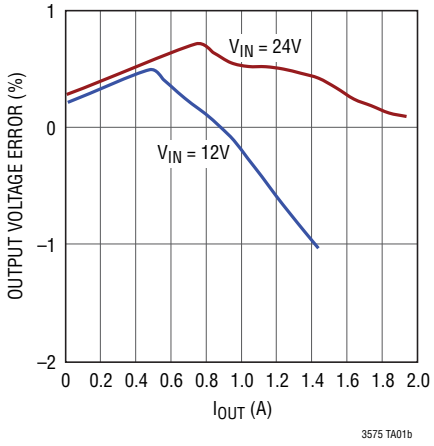
The output voltage is easily set with two external resistors and the transformer turns ratio. Off the shelf transformers are available for many applications.

TYPICAL APPLICATION

5V Isolated Flyback Converter



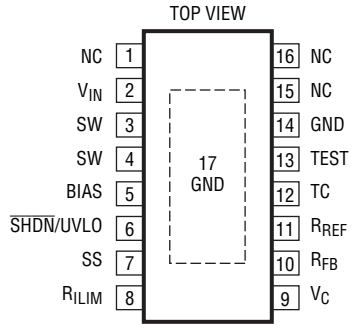
Load Regulation



ABSOLUTE MAXIMUM RATINGS

SW 60V
V_{IN}, $\overline{SHDN}$/UVLO, R_{FB}, BIAS 40V
SS, V_C, TC, R_{REF}, R_{ILIM} 5V
Maximum Junction Temperature ..... 125°C
Operating Junction Temperature Range (Note 2)
LT3575E, LT3575I.....–40°C to 125°C
Storage Temperature Range .....–65°C to 150°C

PIN CONFIGURATION



FE PACKAGE
16-LEAD PLASTIC TSSOP

T_{JMAX} = 125°C, θ_{JA} = 38°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE CONNECTED TO GND

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3575EFE#PBF	LT3575EFE#TRPBF	3575FE	16-Lead Plastic TSSOP	–40°C to 125°C
LT3575IFE#PBF	LT3575IFE#TRPBF	3575FE	16-Lead Plastic TSSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range		●	3		40	V
Quiescent Current	SS = 0V $V_{\overline{SHDN}/UVLO}$ = 0V			4.5 0	 1	mA µA
Soft-Start Current	SS = 0.4V			7		µA
$\overline{SHDN}$/UVLO Pin Threshold	UVLO Pin Voltage Rising	●	1.15	1.22	1.32	V
$\overline{SHDN}$/UVLO Pin Hysteresis Current	V_{UVLO} = 1V		2.2	2.8	3.2	µA
Soft-Start Threshold				0.7		V
Maximum Switching Frequency				1000		kHz
Switch Current Limit	R_{ILIM} = 10k		2.8	3.5	4.2	A
Minimum Current Limit	V_C = 0V			400		mA
Switch V_{CESAT}	I_{SW} = 0.5A			75	125	mV
R_{REF} Voltage	V_{IN} = 3V	 ●	1.21 1.20	1.23	1.25 1.26	V
R_{REF} Voltage Line Regulation	3V < V_{IN} < 40V			0.01	0.03	%/V
R_{REF} Pin Bias Current	(Note 3)	●		100	600	nA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{REF} Reference Current	Measured at R_{FB} Pin with R_{REF} = 6.49k			190		µA
Error Amplifier Voltage Gain	V_{IN} = 3V			150		V/V
Error Amplifier Transconductance	ΔI = 10µA, V_{IN} = 3V			150		µmhos
Minimum Switching Frequency	V_C = 0.35V			40		kHz
TC Current into R_{REF}	R_{TC} = 20.1k			27.5		µA
BIAS Pin Voltage	I_{BIAS} = 30mA		2.9	3	3.1	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

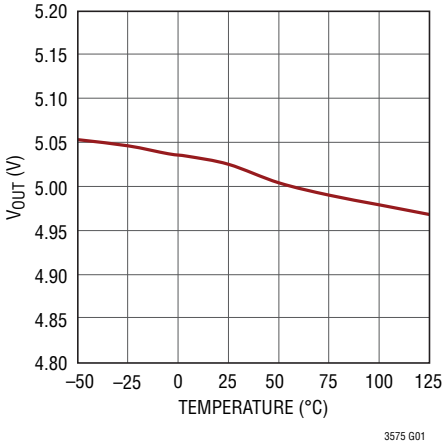
Note 2: The LT3575E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design characterization and correlation with statistical process controls. The LT3575I is guaranteed over the full –40°C to 125°C operating junction temperature range.

Note 3: Current flows out of the R_{REF} pin.

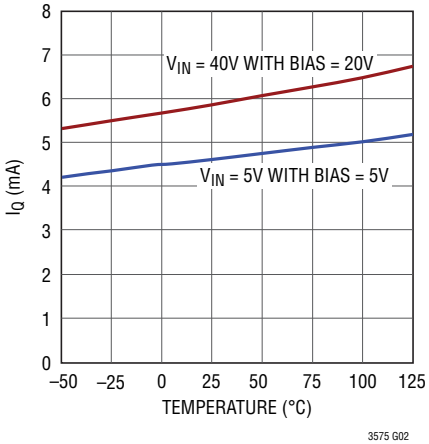
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

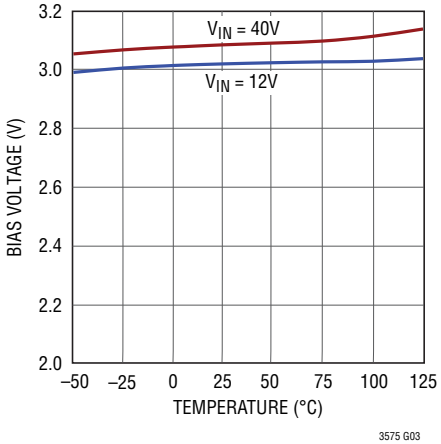
Output Voltage



Quiescent Current

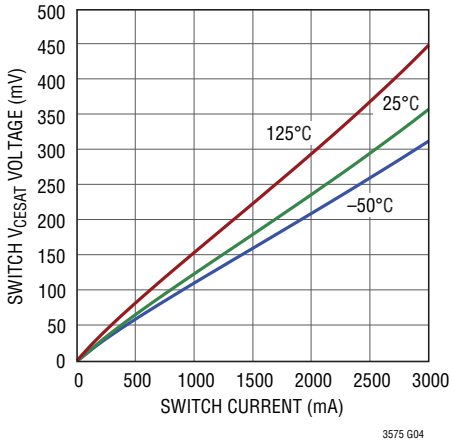


Bias Pin Voltage

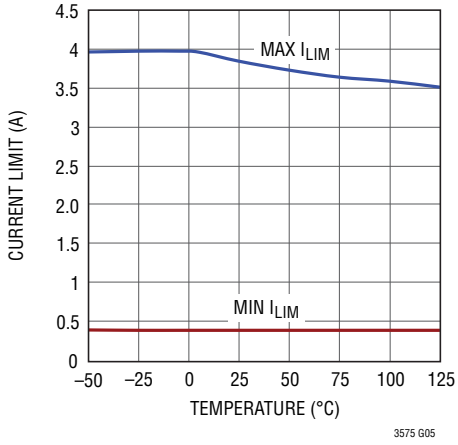


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

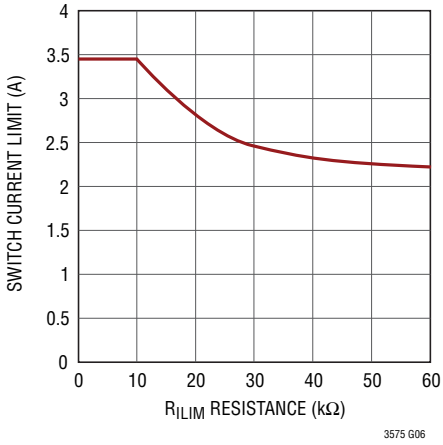
Switch Saturation Voltage



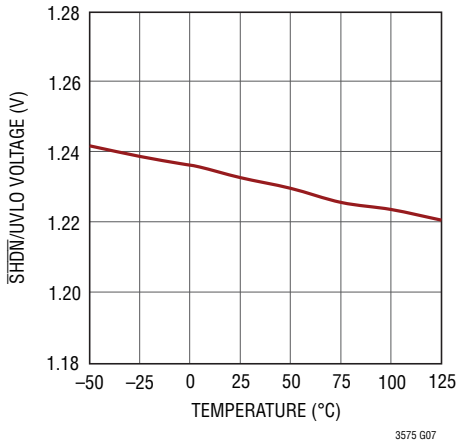
Switch Current Limit



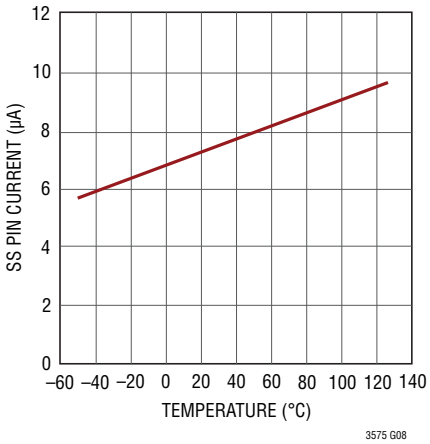
Switch Current Limit vs R_{ILIM}



$\overline{SHDN}$/UVLO Falling Threshold



SS Pin Current



PIN FUNCTIONS

NC (Pins 1, 15, 16): No Connect Pins. Can be left open or connected to any ground plane.

V_{IN} (Pin 2): Input Voltage. This pin supplies current to the internal start-up circuitry and as a reference voltage for the DCM comparator and feedback circuitry. This pin must be locally bypassed with a capacitor.

SW (Pins 3, 4): Collector Node of the Output Switch. This pin has large currents flowing through it. Keep the traces to the switching components as short as possible to minimize electromagnetic radiation and voltage spikes.

BIAS (Pin 5): Bias Voltage. This pin supplies current to the switch driver and internal circuitry of the LT3575. This pin must be locally bypassed with a capacitor. This pin may also be connected to V_{IN} if a third winding is not used and if $V_{IN} \leq 15V$. If a third winding is used, the BIAS voltage should be lower than the input voltage for proper operation.

$\overline{SHDN}$/UVLO (Pin 6): Shutdown/Undervoltage Lockout. A resistor divider connected to V_{IN} is tied to this pin to program the minimum input voltage at which the LT3575 will operate. At a voltage below ~0.7V, the part draws no quiescent current. When below 1.22V and above ~0.7V, the part will draw 7µA of current, but internal circuitry will remain off. Above 1.22V, the internal circuitry will start and a 7µA current will be fed into the SS pin. When this pin falls below 1.22V, 2.8µA will be pulled from the pin to provide programmable hysteresis for UVLO.

SS (Pin 7): Soft-Start Pin. Place a soft-start capacitor here to limit start-up inrush current and output voltage ramp rate. Switching starts when the voltage at this pin reaches ~0.7V.

R_{ILIM} (Pin 8): Maximum Current Limit Adjust Pin. A resistor should be tied to this pin to ground to set the current limit. Use a 10k resistor for the full current capabilities of the switch.

V_C (Pin 9): Compensation Pin for Internal Error Amplifier. Connect a series RC from this pin to ground to compensate the switching regulator. A 100pF capacitor in parallel helps eliminate noise.

R_{FB} (Pin 10): Input Pin for External Feedback Resistor. This pin is connected to the transformer primary (V_{SW}). The ratio of this resistor to the R_{REF} resistor, times the internal bandgap reference, determines the output voltage (plus the effect of any non-unity transformer turns ratio). The average current through this resistor during the flyback period should be approximately 200µA. For nonisolated applications, this pin should be connected to V_{IN}.

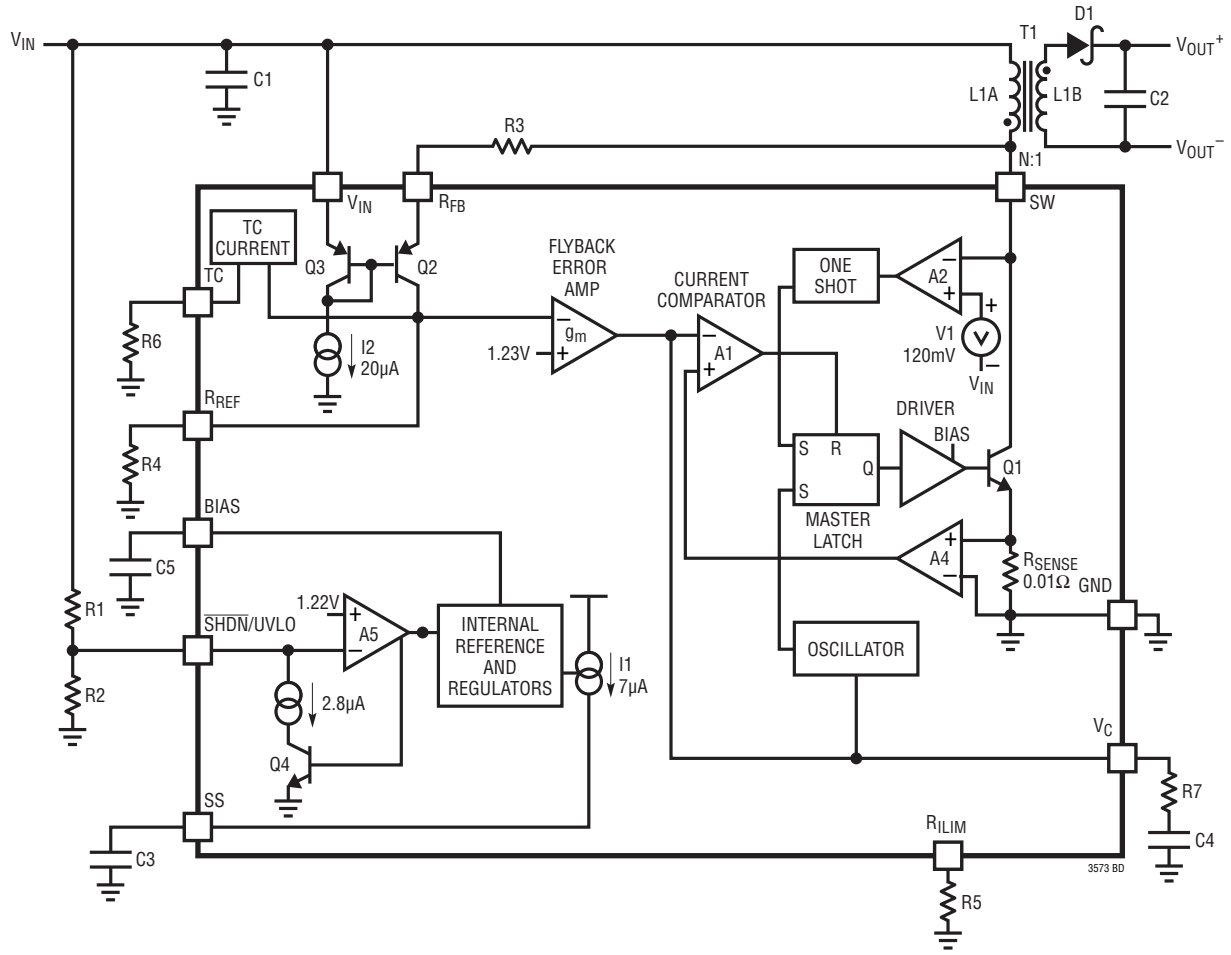
R_{REF} (Pin 11): Input Pin for External Ground-Referred Reference Resistor. This resistor should be in the range of 6k, but for convenience, need not be precisely this value. For nonisolated applications, a traditional resistor voltage divider may be connected to this pin.

TC (Pin 12): Output Voltage Temperature Compensation. Connect a resistor to ground to produce a current proportional to absolute temperature to be sourced into the R_{REF} node. $I_{TC} = 0.55V/R_{TC}$.

TEST (Pin 13): This pin is used for testing purposes only and must be connected to ground for the part to operate properly.

GND (Pin 14, Exposed Pad Pin 17): Ground. The exposed pad of the package provides both electrical contact to ground and good thermal contact to the printed circuit board. The exposed pad must be soldered to the circuit board for proper operation and should be well connected with many vias to an internal ground plane.

BLOCK DIAGRAM



OPERATION

The LT3575 is a current mode switching regulator IC designed specifically for the isolated flyback topology. The special problem normally encountered in such circuits is that information relating to the output voltage on the isolated secondary side of the transformer must be communicated to the primary side in order to maintain regulation. Historically, this has been done with optoisolators or extra transformer windings. Optoisolator circuits waste output power and the extra components increase the cost and physical size of the power supply. Optoisolators can also exhibit trouble due to limited dynamic response, nonlinearity, unit-to-unit variation and aging over life. Circuits employing extra transformer windings also exhibit deficiencies. Using an extra winding adds to the transformer's physical size and cost, and dynamic response is often mediocre.

The LT3575 derives its information about the isolated output voltage by examining the primary side flyback pulse waveform. In this manner, no optoisolator nor extra transformer winding is required for regulation. The output voltage is easily programmed with two resistors. Since this IC operates in boundary control mode, the output voltage is calculated from the switch pin when the secondary current is almost zero. This method improves load regulation without external resistors and capacitors.

The Block Diagram shows an overall view of the system. Many of the blocks are similar to those found in traditional switching regulators including: internal bias regulator, oscillator, logic, current amplifier and comparator, driver, and output switch. The novel sections include a special flyback error amplifier and a temperature compensation circuit. In addition, the logic system contains additional logic for boundary mode operation, and the sampling error amplifier.

The LT3575 features a boundary mode control method, where the part operates at the boundary between continuous conduction mode and discontinuous conduction mode. The V_C pin controls the current level just as it does in normal current mode operation, but instead of turning the switch on at the start of the oscillator period, the part detects when the secondary side winding current is zero.

Boundary Mode Operation

Boundary mode is a variable frequency, current-mode switching scheme. The switch turns on and the inductor current increases until a V_C pin controlled current limit. The voltage on the SW pin rises to the output voltage divided by the secondary-to-primary transformer turns ratio plus the input voltage. When the secondary current through the diode falls to zero, the SW pin voltage falls below V_{IN}. A discontinuous conduction mode (DCM) comparator detects this event and turns the switch back on.

Boundary mode returns the secondary current to zero every cycle, so the parasitic resistive voltage drops do not cause load regulation errors. Boundary mode also allows the use of a smaller transformer compared to continuous conduction mode and no subharmonic oscillation.

At low output currents the LT3575 delays turning on the switch, and thus operates in discontinuous mode. Unlike a traditional flyback converter, the switch has to turn on to update the output voltage information. Below 0.6V on the V_C pin, the current comparator level decreases to its minimum value, and the internal oscillator frequency decreases in frequency. With the decrease of the internal oscillator, the part starts to operate in DCM. The output current is able to decrease while still allowing a minimum switch off-time for the error amp sampling circuitry. The typical minimum internal oscillator frequency with V_C equal to 0V is 40kHz.

APPLICATIONS INFORMATION

ERROR AMPLIFIER—PSEUDO DC THEORY

In the Block Diagram, the R_{REF} (R4) and R_{FB} (R3) resistors can be found. They are external resistors used to program the output voltage. The LT3575 operates much the same way as traditional current mode switchers, the major difference being a different type of error amplifier which derives its feedback information from the flyback pulse.

Operation is as follows: when the output switch, Q1, turns off, its collector voltage rises above the V_{IN} rail. The amplitude of this flyback pulse, i.e., the difference between it and V_{IN}, is given as:

$V_{FLBK} = (V_{OUT} + V_F + I_{SEC} \bullet ESR) \bullet N_{PS}$

V_F = D1 forward voltage

I_{SEC} = Transformer secondary current

ESR = Total impedance of secondary circuit

N_{PS} = Transformer effective primary-to-secondary turns ratio

The flyback voltage is then converted to a current by the action of R_{FB} and Q2. Nearly all of this current flows through resistor R_{REF} to form a ground-referred voltage. This voltage is fed into the flyback error amplifier. The flyback error amplifier samples this output voltage information when the secondary side winding current is zero. The error amplifier uses a bandgap voltage, 1.23V, as the reference voltage.

The relatively high gain in the overall loop will then cause the voltage at the R_{REF} resistor to be nearly equal to the bandgap reference voltage V_{BG}. The relationship between V_{FLBK} and V_{BG} may then be expressed as:

$$\alpha\left(\frac{V_{FLBK}}{R_{FB}}\right) = \frac{V_{BG}}{R_{REF}} \quad \text{or,}$$

$$V_{FLBK} = V_{BG}\left(\frac{R_{FB}}{R_{REF}}\right)\left(\frac{1}{\alpha}\right)$$

α = Ratio of Q1 I_C to I_E, typically ≈ 0.986

V_{BG} = Internal bandgap reference

In combination with the previous V_{FLBK} expression yields an expression for V_{OUT}, in terms of the internal reference, programming resistors, transformer turns ratio and diode forward voltage drop:

$$V_{OUT} = V_{BG}\left(\frac{R_{FB}}{R_{REF}}\right)\left(\frac{1}{\alpha\, N_{PS}}\right) - V_F - I_{SEC}\,(ESR)$$

Additionally, it includes the effect of nonzero secondary output impedance (ESR). This term can be assumed to be zero in boundary control mode. More details will be discussed in the next section.

Temperature Compensation

The first term in the V_{OUT} equation does not have a temperature dependence, but the diode forward drop has a significant negative temperature coefficient. To compensate for this, a positive temperature coefficient current source is connected to the R_{REF} pin. The current is set by a resistor to ground connected to the TC pin. To cancel the temperature coefficient, the following equation is used:

$$\frac{\delta V_F}{\delta T} = -\frac{R_{FB}}{R_{TC}} \bullet \frac{1}{N_{PS}} \bullet \frac{\delta V_{TC}}{\delta T} \quad \text{or,}$$

$$R_{TC} = \frac{-R_{FB}}{N_{PS}} \bullet \frac{1}{\delta V_F / \delta T} \bullet \frac{\delta V_{TC}}{\delta T} \approx \frac{R_{FB}}{N_{PS}}$$

$(\delta V_F/\delta_T)$ = Diode's forward voltage temperature coefficient

$(\delta V_{TC}/\delta T) = 2mV$

$V_{TC} = 0.55V$

The resistor value given by this equation should also be verified experimentally, and adjusted if necessary to achieve optimal regulation overtemperature.

The revised output voltage is as follows:

$$V_{OUT} = V_{BG}\left(\frac{R_{FB}}{R_{REF}}\right)\left(\frac{1}{N_{PS}\,\alpha}\right) - V_F - \left(\frac{V_{TC}}{R_{TC}}\right) \bullet \frac{R_{FB}}{N_{PS}\,\alpha} - I_{SEC}\,(ESR)$$

APPLICATIONS INFORMATION

ERROR AMPLIFIER—DYNAMIC THEORY

Due to the sampling nature of the feedback loop, there are several timing signals and other constraints that are required for proper LT3575 operation.

Minimum Current Limit

The LT3575 obtains output voltage information from the SW pin when the secondary winding conducts current. The sampling circuitry needs a minimum amount of time to sample the output voltage. To guarantee enough time, a minimum inductance value must be maintained. The primary side magnetizing inductance must be chosen above the following value:

$$L_{PRI} \geq V_{OUT} \bullet \frac{t_{MIN}}{I_{MIN}} \bullet N_{PS} = V_{OUT} \bullet N_{PS} \bullet \left(\frac{0.88\mu H}{V}\right)$$

t_{MIN} = minimum off-time, 350ns

I_{MIN} = minimum current limit, 400mA

The minimum current limit is higher than that on the Electrical Characteristics table due to the overshoot caused by the comparator delay.

Leakage Inductance Blanking

When the output switch first turns off, the flyback pulse appears. However, it takes a finite time until the transformer primary side voltage waveform approximately represents the output voltage. This is partly due to the rise time on the SW node, but more importantly due to the transformer leakage inductance. The latter causes a very fast voltage spike on the primary side of the transformer that is not directly related to output voltage (some time is also required for internal settling of the feedback amplifier circuitry). The leakage inductance spike is largest when the power switch current is highest.

In order to maintain immunity to these phenomena, a fixed delay is introduced between the switch turn-off command and the beginning of the sampling. The blanking is internally set to 150ns. In certain cases, the leakage inductance may not be settled by the end of the blanking period, but will not significantly affect output regulation.

Selecting R_{FB} and R_{REF} Resistor Values

The expression for V_{OUT}, developed in the Operation section, can be rearranged to yield the following expression for R_{FB}:

$$R_{FB} = \frac{R_{REF} \bullet N_{PS}\left[(V_{OUT} + V_F)\alpha + V_{TC}\right]}{V_{BG}}$$

where,

V_{OUT} = Output voltage

V_F = Switching diode forward voltage

α = Ratio of Q1, IC to IE, typically 0.986

N_{PS} = Effective primary-to-secondary turns ratio

V_{TC} = 0.55V

The equation assumes the temperature coefficients of the diode and V_{TC} are equal, which is a good first-order approximation.

Strictly speaking, the above equation defines R_{FB} not as an absolute value, but as a ratio of R_{REF}. So, the next question is, "What is the proper value for R_{REF}?" The answer is that R_{REF} should be approximately 6.04k. The LT3575 is trimmed and specified using this value of R_{REF}. If the impedance of R_{REF} varies considerably from 6.04k, additional errors will result. However, a variation in R_{REF} of several percent is acceptable. This yields a bit of freedom in selecting standard 1% resistor values to yield nominal R_{FB}/R_{REF} ratios. The R_{FB} resistor given by this equation should also be verified experimentally, and adjusted if necessary for best output accuracy.

Tables 1-4 are useful for selecting the resistor values for R_{REF} and R_{FB} with no equations. The tables provide R_{FB}, R_{REF} and R_{TC} values for common output voltages and common winding ratios.

Table 1. Common Resistor Values for 1:1 Transformers

V_{OUT} (V)	N_{PS}	R_{FB} (kΩ)	R_{REF} (kΩ)	R_{TC} (kΩ)
3.3	1.00	18.7	6.04	19.1
5	1.00	27.4	6.04	28
12	1.00	64.9	6.04	66.5
15	1.00	80.6	6.04	80.6
20	1.00	107	6.04	105

APPLICATIONS INFORMATION

Table 2. Common Resistor Values for 2:1 Transformers

V_{OUT} (V)	N_{PS}	R_{FB} (kΩ)	R_{REF} (kΩ)	R_{TC} (kΩ)
3.3	2.00	37.4	6.04	18.7
5	2.00	56	6.04	28
12	2.00	130	6.04	66.5
15	2.00	162	6.04	80.6

Table 3. Common Resistor Values for 3:1 Transformers

V_{OUT} (V)	N_{PS}	R_{FB} (kΩ)	R_{REF} (kΩ)	R_{TC} (kΩ)
3.3	3.00	56.2	6.04	20
5	3.00	80.6	6.04	28.7
10	3.00	165	6.04	54.9

Table 4. Common Resistor Values for 4:1 Transformers

V_{OUT} (V)	N_{PS}	R_{FB} (kΩ)	R_{REF} (kΩ)	R_{TC} (kΩ)
3.3	4.00	76.8	6.04	19.1
5	4.00	113	6.04	28

Output Power

A flyback converter has a complicated relationship between the input and output current compared to a buck or a boost. A boost has a relatively constant maximum input current regardless of input voltage and a buck has a relatively constant maximum output current regardless of input voltage. This is due to the continuous nonswitching behavior of the two currents. A flyback converter has both discontinuous input and output currents which makes it similar to a nonisolated buck-boost. The duty cycle will affect the input and output currents, making it hard to predict output power. In addition, the winding ratio can be changed to multiply the output current at the expense of a higher switch voltage.

The graphs in Figures 1-3 show the maximum output power possible for the output voltages 3.3V, 5V, and 12V. The maximum power output curve is the calculated output power if the switch voltage is 50V during the off-time. To achieve this power level at a given input, a winding ratio value must be calculated to stress the switch to 50V, resulting in some odd ratio values. The curves below are examples of common winding ratio values and the amount of output power at given input voltages.

One design example would be a 5V output converter with a minimum input voltage of 20V and a maximum input voltage of 30V. A three-to-one winding ratio fits this design example perfectly and outputs close to ten watts at 30V but lowers to eight watts at 20V.

TRANSFORMER DESIGN CONSIDERATIONS

Transformer specification and design is perhaps the most critical part of successfully applying the LT3575. In addition to the usual list of caveats dealing with high frequency isolated power supply transformer design, the following information should be carefully considered.

Linear Technology has worked with several leading magnetic component manufacturers to produce pre-designed flyback transformers for use with the LT3575. Table 5 shows the details of several of these transformers.

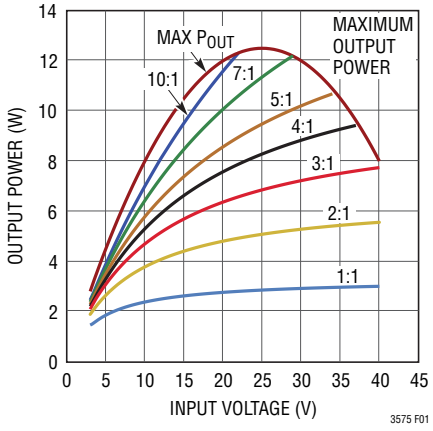


Figure 1. Output Power for 3.3V Output

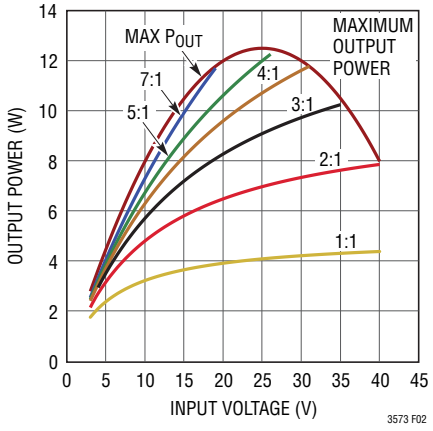


Figure 2. Output Power for 5V Output

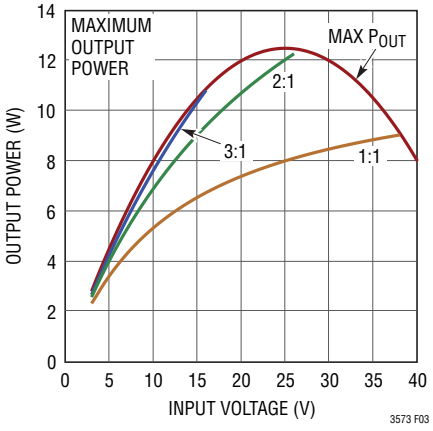


Figure 3. Output Power for 12V Output

APPLICATIONS INFORMATION

Table 5. Predesigned Transformers—Typical Specifications, Unless Otherwise Noted

TRANSFORMER PART NUMBER	DIMENSION (W × L × H) (mm)	L_{PRI} (µH)	$L_{LEAKAGE}$ (nH)	N_P:N_S	R_{PRI} (mΩ)	R_{SEC} (mΩ)	VENDOR	TARGET APPLICATION*	
								V_O (V)	I_O (A)
750311306	15.24 × 13.3 × 11.43	100	1750	3:1	285	46	Würth Elektronik	12	1
750311307	15.24 × 13.3 × 11.43	100	2000	2:1	290	104	Würth Elektronik	24	0.5
750311308	15.24 × 13.3 × 11.43	100	2100	1:1	325	480	Würth Elektronik	24	0.5
750310564	15.24 × 13.3 × 11.43	63	450	3:1	115	50	Würth Elektronik	±5	1
750311303	15.24 × 13.3 × 11.43	50	800	5:1	106	13	Würth Elektronik	5	3
750311304	15.24 × 13.3 × 11.43	50	800	4:1	146	17	Würth Elektronik	5	3
750311305	15.24 × 13.3 × 11.43	50	1200	3:1	175	28	Würth Elektronik	12	1
PA2627NL	15.24 × 13.3 × 11.43	50	766	3:1	420	44	Pulse Engineering	3.3	3
750310471	15.24 × 13.3 × 11.43	25	350	3:1	57	11	Würth Elektronik	5	2
750310562	15.24 × 13.3 × 11.43	25	330	2:1	60	20	Würth Elektronik	12	0.8
750310563	15.24 × 13.3 × 11.43	25	325	1:1	60	60	Würth Elektronik	12	0.8
PA2364NL	15.24 × 13.3 × 11.43	25	1000	7:1	125	5.6	Pulse Engineering	3.3	1.5
PA2363NL	15.24 × 13.3 × 11.43	25	850	5:1	117	7.5	Pulse Engineering	5	1
PA2362NL	15.24 × 13.3 × 11.43	24	550	4:1	117	9.5	Pulse Engineering	3.3	1.5
PA2454NL	15.24 × 13.3 × 11.43	24	430	3:1	82	11	Pulse Engineering	5	1
PA2455NL	15.24 × 13.3 × 11.43	25	450	2:1	82	22	Pulse Engineering	12	0.5
PA2456NL	15.24 × 13.3 × 11.43	25	390	1:1	82	84	Pulse Engineering	12	0.3
750310559	15.24 × 13.3 × 11.43	24	400	4:1	51	16	Würth Elektronik	3.3	1.5
750311675	15.24 × 13.3 × 11.43	25	130	3:1	51	11	Würth Elektronik	5	2
750311342	15.24 × 13.3 × 11.43	15	440	2:1	85	22	Würth Elektronik	5	1.5
750311567	15.24 × 13.3 × 11.43	8	425	2:1	53	22	Würth Elektronik	5	2
750311422	17.7 × 14.0 × 12.7	50	574	5:1	80	8	Würth Elektronik	3.3	4
750311423	17.7 × 14.0 × 12.7	50	570	4:1	90	12	Würth Elektronik	5	2.4
750311457	17.7 × 14.0 × 12.7	50	600	4:1	115	12	Würth Elektronik	5	2.4
750311688	17.7 × 14.0 × 12.7	50	600	5:1	80	8	Würth Elektronik	3.3	4
750311689	17.7 × 14.0 × 12.7	50	600	4:1	115	12	Würth Elektronik	5	2.4
750311439	17.7 × 14.0 × 12.7	37	750	2:1	89	28	Würth Elektronik	12	1
PA2467NL	17.7 × 14.0 × 12.7	37	750	2:1	89	28	Pulse Engineering	12	1
PA2466NL	17.7 × 14.0 × 12.7	37	750	6:1	89	4.6	Pulse Engineering	3.3	4
PA2369NL	17.7 × 14.0 × 12.7	37	750	5:1	89	6.2	Pulse Engineering	5	2.5
750311458	17.7 × 14.0 × 12.7	15	175	3:1	35	6	Würth Elektronik	3.3	4
750311625	17.7 × 14.0 × 12.7	9	350	4:1	43	6	Würth Elektronik	3.3	4
750311564	17.7 × 14.0 × 12.7	9	120	3:1	36	7	Würth Elektronik	5	2.5
750311624	17.7 × 14.0 × 12.7	9	180	3:2	34	21	Würth Elektronik	15	1

*Target applications, not guaranteed

APPLICATIONS INFORMATION

Turns Ratio

Note that when using an R_{FB}/R_{REF} resistor ratio to set output voltage, the user has relative freedom in selecting a transformer turns ratio to suit a given application.In contrast, simpler ratios of small integers, e.g., 1:1, 2:1, 3:2, etc., can be employed to provide more freedom in setting total turns and mutual inductance.

Typically, the transformer turns ratio is chosen to maximize available output power. For low output voltages (3.3V or 5V), a N:1 turns ratio can be used with multiple primary windings relative to the secondary to maximize the transformer's current gain (and output power). However, remember that the SW pin sees a voltage that is equal to the maximum input supply voltage plus the output voltage multiplied by the turns ratio. This quantity needs to remain below the ABS MAX rating of the SW pin to prevent breakdown of the internal power switch. Together these conditions place an upper limit on the turns ratio, N, for a given application. Choose a turns ratio low enough to ensure:

$$N < \frac{50V - V_{IN(MAX)}}{V_{OUT} + V_F}$$

For larger N:1 values, a transformer with a larger physical size is needed to deliver additional current and provide a large enough inductance value to ensure that the off-time is long enough to accurately measure the output voltage.

For lower output power levels, a 1:1 or 1:N transformer can be chosen for the absolute smallest transformer size. A 1:N transformer will minimize the magnetizing inductance (and minimize size), but will also limit the available output power. A higher 1:N turns ratio makes it possible to have very high output voltages without exceeding the breakdown voltage of the internal power switch.

Leakage Inductance

Transformer leakage inductance (on either the primary or secondary) causes a voltage spike to appear at the primary after the output switch turns off. This spike is increasingly prominent at higher load currents where more stored energy must be dissipated. In most cases, a snubber circuit will be required to avoid overvoltage breakdown at the output switch node. Transformer leakage inductance should be minimized.

An RCD (resistor capacitor diode) clamp, shown in Figure 4, is required for most designs to prevent the leakage inductance spike from exceeding the breakdown voltage of the power device. The flyback waveform is depicted in Figure 5. In most applications, there will be a very fast voltage spike caused by a slow clamp diode that may not exceed 60V. Once the diode clamps, the leakage inductance current is absorbed by the clamp capacitor. This period should not last longer than 150ns so as not to interfere with the output regulation, and the voltage during this clamp period must not exceed 55V. The clamp diode turns off after the leakage inductance energy is absorbed and the switch voltage is then equal to:

$$V_{SW(MAX)} = V_{IN(MAX)} + N(V_{OUT} + V_F)$$

This voltage must not exceed 50V. This same equation also determines the maximum turns ratio.

When choosing the snubber network diode, careful attention must be paid to maximum voltage seen by the SW pin. Schottky diodes are typically the best choice to be used in the snubber, but some PN diodes can be used if they turn on fast enough to limit the leakage inductance spike. The leakage spike must always be kept below 60V. Figures 6 and 7 show the SW pin waveform for a $24V_{IN}$, $5V_{OUT}$ application at a 1A load current. Notice that the leakage spike is very high (more than 65V) with the "bad" diode, while the "good" diode effectively limits the spike to less than 55V.

An alternative to RC network is a Zener diode clamping. The Zener diode must be able to handle the voltage rating and power dissipating during the switch turn-off time. Application Note 19 has more details on Zener diode snubber design for flyback converters.

For applications with SW voltage exceeding 50V, Zener diode clamp must be considered. At higher operating primary current, the leakage inductance spike can potentially exceed the breakdown voltage of the internal power switch.

APPLICATIONS INFORMATION

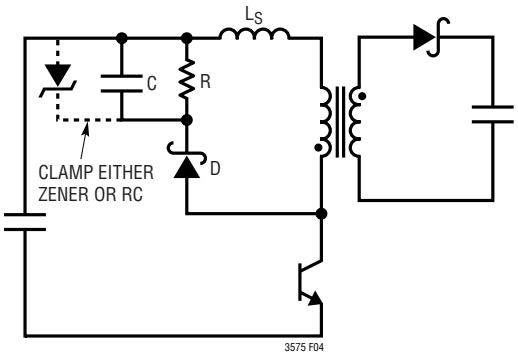


Figure 4. Snubber Clamping

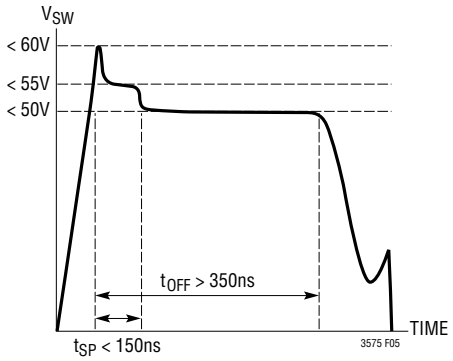


Figure 5. Maximum Voltages for SW Pin Flyback Waveform

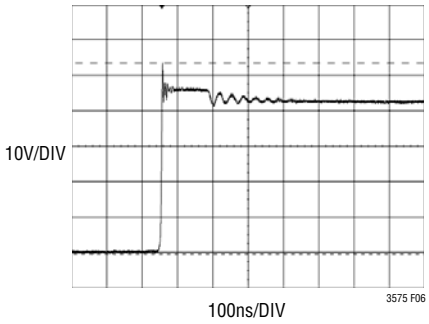


Figure 6. Good Snubber Diode Limits SW Pin Voltage

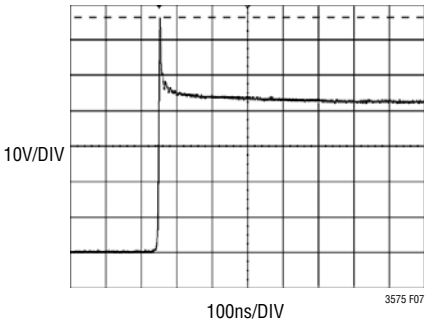


Figure 7. Bad Snubber Diode Does Not Limit SW Pin Voltage

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Secondary Leakage Inductance

In addition to the previously described effects of leakage inductance in general, leakage inductance on the secondary in particular exhibits an additional phenomenon. It forms an inductive divider on the transformer secondary that effectively reduces the size of the primary-referred flyback pulse used for feedback. This will increase the output voltage target by a similar percentage. Note that unlike leakage spike behavior, this phenomenon is load independent. To the extent that the secondary leakage inductance is a constant percentage of mutual inductance (over manufacturing variations), this can be accommodated by adjusting the R_{FB}/R_{REF} resistor ratio.

Winding Resistance Effects

Resistance in either the primary or secondary will reduce overall efficiency (P_{OUT}/P_{IN}). Good output voltage regulation will be maintained independent of winding resistance due to the boundary mode operation of the LT3575.

Bifilar Winding

A bifilar, or similar winding technique, is a good way to minimize troublesome leakage inductances. However, remember that this will also increase primary-to-secondary capacitance and limit the primary-to-secondary breakdown voltage, so, bifilar winding is not always practical. The Linear Technology applications group is available and extremely qualified to assist in the selection and/or design of the transformer.

Setting the Current Limit Resistor

The maximum current limit can be set by placing a resistor between the R_{ILIM} pin and ground. This provides some flexibility in picking standard off-the-shelf transformers that may be rated for less current than the LT3575's internal power switch current limit. If the maximum current limit is needed, use a 10k resistor. For lower current limits, the following equation sets the approximate current limit:

$$R_{ILIM} = 65 \bullet 10^3 (3.5A - I_{LIM}) + 10k$$

The Switch Current Limit vs R_{ILIM} plot in the Typical Performance Characteristics section depicts a more accurate current limit.

Undervoltage Lockout (UVLO)

The $\overline{SHDN}$/UVLO pin is connected to a resistive voltage divider connected to V_{IN} as shown in Figure 8. The voltage threshold on the $\overline{SHDN}$/UVLO pin for V_{IN} rising is 1.22V. To introduce hysteresis, the LT3575 draws 2.8µA from the $\overline{SHDN}$/UVLO pin when the pin is below 1.22V. The hysteresis is therefore user-adjustable and depends on the value of R1. The UVLO threshold for V_{IN} rising is:

$$V_{IN(UVLO,RISING)} = \frac{1.22V \bullet (R1 + R2)}{R2} + 2.8\mu A \bullet R1$$

The UVLO threshold for V_{IN} falling is:

$$V_{IN(UVLO,FALLING)} = \frac{1.22V \bullet (R1 + R2)}{R2}$$

To implement external run/stop control, connect a small NMOS to the UVLO pin, as shown in Figure 8. Turning the NMOS on grounds the UVLO pin and prevents the LT3575 from operating, and the part will draw less than a 1µA of quiescent current.

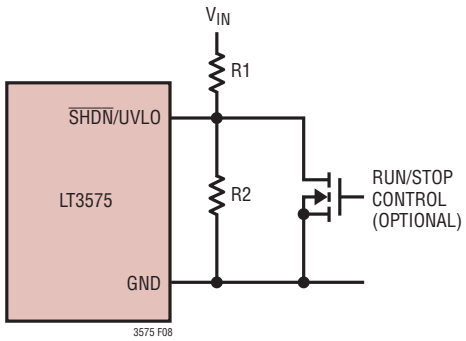


Figure 8. Undervoltage Lockout (UVLO)

APPLICATIONS INFORMATION

Minimum Load Requirement

The LT3575 obtains output voltage information through the transformer while the secondary winding is conducting current. During this time, the output voltage (multiplied times the turns ratio) is presented to the primary side of the transformer. The LT3575 uses this reflected signal to regulate the output voltage. This means that the LT3575 must turn on every so often to sample the output voltage, which delivers a small amount of energy to the output. This sampling places a minimum load requirement on the output of 1% to 2% of the maximum load.

A Zener diode with a Zener breakdown of 20% higher than the output voltage can serve as a minimum load if pre-loading is not acceptable. For a 5V output, use a 6V Zener with cathode connected to the output.

BIAS Pin Considerations

For applications with an input voltage less than 15V, the BIAS pin is typically connected directly to the V_{IN} pin. For input voltages greater than 15V, it is preferred to leave the BIAS pin separate from the V_{IN} pin. In this condition, the BIAS pin is regulated with an internal LDO to a voltage of 3V. By keeping the BIAS pin separate from the input voltage at high input voltages, the physical size of the capacitors can be minimized (the BIAS pin can then use a 6.3V or 10V rated capacitor).

Overdriving the BIAS Pin with a Third Winding

The LT3575 provides excellent output voltage regulation without the need for an optocoupler, or third winding, but for some applications with higher input voltages (>20V), it may be desirable to add an additional winding (often called a third winding) to improve the system efficiency. For proper operation of the LT3575, if a winding is used as a supply for the BIAS pin, ensure that the BIAS pin voltage is at least 3.15V and always less than the input voltage. For a typical 24V_{IN} application, overdriving the BIAS pin will improve the efficiency gain 4-5%.

Loop Compensation

The LT3575 is compensated using an external resistor-capacitor network on the V_C pin. Typical values are in the range of R_C = 50k and C_C = 1.5nF (see the numerous schematics in the Typical Applications section for other possible values). If too large of an R_C value is used, the part will be more susceptible to high frequency noise and jitter. If too small of an R_C value is used, the transient performance will suffer. The value choice for C_C is somewhat the inverse of the R_C choice: if too small a C_C value is used, the loop may be unstable, and if too large a C_C value is used, the transient performance will also suffer. Transient response plays an important role for any DC/DC converter.

Design Example

The following example illustrates the converter design process using LT3575.

Given the input voltage of 20V to 28V, the required output is 5V, 1A.

$V_{IN(MIN)}$ = 20V, $V_{IN(MAX)}$ = 28V, V_{OUT} = 5V, V_F = 0.5V and I_{OUT} = 1A

1. Select the transformer turns ratio to accommodate the output.

The output voltage is reflected to the primary side by a factor of turns ratio N. The switch voltage stress V_{SW} is expressed as:

$$N = \frac{N_P}{N_S}$$

$$V_{SW(MAX)} = V_{IN} + N(V_{OUT} + V_F) < 50V$$

Or rearranged to:

$$N < \frac{50 - V_{IN(MAX)}}{(V_{OUT} + V_F)}$$

On the other hand, the primary side current is multiplied by the same factor of N. The converter output capability is:

$$I_{OUT(MAX)} = 0.8 \bullet (1-D) \bullet \frac{1}{2} NI_{PK}$$

$$D = \frac{N(V_{OUT} + V_F)}{V_{IN} + N(V_{OUT} + V_F)}$$

APPLICATIONS INFORMATION

The transformer turns ratio is selected such that the converter has adequate current capability and a switch stress below 50V. Table 6 shows the switch voltage stress and output current capability at different transformer turns ratio.

Table 6. Switch Voltage Stress and Output Current Capability vs Turns-Ratio

N	$V_{SW(MAX)}$ AT $V_{IN(MAX)}$ (V)	$I_{OUT(MAX)}$ AT $V_{IN(MIN)}$ (A)	DUTY CYCLE (%)
1:1	33.5	1.26	16~22
2:1	39	2.07	28~35
3:1	44.5	2.63	37~45
4:1	50	3.05	44~52

BIAS winding turns ratio is selected to program the BIAS voltage to 3V~5V. The BIAS voltage shall not exceed the input voltage.

The turns ratio is then selected as primary: secondary: BIAS = 3:1:1.

2. Select the transformer primary inductance for target switching frequency.

The LT3575 requires a minimum amount of time to sample the output voltage during the off-time. This off-time, $t_{OFF(MIN)}$, shall be greater than 350ns over all operating conditions. The converter also has a minimum current limit, I_{MIN}, of 400mA to help create this off-time. This defines the minimum required inductance as defined as:

$$L_{MIN} = \frac{N(V_{OUT} + V_F)}{I_{MIN}} \bullet t_{OFF(MIN)}$$

The transformer primary inductance also affects the switching frequency which is related to the output ripple. If above the minimum inductance, the transformer's primary inductance may be selected for a target switching frequency range in order to minimize the output ripple.

The following equation estimates the switching frequency.

$$f_{SW} = \frac{1}{t_{ON} + t_{OFF}} = \frac{1}{\frac{I_{PK}}{V_{IN}/L} + \frac{I_{PK}}{N_{PS}(V_{OUT} + V_F)/L}}$$

Table 7.Switching Frequency at Different Primary Inductance at I_{PK}

L (µH)	f_{SW} AT $V_{IN(MIN)}$ (kHz)	f_{SW} AT $V_{IN(MAX)}$ (kHz)
15	174	205
30	87	103
60	44	51

Note: The switching frequency is calculated at maximum output.

In this design example, the minimum primary inductance is used to achieve a nominal switching frequency of 200kHz at full load. The 750311458 from Würth Elektronik is chosen as the flyback transformer.

Given the turns ratio and primary inductance, a customized transformer can be designed by magnetic component manufacturer or a multi-winding transformer such as a Coiltronics Versa-Pac may be used.

3. Select the output diodes and output capacitor.

The output diode voltage stress V_D is the summation of the output voltage and reflection of input voltage to the secondary side. The average diode current is the load current.

$$V_D = V_{OUT} + \frac{V_{IN}}{N}$$

The output capacitor should be chosen to minimize the output voltage ripple while considering the increase in size and cost of a larger capacitor. The following equation calculates the output voltage ripple.

$$\Delta V_{MAX} = \frac{L I^2_{PK}}{2 C V_{OUT}}$$

4. Select the snubber circuit to clamp the switch voltage spike.

A flyback converter generates a voltage spike during switch turn-off due to the leakage inductance of the transformer. In order to clamp the voltage spike below the maximum rating of the switch, a snubber circuit is used. There are many types of snubber circuits, for example R-C, R-C-D and

APPLICATIONS INFORMATION

Zener clamps. Among them, RCD is widely used. Figure 9 shows the RCD snubber in a flyback converter.

A typical switch node waveform is shown in Figure 10.

During switch turn-off, the energy stored in the leakage inductance is transferred to the snubber capacitor, and eventually dissipated in the snubber resistor.

$$\frac{1}{2} L_S I^2_{PK} f_{SW} = \frac{V_C (V_C - N \bullet V_{OUT})}{R}$$

The snubber resistor affects the spike amplitude V_C and duration t_{SP}, the snubber resistor is adjusted such that t_{SP} is about 150ns. Prolonged t_{SP} may cause distortion to the output voltage sensing.

The previous steps finish the flyback power stage design.

5. Select the feedback resistor for proper output voltage.

Using the resistor Tables 1-4, select the feedback resistor R_{FB}, and program the output voltage to 5V. Adjust the R_{TC} resistor for temperature compensation of the output voltage. R_{REF} is selected as 6.04k.

A small capacitor in parallel with R_{REF} filters out the noise during the voltage spike, however, the capacitor should limit to 10pF. A large capacitor causes distortion on voltage sensing.

6. Optimize the compensation network to improve the transient performance.

The transient performance is optimized by adjusting the compensation network. For best ripple performance, select a compensation capacitor not less than 1.5nF, and select a compensation resistor not greater than 50k.

7. Current limit resistor, soft-start capacitor and UVLO resistor divider

Use the current limit resistor R_{LIM} to lower the current limit if a compact transformer design is required. Soft-start capacitor helps during the start-up of the flyback converter . Select the UVLO resistor divider for intended input operation range. These equations are aforementioned.

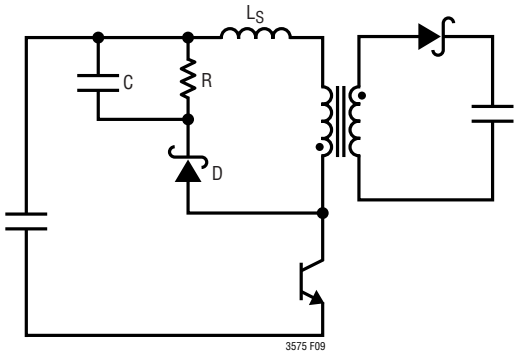


Figure 9. RCD Snubber in a Flyback Converter

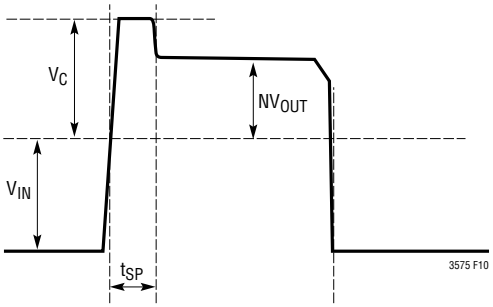
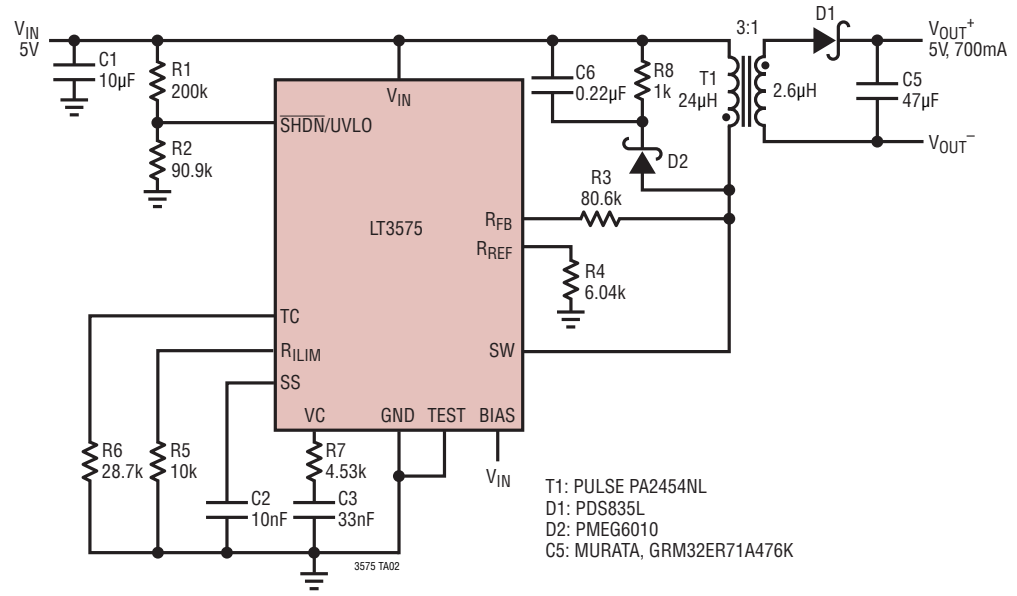


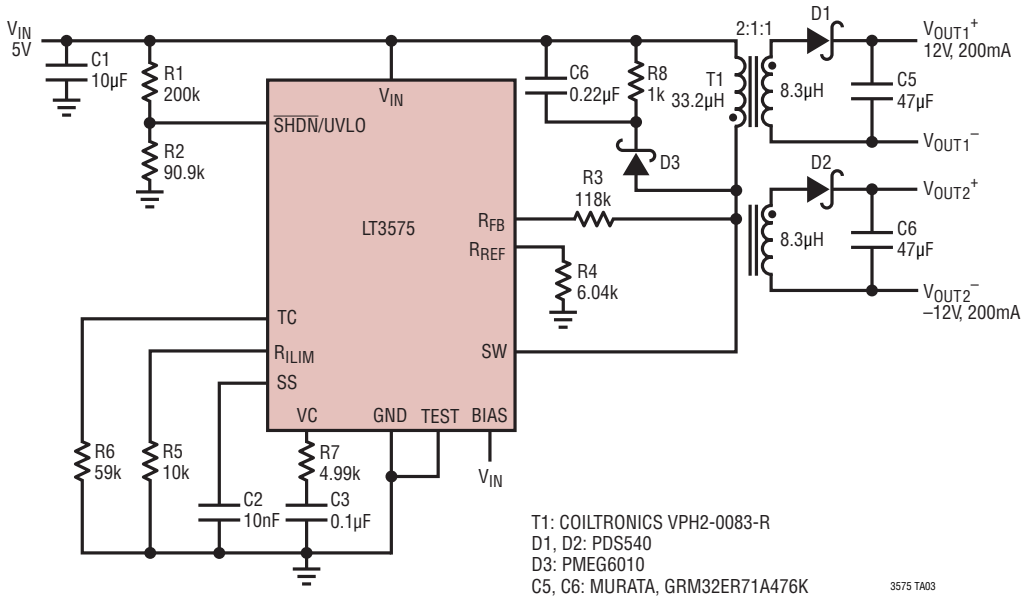
Figure 10. Typical Switch Node Waveform

TYPICAL APPLICATIONS

Low Input Voltage 5V Isolated Flyback Converter

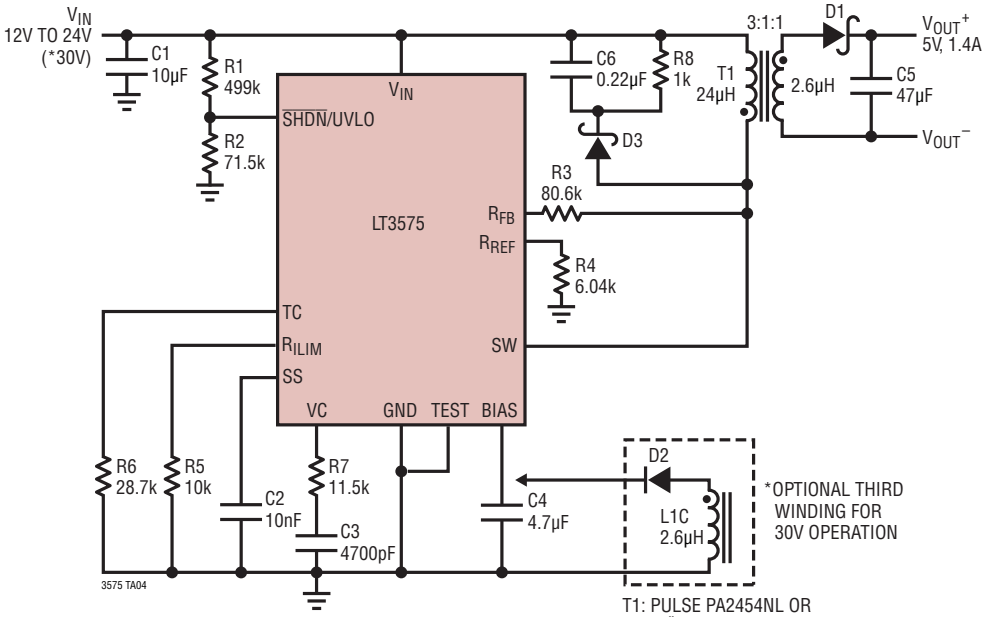


±12V Isolated Flyback Converter



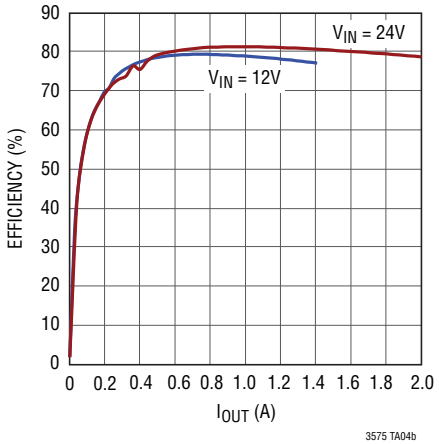
TYPICAL APPLICATIONS

5V Isolated Flyback Converter



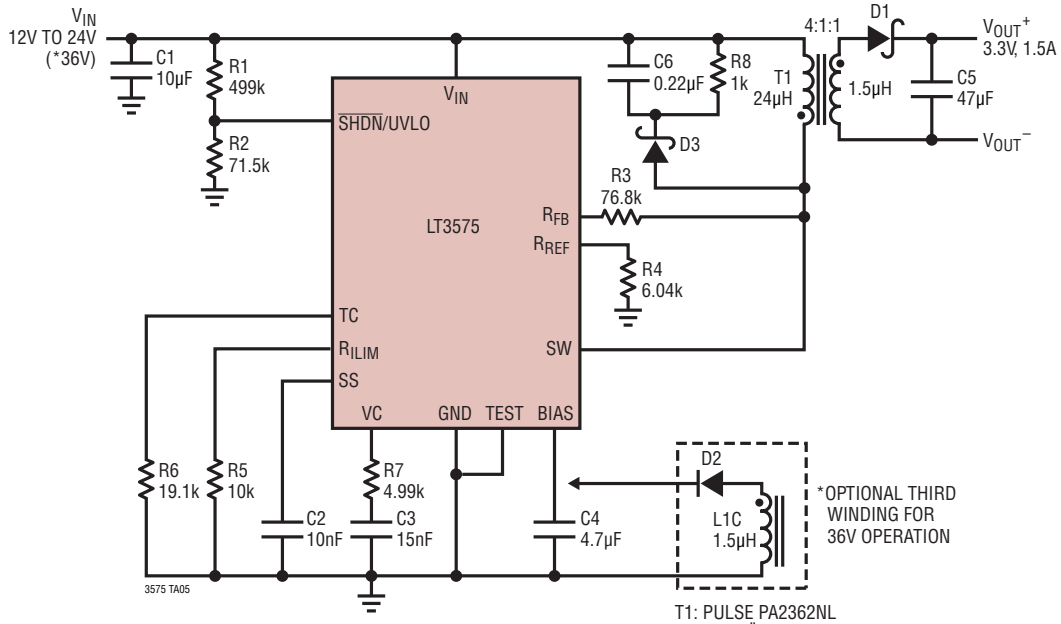
T1: PULSE PA2454NL OR
WÜRTH ELEKTRONIK 750310471/750311675
D1: PDS835L
D3: PMEG6010
C5: MURATA, GRM32ER71A476K

Efficiency



TYPICAL APPLICATIONS

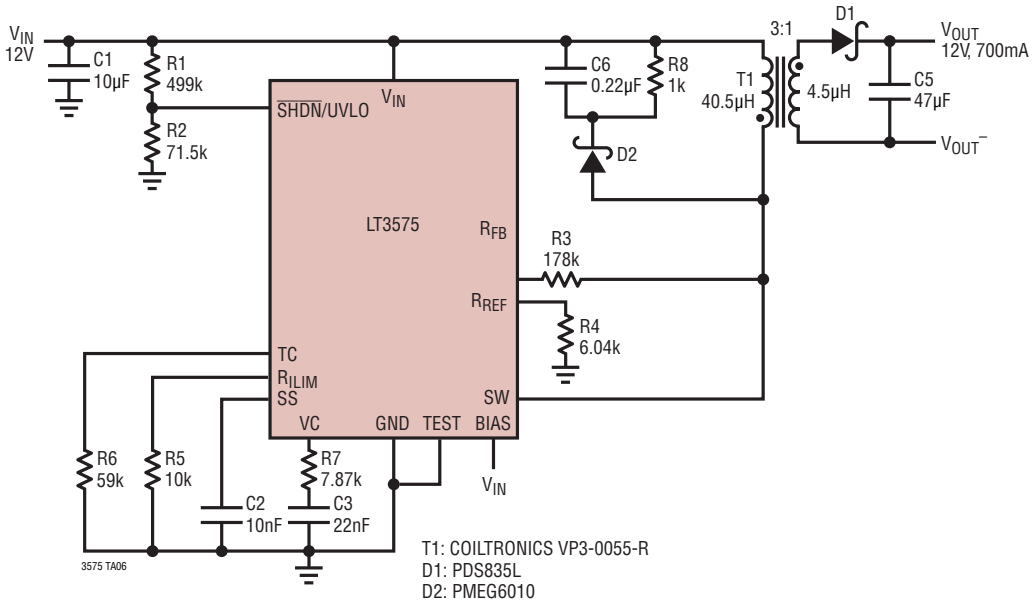
3.3V Isolated Flyback Converter



T1: PULSE PA2362NL
OR WÜRTH ELEKTRONIK 750310559
D1: PDS835L
D3: PMEG6010

TYPICAL APPLICATIONS

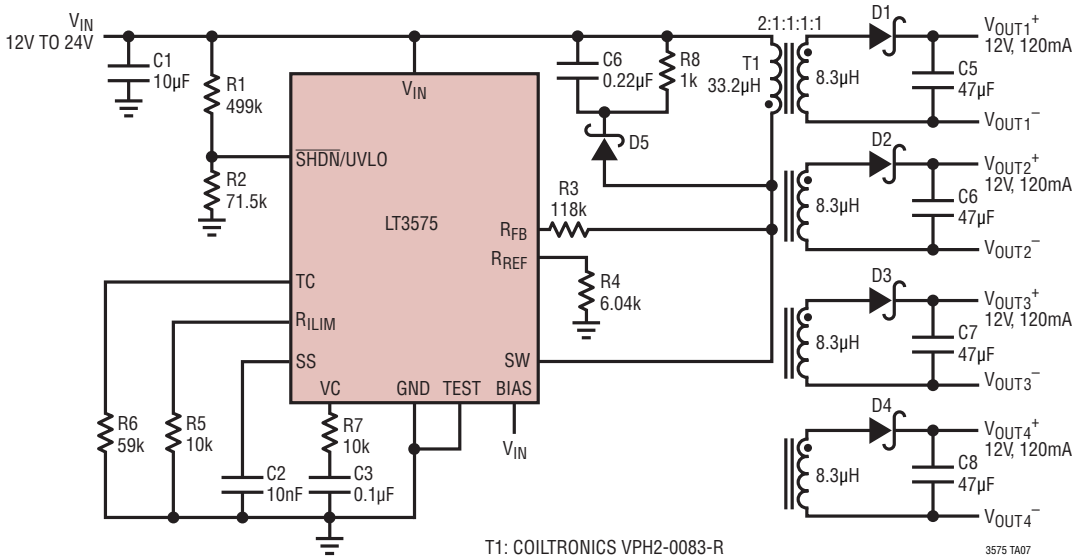
12V Isolated Flyback Converter



T1: COILTRONICS VP3-0055-R
D1: PDS835L
D2: PMEG6010

TYPICAL APPLICATIONS

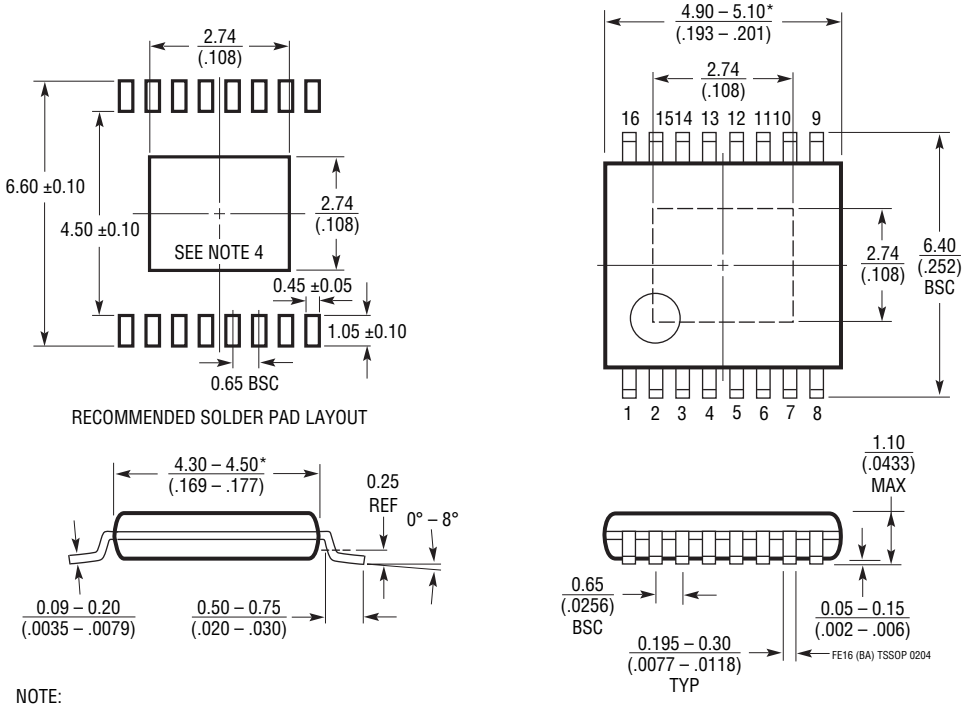
Four Output 12V Isolated Flyback Converter



T1: COILTRONICS VPH2-0083-R
D1-D4: PDS540
D5: PMEG6010

PACKAGE DESCRIPTION

FE Package
16-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)
Exposed Pad Variation BA



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE